Narrow Band Multi-Channel RF Transceiver Module

Product Description

The RC1240, RC1280 and RC1290 RF Transceiver Modules are compact surface-mounted high performance modules for 25 kHz narrow band FSK operation with embedded protocol. The modules are completely shielded and pre-certified for operation under the European and US radio regulations for license-free use. When used with quarter-wave antennas a line-of-sight range of 2-4 km can be achieved at 433 MHz.

Applications

- OEM equipment
- Radio modems
- · Alarm and security systems
- Point-of-sales terminals
- Bar code scanners
- Telemetry stations
- Fleet management



- Smallest in the world (12.7 x 25.4 x 3.5 mm)
- 25 kHz narrow band multi-channel operation
- Very low current consumption, 3nA OFF mode
- Embedded RC232™ protocol
- Addressing and Error check
- 128 byte data buffer
- Simple UART interface for easy RS232/422/485 wire replacement
- Compact shielded module for SMD mounting
- No external components
- No configuration required for single-channel use
- Easy to use data interface, 3/5 V tolerant I/O
- Wide supply voltage range, 2.8 5.5 V
- Conforms with EU R&TTE directive (EN 300 220, EN 301 489, EN 60950) for 25kHz
- Conforms with FCC CFR 47 part 15

Quick Reference Data

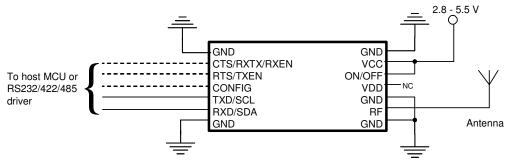
Parameter	RC1240	RC1280	RC1290	Unit
Frequency band	433.05-434.79	868 – 870	902 – 928	MHz
Number of channels	69	80	51	
Channel bandwidth	25	25	25-100	kHz
Data rate	4.8	4.8	1.2-19.2	kbit/s
Max output power	8	3	2*	dBm
Sensitivity	-115	-110	-110	dBm
Supply voltage		2.8 - 5.5		Volt
Current consumption, RX	20.2	20.7	20.7	mA
Current consumption, TX	26	28	22.9**	mA
Current consumption, SLEEP		mA		
Current consumption, OFF		0.003		uA

^{*} Programmable. Maximum allowed radiated power under FCC CFR 47, part 15 is -1 dBm ERP.



^{**} Apply for -1 dBm.

Typical Application Circuit



Quick Product Introduction

How do I transmit data?

Send your data to the RXD pin on the module. Use the UART format with settings (19200, 8, 1, N, no flow control), use 2 stop-bits if CTS is enabled. Up to 128 bytes are buffered in the module. The module will transmit the data when

- · the max packet length is reached
- · the unique end character is sent
- the modem timeout limit is reached

The packet length, end character and timeout limit are configurable in-circuit.

How do I receive data?

Any received data packet with correct address and check sum will be sent on the TXD pin using the same UART format as for transmit.

What about the antenna?

In most cases a simple quarter wavelength wire or a PCB track will do. Connect a piece of wire to the RF pin with length corresponding to the quarter of a wavelength. For space limited products, contact Radiocrafts and we will recommend the best antenna solution for your application.

How do I change the RF channel or any other parameter?

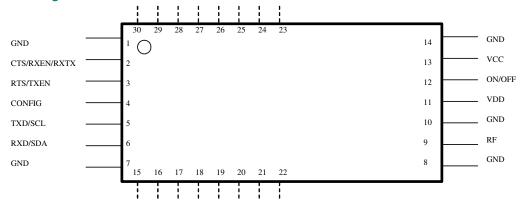
To change configurable parameters, assert the CONFIG pin, and send the command string using the same serial interface as for transmitting data. Parameters can be changed permanently and stored in non-volatile memory in the module.



Embedded Wireless Solutions

RC1240/1280/1290

Pin Assignment



Pin Description

Pin no	Pin name	Description	Equivalent circuit
1	GND	System ground	GND O
2	CTS/RXTX/RXEN	UART Clear to Send, UART RXTX, Receive Mode Enable, or SLEEP mode activation. Connect to VDD if not used. Internal 100 kΩ series resistor.	Input: VDD (2.7V)
3	RTS/TXEN	UART Request to Send, Transmit Mode Enable, or SLEEP mode activation. Connect to VDD if not used. Internal 100 kΩ series resistor.	
4	CONFIG	Configuration Enable. Active low. Should normally be set high. Connect to VDD if not used. Internal 100 k Ω series resistor.	VDD (2.7V) Output:
5	TXD/SCL	UART TX Data, or serial data clock. Internal 100 kΩ series resistor.	100k
6	RXD/SDA	UART RX Data, or serial data I/O. Internal 100 kΩ series resistor.	
7	GND	System ground	GND ♦——
8	GND	System ground	
9	RF	RF I/O connection to antenna	220p RF 0————————————————————————————————————



10	GND	System ground	GND O
		g. come	
			-
11	VDD	Supply voltage output, regulated. Should normally be left open	VREG 2u2
12	ON/OFF	Module on/off (shutdown). ON when high, OFF when low. For threshold see Electrical Specifications. Or connect to VCC. See important note under Power Management page 7.	ON/OFF 0
13	VCC	Supply voltage input. Internally regulated. Maximum rise-time requirement apply, see Electrical Specification.	VCC 0 2.7 V VREG 202 =
14	GND	System ground	GND O
			<u> </u>
15-21	RESERVED	Test pins or pins reserved for future use. <i>Do not connect!</i>	
22	RESET	Main reset (active low). Should normally be left open. Internal $100 \text{ k}\Omega$ pull-up resistor, no series resistor.	VDD (2.7V)
23	PA_EN	External PA enable output, active high	VDD (2.7V)
24	LNA_EN	External LNA enable output, active high	
25-30	RESERVED	Test pins or pins reserved for future use. <i>Do not connect!</i>	

Note 1: In UART mode the TXD and RXD are used for serial data, and CTS/RXTX and RTS for flow control (optional). If flow control is not used, and RXEN and TXEN are both asserted (active low) the module is set in SLEEP mode. RXEN and TXEN should be connected to VDD if not used for SLEEP mode activation. A pull-up resistor is not necessary due to an internal series resistor.

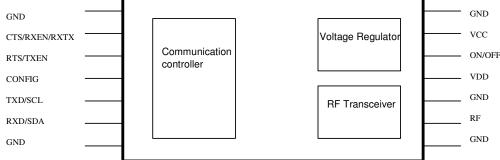


Note 2: In synchronous mode the SCL (data clock) and SDA (Data input and output) are used for serial data. The RXEN and TXEN pins are then used to select the operation mode of the device. Signals are active low. Note 3: The CONFIG pin is used to enter configuration mode (change of default settings). Active low. Note 4: Do not use VDD for supply to external circuits. Should only be used for pull-ups, if required. Note 5: RXEN, TXEN, CONFIG, TXD and RXD have internal 100 k Ω series resistors. Driving capability when used as outputs is therefore limited and should be connected to CMOS inputs only.

Note 6: Other digital interfaces may be specified upon request.



Block Diagram



Circuit Description

The module contains a communication controller with embedded RC232™ protocol software, a narrow band high performance RF transceiver and an internal voltage regulator.

The communication controller handles the radio packet protocol, the UART interface and controls the RF transceiver. Data to be sent by the host is received at the RXD pin and buffered in the communication controller. The data packet is then assembled with preamble, start-of-frame delimited (SOF), address information and CRC check sum before it is transmitted on RF. The preamble and SOF is always used. The address and CRC are optional.

The RF transceiver modulates the data to be transmitted on RF frequency, and demodulates data that are received. Narrow band technology is used to enhance sensitivity and selectivity.

Received data are checked for correct address and CRC by the communication controller. If the address matches the modules own address, and no CRC errors were detected, the data packet is sent to the host on the TXD line after removing the header.

The asynchronous UART interface consists of RXD and TXD. Optionally CTS, RTS/RXTX can be used for hardware handshake flow control. RTS/RXTX can be used to control the direction of an RS485 driver circuit.

The module can also be used in an un-buffered transparent mode. In this case the data interface is synchronous using SCL and SDA for data transfer to/from the host. The RXEN and TXEN are then used to set the operational mode.

When the CONFIG pin is asserted the communication controller interprets data received on the RXD pin as configuration commands. There are commands to change the radio channel, the output power, the destination address etc. Permanent changes of the configuration is also possible and are then stored in internal non-volatile memory (EEPROM).

The RF protocol and the configuration commands are described in detail in the RC232™ User Manual.

The supply voltage is connected to the VCC pin. The module contains an internal voltage regulator and can therefore operate over a wide supply voltage range. The regulated voltage is available at the VDD pin, but should not be used to supply external circuits.

The ON/OFF pin can be used to turn the module completely off, and hence reduce the power consumption to a minimum. For normal operation the ON/OFF pin must be connected to VCC. To turn the module completely off, connect the ON/OFF pin to ground (logic low level).



RC232™ Embedded Protocol

The module offers a buffered packet radio as well as an un-buffered transparent mode in the RC232™ embedded protocol.

Using the buffered packet radio mode, all data to be sent is stored in the module before they are transmitted by the RF circuitry. Likewise, when data is received they are stored in the module before they are sent to the host. This allows the communication controller to add address information and to do error check of the data. In buffered mode the UART interface is used to communicate with the host.

If the application requires a transparent data link, the module can be configured to operate in an un-buffered mode. In this mode the module adds only a preamble and start-of-frame bytes to synchronize the receiver. No addressing or checksum is provided in this case. A synchronous interface is used to transfer data to/from the host. Note however, that the configuration of the module is done using the UART even if the un-buffered mode is used for data transfer.

The embedded protocol, configuration commands and configuration memory is described in the RC232TM User Manual. This protocol is used in a wide range of RF modules available from Radiocrafts. Please refer to the latest revision available on Radiocrafts web-site.

Power Management

The module can be set in SLEEP mode or OFF mode in order to reduce the power consumption.

The low power SLEEP mode is entered by using the SLEEP command, see RC232™ User Manual, or by pulling both RXEN and TXEN low. In sleep mode the module will not receive or detect incoming data, neither from the host (UART port) nor from the RF transceiver. The module is awakened from the SLEEP mode by a positive edge on the CONFIG, RXEN or TXEN pins if the module was set in SLEEP mode using the 'Z' command. The module is awakened by a positive edge on the RXEN or TXEN pin if these two pins were used to enter SLEEP mode. CONFIG must be high when awakening the module to avoid setting the module directly in configuration mode.

Note: If UART handshake is used, the RXEN and TXEN pins can not be used to enter SLEEP mode. In this case, use the SLEEP command.

The ultra-low power OFF mode is entered by pulling the ON/OFF pin low. The module will then shut down completely. The module is turned on by setting the ON/OFF pin high (to VCC). After the module has been in OFF mode all operational parameters are set to the values stored in configuration memory.

The VDD output should not be used to supply external circuits, other than for pull-ups for RXEN, TXEN and CONFIG.



Power on Reset

In order to ensure that the internal Power on Reset (POR) operates correctly, the maximum rise-time specification for VCC must be met (see Electrical Specifications). Longer VCC rise-time or short supply voltage interrupts may cause improper operation that is not handled by the internal POR. For proper operation it is crucial to use an external control of the RESET pin as described below (see also Application Note AN001).

When turning the module OFF by setting ON/OFF low, or switching VCC off, great care should be taken to ensure proper power-on-reset (POR). I/O pins driving the module when the module is off can give a low residual voltage in the module that prevents trigging of the internal POR. Also in this case an external RESET signal is required to ensure proper startup.

The figures below shows suggested circuits for RESET control. The MCU can operate over the whole VCC operation range. But do note that the module TXD output operates at 2.7 V, and hence the host MCU must accept this lower voltage swing. If not, a voltage translator must be used, see section 'I/O pin Interfaces' page 11). The suggested solutions are:

- Control the RESET pin by a separate I/O pin from the MCU using a 10 kOhm series resistor (RESET does not have any internal serial resistor, but a 100k pull-up to VDD). Set RESET low before ON/OFF is turned low, and keep low until ON/OFF is high again (VCC 10%). This will ensure proper power-on reset (POR). See Figure 1 below.
- Control the RESET pin by the same I/O in used to control ON/FF. A 10 kOhm series
 resistor is used for the RESET pin to limit the input current from the 3 / 5V signal from
 the MCU. See Figure 2 below.
- Use an external POR and brown-out supervisory circuit. The circuit should be connected between VDD and GND, controlling RESET. This solution will force RESET low as long as VDD is below the threshold voltage. The RESET has an internal pull-up resistor to VDD, thus an open-drain output supervisory circuit can be used. A threshold voltage between 2.3 and 2.6 V is recommended. See Figure 3. Supervisory circuits are suggested below.
- If the host system already has an external POR and brown-out supervisory circuit, this can also be used to control the module RESET. The supervisory circuit should be connected between VCC (or the MCU supply voltage if different) and GND, controlling RESET through a 10k resistor. This solution will force RESET low as long as VCC is below the threshold voltage. The RESET has an internal pull-up resistor to VDD, thus an open-drain output supervisory circuit can be used. A threshold voltage of 2.8 V or higher is recommended. See Figure 4. Supervisory circuits are suggested below.



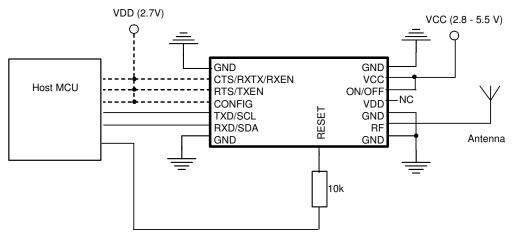


Figure 1. Reset circuit using host MCU

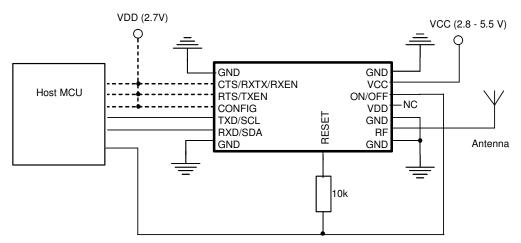


Figure 2. Reset circuit controlling ON/OFF



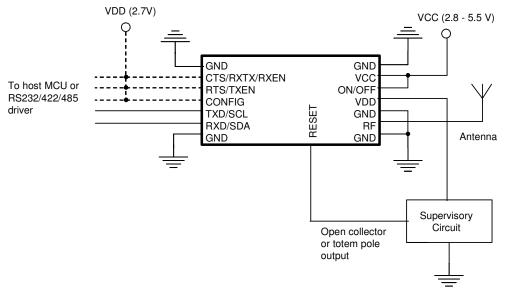


Figure 3. Reset circuit using supervisory circuit on VDD

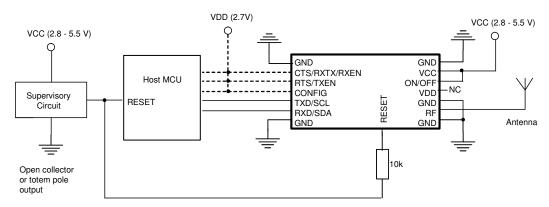


Figure 4. Reset circuit using supervisory circuit on VCC

As a reference, potential suppliers of supervisory circuits are provided below. Radiocrafts does not endorse any specific vendor. In most cases, similar components from other suppliers will provide satisfactory performance. A threshold voltage of $2.3-2.6\ V$ is recommended if the supervisory circuit is connected to VDD.

Manufactur er	Model number	Delay [ms]	Nominal trigger volt.	Max trigger volt.	Output	Package	Distributor
Microchip	MCP100- 270	150- 700	2.62	2.70	Push-pull	SOT-23/3 & TO92	Future, Digi-Key
Microchip	TC1275- 20ENB	100- 300	2.55	2.64	ry 100k pull down for RST=0V	SOT-23B/3	Future, Digi-Key
Maxim	MAX803R/	140-	2.63	2.70	Open-drain/	SOT-23/3	Maxim direct



	MAX809R	460			push-pull	SC-70/3	
Maxim	MAX6328_ R25-T	100- 280	2.50	2.562	Open drain, external pull-	SOT-23/3 SC-70/3	Maxim direct
					up resistor		
Analog	ADM809_	140-	2.32	2.38	Push-pull	SOT-23/3	Arrow
Devices	Z	460				SC-70/3	
Texas	TPS3800G	60-	2.5	2.55	Push-pull	SC-70/5	Avnet,
Instruments	27	140					Digi-Key
Texas	TPS3809J	120-	2.25	2.30	Push-pull	SOT-23/3	Avnet,
Instruments	25	280					Digi-Key
Texas	TPS3836J	5-15	2.25	2.29	Push-pull	SOT-23/5	Avnet,
Instruments	25						Digi-Key
Sipex	SP810EK-	100-	2.3	2.346	Push-pull	SOT-23/3	Future,
	2-3	1030					Newark
National	LM3722E	100-	2.32	2.37	Push-pull	SOT-23/5	Future
Semiconduc	M5-2.32	560					
tor							

I/O pin Interfaces

As noted in the Pin Description, RXEN (CTS/RXTX), TXEN (RTS) and CONFIG pins should have their pull-ups connected to VDD, not VCC. If RXEN is used as CTS (hardware handshake) or as RXTX (RS485) output, no pull-up is required and should be avoided as this reduces the voltage swing due to the internal resistor.

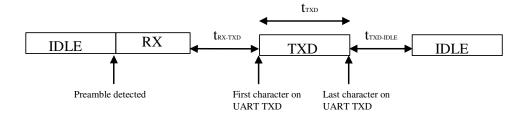
Important note: The RXEN (CTS/RXTX) and TXD (SCL) and SDA pins are logic signals with 0 – VDD voltage swing, where VDD is 2.7 V. When connecting these signals to external circuitry operating on supply voltage above 2.7 V, a level translator may be required. Single transistor buffers or integrated level translators can be used for this purpose. An example of such a level translator is SN74LVC1t45.

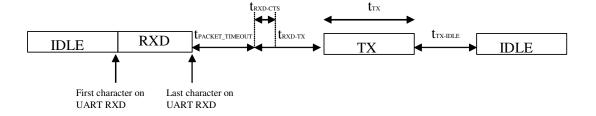
Timing Information

The figure and table below shows the timing information for the module when changing between different operating states.

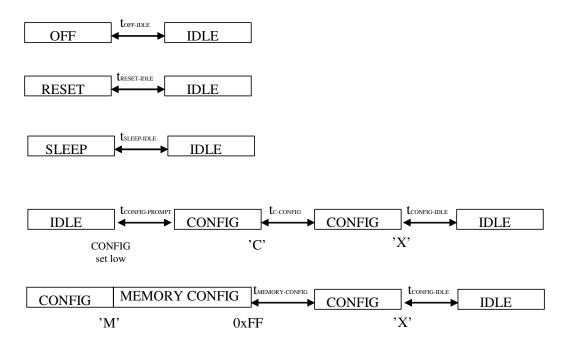
The IDLE state is the normal state where the module search for preamble on the air and wait for a character to be received on the UART. RXD is the state when receiving characters from the host filling up the internal buffer. TX state is when the data is transmitted on the air. RX state is when data is received from the air after preamble detection. TXD is the state where the received data is sent to the host on the UART.

CONFIG is the state entered by asserting the CONFIG pin and used during parameter configuration, while MEMORY CONFIG is the sub-state entered by the 'M' command where the configuration memory is being programmed. Note the limitation on maximum number of write cycles using the 'M' command, see Electrical Specifications.









Symbol	Value	Description / Note
t _{RX-TXD}	500 us	Time from last byte is received from the air until first character is sent
		on the UART
t _{TXD}	Min 621 us	t _{TXD} = # bytes received x 621 us/char (10 bits at 19.2 kBd + 100 us
		delay per character)
t _{TXD-IDLE}	5 ms	Time from last character is sent on the UART until module is in IDLE
		mode (ready for RXD and RX)
t _{PACKET} -	Programmable	If enabled, the packet timeout can be configured from 32 ms to 4.08
TIMEOUT		s. If end character or fixed packet length is used, the timeout is 0.
T _{RXD-CTS}	25 us	Time from last character is received by the UART (including any
		timeout) until CTS is activated
t _{RXD-TX}	1.3 ms	Time from last character is received by the UART (including any
_	_	timeout) until the module sends the first byte on the air.
T _{TX-IDLE}	5 ms	Time from last character is sent on the air until module is in IDLE
	100	mode (ready for RXD and RX)
t _{OFF-IDLE}	160 ms	
t _{RESET-IDLE}	160 ms	
t _{SLEEP-IDLE}	55 ms	T' (OONEIO ' ' II II III II II III III III III I
t _{CONFIG-}	1.7 ms	Time from CONFIG pin is set low until prompt (">")
PROMPT	10	Deleveration above allocate is constructed assessed (6.2). (For other
t _{C#-CONFIG}	43 ms	Delay after channel-byte is sent until prompt (">"). (For other
	CC ma	commands like 'M', 'T' there is no delay but immediate prompt)
t _{MEMORY}	66 ms	In this period the internal flash is programmed. <i>Do not reset, turn the</i>
CONFIG		module off, or allow any power supply dips in this period as it may cause permanent error in the Flash configuration memory. After 0xFF
		the host should wait for the '>' prompt before any further action is
		done to ensure correct re-configuration.
T _{CONFIG} -	5 ms	dono to onoure correct to corrigaration.
IDLE	0 1110	
t _{TX}	Min 21.7 ms	t _{TX} = # bytes to send x 1.67 ms/byte (at 4.8 kbit/s). Add 13 overhead
-17		bytes if addressing and CRC is not used. Add additionally 2 extra



bytes for addressing and 2 extra bytes for CRC if enabled.

Note also that in IDLE mode every 13.6 seconds the module recalibrates its internal UART clock reference in order to compensate for temperature drift. The recalibration takes approximately 5 ms. There is no recalibration in CONFIG mode, therefore the module should not be left in CONFIG mode for an extended time if the temperature is likely to change by more than +/- 5 degrees.

RF Frequency, Output Power Levels and Data Rates

The following table shows the available RF channels and their corresponding frequencies, nominal output power levels and available data rates.

Model	RF channel	Output power	Data rate
RC1240	1-69:	1: -14 dBm	4.8 kbit/s fixed
		2: -6 dBm	
	f _{RF} =433.0775+(N-1)*0.025 MHz	3: 0 dBm	
	where N is the channel number	4: 5 dBm	
		5: 8 dBm	
	Factory setting: 54: 434.4025 MHz		
RC1280	1-80:	1: -15 dBm	4.8 kbit/s fixed
		2: -10 dBm	
	f _{RF} =868.0125+(N-1)*0.025 MHz	3: -5 dBm	
	where N is the channel number	4: 0 dBm	
		5: 3 dBm	
	Factory setting: 41: 869.0125 MHz		
RC1290	1-51:	1: -15 dBm	1: NA
		2: -10 dBm	2: NA
	f _{RF} =902.5+(N-1)*0.5 MHz	3: -5 dBm	3: 4.8 kbit/s
	where N is the channel number	4: -1 dBm	4: 9.6 kbit/s
	(except channel 47: 925.6 MHz)	5: 2 dBm	5: 19.2 kbit/s
	Factory setting: 26: 915.0000 MHz		

RF channel and output power level can be set using the configuration commands 'C' and 'P' respectively. The data rate can *only* be changed in configuration memory by using the 'M' command setting RF_DATA_RATE. The *default* RF channel and output power level can be set in the configuration memory by using the 'M' command setting RF_CHANNEL and RF_POWER. The default values are used after power ON and RESET. The default factory settings are shown in **bold** in the table above.

For more details on changing the RF channel, output power or data rate, refer to the RC232[™] User Manual describing the configuration commands.

The use of RF frequencies and maximum allowed RF power is limited by national regulations. The RC1240 and RC1280 are complying with the applicable directives within the European Union. The RC1290 is pending approval under FCC for use in the US and Canada. For more information see section *Regulatory Compliance Information* page 21.

External PA and LNA control

Pin 23 and 24 can be used to control an external Power Amplifier (PA), external Low Noise Amplifier (LNA) and Transmit/Receive (T/R) switch. The control signals are active high logic level (VDD) digital outputs. The PA_EN signal is active while the internal PA is on, while LNA_EN is active when the internal LNA is on. The PA is on during transmit mode, the LNA is on during receive mode and idle mode.

RSSI Reading

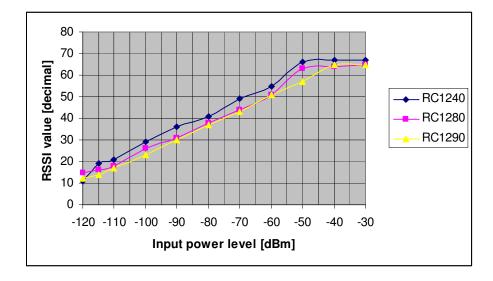
The module provide a digital Received Signal Strength Indicator (RSSI) through the 'S' command. The module returns an 8 bit character (one byte) indicating the current input signal strength (followed immediately by a second character which is the prompt ('>')). The signal strength can be used as an indication of fading margin, or as a carrier sense signal to avoid collisions.

Do note that if the signal strength for an incoming packet is to be measured, the 'S' command must be performed while the packet is being received. To simplify the test of a link, and avoid timing problems, the transmitter can be set to continuous transmission using the '2' test command, while the receiver use the 'S' command to read the signal strength.

The RSSI value increases with increased input signal strength. Input signal strength is given by (typ.):

 $P = 1.5 \times RSSI - 144 \text{ [dBm] for RC1240}$ $P = 1.5 \times RSSI - 137 \text{ [dBm] for RC1280}$ $P = 1.5 \times RSSI - 138 \text{ [dBm] for RC1290}$

Typical RSSI value as a function of input signal strength is shown in the figure below.





Antenna Connection

The antenna should be connected to the RF pin. The RF pin is matched to 50 Ohm. If the antenna connector is placed away from the module at the motherboard, the track between the RF pin and the connector should be a 50 Ohm transmission line.

On a two layer board made of FR4 the width of a microstrip transmission line should be 1.8 times the thickness of the board, assuming a dielectric constant of 4.8. The line should be run at the top of the board, and the bottom side should be a ground plane.

Example: For a 1.6 mm thick FR4 board, the width of the trace on the top side should be 1.8 x 1.6 mm = 2.88 mm.

The simplest antenna to use is the quarter wave whip antenna. A quarter wave whip antenna above a ground plane yields 37 Ohm impedance and a matching circuit for 50 Ohm are usually not required.

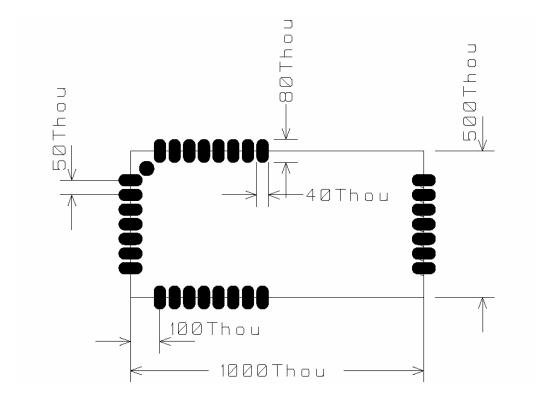
A PCB antenna can be made as a copper track where the ground plane is removed on the back side. The rest of the PCB board should have a ground plane as large as possible, preferably as large as the antenna itself, to make it act as a counterweight to the antenna. If the track is shorter than a quarter of a wavelength, the antenna should be matched to 50 ohms.

The lengths of a quarter wave antenna for different operational frequencies are given in the table below.

Frequency [MHz]	Length [cm]
433	16.4
868	8.2
915	7.8

PCB Layout Recommendations

The recommended layout pads for the module are shown in the figure below. All dimensions are in thousands of an inch (mil). The circle in upper left corner is an orientation mark only, and should not be a part of the copper pattern.

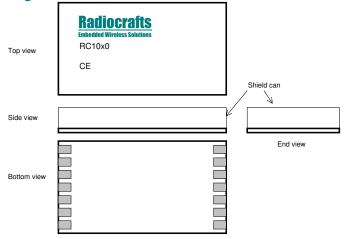


A PCB with two or more layers and with a solid ground plane in one of the inner- or bottom layer(s) is recommended. All GND-pins of the module shall be connected to this ground plane with vias with shortest possible routing, one via per GND-pin.

On the back side of the module there are several test pads. These test pads shall not be connected, and the area underneath the module should be covered with solder resist. If any routing or vias is required under the module, the routing and vias must be covered with solder resist to prevent short circuiting of the test pads. It is recommended that vias are tented.

Reserved pins should be soldered to the pads but the pads must be left floating.

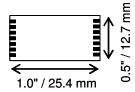
Mechanical Drawing



Drawings are not to scale

Mechanical Dimensions

The module size is 12.7 x 25.4 x 3.5 mm.



Carrier Tape and Reel Specification

Carrier tape and reel is in accordance with EIA Specification 481.

Tape width	Component pitch	Hole pitch	Reel diameter	Units per reel
44 mm	16 mm	4 mm	13"	Max 1000

Soldering Profile Recommendation

JEDEC standard IEC/JEDEC J-STD-020B (page 11 and 12), Pb-Free Assembly is recommended.

The standard requires that the heat dissipated in the "surroundings" on the PCB is taken into account. The peak temperature should be adjusted so that it is within the window specified in the standard for the actual motherboard.



Embedded Wireless Solutions

RC1240/1280/1290

Absolute Maximum Ratings

Parameter	Min	Max	Unit
Supply voltage, VCC	-0.3	5.5	V
Voltage on any pin	-0.3	5.5	V
Input RF level		10	dBm
Storage temperature	-50	150	°C
Operating temperature	-20	55	°C



Caution! ESD sensitive device. Precaution should be used when handling the device in order to prevent permanent damage.

Under no circumstances the absolute maximum ratings given above should be violated. Stress exceeding one or more of the limiting values may cause permanent damage to the device.

Electrical Specifications

T=25°C, VCC = 3.0V if nothing else stated.

Parameter	Min	Тур.	Max	Unit	Condition / Note
		Typ.	IVICIA	Ont	Condition / Note
Operating frequency					
RC1240	433.050		434.790	MHz	
RC1280	868.0		870.0		
RC1290	902		928		
NC1290	902		920		
Number of channels					
RC1240		69			
RC1280		80			
RC1290		51			
NC1290		51			
Channel spacing		25		kHz	
Channel spacing		25		KHZ	
1 1/ 1 1		50		01	
Input/output impedance		50		Ohm	
B		4.0	10.0*	1.1.217	*B04000 I
Data rate		4.8	19.2*	kbit/s	*RC1290 only
			/ 0 =		
Frequency stability			+/-2.5	ppm	
Transmit power					Typical values are for default
RC1240	-20	6	8	dBm	settings
RC1280	-20	3	3	_	3-
RC1290	-20	-1	2		
NC1290	-20	-1	2		
FOX deviction		+/- 2.4	+/- 9.6*	1-11-	*D04000
FSK deviation		+/- 2.4	+/- 9.6"	kHz	*RC1290 only
Adjacent channel power		-55	-45	dBc	
Occupied bandwidth		14	16	kHz	99.5%
Spurious emission, TX					
RC1240/RC1280					
< 1 GHz			-37	dBm	
				иын	
➤ 1 GHz			-30		
RC1290					
< 960 MHz			-49		
> 960 MHz			-41		
900 1011 12			-41		
Sensitivity					
	1	115		٠ الم	
RC1240	1	-115		dBm	
RC1280	1	-110			
RC1290, 4.8 kbit/s	1	-110			
RC1290, 9.6 kbit/s	1	-108			
	İ				
RC1290, 19.2 kbit/s		-106			
Adia a ant alsa ann a l	 	20		٩D	
Adjacent channel rejection	1	30		dB	
Alternate channel calcativity		40		dB	
Alternate channel selectivity		40		uв	
Image channel rejection		40		dB	
Image channel rejection	1	40		uв	



Blocking / Interferer rejection / desensitization +/- 1 MHz +/- 2 MHz +/- 5 MHz +/- 10 MHz	40 40 50 60	60 60 70 75		dB	Wanted signal 3 dB above sensitivity level, CW interferer. Minimum numbers corresponds to class 2 receiver requirements in EN300220.
Saturation		10		dBm	
Input IP3		-18		dBm	
Spurious emission, RX RC1240/RC1280 RC1290			-57 -49	dBm	
Supply voltage	2.8		5.5	V	
Supply voltage rise time			150	us	If appropriate rise time can not be guaranteed, the RESET pin should be activated after supply voltage is stable.
Current consumption, RX/IDLE RC1240 RC1280 RC1290		20.2 20.7 20.7		mA	Apply over entire supply voltage range
Current consumption, TX RC1240, 6 dBm RC1280, 3 dBm RC1290, -1 dBm		26 28 22.9		mA	Apply over entire supply voltage range
Current consumption, SLEEP		0.9	1.5	mA	Max value in bold apply over the entire temperature and supply voltage range
Current consumption, OFF		0.003	1.5	μА	Max value in bold apply over the entire temperature and supply voltage range
Digital I/O Input logic level, low Input logic level, high Output logic level, low (1μA) Output logic level, high(-1μA)	1.7 0 2.6		0.7 5.5 0.1 2.7	V	RXEN, TXEN, CONFIG, TXD and RXD have internal 100 k Ω series resistors. No internal pull-ups. Outputs should not be loaded resistively.
RESET pin Input logic level, low Input logic level, high	1.7		0.7 2.7	V	Internal 100 k Ω pull-up resistor to VDD
ON/OFF pin Input logic level, low Input logic level, high	1.4		0.4 VCC	V	No internal pull-up resistor
UART Baud Rate tolerance		+/- 2		%	UART receiver and transmitter
Configuration memory write cycles	10 000	100 000			The guaranteed number of write cycles using the 'M' command is limited



Regulatory Compliance Information

The use of RF frequencies and maximum allowed RF power is limited by national regulations. The RC1240 and RC1280 have been designed to comply with the R&TTE directive 1999/5/EC.

According to R&TTE directives, it is the responsibility of Radiocrafts' customers (i.e. RC12x0 end user) to check that the host product (i.e. final product) is compliant with R&TTE essential requirements. The use of a CE marked radio module can avoid re-certification of the final product, provided that the end user respects the recommendations established by Radiocrafts. A Declaration of Conformity is available from Radiocrafts on request.

The RC1290 has been tested towards FCC regulations for license free operation under part 15. However, a final approval is required by FCC for the end product.

The relevant regulations are subject to change. Radiocrafts AS do not take responsibility for the validity and accuracy of the understanding of the regulations referred above. Radiocrafts only guarantee that this product meets the specifications in this document. Radiocrafts is exempt from any responsibilities related to regulatory compliance.



Document Revision History

Document Revision	Changes		
1.0	First release		
1.1	Data buffer length changed from 200 to 145 RC1240: Number of channels increased from 30 to 69 Sleep current typo corrected from 85 uA to 0.9 mA on first page Active polarity and RESET added in pin description		
1.2	Data buffer length changed from 145 to 128 Added more information in the Pin description Added PCB layout recommendation Added carrier tape and reel specification Digital I/O specifications added in Electrical Specifications Updated Electrical Specifications Added timing information Added RSSI data Minor corrections for clarity		
1.3	Timing information changed according to latest firmware upgrade (rev 1.16 and later) Minor spelling errors corrected, clarifications added Emphasized that some digital I/Os have 100 kOhm series resistors Note on VCC rise-time in the Power Management section Pin description for PA_EN and LNA_EN added New section on external PA and LNA control added Spurious emission in TX corrected in Electrical Specifications Added more information on power-on-reset when using ON/OFF		
1.4	Power Management: Corrected reset signal series resistor value from 100kOhm to 10kOhm Timing Information: Added a note on periodic recalibration of UART time base		
1.5	Added timing info on Config pin low to prompt Updated product status to Full Production		
1.61	Added pin description equivalent circuits Added UART baud rate tolerance specification Added soldering profile recommendation Added note on 2 stop-bits if CTS is used Added note on RSSI measurement is followed by a new prompt Added note on delay after channel-byte in timing information Added configuration memory write cycle specification, and note in the text Added new section and more information on Power on Reset and reset circuits Added new section and more information on I/O pin interfaces Added new section and more information on low pin interfaces Added note on digital signal output level and level translators Added new section on regulatory compliance information Clarified awakening from SLEEP mode using RXEN and TXEN Clarified Product Status and Definition Clarified layout recommendations		



Product Status and Definitions

Current Status	Data Sheet Identification	Product Status	Definition
	Advance Information	Planned or under development	This data sheet contains the design specifications for product development. Specifications may change in any manner without notice.
	Preliminary	Engineering Samples and First Production	This data sheet contains preliminary data, and supplementary data will be published at a later date. Radiocrafts reserves the right to make changes at any time without notice in order to improve design and supply the best possible product.
X	No Identification Noted	Full Production	This data sheet contains final specifications. Radiocrafts reserves the right to make changes at any time without notice in order to improve design and supply the best possible product.
	Obsolete	Not in Production	This data sheet contains specifications on a product that has been discontinued by Radiocrafts. The data sheet is printed for reference information only.



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As far as possible, major changes of product specifications and functionality, will be stated in product specific Errata Notes published at the Radiocrafts website. Customers are encouraged to check regularly for the most recent updates on products and support tools.

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Life Support Policy

This Radiocrafts product is not designed for use in life support appliances, devices, or other systems where malfunction can reasonably be expected to result in significant personal injury to the user, or as a critical component in any life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness. Radiocrafts AS customers using or selling these products for use in such applications do so at their own risk and agree to fully indemnify Radiocrafts AS for any damages resulting from any improper use or sale.

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