DAC161P997

DAC161P997 Single-Wire 16-bit DAC for 4-20mA Loops

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DAC161P997

Single-Wire 16-bit DAC for 4-20mA Loops

1.0 General Description

The DAC161P997 is a 16- bit ∑Δ digital-to-analog converter (DAC) for transmitting an analog output current over an industry standard 4-20 mA current loop. It offers 16-bit accuracy with a low output current temperature coefficient (29ppm/°C) and excellent long-term output current drift (90 ppmFS) while consuming less than 190µA.

The data link to the DAC161P997 is a Single Wire Interface (SWIF) which allows sensor data to be transferred in digital format over an isolation boundary using a single isolation component. The DAC161P997's digital input is compatible with standard isolation transformers and optocouplers. Error detection and handshaking features within the SWIF protocol ensure error free communication across the isolation boundary. For applications where isolation is not required, the DAC161P997 interfaces directly to a microcontroller.

The loop drive of the DAC161P997 interfaces to a HART (Highway Addressable Remote Transducer) modulator, allowing injection of FSK modulated digital data into the 4-20mA current loop. This combination of specifications and features makes the DAC161P997 ideal for 2- and 4-wire industrial transmitters.

The DAC161P997 is available in a 16–lead LLP package and is specified over the extended industrial temperature range of -40°C to 105°C.

2.0 Applications

- Two-wire, 4-20 mA current loop transmitter
- Industrial Process Control
- Actuator control
- Factory Automation
- Building Automation
- Precision Instruments
- Data Acquisition Systems
- Test Systems

3.0 Features

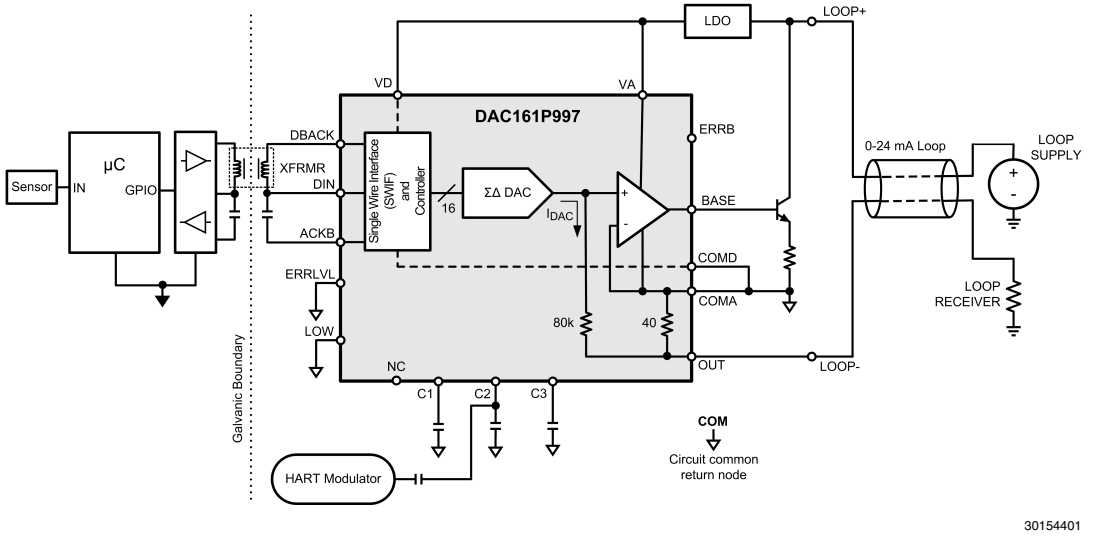
- 16-bit linearity
- Single-Wire Interface (SWIF), with handshake
- Digital Data transmission (no loss of fidelity)
- Pin Programmable Power-Up Condition
- Self adjusting to input data rate
- Loop error detection and reporting
- Programmable output current error level
- No external precision components
- Simple interface to HART modulator
- Small package: LLP-16 (4x4 mm, 0.5 mm pitch)

4.0 Key Specifications

Output Current TempCo	29 ppmFS/°C(max)
Long-Term Output Current Drift	90 ppmFS(typ)
INL	+3.3/–2.1 µA(max)
Total Supply Current	190 µA(max)

5.0 Typical Application - Conceptual Schematic

Industrial 4-20mA Transmitter



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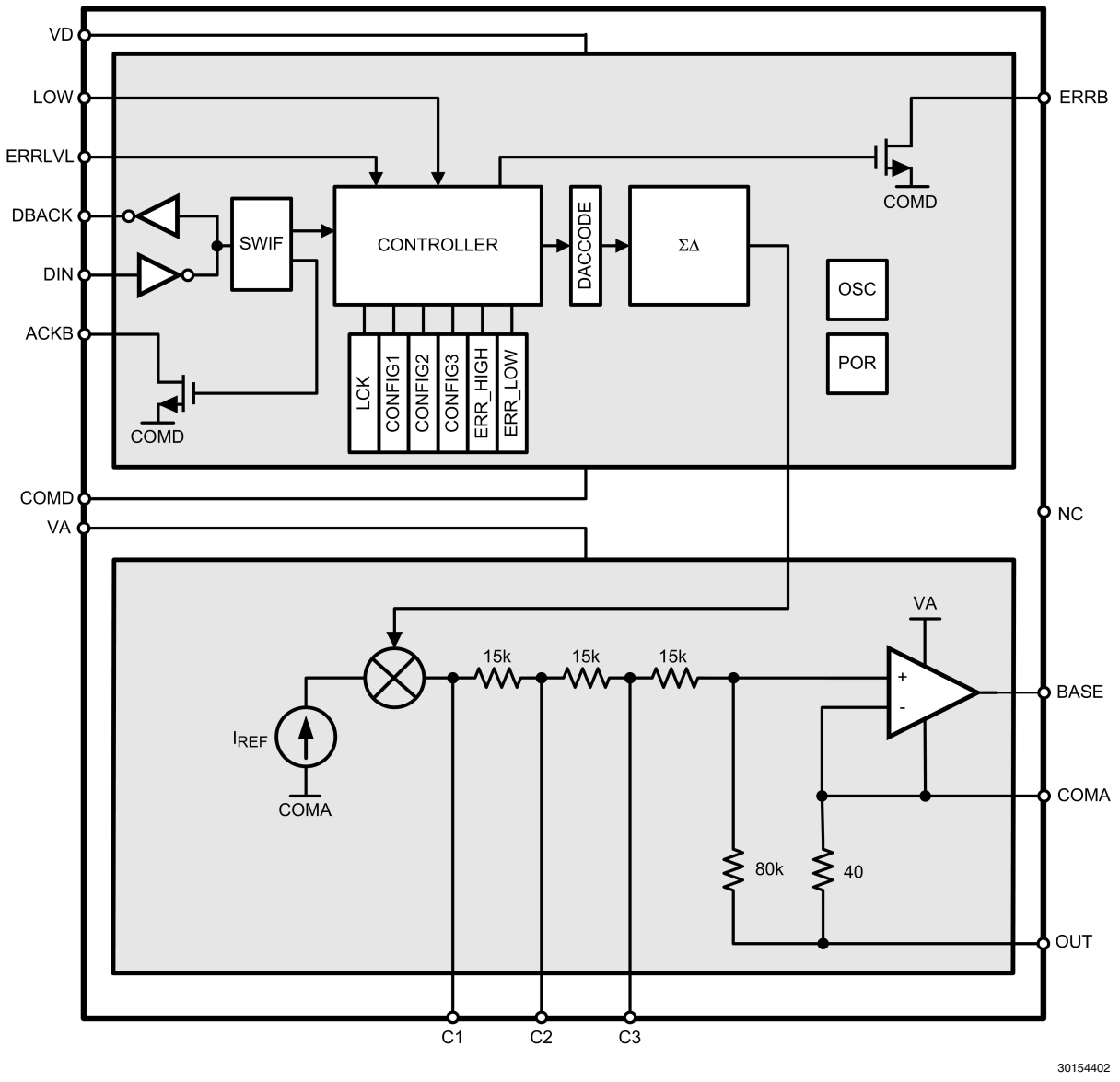
6.0 Block Diagram



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7.0 Functional Overview

7.1 4-20 mA CURRENT LOOP TRANSMITTER

The DAC161P997 is a 16-bit DAC realized as a ∑Δ modulator. The DAC's output is a current pulse train that is filtered by the on-board low pass RC filter. The final output current is a multiplied copy of the filtered modulator output. This architecture guarantees an excellent linearity performance, while minimizing power consumption of the device.

The DAC161P997 eases the design of robust, precise, long-term stable industrial systems by integrating all precision elements on-chip. Only a few external components are needed to realize a low-power, high-precision industrial 4 - 20 mA transmitter.

In case of a fault, or during initial power-up the DAC161P997 will output current in either upper or lower error current band. The choice of band is user selectable via a device pin. The error current value is user programmable via the SWIF link by the Master.

7.2 SINGLE-WIRE INTERFACE (SWIF)

SWIF is a versatile and robust solution for transmitting digital data over the galvanic isolation boundary using just one isolation element: a pulse transformer.

Digital data format achieves the information transmission without the loss of fidelity which usually afflicts transmissions employing PWM (Pulse Width Modulation) schemes. Digital transmission format also makes possible data differentiation: user can specify whether given data word is a DAC input to be converted to loop current, or it is a device configuration word.

SWIF was designed to use in conjunction with pulse transformer as an isolation element. The use of the transformers to cross the isolation boundary is typical in the legacy systems due to their robustness, low-power consumption, and low cost. However, system implementation is not limited to the transformer as a link since SWIF easily interfaces with opto-couplers, or it can be directly driven by a CMOS gate.

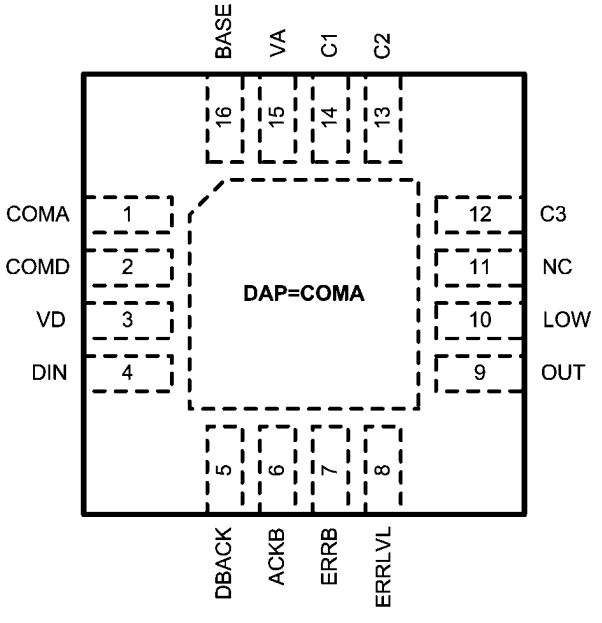
SWIF incorporates a number of features that address robustness aspect of the data link design:

1. Bidirectional signal flow: the DAC161P997 can issue an ACKNOWLEDGE pulse back to the master transmitter, via the same physical channel, to confirm the reception of the valid data;
2. Error Detection: SWIF protocol incorporates frame length detection and parity checks as a method of verifying the integrity of the received data;
3. Channel Activity Detection: SWIF can monitor the data channel and raise an error flag should the expected activity drop below programmable threshold, due to , for example, damage to the physical channel.

In the typical system the Master is a micro controller. SWIF has been implemented on a number of popular micro controllers where it places minimum demands on the hardware or software resources even of the simple 8-bit devices.

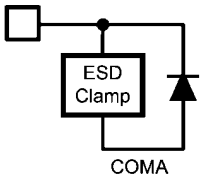
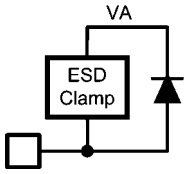
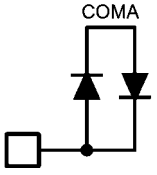
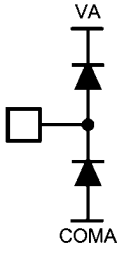
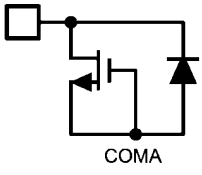
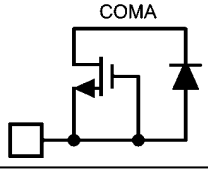
SWIF gives the system designer flexibility is balancing the trade-offs between the data rate, activity monitoring functionality and the power consumption in the transformer coupled data channel. At lowest data rates, with long inactive inter-frame periods, the power consumed by SWIF is negligible. See *Section 17.2.2 Inter-Frame Period*

8.0 Connection Diagram



LLP-16 (SQ16A)
Top View

9.0 Pin Descriptions

Name	Pin	Function	ESD Protection
VA	15	Analog block positive supply rail	
COMA	1	Analog block negative supply rail (local COMMMON)	
COMD	2	Digital block negative supply rail (local COMMON)	
VD	3	Digital block positive supply rail	
DIN	4	SWIF input	
DBACK	5	SWIF input loop back	
ACKB	6	SWIF acknowledge output - open drain, active LOW	
ERRLVL	8	Sets the output current level at power-up	
LOW	10	Must be tied to COMA, COMD potential	
C1	14	External capacitor	
C2	13	External capacitor, HART Input	
C3	12	External capacitor	
BASE	16	External NPN base drive	
N.C.	11	User must not connect to this pin	
ERRB	7	Error flag output open drain, active LOW	
OUT	9	Loop output current source	
DAP	-	Die Attach Pad. For best thermal conductivity and best noise immunity DAP should be soldered to the PCB pad which is connected directly to circuit common node (COMA, COMD)	-

10.0 Ordering Information

Order Number	NS Package Number	Transport Media
DAC161P997CISQ	SQ16A	Tape-and reel: 1000 pieces
DAC161P997CISQX		Tape-and reel: 2500 pieces

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11.0 Absolute Maximum Ratings (*Note 1*, *Note 2*)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply relative to common (VA, VD to COMA, COMD)	−0.3V to 6.0V
Voltage between any 2 pins(*Note 3*)	6.0V
Current IN or OUT of any pin - except OUT (*Note 3*)	5 mA
Output current at OUT	50 mA
Junction Temperature	+150°C
Storage Temperature Range	−65°C to +150°C
ESD Susceptibility	
(*Note 4*) Human Body Model	5500V
Machine Model	500V
Charged Device Model	1250V

12.0 Operating Conditions (*Note 1*, *Note 2*)

Operating Temperature (T_A)	−40°C to 105°C
Supply Voltage Range	2.7V to 3.6V
(VA - VD)	0V
(COMA - COMD)	0V
BASE load to COMA	0 to 15 pF
OUT load to COMA	none

Package	θ_{JA}
LLP16	35°C/W

For Soldering specifications:

See product folder at www.national.com and www.national.com/ms/MS-SOLDERING.pdf.

13.0 Electrical Characteristics

Unless otherwise noted, these specifications apply for VA = VD = 2.7V to 3.6V, T_A=25°C, external bipolar transitor: 2N3904, R_E=22Ω, C_1=C_2=C_3=2.2nF. **Boldface** limits are over the temperature range of −40°C ≤ T_A ≤ 105°C unless otherwise noted.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
		POWER SUPPLY				
VA, VD	Supply Voltage	VA = VD	**2.7**		**3.6**	V
	VA Supply Current	DACCODE=0x0200 (*Note 5*)			**75**	µA
	VD Supply Current				**115**	µA
	Total Supply Current				**190**	µA
VPOR	Power On Reset supply rail potential threshold		**1.3**		**1.9**	V
		DC ACCURACY				
N	Resolution			16		Bits
INL	Integral Non-Linearity	0x2AAA<DACCODE<0xD555 (4mA<I_{LOOP}<20 mA)	**−2.1**		**+3.3**	µA
DNL	Differential Non-Linearity	(*Note 10*)	**−0.2**		**+0.2**	
TUE	Total Unadjusted Error	0x2AAA<DACCODE<0xD555	**−0.23**		**+0.23**	%FS
OE	Offset Error	(*Note 6*)	**−9.16**		**+9.16**	µA
	Offset Error Temp. Coefficient				**138**	nA/°C
GE	Gain Error	(*Note 7*)	**−0.22**		**0.22**	%FS
	Gain Error Temp. Coefficient			5	**29**	ppmFS/°C
	4mA Loop Current Error	DACCODE = 0x2AAA	**−18**		**+18**	µA
	20 mA Loop Current Error	DACCODE = 0xD555	**−55**		**+55**	
IERRL	LOW ERROR Current	ERR_LOW = default	**3361**	3375	**3391**	
IERRH	HIGH ERROR Current	ERR_HIGH = default	**21702**	21750	**21817**	
LTD	Long Term Drift — mean shift of 12 mA output current after 1000 hrs at 150°C			90		ppmFS
		LOOP CURRENT OUTPUT (OUT)				
	Output Current	Minimum tested at DACCODE = 0x01C2 (*Note 8*)	**0.18**		**24**	mA
	Output Impedance		**100**			MΩ
	COMA to OUT voltage drop	I_{OUT} = 24 mA		960		mV
		BASE OUTPUT				
	BASE short circuit output current	BASE forced to COMA potential		10		mA

Symbol	Parameter	Conditions	Min	Typ	Max	Units
		DYNAMIC CHARACTERISTICS				
	Output Noise Density	1kHz		20		nA/√Hz
	Integrated Output Noise	1Hz to 1kHz band		300		nA_{RMS}
		SWIF I/O CHARACTERISTICS				
VIH	DIN		**0.7*VD**			V
VIL	DIN				**0.3*VD**	
CDIN	DIN input capacitance			10		pF
VOH	DBACK	I = 3mA	**2216**			mV
		I = 5mA	**1783**			
VOL	DBACK	I = 3mA			**547**	
		I = 5mA			**1260**	
TD	DIN to DBACK delay				**8**	ns
		OPEN DRAIN OUTPUTS				
VOL	ACKB	I = 3mA			**550**	mV
		I = 5mA			**1370**	
VOL	ERRB	I = 300 µA			**66**	mV
		I = 3mA			**602**	
IOZ	ACKB	Leakage current when output device is off			**1**	µA
	ERRB	Leakage current when output device is off			**1**	
		SWIF TIMING				
	Symbol rate: 1/TP		**0.3**		**19.2**	kHz
	“D” symbol duty cycle: THD/TP		**7/16**	1/2	**9/16**	
	“0” symbol duty cycle: TH0/TP		**3/16**	1/4	**5/16**	
	"1” symbol duty cycle: TH1/TP		**11/16**	3/4	**13/16**	
	ACKB assert: TA/TP		**1/16**	1/4	**4/8**	
	ACKB deassert: TB/TP		**12/8**	7/4	**31/16**	
		Internal Timer				
TM	Timeout Period		**90**	100	**110**	ms

Note 1: “Absolute Maximum Ratings” indicate limits beyond which damage to the device may occur, including inoperability and degradation of device reliability and/or performance. Functional operation of the device and/or non-degradation at the Absolute Maximum Ratings or other conditions beyond those indicated in the Recommended Operating Conditions is not implied. The recommended Operating Conditions indicate conditions at which the device is functional and the device should not be operated beyond such conditions.

Note 2: All voltages are measured with respect to COMA = COMD = 0V, unless otherwise specified.

Note 3: When the input voltage (VIN) at any pin exceeds power supplies (VIN < COMA or VIN > VA), the current at that pin must not exceed 5 mA, and the voltage (VIN) at that pin relative to any other pin must not exceed 6.0V. See *Section 9.0 Pin Descriptions* for additional details of input structures.

Note 4: The Human Body Model (HBM) is a 100 pF capacitor charged to the specified voltage then discharged through a 1.5 kΩ resistor into each pin. The Machine Model (MM) is a 200 pF capacitor charged to specified voltage then discharged directly into each pin. The Charged Device Model (CDM) is a specified circuit characterizing an ESD event that occurs when a device acquires charge through some triboelectric (frictional) or electrostatic induction process and then abruptly touches a grounded object or surface.

Note 5: At code 0x0200 the BASE current is minimal, i.e., device current contribution to power consumption is minimized. The SWIF link is inactive, i.e., after transmitting code 0x200 to the DAC161P997, there are no more transitions in the channel during the supply current measurement.

Note 6: Here offset is the y-intercept of the straight line defined by 4 mA and 20 mA points of the measured transfer characteristic.

Note 7: Here Gain Error is the difference in slope of the straight line defined by measured 4 mA and 20 mA points of transfer characteristic, and that of the ideal characteristic.

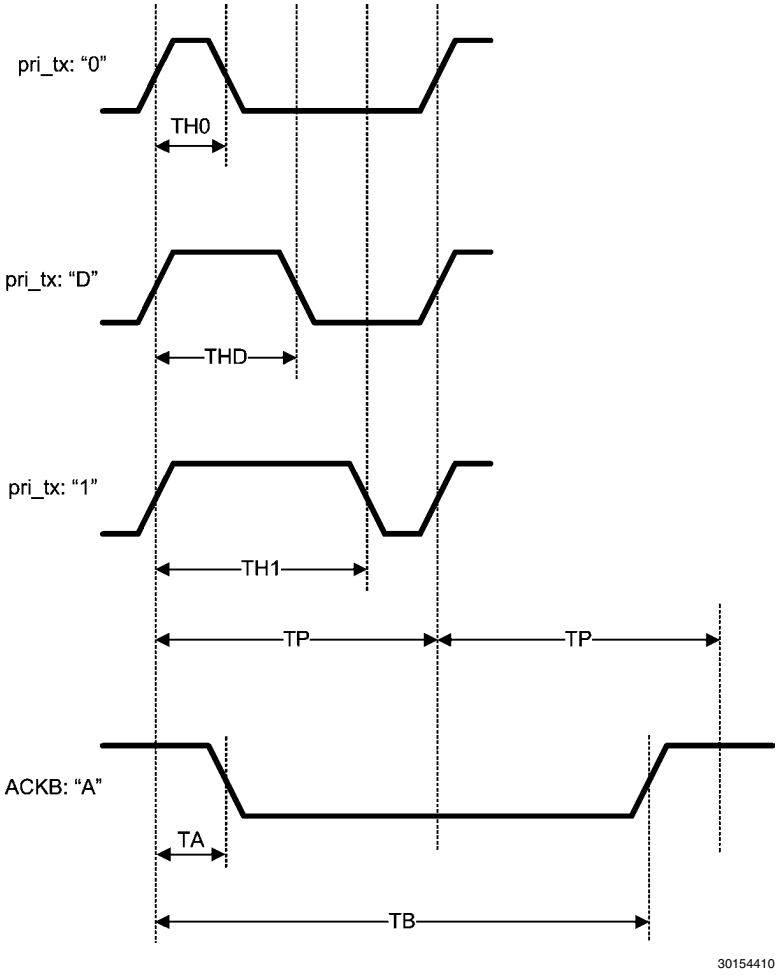
Note 8: This should be treated as the minimum LOOP current guarantee.

Note 9: INL is measured using “best fit” method in the output current range of 4 mA to 20 mA.

Note 10: Guaranteed by design.

14.0 Single-Wire Interface (SWIF) Timing Diagram

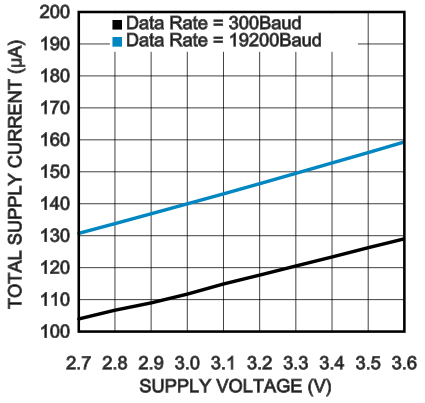
See section *Section 17.2.3 Symbol Set* for SWIF waveform description



15.0 Typical Performance Characteristics

Unless otherwise noted, data presented here was collected under these conditions VA = VD = 3.3V, T_A=25°C, external bipolar transistor: 2N3904, R_E=22Ω, C_1=C_2=C_3=2.2 nF.

Supply Current vs Supply Voltage



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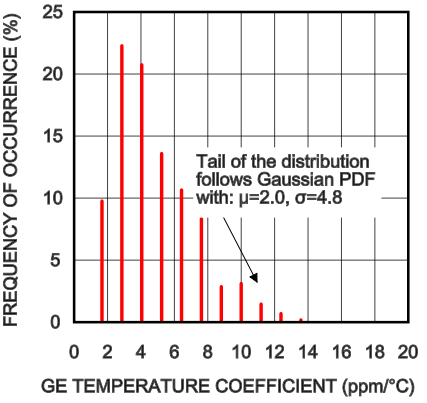
Gain Error TC distribution



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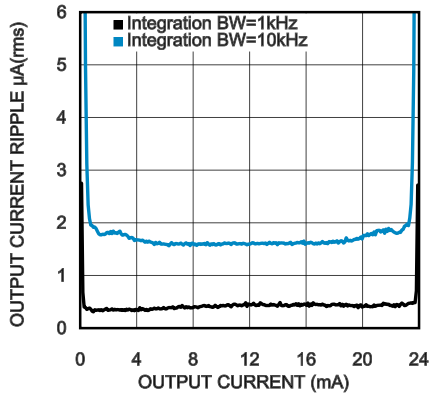
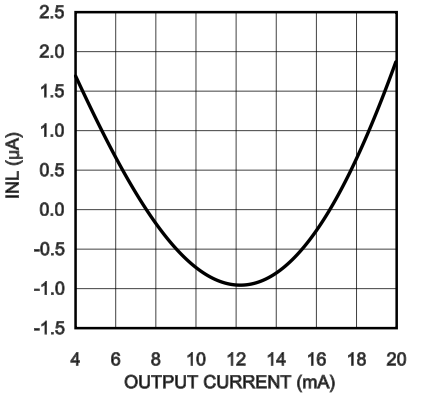
Integrated Noise vs I_{LOOP}



30154434

Linearity vs I_{LOOP}



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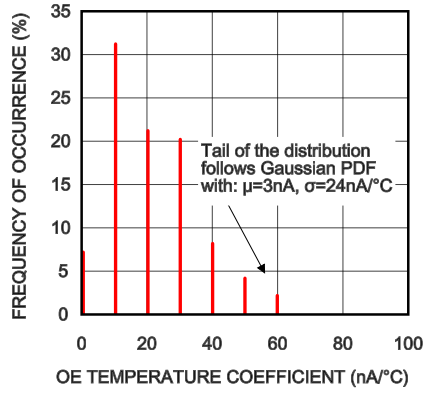
Offset Error TC Distribution



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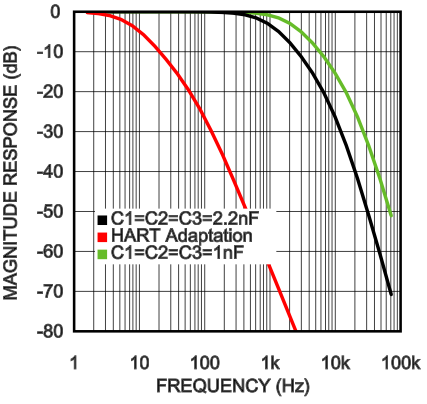
ΣΔ Modulator Filter Response



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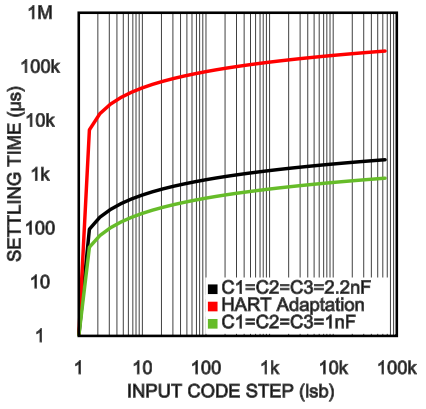
Settling Time vs Input Step Size



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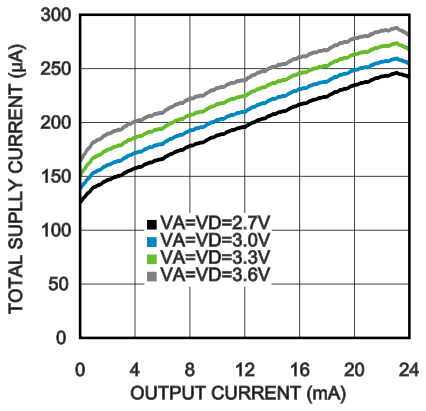
Supply Current vs I_{LOOP}



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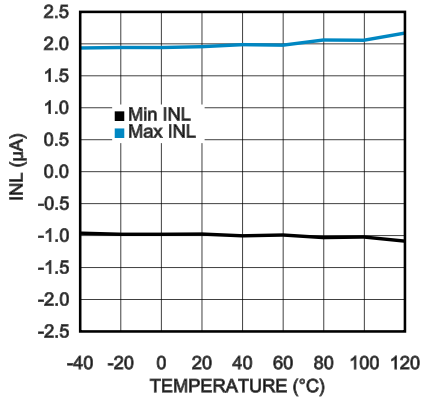
Output Linearity vs Temperature



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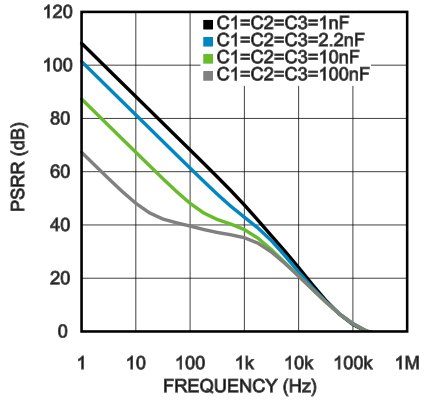
PSRR: I_{LOOP}=4mA



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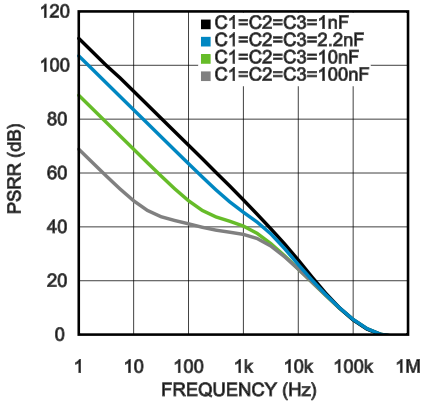
PSRR: I_{LOOP}=20mA



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16.0 Register Set

16.1 LCK: Address=0x00; Default=0x00

Bit Field	Name	Description
7:0		0x95 - registers unlocked 0x** - any value written locks registers A register lock prevents inadvertent changes to the configuration. The DAC output cannot be updated while software configuration registers are unlocked.

16.2 CONFIG1: Address=0x01; Default=0x08

Bit Field	Name	Description
7:5		RESERVED. Always write 0.
4:3	SERR	0b00 - NOP 0b01 - set error 0b10 - clear error 0b11 - NOP Sets or clears the error condition. At power-on the error is set. Error is also cleared after reception of valid SWIF frame. These bits are self clearing. This functionality can be used for diagnostic purposes, e.g. Master can use SERR to force I_{LOOP} into an error band, and then return it to previously held output level.
2:1		RESERVED. Always write 0.
0	RST	0 - NOP 1- same as power-on reset. Once device is reset to default state the bit clears automatically

16.3 CONFIG2: Address=0x02; Default=0x1F

Bit Field	Name	Description
7:5		RESERVED. Always write 0.
4	ACK_EN	Set to enable ACK When enabled, an acknowledgement is indicated on the serial interface upon detection of each valid frame. See *Section 17.2.1 Frame Format*
3	FRAME	Set to enable framing error reporting. See table in *Section 17.3 ERROR DETECTION AND REPORTING*
2	PARITY	Set to enable parity error reporting. See table in *Section 17.3 ERROR DETECTION AND REPORTING*
1	CHANNEL	Set to enable channel-inactive reporting. See table in *Section 17.3 ERROR DETECTION AND REPORTING*
0	LOOP	Set to enable loop error reporting. See table in *Section 17.3 ERROR DETECTION AND REPORTING*

16.4 CONFIG3: Address=0x03; Default=0x08

Bit Field	Name	Description
7:4		RESERVED. Always write 0.
3:0	RX_ERR_CNT	0 <= RX_ERR_CNT ≤ 15 Threshold = 1 + RX_ERR_CNT The slave enters the error state once 'Threshold' number of consecutive FRAME or PARITY errors are counted. The threshold is programmable to prevent occasional errors from being reported. See table in *Section 17.3 ERROR DETECTION AND REPORTING*

16.5 ERR_LOW: Address=0x04; Default=0x24

Bit Field	Name	Description
7:0		8-bit value. If ERRLVL = LOW, the DAC will use the value stored in ERR_LOW register to set the output current sourced from OUT pin when reporting an error condition. The ERR_LOW value is used as the upper byte of the DACCODE, while the lower byte is forced to 0x00. At power up the ERR_LOW defaults to a value which forces IERRL output current. See *Section 13.0 Electrical Characteristics*

16.6 ERR_HIGH: Address=0x05; Default=0xE8

Bit Field	Name	Description
7:0		If ERRLVL = HIGH, the DAC will use the value stored in ERR_HIGH register to set the output current sourced from OUT pin when reporting an error condition. The ERR_HIGH value is used as the upper byte of the DACCODE, while the lower byte is forced to 0x00. At power-up the ERR_HIGH defaults to a value which forces IERRH output current. See *Section 13.0 Electrical Characteristics*

17.0 Application Information

17.1 16-BIT DAC AND LOOP DRIVE

17.1.1 DC Characteristics

The DAC converts the 16-bit input code in the DACCODE register to an equivalent current output. The ∑Δ DAC output is a current pulse which is then filtered by a 3rd order RC low-pass filter and boosted to produce the loop current I_{LOOP} at the device OUT pin.

Figure 1 shows the principle of operation of the DAC161P997 in the Loop Powered Transmitter - the circuit details were omitted for clarity. In this figure I_D and I_A represent supply (quiescent) currents of the internal digital and analog blocks. I_{AUX} represents supply (quiescent) current of companion devices present in the system, such as the voltage regulator and the SWIF channel.

By observing that the control loop formed by the amplifier and the bipolar transistor forces the voltage across R_1 and R_2 to be equal, it can be shown that, under normal conditions, the I_{LOOP} is dependent only on I_{DAC} through the following relationship:

$$I_{LOOP} = \left(1 + \frac{R1}{R2}\right) I_{DAC}, \text{where } I_{DAC} = f(\text{DACCODE})$$

While I_{LOOP} has a number of component currents, $I_{LOOP} = I_{DAC}+I_D+I_A+I_{AUX}+I_E$, it is only I_E that is regulated by the loop to maintain the relationship shown above.

Since it is only I_E's magnitude that is controlled, not its direction, there is a lower limit to I_{LOOP}. This limit is dependent on the fixed components I_A and I_D, and on system implementation through I_{AUX}.

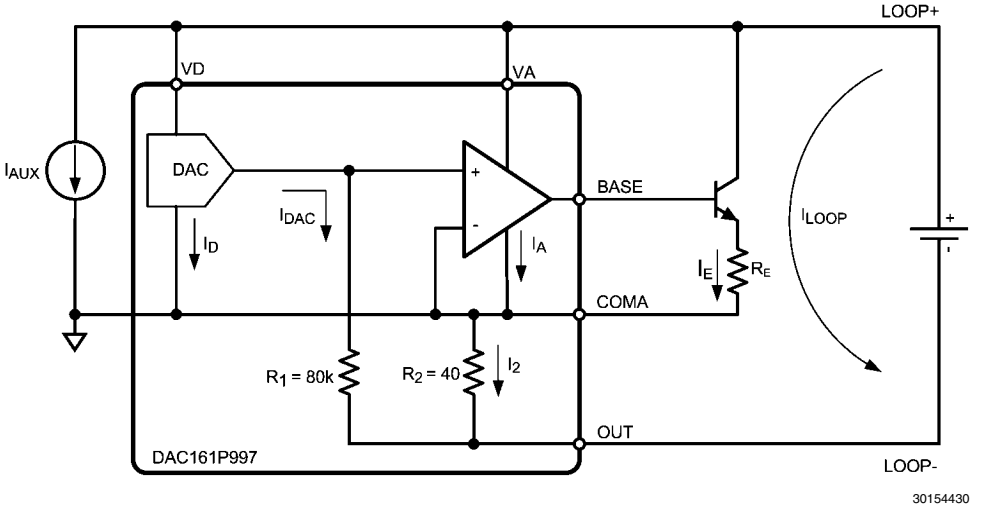


FIGURE 1. Loop-Powered Transmitter

Figure 2 shows the variant of the transmitter where the supply currents to the system blocks are provided by the local supply, and not the 4 - 20 mA loop Self-Powered Transmitter. Same basic relationship between the I_{LOOP} and I_{DAC} holds, but the component currents of I_{LOOP} are only I_{DAC} and I_E.

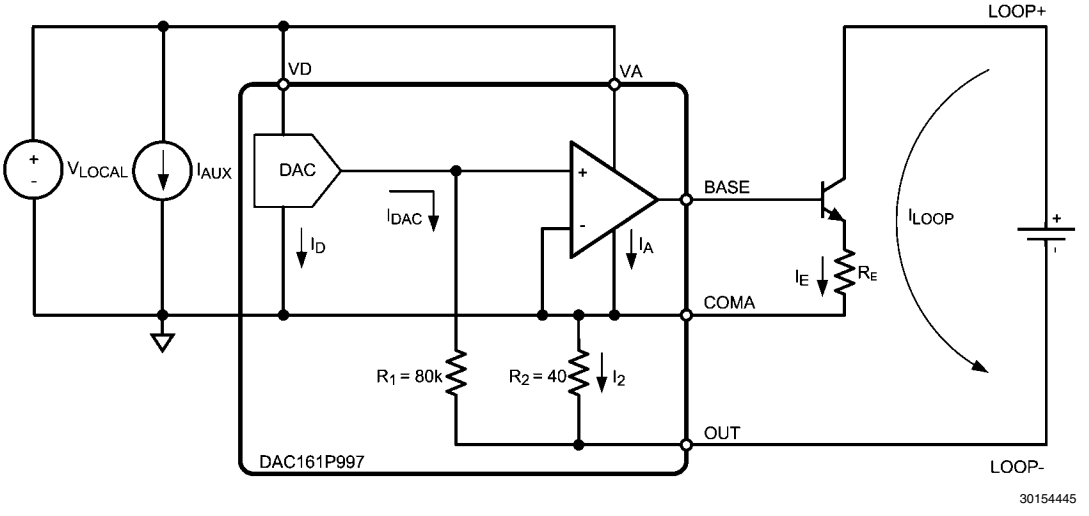


FIGURE 2. Self-Powered Transmitter

17.1.1.1 DC Input-Output Transfer Function

The output current sourced by the OUT pin of the device is expressed by:

$$I_{LOOP} = \left(\frac{DACCODE}{2^{16}}\right) 24mA$$

The valid DACCODE range is the full 16-bit code space (0x0000 to 0xFFFF), which results in the I_{DAC} range of 0 to approximately 12 µA. This, however, does not result in the I_{LOOP} range of 0 to 24 mA.

The maximum output current sourced out of OUT pin, I_{LOOP}, is 24 mA. The minimum output current is dependent on the system implementation. The minimum output current is the sum of supply currents of the DAC161P997 internal blocks, I_A, I_D, and companion devices present in the system, I_{AUX}. The last component current I_E can theoretically be controlled down to 0 but, due to the stability considerations of the control loop, it is advised not to allow the I_E to drop below 200 µA.

The graph in *Figure 3* shows the DC transfer characteristic of the 4 - 20 mA transmitter, including minimum current limits. The minimum current limit for the Loop-Powered Transmitter is typically around 400 µA (I_D+I_A+I_{AUX}+I_E). The minimum current limit for the Self-Powered Transmitter is typically around 200 µA (I_E).

Typical values for I_D and I_A are listed in the Electrical Characteristics table. I_E depends on the BJT device used.

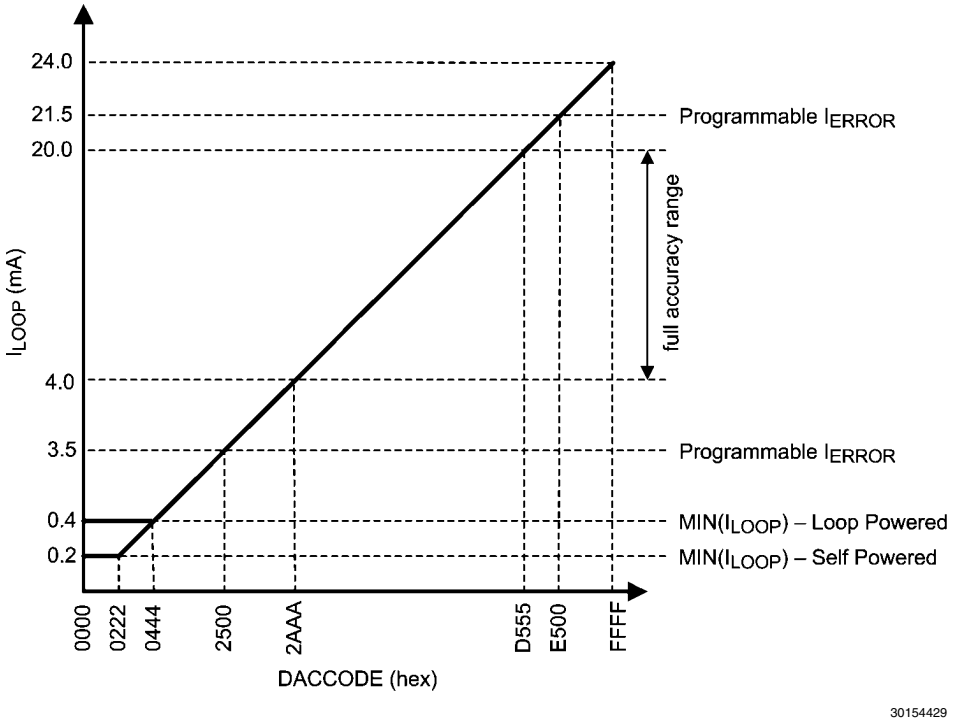


FIGURE 3. DAC DC Transfer Function

17.1.1.2 Loop Interface

The DAC161P997 cannot directly interface to the typical 4 - 20 mA loop due to the excessive loop supply voltage. The loop interface has to provide the means of stepping down the LOOP Supply down to 3.6V. This can be accomplished with either a linear regulator (LDO) or switching regulator while keeping in mind that the regulator's quiescent current will have direct effect on the minimum achievable I_{LOOP} (see *Section 17.1.1.1 DC Input-Output Transfer Function*).

The second component of the loop interface is the external NPN transistor (BJT). This device is part of the control circuit that regulates the transmitter's output current (I_{LOOP}). Since the BJT operates over the wide current range, spanning at least 4 - 20 mA, it is necessary to degenerate the emitter in order to stabilize transistor's transconductance (g_m). The degeneration resistor of 22Ω is suggested in typical applications. For circuit details, see *Section 18.0 Application Circuit Examples*.

The NPN BJT should not be replaced with an N-channel FET (Field Effect Transistor) for the following reasons: discrete FET's typically have high threshold voltages (VT), in the order of 1.5V to 2V, which is beyond the BASE output maximum range; discrete FET's present higher load capacitance which may degrade system stability margins; and BASE output relies on the BJT's base current for biasing.

17.1.1.3 Loop Compliance

The maximum V(LOOP+,LOOP-) potential is limited by the choice of step-down regulator, and the external BJT's Collector Emitter breakdown voltage. For minimum V(LOOP+, LOOP−) potential consider *Figure 2*. Here, observe that V (LOOP+,LOOP−)≅min(V_{CE}) + $I_{LOOP}R_E$ + $I_{LOOP}R_2$=min(V_{CE}) + 0.53V + 0.96V=3.66V, at I_{LOOP}=24mA. The voltage drop across internal R_2 is specified in *Section 13.0 Electrical Characteristics*

17.1.2 AC Characteristics

The approximate frequency dependent characteristics of the loop drive circuit can be analyzed using the circuit in *Figure 4*:

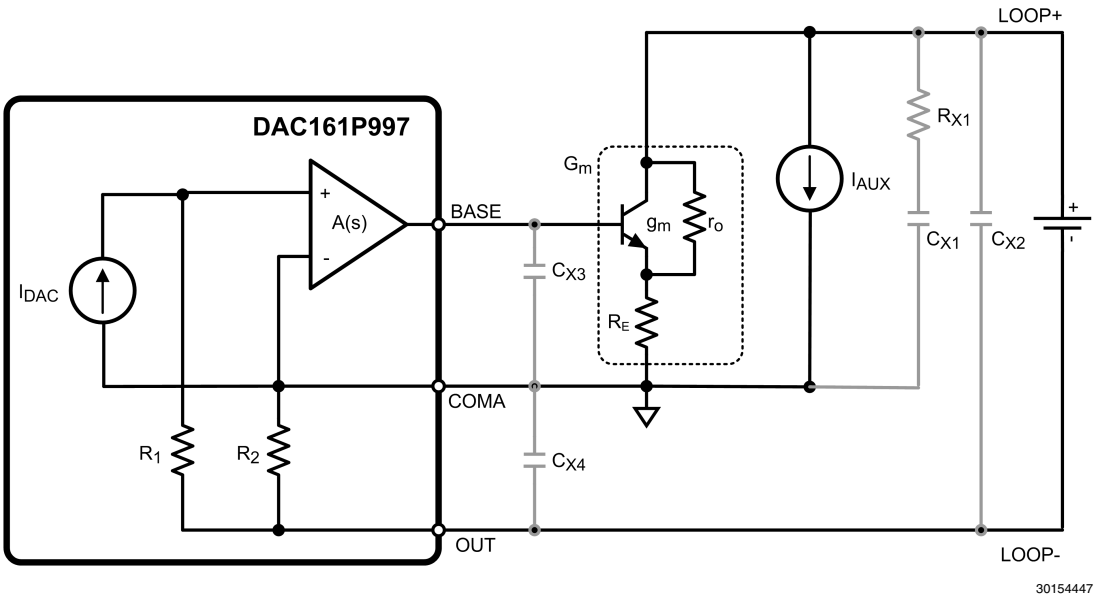


FIGURE 4. Capacitances affecting Control Loop

Here it is assumed that the internal amplifier dominates the frequency response of the system, and it has a single pole response. The BJT's response, in the bandwidth of the control loop, is assumed to be frequency independent and is characterized by the transconductance g_m and the output resistance r_o.

As in previous sections I_{DAC} and I_{AUX} represent the filtered output of the $\sum\Delta$ modulator and the quiescent current of the companion devices.

The circuit in *Figure 4* can be further simplified by omitting the on-board capacitances, whose effect will be discussed in *Section 17.1.2.4 Stability*, and by combining the amplifier, the external transistor and resistor R_E into one G_m block. The resulting circuit is shown in *Figure 5*.

By assuming that the BJT's output resistance (r_o) is large, the loop current I_{LOOP} can be expressed as:

$$I_{LOOP} = I_{AUX} + A(s)\, G_m\, v_e$$

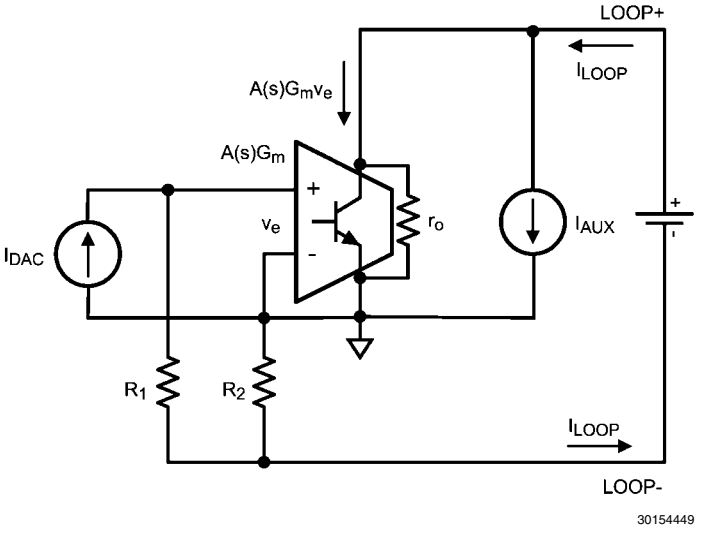


FIGURE 5. AC Analysis Model of a Transmitter

The sum of voltage drops around the path containing R_1, R_2 and v_e is:

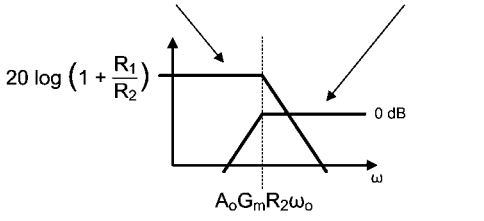
$$v_e = I_{DAC} R_1 - \left[I_{AUX} + A(s) G_m v_e - I_{DAC} \right] R_2$$

an assumption is made on the response of the internal amplifier::

$$A(s) = \frac{A_o \omega_o}{s}$$

By combining the above the final expression for the I_{LOOP} as a function of 2 inputs I_{DAC} and I_{AUX} is:

$$I_{LOOP} = I_{DAC} \left(1 + \frac{R_1}{R_2}\right) \frac{A_o G_m R_2 \omega_o}{s + A_o G_m R_2 \omega_o} + I_{AUX} \frac{s}{s + A_o G_m R_2 \omega_o}$$



The result above reveals that there are 2 distinct paths from the inputs I_{DAC} and I_{AUX} to the output I_{LOOP}. I_{DAC} follows the low-pass, and the I_{AUX} follows the high-pass path.

In both cases the corner frequency is dependent on the effective transconductance, G_m, of the external transistor. This implies that control loop dynamics could vary with the output current I_{LOOP} if G_m were allowed to be just native device transconductance g_m. This undesirable behavior is mitigated by the degenerating resistor R_E which stabilizes G_m as follows:

$$G_m \cong \frac{1}{1/g_m + R_E} \cong \frac{1}{R_E}$$

This results in the frequency response which is largely independent of the output current I_{LOOP}:

$$I_{LOOP} = I_{DAC} \left(1 + \frac{R_1}{R_2}\right) \frac{A_o \frac{R_2}{R_E} \omega_o}{s + A_o \frac{R_2}{R_E} \omega_o} + I_{AUX} \frac{s}{s + A_o \frac{R_2}{R_E} \omega_o}$$

While the bandwidth of the I_{DAC} path may not be of great consequence given the low frequency nature of the 4-20 mA current loop systems, the location of the pole in the I_{AUX} path directly affects PSRR of the transmitter circuit. This is further discussed in *Section 17.1.2.3 PSRR*.

17.1.2.1 Step Response

The transient input-output characteristics of the DAC161P997 are dominated by the response of the RC filter at the output of the ∑Δ DAC. Settling times due to step input are shown in *Section 15.0* .

17.1.2.2 Output impedance

The output impedance is described as:

$$R_{OUT} = \frac{\Delta V_{LOOP}}{\Delta I_{LOOP}}$$

By considering the circuit in *Figure 5*, and setting $I_{DAC} = I_{AUX} = 0$, the following expression can be obtained:

$$R_{OUT}(s) = R_2 + \left[1 + A(s) G_m R_2\right] r_o$$

As in *Section 17.1.2 AC Characteristics* an assumption can be made on the frequency response of the internal amplifier, and the effective transconductance G_m should be stabilized with external R_E leading to:

$$R_{OUT}(s) \approx \frac{A_o \left(\frac{R_2}{R_E}\right) \omega_o r_o}{s}$$

The output impedance of the transmitter is a product of the external BJT's output resistance r_o, and the frequency characteristics of the internal amplifier. At low frequencies this results in a large impedance that does not significantly affect the output current accuracy.

17.1.2.3 PSRR

Power Supply Rejection Ratio is defined as the ability of the current control loop to reject the variations in the supply current of the companion devices, I_{AUX}. Specifically:

$$PSRR = 20 \times \log_{10} \left(\frac{\Delta I_{LOOP}}{\Delta I_{AUX}} \right)$$

It was shown in *Section 17.1.2 AC Characteristics* that the I_{AUX} affects I_{LOOP} via the high-pass path whose corner frequency is dependent on the effective Gm of the external BJT. If that dependence were not mitigated with the degenerating resistor R_E, the PSRR would be degraded at low output current I_{LOOP}.

The typical PSRR performance of the transmitter shown in *Section 18.0 Application Circuit Examples* is shown in *Section 15.0* .

17.1.2.4 Stability

The current control loop's stability is affected by the impedances present in the system. *Figure 4* shows the simplified diagram of the control loop, formed by the on-board amplifier and an external BJT, and the lumped capacitances C_{X1} through C_{X4} that model any other external elements.

C_{X1} typically represents a local step-down regulator, or LDO, and any other companion devices powered from the LOOP+. This capacitance reduces the stability margins of the control loop, and therefore it should be limited. RX1 can be used to isolate C_{X1} from LOOP+ node and thus remedy the stability margin reduction. If $R_{X1} = 0$, C_{X1} cannot exceed 10 nF. $R_{X1} = 200\Omega$ is recommended if it can be tolerated. Minimum $R_{X1} = 40\Omega$ if C_{X1} exceeds 10 nF.

C_{X3} also adversely affects stability of the loop and it must be limited to 20 pF. C_{X4} affects the control loop in the same way as C_{X1}, and it should be treated in the same way as C_{X1}. C_{X2} is the only capacitance that improves stability margins of the control loop. Its maximum size is limited only by the safety requirements.

Stability is a function of I_{LOOP} as well. Since I_{LOOP} is approximately equal to the collector current of the external BJT, G_m of the BJT, and thus loop dynamics, depend on I_{LOOP}. This

dependence can be reduced by degenerating the emitter of the BJT with a small resistance as discussed in *Section 17.1.1.2 Loop Interface*. Inductance in series with the LOOP+ and LOOP– do not significantly affect the control loop.

17.1.2.5 Noise and Ripple

The output of the DAC is a current pulse train. The transition density varies throughout the DAC input code range (I_{LOOP} range). At the extremes of the code range, the transition density is the lowest which results in low frequency components of the DAC output passing through the RC filter. Hence, the magnitude of the ripple present in I_{LOOP} is the highest at the ends of the transfer characteristic of the device (see *Section 15.0*).

It should be noted that at wide noise measurement bandwidth, it is the ripple due to the ∑Δ modulator that dominates the noise performance of the device throughout the entire code range of the DAC. This results in the “U” shaped noise characteristic as a function of output current. At narrow bandwidths, and particularly at mid-scale output currents, it is the amplifier driving the external BJT that starts to dominate as a noise source.

17.1.2.6 Digital Feedthrough

Digital feedthrough is indiscernible from the ripple induced by the ∑Δ modulator.

17.1.2.7 HART Signal Injection

The HART specification requires minimum suppression of the sensor signal in the HART signal band (1-2 kHz) of about 60 dB. The filter in *Figure 6* below meets that requirement.

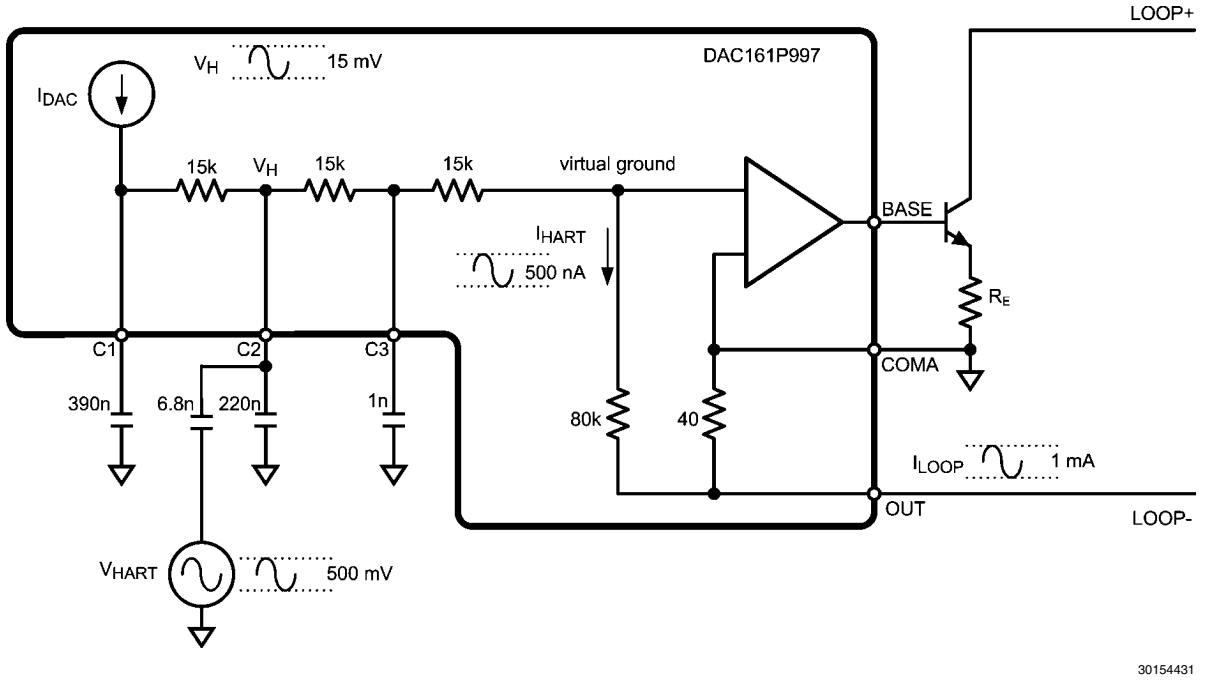


FIGURE 6. HART Signal Injection

17.1.2.8 RC Filter Limitation

In an effort to speed up the transient response of the device the user can reduce the capacitances associated with the low-pass filter at the output of the ∑Δ modulator. However, to maintain stability margins of the current control loop it is necessary to have at least C_1=C_2=C_3=1nF.

17.1.3 Alarm Current

The DAC161P997 reports faults to the plant controller by forcing the OUT current into one of the error bands. The error current bands are defined as either above 20 mA, or below 4mA. The error band selection is done via the ERRLVL pin. The exact value of the output current used to indicate fault is dictated by the contents of ERR_HIGH and ERR_LOW registers. See *Section 16.5 ERR_LOW: Address=0x04; Default=0x24* and *Section 16.6 ERR_HIGH: Address=0x05; Default=0xE8*.

The default settings for LOW ERROR CURRENT and HIGH ERROR CURRENT are specified in *Section 13.0 Electrical Characteristics*

17.2 SINGLE-WIRE INTERFACE (SWIF)

SWIF provides flexible and easy to implement digital data link between the Master (transmitter) and the Slave (receiver). The Master encodes the digital data into a square (NRZ) CMOS level waveform which can be generated using common microcontroller resources. The Slave (DAC161P997) translates the waveform back into a bit stream which is then interpreted as the output current update or configuration data.

SWIF can operate in both Simplex (unidirectional) and Half-Duplex (bidirectional) modes. In the DAC161P997's implementation of SWIF, an Acknowledge pulse constitutes the reverse data flowing from the Slave back to the Master.

In its simplest implementation, the waveform can be directly coupled to the DAC161P997 input. In typical systems, however, SWIF data is transmitted via the galvanic isolation element such as pulse transformer or an opto-coupler. The details of the circuit implementations are discussed in *Section 17.2.4 Interface Circuit*.

Section 17.2.1 Frame Format through *Section 17.2.3 Symbol Set* describe the data encoding and the SWIF protocol.

17.2.1 Frame Format

A frame begins with a minimum of one idle symbol. There can be more than one and each has the effect of resetting the frame buffer of the DAC161P997. After idle symbol "D" a Tag Bit specifies the destination of the frame. If the tag is symbol '0' then frame's destination is the DACCODE register. If tag is a '1' the destination is one of the configuration registers.

The following 16 symbols constitute the data payload. If current frame is a DAC frame, the entire payload is a single DACCODE word. If it is a configuration frame, the first byte is the register address and the second byte is the register data. Words are transmitted MSB first.

Two parity symbols follow the payload. The first parity symbol is determined by the bit parity of the tag bit and the first byte of payload (HIGH Slice) – a total of nine symbols. The second parity symbol corresponds to bit parity of the second byte of payload only (LOW Slice) – a total of 8 symbols.

P0 = [(Number of ones in LOW Slice) mod 2 == 0]

P1 = [(Number of ones in HIGH Slice) mod 2 == 0]

Symbol 'D' after the parity bits completes a valid frame.

The symbol "A" is optional, but if present it has to immediately follow the last "D" symbol of the frame. The duration of acknowledge symbol "A" is always twice the duration of P0 symbol preceding it. See *Figure 7*.

SWIF does not require that all symbols in valid frames are sent by the Master at a fixed Baud rate. Each symbol is evaluated individually and is recognized as valid as long as it conforms to the duration requirement (Tp) and its duty cycle falls outside of noise margins. (See *Table 1* below.)

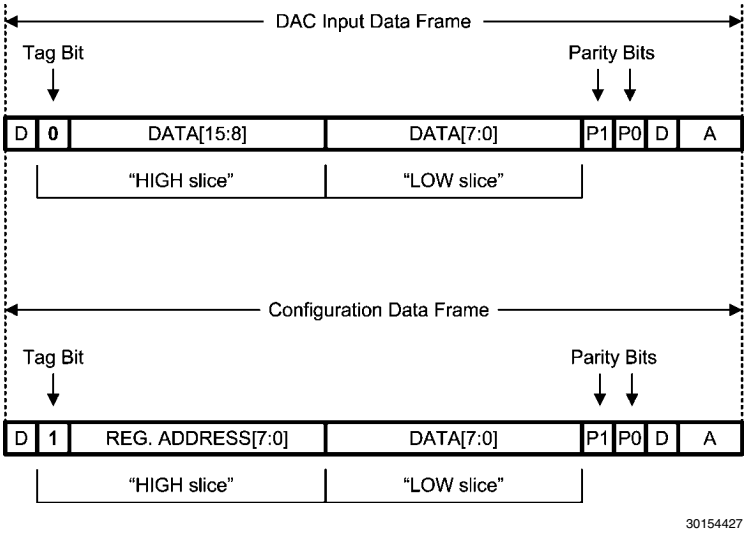
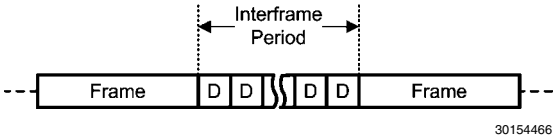


FIGURE 7. Data Frame Format

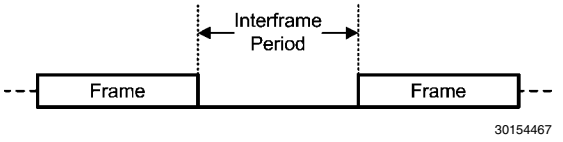
17.2.2 Inter-Frame Period

The fastest DAC update rate is achieved when Master sends the valid frames back to back, Continuous Mode, at the fastest Baud rate. This, however, results in the least power efficient implementation.

SWIF is designed to operate in the Burst Mode as well, where the valid frames are separated by the inter-frame periods that do not carry any data. The inter-frame period can be occupied by a stream of idle 'D' or 'L' symbols.



Sending the 'D' symbol in the inter-frame period provides continuous verification of integrity of the data link. The device by default monitors the activity of the SWIF link, and if the activity ceases the ERRB flag is asserted. See *Section 16.3 CONFIG2: Address=0x02; Default=0x1F* and *Section 17.3 ERROR DETECTION AND REPORTING*.



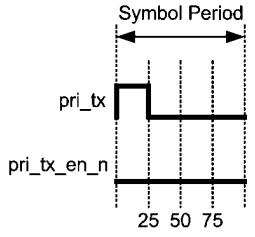
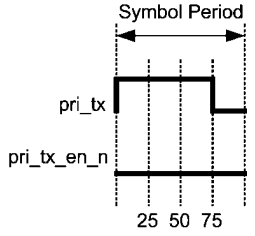
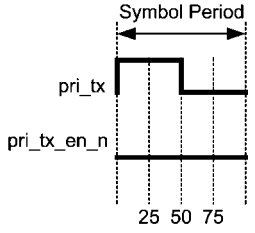
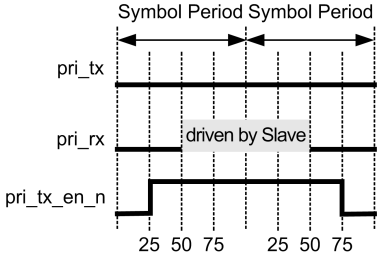
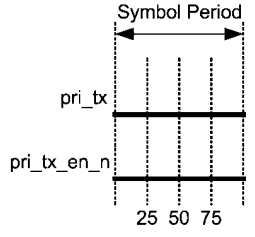
Sending the 'L' in the inter-frame period results in the transmission line being inactive (transition-free) except when the data frames are being transmitted. This is the most power efficient implementation of SWIF link, but it does not facilitate link integrity reporting. To avoid ERRB being asserted due to the channel inactivity, CONFIG2.CHANNEL should be cleared.

17.2.3 Symbol Set

The digital data encoding scheme is outlined in the table below. The signal names in the table correspond to the nodes shown in *Figure 13*.

The signal waveforms due to a random symbol stream are shown in *Figure 8*

TABLE 1. Symbol Set Table

Character Mnemonic	SWIF Symbol	Comments
"0"		— Occupies one symbol period — Transmit from Master only — 25% duty-cycle square waveform — Terminates LOW
"1"		— Occupies one symbol period — Transmit from Master only — 75% duty-cycle square waveform — Terminates LOW
"D"		— Occupies one symbol period — Transmit from Master only — 50% duty-cycle square waveform — Terminates LOW
"A"		— Occupies **two** symbol periods — Master stops driving the SWIF and "listens" for acknowledge pulse from the Slave — Slave pulls ACKB LOW to reverse the direction of data flow through the transformer — Slave's DBACK will drive the SWIF pri_rx line between 50% points of the adjacent periods - in this interval Master must de-assert pri_tx_en_n — Terminates with pri_tx=LOW and pri_tx_en_n=LOW
"L"		— Occupies one symbol period, but can be repeated indefinitely — Transmit from Master only — Always LOW — Does not carry any meaningful information — Used as an inter-frame symbol, i.e., sent by the Master between valid data frames

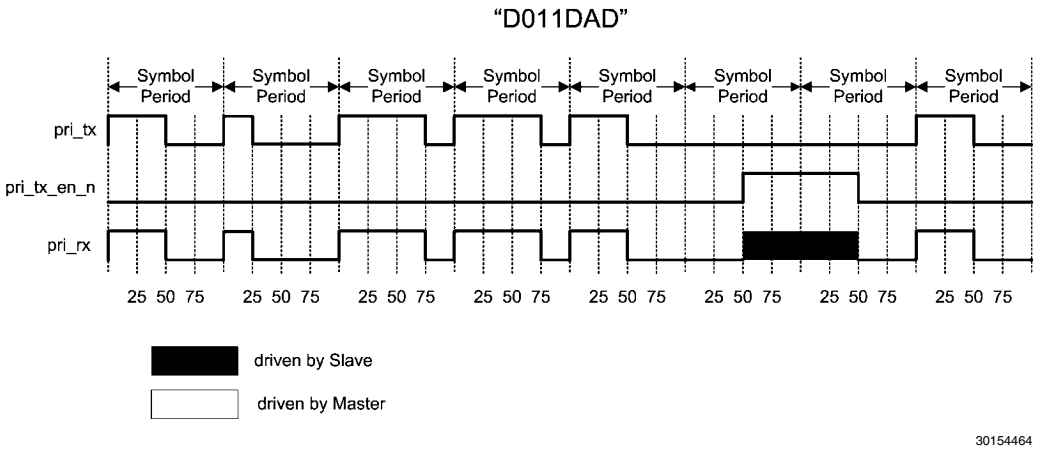


FIGURE 8. Symbol stream example

17.2.4 Interface Circuit

SWIF interface components are shown in *Figure 9*. The buffers A and B comprise a square waveform recovery circuit in applications where a pulse transformer is used to cross the galvanic isolation boundary, see *Section 17.2.4.1 Transformer Coupled Interface - Data Flow to the DAC*. The ACKB output and its internal NMOS switch provide the means of reversing the direction of data flow through the coupling transformer see *Section 17.2.4.2 Transformer Coupled Interface - Acknowledge Pulse*. In simple cases where the data link is DC coupled buffer A alone acts as a data receiver. The buffer C is provided for cases where improved noise immunity is required, see *Section 17.2.4.3 DC-Coupled Interface*.

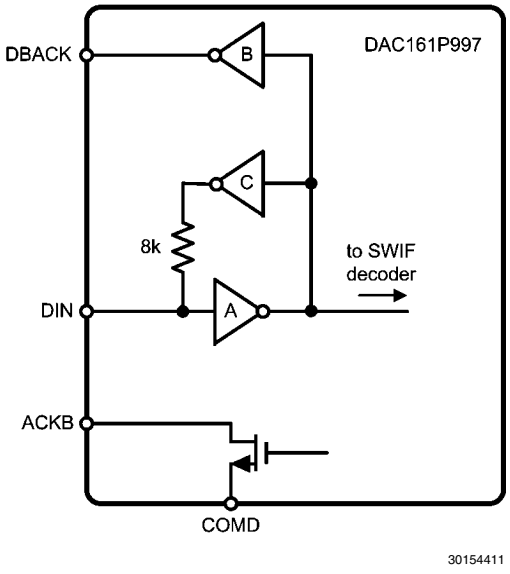


FIGURE 9. SWIF Front End

17.2.4.1 Transformer Coupled Interface - Data Flow to the DAC

In systems requiring galvanic isolation between the transmitter (micro-controller) and the receiver, the commonly used coupling element is a pulse transformer. Transformer passes only the AC components of the square input waveform resulting in an impulse train across the secondary winding. Buffers A and B form a latch circuit around the secondary winding that recovers the square waveform from the impulse train.

Figure 10 shows the details of the square waveform transmission from the primary side and recovery of the signal on the secondary side. Transmitter's DC component is blocked by the capacitor CP. The transmitter's output waveform VO results in the impulse train VP across the primary winding. Similar impulse train then appears across the secondary winding. If the magnitude of the impulse exceeds the threshold on the A buffer, the latch formed by A and B buffers will change state. The new latch state will persist until an opposite polarity impulse appears across the secondary winding.

Note that in *Figure 10* the capacitor CS bottom plate floats, and thus does not affect the operation of this circuit.

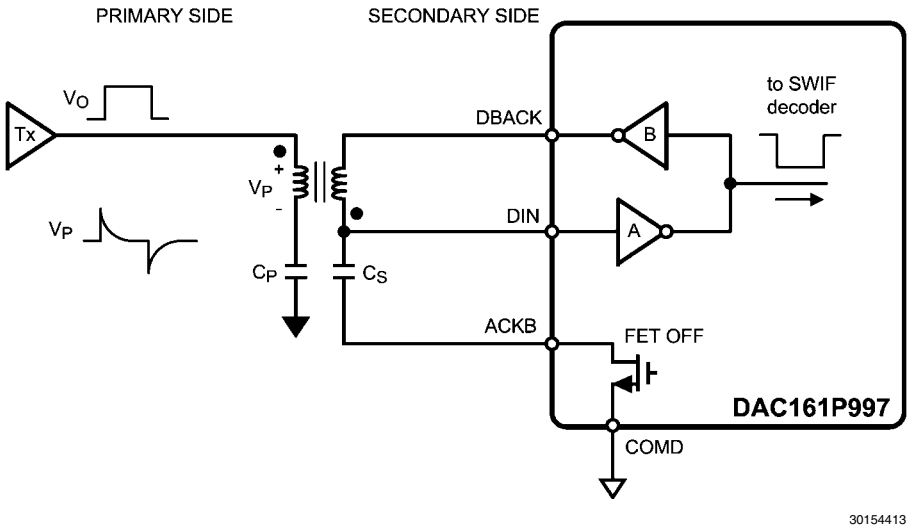


FIGURE 10. Transformer coupled SWIF link with the DAC161P997 as Receiver

17.2.4.2 Transformer Coupled Interface - Acknowledge Pulse

Since the transformer is a symmetrical device (particularly one with 1:1 winding ratio), it is simple to reverse the data flow through it.

Figure 11 shows the SWIF interface circuit during the transmission of the Acknowledge pulse from the DAC161P997 on the secondary side back to the micro-controller on the primary side.

On the secondary side buffer B drives the square waveform across the transformer. Capacitor CS, whose bottom plate is now grounded via the ACKB pin, blocks the DC component of the square waveform. Buffer A is inactive.

On the primary side a square waveform recovery is performed by the now familiar latch.

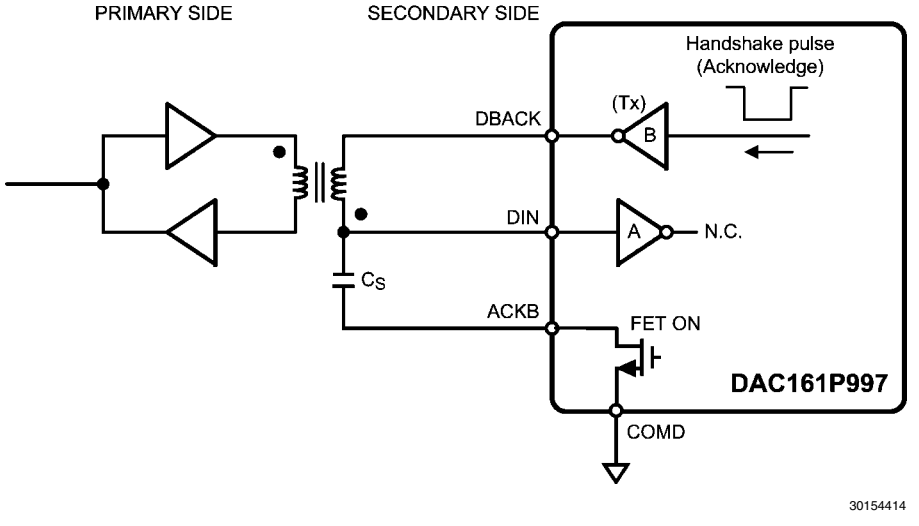


FIGURE 11. Transformer coupled SWIF link with the DAC161P997 as transmitter

17.2.4.3 DC-Coupled Interface

DC coupled signal path between the transmitter and the receiver is shown in *Figure 12*. Such circuit as the internal buffer A is sufficient for the signal recovery as the signal presented at the DIN input is a square CMOS level waveform.

In noisy environments it may be necessary to implement a Hysteresis loop around the DIN input to improve noise immunity of the input circuit. Presence of the buffer C and its output resistor facilitate this. The Hysteresis can be easily realized by inserting R_{IN} between the transmitter and DIN input.

Note that when R_{IN}=0 the presence of the buffer C can be ignored.

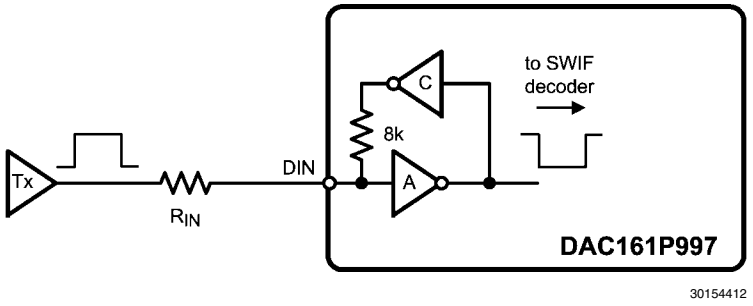


FIGURE 12. DC-Coupled SWIF Input

17.2.4.4 SWIF Implementation Examples

An example of implementation of the SWIF data link is shown in the figure below. This implementation uses the components already present in the systems employing the standard methods for PWM signal transmission over an isolation boundary. In this example Master uses 2 digital I/Os:

- One bidirectional port for transmitting encoded data to, and receiving the acknowledge signal from the slave – pri_tx/pri_rx.
- One output sourcing the pri_tx_en_n signal that governs the direction of the data flow over the SWIF link.

While transmitting, Master drives the pri_tx_en_n LOW and sources data stream onto the pri_tx. The circuit path is through buffer 'a', transformer primary winding, DC blocking capacitor to GND.

While receiving, Master drives the pri_tx_en_n HIGH and 'listens' for acknowledge signal pri_rx. In this mode the buffers 'a' and 'b' form the latch around the transformer winding, and buffer 'c' floats the DC blocking capacitor.

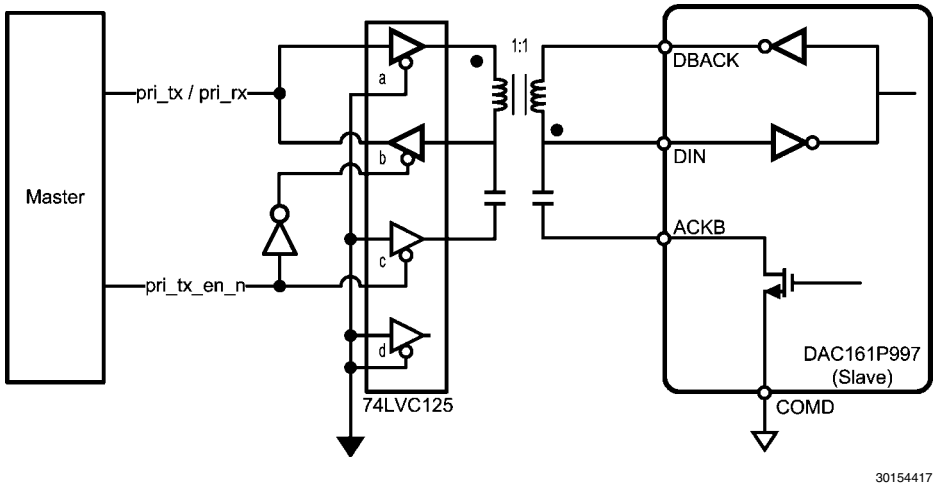


FIGURE 13. Typical SWIF implementation

The interface implementation shown in *Figure 13* can be expanded or simplified depending on the requirements of the system and capabilities of the Master controller. A number of other possible implementations are shown in the figures below.

Figure 14 shows the circuit analogous in its functionality to the circuit in *Figure 13* but with fewer active components. Here instead of disabling 'b' buffer during data transmission, its output impedance is increased to the point where its drive is significant only during the data reception form the Slave.

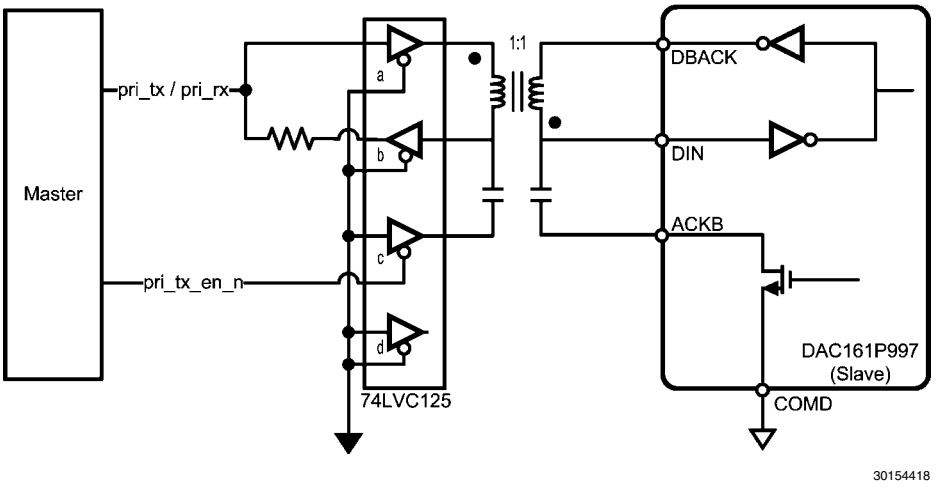


FIGURE 14. SWIF Link with Simplified Control

Figure 15 shows the SWIF link circuit when the Master does not have a bidirectional I/O available. The Master output driving pri_tx is split away from the Master receiving pri_rx input by using a buffer 'd', until now unused, on 74LVC125.

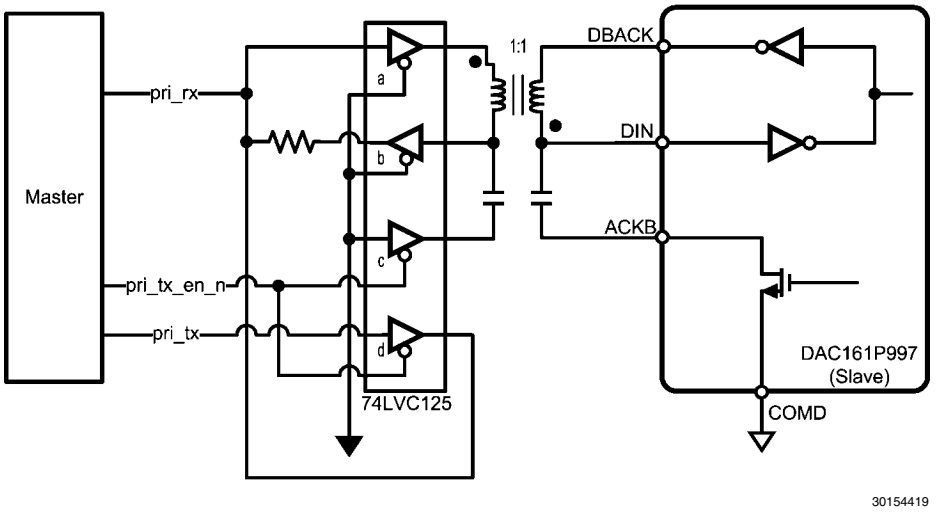


FIGURE 15. Master without Bidirectional I/O

Figure 16 shows the trivial circuit realization of the SWIF link in simplex mode, unidirectional data flow.

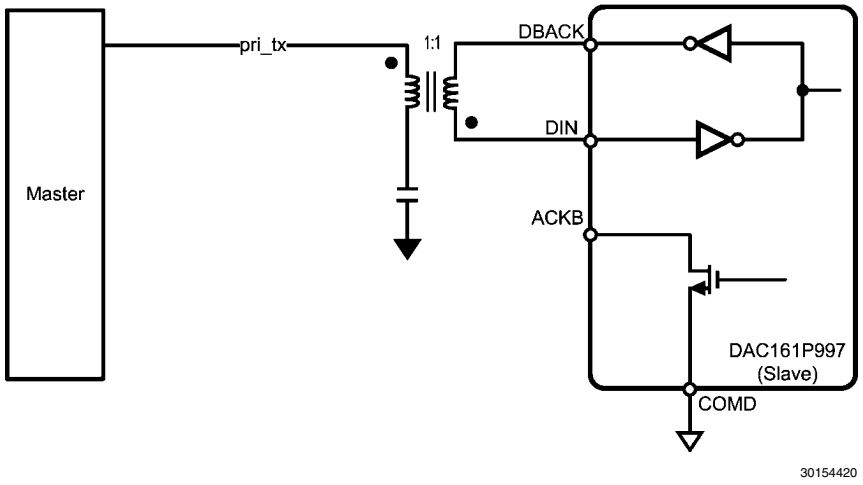


FIGURE 16. SWIF without Acknowledge Capability

Figure 17 shows the DC coupled SWIF link realization. In this example ACKB output is used to generate the Acknowledge pulse. This is equivalent to the Acknowledge pulse generated at DBACK, since in transformer coupled application both ACKB and DBACK have to be pulsed to transmit back to the Master. Note that the pulse generated by ACKB is active LOW.

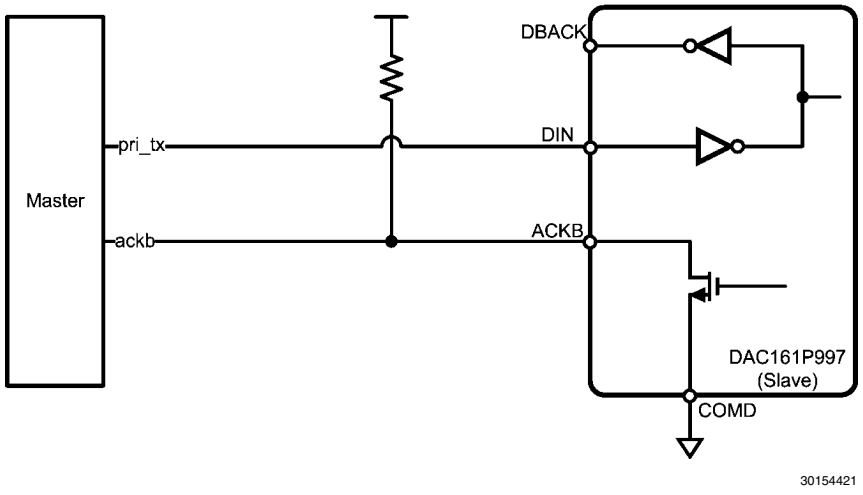


FIGURE 17. DC-Coupled SWIF Link

The SWIF link realization using opto-couplers (opto-isolators) is shown in *Figure 18*. Points of note here are: the opto-couplers invert the SWIF symbol waveform, and there is increased power consumption due to the relatively large currents required to turn on the internal diodes and standing current in the pull-up resistors.

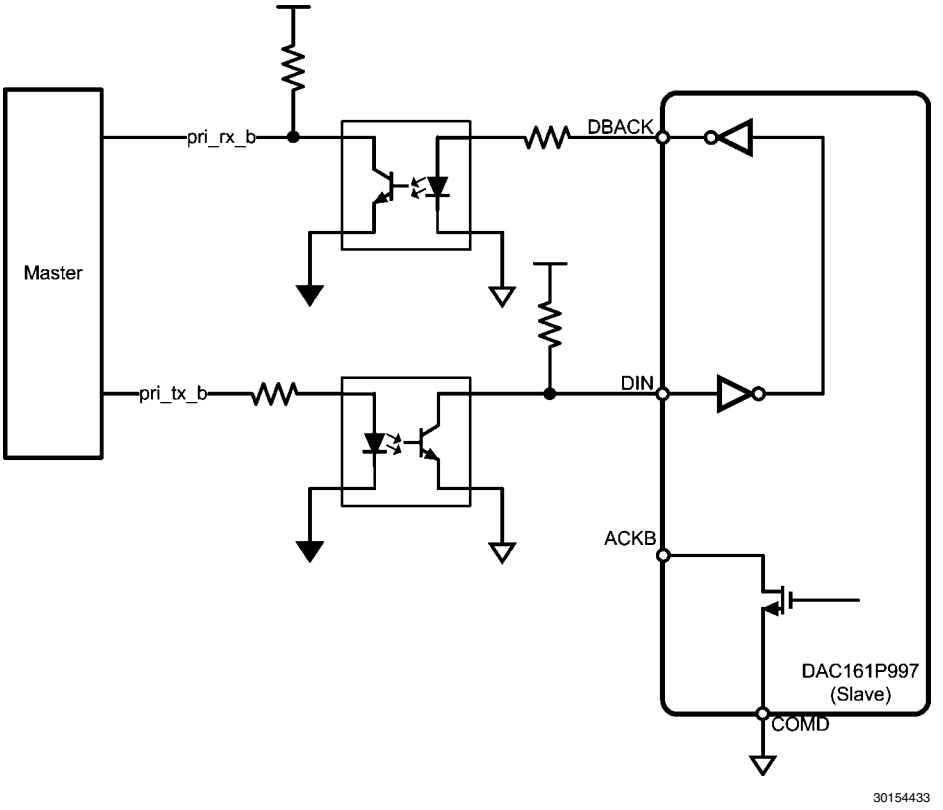


FIGURE 18. SWIF Link Realized with Octo-couplers

17.2.4.5 Transformer Selection and SWIF Data Link Circuit Design

In general, the transformers developed for T1/E1 telecom applications are well suited as the interface element for the DAC161P997 in the galvanically isolated industrial transmitter. The application circuit schematic utilizing T1/E1 transformer as the isolation element is shown in *Section 18.0 Application Circuit Examples*. A number of suggested off the shelf transformers are listed in *Table 2*.

TABLE 2. Examples of Transformers Suitable in the DAC161P997 Applications

Manuf	P/N	LM (mH)	LLP/S (µH)	RP/S (O)	CWW (pF)	Isolation Voltage (Vrms)
Pulse	TX1491	1.2	1.2	2.7	35	1500
Coilcraft	S5394–CLB	0.4	Not Specified	0.95	0.92	1500
Halo	TG02-1205	1.2	Not Specified	0.7	30	1500
XFMRS	XF7856-GD11	0.785	0.5	0.52	Not Specified	1500

Model suitable for simulating the behavior of the pulse transformer is shown in *Figure 19*. The model parameters are readily available in the datasheets provided by the transformer manufacturers, see *Table 2* for examples.

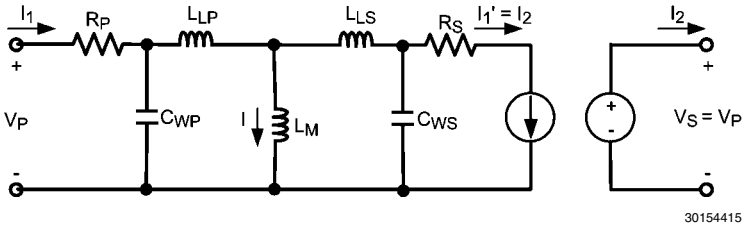


FIGURE 19. Pulse Transformer Model - Winding Ratio 1:1

TABLE 3. Transformer Model Parameters' Legend

Parameter	Description
L_M	Magnetizing inductance, in Data Sheets shown as OCL (open circuit inductance)
$L_{LP/S}$	Leakage inductance of the primary (secondary) winding
$C_{WP/S}$	Winding capacitance. Dominated by the CWW (winding to winding) component. Here it is assumed that CWS=CWP=½CWW
$R_{P/S}$	Winding resistance

The circuit behavior will be dominated by the DC blocking capacitance C_P and the magnetizing inductance L_M. In the example circuit shown in *Figure 20* the rising edge of VO ultimately results in an impulse at the input DIN, see *Figure 21*. Once voltage at DIN is above VIH of the A buffer, the A buffer will change its state. However, the latch will acquire a new state only if the voltage at DIN persists above VIH for T_{PEAK} > TD.

The parasitic elements in the transformer model: L_{LS}, L_{SP}, C_{WS}, C_{WP} may result in the oscillating component superimposed on the dominant impulse response waveform shown in *Figure 21*. The oscillation should be controlled so that the condition T_{PEAK}> TD is maintained. The typical method for controlling this parasitic oscillation is to insert a damping element into the signal path. A small resistance in series with transformer winding is such damping element. The typical application example in *Section 18.0 Application Circuit Examples* illustrates this.

The delay around the SWIF input latch, from DIN to DBACK, TD is specified in*Section 13.0 Electrical Characteristics* .

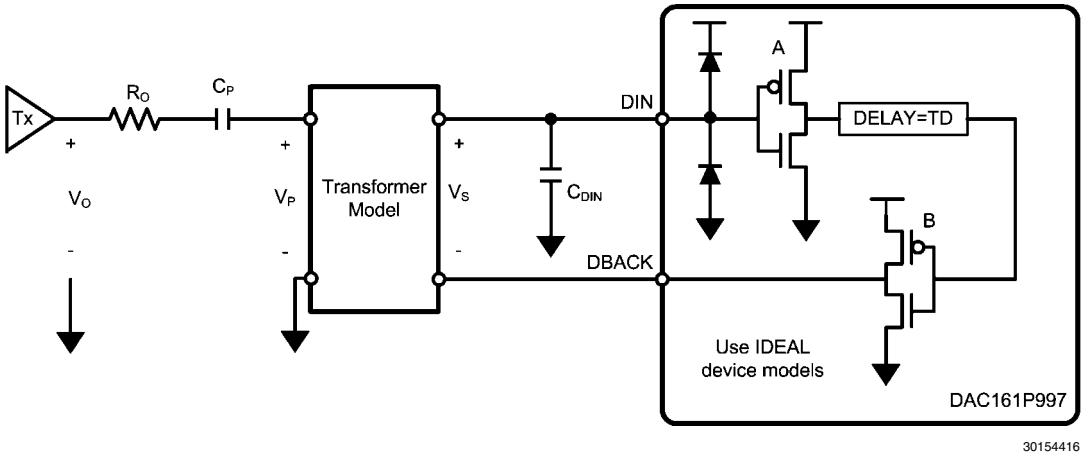


FIGURE 20. NRZ Waveform Transmission and Recovery Circuit Model

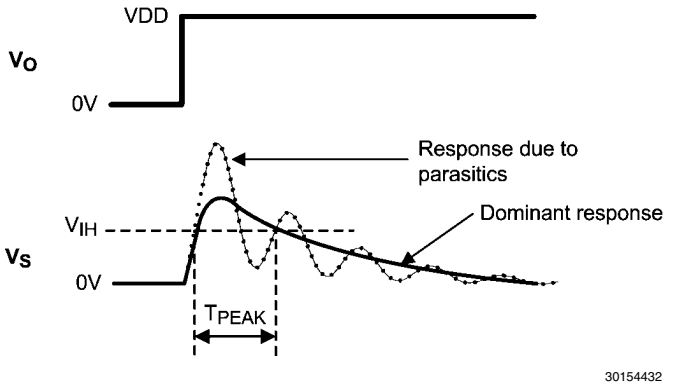


FIGURE 21. SWIF Link Circuit Response to Step Input

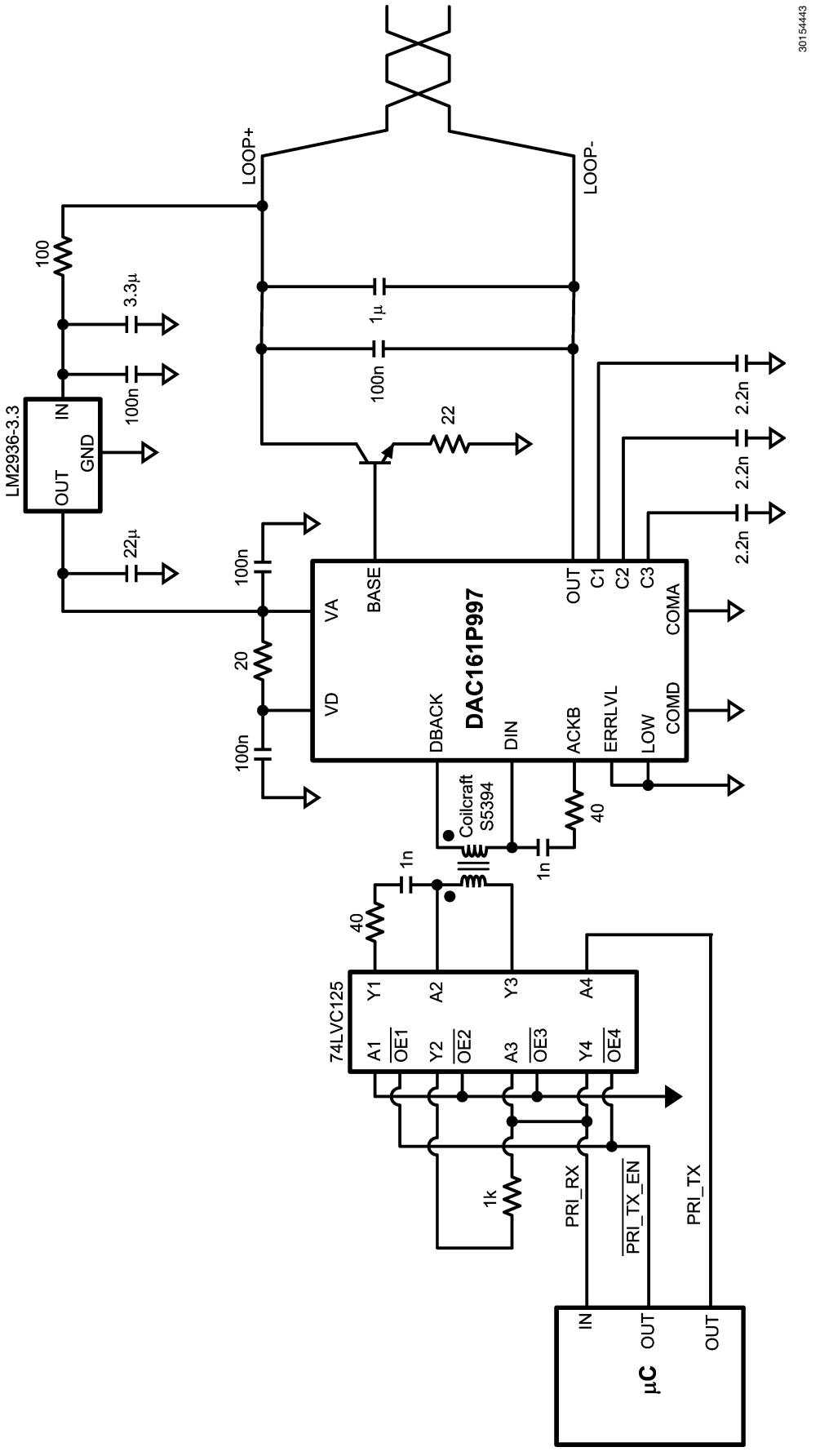
17.3 ERROR DETECTION AND REPORTING

The user can modify the CONFIG2:(LOOP | CHANNEL | PARITY | FRAME) bits to mask or enable the reporting of any of the detectable fault conditions. The DAC161P997 reports errors by asserting the ERRB signal, and by setting the current sourced by OUT to a value dictated by the state at ERRLVL pin and the contents of the ERR_HIGH and ERR_LOW registers. Once the condition causing the fault is removed the OUT will return to the last valid output level prior to the occurrence of the fault.

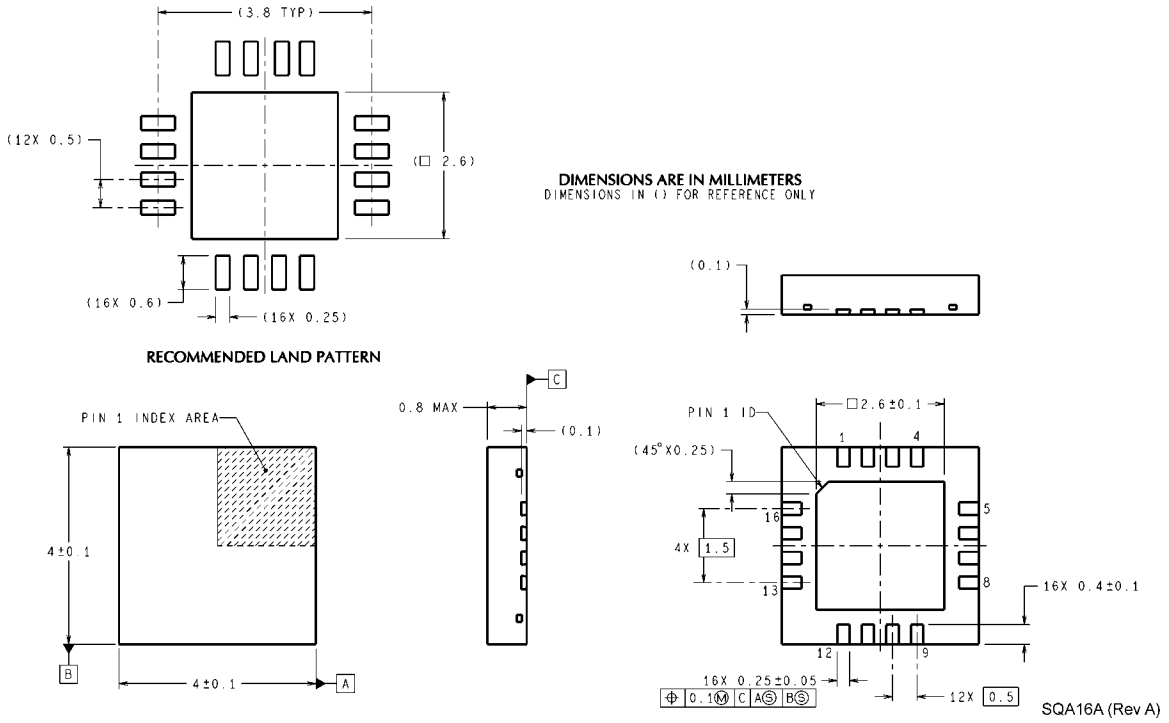
Table below summarizes the detectable faults, and means of reporting. The interval TM is governed by the internal timer and is specified in *Section 13.0 Electrical Characteristics* .

ERROR	CAUSE	REPORTING	
		ERRB	Value used by the DAC to set OUT pin current
LOOP	The device cannot sustain the required output current at OUT pin, typically caused by drop in loop supply, or increased load impedance. The DAC161P997 automatically clears this fault after interval of TM and attempts to establish output current dictated by the value in the DACCODE register	LOW	ERR_LOW
CHANNEL	no valid symbols have been received on DIN in last interval of TM	LOW	ERRLVL=1: ERR_HIGH ERRLVL=0: ERR_LOW
PARITY	SWIF received a valid data frame, but a bit error has been detected by parity check	LOW	ERRLVL=1: ERR_HIGH ERRLVL=0: ERR_LOW
FRAME	invalid symbol received, or an incorrect number of valid symbols were detected in the frame	LOW	ERRLVL=1: ERR_HIGH ERRLVL=0: ERR_LOW

18.0 Application Circuit Examples



19.0 Physical Dimensions inches (millimeters) unless otherwise noted



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Notes

Notes

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