RQK2001HQDQA

Silicon N Channel MOS FET
Power Switching

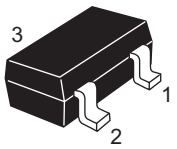
R07DS0311EJ0200
(Previous: REJ03G1731-0100)
Rev.2.00
Mar 28, 2011

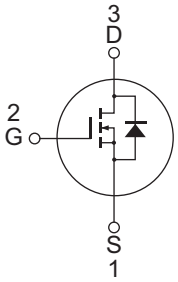
Features

- High drain to source voltage and Low gate drive
  V_{DSS} : 200 V and V_{GSS} : ±30 V
- Low drive current
- High speed switching
- Small traditional package (MPAK)

Outline

RENESAS Package code: PLSP0003ZB-A
(Package name: MPAK)





1. Source
2. Gate
3. Drain

Note: Marking is "HQ".

Absolute Maximum Ratings

(Ta = 25°C)

Item	Symbol	Ratings	Unit
Drain to source voltage	V_{DSS}	200	V
Gate to source voltage	V_{GSS}	±30	V
Drain current	I_D	0.4	A
Drain peak current	$I_{D(pulse)}$ Note1	1.6	A
Body - drain diode reverse drain current	I_{DR}	0.4	A
Channel dissipation	Pch Note2	0.8	W
Thermal resistance	Rth(ch-a) Note2	156	°C / W
Channel temperature	Tch	150	°C
Storage temperature	Tstg	–55 to +150	°C

Notes: 1. PW ≤ 10 µs, Duty cycle ≤ 1%
2. When using the glass epoxy board (FR-4 40 × 40 × 1 mm)

Electrical Characteristics

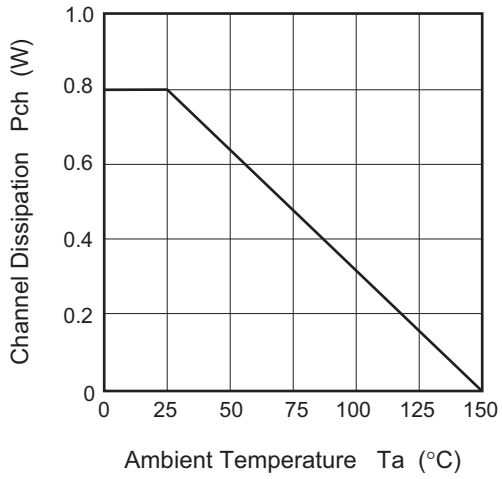
(Ta = 25°C)

Item	Symbol	Min	Typ	Max	Unit	Test conditions
Drain to source breakdown voltage	$V_{(BR)DSS}$	200	—	—	V	I_D = 10 mA, V_{GS} = 0
Gate to source leak current	I_{GSS}	—	—	+0.1	µA	V_{GS} = +30 V, V_{DS} = 0
Gate to source leak current	I_{GSS}	—	—	–0.1	µA	V_{GS} = –30 V, V_{DS} = 0
Zero gate voltage drain current	I_{DSS}	—	—	1	µA	V_{DS} = 200 V, V_{GS} = 0
Gate to source cutoff voltage	$V_{GS(off)}$	3	—	4.5	V	V_{DS} = 10 V, I_D = 1 mA
Drain to source on state resistance	$R_{DS(on)}$	—	5.0	6.7	Ω	I_D = 0.15 A, V_{GS} =10 V [Note3]
Forward transfer admittance	$\|y_{fs}\|$	0.2	0.3	—	S	I_D = 0.15 A, V_{DS} = 10 V [Note3]
Input capacitance	Ciss	—	30	—	pF	V_{DS} = 25 V V_{GS} = 0 f = 1 MHz
Output capacitance	Coss	—	5	—	pF	
Reverse transfer capacitance	Crss	—	2	—	pF	
Turn - on delay time	$t_{d(on)}$	—	13	—	ns	I_D = 0.15 A V_{GS} = 10 V R_L = 667 Ω Rg = 50 Ω
Rise time	t_r	—	12	—	ns	
Turn - off delay time	$t_{d(off)}$	—	42	—	ns	
Fall time	t_f	—	38	—	ns	
Total gate charge	Qg	—	1.8	—	nC	V_{DD} = 100 V V_{GS} = 10 V I_D = 0.4 A
Gate to Source charge	Qgs	—	0.4	—	nC	
Gate to drain charge	Qgd	—	0.9	—	nC	
Body - drain diode forward voltage	V_{DF}	—	0.8	1.2	V	I_F = 0.4 A, V_{GS} = 0 [Note3]

Notes: 3. Pulse test

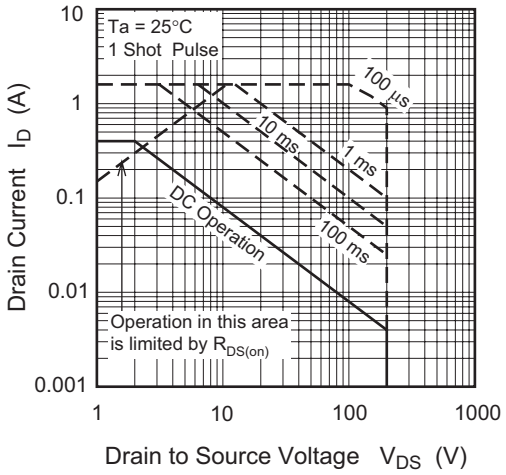
Main Characteristics

Maximum Channel Power Dissipation Curve

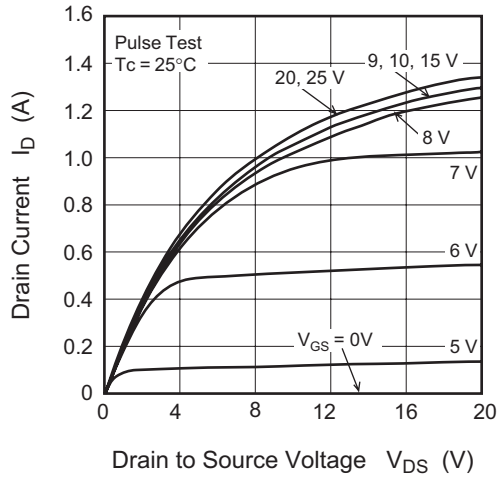


*When using the glass epoxy board (FR-4 40 x 40 x 1 mm)

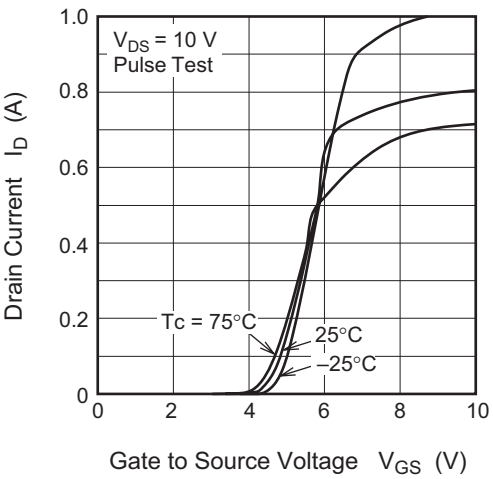
Maximum Safe Operation Area



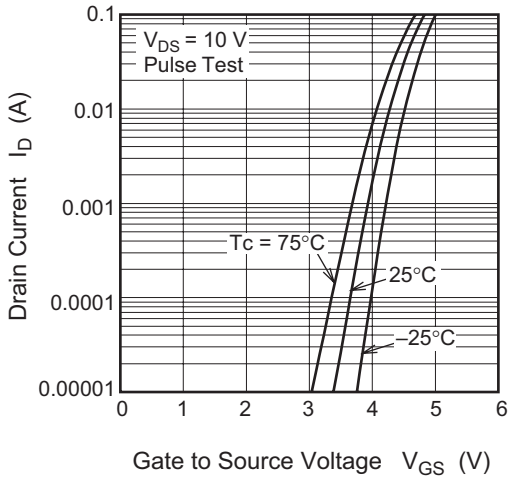
Typical Output Characteristics



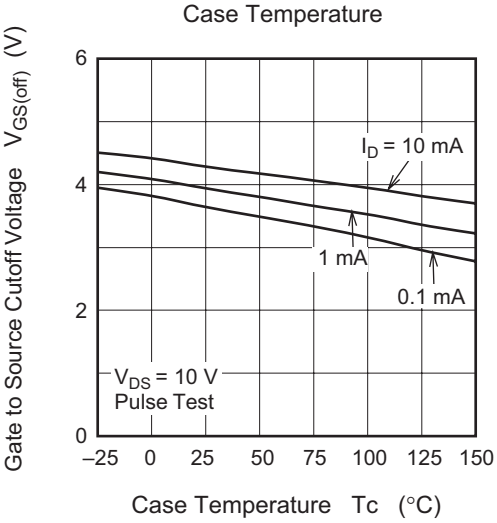
Typical Transfer Characteristics (1)



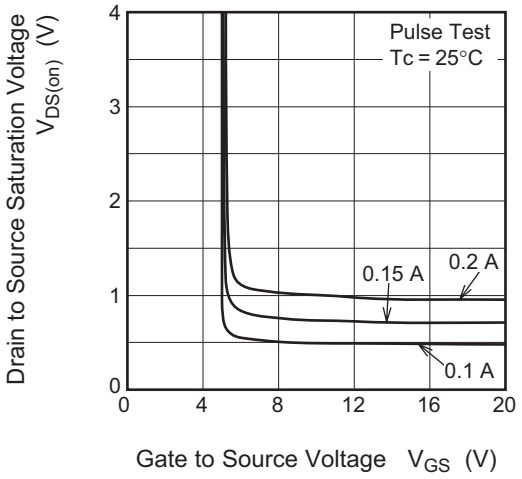
Typical Transfer Characteristics (2)



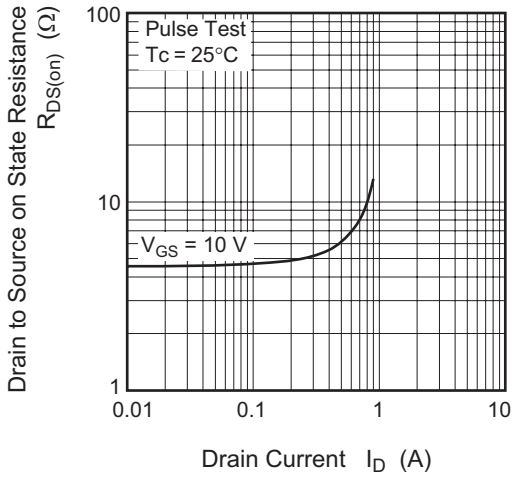
Gate to Source Cutoff Voltage vs. Case Temperature



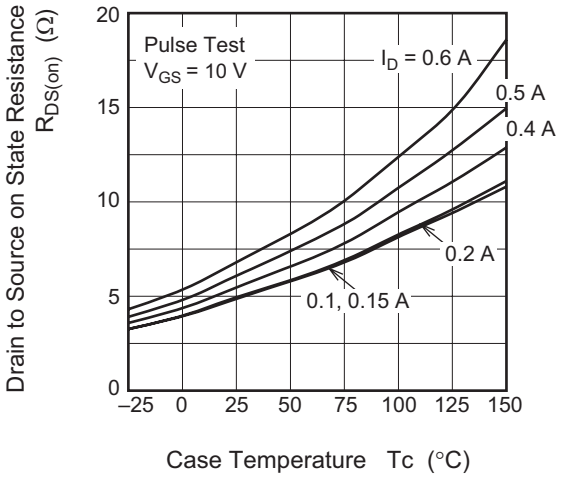
Drain to Source Saturation Voltage vs. Gate to Source Voltage



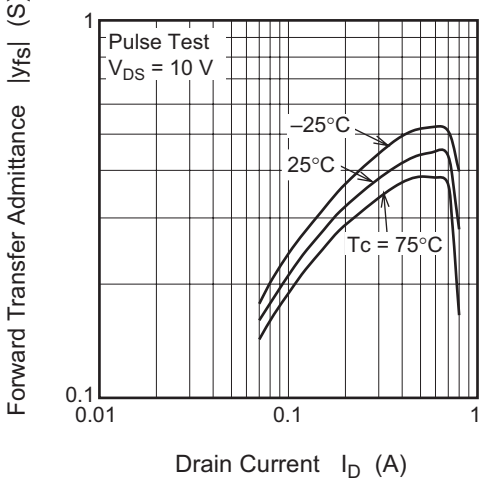
Static Drain to Source on State Resistance vs. Drain Current



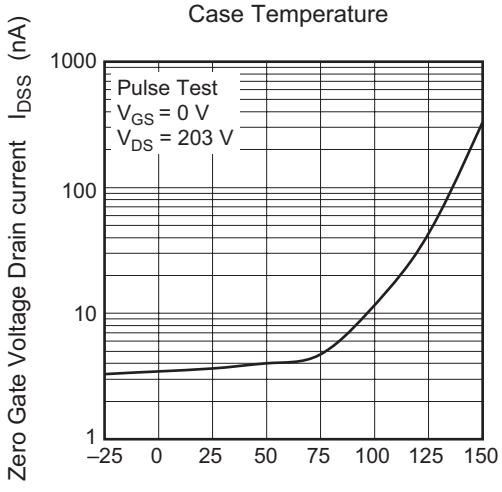
Static Drain to Source on State Resistance vs. Case Temperature (1)



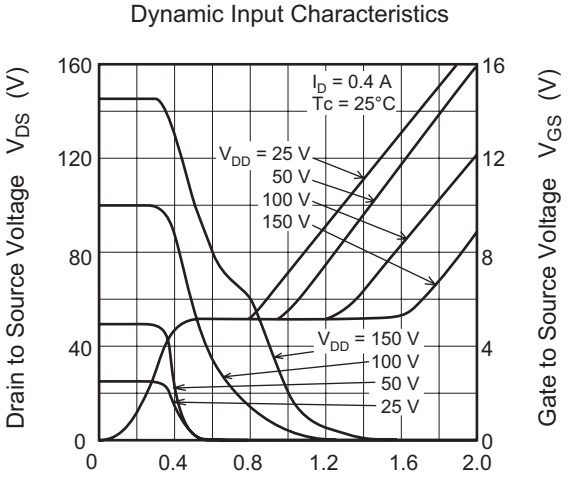
Forward Transfer Admittance vs. Drain Current



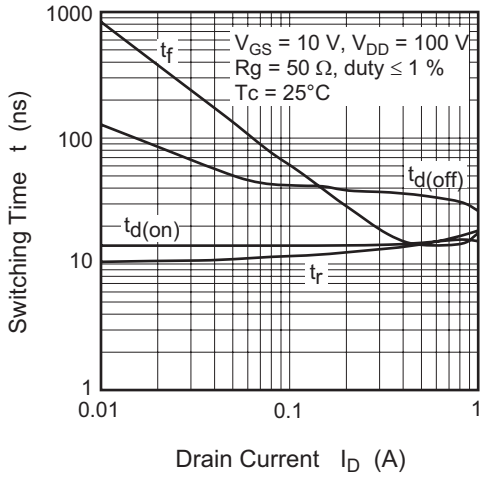
Zero Gate Voltage Drain current vs. Case Temperature



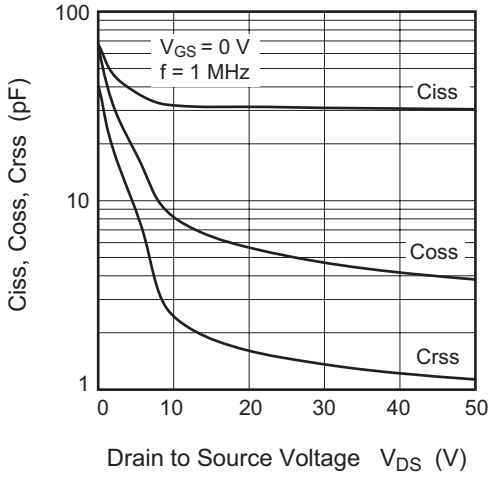
Dynamic Input Characteristics



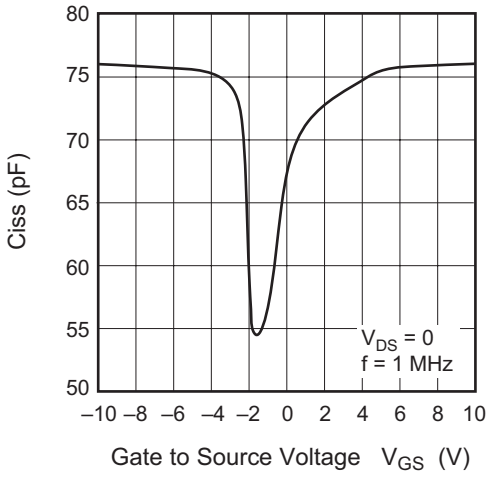
Switching Characteristics



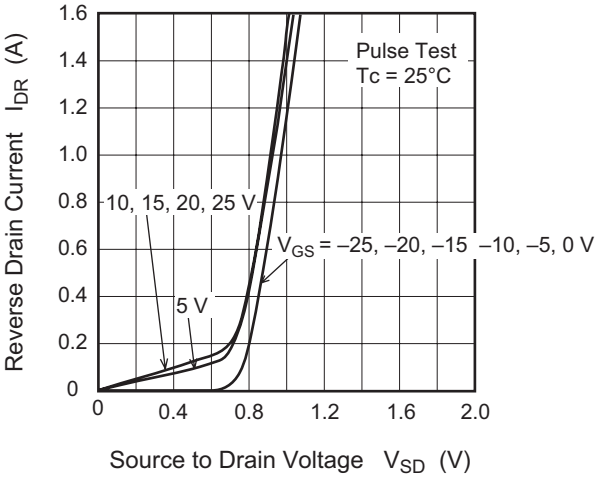
Typical Capacitance vs. Drain to Source Voltage



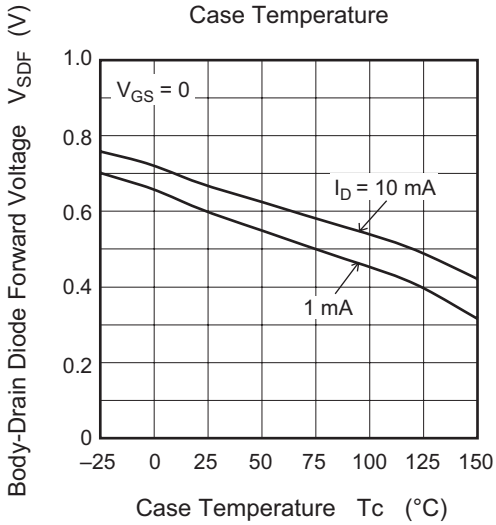
Input Capacitance vs. Gate to Source Voltage



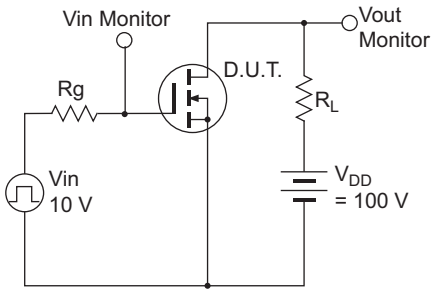
Reverse Drain Current vs. Source to Drain Voltage



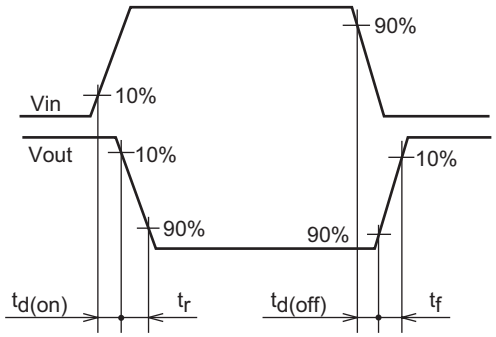
Body-Drain Diode Forward Voltage vs. Case Temperature



Switching Time Test Circuit

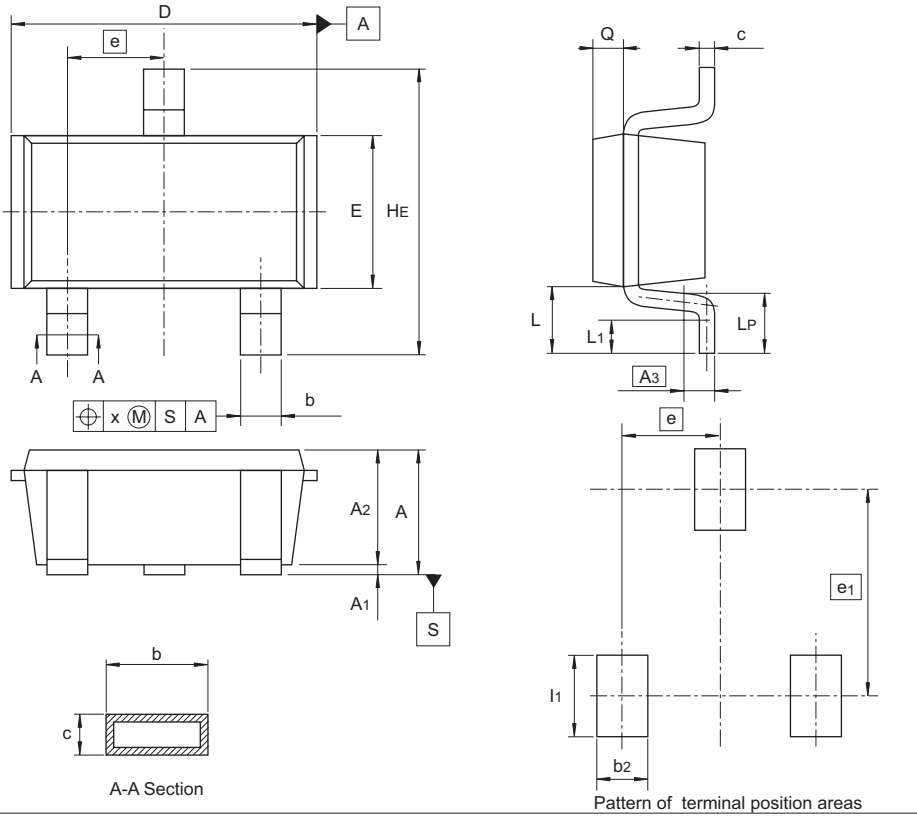


Switching Time Waveform



Package Dimensions

Package Name	JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]
MPAK	SC-59A	PLSP0003ZB-A	MPAK(T) / MPAK(T)V	0.011g



Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
A	1.0	–	1.3
A_1	0	–	0.1
A_2	1.0	1.1	1.2
A_3	–	0.25	–
b	0.35	0.4	0.5
c	0.1	0.16	0.26
D	2.7	–	3.1
E	1.35	1.5	1.65
e	–	0.95	–
H_E	2.2	2.8	3.0
L	0.35	–	0.75
L_1	0.15	–	0.55
L_P	0.25	–	0.65
x	–	–	0.05
b_2	–	–	0.55
e_1	–	1.95	–
l_1	–	–	1.05
Q	–	0.3	–

Ordering Information

Orderable Part Number	Quantity	Shipping Container
RQK2001HQDQATL-H	3000 pcs.	ϕ178 mm reel, 8 mm Emboss taping

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