LM3075

LM3075 High Efficiency, Synchronous Current Mode Buck Controller

Literature Number: SNVS398
**LM3075**

**High Efficiency, Synchronous Current Mode Buck Controller**

**General Description**

The LM3075 is a current mode control, synchronous buck controller IC. Use of synchronous rectification and pulse-skipping operation at light load achieves high efficiency over a wide load range. Fixed frequency operation can be obtained by disabling the pulse-skipping mode. Current mode control assures excellent line and load regulation and a wide loop bandwidth for fast response to load transients.

Current mode control can be achieved by either sensing across the high side NFET or a sense resistor. The switching frequency can be selected as either 200 kHz or 300 kHz from an internal clock.

The LM3075 is available with an adjustable output in a TSSOP-20 package.

**Features**

- Input voltage range of 4.5V-36V
- Current Mode Control
- Skip mode operation available
- Cycle by cycle current limit
- 1.24V ±2% Reference

**Applications**

- Automotive Power Supplies
- Distributed Power Systems

---

**Typical Application Circuit**

![Typical Application Circuit Diagram](image-url)
Connection Diagram

TOP VIEW

Ordering Information

<table>
<thead>
<tr>
<th>Order Number</th>
<th>Package Type</th>
<th>NSC Package Drawing</th>
<th>Supplied As</th>
</tr>
</thead>
<tbody>
<tr>
<td>LM3075MTC</td>
<td>TSSOP-20</td>
<td>MTC-20</td>
<td>73 Units per Anti-Static Tube</td>
</tr>
<tr>
<td>LM3075MTCX</td>
<td>TSSOP-20</td>
<td>MTC-20</td>
<td>2500 Units on Tape and Reel</td>
</tr>
</tbody>
</table>

Pin Descriptions

<table>
<thead>
<tr>
<th>LM3075 Pin #</th>
<th>Name</th>
<th>Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>VLIN5</td>
<td>5V linear regulator output</td>
</tr>
<tr>
<td>2</td>
<td>VIN</td>
<td>Input voltage supply</td>
</tr>
<tr>
<td>3</td>
<td>EXT</td>
<td>External power connection for VLIN5</td>
</tr>
<tr>
<td>4</td>
<td>FS</td>
<td>Frequency select</td>
</tr>
<tr>
<td>5</td>
<td>EN</td>
<td>Enable pin</td>
</tr>
<tr>
<td>6</td>
<td>FB</td>
<td>Feedback pin</td>
</tr>
<tr>
<td>7</td>
<td>FPWM</td>
<td>Forced PWM selection</td>
</tr>
<tr>
<td>8</td>
<td>COMP</td>
<td>Compensation pin</td>
</tr>
<tr>
<td>9</td>
<td>SS</td>
<td>Output enable / soft-start pin</td>
</tr>
<tr>
<td>10</td>
<td>AGND</td>
<td>Analog ground</td>
</tr>
<tr>
<td>11</td>
<td>PGND</td>
<td>Power ground</td>
</tr>
<tr>
<td>12</td>
<td>LDRV</td>
<td>Low side gate drive</td>
</tr>
<tr>
<td>13</td>
<td>VDD</td>
<td>Low side gate drive supply</td>
</tr>
<tr>
<td>14</td>
<td>CBOOT</td>
<td>Bootstrap capacitor connection</td>
</tr>
<tr>
<td>15</td>
<td>HDRV</td>
<td>High side gate drive</td>
</tr>
<tr>
<td>16</td>
<td>SW</td>
<td>Switch node</td>
</tr>
<tr>
<td>17</td>
<td>CSL</td>
<td>Current sense low</td>
</tr>
<tr>
<td>18</td>
<td>CSH</td>
<td>Current sense high</td>
</tr>
<tr>
<td>19</td>
<td>ILIM</td>
<td>Current limit threshold adjustment</td>
</tr>
<tr>
<td>20</td>
<td>PGOOD</td>
<td>Power good flag</td>
</tr>
</tbody>
</table>
**Absolute Maximum Ratings** *(Note 1)*

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Volatges from the indicated pins to GND:
- VIN, ILIM, CSH: −0.3V to 38V
- SW, CSL: −0.3 to (VIN + 0.3V)
- PGOOD, FB, VDD, EXT, EN: −0.3V to +7V
- COMP, SS, FPWM, FS: −0.3V to (VLIN5 + 0.3)V
- CBOOT: −0.3V to +43V
- CBOOT to SW: −0.3V to 7V
- LDRV: −0.3V to (VDD + 0.3V)
- HDRV to SW: −0.3V
- HDRV to CBOOT: +0.3V
- Storage Temperature Range: −65˚C to +150˚C
- Junction Temperature: 150˚C
- Lead Temperature (Soldering, 10 sec): 260˚C
- ESD Rating (Note 2): 1.5kV

**Junction Temperature:** −40˚C to +125˚C

**VIN to GND:** 4.5V to 36V

**EXT:** 6V Max

**Operating Ratings** *(Note 1)*

**Electrical Characteristics** Limits in standard type are for T<sub>J</sub> = 25˚C only, and limits in boldface type apply over the junction temperature T<sub>J</sub> range of -40˚C to +125˚C. Minimum and Maximum limits are guaranteed through test, design, or statistical correlation. Typical values represent the most likely parametric norm at T<sub>J</sub> = 25˚C, and are provided for reference purposes only. Unless otherwise specified V<sub>IN</sub> = 12V.

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Conditions</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>V&lt;sub&gt;FB&lt;/sub&gt;</td>
<td>Feedback pin voltage</td>
<td>V&lt;sub&gt;IN&lt;/sub&gt; = 4.5V to 36V</td>
<td>1.213</td>
<td>1.238</td>
<td>1.259</td>
<td>V</td>
</tr>
<tr>
<td>ΔV&lt;sub&gt;OUT&lt;/sub&gt;/ΔV&lt;sub&gt;IN&lt;/sub&gt;</td>
<td>Load Regulation</td>
<td>V&lt;sub&gt;COMP&lt;/sub&gt; = 0.5V to 1.5V</td>
<td>0.04</td>
<td>%</td>
<td></td>
<td></td>
</tr>
<tr>
<td>ΔV&lt;sub&gt;OUT&lt;/sub&gt;/ΔI&lt;sub&gt;IN&lt;/sub&gt;</td>
<td>Line Regulation</td>
<td>V&lt;sub&gt;IN&lt;/sub&gt; = 4.5V to 36V</td>
<td>0.04</td>
<td>%</td>
<td></td>
<td></td>
</tr>
<tr>
<td>I&lt;sub&gt;Q&lt;/sub&gt;</td>
<td>Operating Quiescent current</td>
<td>V&lt;sub&gt;IN&lt;/sub&gt; = 4.5V to 36V</td>
<td>1.0</td>
<td>2</td>
<td></td>
<td>mA</td>
</tr>
<tr>
<td>I&lt;sub&gt;SD&lt;/sub&gt;</td>
<td>Shutdown Quiescent current</td>
<td>V&lt;sub&gt;EN&lt;/sub&gt; = 0V</td>
<td>60</td>
<td>100</td>
<td></td>
<td>µA</td>
</tr>
<tr>
<td>V&lt;sub&gt;LINE&lt;/sub&gt;</td>
<td>V&lt;sub&gt;LINE&lt;/sub&gt; Output Voltage</td>
<td>V&lt;sub&gt;LINE&lt;/sub&gt; = 0 to 25mA</td>
<td>4.7</td>
<td>5</td>
<td>5.3</td>
<td>V</td>
</tr>
<tr>
<td>V&lt;sub&gt;UL&lt;/sub&gt;</td>
<td>V&lt;sub&gt;UL&lt;/sub&gt; Under Voltage</td>
<td></td>
<td>3.7</td>
<td>3.9</td>
<td>4.1</td>
<td>V</td>
</tr>
<tr>
<td>V&lt;sub&gt;UL&lt;/sub&gt;_HYS</td>
<td>V&lt;sub&gt;UL&lt;/sub&gt; Under Voltage Lockout Hysteresis</td>
<td></td>
<td>0.2</td>
<td></td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>V&lt;sub&gt;CL&lt;/sub&gt;_os</td>
<td>Current Limit Comparator Offset (V&lt;sub&gt;ILIM&lt;/sub&gt; − V&lt;sub&gt;CSL&lt;/sub&gt;)</td>
<td></td>
<td>±0.2</td>
<td>mV</td>
<td></td>
<td></td>
</tr>
<tr>
<td>I&lt;sub&gt;ILIM&lt;/sub&gt;</td>
<td>ILIM sink current</td>
<td></td>
<td>8.3</td>
<td>10</td>
<td>11.3</td>
<td>µA</td>
</tr>
<tr>
<td>I&lt;sub&gt;SS&lt;/sub&gt;_SRC</td>
<td>Soft-Start Pin Source Current</td>
<td>V&lt;sub&gt;SS&lt;/sub&gt; = 1.2V</td>
<td>1</td>
<td>2</td>
<td>3</td>
<td>µA</td>
</tr>
<tr>
<td>I&lt;sub&gt;SS&lt;/sub&gt;_SNK</td>
<td>Soft-Start Pin Sink Current</td>
<td>V&lt;sub&gt;SS&lt;/sub&gt; = 2V</td>
<td>4</td>
<td></td>
<td></td>
<td>µA</td>
</tr>
<tr>
<td>V&lt;sub&gt;DVP&lt;/sub&gt;</td>
<td>Over Voltage Protection Rising Threshold</td>
<td>With respect to V&lt;sub&gt;FB&lt;/sub&gt;</td>
<td>105</td>
<td>111</td>
<td>117</td>
<td>%</td>
</tr>
<tr>
<td>V&lt;sub&gt;DVP&lt;/sub&gt;_HYS</td>
<td>Over Voltage Protection Hysteresis</td>
<td>With respect to V&lt;sub&gt;FB&lt;/sub&gt;</td>
<td>2.8</td>
<td></td>
<td></td>
<td>%</td>
</tr>
</tbody>
</table>

**POWERGOOD**

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Conditions</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>V&lt;sub&gt;PGOOD&lt;/sub&gt;_RISING</td>
<td>PGOOD Rising Threshold</td>
<td></td>
<td>92.5</td>
<td>95.5</td>
<td>98.5</td>
<td>%</td>
</tr>
<tr>
<td>V&lt;sub&gt;PGOOD&lt;/sub&gt;_FALLING</td>
<td>PGOOD Falling Threshold</td>
<td></td>
<td>87</td>
<td>90.5</td>
<td>95</td>
<td>%</td>
</tr>
<tr>
<td>T&lt;sub&gt;PGOOD&lt;/sub&gt;</td>
<td>PGOOD delay</td>
<td>PGOOD pin de-asserting</td>
<td>10</td>
<td>µs</td>
<td></td>
<td></td>
</tr>
<tr>
<td>I&lt;sub&gt;OL&lt;/sub&gt;</td>
<td>PGOOD Low Sink Current</td>
<td>V&lt;sub&gt;PGOOD&lt;/sub&gt; = 0.4V</td>
<td>0.6</td>
<td>1</td>
<td></td>
<td>mA</td>
</tr>
<tr>
<td>I&lt;sub&gt;OH&lt;/sub&gt;</td>
<td>PGOOD High Leakage Current</td>
<td>V&lt;sub&gt;PGOOD&lt;/sub&gt; = 5V</td>
<td>5</td>
<td>200</td>
<td></td>
<td>nA</td>
</tr>
</tbody>
</table>

**GATE DRIVE**
**Electrical Characteristics** Limits in standard type are for \( T_J = 25^\circ C \) only, and limits in **boldface type** apply over the junction temperature \( T_J \) range of -40°C to +125°C. Minimum and Maximum limits are guaranteed through test, design, or statistical correlation. Typical values represent the most likely parametric norm at \( T_J = 25^\circ C \), and are provided for reference purposes only. Unless otherwise specified \( V_{IN} = 12V \). (Continued)

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Conditions</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>( I_{CBOOT} )</td>
<td>( C_{BOOT} ) Leakage Current</td>
<td>( V_{CBOOT} = 7V )</td>
<td>10</td>
<td></td>
<td></td>
<td>nA</td>
</tr>
<tr>
<td>( R_{ds, on 1} )</td>
<td>HDRV FET driver pull-up On resistance</td>
<td>( \Omega )</td>
<td>2.9</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>( R_{ds, on 2} )</td>
<td>HDRV FET driver pull-down On resistance</td>
<td>( \Omega )</td>
<td>1.7</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>( R_{ds, on 3} )</td>
<td>LDRV FET driver pull-up On resistance</td>
<td>( \Omega )</td>
<td>2.4</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>( R_{ds, on 4} )</td>
<td>LDRV FET driver pull-down On resistance</td>
<td>( \Omega )</td>
<td>0.8</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>( f_{OSC} )</td>
<td>Oscillator Frequency</td>
<td>( V_{FS} = 5V )</td>
<td>255</td>
<td>300</td>
<td>330</td>
<td>kHz</td>
</tr>
<tr>
<td>( D_{MAX} )</td>
<td>Maximum Duty Cycle</td>
<td>( V_{FB} = 1V )</td>
<td>95.5</td>
<td>98</td>
<td></td>
<td>%</td>
</tr>
<tr>
<td>( T_{ON,MIN} )</td>
<td>Minimum On Time</td>
<td>( )</td>
<td>180</td>
<td>260</td>
<td></td>
<td>ns</td>
</tr>
</tbody>
</table>

**ERROR AMPLIFIER**

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Conditions</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>( I_{FB} )</td>
<td>Feedback pin bias current</td>
<td>( V_{FB} = 1.5V )</td>
<td>50</td>
<td></td>
<td></td>
<td>nA</td>
</tr>
<tr>
<td>( I_{COMP, SRC} )</td>
<td>COMP Output Source Current</td>
<td>( V_{FB} = 1V )</td>
<td>120</td>
<td></td>
<td></td>
<td>µA</td>
</tr>
<tr>
<td>( I_{COMP, SNK} )</td>
<td>COMP Output Sink Current</td>
<td>( V_{FB} = 1.5V ), ( V_{COMP} = 0.5V )</td>
<td>110</td>
<td></td>
<td></td>
<td>µA</td>
</tr>
<tr>
<td>( Gm )</td>
<td>Error Amplifier Transconductance</td>
<td></td>
<td>620</td>
<td></td>
<td></td>
<td>µmho</td>
</tr>
<tr>
<td>( A_{VOL} )</td>
<td>Error Amplifier Voltage Gain</td>
<td></td>
<td>1250</td>
<td></td>
<td></td>
<td>V/V</td>
</tr>
<tr>
<td>( V_{SL} )</td>
<td>Slope Compensation (referred to the internal summing node)</td>
<td>( V_{FS} = 0V )</td>
<td>0.051</td>
<td></td>
<td></td>
<td>V/µs</td>
</tr>
<tr>
<td>( A_{CS} )</td>
<td>Current Sense Amplifier Gain</td>
<td>( V_{COMP} = 1.25V )</td>
<td>4</td>
<td>5</td>
<td>6</td>
<td>V/V</td>
</tr>
</tbody>
</table>

**LOGIC**

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Conditions</th>
<th>Min</th>
<th>Typ</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>( V_{IL} )</td>
<td>FS, /FPWM Pin Maximum Low Level Input Level</td>
<td></td>
<td>0.8</td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>( V_{IH} )</td>
<td>FS, /FPWM Pin Minimum High Level Input Level</td>
<td></td>
<td>2</td>
<td></td>
<td>V</td>
</tr>
</tbody>
</table>

**THERMAL SHUTDOWN**

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Conditions</th>
<th>Min</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>( T_{SD} )</td>
<td>Thermal Shutdown</td>
<td></td>
<td>160</td>
<td>°C</td>
</tr>
<tr>
<td>( T_{SD, HYS} )</td>
<td>Thermal Shutdown Hysteresis</td>
<td></td>
<td>10</td>
<td>°C</td>
</tr>
</tbody>
</table>

**EXT**

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Conditions</th>
<th>Min</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>( R_{EXT} )</td>
<td>EXT pin on resistance</td>
<td>( V_{EXT} = 5V ), ( I_{VLIN5} = 50 \text{ mA} )</td>
<td>4</td>
<td>Ø</td>
</tr>
<tr>
<td>( T_{TH_{EXT}} )</td>
<td>VLIN5 to EXT Switch Over Rising Threshold</td>
<td></td>
<td>4.6</td>
<td>V</td>
</tr>
</tbody>
</table>

---

www.national.com
Electrical Characteristics  Limits in standard type are for $T_J = 25°C$ only, and limits in boldface type apply over the junction temperature $T_J$ range of -40°C to +125°C. Minimum and Maximum limits are guaranteed through test, design, or statistical correlation. Typical values represent the most likely parametric norm at $T_J = 25°C$, and are provided for reference purposes only. Unless otherwise specified $V_{IN} = 12V$. (Continued)

Note 1: Absolute maximum ratings indicate limits beyond which damage to the device may occur. Operating Range indicates conditions for which the device is intended to be functional, but does not guarantee specific performance limits. For guaranteed specifications and test conditions, see the Electrical Characteristics. The guaranteed specifications apply only for the test conditions. Some performance characteristics may degrade when the device is not operated under the listed test conditions.

Note 2: For testing purposes, ESD was applied using the human-body model, a 100pF capacitor discharged through a 1.5kΩ resistor.
Typical Performance Characteristics

Efficiency ($V_{IN} = 12V$ to $V_{OUT} = 1.8V$)

Efficiency ($V_{IN} = 12V$ to $V_{OUT} = 3.3V$)

Efficiency ($V_{IN} = 12V$ to $V_{OUT} = 5V$)

Switching Frequency vs Temperature

Error Amplifier Gm vs Temperature

ILIM vs Temperature
Typical Performance Characteristics (Continued)

**ILIM vs V\textsubscript{IN}**

![](image1)

**IQ vs Temperature (Normal Operation)**

![](image2)

**IQ vs Temperature (Shutdown)**

![](image3)

**IQ vs V\textsubscript{IN} (Shutdown)**

![](image4)

**V\textsubscript{FB} vs Temperature**

![](image5)

**V\textsubscript{LINS} vs V\textsubscript{IN}**

![](image6)
Typical Performance Characteristics (Continued)

**Line Regulation**

![Line Regulation Graph](Image)

**Load Regulation**

![Load Regulation Graph](Image)
Operating Descriptions

GENERAL
The LM3075 solves the need within many portable systems for 5V, 3.3V, 3.3V standby and 12V legacy power supplies. The controller (IC) uses synchronous rectification and employs a peak current mode control scheme. Protection features include over-voltage protection (OVP), under-voltage protection (UVP), thermal protection, and positive and negative peak current limiting. UVP functionality is automatically disabled during soft-start and then enabled once the IC has correctly started. The device operates with a wide input voltage range from 4.5V to 36V.

SOFT START
In normal operation the soft-start functions as follows:
As the input voltage rises above the 4.2V UVLO threshold, where the internal circuitry is powered on, an internal 2 µA current starts to charge the capacitor connected between the SS pin and ground. A minimum on-time comparator generates the soft-start PWM pulses. As the SS pin voltage ramps up, the duty cycle increases, causing the output voltage to ramp up. During this time, the error amplifier output voltage is clamped at 2V, and the duty cycle generated by the PWM comparator is ignored. When the output voltage exceeds 98.5% (typical) of the set target voltage, the regulator transitions from soft-start to operating mode. Beyond this point, once the PWM pulses generated by the PWM comparator are narrower than those generated by the minimum on-time comparator, the PWM comparator takes over and starts to regulate the output voltage. Peak current mode control now takes place. The rate at which the duty cycle increases depends on the capacitance of the soft-start capacitor. The higher the capacitance, the slower the output voltage ramps up.

A unique feature of the LM3075 is that the rate at which the duty cycle grows is independent of the input voltage. This is because the ramp signal used to generate the soft-start duty cycle has a peak value proportional to the input voltage, making the product of duty cycle and input voltage a constant. This makes the soft-start process more predictable and reliable.

During soft-start, under-voltage protection is temporarily suspended but over-voltage protection and current limit remain in effect. When the SS pin voltage exceeds 2V, a soft-start time out signal is issued. This signal sets the under-voltage protection into ready mode. This is discussed more in the Under-Voltage Protection section.

If the SS pin is short-circuited to ground before startup, the LM3075 operates at minimum duty cycle when it is enabled, and the under-voltage protection is disabled.

FAULT STATE
When a fault condition is detected, a “fault” signal is generated internally. This signal discharges the capacitor connected between the SS pin and ground with 4 µA of current until the SS pin reaches 60mV. Once a level of 60mV is reached at the SS pin, the IC restarts normally and resumes operation assuming the cause of the fault condition has been removed.

FORCE PWM MODE
Pulling the FPWM pin to logic low activates the force PWM mode. In this mode, the top FET and the bottom FET gate signals are always complementary to each other and the Negative Current Limit comparator is activated (see Negative Current Limit section). In force PWM mode, the regulator always operates in Continuous Conduction Mode (CCM) and the duty cycle, which is approximately \( V_{OUT}/V_{IN} \) in this mode, is almost independent of load. The force PWM mode is good for applications where fixed switching frequency is required. In forced PWM mode, the top FET has to be turned on for a minimum of typically 180 ns each cycle. However, if the required duty cycle is less than the minimum value, the IC is unable to reach the desired voltage output in FPWM mode. This causes the chip to enter a fault state and the IC attempts to restart until the cause of the fault has been removed (see the Fault State section).

SKIP COMPARATOR
Whenever the output voltage of the error amplifier (COMP pin) goes below a 0.5V threshold, the PWM cycles are “skipped” until that voltage exceeds the threshold again. Due to the time required for the system loop to respond to changes, it is unlikely that the system will oscillate around the threshold and thus the system remains stable.

PULSE-SKIP MODE
Pulse-skip mode is activated by pulling the FPWM pin to a TTL-compatible logic high. In this mode, the Zero-Crossing / Negative Current Limit comparator detects the bottom FET current. Once the bottom FET current flows from drain to source, the bottom FET is turned off. This prevents negative inductor current.

In force PWM operation, the inductor current is allowed to go negative, so the regulator is always in Continuous Conduction Mode (CCM), no matter what the load is. In pulse-skip mode, the regulator enters Discontinuous Conduction Mode (DCM) under light loads. Once the regulator enters DCM, its switching frequency drops as the load current decreases. The minimum on-time comparator takes over causing the output voltage to continuously rise and COMP pin voltage (the error amplifier output voltage) to continuously drop. When the COMP pin voltage hits the 0.5V level, the Cycle Skip comparator toggles, causing the present switching cycle to be “skipped”, i.e., both FETs remain off during the whole cycle. As long as the COMP pin voltage is below 0.5V, no switching of the FETs happens. As a result, the output voltage drops, and the COMP pin voltage rises. When the COMP pin goes above the 0.5V level, the Cycle Skip comparator flips and allows a series of on-time pulses to happen. If the load current is so small that this series of pulses is enough to bring the output voltage up to such a level that the COMP pin drops below 0.5V again, the pulse skipping happens again. Otherwise it may take a number of consecutive pulses to bring the COMP pin voltage down to 0.5V again. As the load current increases, it takes more and more consecutive pulses to drive the COMP pin voltage to 0.5V. The pulse-skipping stops when the load current is sufficiently high. In pulse-skip mode, the frequency of the burst of switching pulses varies directly with the load current. Since the load is usually very light in pulse-skip mode, conducted noise is very low and the variable operating frequency should cause no EMI problems in the system.

The LM3075 pulse-skip mode helps the light load efficiency for two reasons. First, the bottom FET is turned on only when inductor current is in the positive conduction region, this eliminates circulating energy loss. Second, the FETs switch only when necessary, rather than every cycle, thus reducing the FETs switching losses and gate drive power losses.
CURRENT SENSING

The inductor current information is extracted by the current sense pins CSH and CSL. As shown in Figure 1 and Figure 2, current sensing is accomplished by either sensing the V_{ds} of the top FET, or sensing the voltage across a current sense resistor connected from V_{IN} to the drain of the top FET. Both approaches have advantages and disadvantages that need to be weighed for each specific application. The advantage of sensing current through the top FET is reduced parts count, board space, and cost but it also has the disadvantage of accuracy. Using a current sense resistor is the opposite, improving current sense accuracy but requiring additional parts, cost, and board space. The use of a current sense resistor has the additional disadvantage of increasing power loss and thus decreasing efficiency.

To ensure linear operation of the current amplifier, the current sense voltage input should not exceed 200 mV. Therefore, the R_{DS} of the top FET or the current sense resistor must be calculated carefully to ensure that, when the top FET is conducting the maximum current for that application, the current sense voltage does not exceed 200 mV.

Assuming a maximum of 200 mV across the CSL/R_{DS} resistor, the maximum allowable resistance can be calculated as follows:

$$R_{MAX} = \frac{200 \text{ mV}}{I_{MAX} \times \frac{1}{2} \Delta I_L}$$

Where I_{MAX} is the maximum expected load current, including an overload multiplier (typically 120%), and \Delta I_L is the inductor ripple current.

Note that the above equation defines only the maximum allowable value and not necessarily the recommended value. As the resistance increases, so do the switching losses.

CURRENT LIMITING

There is a leading edge blanking circuit that forces the top FET to be on for at least 180 ns. Beyond this minimum on time, the output of the PWM comparator is used to turn off the top FET. With an external resistor connected between the ILIM pin and the CSH pin the 10 μA current sink on the ILIM pin produces a voltage across the resistor to serve as the reference voltage for current limit. Adding a 10 nF capacitor across this resistor filters unwanted noise that could improperly trip the current limit comparator. Current limit is activated if the inductor current is too high causing the voltage at the CSL pin to be lower than that of the ILIM pin, toggling the comparator thus turning off the top FET immediately. The comparator is disabled either when the top FET is turned off or during the leading edge blanking time. The equation for the current limit resistor, RLIM, is as follows:

$$R_{LIM} = \left(\frac{I_{LIM} + \frac{1}{2} \Delta I_L}{10 \mu A}\right) R_{SNS}$$

NEGATIVE CURRENT LIMIT

The purpose of negative current limit is to ensure that the inductor does not saturate during negative current flow causing excessive current to flow through the bottom FET. The negative current limit is realized through sensing the bottom FET V_{ds}. An internally generated 100mV (typical) reference is used to compare with the bottom FET V_{ds} when it is on. Upon sensing too high a V_{ds}, the bottom FET is turned off. The negative current limit is only activated in force PWM mode.

OVER VOLTAGE PROTECTION (OVP)

The LM3075 responds to over-voltage events by attempting to recover without the need to restart the IC. There is a trip point at approximately 111% (typical) of V_{OUT} that, once reached, causes the circuit to shut off the HDRV FET and turn on the LDRV FET immediately to drive the bottom FET to discharge the output capacitor through the filter inductor. The system stays in this configuration until the output falls below approximately 108% (typical) of V_{OUT}. Once this lower level has been reached, the system resumes operation in either DCM or CCM. This scenario repeats until the cause of the over-voltage condition is removed.

UNDER VOLTAGE PROTECTION

When an under-voltage event is detected by the LM3075 and the under-voltage protection (UVP) is in ready mode, the IC attempts to restart the entire system. It does so by shutting off both the LDRV and HDRV FETs until the soft-start capacitor has discharged below a level of 60mV (typical). At this point, the IC shuts off the UVP and restarts the system as though it had just been powered up. The UVP is re-engaged once the soft-start capacitor voltage reaches a...
Operating Descriptions (Continued)

level of 2V (typical) and it enters ready mode as it does when the IC first was powered up. The UVP stays in ready mode until a new under-voltage event is detected.

POWER GOOD FUNCTION
A power good signal is available for indicating the general state of the IC. The function is realized through the internal MOSFET tied from the PGOOD pin to ground. The power good signal is asserted by turning off the MOSFET. The on resistance of the power good MOSFET is about 300Ω. The internal power good MOSFET is not turned on unless at least one of the following occurs:

1. There is an output over-voltage event.
2. The output voltage is below the power good lower limit (UVP event).
3. System is in shutdown mode, i.e. the EN pin voltage is below 0.6V.

As with the other protection responses, the power good signal has built-in hysteresis. See Vpwr_good in the Electrical Characteristics table.

FREQUENCY SELECT
The operating frequency may be set at 200 kHz or 300 kHz by the voltage on the frequency select (FS) pin. A voltage of 0V corresponds to a frequency of 200 kHz and a voltage of 5V corresponds to a frequency of 300 kHz. See the Electrical Characteristics table for more information.

VLIN5, VDD and EXT
An internal 5V supply (V_LIN5) is generated from the V_IN voltage through an internal linear regulator. This 5V supply is mainly for internal circuitry use, but can also be used externally. When used externally, it is recommended that the V_LIN5 voltage only be used for powering the gate drivers, i.e. supplying the bias for the top drivers’ bootstrap circuit and the bottom drivers’ VDD pins. When the voltage applied to the EXT pin is below 4.7V, an internal 5V low dropout regulator supplies the power for the V_LIN5. If the EXT voltage is taken above 4.7V, the 5V regulator is turned off and an internal switch is turned on to connect the EXT pin to the V_LIN5 pin. This allows the V_LIN5 power to be derived from a high efficiency source such as the output of the switching channel, when the channel is configured to operate in fixed 5V mode. The V_LIN5 voltage output comes from the EXT pin whenever the voltage applied to the EXT pin is higher than 4.7V. The externally applied voltage is required to be less than the voltage supplied to the VIN pin at all times. This prevents a voltage feedback situation from the EXT pin to the VIN pin. When the input voltage must be guaranteed to be within 4.5V to 5.5V, tie the V_LIN5 pin directly to the VIN pin and tie the EXT pin to ground. In this mode, the V_LIN5 current directly comes from power stage input rail and power loss due to the internal linear regulation is no longer an issue. Always connect the VDD pin to the V_LIN5 pin through a 4.7Ω resistor and connect a ceramic capacitor of at least 1 µF to bypass the VDD pin to ground.

THERMAL PROTECTION
The LM3075 IC enters thermal protection mode if the die temperature exceeds 160˚C. In this mode, the top and bottom FETs are turned off immediately. The IC then behaves in a manner as described in the Fault State section.

OUTPUT CAPACITORS FOR LINEAR REGULATORS
Like any linear regulator, the linear output that is either generated or controlled by the LM3075 requires an output capacitor to ensure stability. The output of V_LIN5 needs a minimum of 4.7 µF.

SWITCHING NOISE REDUCTION
Power MOSFETs are very fast switching devices. In a synchronous rectifier converter, the rapid drain current rise rate of the top FET coupled with parasitic inductance generates unwanted Ldi/dt spike noise at the source node of the FET (SW pin). The magnitude of the spike noise increases as the output current increases. This parasitic spike noise may turn into electromagnetic interference (EMI) that may cause trouble to the system performance. Therefore, it is vital to correct system performance to suppress this kind of noise. As shown in Figure 3, adding a resistor in series with the CBOOT pin scales the spikes and slow down the gate drive (HDRV) rise time of the top FET to yield a desired drain current transition time. Usually a 3.3Ω to 5.1Ω resistor is sufficient to suppress the noise. It is important to note that the addition of these resistors does increase the power loss in the system and thus decreases the efficiency. It is therefore important to choose the size of the resistor carefully; the top FET switching losses increases with higher resistance values.

Component Selection

OUTPUT VOLTAGE SETTING
The output voltage for each channel is set by the ratio of a voltage divider as shown in Figure 4. The resistor values can be determined by the following equation:

\[
R1 = \frac{R2}{\left(\frac{V_{OUT}}{V_{FB}} - 1\right)}
\]

Where \(V_{FB}\) is the typical value of feedback pin voltage and \(V_{OUT}\) is the nominal output voltage. Although increasing the value of \(R1\) and \(R2\) increases efficiency, this also decreases accuracy. Therefore, a maximum value is recommended for \(R2\) in order to keep the output within 0.3% of \(V_{OUT}\). This maximum \(R2\) value should be calculated first with the following equation:
Component Selection (Continued)

\[ R_{2\_\text{MAX}} = \frac{0.3\% \times V_{\text{OUT}}}{I_{\text{FB\_MAX}}} \]

Where \( I_{\text{FB\_MAX}} \) is the maximum current drawn by the FB pin.

Example: \( V_{\text{OUT}} = 5\, \text{V}, \, V_{\text{FB}} = 1.238\, \text{V}, \, I_{\text{FB\_MAX}} = 200\, \text{nA} \).

Output Capacitor Selection

In applications that exhibit large and fast load current swings, the slew rate of such a load current transient may be beyond the response speed of the regulator. Therefore, to meet voltage transient requirements during worst-case load transients, special consideration should be given to output capacitor selection. The total combined ESR of the output capacitors must be lower than a certain value, while the total capacitance must be greater than a certain value. Also, in applications where the specification of output voltage regulation is tight and ripple voltage must be low, starting from the required output voltage ripple (\( \Delta V_{\text{OUT}} \)) often results in fewer design iterations.

ALLOWED TRANSIENT VOLTAGE EXCURSION

The allowed output voltage excursion during a load transient (\( \Delta V_{\text{TRANS}} \)) is:

\[ \Delta V_{\text{TRANS}} = (\delta\% - \varepsilon\%) \times V_{\text{OUT}} - \frac{1}{2} \Delta V_{\text{OUT}} \]

Where \( \delta\% \) is the output voltage regulation window, \( \varepsilon\% \) is the output voltage initial accuracy \( V_{\text{OUT}} \) is the nominal output voltage, and \( \Delta V_{\text{OUT}} \) is the output voltage ripple.

Example: \( V_{\text{OUT}} = 5\, \text{V}, \, \delta\% = 7\%, \, \varepsilon\% = 3.4\%, \, \Delta V_{\text{OUT}} = 40\, \text{mV} \) peak-to-peak.

\[ \Delta V_{\text{TRANS}} = (7\% - 3.4\%) \times 5\, \text{V} - \frac{40\, \text{mV}}{2} \]

\[ = 160\, \text{mV}. \]

Since the ripple voltage is included in the calculation of \( \Delta V_{\text{TRANS}} \), the inductor ripple current should not be included in the worst-case load current excursion. That is, the worst-case load current excursion should be simply maximum load current change specification, \( \Delta I_{\text{TRANS}} \).

MAXIMUM ESR CALCULATION

Unless the rise and fall times of a load transient are slower than the response speed of the control loop, if the total combined ESR (\( R_{\text{ESR\_MAX}} \)) is too high, the load transient requirement is not met, no matter how large the capacitance. The maximum allowed total combined ESR is:

\[ R_{\text{ESR\_MAX}} = \frac{\Delta V_{\text{TRANS}}}{\Delta I_{\text{TRANS}}} \]

Example: \( \Delta V_{\text{TRANS}} = 160\, \text{mV}, \, \Delta I_{\text{TRANS}} = 3\, \text{A} \). Then \( R_{\text{ESR\_MAX}} = 53.3\, \text{m\Omega} \).

Maximum ESR criterion can be used when the associated capacitance is high enough, otherwise more capacitors than the number determined by this criterion should be used in parallel.

MINIMUM CAPACITANCE CALCULATION

In a switch mode power supply, the minimum output capacitance is typically dictated by the load transient requirement. If there is not enough capacitance, the output voltage excursion will exceed the maximum allowed value even if the maximum ESR requirement is met. The worst-case load transient is an unloading transient that happens when the
Output Capacitor Selection

(Continued)

input voltage is the highest and when the present switching cycle has just finished. The corresponding minimum capacitance is calculated as follows:

\[
C_{\text{MIN}} = \frac{L x \Delta V_{\text{TRANS}}}{V_{\text{OUT}} x R_{\text{ESR}}^2} \sqrt{\left(\frac{\Delta V_{\text{TRANS}}}{\Delta V_{\text{TRANS}} x R_{\text{ESR}}}\right)^2 - \left(\frac{\Delta I_{\text{TRANS}}}{R_{\text{ESR}}}\right)^2}
\]

Notice it is already assumed the total ESR, \(R_{\text{ESR}}\), is no greater than \(R_{\text{ESR, max}}\); otherwise the term under the square root will be a negative value. Also, it is assumed that \(L\) has already been selected, therefore the minimum \(L\) value should be calculated before \(C_{\text{MIN}}\) and after \(R_{\text{ESR}}\) (see Inductor Selection below). Example: \(R_{\text{ESR}} = 20 m\Omega\), \(V_{\text{OUT}} = 5 V\), \(\Delta V_{\text{TRANS}} = 160 mV\), \(\Delta I_{\text{TRANS}} = 3A\), \(L = 8\mu H\)

\[
C_{\text{MIN}} = \frac{8\mu H \times \sqrt{160 mV - \sqrt{(160 mV)^2 - (5A \times 20 m\Omega)^2}}}{5 x (20 m\Omega)^2}
= 140 \mu F.
\]

Generally speaking, \(C_{\text{MIN}}\) decreases with decreasing \(R_{\text{ESR}}, \Delta I_{\text{TRANS}}, \) and \(L\), but with increasing \(V_{\text{OUT}}\) and \(\Delta V_{\text{TRANS}}\). The output capacitance can therefore be chosen to be slightly larger than the calculated value so that it is more easily available. Here we would likely be fine choosing 220 \(\mu F\).

Inductor Selection

The size of the output inductor can be determined from the desired output ripple voltage, \(\Delta V_{\text{OUT}}\), and the impedance of the output capacitors at the switching frequency. The equation to determine the minimum inductance value is as follows:

\[
L_{\text{MIN}} = \frac{V_{\text{IN}} - V_{\text{OUT}}}{f_{\text{SW}} x V_{\text{IN}}} x \frac{V_{\text{OUT}} x R_{\text{ESR}}}{\Delta V_{\text{OUT}}}
\]

In the above equation, \(R_{\text{ESR}}\) is used in place of the impedance of the output capacitors. This is because in most cases, the impedance of the output capacitors at the switching frequency is very close to \(R_{\text{ESR}}\). In the case of ceramic capacitors, replace \(R_{\text{ESR}}\) with the true impedance.

Example: \(V_{\text{IN,MAX}} = 36V\), \(V_{\text{OUT}} = 5.0V\), \(\Delta V_{\text{OUT}} = 40 mV\), \(R_{\text{ESR}} = 20 m\Omega\), \(f_{\text{SW}} = 300 kHz\),

\[
L_{\text{MIN}} = \frac{36V - 5.0V}{300 kHz x 36V} x \frac{5.0V x 20 m\Omega}{40 mV}
= 7.17 \mu H
\]

The actual selection process usually involves several iterations of all of the above steps, from ripple voltage selection, to capacitor selection, to inductance calculations. Both the highest and the lowest input and output voltages and load transient requirements should be considered. If an inductance value larger than \(L_{\text{MIN}}\) is selected, make sure that the \(C_{\text{MIN}}\) requirement is not violated.

Priority should be given to parameters that are not flexible or more costly. For example, if there are very few types of capacitors to choose from, it may be a good idea to adjust the inductance value so that a requirement of 3.2 capacitors can be reduced to 3 capacitors.

Since inductor ripple current is often the criterion for selecting an output inductor, it is a good idea to double-check this value. The equation is:

\[
\Delta I_{L} = \frac{(V_{\text{IN}} - V_{\text{OUT}})}{f_{\text{SW}} x L} x D
\]

Where \(D\) is the duty cycle, defined by \(V_{\text{OUT}}/V_{\text{IN}}\).

Also important is the ripple current, which is defined by \(\Delta I_{L}/I_{\text{NOM}}\), where \(I_{\text{NOM}}\) is the nominal output current. Generally speaking, a ripple content of less than 50% is ok. Larger ripple content causes excessive losses in the inductor.

Example: \(V_{\text{IN}} = 12V\), \(V_{\text{OUT}} = 5.0V\), \(f_{\text{SW}} = 300 kHz\), \(L = 8 \mu H\)

\[
\Delta I_{L} = \frac{12V - 5.0V}{300 kHz x 8 \mu H} x \frac{5.0V}{12V} = 1.22A
\]

Given a maximum load current of 5A, the ripple content is 1.2A / 5A = 24%. When choosing an inductor, the saturation current should be higher than the maximum peak inductor current and the RMS current rating should be higher than the maximum load current.

Input Capacitor Selection

The input capacitor must be selected such that it can handle both the maximum ripple RMS current at highest ambient temperature and the maximum input voltage. The equation for the RMS current through the input capacitor is then

\[
I_{\text{RMS}} = I_{\text{MAX}} \sqrt{D(1-D)}
\]

Where \(I_{\text{MAX}}\) is maximum load current and \(D\) is the duty cycle. Example: \(I_{\text{MAX}} = 5A\) and \(D = 0.42\)

\[
I_{\text{RMS}} = 5A \sqrt{0.42 \times (1 - 0.42)} = 2.46A
\]

The function \(D(1-D)\) has a maxima at \(D = 0.5\). This duty cycle corresponds to the maximum RMS input current that may be used as a worst case in selecting an input capacitor. Input capacitors must meet the minimum requirements of voltage and ripple current capacity. The size of the capacitor should then be selected based on hold up time requirements. Bench testing for individual applications is still the best way to determine a reliable input capacitor value. The input capacitor should always be placed as close as possible to the current sense resistor or the drain of the top FET.

MOSFET Selection

BOTTOM FET SELECTION

During normal operation, the bottom FET is switching at almost zero voltage and therefore only conduction losses are present in the bottom FET. This makes the on resistance \(R_{\text{DS(OFF)}}\) the most important parameter when selecting the bottom FET; the lower the on resistance, the lower the power loss. The bottom FETs’ power losses peak at the maximum
MOSFET Selection (Continued)

input voltage and load current. The equation for the maximum allowable on resistance at room temperature for a given FET package, is:

\[
R_{\text{dson_max}} = \frac{1}{I_{\text{MAX}}^2 \times \left(1 - \frac{V_{\text{OUT}}}{V_{\text{IN_MAX}}}ight)} \times \frac{T_{\text{J_MAX}} - T_{\text{A_MAX}}}{1 + T_{\text{C}} \times (T_{\text{J_MAX}} - 25^\circ\text{C})} \times R_{\text{JJA}}
\]

(16)

where \(T_{\text{J_MAX}}\) is the maximum allowed junction temperature in the FET, \(T_{\text{A_MAX}}\) is the maximum ambient temperature, \(R_{\text{JJA}}\) is the junction-to-ambient thermal resistance of the FET, and \(T_{\text{C}}\) is the temperature coefficient of the on resistance which is typically in the range of 10,000ppm/°C.

If the calculated \(R_{\text{dson_max}}\) is smaller than the lowest value available, multiple FETs can be used in parallel. This effectively reduces the \(I_{\text{MAX}}\) term in the above equation, thus reducing \(R_{\text{dson}}\). When using two FETs in parallel, multiply the calculated \(R_{\text{dson_max}}\) by 4 to obtain the \(R_{\text{dson}}\) for each FET. In the case of three FETs, multiply by 9.

Example: \(T_{\text{J_MAX}} = 100^\circ\text{C}, T_{\text{A_MAX}} = 60^\circ\text{C}, R_{\text{JJA}} = 60^\circ\text{C/}W, V_{\text{IN_MIN}} = 36V, V_{\text{OUT}} = 5V,\) and \(I_{\text{MAX}} = 5A\).

\[
R_{\text{dson_max}} = \frac{1}{(5A)^2 \times \left(1 - \frac{5V}{36V}\right)} \times \frac{60^\circ\text{C} - 60^\circ\text{C}}{1 + 0.01^\circ\text{C} \times (100^\circ\text{C} - 25^\circ\text{C})} \times 60^\circ\text{C}/W = 17.7 \text{ m}\Omega
\]

(17)

If the selected FET has an \(R_{\text{dson}}\) value higher than 17.7Ω, then two FETs with an \(R_{\text{dson}}\) less than 30mΩ can be used in parallel. In this case, the temperature rise on each FET will not go to \(T_{\text{J_MAX}}\) because each FET is now dissipating only half of the total power.

TOP FET SELECTION

The output resistance for the top FET driver is 3.1Ω (maximum). The bias voltage is developed by an external bootstrap supply circuit, which is comprised of a diode and a capacitor. Before selecting the top FET, it is recommended to select the driving voltage for the bootstrap circuit first (see more in the Bootstrap Component Selection section).

If VLIN5 is chosen to drive the bootstrap circuit, care must be taken to ensure that the gate threshold voltage of the top FET is less than 3V (maximum). The top FET starts to turn on when the input voltage exceeds the threshold voltage of the UVLO, which has a minimum threshold of 3.8V. In this case, VLIN5 follows at approximately 3.8V also and thus the bias voltage to the top FET driver is about 3V after the bootstrap diode.

The top FET has two types of losses: switching loss and conduction loss. The switching losses mainly consist of crossover loss and bottom diode reverse recovery loss. Since it is rather difficult to estimate the switching loss, a general starting point is to allot 60% of the top FET thermal capacity to switching losses. The best way to precisely determine switching losses is through bench testing. The equation for calculating the on resistance of the top FET is thus:

\[
R_{\text{dson_max}} = \frac{V_{\text{IN_MIN}} \times 0.4}{I_{\text{MAX}}^2 \times V_{\text{OUT}}} \times \frac{T_{\text{J_MAX}} - T_{\text{A_MAX}}}{1 + T_{\text{C}} \times (T_{\text{J_MAX}} - 25^\circ\text{C})} \times R_{\text{JJA}}
\]

(18)

Example: \(T_{\text{J_MAX}} = 100^\circ\text{C}, T_{\text{A_MAX}} = 60^\circ\text{C}, R_{\text{JJA}} = 60^\circ\text{C/}W, V_{\text{IN_MIN}} = 5.5V, V_{\text{NOM}} = 5V,\) and \(I_{\text{MAX}} = 5A\).

\[
R_{\text{DSON_MAX}} = \frac{5.5V \times 0.4}{(5A)^2 \times 5V} \times \frac{100^\circ\text{C} - 60^\circ\text{C}}{1 + 0.01^\circ\text{C} \times (100^\circ\text{C} - 25^\circ\text{C})} \times 60^\circ\text{C}/W = 6.7 \text{ m}\Omega
\]

(19)

When using FETs in parallel, the same guidelines apply to the top FET as apply to the bottom FET.

BOOTSTRAP COMPONENT SELECTION

Selection of the bootstrap components can be done after top FET and driving voltage are chosen. VLIN5 or another supply such as input may be used as the driving voltage. Once chosen, the bootstrap components can be selected.

Typically a 0.1µF ceramic (X5R, X7R) works well. Any suitably sized Schottky diode works well for the bootstrap Diode. If excessive leakage current is seen, a larger bootstrap capacitance may be needed.

Loop Compensation

The purpose of loop compensation is to meet static and dynamic performance requirements while maintaining stability. Loop gain is usually checked to determine small-signal performance. Loop gain is equal to the product of the control-output transfer function and the output-control transfer function (the compensation network transfer function). Generally speaking, it is a good idea to have a loop gain slope that is -20dB/decade from a very low frequency to well beyond the crossover frequency. The crossover frequency should not exceed one-fifth of the switching frequency. The higher the bandwidth, the faster the load transient response speed unless duty cycle saturates during a load transient. Since the control-output transfer function usually has very limited low frequency gain, it is a good idea to place a pole in the compensation at zero frequency, so that the low frequency gain is relatively large. A large DC gain means high DC regulation accuracy (i.e. DC voltage changes little with load or line variations). The rest of the compensation scheme depends highly on the shape of the control-output plot. As shown in Figure 6, the control-output transfer function consists of one pole \(f_n\), one zero \(f_z\), and a double pole at \(f_c\) (half the switching frequency). The following can be done to create a -20dB/decade roll-off of the loop gain: Place the first pole at 0Hz, the first zero at \(f_n\), the second pole at \(f_n\), and the second zero at \(f_c\). The resulting output-control transfer function is shown in Figure 7.
Loop Compensation (Continued)

The control-output corner frequencies, and thus the desired compensation corner frequencies, can be determined approximately by the following equations:

\[
\frac{1}{2\pi R_C} C_{OUT} = f_Z = \frac{1}{2\pi R_{ESR} C_{OUT}}
\]

(20)

\[
f_P = \frac{1}{2\pi R_C} + \frac{0.5}{2\pi L_f C_O}
\]

(21)

Since \( f_p \) is determined by the output network, it shifts with loading \( (R_o) \) and duty cycle. First determine the range of frequencies \( (f_{p_{min/max}}) \) of the pole across the expected load range and then place the first compensation zero within that range.

**Example:** \( R_{asr} = 20m\Omega, \ C_O = 100uF, \ R_{omax} = 5V/100mA=50\Omega, \ R_{omin} = 5V/5A = 1\Omega, \ L = 8 \mu H \)

\[
f_Z = \frac{1}{2\pi \times 20m\Omega \times 220 \mu F} = 36 \text{ kHz}
\]

(22)

\[
f_{P_{MIN}} = \frac{1}{2\pi \times 500 \Omega \times 220 \mu F} + 0.5 \frac{1}{2\pi \times 300 \text{ kHz} \times 8 \mu H \times 220 \mu F} = 165 \text{ Hz}
\]

(23)

\[
f_{P_{MAX}} = \frac{1}{2\pi \times 1\Omega \times 220 \mu F} + 0.5 \frac{1}{2\pi \times 300 \text{ kHz} \times 8 \mu H \times 220 \mu F} = 874 \text{ Hz}
\]

(24)

Once the \( f_p \) range is determined, \( R_{c_1} \) should be calculated using:

\[
R_{c_1} = \frac{B}{gm} \left( \frac{R_1 + R_2}{R_1} \right) \times 10^3
\]

(25)

Where \( B \) is the desired gain in V/V at \( f_p \) \( (f_{z_1}) \), \( gm \) is the transconductance of the error amplifier, and \( R_1 \) and \( R_2 \) are the feedback resistors.

A gain value around 10dB \( (3.3V/V) \) is generally a good starting point.

**Example:** \( B = 3.3 \text{ V/V}, \ gm = 0.650 \mu \text{mho}, \ R_1 = 20 \Omega, \ R_2 = 60.4 \Omega \)

\[
R_{c_1} = \frac{3.3}{0.650} \left( \frac{20 \Omega + 60.4 \text{ k}\Omega}{20 \text{ k}\Omega} \right) = 20.4 \text{ k}\Omega \equiv 20 \text{ k}\Omega
\]

(26)

Bandwidth varies proportionally to the value of \( R_{c_1} \). Next, \( C_{c_1} \) can be determined with the following equation:

\[
C_{c_1} = \frac{1}{2\pi f_{p_{min}} R_{c_1}}
\]

(27)

**Example:** \( f_{p_{min}} = 313\text{ Hz}, \ R_{c_1} = 20k\Omega \)

\[
C_{c_1} = \frac{1}{2\pi \times 165 \text{ kHz} \times 20 \text{ k}\Omega} = 48 \text{nF} \equiv 47 \text{nF}
\]

(28)

The value of \( C_{c_1} \) should be within the range determined by \( f_{p_{min/max}} \). A higher value generally provides a more stable loop, but too high a value slows the transient response time.

The compensation network also introduces a low frequency pole that is close to 0Hz. A second pole should also be placed at \( f_p \). This pole can be created with a single capacitor \( C_{c_2} \) and a shorted \( R_{c_2} \) (see Figure 9). The minimum value for this capacitor can be calculated by:

\[
C_{c_2 \min} = \frac{1}{2\pi f_{z} R_{c_1}}
\]

(29)

\( C_{c_2} \) may not be necessary, however it does create a more stable control loop. This is especially important with high load currents and in current sharing mode.

**Example:** \( f_z = 36k\text{Hz}, \ R_{c_1} = 20k\Omega \)
Loop Compensation (Continued)

\[ C_{\text{C2MIN}} = \frac{1}{2\pi \times 36 \text{ kHz} \times 20 \ \text{k}\Omega} = 221 \ \text{pF} \]  

(30)

FIGURE 8. Compensation Network

Typical Application Circuit
Physical Dimensions  inches (millimeters) unless otherwise noted

20-Lead TSSOP Package  
Order Number LM3075MTC  
NS Package Number MTC20

LIFE SUPPORT POLICY
NATIONAL'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF THE PRESIDENT AND GENERAL COUNSEL OF NATIONAL SEMICONDUCTOR CORPORATION. As used herein:

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, and whose failure to perform when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury to the user.

2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

BANNED SUBSTANCE COMPLIANCE
National Semiconductor manufactures products and uses packing materials that meet the provisions of the Customer Products Stewardship Specification (CSP-9-111C2) and the Banned Substances and Materials of Interest Specification (CSP-9-111S2) and contain no “Banned Substances” as defined in CSP-9-111S2.

Leadfree products are RoHS compliant.
IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, modifications, enhancements, improvements, and other changes to its products and services at any time and to discontinue any product or service without notice. Customers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All products are sold subject to TI’s terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its hardware products to the specifications applicable at the time of sale in accordance with TI’s standard warranty. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by government requirements, testing of all parameters of each product is not necessarily performed.

TI assumes no liability for applications assistance or customer product design. Customers are responsible for their products and applications using TI components. To minimize the risks associated with customer products and applications, customers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any TI patent right, copyright, mask work right, or other TI intellectual property right relating to any combination, machine, or process in which TI products or services are used. Information published by TI regarding third-party products or services does not constitute a license from TI to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of TI.

Reproduction of TI information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. Reproduction of this information with alteration is an unfair and deceptive business practice. TI is not responsible or liable for such altered documentation. Information of third parties may be subject to additional restrictions.

Resale of TI products or services with statements different from or beyond the parameters stated by TI for that product or service voids all express and any implied warranties for the associated TI product or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

TI products are not authorized for use in safety-critical applications (such as life support) where a failure of the TI product would reasonably be expected to cause severe personal injury or death, unless officers of the parties have executed an agreement specifically governing such use. Buyers represent that they have all necessary expertise in the safety and regulatory ramifications of their applications, and acknowledge and agree that they are solely responsible for all legal, regulatory and safety-related requirements concerning their products and any use of TI products in such safety-critical applications. TI products are neither designed nor intended for use in such safety-critical applications.

TI products are neither designed nor intended for use in military/aerospace applications or environments unless the TI products are specifically designated by TI as military-grade or "enhanced plastic." Only products designated by TI as military-grade meet military specifications. Buyers acknowledge and agree that any such use of TI products which TI has not designated as military-grade is solely at the Buyer's risk, and that they are solely responsible for compliance with all legal and regulatory requirements in connection with such use.

TI products are neither designed nor intended for use in automotive applications or environments unless the specific TI products are designated by TI as compliant with ISO/TS 16949 requirements. Buyers acknowledge and agree that, if they use any non-designated products in automotive applications, TI will not be responsible for any failure to meet such requirements.

Following are URLs where you can obtain information on other Texas Instruments products and application solutions:

**Products** | **Applications**
--- | ---
Audio | Communications and Telecom
Amplifiers | Computers and Peripherals
Data Converters | Consumer Electronics
DLP® Products | Energy and Lighting
DSP | Industrial
Clocks and Timers | Medical
Interface | Security
Logic | Space, Avionics and Defense
Power Mgmt | Transportation and Automotive
Microcontrollers | Video and Imaging
RFID | www.ti.com/wirelessconnectivity
OMAP Mobile Processors | e2e.ti.com
Wireless Connectivity | www.ti.com/wirelessconnectivity

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265
Copyright © 2011, Texas Instruments Incorporated