S25FL032P

32-Mbit CMOS 3.0 Volt Flash Memory with 104-MHz SPI (Serial Peripheral Interface) Multi I/O Bus

Data Sheet *(Preliminary)*

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S25FL032P

32-Mbit CMOS 3.0 Volt Flash Memory with 104-MHz SPI (Serial Peripheral Interface) Multi I/O Bus

Data Sheet *(Preliminary)*

Distinctive Characteristics

Architectural Advantages

- **Single power supply operation**
  - Full voltage range: 2.7 to 3.6V read and write operations
- **Memory architecture**
  - Uniform 64 KB sectors
  - Top or bottom parameter block (Two 64-KB sectors (top or bottom) broken down into sixteen 4-KB sub-sectors each)
  - 256-byte page size
  - Backward compatible with the S25FL032A device
- **Program**
  - Page Program (up to 256 bytes) in 1.5 ms (typical)
  - Program operations are on a page by page basis
  - Accelerated programming mode via 9V W#/ACC pin
  - Quad Page Programming
- **Erase**
  - Bulk erase function
  - Sector erase (SE) command (D8h) for 64 KB sectors
  - Sub-sector erase (P4E) command (20h) for 4 KB sectors
  - Sub-sector erase (P8E) command (40h) for 8 KB sectors
- **Cycling endurance**
  - 100,000 cycles per sector typical
- **Data retention**
  - 20 years typical
- **Device ID**
  - JEDEC standard two-byte electronic signature
  - RES command one-byte electronic signature for backward compatibility
- **One time programmable (OTP) area for permanent, secure identification; can be programmed and locked at the factory or by the customer**
- **CFI (Common Flash Interface) compliant: allows host system to identify and accommodate multiple flash devices**
- **Process technology**
  - Manufactured on 0.09 µm MirrorBit® process technology
- **Package option**
  - Industry Standard Pinouts
  - 8-pin SO package (208 mils)
  - 16-pin SO package (300 mils)
  - 8-contact USON package (5 x 6 mm)
  - 8-contact WSON package (6 x 8 mm)

Performance Characteristics

- **Speed**
  - Normal READ (Serial): 40 MHz clock rate
  - FAST_READ (Serial): 104 MHz clock rate (maximum)
  - DUAL I/O FAST_READ: 80 MHz clock rate or 20 MB/s effective data rate
  - QUAD I/O FAST_READ: 80 MHz clock rate or 40 MB/s effective data rate
- **Power saving standby mode**
  - Standby Mode 80 µA (typical)
  - Deep Power-Down Mode 3 µA (typical)

Memory Protection Features

- **Memory protection**
  - W#/ACC pin works in conjunction with Status Register Bits to protect specified memory areas
  - Status Register Block Protection bits (BP2, BP1, BP0) in status register configure parts of memory as read-only

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General Description

The S25FL032P is a 3.0 Volt (2.7V to 3.6V), single-power-supply Flash memory device. The device consists of 64 uniform 64 KB sectors with the two (Top or Bottom) 64 KB sectors further split up into thirty-two 4KB sub sectors. The S25FL032P device is fully backward compatible with the S25FL032A device.

The device accepts data written to SI (Serial Input) and outputs data on SO (Serial Output). The devices are designed to be programmed in-system with the standard system 3.0-volt V_{CC} supply.

The S25FL032P device adds the following high-performance features using 5 new instructions:

- Dual Output Read using both SI and SO pins as output pins at a clock rate of up to 80 MHz
- Quad Output Read using SI, SO, W#/ACC and HOLD# pins as output pins at a clock rate of up to 80 MHz
- Dual I/O High Performance Read using both SI and SO pins as input and output pins at a clock rate of up to 80 MHz
- Quad I/O High Performance Read using SI, SO, W#/ACC and HOLD# pins as input and output pins at a clock rate of up to 80 MHz
- Quad Page Programming using SI, SO, W#/ACC and HOLD# pins as input pins to program data at a clock rate of up to 80 MHz

The memory can be programmed 1 to 256 bytes at a time, using the Page Program command. The device supports Sector Erase and Bulk Erase commands.

Each device requires only a 3.0-volt power supply (2.7V to 3.6V) for both read and write functions. Internally generated and regulated voltages are provided for the program operations. This device requires a high voltage supply to the W#/ACC pin to enable the Accelerated Programming mode.

The S25FL032P device also offers a One-Time Programmable area (OTP) of up to 128-bits (16 bytes) for permanent secure identification and an additional 490 bytes of OTP space for other use. This OTP area can be programmed or read using the OTPP or OTPR instructions.

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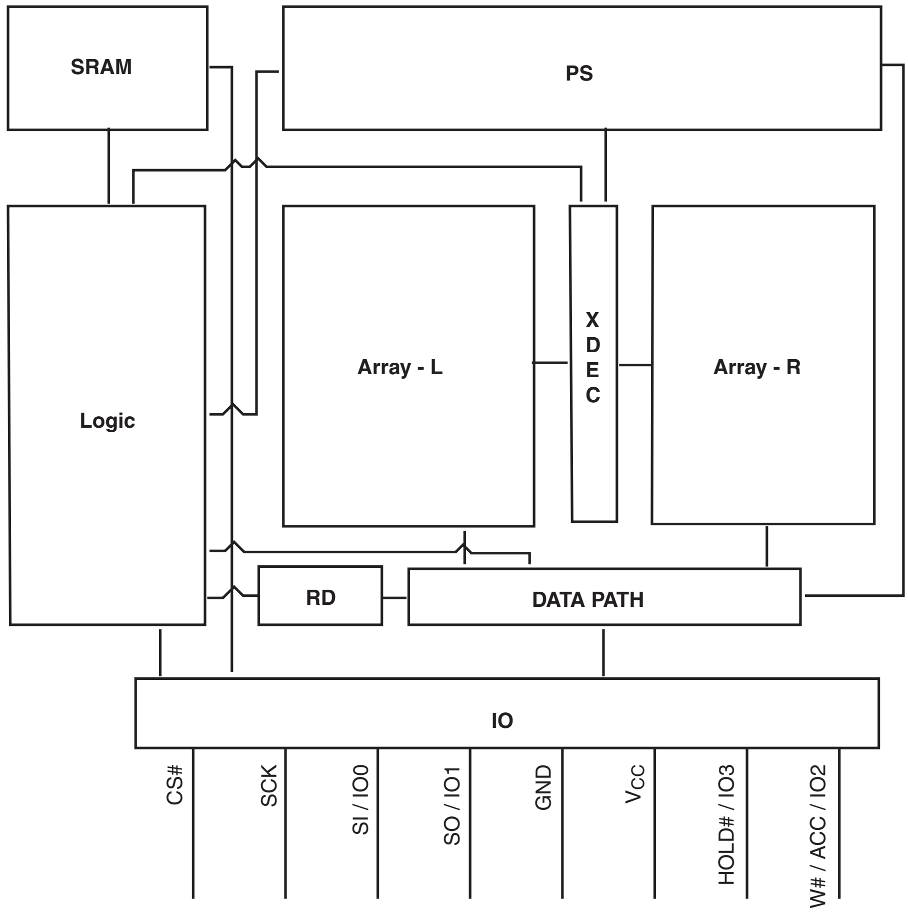
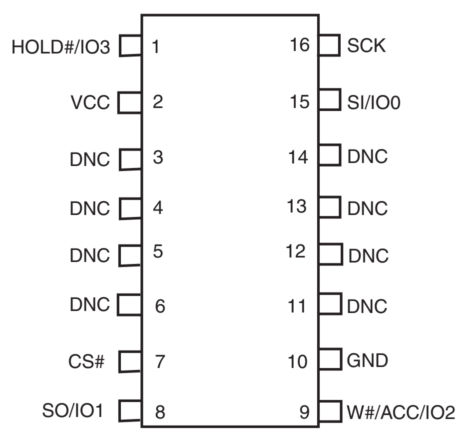
1. Block Diagram



2. Connection Diagrams

Figure 2.1 16-pin Plastic Small Outline Package (SO)



Note
DNC = Do Not Connect (Reserved for future use)

Figure 2.2 8-pin Plastic Small Outline Package (SO)

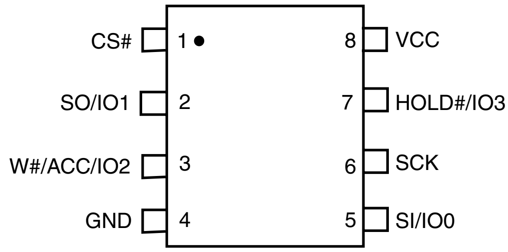


Figure 2.3 8-contact USON (5 x 6 mm) Package

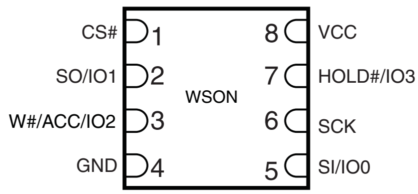
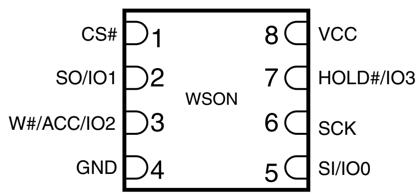


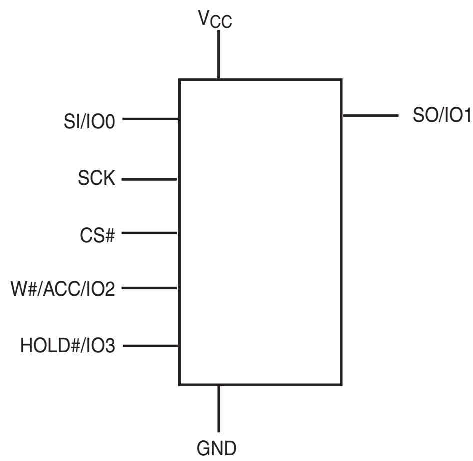
Figure 2.4 8-contact WSON Package (6 x 8 mm)



3. Input/Output Descriptions

Signal	I/O	Description
SO/IO1	I/O	**Serial Data Output**: Transfers data serially out of the device on the falling edge of SCK. Functions as an input pin in Dual and Quad I/O, and Quad Page Program modes.
SI/IO0	I/O	**Serial Data Input**: Transfers data serially into the device. Device latches commands, addresses, and program data on SI on the rising edge of SCK. Functions as an output pin in Dual and Quad I/O mode.
SCK	Input	**Serial Clock**: Provides serial interface timing. Latches commands, addresses, and data on SI on rising edge of SCK. Triggers output on SO after the falling edge of SCK.
CS#	Input	**Chip Select**: Places device in active power mode when driven low. Deselects device and places SO at high impedance when high. After power-up, device requires a falling edge on CS# before any command is written. Device is in standby mode when a program, erase, or Write Status Register operation is not in progress.
HOLD#/IO3	I/O	**Hold**: Pauses any serial communication with the device without deselecting it. When driven low, SO is at high impedance, and all input at SI and SCK are ignored. Requires that CS# also be driven low. Functions as an output pin in Quad I/O mode.
W#/ACC/IO2	I/O	**Write Protect**: Protects the memory area specified by Status Register bits BP2:BP0. When driven low, prevents any program or erase command from altering the data in the protected memory area. Functions as an output pin in Quad I/O mode.
V_{CC}	Input	**Supply Voltage**
GND	Input	**Ground**

4. Logic Symbol



5. Ordering Information

The ordering part number is formed by a valid combination of the following:

S25FL 032 P 0X M F I 00 1

Packing Type (Note 1)
0 = Tray
1 = Tube
3 = 13” Tape and Reel

Model Number (Additional Ordering Options)
01 = 8-pin SO package / 8-contact USON package
00 = 16-pin SO package / 8-contact WSON package

Temperature Range
I = Industrial (–40°C to + 85°C)

Package Materials
F = Lead (Pb)-free

Package Type
M = 8-pin / 16-pin SO package
N = 8-contact USON / WSON package

Speed
0X = 104 MHz

Device Technology
P = 0.09 µm MirrorBit® Process Technology

Density
032 = 32 Mbit

Device Family
S25FL
Spansion Memory 3.0 Volt-only, Serial Peripheral Interface (SPI) Flash Memory

5.1 Valid Combinations

Table 5.1 lists the valid combinations configurations planned to be supported in volume for this device.

Table 5.1 S25FL032P Valid Combinations Table

S25FL032P Valid Combinations					Package Marking
Base Ordering Part Number	**Speed Option**	**Package & Temperature**	**Model Number**	**Packing Type**	
S25FL032P	0X	MFI	00, 01	0, 1, 3	FL032P + (Temp) + F
		NFI			

Note

1. The last OPN character “x” signifies the Packing type.

6. Spansion SPI Modes

A microcontroller can use either of its two SPI modes to control Spansion SPI Flash memory devices:

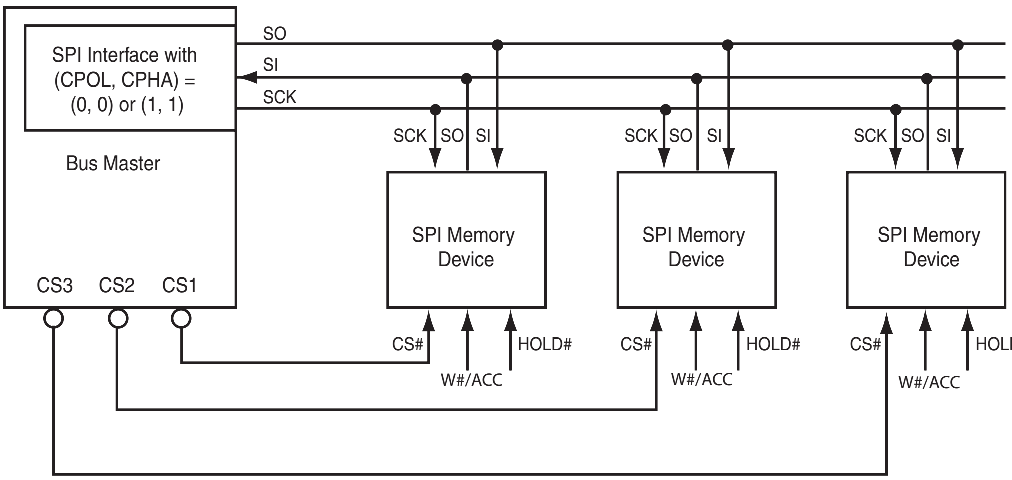
- CPOL = 0, CPHA = 0 (Mode 0)
- CPOL = 1, CPHA = 1 (Mode 3)

Input data is latched in on the rising edge of SCK, and output data is available from the falling edge of SCK for both modes.

When the bus master is in standby mode, SCK is as shown in Figure 6.2 for each of the two modes:

- SCK remains at 0 for (CPOL = 0, CPHA = 0 Mode 0)
- SCK remains at 1 for (CPOL = 1, CPHA = 1 Mode 3)

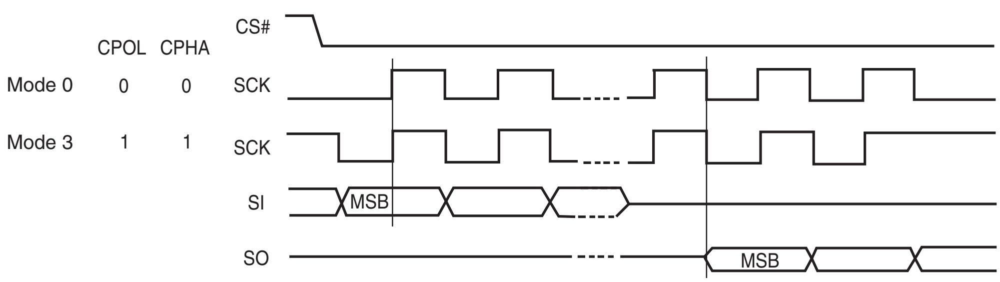
Figure 6.1 Bus Master and Memory Devices on the SPI Bus



Note

The Write Protect/Accelerated Programming (W#/ACC) and Hold (HOLD#) signals should be driven high (logic level 1) or low (logic level 0) as appropriate.

Figure 6.2 SPI Modes Supported



7. Device Operations

All Spansion SPI devices accept and output data in bytes (8 bits at a time).

7.1 Byte or Page Programming

Programming data requires two commands: Write Enable (WREN), which is one byte, and a Page Program (PP) sequence, which consists of four bytes plus data. The Page Program sequence accepts from 1 byte up to 256 consecutive bytes of data (which is the size of one page) to be programmed in one operation. Programming means that bits can either be left at 0, or programmed from 1 to 0. Changing bits from 0 to 1 requires an erase operation.

7.2 Quad Page Programming

The Quad Page Program (QPP) instruction allows up to 256 bytes of data to be programmed at previously erased (FFh) memory locations using 4 pins as inputs at the same time, thus effectively quadrupling the data transfer rate, compared to the Page Program (PP) instruction.

7.3 Dual and Quad I/O Mode

The S25FL032P device supports Dual and Quad I/O operation when using the Dual/Quad Output Read Mode and the Dual/Quad I/O High Performance Mode instructions. Using the Dual or Quad I/O instructions allows data to be transferred to or from the device at two to four times the rate of standard SPI devices. When operating in the Dual or Quad I/O High Performance Mode (BBh or EBh instructions), data can be read at fast speed using two or four data bits at a time, and the 3-byte address can be input two or four address bits at a time.

7.4 Sector Erase / Bulk Erase

The Sector Erase (SE) and Bulk Erase (BE) commands set all the bits in a sector or the entire memory array to 1. While bits can be individually programmed from 1 to 0, erasing bits from 0 to 1 must be done on a sector-wide (SE) or array-wide (BE) level. In addition to the 64-KB Sector Erase (SE), the S25FL032P device also offers 4-KB Parameter Sector Erase (P4E) and 8-KB Parameter Sector Erase (P8E).

7.5 Monitoring Write Operations Using the Status Register

The host system can determine when a Write Register, program, or erase operation is complete by monitoring the Write in Progress (WIP) bit in the Status Register. The Read from Status Register command provides the state of the WIP bit. In addition, the S25FL032P device offers two additional bits in the Status Register (P_ERR, E_ERR) to indicate whether a Program or Erase operation was a success or failure.

7.6 Active Power and Standby Power Modes

The device is enabled and in the Active Power mode when Chip Select (CS#) is Low. When CS# is high, the device is disabled, but may still be in the Active Power mode until all program, erase, and Write Registers operations have completed. The device then goes into the Standby Power mode, and power consumption drops to I_{SB}. The Deep Power-Down (DP) command provides additional data protection against inadvertent signals. After writing the DP command, the device ignores any further program or erase commands, and reduces its power consumption to I_{DP}.

7.7 Status Register

The Status Register contains the status and control bits that can be read or set by specific commands (see Table 9.1 on page 22). These bits configure different protection configurations and supply information of operation of the device. (for details see Table 9.8, *S25FL032P Status Register* on page 36):

- **Write In Progress (WIP):** Indicates whether the device is performing a Write Registers, program or erase operation.
- **Write Enable Latch (WEL):** Indicates the status of the internal Write Enable Latch.
- **Block Protect (BP2, BP1, BP0):** Non-volatile bits that define memory area to be software-protected against program and erase commands.
- **Erase Error (E_ERR):** The Erase Error Bit is used as an Erase operation success and failure check.
- **Program Error (P_ERR):** The Program Error Bit is used as an program operation success and failure check.
- **Status Register Write Disable (SRWD):** Places the device in the Hardware Protected mode when this bit is set to 1 and the W#/ACC input is driven low. In this mode, the non-volatile bits of the Status Register (SRWD, BP2, BP1, BP0) become read-only bits.

7.8 Configuration Register

The Configuration Register contains the control bits that can be read or set by specific commands. These bits configure different configurations and security features of the device.

- The FREEZE bit locks the BP2-0 bits in Status Register and the TBPROT and TBPARM bits in the Configuration Register. Note that once the FREEZE bit has been set to ‘1’, then it cannot be cleared to ‘0’ until a power-on-reset is executed. As long as the FREEZE bit is set to ‘0’, then the other bits of the Configuration Register, including FREEZE bit, can be written to.
- The QUAD bit is non-volatile and sets the pin out of the device to Quad mode; that is, W#/ACC becomes IO2 and HOLD# becomes IO3. The instructions for Serial, Dual Output, and Dual I/O reads will function as normal. The W#/ACC and HOLD# functionality will not work when the device is set in Quad mode.
- The TBPARM bit defines the logical location of the 4 KB parameter sectors. The parameter sectors consist of thirty two 4 KB sectors. All sectors other than the parameter sectors are defined to be 64-KB uniform in size. When TBPARM is set to a ‘1’, the 4 KB parameter sectors starts at the top of the array. When TBPARM is set to a ‘0’, the 4 KB parameter sectors starts at the bottom of the array. Note that once this bit is set to a '1', it cannot be changed back to '0'.
- The BPNV bit defines whether or not the BP2-0 bits in the Status Register are volatile or non-volatile. When BPNV is set to a ‘1’, the BP2-0 bits in the Status Register are volatile and will be reset to binary 111 after power on reset. When BPNV is set to a ‘0’, the BP2-0 bits in the Status Register are non-volatile. Note that once this bit is set to a '1', it cannot be changed back to '0'.
- The TBPROT bit defines the operation of the block protection bits BP2, BP1, and BP0 in the Status Register. When TBPROT is set to a ‘0’, then the block protection is defined to start from the top of the array. When TBPROT is set to a ‘1’, then the block protection is defined to start from the bottom of the array. Note that once this bit is set to a '1', it cannot be changed back to '0'.

Note: In case BPNV=1 (Volatile), the BP2-0 bits will always be considered as non-volatile.

Table 7.1 Configuration Register Table

Bit	Bit Name	Bit Function	Description
7	NA	-	Not Used
6	NA	-	Not Used
5	TBPROT	Configures start of block protection	1 = Bottom Array (low address) 0 = Top Array (high address) (Default)
4	NA	-	Not Used
3	BPNV	Configures BP2-0 bits in the Status Register	1 = Volatile 0 = Non-volatile (Default)
2	TBPARM	Configures Parameter sector location	1 = Top Array (high address) 0 = Bottom Array (low address) (Default)
1	QUAD	Puts the device into Quad I/O mode	1 = Quad I/O 0 = Dual or Serial I/O (Default)
0	FREEZE	Locks BP2-0 bits in the Status Register	1 = Enabled 0 = Disabled (Default)

Note
(Default) indicates the value of each Configuration Register bit set upon initial factory shipment.

7.9 Data Protection Modes

Spansion SPI Flash memory devices provide the following data protection methods:

- **The Write Enable (WREN) command:** Must be written prior to any command that modifies data. The WREN command sets the Write Enable Latch (WEL) bit. The WEL bit resets (disables writes) on power-up or after the device completes the following commands:
  - Page Program (PP)
  - Sector Erase (SE)
  - Bulk Erase (BE)
  - Write Disable (WRDI)
  - Write Register (WRR)
  - Parameter 4 KB Sector Erase (P4E)
  - Parameter 8 KB Sector Erase (P8E)
  - Quad Page Programming (QPP)
  - OTP Byte Programming (OTPP)
- **Software Protected Mode (SPM):** The Block Protect (BP2, BP1, BP0) bits define the section of the memory array that can be read but not programmed or erased. Table 7.2 and Table 7.3 shows the sizes and address ranges of protected areas that are defined by Status Register bits BP2:BP0.
- **Hardware Protected Mode (HPM):** The Write Protect (W#/ACC) input and the Status Register Write Disable (SRWD) bit together provide write protection.
- **Clock Pulse Count:** The device verifies that all program, erase, and Write Register commands consist of a clock pulse count that is a multiple of eight before executing them.

Table 7.2 TBPROT = 0 (Starts Protection from TOP of Array)

Status Register Block			Memory Array				Protected Portion of Total Memory Area
BP2	BP1	BP0	Protected Address Range	Protected Sectors	Unprotected Address Range	Unprotected Sectors	
0	0	0	None	0	000000h-3FFFFFh	SA63:SA0	0
0	0	1	3F0000h-3FFFFFh	(1) SA63	000000h-3EFFFFh	SA62:SA0	1/64
0	1	0	3E0000h-3FFFFFh	(2) SA63:SA62	000000h-3DFFFFh	SA61:SA0	1/32
0	1	1	3C0000h-3FFFFFh	(4) SA63:SA60	000000h-3BFFFFh	SA59:SA0	1/16
1	0	0	380000h-3FFFFFh	(8) SA63:SA56	000000h-37FFFFh	SA55:SA0	1/8
1	0	1	300000h-3FFFFFh	(16) SA63:SA48	000000h-2FFFFFh	SA47:SA0	1/4
1	1	0	200000h-3FFFFFh	(32) SA63:SA32	000000h-1FFFFFh	SA31:SA0	1/2
1	1	1	000000h-3FFFFFh	(64) SA63:SA0	None	None	All

Table 7.3 TBPROT=1 (Starts Protection from BOTTOM of Array)

Status Register Block			Memory Array				Protected Portion of Total Memory Area
BP2	BP1	BP0	Protected Address Range	Protected Sectors	Unprotected Address Range	Unprotected Sectors	
0	0	0	None	0	000000h-3FFFFFh	SA0:SA63	0
0	0	1	000000h-00FFFFh	(1) SA0	010000h-3FFFFFh	SA1:SA63	1/64
0	1	0	000000h-01FFFFh	(2) SA0:SA1	020000h-3FFFFFh	SA2:SA63	1/32
0	1	1	000000h-03FFFFh	(4) SA0:SA3	040000h-3FFFFFh	SA4:SA63	1/16
1	0	0	000000h-07FFFFh	(8) SA0:SA7	080000h-3FFFFFh	SA8:SA63	1/8
1	0	1	000000h-0FFFFFh	(16) SA0:SA15	100000h-3FFFFFh	SA16:SA63	1/4
1	1	0	000000h-1FFFFFh	(32) SA0:SA31	200000h-3FFFFFh	SA32:SA63	1/2
1	1	1	000000h-3FFFFFh	(64) SA0:SA63	None	None	ALL

7.10 Hold Mode (HOLD#)

The Hold input (HOLD#) stops any serial communication with the device, but does not terminate any Write Registers, program or erase operation that is currently in progress.

The Hold mode starts on the falling edge of HOLD# if SCK is also low (see Figure 7.1, standard use). If the falling edge of HOLD# does not occur while SCK is low, the Hold mode begins after the next falling edge of SCK (non-standard use).

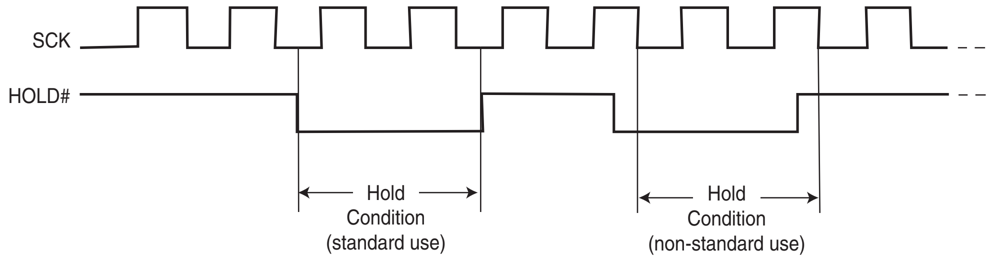
The Hold mode ends on the rising edge of HOLD# signal (standard use) if SCK is also low. If the rising edge of HOLD# does not occur while SCK is low, the Hold mode ends on the next falling edge of CLK (non-standard use) See Figure 7.1.

The SO output is high impedance, and the SI and SCK inputs are ignored (don't care) for the duration of the Hold mode.

CS# must remain low for the entire duration of the Hold mode to ensure that the device internal logic remains unchanged. If CS# goes high while the device is in the Hold mode, the internal logic is reset. To prevent the device from reverting to the Hold mode when device communication is resumed, HOLD# must be held high, followed by driving CS# low.

Note: The HOLD Mode feature is disabled during Quad I/O Mode.

Figure 7.1 Hold Mode Operation



7.11 Accelerated Programming Operation

The device offers accelerated program operations through the ACC function. This function is primarily intended to allow faster manufacturing throughput at the factory. If the system asserts V_{HH} on this pin, the device uses the higher voltage on the pin to reduce the time required for program operations. Removing V_{HH} from the W#/ACC pin returns the device to normal operation. Note that the W#/ACC pin must not be at V_{HH} for operations other than accelerated programming, or device damage may result. In addition, the W#/ACC pin must not be left floating or unconnected; inconsistent behavior of the device may result.

8. Sector Address Table

The Sector Address tables show the size of the memory array, sectors, and pages. The device uses pages to cache the program data before the data is programmed into the memory array. Each page or byte can be individually programmed (bits are changed from 1 to 0). The data is erased (bits are changed from 0 to 1) on a sub-sector, sector- or device-wide basis using the P4E/P8E, SE or BE commands. Table 8.1 and Table 8.2 show the starting and ending address for each sector. The complete set of sectors comprises the memory array of the Flash device.

Table 8.1 S25FL032P Sector Address Table TBPARM=0

Sector	Address range		Sector	Address range		Sector	Address range	
	Start address	End address		Start address	End address		Start address	End address
SA63	3F0000h	3FFFFFh	SA31	1F0000h	1FFFFFh	SS31	01F000h	01FFFFh
SA62	3E0000h	3EFFFFh	SA30	1E0000h	1EFFFFh	SS30	01E000h	01EFFFh
SA61	3D0000h	3DFFFFh	SA29	1D0000h	1DFFFFh	SS29	01D000h	01DFFFh
SA60	3C0000h	3CFFFFh	SA28	1C0000h	1CFFFFh	SS28	01C000h	01CFFFh
SA59	3B0000h	3BFFFFh	SA27	1B0000h	1BFFFFh	SS27	01B000h	01BFFFh
SA58	3A0000h	3AFFFFh	SA26	1A0000h	1AFFFFh	SS26	01A000h	01AFFFh
SA57	390000h	39FFFFh	SA25	190000h	19FFFFh	SS25	019000h	019FFFh
SA56	380000h	38FFFFh	SA24	180000h	18FFFFh	SS24	018000h	018FFFh
SA55	370000h	37FFFFh	SA23	170000h	17FFFFh	SS23	017000h	017FFFh
SA54	360000h	36FFFFh	SA22	160000h	16FFFFh	SS22	016000h	016FFFh
SA53	350000h	35FFFFh	SA21	150000h	15FFFFh	SS21	015000h	015FFFh
SA52	340000h	34FFFFh	SA20	140000h	14FFFFh	SS20	014000h	014FFFh
SA51	330000h	33FFFFh	SA19	130000h	13FFFFh	SS19	013000h	013FFFh
SA50	320000h	32FFFFh	SA18	120000h	12FFFFh	SS18	012000h	012FFFh
SA49	310000h	31FFFFh	SA17	110000h	11FFFFh	SS17	011000h	011FFFh
SA48	300000h	30FFFFh	SA16	100000h	10FFFFh	SS16	010000h	010FFFh
SA47	2F0000h	2FFFFFh	SA15	0F0000h	0FFFFFh	SS15	00F000h	00FFFFh
SA46	2E0000h	2EFFFFh	SA14	0E0000h	0EFFFFh	SS14	00E000h	00EFFFh
SA45	2D0000h	2DFFFFh	SA13	0D0000h	0DFFFFh	SS13	00D000h	00DFFFh
SA44	2C0000h	2CFFFFh	SA12	0C0000h	0CFFFFh	SS12	00C000h	00CFFFh
SA43	2B0000h	2BFFFFh	SA11	0B0000h	0BFFFFh	SS11	00B000h	00BFFFh
SA42	2A0000h	2AFFFFh	SA10	0A0000h	0AFFFFh	SS10	00A000h	00AFFFh
SA41	290000h	29FFFFh	SA9	090000h	09FFFFh	SS9	009000h	009FFFh
SA40	280000h	28FFFFh	SA8	080000h	08FFFFh	SS8	008000h	008FFFh
SA39	270000h	27FFFFh	SA7	070000h	07FFFFh	SS7	007000h	007FFFh
SA38	260000h	26FFFFh	SA6	060000h	06FFFFh	SS6	006000h	006FFFh
SA37	250000h	25FFFFh	SA5	050000h	05FFFFh	SS5	005000h	005FFFh
SA36	240000h	24FFFFh	SA4	040000h	04FFFFh	SS4	004000h	004FFFh
SA35	230000h	23FFFFh	SA3	030000h	03FFFFh	SS3	003000h	003FFFh
SA34	220000h	22FFFFh	SA2	020000h	02FFFFh	SS2	002000h	002FFFh
SA33	210000h	21FFFFh	SA1	010000h	01FFFFh	SS1	001000h	001FFFh
SA32	200000h	20FFFFh	SA0	000000h	00FFFFh	SS0	000000h	000FFFh

Note

Sector SA0 is split up into sub-sectors SS0 - SS15 (dark gray shading)

Sector SA1 is split up into sub-sectors SS16 - SS31(light gray shading)

Table 8.2 S25FL032P Sector Address Table TBPARM=1

Sector	Address Range		Sector	Address Range		Sector	Address Range	
	Start Address	End Address		Start Address	End Address		Start Address	End Address
SS31	3FF000h	3FFFFFh	SA63	3F0000h	3FFFFFh	SA31	1F0000h	1FFFFFh
SS30	3FE000h	3FEFFFh	SA62	3E0000h	3EFFFFh	SA30	1E0000h	1EFFFFh
SS29	3FD000h	3FDFFFh	SA61	3D0000h	3DFFFFh	SA29	1D0000h	1DFFFFh
SS28	3FC000h	3FCFFFh	SA60	3C0000h	3CFFFFh	SA28	1C0000h	1CFFFFh
SS27	3FB000h	3FBFFFh	SA59	3B0000h	3BFFFFh	SA27	1B0000h	1BFFFFh
SS26	3FA000h	3FAFFFh	SA58	3A0000h	3AFFFFh	SA26	1A0000h	1AFFFFh
SS25	3F9000h	3F9FFFh	SA57	390000h	39FFFFh	SA25	190000h	19FFFFh
SS24	3F8000h	3F8FFFh	SA56	380000h	38FFFFh	SA24	180000h	18FFFFh
SS23	3F7000h	3F7FFFh	SA55	370000h	37FFFFh	SA23	170000h	17FFFFh
SS22	3F6000h	3F6FFFh	SA54	360000h	36FFFFh	SA22	160000h	16FFFFh
SS21	3F5000h	3F5FFFh	SA53	350000h	35FFFFh	SA21	150000h	15FFFFh
SS20	3F4000h	3F4FFFh	SA52	340000h	34FFFFh	SA20	140000h	14FFFFh
SS19	3F3000h	3F3FFFh	SA51	330000h	33FFFFh	SA19	130000h	13FFFFh
SS18	3F2000h	3F2FFFh	SA50	320000h	32FFFFh	SA18	120000h	12FFFFh
SS17	3F1000h	3F1FFFh	SA49	310000h	31FFFFh	SA17	110000h	11FFFFh
SS16	3F0000h	3F0FFFh	SA48	300000h	30FFFFh	SA16	100000h	10FFFFh
SS15	3EF000h	3EFFFFh	SA47	2F0000h	2FFFFFh	SA15	0F0000h	0FFFFFh
SS14	3EE000h	3EEFFFh	SA46	2E0000h	2EFFFFh	SA14	0E0000h	0EFFFFh
SS13	3ED000h	3EDFFFh	SA45	2D0000h	2DFFFFh	SA13	0D0000h	0DFFFFh
SS12	3EC000h	3ECFFFh	SA44	2C0000h	2CFFFFh	SA12	0C0000h	0CFFFFh
SS11	3EB000h	3EBFFFh	SA43	2B0000h	2BFFFFh	SA11	0B0000h	0BFFFFh
SS10	3EA000h	3EAFFFh	SA42	2A0000h	2AFFFFh	SA10	0A0000h	0AFFFFh
SS9	3E9000h	3E9FFFh	SA41	290000h	29FFFFh	SA9	090000h	09FFFFh
SS8	3E8000h	3E8FFFh	SA40	280000h	28FFFFh	SA8	080000h	08FFFFh
SS7	3E7000h	3E7FFFh	SA39	270000h	27FFFFh	SA7	070000h	07FFFFh
SS6	3E6000h	3E6FFFh	SA38	260000h	26FFFFh	SA6	060000h	06FFFFh
SS5	3E5000h	3E5FFFh	SA37	250000h	25FFFFh	SA5	050000h	05FFFFh
SS4	3E4000h	3E4FFFh	SA36	240000h	24FFFFh	SA4	040000h	04FFFFh
SS3	3E3000h	3E3FFFh	SA35	230000h	23FFFFh	SA3	030000h	03FFFFh
SS2	3E2000h	3E2FFFh	SA34	220000h	22FFFFh	SA2	020000h	02FFFFh
SS1	3E1000h	3E1FFFh	SA33	210000h	21FFFFh	SA1	010000h	01FFFFh
SS0	3E0000h	3E0FFFh	SA32	200000h	20FFFFh	SA0	000000h	00FFFFh

Note
Sector SA62 is split up into sub-sectors SS0 - SS15 (dark gray shading)
Sector SA63 is split up into sub-sectors SS16 - SS31 (light gray shading)

9. Command Definitions

The host system must shift all commands, addresses, and data in and out of the device, beginning with the most significant bit. On the first rising edge of SCK after CS# is driven low, the device accepts the one-byte command on SI (all commands are one byte long), most significant bit first. Each successive bit is latched on the rising edge of SCK. Table 9.1 lists the complete set of commands.

Every command sequence begins with a one-byte command code. The command may be followed by address, data, both, or nothing, depending on the command. CS# must be driven high after the last bit of the command sequence has been written.

The Read Data Bytes (READ), Read Data Bytes at Higher Speed (FAST_READ), Dual Output Read (DOR), Quad Output Read (QOR), Dual I/O High Performance Read (DIOR), Quad I/O High Performance Read (QIOR), Read Status Register (RDSR), Read Configuration Register (RCR), Read OTP Data (OTPR), Read Manufacturer and Device ID (READ_ID), Read Identification (RDID) and Release from Deep Power-Down and Read Electronic Signature (RES) command sequences are followed by a data output sequence on SO. CS# can be driven high after any bit of the sequence is output to terminate the operation.

The Page Program (PP), Quad Page Program (QPP), 64 KB Sector Erase (SE), 4 KB Parameter Sector Erase (P4E), 8 KB Parameter Sector Erase (P8E), Bulk Erase (BE), Write Status and Configuration Registers (WRR), Program OTP space (OTPP), Write Enable (WREN), or Write Disable (WRDI) commands require that CS# be driven high at a byte boundary, otherwise the command is not executed. Since a byte is composed of eight bits, CS# must therefore be driven high when the number of clock pulses after CS# is driven low is an exact multiple of eight.

The device ignores any attempt to access the memory array during a Write Registers, program, or erase operation, and continues the operation uninterrupted.

The instruction set is listed in Table 9.1.

Table 9.1 Instruction Set

Operation	Command	One byte Command Code	Description	Address Byte Cycle	Mode Bit Cycle	Dummy Byte Cycle	Data Byte Cycle
Read	READ	(03h) 0000 0011	Read Data bytes	3	0	0	1 to ∞
	FAST_READ	(0Bh) 0000 1011	Read Data bytes at Fast Speed	3	0	1	1 to ∞
	DOR	(3Bh) 0011 1011	Dual Output Read	3	0	1	1 to ∞
	QOR	(6Bh) 0110 1011	Quad Output Read	3	0	1	1 to ∞
	DIOR	(BBh) 1011 1011	Dual I/O High Performance Read	3	1	0	1 to ∞
	QIOR	(EBh) 1110 1111	Quad I/O High Performance Read	3	1	2	1 to ∞
	RDID	(9Fh) 1001 1111	Read Identification	0	0	0	1 to 81
	READ_ID	(90h) 1001 0000	Read Manufacturer and Device Identification	3	0	0	1 to ∞
Write Control	WREN	(06h) 0000 0110	Write Enable	0	0	0	0
	WRDI	(04h) 0000 0100	Write Disable	0	0	0	0
Erase	P4E	(20h) 0010 0000	4 KB Parameter Sector Erase	3	0	0	0
	P8E	(40h) 0100 0000	8 KB (two 4KB) Parameter Sector Erase	3	0	0	0
	SE	(D8h) 1101 1000	64KB Sector Erase	3	0	0	0
	BE	(60h) 0110 0000 or (C7h) 1100 0111	Bulk Erase	0	0	0	0
Program	PP	(02h) 0000 0010	Page Programming	3	0	0	1 to 256
	QPP	(32h) 0011 0010	Quad Page Programming	3	0	0	1 to 256
Status & Configuration Register	RDSR	(05h) 0000 0101	Read Status Register	0	0	0	1 to ∞
	WRR	(01h) 0000 0001	Write (Status & Configuration) Register	0	0	0	1 to 2
	RCR	(35h) 0011 0101	Read Configuration Register (CFG)	0	0	0	1 to ∞
	CLSR	(30h) 0011 0000	Reset the Erase and Program Fall Flag (SRS and SR6) and restore normal operation)	0	0	0	1
Power Saving	DP	(B9h) 1011 1001	Deep Power-Down	0	0	0	0
	RES	(ABh) 1010 1011	Release from Deep Power-Down Mode	0	0	0	0
		(ABh) 1010 1011	Release from Deep Power-Down and Read Electronic Signature	0	0	3	1 to ∞
OTP	OTPP	(42h) 0100 0010	Program one byte of data in OTP memory space	3	0	0	1
	OTPR	(4Bh) 0100 1011	Read data in the OTP memory space	3	0	1	1 to ∞

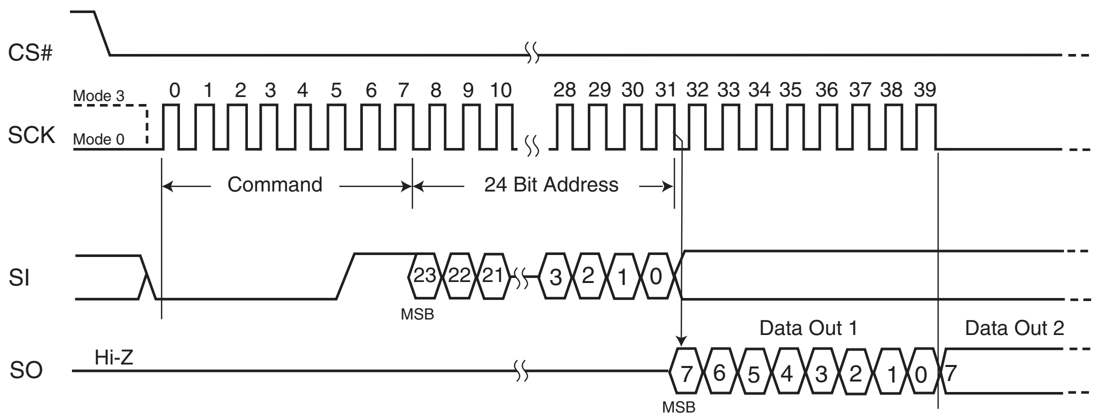
9.1 Read Data Bytes (READ)

The Read Data Bytes (READ) command reads data from the memory array at the frequency (f_{SCK}) presented at the SCK input, with a maximum speed of 40 MHz. The host system must first select the device by driving CS# low. The READ command is then written to SI, followed by a 3 byte address (A23-A0). Each bit is latched on the rising edge of SCK. The memory array data, at that address, are output serially on SO at a frequency f_{SCK}, on the falling edge of SCK.

Figure 9.1 and Table 9.1 on page 22 detail the READ command sequence. The first address byte specified can start at any location of the memory array. The device automatically increments to the next higher address after each byte of data is output. The entire memory array can therefore be read with a single READ command. When the highest address is reached, the address counter reverts to 00000h, allowing the read sequence to continue indefinitely.

The READ command is terminated by driving CS# high at any time during data output. The device rejects any READ command issued while it is executing a program, erase, or Write Registers operation, and continues the operation uninterrupted.

Figure 9.1 Read Data Bytes (READ) Command Sequence



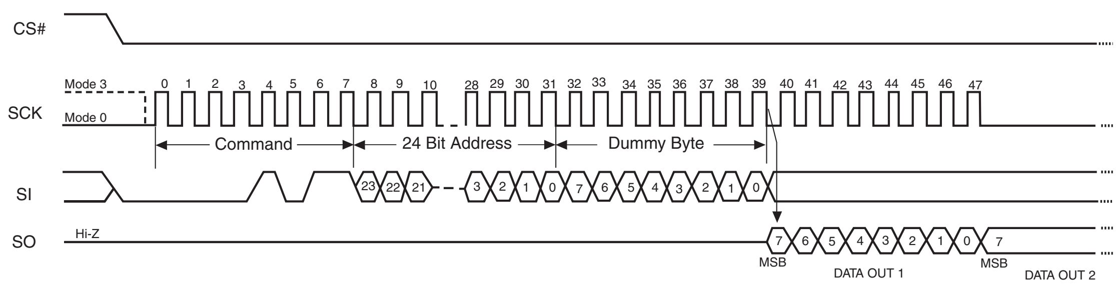
9.2 Read Data Bytes at Higher Speed (FAST_READ)

The FAST_READ command reads data from the memory array at the frequency (f_{SCK}) presented at the SCK input, with a maximum speed of 104 MHz. The host system must first select the device by driving CS# low. The FAST_READ command is then written to SI, followed by a 3 byte address (A23-A0) and a dummy byte. Each bit is latched on the rising edge of SCK. The memory array data, at that address, are output serially on SO at a frequency f_{SCK}, on the falling edge of SCK.

The FAST_READ command sequence is shown in Figure 9.2 and Table 9.1 on page 22. The first address byte specified can start at any location of the memory array. The device automatically increments to the next higher address after each byte of data is output. The entire memory array can therefore be read with a single FAST_READ command. When the highest address is reached, the address counter reverts to 000000h, allowing the read sequence to continue indefinitely.

The FAST_READ command is terminated by driving CS# high at any time during data output. The device rejects any FAST_READ command issued while it is executing a program, erase, or Write Registers operation, and continues the operation uninterrupted.

Figure 9.2 Read Data Bytes at Higher Speed (FAST_READ) Command Sequence



9.3 Dual Output Read Mode (DOR)

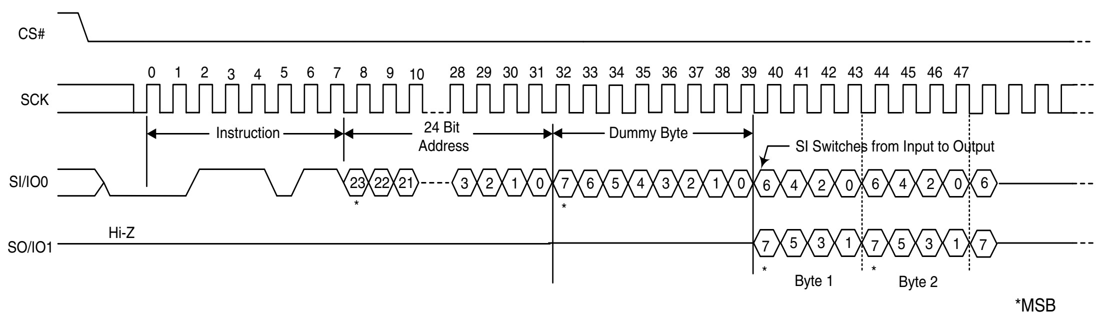
The Dual Output Read instruction is similar to the FAST_READ instruction, except that the data is shifted out 2 bits at a time using 2 pins (SI/IO0 and SO/IO1) instead of 1 bit, at a maximum frequency of 80 MHz. The Dual Output Read mode effectively doubles the data transfer rate compared to the FAST_READ instruction.

The host system must first select the device by driving CS# low. The Dual Output Read command is then written to SI, followed by a 3-byte address (A23-A0) and a dummy byte. Each bit is latched on the rising edge of SCK. Then the memory contents, at the address that is given, are shifted out two bits at a time through the IO0 (SI) & IO1 (SO) pins at a frequency f_{SCK} on the falling edge of SCK.

The Dual Output Read command sequence is shown in Figure 9.3 and Table 9.1 on page 22. The first address byte specified can start at any location of the memory array. The device automatically increments to the next higher address after each byte of data is output. The entire memory array can therefore be read with a single Dual Output Read command. When the highest address is reached, the address counter reverts to 00000h, allowing the read sequence to continue indefinitely.

The Dual Output Read command is terminated by driving CS# high at any time during data output. The device rejects any Dual Output Read command issued while it is executing a program, erase, or Write Registers operation, and continues the operation uninterrupted.

Figure 9.3 Dual Output Read Instruction Sequence



9.4 Quad Output Read Mode (QOR)

The Quad Output Read instruction is similar to the FAST_READ instruction, except that the data is shifted out 4 bits at a time using 4 pins (SI/IO0, SO/IO1, W#/ACC/IO2 and HOLD#/IO3) instead of 1 bit, at a maximum frequency of 80 MHz. The Quad Output Read mode effectively doubles the data transfer rate compared to the Dual Output Read instruction, and is four times the data transfer rate of the FAST_READ instruction.

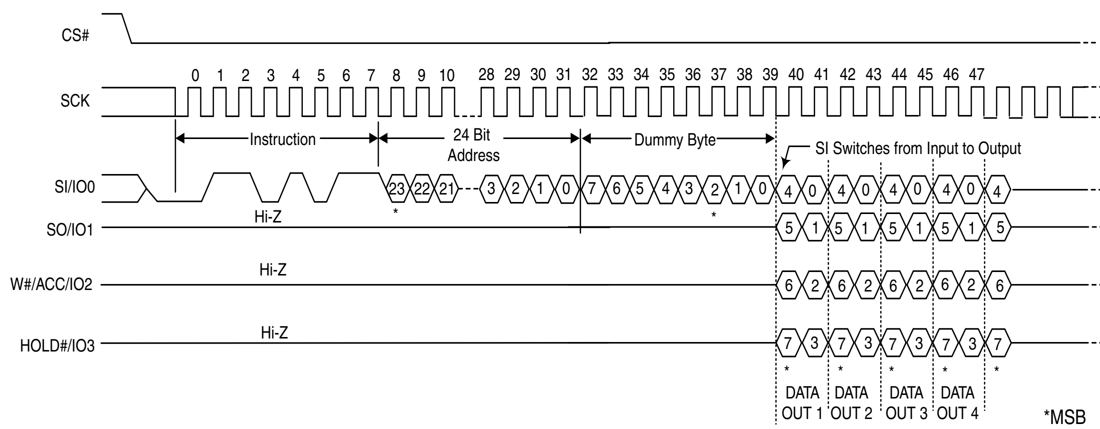
The host system must first select the device by driving CS# low. The Quad Output Read command is then written to SI, followed by a 3-byte address (A23-A0) and a dummy byte. Each bit is latched on the rising edge of SCK. Then the memory contents, at the address that are given, are shifted out four bits at a time through IO0 (SI), IO1 (SO), IO2 (W#/ACC), and IO3 (HOLD#) pins at a frequency f_{SCK} on the falling edge of SCK.

The Quad Output Read command sequence is shown in Figure 9.4 and Table 9.1 on page 22. The first address byte specified can start at any location of the memory array. The device automatically increments to the next higher address after each byte of data is output. The entire memory array can therefore be read with a single Quad Output Read command. When the highest address is reached, the address counter reverts to 00000h, allowing the read sequence to continue indefinitely.

The Quad Output Read command is terminated by driving CS# high at any time during data output. The device rejects any Quad Output Read command issued while it is executing a program, erase, or Write Registers operation, and continues the operation uninterrupted.

The Quad bit of Configuration Register must be set (CR Bit1 = 1) to enable the Quad mode capability of the S25FL device.

Figure 9.4 Quad Output Read Instruction Sequence



9.5 DUAL I/O High Performance Read Mode (DIOR)

The Dual I/O High Performance Read instruction is similar to the Dual Output Read instruction, except that it improves throughput by allowing input of the address bits (A23-A0) using 2 bits per SCK via two input pins (SI/IO2 and SO/IO1), at a maximum frequency of 80 MHz.

The host system must first select the device by driving CS# low. The Dual I/O High Performance Read command is then written to SI, followed by a 3-byte address (A23-A0) and a 1-byte Mode instruction, with two bits latched on the rising edge of SCK. Then the memory contents, at the address that is given, are shifted out two bits at a time through IO0 (SI) and IO1 (SO).

The DUAL I/O High Performance Read command sequence is shown in Figure 9.5 and Table 9.1 on page 22. The first address byte specified can start at any location of the memory array. The device automatically increments to the next higher address after each byte of data is output. The entire memory array can therefore be read with a single DUAL I/O High Performance Read command. When the highest address is reached, the address counter reverts to 00000h, allowing the read sequence to continue indefinitely.

In addition, address jumps can be done without exiting the Dual I/O High Performance Mode through the setting of the Mode bits (after the Address (A23-0) sequence, as shown in Figure 9.5). This added feature removes the need for the instruction sequence and greatly improves code execution (XIP). The upper nibble (bits 7-4) of the Mode bits control the length of the next Dual I/O High Performance instruction through the inclusion or exclusion of the first byte instruction code. The lower nibble (bits 3-0) of the Mode bits are DON'T CARE ("x"). If the Mode bits equal Axh, then the device remains in Dual I/O High Performance Read Mode and the next address can be entered (after CS# is raised high and then asserted low) without requiring the BBh instruction opcode, as shown in Figure 9.6, thus eliminating eight cycles for the instruction sequence. However, if the Mode bits are any value other than Axh, then the next instruction (after CS# is raised high and then asserted low) requires the instruction sequence, which is normal operation. The following sequences will release the device from Dual I/O High Performance Read mode; after which, the device can accept standard SPI instructions:

1. During the Dual I/O High Performance Instruction Sequence, if the Mode bits are any value other than Axh, then the next time CS# is raised high and then asserted low, the device will be released from Dual I/O High Performance Read mode.
2. Furthermore, during any operation, if CS# toggles high to low to high for eight cycles (or less) **and** data input (IO0 & IO1) are not set for a valid instruction sequence, then the device will be released from Dual I/O High Performance Read mode.

It is important that the I/O pins be set to high-impedance prior to the falling edge of the first data out clock.

The read instruction can be terminated by driving the CS# pin to the logic high state. The CS# pin can be driven high at any time during data output to terminate a read operation.

Figure 9.5 DUAL I/O High Performance Read Instruction Sequence

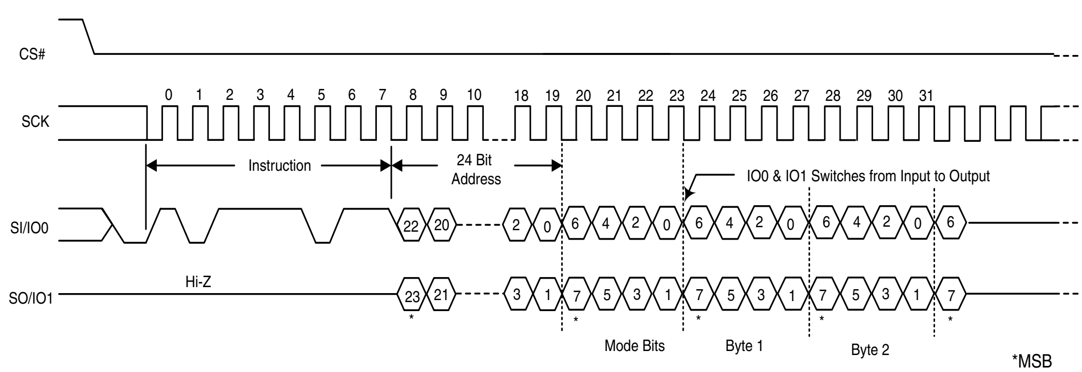
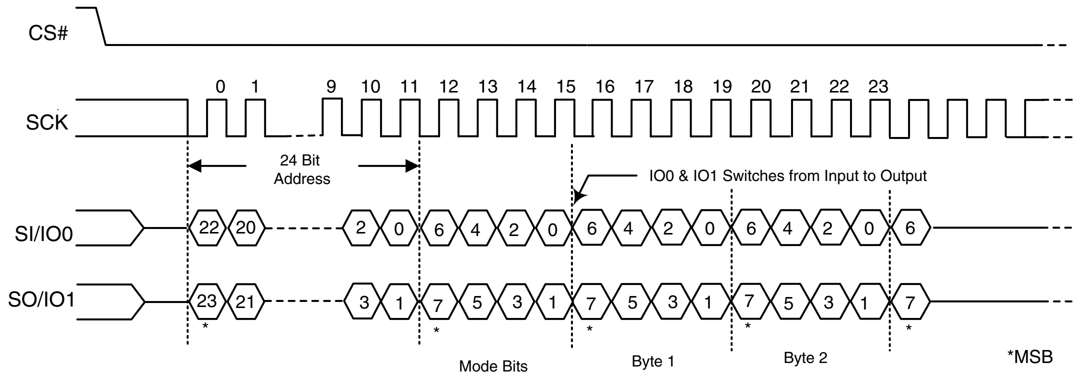


Figure 9.6 Continuous Dual I/O High Performance Read Instruction Sequence



9.6 Quad I/O High Performance Read Mode (QIOR)

The Quad I/O High Performance Read instruction is similar to the Quad Output Read instruction, except that it further improves throughput by allowing input of the address bits (A23-A0) using 4 bits per SCK via four input pins (SI/IO0, SO/IO1, W#/ACC/IO2 and HOLD#/IO3), at a maximum frequency of 80 MHz.

The host system must first select the device by driving CS# low. The Quad I/O High Performance Read command is then written to SI, followed by a 3-byte address (A23-A0) and a 1-byte Mode instruction, with four bits latched on the rising edge of SCK. Note that four dummy clocks are required prior to the data input. Then the memory contents, at the address that is given, are shifted out four bits at a time through IO0 (SI), IO1 (SO), IO2 (W#/ACC), and IO3 (HOLD#).

The Quad I/O High Performance Read command sequence is shown in Figure 9.7 and Table 9.1 on page 22. The first address byte specified can start at any location of the memory array. The device automatically increments to the next higher address after each byte of data is output. The entire memory array can therefore be read with a single Quad I/O High Performance Read command. When the highest address is reached, the address counter reverts to 00000h, allowing the read sequence to continue indefinitely.

In addition, address jumps can be done without exiting the Quad I/O High Performance Mode through the setting of the Mode bits (after the Address (A23-0) sequence, as shown in Figure 9.7). This added feature the removes the need for the instruction sequence and greatly improves code execution (XIP). The upper nibble (bits 7-4) of the Mode bits control the length of the next Quad I/O High Performance instruction through the inclusion or exclusion of the first byte instruction code. The lower nibble (bits 3-0) of the Mode bits are DON'T CARE ("x"). If the Mode bits equal Axh, then the device remains in Quad I/O High Performance Read Mode and the next address can be entered (after CS# is raised high and then asserted low) without requiring the EBh instruction opcode, as shown in Figure 9.8, thus eliminating eight cycles for the instruction sequence. The following sequences will release the device from Quad I/O High Performance Read mode; after which, the device can accept standard SPI instructions:

1. During the Quad I/O High Performance Instruction Sequence, if the Mode bits are any value other than Axh, then the next time CS# is raised high and then asserted low the device will be released from Quad I/O High Performance Read mode.
2. Furthermore, during any operation, if CS# toggles high to low to high for eight cycles (or less) **and** data input (IO0, IO1, IO2, & IO3) are not set for a valid instruction sequence, then the device will be released from Quad I/O High Performance Read mode.

It is important that the I/O pins be set to high-impedance prior to the falling edge of the first data out clock.

The read instruction can be terminated by driving the CS# pin to the logic high state. The CS# pin can be driven high at any time during data output to terminate a read operation.

Figure 9.7 QUAD I/O High Performance Instruction Sequence

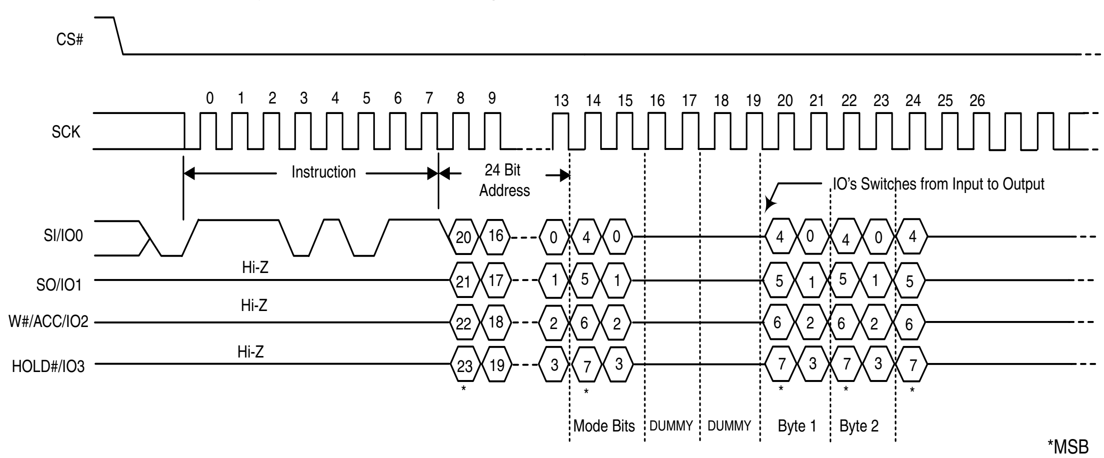
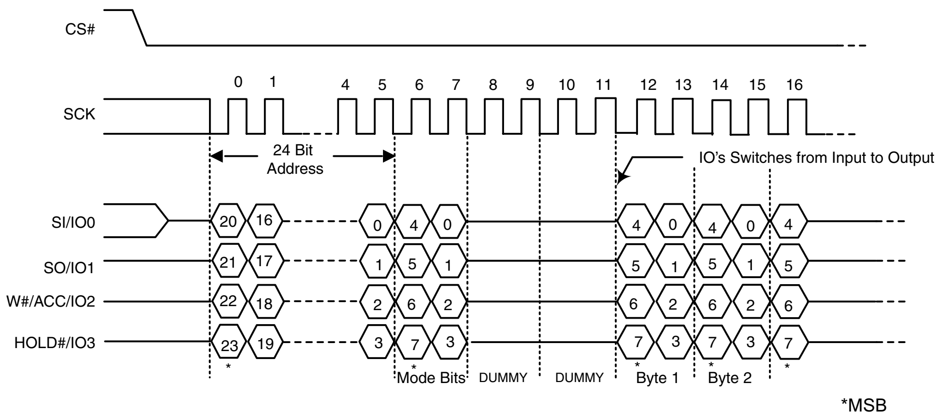


Figure 9.8 Continuous QUAD I/O High Performance Instruction Sequence



9.7 Read Identification (RDID)

The Read Identification (RDID) command outputs the one-byte manufacturer identification, followed by the two-byte device identification and the bytes for the Common Flash Interface (CFI) tables. The manufacturer identification is assigned by JEDEC; for Spansion devices, it is 01h. The device identification (2 bytes) and CFI bytes are assigned by the device manufacturer.

See Table 9.2 on page 31 for device ID data.

The Common Flash Interface (CFI) specification outlines device and host system software interrogation handshake, which allows vendor-specified software algorithms to be used for entire families of devices. Software support can then be device-independent, JEDEC ID-independent, and forward- and backward-compatible for the specified flash device families. Flash vendors can standardize their existing interfaces for long-term compatibility. The system can read CFI information at the addresses given in Table 9.3.

The host system must first select the device by driving CS# low. The RDID command is then written to SI, and each bit is latched on the rising edge of SCK. The 3-byte device identification data is output from the memory array on SO at a frequency f_{SCK}, on the falling edge of SCK.

The RDID command sequence is shown in Figure 9.9 and Table 9.1 on page 22.

Driving CS# high after the device identification data has been read at least once terminates the RDID command. Driving CS# high at any time during data output (for example, while reading the extended CFI bytes), also terminates the RDID operation.

The device rejects any RDID command issued while it is executing a program, erase, or Write Registers operation, and continues the operation uninterrupted.

Figure 9.9 Read Identification (RDID) Command Sequence and Data-Out Sequence

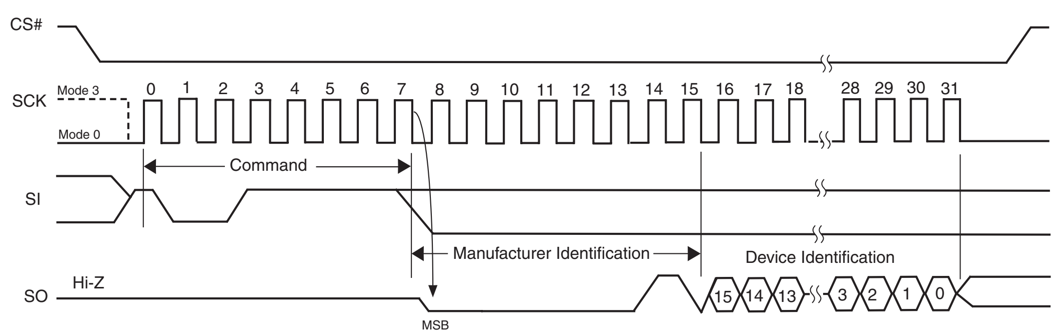


Table 9.2 Manufacturer & Device ID - RDID (JEDEC 9Fh):

Device	Manuf. ID	Device Id		# Extended bytes
	Byte 0	Byte 1	Byte 2	Byte 3
S25FL032P SPI Flash	01h	02h	15h	4Dh

Notes
1. *Byte 0 is Manufacturer ID of Spansion.*
2. *Byte 1 & 2 is Device Id.*
3. *Byte 3 is Extended Device Information String Length, to indicate how many Extended Device Information bytes will follow.*
4. *Bytes 4, 5 and 6 are Spansion reserved (do not use).*
5. *For Bytes 07h-0Fh and 3Dh-3Fh, the data will be read as 0xFF.*
6. *Bytes 10h-50h are factory programmed per JEDEC standard.*

Table 9.3 Product Group CFI Query Identification String

Byte	Data	Description
10h 11h 12h	51h 52h 59h	Query Unique ASCII string "QRY"
13h 14h	02h 00h	Primary OEM Command Set
15h 16h	40h 00h	Address for Primary Extended Table
17h 18h	00h 00h	Alternate OEM Command Set (00h = none exists)
19h 1Ah	00h 00h	Address for Alternate OEM Extended Table (00h = none exists)

Table 9.4 Product Group CFI System Interface String

Byte	Data	Description
1Bh	27h	V_{CC} Min. (erase/program): (D7-D4: Volt, D3-D0: 100 mV)
1Ch	36h	V_{CC} Max. (erase/program): (D7-D4: Volt, D3-D0: 100 mV)
1Dh	00h	V_{PP} Min. voltage (00h = no VPP pin present)
1Eh	00h	V_{PP} Max. voltage (00h = no VPP pin present)
1Fh	0Bh	Typical timeout per single byte program 2^N µs
20h	0Bh	Typical timeout for Min. size Page program 2^N µs (00h = not supported)
21h	09h	Typical timeout per individual sector erase 2^N ms
22h	0Fh	Typical timeout for full chip erase 2^N ms (00h = not supported)
23h	01h	Max. timeout for byte program 2^N times typical
24h	01h	Max. timeout for page program 2^N times typical
25h	02h	Max. timeout per individual sector erase 2^N times typical
26h	01h	Max. timeout for full chip erase 2^N times typical (00h = not supported)

Table 9.5 Product Group CFI Device Geometry Definition

Byte	Data	Description
27h	16h	Device Size = 2^N byte;
28h	05h	Flash Device Interface Description; 00h = x8 only 01h = x16 only 02h = x8/x16 capable 03h = x32 only 04h = Single I/O SPI, 3-byte address 05h = Multi I/O SPI, 3-byte address
29h	00h	
2Ah	08h	Max. number of bytes in multi-byte write = 2^N (00 = not supported)
2Bh	00h	
2Ch	02h	Number of Erase Block Regions within device 1 = Uniform Device, 2 = Parameter Block
2Dh	1Fh	Erase Block Region 1 Information (refer to CFI publication 100)
2Eh	00h	
2Fh	10h	
30h	00h	
31h	3Dh	Erase Block Region 2 Information (refer to CFI publication 100)
32h	00h	
33h	00h	
34h	01h	
35h	00h	Erase Block Region 3 Information (refer to CFI publication 100)
36h	00h	
37h	00h	
38h	00h	
39h	00h	Erase Block Region 4 Information (refer to CFI publication 100)
3Ah	00h	
3Bh	00h	
3Ch	00h	

Table 9.6 Product Group CFI Primary Vendor-Specific Extended Query

Byte	Data	Description
40h	50h	Query-unique ASCII string “PRI”
41h	52h	
42h	49h	
43h	31h	Major version number, ASCII
44h	33h	Minor version number, ASCII
45h	15h	Address Sensitive Unlock (Bits 1-0) 00b = Required, 01b = Not Required Process Technology (Bits 5-2) 0000b = 0.23 µm Floating Gate 0001b = 0.17 µm Floating Gate 0010b = 0.23 µm MirrorBit 0010b = 0.20 µm MirrorBit 0011b = 0.11 µm Floating Gate 0100b = 0.11 µm MirrorBit 0101b = 0.09 µm MirrorBit 1000b = 0.065 µm MirrorBit
46h	00h	Erase Suspend 0 = Not Supported, 1 = Read Only, 2 = Read & Write
47h	01h	Sector Protect 00 = Not Supported, X = Number of sectors in per smallest group
48h	00h	Temporary Sector Unprotect 00 = Not Supported, 01 = Supported
49h	05h	Sector Protect/Unprotect Scheme 04 = High Voltage Method 05 = Software Command Locking Method 08 = Advanced Sector Protection Method
4Ah	00h	Simultaneous Operation 00 = Not Supported, X = Number of Sectors outside Bank 1
4Bh	01h	Burst Mode Type 00 = Not Supported, 01 = Supported
4Ch	03h	Page Mode Type 00 = Not Supported, 01 = 4 Word Page, 02 = 8 Word Page, 03 = 256 Byte Page
4Dh	85h	ACC (Acceleration) Supply Minimum 00 = Not Supported, (D7-D4: Volt, D3-D0: 100 mV)
4Eh	95h	ACC (Acceleration) Supply Maximum 00 = Not Supported, (D7-D4: Volt, D3-D0: 100 mV)
4Fh	07h	W# Protection 07 = Uniform Device with Top or Bottom Write Protect (user select)
50h	00h	Program Suspend 00 = Not Supported, 01 = Supported

Note

CFI data related to V_{CC} and time-outs may differ from actual V_{CC} and time-outs of the product. Please consult the Ordering Information tables to obtain the V_{CC} range for particular part numbers. Please consult the *AC Characteristics on page 56* *for typical timeout specifications.*

9.8 Read-ID (READ_ID)

The READ_ID instruction provides the S25FL032P manufacturer and device information and is provided as an alternative to the Release from Deep Power-Down and Read Electronic Signature (RES), and the JEDEC Read Identification (RDID) commands.

The instruction is initiated by driving the CS# pin low and shifting in (via the SI input pin) the instruction code "90h" followed by a 24-bit address (which is either 00000h or 00001h). Following this, the Manufacturer ID and the Device ID are shifted out on the SO output pin starting after the falling edge of the SCK serial clock input signal. If the 24-bit address is set to 000000h, the Manufacturer ID is read out first followed by the Device ID. If the 24-bit address is set to 000001h, then the Device ID is read out first followed by the Manufacturer ID. The Manufacturer ID and the Device ID are always shifted out on the SO output pin with the MSB first, as shown in Figure 10-14. Once the device is in Read-ID mode, the Manufacturer ID and Device ID output data toggles between address 000000H and 000001H until terminated by a low to high transition on the CS# input pin. The maximum clock frequency for the Read-ID (90h) command is at 104 MHz (FAST_READ). The Manufacturer ID & Device ID is output continuously until terminated by a low to high transition on CS# chip select input pin.

Figure 9.10 Read-ID (RDID) Command Timing Diagram

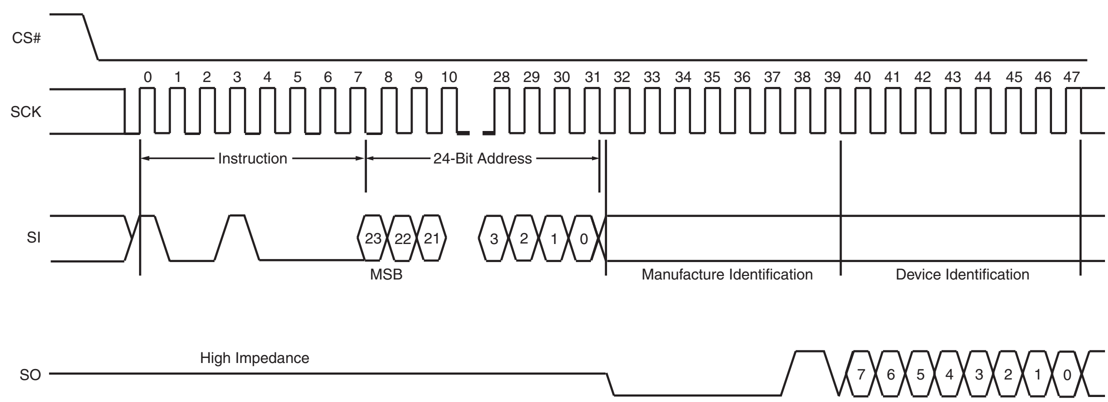


Table 9.7 READ_ID Data-Out Sequence

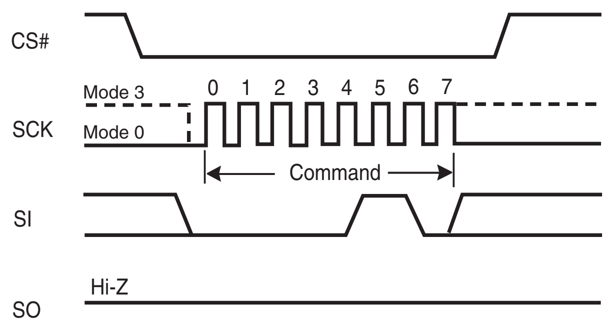
	Address	Uniform
Manufacturer Identification	00000h	01h
Device Identification	00001h	15h

9.9 Write Enable (WREN)

The Write Enable (WREN) command (see Figure 9.11) sets the Write Enable Latch (WEL) bit to a 1, which enables the device to accept a Write Status Register, program, or erase command. The WEL bit must be set prior to every Page Program (PP), Quad Page Program (QPP), Parameter Sector Erase (P4E, P8E), Erase (SE or BE), Write Registers (WRR) and OTP Program (OTPP) command.

The host system must first drive CS# low, write the WREN command, and then drive CS# high.

Figure 9.11 Write Enable (WREN) Command Sequence



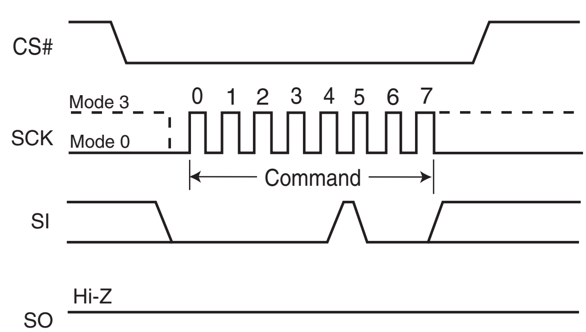
9.10 Write Disable (WRDI)

The Write Disable (WRDI) command (see Figure 9.12) resets the Write Enable Latch (WEL) bit to a 0, which disables the device from accepting a Page Program (PP), Quad Page Program (QPP), Parameter Sector Erase (P4E, P8E), Erase (SE, BE), Write Registers (WRR) and OTP Program (OTPP) command. The host system must first drive CS# low, write the WRDI command, and then drive CS# high.

Any of following conditions resets the WEL bit:

- Power-up
- Write Disable (WRDI) command completion
- Write Registers (WRR) command completion
- Page Program (PP) command completion
- Quad Page Program (QPP) completion
- Parameter Sector Erase (P4E, P8E) completion
- Sector Erase (SE) command completion
- Bulk Erase (BE) command completion
- OTP Program (OTPP) completion

Figure 9.12 Write Disable (WRDI) Command Sequence



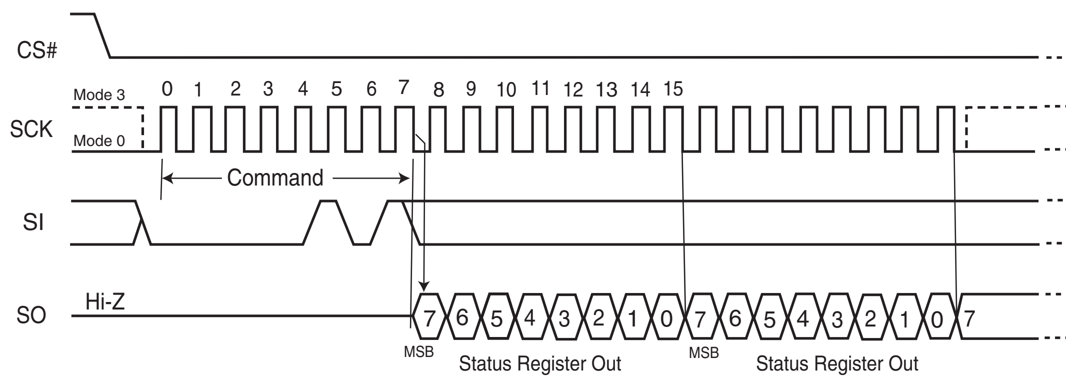
9.11 Read Status Register (RDSR)

The Read Status Register (RDSR) command outputs the state of the Status Register bits. Table 9.8 shows the status register bits and their functions. The RDSR command may be written at any time, even while a program, erase, or Write Registers operation is in progress. The host system should check the Write In Progress (WIP) bit before sending a new command to the device if an operation is already in progress. Figure 9.13 shows the RDSR command sequence, which also shows that it is possible to read the Status Register continuously until CS# is driven high.

Table 9.8 S25FL032P Status Register

Bit	Status Register Bit	Bit Function	Description
7	SRWD	Status Register Write Disable	1 = Protects when W#/ACC is low 0 = No protection, even when W#/ACC is low
6	P_ERR	Programming Error Occurred	0 = No Error 1 = Error occurred
5	E_ERR	Erase Error Occurred	0 = No Error 1 = Error occurred
4	BP2	Block Protect	Protects selected Block from Program or Erase
3	BP1		
2	BP0		
1	WEL	Write Enable Latch	1 = Device accepts Write Registers, program or erase commands 0 = Ignores Write Registers, program or erase commands
0	WIP	Write in Progress	1 = Device Busy a Write Registers, program or erase operation is in progress 0 = Ready. Device is in standby mode and can accept commands.

Figure 9.13 Read Status Register (RDSR) Command Sequence



The following describes the status and control bits of the Status Register.

Write In Progress (WIP) bit: Indicates whether the device is busy performing a Write Registers, program, or erase operation. This bit is read-only, and is controlled internally by the device. If WIP is 1, one of these operations is in progress; if WIP is 0, no such operation is in progress. This bit is a Read-only bit.

Write Enable Latch (WEL) bit: Determines whether the device will accept and execute a Write Registers, program, or erase command. When set to 1, the device accepts these commands; when set to 0, the device rejects the commands. This bit is set to 1 by writing the WREN command, and set to 0 by the WRDI command, and is also automatically reset to 0 after the completion of a Write Registers, program, or erase operation, and after a power down/power up sequence. WEL cannot be directly set by the WRR command.

Block Protect (BP2, BP1, BP0) bits: Define the portion of the memory area that will be protected against any changes to the stored data. The Block Protection (BP2, BP1, BP0) bits are either volatile or non-volatile, depending on the state of the non-volatile bit BPNV in the Configuration register. The Block Protection (BP2, BP1, BP0) bits are written with the Write Registers (WRR) instruction. When one or more of the Block Protect (BP2, BP1, BP0) bits is set to 1's, the relevant memory area is protected against Page Program (PP), Parameter Sector Erase (P4E, P8E), Sector Erase (SE), Quad Page Programming (QPP) and Bulk Erase (BE) instructions. If the Hardware Protected mode is enabled, BP2:BP0 cannot be changed.

The Bulk Erase (BE) instruction can be executed only when the Block Protection (BP2, BP1, BP0) bits are set to 0's.

The default condition of the BP2-0 bits is binary 000 (all 0's).

Erase Error bit (E_ERR): The Erase Error Bit is used as a Erase operation success and failure check. When the Erase Error bit is set to a "1", it indicates that there was an error which occurred in the last erase operation. With the Erase Error bit set to a "1", this bit is reset with the Clear Status Register (CLSR) command.

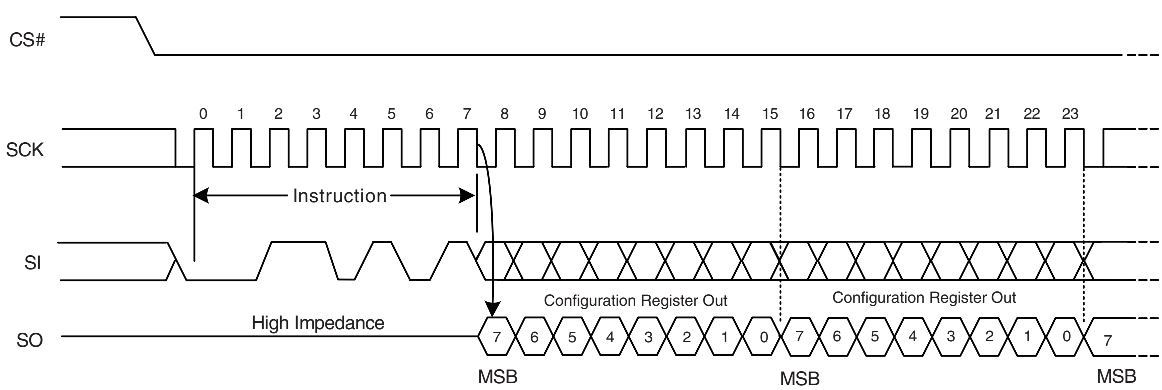
Program Error bit (P_ERR): The Program Error Bit is used as a Program operation success and failure check. When the Program Error bit is set to a "1", it indicates that there was an error which occurred in the last program operation. With the Program Error bit set to a "1", this bit is reset with the Clear Status Register (CLSR) command.

Status Register Write Disable (SRWD) bit: Provides data protection when used together with the Write Protect (W#/ACC) signal. The Status Register Write Disable (SRWD) bit is operated in conjunction with the Write Protect (W#/ACC) input pin. The Status Register Write Disable (SRWD) bit and the Write Protect (W#/ACC) signal allow the device to be put in the Hardware Protected mode. With the Status Register Write Disable (SRWD) bit set to a "1" and the W#/ACC driven to the logic low state, the device enters the Hardware Protected mode; the non-volatile bits of the Status Register (SRWD, BP2, BP1, BP0) and the nonvolatile bits of the Configuration Register (TBPARM, TBPROT, BPNV and QUAD) become read-only bits and the Write Registers (WRR) instruction opcode is no longer accepted for execution.

9.12 Read Configuration Register (RCR)

The Read Configuration Register (RCR) instruction opcode allows the Configuration Register contents to be read out of the SO serial output pin. The Configuration Register contents may be read at any time, even while a program, erase, or write cycle is in progress. When one of these cycles is in progress, it is recommended to the user to check the Write In Progress (WIP) bit of the Status Register before issuing a new instruction opcode to the device. The Configuration Register originally shows 00h when the device is first shipped from the factory to the customer.

Figure 9.14 Read Configuration Register (RCR) Instruction Sequence



9.13 Write Registers (WRR)

The Write Registers (WRR) command allows changing the bits in the Status and Configuration Registers. A Write Enable (WREN) command, which itself sets the Write Enable Latch (WEL) in the Status Register, is required prior to writing the WRR command. Table 9.8 shows the status register bits and their functions.

The host system must drive CS# low, then write the WRR command and the appropriate data byte on SI Figure 9.15.

The WRR command cannot change the state of the Write Enable Latch (bit 1). The WREN command must be used for that purpose.

The Status Register consists of one data byte in length; similarly, the Configuration Register is also one data byte in length. The CS# pin must be driven to the logic low state during the entire duration of the sequence.

The WRR command also controls the value of the Status Register Write Disable (SRWD) bit. The SRWD bit and W#/ACC pin together place the device in the Hardware Protected Mode (HPM). The device ignores all WRR commands once it enters the Hardware Protected Mode (HPM). Table 9.9 shows that W#/ACC must be driven low and the SRWD bit must be 1 for this to occur.

The Write Registers (WRR) instruction has no effect on the P/E Error and the WIP bits of the Status & Configuration Registers. Any bit reserved for the future is always read as a ‘0’

The CS# chip select input pin must be driven to the logic high state after the eighth (see Figure 9.15) or sixteenth (see Figure 9.16) bit of data has been latched in. If not, the Write Registers (WRR) instruction is not executed. If CS# is driven high after the eighth cycle then only the Status Register is written to; otherwise, after the sixteenth cycle both the Status and Configuration Registers are written to. As soon as the CS# chip select input pin is driven to the logic high state, the self-timed Write Registers cycle is initiated. While the Write Registers cycle is in progress, the Status Register may still be read to check the value of the Write In Progress (WIP) bit. The Write In Progress (WIP) bit is a ‘1’ during the self-timed Write Registers cycle, and is a ‘0’ when it is completed. When the Write Registers cycle is completed, the Write Enable Latch (WEL) is set to a ‘0’. The WRR command can operate at a maximum clock frequency of 104 MHz.

Figure 9.15 Write Registers (WRR) Instruction Sequence – 8 data bits

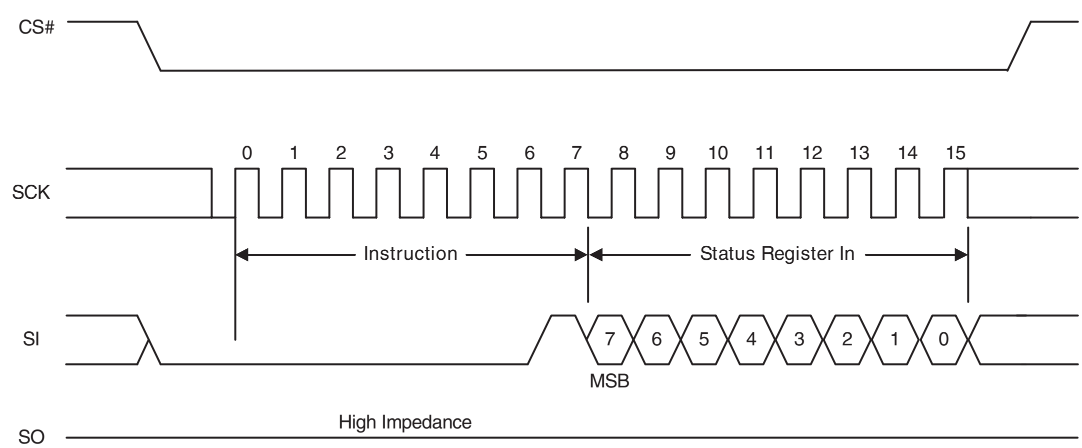


Figure 9.16 Write Registers (WRR) Instruction Sequence – 16 data bits

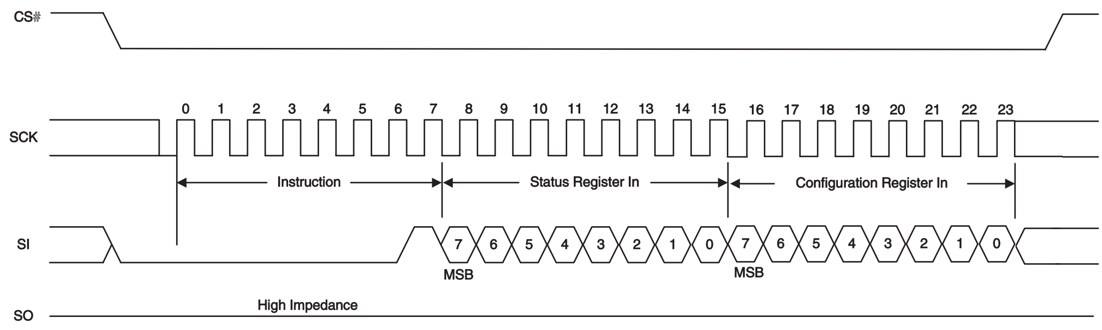


Table 9.9 Protection Modes

W#/ ACC	SRWD Bit	Mode	Write Protection of Registers	Memory Content	
				Protected Area	Unprotected Area
1	1	Software Protected (SPM)	Status & Configuration Registers are Writable (if WREN instruction has set the WEL bit). The values in the SRWD, BP2, BP1, & BP0 bits & those in the Configuration Register can be changed	Protected against Page Program, Quad Page Program, Parameter Sector Erase, Sector Erase, and Bulk Erase	Ready to accept Page Program, Quad Page Program, Parameter Sector Erase, & Sector Erase instructions
1	0				
0	0				
0	1	Hardware Protected (HPM)	Status & Configuration Registers are Hardware Write Protected. The values in the SRWD, BP2, BP1, & BP0 bits & those in the Configuration Register cannot be changed	Protected against Page Program, Quad Input Program, Sector Erase, and Bulk Erase	Ready to accept Page Program, Quad Input Program & Sector Erase instructions

Note
As defined by the values in the Block Protect (BP2, BP1, BP0) bits of the Status Register, as shown in *Table 7.2 on page 17**.*

Table 9.9 shows that neither W#/ACC or SRWD bit by themselves can enable HPM. The device can enter HPM either by setting the SRWD bit after driving W#/ACC low, or by driving W#/ACC low after setting the SRWD bit. However, the device disables HPM only when W#/ACC is driven high.

Note that HPM only protects against changes to the status register. Since BP2:BP0 cannot be changed in HPM, the size of the protected area of the memory array cannot be changed. Note that HPM provides no protection to the memory array area outside that specified by BP2:BP0 (Software Protected Mode, or SPM).

If W#/ACC is permanently tied high, HPM can never be activated, and only the SPM (BP2:BP0 bits of the Status Register) can be used.

The Status and Configuration registers originally default to 00h, when the device is first shipped from the factory to the customer.

9.14 Page Program (PP)

The Page Program (PP) command changes specified bytes in the memory array (from 1 to 0 only). A WREN command is required prior to writing the PP command.

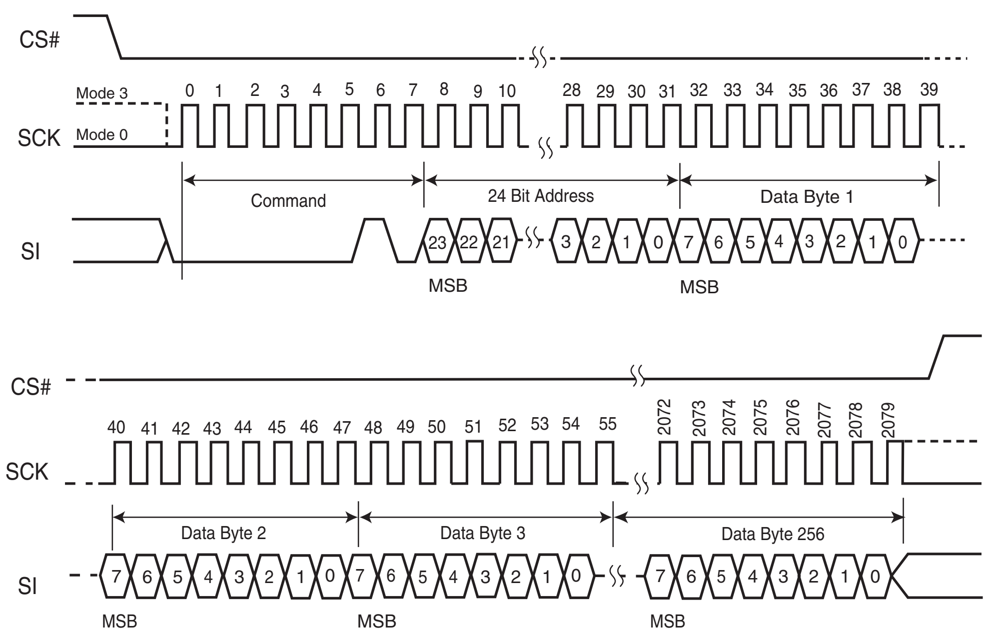
The host system must drive CS# low, and then write the PP command, three address bytes, and at least one data byte on SI. If the 8 least significant address bits (A7-A0) are not all zero, all transmitted data that goes beyond the end of the currently selected page are programmed from the starting address of the same page (from the address whose 8 least significant bits are all zero). CS# must be driven low for the entire duration of the PP sequence. The command sequence is shown in Figure 9.17 and Table 9.1 on page 22.

The device programs only the last 256 data bytes sent to the device. If the 8 least significant address bits (A7-A0) are not all zero, all transmitted data that goes beyond the end of the currently selected page are programmed from the starting address of the same page (from the address whose 8 least significant bits are all zero). If fewer than 256 data bytes are sent to device, they are correctly programmed at the requested addresses without having any effect on the other bytes in the same page.

The host system must drive CS# high after the device has latched the 8th bit of the data byte, otherwise the device does not execute the PP command. The PP operation begins as soon as CS# is driven high. The device internally controls the timing of the operation, which requires a period of t_{PP}. The Status Register may be read to check the value of the Write In Progress (WIP) bit while the PP operation is in progress. The WIP bit is 1 during the PP operation, and is 0 when the operation is completed. The device internally resets the Write Enable Latch to 0 before the operation completes (the exact timing is not specified).

The device does not execute a Page Program (PP) command that specifies a page that is protected by the Block Protect bits (BP2:BP0) (see Table 7.2 on page 17).

Figure 9.17 Page Program (PP) Command Sequence

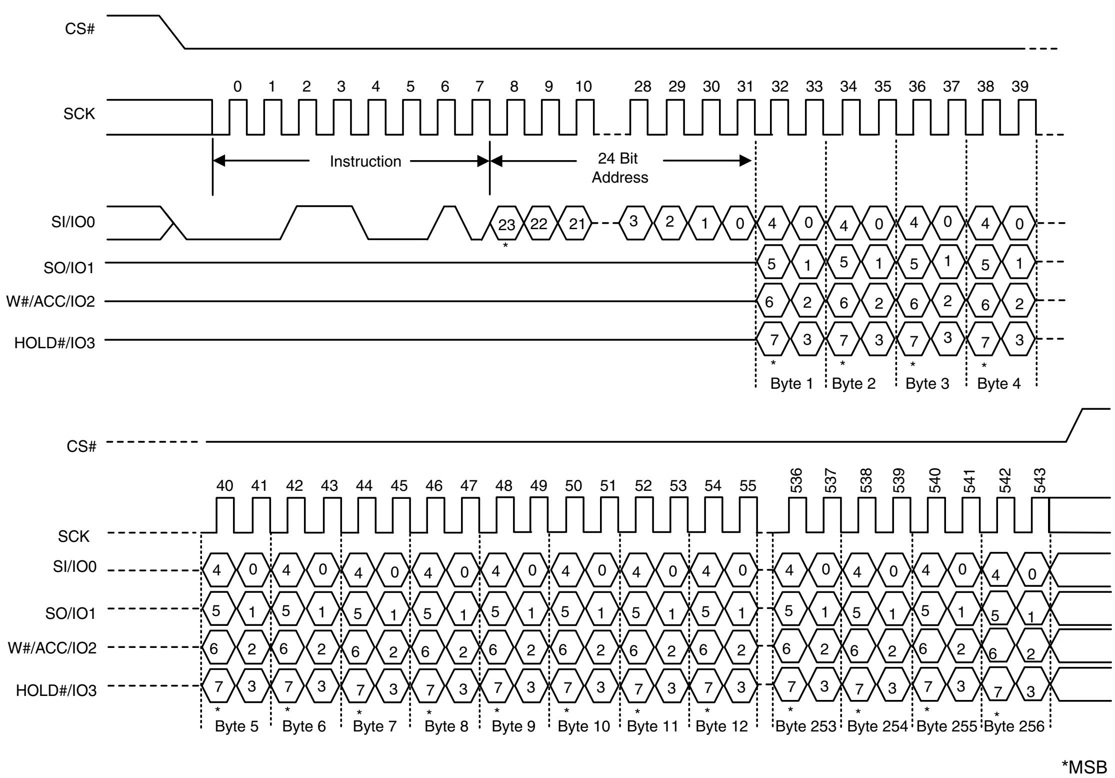


9.15 QUAD Page Program (QPP)

The Quad Page Program instruction is similar to the Page Program instruction, except that the Quad Page Program (QPP) instruction allows up to 256 bytes of data to be programmed at previously erased (FFh) memory locations using four pins: IO0 (SI), IO1 (SO), IO2 (W#/ACC), and IO3 (HOLD#), instead of just one pin (SI) as in the case of the Page Program (PP) instruction. This effectively increases the data transfer rate by up to four times, as compared to the Page Program (PP) instruction. The QPP feature can improve performance for PROM Programmer and applications that have slow clock speeds < 5 MHz. Systems with faster clock speed will not realize much benefit for the QPP instruction since the inherent page program time is much greater than the time it take to clock-in the data.

To use QPP, the Quad Enable Bit in the Configuration Register must be set (QUAD = 1). A Write Enable instruction must be executed before the device will accept the Quad Page Program instruction (Status Register-1, WEL = 1). The instruction is initiated by driving the CS# pin low then shifting the instruction code "32h" followed by a 24 bit address (A23-A0) and at least one data byte, into the IO pins. The CS# pin must be held low for the entire length of the instruction while data is being sent to the device. All other functions of Quad Input Page Program are identical to standard Page Program. The QPP instruction sequence is shown below.

Figure 9.18 QUAD Page Program Instruction Sequence



9.16 Parameter Sector Erase (P4E, P8E)

The Parameter Sector Erase (P4E, P8E) command sets all bits at all addresses within a specified sector to a logic 1 (FFh). A WREN command is required prior to writing the Parameter Sector Erase commands.

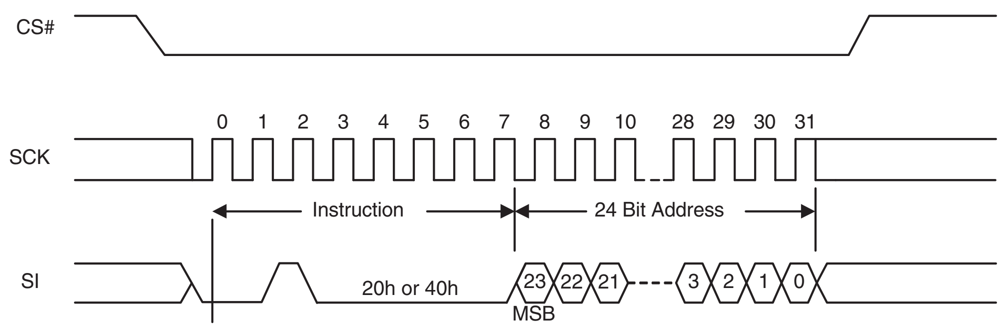
The host system must drive CS# low, and then write the P4E or P8E command, plus three address bytes on SI. Any address within the sector (see Table 5.1 on page 12) is a valid address for the P4E or P8E command. CS# must be driven low for the entire duration of the P4E/P8E sequence. The command sequence is shown in Figure 9.19 and Table 9.1 on page 22.

The host system must drive CS# high after the device has latched the 8th bit of the P4E/P8E command, otherwise the device does not execute the command. The parameter sector erase operation begins as soon as CS# is driven high. The device internally controls the timing of the operation, which requires a period of t_{SE}. The Status Register may be read to check the value of the Write In Progress (WIP) bit while the parameter sector erase operation is in progress. The WIP bit is 1 during the P4E/P8E operation, and is 0 when the operation is completed. The device internally resets the Write Enable Latch to 0 before the operation completes (the exact timing is not specified).

A Parameter Sector Erase (P4E, P8E) instruction applied to a sector that has been Write Protected through the Block Protect Bits will not be executed.

The Parameter Sector Erase Command (P8E) erases two of the 4 KB Sectors in selected address space. The Parameter Sector Erase Command (P8E) erases two sequential 4 KB Parameter Sectors in the selected address space. The address LSB is disregarded so that two sequential 4 KB Parameter Sectors are erased. The 24 Bit Address is any location within the first Sector to be erased (n), and the next sequential 4 KB Parameter Sector will also be erased (n+1). The 4 KB parameter Sector will only be erased properly if n or n+1 is a valid 4 KB parameter Sector. i.e. If n is not a valid 4K parameter Sector, then it will not be erased. If n+1 is not a valid 4 KB parameter Sector, then it will not be erased.

Figure 9.19 Parameter Sector Erase (P4E, P8E) Instruction Sequence



9.17 Sector Erase (SE)

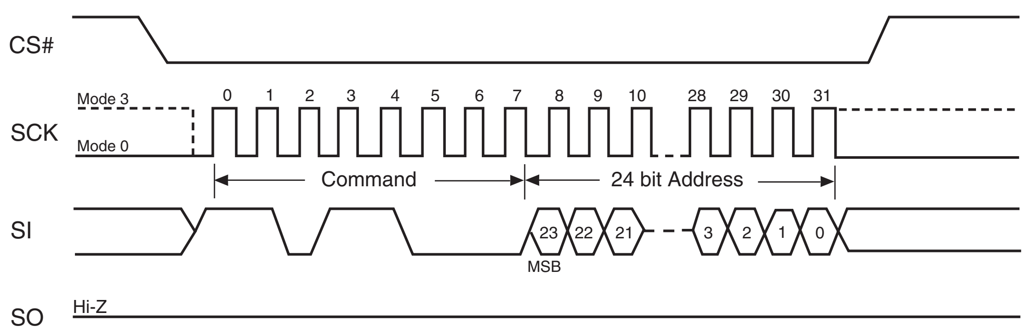
The Sector Erase (SE) command sets all bits at all addresses within a specified sector to a logic 1. A WREN command is required prior to writing the SE command.

The host system must drive CS# low, and then write the SE command plus three address bytes on SI. Any address within the sector (see Table 7.2 on page 17) is a valid address for the SE command. CS# must be driven low for the entire duration of the SE sequence. The command sequence is shown in Figure 9.20 and Table 9.1 on page 22.

The host system must drive CS# high after the device has latched the 8th bit of the SE command, otherwise the device does not execute the command. The SE operation begins as soon as CS# is driven high. The device internally controls the timing of the operation, which requires a period of t_{SE}. The Status Register may be read to check the value of the Write In Progress (WIP) bit while the SE operation is in progress. The WIP bit is 1 during the SE operation, and is 0 when the operation is completed. The device internally resets the Write Enable Latch to 0 before the operation completes (the exact timing is not specified).

The device only executes a SE command if all Block Protect bits (BP2:BP0) are 0 (see Table 7.2 on page 17). Otherwise, the device ignores the command.

Figure 9.20 Sector Erase (SE) Command Sequence



9.18 Bulk Erase (BE)

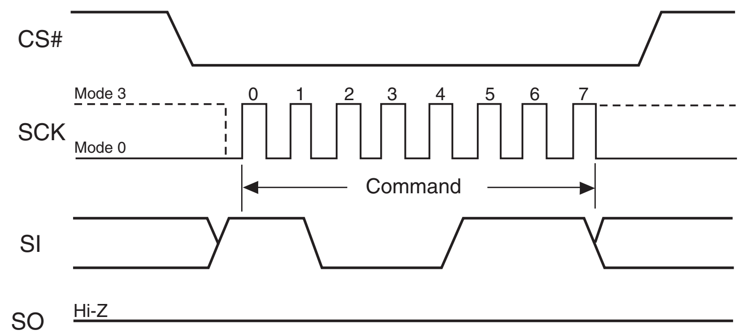
The Bulk Erase (BE) command sets all the bits within the entire memory array to logic 1s. A WREN command is required prior to writing the BE command.

The host system must drive CS# low, and then write the BE command on SI. CS# must be driven low for the entire duration of the BE sequence. The command sequence is shown in Figure 9.21 and Table 9.1 on page 22.

The host system must drive CS# high after the device has latched the 8th bit of the CE command, otherwise the device does not execute the command. The BE operation begins as soon as CS# is driven high. The device internally controls the timing of the operation, which requires a period of t_{BE}. The Status Register may be read to check the value of the Write In Progress (WIP) bit while the BE operation is in progress. The WIP bit is 1 during the BE operation, and is 0 when the operation is completed. The device internally resets the Write Enable Latch to 0 before the operation completes (the exact timing is not specified).

The device only executes a BE command if all Block Protect bits (BP2:BP0) are 0 (see Table 7.2 on page 17). Otherwise, the device ignores the command.

Figure 9.21 Bulk Erase (BE) Command Sequence



9.19 Deep Power-Down (DP)

The Deep Power-Down (DP) command provides the lowest power consumption mode of the device. It is intended for periods when the device is not in active use, and ignores all commands except for the Release from Deep Power-Down (RES) command. *The DP mode therefore provides the maximum data protection against unintended write operations.* The standard standby mode, which the device goes into automatically when CS# is high (and all operations in progress are complete), should generally be used for the lowest power consumption when the quickest return to device activity is required.

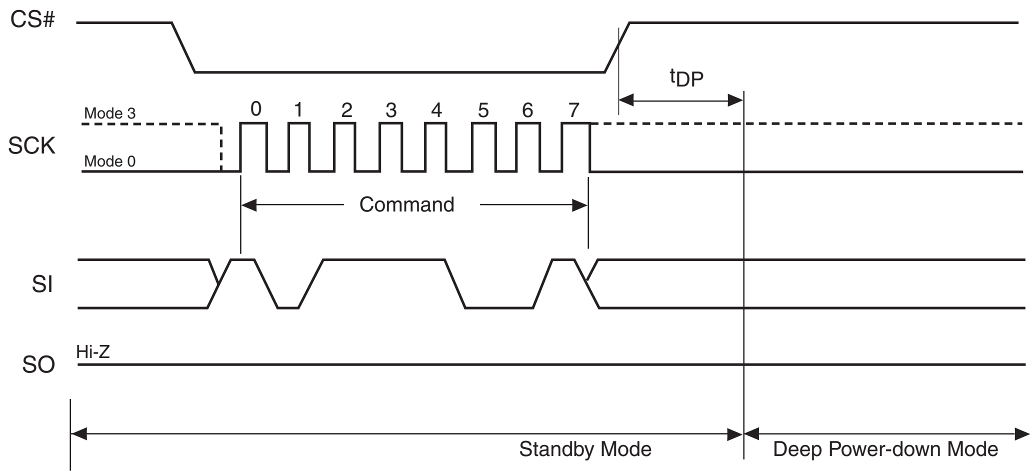
The host system must drive CS# low, and then write the DP command on SI. CS# must be driven low for the entire duration of the DP sequence. The command sequence is shown in Figure 9.22 and Table 9.1 on page 22.

The host system must drive CS# high after the device has latched the 8th bit of the DP command, otherwise the device does not execute the command. After a delay of t_{DP}, the device enters the DP mode and current reduces from I_{SB} to I_{DP} (see Table 16.1 on page 55).

Once the device has entered the DP mode, all commands are ignored except the RES command (which releases the device from the DP mode). The RES command also provides the Electronic Signature of the device to be output on SO, if desired (see Section 9.20 and 9.20.1).

DP mode automatically terminates when power is removed, and the device always powers up in the standard standby mode. The device rejects any DP command issued while it is executing a program, erase, or Write Registers operation, and continues the operation uninterrupted.

Figure 9.22 Deep Power-Down (DP) Command Sequence



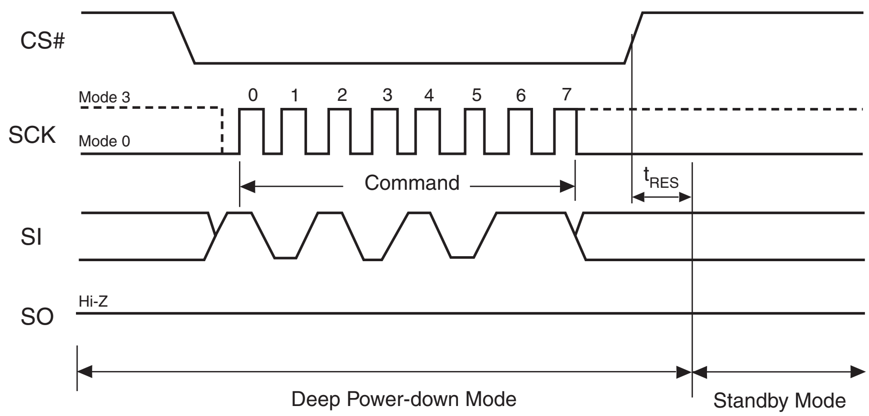
9.20 Release from Deep Power-Down (RES)

The device requires the Release from Deep Power-Down (RES) command to exit the Deep Power-Down mode. When the device is in the Deep Power-Down mode, all commands except RES are ignored.

The host system must drive CS# low and write the RES command to SI. CS# must be driven low for the entire duration of the sequence. The command sequence is shown in Figure 9.23 and Table 9.1 on page 22.

The host system must drive CS# high $t_{RES(max)}$ after the 8-bit RES command byte. The device transitions from DP mode to the standby mode after a delay of t_{RES} (see Figure 18.1). In the standby mode, the device can execute any read or write command.

Figure 9.23 Release from Deep Power-Down (RES) Command Sequence



9.20.1 Release from Deep Power-Down and Read Electronic Signature (RES)

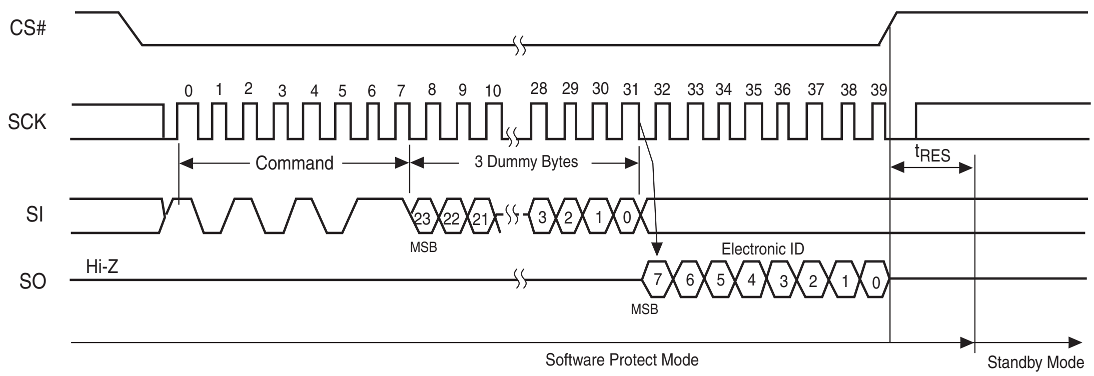
The device features an 8-bit Electronic Signature, which can be read using the RES command. See Figure 9.24 and Table 9.1 on page 22 for the command sequence and signature value. The Electronic Signature is not to be confused with the identification data obtained using the RDID command. The device offers the Electronic Signature so that it can be used with previous devices that offered it; however, the Electronic Signature should not be used for new designs, which should read the RDID data instead.

After the host system drives CS# low, it must write the RES command followed by 3 dummy bytes to SI (each bit is latched on SI during the rising edge of SCK). The Electronic Signature is then output on SO; each bit is shifted out on the falling edge of SCK. The RES operation is terminated by driving CS# high after the Electronic Signature is read at least once. Additional clock cycles on SCK with CS# low cause the device to output the Electronic Signature repeatedly.

When CS# is driven high, the device transitions from DP mode to the standby mode after a delay of t_{RES}, as previously described. The RES command always provides access to the Electronic Signature of the device and can be applied even if DP mode has not been entered.

Any RES command issued while an erase, program, or Write Registers operation is in progress not executed, and the operation continues uninterrupted.

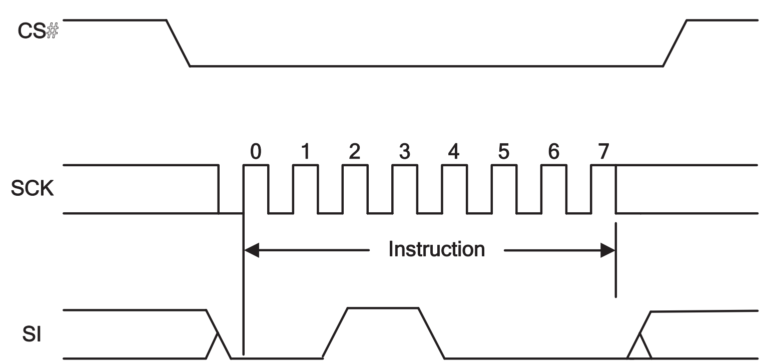
Figure 9.24 Release from Deep Power-Down and RES Command Sequence



9.21 Clear Status Register (CLSR)

The Clear Status Register command resets bit SR5 (Erase Fail Flag) and bit SR6 (Program Fail Flag). It is not necessary to set the WEL bit before the Clear SR Fail Flags command is executed. The WEL bit will be unchanged after this command is executed. This command also resets the State machine and loads latches

Figure 9.25 Clear Status Register (CLSR) Instruction Sequence



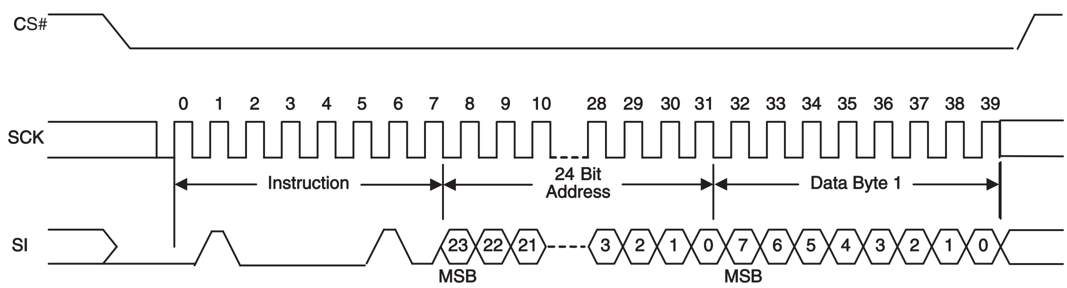
9.22 OTP Program (OTPP)

The OTP Program command programs data in the OTP region, which is in a different address space from the main array data. Refer to, "*OTP Regions*"for details on the OTP region. The protocol of the OTP Program command is the same as the Page Program command, except that the OTP Program command requires exactly one byte of data; otherwise, the command will be ignored. To program the OTP in bit granularity, the rest of the bits within the data byte can be set to "1".

The OTP memory space can be programmed one or more times, provided that the OTP memory space is not locked (as described in "Locking OTP Regions"). Subsequent OTP programming can be performed only on the unprogrammed bits (that is, "1" data).

Note: The Write Enable (WREN) command must precede the OTPP command before programming of the OTP can occur.

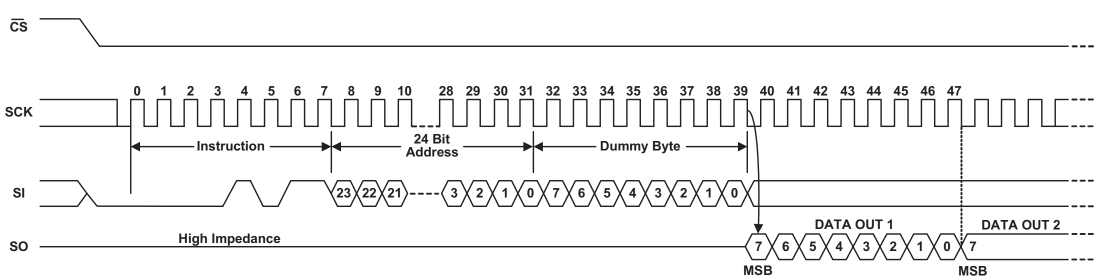
Figure 9.26 OTP Program Instruction Sequence



9.23 Read OTP Data Bytes (OTPR)

The Read OTP Data Bytes command reads data from the OTP region. Refer to "*OTP Regions*" for details on the OTP region. The protocol of the Read OTP Data Bytes command is the same as the Fast Read Data Bytes command except that it will not wrap to the starting address after the OTP address is at its maximum; instead, the data will be indeterminate.

Figure 9.27 Read OTP Instruction Sequence



10. OTP Regions

The OTP Regions are separately addressable from the main array and consists of two 8-byte (ESN), thirty 16-byte, and one 10-byte regions that can be individually locked.

- The two 8-byte regions enable permanent part identification through an Electronic Serial Number (ESN). The customer can utilize the ESN to pair a Flash device with the system CPU/ASIC to prevent system cloning. The Spansion factory programs and locks the lower 8-byte ESN with a 64-bit randomly generated, unique number. The upper 8-byte ESN is left blank for customer use or, if special ordered, Spansion can program (and lock) in a unique customer ID.
- The thirty 16-byte and one 10-byte OTP regions are open for the customer usage.
- The thirty 16-byte, one 10-byte, and upper 8-byte ESN OTP regions can be individually locked by the end user. Once locked, the data cannot changed. The locking process is permanent and cannot be undone.

The following general conditions should be noted with respect to the OTP Regions:

- On power-up, or following a hardware reset, the device reverts to sending commands to the normal address space.
- Reads outside of the OTP Regions will be ignored
- The OTP Region is not accessible when the device is executing an Embedded Program or Embedded Erase algorithm.
- The ACC function is not available when the Secured Silicon Sector is enabled.
- The two 8-byte ESN region is a special order part (please contact your local Spansion sales representative for further details); otherwise, these regions are programmed to all zeroes and locked prior to shipping from the Spansion factory. The thirty 16-byte and one 10-byte OTP regions are left open for customer usage, but special care of the OTP locking must be maintained, or else a malevolent user can permanently lock the OTP regions. This is not a concern, if the OTP regions are not used.

10.1 Programming OTP Address Space

The protocol of the OTP Program command (42h) is the same as the Page Program command. Refer to Table 9.1 for the command description and protocol. The OTP Program command can be issued multiple times to any given OTP address, but this address space can never be erased. After a given OTP region is programmed, it can be locked to prevent further programming with the OTP lock bits (refer to Section 10.3). The valid address range for OTP Program is depicted in the figure below. OTP Program operations outside the valid OTP address range will be ignored.

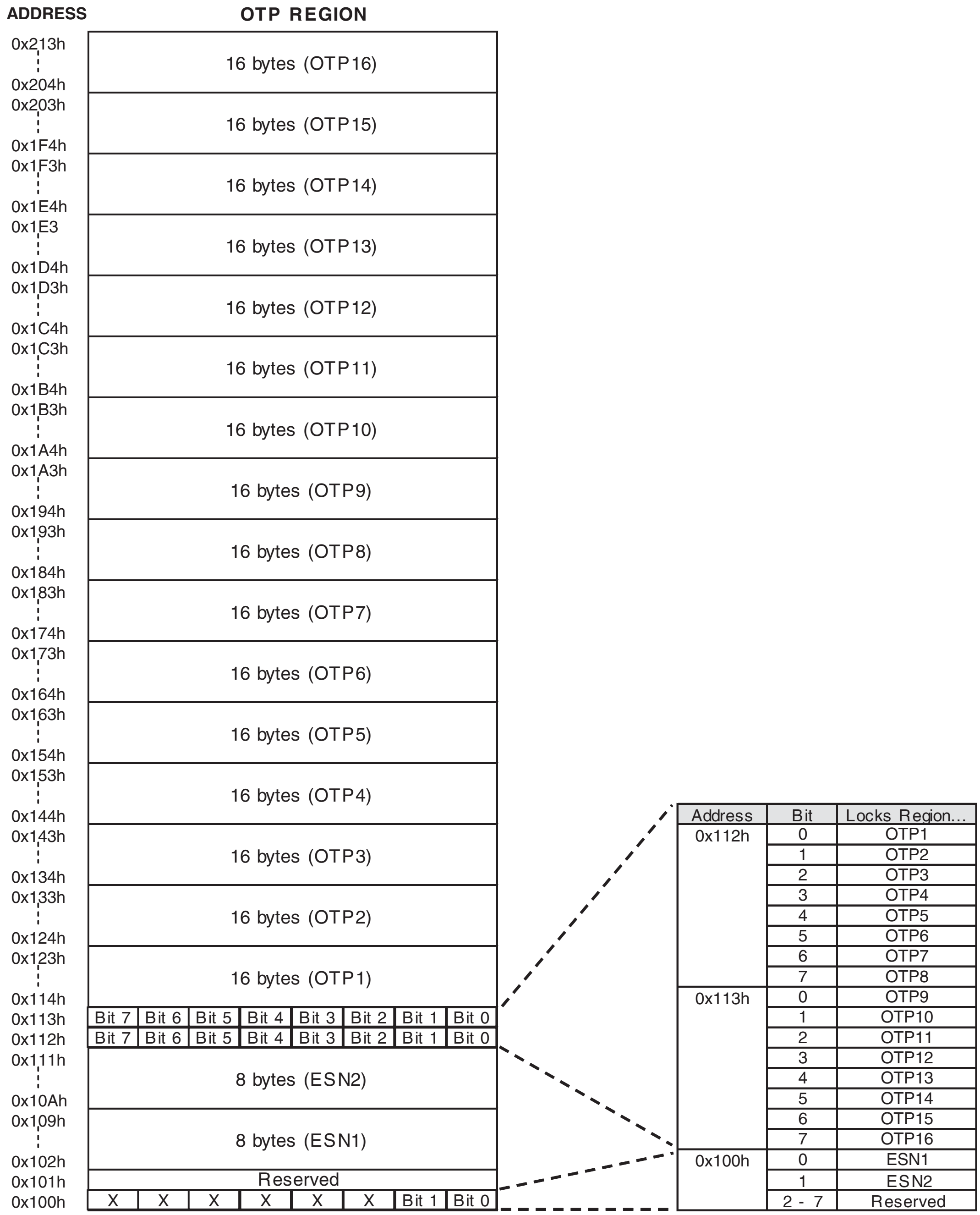
10.2 Reading OTP Data

The protocol of the OTP Read command (4Bh) is the same as that of the Fast Read command. Refer to Table 9.1 for the command description and protocol. The valid address range for OTP Reads is depicted in the figure below. OTP Read operations outside the valid OTP address range will yield indeterminate data.

10.3 Locking OTP Regions

In order to permanently lock the ESN and OTP regions, individual bits at the specified addresses can be set to lock specific regions of OTP memory, as highlighted in Figures 10.1 and 10.2.

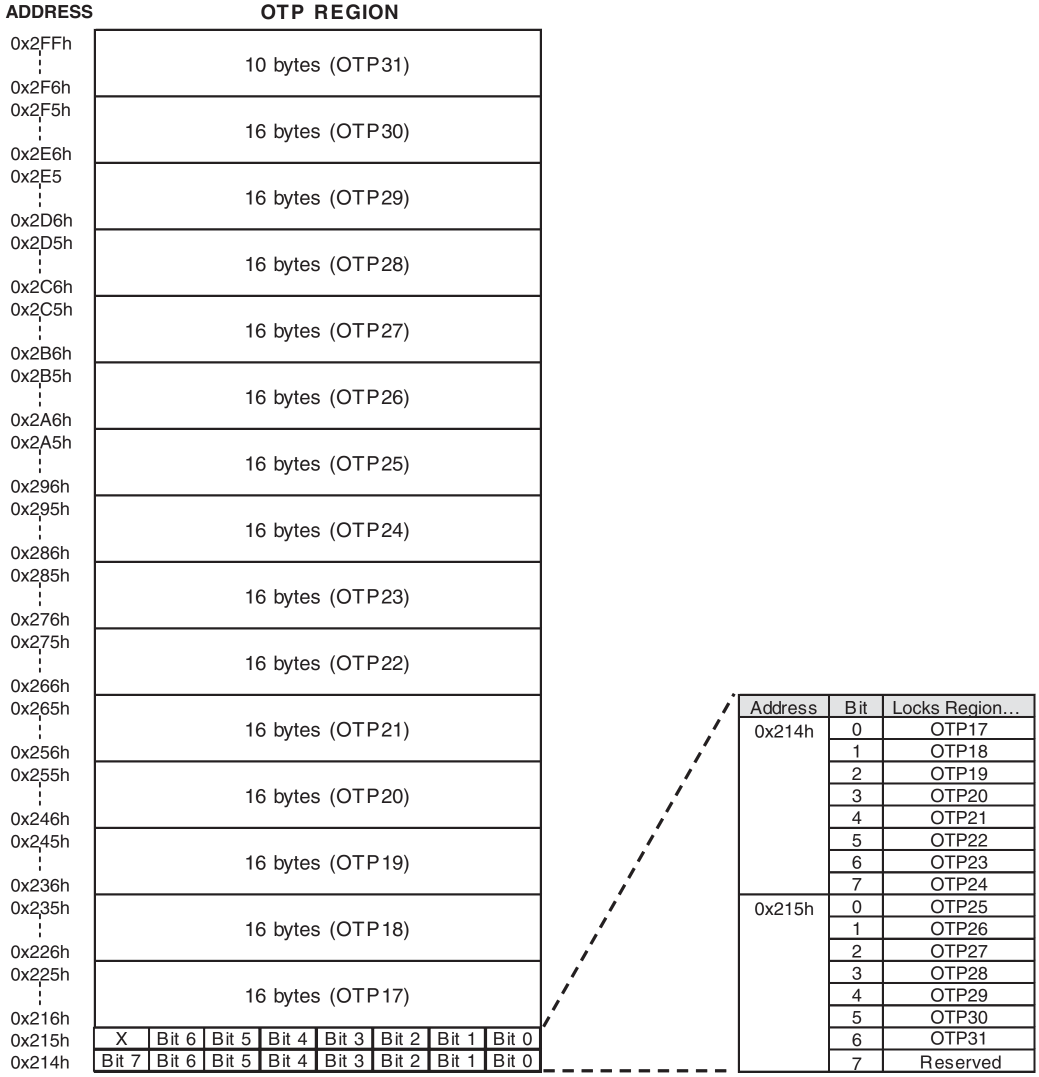
Figure 10.1 OTP Memory Map - Part 1



Notes

1. *Bit 0 at address 0x100h locks ESN1 region.*
2. *Bit 1 at address 0x100h locks ESN1 region.*
3. *Bits 2-7 (“X”) are NOT programmable and will be ignored.*

Figure 10.2 OTP Memory Map - Part 2



Note

1. Bit 7 (“X”) at address 0x215h is NOT programmable and will be ignored.

11. Power-up and Power-down

During power-up and power-down, certain conditions must be observed. CS# must follow the voltage applied on V_{CC}, and must not be driven low to select the device until V_{CC} reaches the allowable values as follows (see Figure 11.1 and Table 11.1 on page 53):

- At power-up, V_{CC} (min.) plus a period of t_{PU}
- At power-down, V_{SS}

A pull-up resistor on Chip Select (CS#) typically meets proper power-up and power-down requirements.

No Write Registers, program, or erase command should be sent to the device until V_{CC} rises to the V_{CC} min., plus a delay of t_{PU}. At power-up, the device is in standby mode (not Deep Power-Down mode) and the WEL bit is reset (0).

Each device in the host system should have the V_{CC} rail decoupled by a suitable capacitor close to the package pins (this capacitor is generally of the order of 0.1 µF), as a precaution to stabilizing the V_{CC} feed.

When V_{CC} drops from the operating voltage to below the minimum V_{CC} threshold at power-down, all operations are disabled and the device does not respond to any commands. Note that data corruption may result if a power-down occurs while a Write Registers, program, or erase operation is in progress.

Figure 11.1 Power-Up Timing Diagram

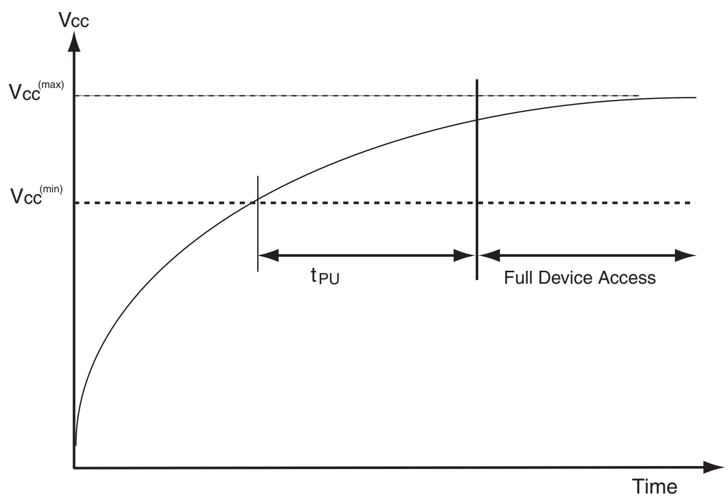


Figure 11.2 Power-down and Voltage Drop

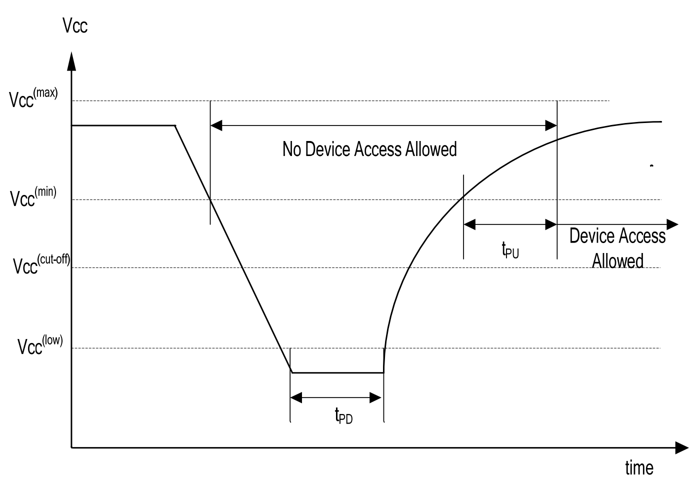


Table 11.1 Power-Up / Power-Down Voltage and Timing

Symbol	Parameter	Min	Max	Unit
$V_{CC(min)}$	V_{CC} (minimum operation voltage)	2.7		V
V_{CC}(cut-off)	V_{CC} (Cut off where re-initialization is needed)	2.4		V
V_{CC}(low)	V_{CC} (Low voltage for initialization to occur at read/standby) V_{CC} (Low voltage for initialization to occur at embedded)	1.0 2.3		V
t_{PU}	V_{CC}(min.) to device operation	300		µs
T_{PD}	V_{CC} (low duration time)	1.0		µs

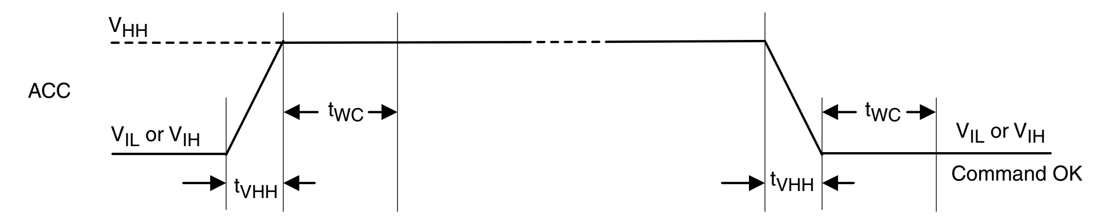
12. Initial Delivery State

The device is delivered with the memory array erased i.e. all bits are set to 1 (FFh) upon initial factory shipment. The Status Register and Configuration Register contains 00h (all bits are set to 0).

13. Program Acceleration via W#/ACC Pin

The program acceleration function requires applying V_{HH} to the W#/ACC input, and then waiting a period of t_{WC}. Minimum V_{HH} rise and fall times is required for W#/ACC to change to V_{HH} from V_{IL} or V_{IH}. Removing V_{HH} from the W#/ACC pin returns the device to normal operation after a period of t_{WC}.

Figure 13.1 ACC Program Acceleration Timing Requirements



Note
Only Read Status Register (RDSR) and Page Program (PP) operation are allow when ACC is at (V_{HH}).
The W#/ACC pin is disabled during Quad I/O mode.

Table 13.1 ACC Program Acceleration Specifications

Symbol	Parameter	Min.	Max	Unit
V_{HH}	A_{CC} Pin Voltage High	8.5	9.5	V
t_{VHH}	A_{CC} Voltage Rise and Fall time	2.2		ns
t_{WC}	ACC at V_{HH} and V_{IL} or V_{IH} to First command	5		ns

14. Electrical Specifications

14.1 Absolute Maximum Ratings

Description	Rating
Ambient Storage Temperature	-65°C to +150°C
Voltage with Respect to Ground: All Inputs and I/Os	-0.5V to V_{CC}+0.5V
Output Short Circuit Current (Note 2)	200 mA

Note

1. *Minimum DC voltage on input or I/Os is -0.5V. During voltage transitions, inputs or I/Os may undershoot V_{SS} to -2.0V for periods of up to 20 ns. See Figure 14.1. Maximum DC voltage on input or I/Os is V_{CC} + 0.5V. During voltage transitions inputs or I/Os may overshoot to V_{CC} + 2.0V for periods up to 20 ns. See Figure 14.2.*
2. *No more than one output may be shorted to ground at a time. Duration of the short circuit should not be greater than one second.*
3. *Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational sections of this data sheet is not implied. Exposure of the device to absolute maximum rating conditions for extended periods may affect device reliability.*

Figure 14.1 Maximum Negative Overshoot Waveform

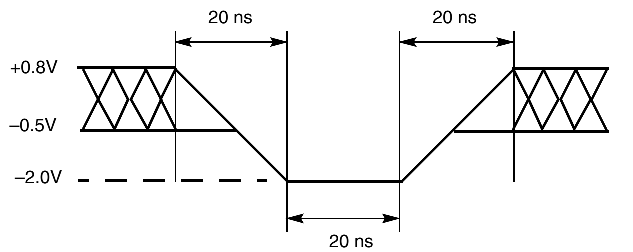
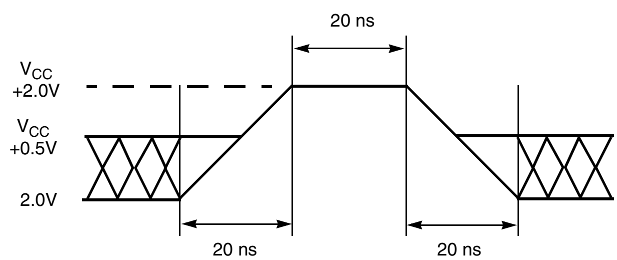


Figure 14.2 Maximum Positive Overshoot Waveform



15. Operating Ranges

Table 15.1 Operating Ranges

Description		Rating
Ambient Operating Temperature (T_A)	Industrial	–40°C to +85°C
Positive Power Supply	Voltage Range	2.7V to 3.6V

Note

Operating ranges define those limits between which functionality of the device is guaranteed.

16. DC Characteristics

This section summarizes the DC Characteristics of the device. Designers should check that the operating conditions in their circuit match the measurement conditions specified in the Test Specifications in Table 17.1 on page 56, when relying on the quoted parameters.

Table 16.1 DC Characteristics (CMOS Compatible)

Symbol	Parameter	Test Conditions	Limits			Unit
			Min.	Typ*	Max	
V_{CC}	Supply Voltage		2.7		3.6	V
V_{HH}	ACC Program Acceleration Voltage	V_{CC} = 2.7V to 3.6V	8.5		9.5	V
V_{IL}	Input Low Voltage**		-0.3		0.3 x V_{CC}	V
V_{IH}	Input High Voltage**		0.7 x V_{CC}		V_{CC} +0.5	V
V_{OL}	Output Low Voltage	I_{OL} = 1.6 mA, V_{CC} = V_{CC} min.			0.4	V
V_{OH}	Output High Voltage	I_{OH} = -0.1 mA	V_{CC}-0.6			V
I_{LI}	Input Leakage Current	V_{CC} = V_{CC} Max, V_{IN} = V_{CC} or GND			±2	µA
I_{LO}	Output Leakage Current	V_{CC} = V_{CC} Max, V_{IN} = V_{CC} or GND			±2	µA
I_{CC1}	Active Power Supply Current - READ (SO = Open)	At 80 MHz (Dual or Quad)			38	mA
		At 104 MHz (Serial)			25	
		At 40 MHz (Serial)			12	
I_{CC2}	Active Power Supply Current (Page Program)	CS# = V_{CC}			26	mA
I_{CC3}	Active Power Supply Current (WRR)	CS# = V_{CC}			15	mA
I_{CC4}	Active Power Supply Current (SE)	CS# = V_{CC}			26	mA
I_{CC5}	Active Power Supply Current (BE)	CS# = V_{CC}			26	mA
I_{SB1}	Standby Current	CS# = V_{CC}; SO + V_{IN} = GND or V_{CC}		80	200	µA
I_{PD}	Deep Power-down Current	CS# = V_{CC}; SO + V_{IN} = GND or V_{CC}		3	10	µA
*Typical values are at T_{AI} = 25°C and V_{CC} = 3V						

Note

Typical values are at T_A = 25°C and 3.0V.

17. Test Conditions

Figure 17.1 AC Measurements I/O Waveform

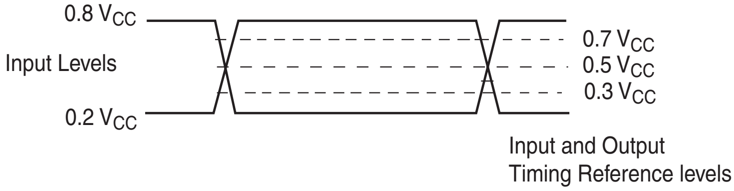


Table 17.1 Test Specifications

Symbol	Parameter	Min	Max	Unit
C_L	Load Capacitance	30		pF
	Input Rise and Fall Times		5	ns
	Input Pulse Voltage	0.2 V_{CC} to 0.8 V_{CC}		V
	Input Timing Reference Voltage	0.3 V_{CC} to 0.7 V_{CC}		V
	Output Timing Reference Voltage	0.5 V_{CC}		V

18. AC Characteristics

Figure 18.1 AC Characteristics (Sheet 1 of 2)

Symbol (Notes)	Parameter (Notes)	Min. (Notes)	Typ (Notes)	Max (Notes)	Unit
FSCK, R	SCK Clock Frequency for READ command	DC		40	MHz
FSCK, C	SCK Clock Frequency for all others: FAST_READ(3)*, PP, QPP, P4E, P8E, SE, BE, DP, RES, WREN, WRDI, RDSR, WRR, RDID, READ_ID	DC		104 (serial) 80 (dual/quad)	MHz
t_{WH}, t_{CH}	Clock High Time (40 MHz) Clock High Time (80 MHz) Clock High Time (104 MHz)	12.0 6.0 4.6			ns
t_{WL}, t_{CL}	Clock Low Time (40 MHz) Clock Low Time (80 MHz) Clock Low Time (104 MHz)	12.0 6.0 4.6			ns
t_{CRT}, t_{CLCH}	Clock Rise Time (slew rate)	0.1			V/ns
t_{CFT}, t_{CHCL}	Clock Fall Time (slew rate)	0.1			V/ns
t_{CS}	CS# High Time (Read Instructions) CS# High Time (Program/Erase)	10 50			ns
t_{CSS}	CS# Active Setup Time (relative to SCK)	3			ns
t_{CSH}	CS# Active Hold Time (relative to SCK)	3			ns
$t_{SU:DAT}$	Data in Setup Time	3			ns
$t_{HD:DAT}$	Data in Hold Time	2			ns
t_V	Clock Low to Output Valid	0		8 (Serial)Δ 9.5 (Dual/Quad)Δ 6.5 (Serial)∞ 8 (Dual/Quad)∞ 7 (Dual/Quad)Ω	ns
t_{HO}	Output Hold Time	0			ns
t_{DIS}	Output Disable Time			8	ns
t_{HLCH}	HOLD# Active Setup Time (relative to SCK)	3			ns

Figure 18.1 AC Characteristics (Sheet 2 of 2)

Symbol (Notes)	Parameter (Notes)	Min. (Notes)	Typ (Notes)	Max (Notes)	Unit
t_{CHHH}	HOLD# Active Hold Time (relative to SCK)	3			ns
t_{HHCH}	HOLD# Non Active Setup Time (relative to SCK)	3			ns
t_{CHHL}	HOLD# Non Active Hold Time (relative to SCK)	3			ns
t_{HZ}	HOLD# enable to Output Invalid			8	ns
t_{LZ}	HOLD# disable to Output Valid			8	ns
t_{WPS}	W#/ACC Setup Time (4)	20			ns
t_{WPH}	W#/ACC Hold Time (4)	100			ns
t_W	WRR Cycle Time			50	ms
t_{PP}	Page Programming (1)(2)		1.5	3	ms
t_{EP}	Page Programming (ACC = 9V) (1)(2)(3)		1.2	2.4	ms
t_{SE}	Sector Erase Time (64 KB) (1)(2)		0.5	2	sec
t_{PE}	Parameter Sector Erase Time (1)(2) (4 KB or 8 KB)		200	800	ms
t_{BE}	Bulk Erase Time (1)(2)		32	64	sec
t_{RES}	Deep Power-down to Standby Mode			30	us
t_{DP}	Time to enter Deep Power-down Mode			10	us
t_{VHH}	ACC Voltage Rise and Fall time	2.2			us
t_{WC}	ACC at VHH and VIL or VIH to first command	5			us

Notes

1. *Typical program and erase times assume the following conditions: 25°C, VCC = 3.0V; 10,000 cycles; checkerboard data pattern.*
2. *Under worst-case conditions of 85°C; V_{CC} = 2.7V; 100,000 cycles.*
3. *Acceleration mode (9V ACC) only in Program mode, not Erase.*
4. *Only applicable as a constraint for WRR instruction when SRWD is set to a '1'.*

∆ Full Vcc range (2.7 – 3.6V) & CL = 30 pF
∞ Regulated Vcc range (3.0 – 3.6V) & CL = 30 pF
Ω Regulated Vcc range (3.0 – 3.6V) & CL = 15 pF

18.1 Capacitance

Symbol	Parameter	Test Conditions	Min	Max	Unit
C_{IN}	Input Capacitance (applies to SCK, PO7-PO0, SI, CS#)	V_{OUT} = 0V		6	pF
C_{OUT}	Output Capacitance (applies to PO7-PO0, SO)	V_{IN} = 0V		8	pF

Figure 18.2 SPI Mode 0 (0,0) Input Timing

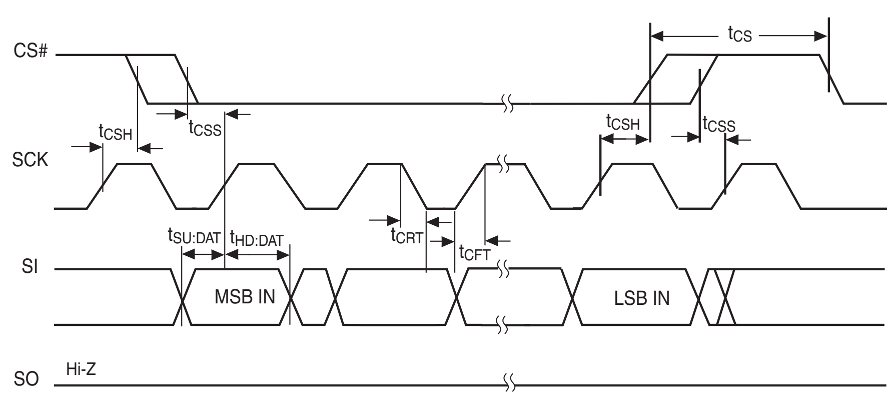


Figure 18.3 SPI Mode 0 (0,0) Output Timing

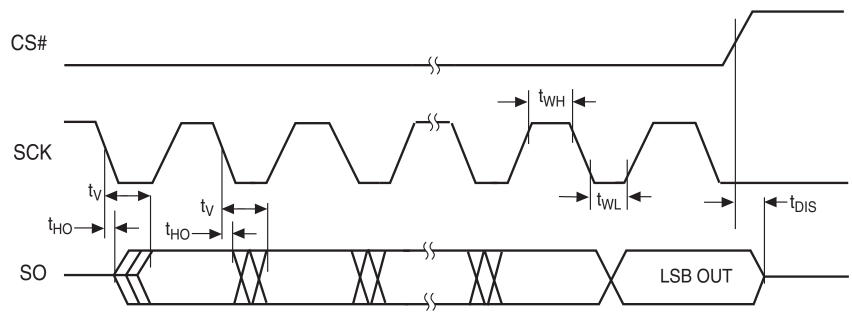


Figure 18.4 HOLD# Timing

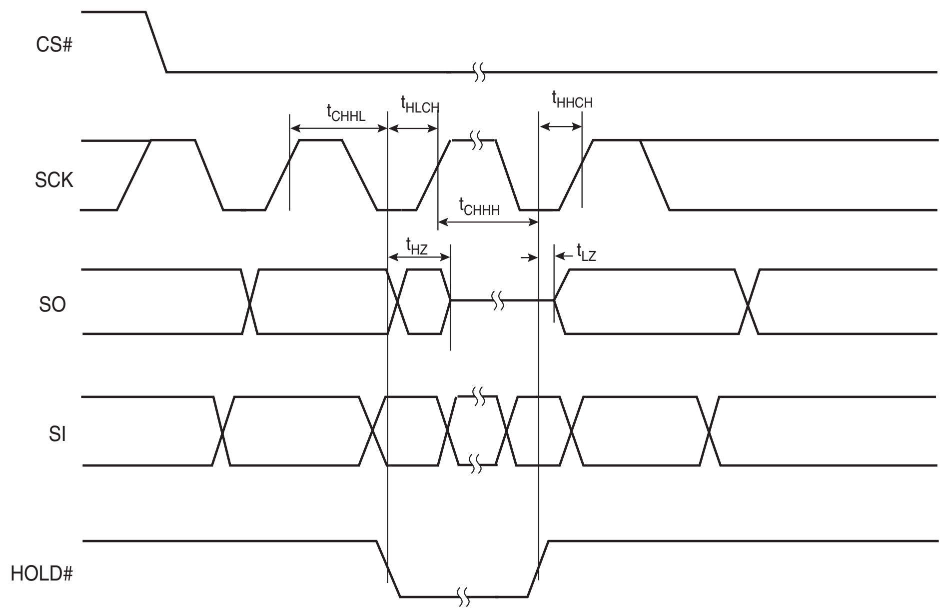
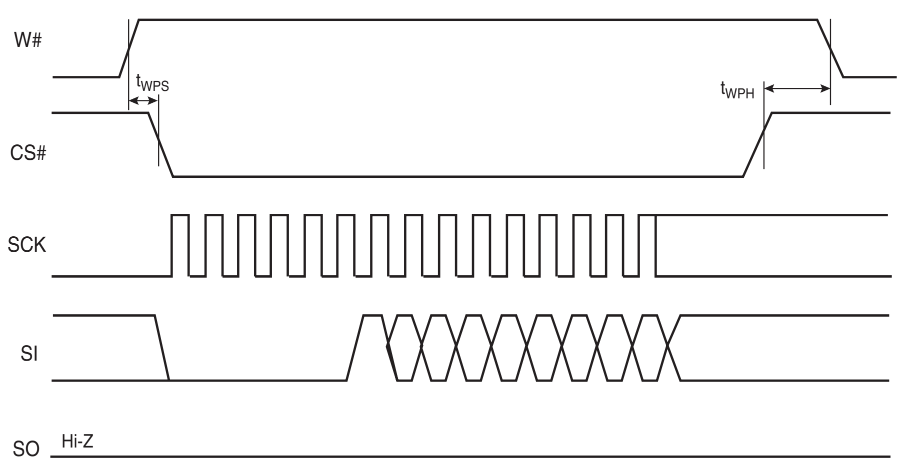
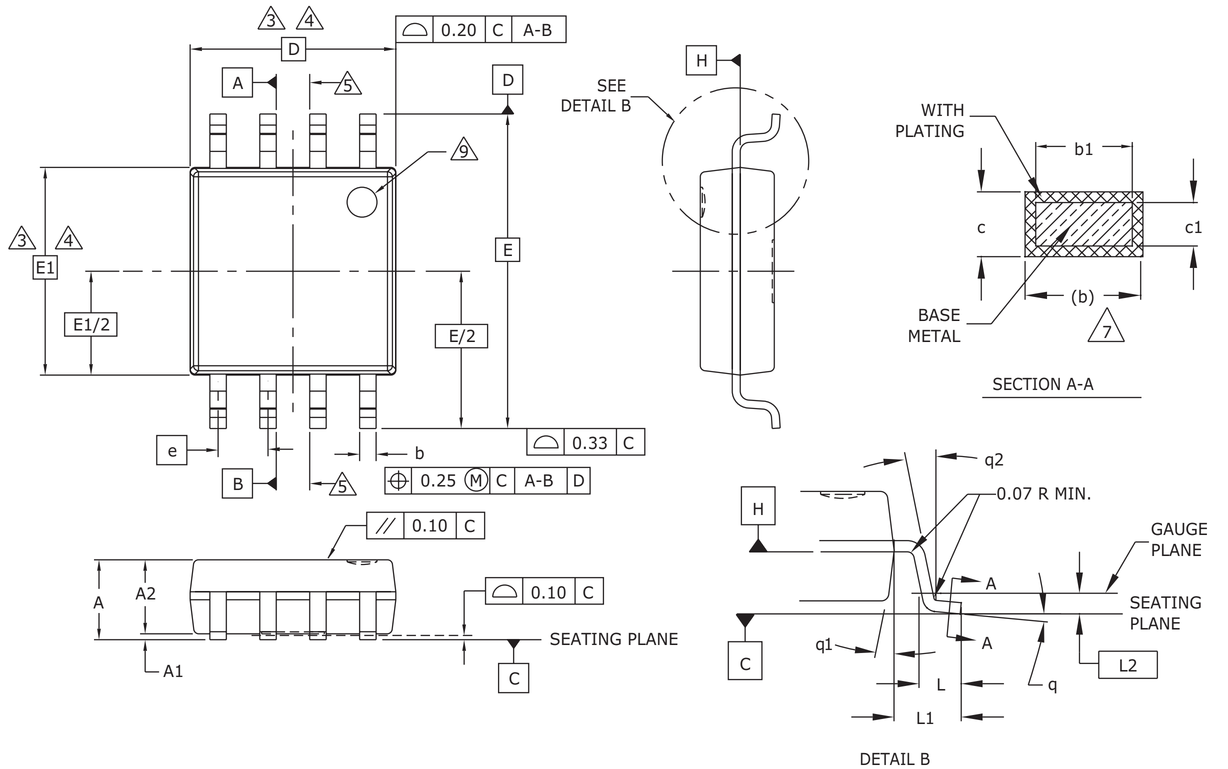


Figure 18.5 Write Protect Setup and Hold Timing during WRR when SRWD = 1



19. Physical Dimensions

19.1 SOC008 wide — 8-pin Plastic Small Outline Package (208-mils Body Width)



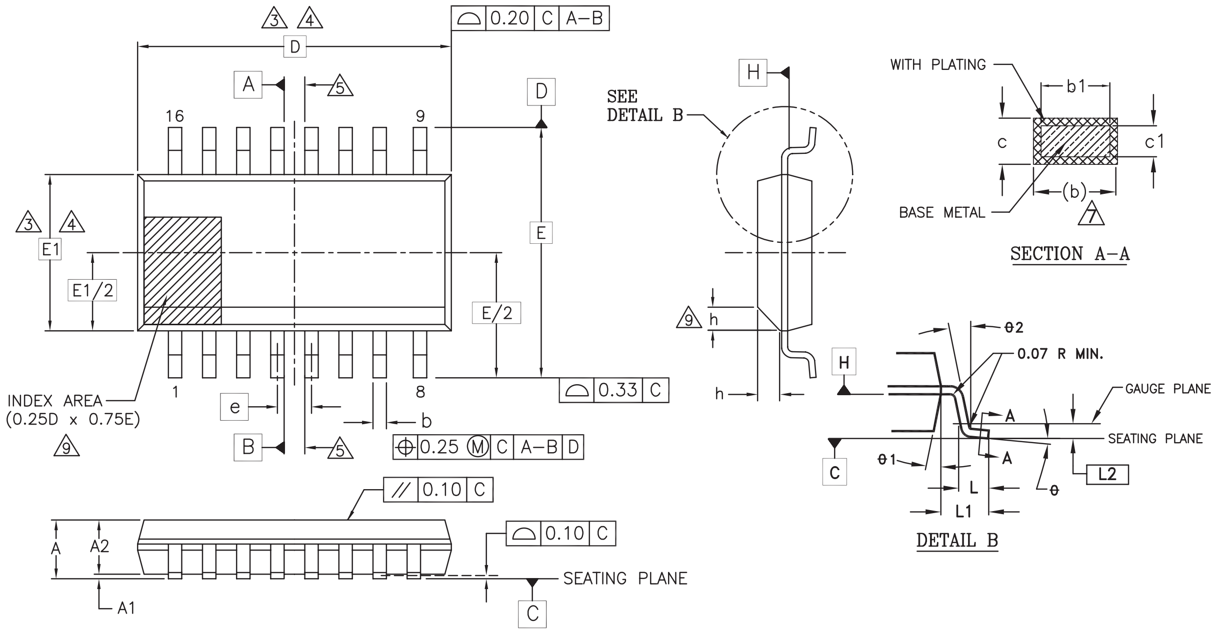
PACKAGE	SOC 008 (inches)		SOC 008 (mm)	
JEDEC				
SYMBOL	MIN	MAX	MIN	MAX
A	0.069	0.085	1.753	2.159
A1	0.002	0.0098	0.051	0.249
A2	0.067	0.075	1.70	1.91
b	0.014	0.019	0.356	0.483
b1	0.013	0.018	0.330	0.457
c	0.0075	0.0095	0.191	0.241
c1	0.006	0.008	0.152	0.203
D	0.208 BSC		5.283 BSC	
E	0.315 BSC		8.001 BSC	
E1	0.208 BSC		5.283 BSC	
e	.050 BSC		1.27 BSC	
L	0.020	0.030	0.508	0.762
L1	.055 REF		1.40 REF	
L2	.010 BSC		0.25 BSC	
N	8		8	
θ	0°	8°	0°	8°
$\theta 1$	5°	15°	5°	15°
$\theta 2$	0°		0°	

NOTES:

1. ALL DIMENSIONS ARE IN BOTH INCHES AND MILLMETERS.
2. DIMENSIONING AND TOLERANCING PER ASME Y14.5M - 1994.
3. DIMENSION D DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.15 mm PER END. DIMENSION E1 DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 mm PER SIDE. D AND E1 DIMENSIONS ARE DETERMINED AT DATUM H.
4. THE PACKAGE TOP MAY BE SMALLER THAN THE PACKAGE BOTTOM. DIMENSIONS D AND E1 ARE DETERMINED AT THE OUTMOST EXTREMES OF THE PLASTIC BODY EXCLUSIVE OF MOLD FLASH, TIE BAR BURRS, GATE BURRS AND INTERLEAD FLASH. BUT INCLUDING ANY MISMATCH BETWEEN THE TOP AND BOTTOM OF THE PLASTIC BODY.
5. DATUMS A AND B TO BE DETERMINED AT DATUM H.
6. "N" IS THE MAXIMUM NUMBER OF TERMINAL POSITIONS FOR THE SPECIFIED PACKAGE LENGTH.
7. THE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.10 TO 0.25 mm FROM THE LEAD TIP.
8. DIMENSION "b" DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.10 mm TOTAL IN EXCESS OF THE "b" DIMENSION AT MAXIMUM MATERIAL CONDITION. THE DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OF THE LEAD FOOT.
9. THIS CHAMFER FEATURE IS OPTIONAL. IF IT IS NOT PRESENT, THEN A PIN 1 IDENTIFIER MUST BE LOCATED WITHIN THE INDEX AREA INDICATED.
10. LEAD COPLANARITY SHALL BE WITHIN 0.10 mm AS MEASURED FROM THE SEATING PLANE.

3432 \ 16-038.03 \ 10.28.04

19.2 SO3 016 — 16-pin Wide Plastic Small Outline Package (300-mil Body Width)



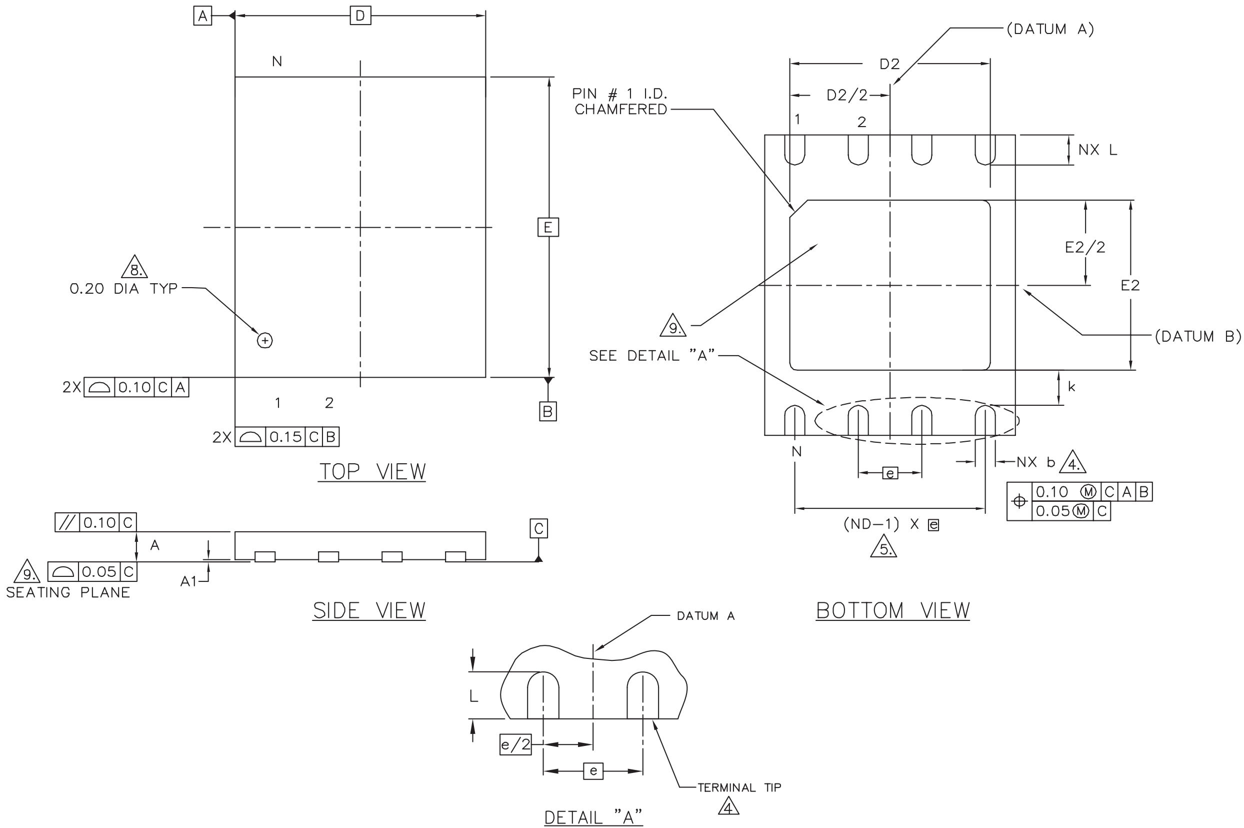
PACKAGE	SO3 016 (inches)		SO3 016 (mm)	
JEDEC	MS-013(D)AA		MS-013(D)AA	
SYMBOL	MIN	MAX	MIN	MAX
A	0.093	0.104	2.35	2.65
A1	0.004	0.012	0.10	0.30
A2	0.081	0.104	2.05	2.55
b	0.012	0.020	0.31	0.51
b1	0.011	0.019	0.27	0.48
c	0.008	0.013	0.20	0.33
c1	0.008	0.012	0.20	0.30
D	0.406 BSC		10.30 BSC	
E	0.406 BSC		10.30 BSC	
E1	0.295 BSC		7.50 BSC	
e	.050 BSC		1.27 BSC	
L	0.016	0.050	0.40	1.27
L1	.055 REF		1.40 REF	
L2	.010 BSC		0.25 BSC	
N	16		16	
h	0.10	0.30	0.25	0.75
θ	0°	8°	0°	8°
θ1	5°	15°	5°	15°
θ2	0°		0°	

NOTES:

1. ALL DIMENSIONS ARE IN BOTH INCHES AND MILLMETERS.
2. DIMENSIONING AND TOLERANCING PER ASME Y14.5M - 1994.
3. DIMENSION D DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.15 mm PER END. DIMENSION E1 DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 mm PER SIDE. D AND E1 DIMENSIONS ARE DETERMINED AT DATUM H.
4. THE PACKAGE TOP MAY BE SMALLER THAN THE PACKAGE BOTTOM. DIMENSIONS D AND E1 ARE DETERMINED AT THE OUTMOST EXTREMES OF THE PLASTIC BODY EXCLUSIVE OF MOLD FLASH, TIE BAR BURRS, GATE BURRS AND INTERLEAD FLASH. BUT INCLUDING ANY MISMATCH BETWEEN THE TOP AND BOTTOM OF THE PLASTIC BODY.
5. DATUMS A AND B TO BE DETERMINED AT DATUM H.
6. "N" IS THE MAXIMUM NUMBER OF TERMINAL POSITIONS FOR THE SPECIFIED PACKAGE LENGTH.
7. THE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.10 TO 0.25 mm FROM THE LEAD TIP.
8. DIMENSION "b" DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.10 mm TOTAL IN EXCESS OF THE "b" DIMENSION AT MAXIMUM MATERIAL CONDITION. THE DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OF THE LEAD FOOT.
9. THIS CHAMFER FEATURE IS OPTIONAL. IF IT IS NOT PRESENT, THEN A PIN 1 IDENTIFIER MUST BE LOCATED WITHIN THE INDEX AREA INDICATED.
10. LEAD COPLANARITY SHALL BE WITHIN 0.10 mm AS MEASURED FROM THE SEATING PLANE.

3601 \ 16-038.03 \ 8.31.6

19.3 USON 8-contact (5 x 6 mm) No-Lead Package



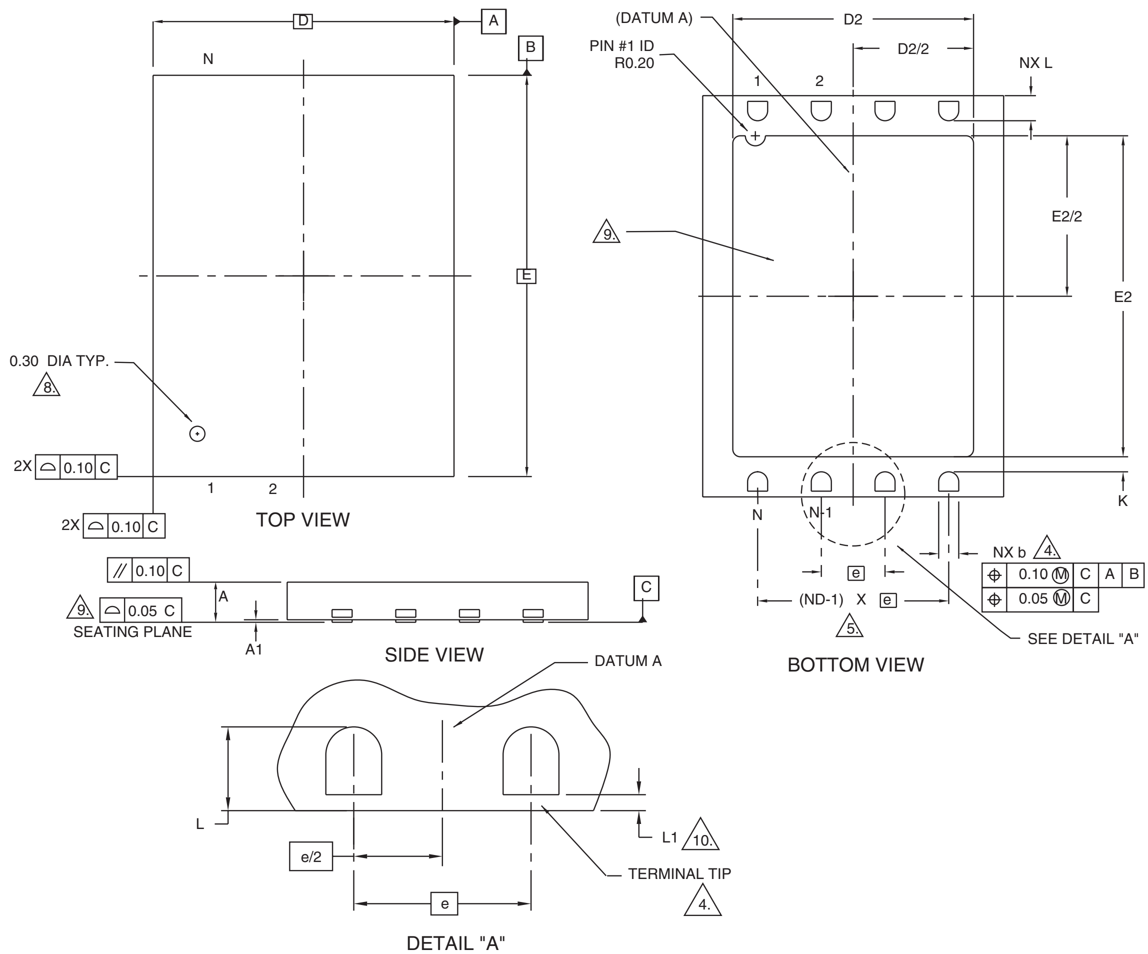
QUAD FLAT NO LEAD PACKAGES (UNE) - PLASTIC				
	DIMENSIONS			
SYMBOL	MIN	NOM	MAX	NOTE
e		1.27 BSC		
N		8		3
ND		4		5
L	0.55	0.60	0.65	
b	0.35	0.40	0.45	4
D2	3.90	4.00	4.10	
E2	3.30	3.40	3.50	
D		5.00 BSC		
E		6.00 BSC		
A	0.45	0.50	0.55	
A1	0.00	0.02	0.05	
K		0.20 MIN.		
θ	0	---	12	2

NOTES:

1. DIMENSIONING AND TOLERANCING CONFORMS TO ASME Y14.5M-1994.
2. ALL DIMENSIONS ARE IN MILLIMETERS, 0 IS IN DEGREES.
3. N IS THE TOTAL NUMBER OF TERMINALS.
4. DIMENSION b APPLIES TO METALLIZED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.30 mm FROM TERMINAL TIP. IF THE TERMINAL HAS THE OPTIONAL RADIUS ON THE OTHER END OF THE TERMINAL, THE DIMENSION b SHOULD NOT BE MEASURED IN THAT RADIUS AREA.
5. ND REFERS TOT HE NUMBER OF TERMINALS ON D SIDE.
6. MAXIMUM PACKAGE WARPAGE IS 0.05 mm.
7. MAXIMUM ALLOWABLE BURRS IS 0.076 mm IN ALL DIRECTIONS.
8. PIN #1 ID ON TOP WILL BE LASER MARKED.
9. BILATERAL COPLANARITY ZONE APPLIES TO THE EXPOSED HEAT SINK SLUG AS WELL AS THE TERMINALS.

3448\ 16-038.28 \ 04.19.05

19.4 WSON 8-contact (6 x 8 mm) No-Lead Package



QUAD FLAT NO LEAD PACKAGES (WSNB) - PLASTIC				
	DIMENSIONS			
SYMBOL	MIN	NOM	MAX	NOTE
e		1.27 BSC		
N		8		3
ND		4		5
L	0.45	0.50	0.55	
b	0.35	0.40	0.45	4
D2	4.70	4.80	4.90	
E2	6.30	6.40	6.50	
D		6.00 BSC		
E		8.00 BSC		
A	0.70	0.75	0.80	
A1	0.00	0.02	0.05	
L1		0.15 MAX.		10
θ	0	---	12	2
K		0.20 MIN.		

NOTES:

1. DIMENSIONING AND TOLERANCING CONFORMS TO ASME Y14.5M-1994.
2. ALL DIMENSIONS ARE IN MILLIMETERS, SYM θ IS IN DEGREES.
3. N IS THE TOTAL NUMBER OF TERMINALS.
4. DIMENSION b APPLIES TO METALLIZED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.30 mm FROM TERMINAL TIP. IF THE TERMINAL HAS THE OPTIONAL RADIUS ON THE OTHER END OF THE TERMINAL, THE DIMENSION b SHOULD NOT BE MEASURED IN THAT RADIUS AREA.
5. ND REFERS TOT HE NUMBER OF TERMINALS ON D SIDE.
6. MAXIMUM PACKAGE WARPAGE IS 0.05 mm.
7. MAXIMUM ALLOWABLE BURRS IS 0.076 mm IN ALL DIRECTIONS.
8. PIN #1 ID ON TOP WILL BE LASER MARKED.
9. BILATERAL COPLANARITY ZONE APPLIES TO THE EXPOSED HEAT SINK SLUG AS WELL AS THE TERMINALS.
10. A MAXIMUM 0.15 mm PULL BACK (L1) MAY BE PRESENT.

3408\ 16-038.28a

20. Revision History

Section	Description
Revision 01 (June 9, 2008)	
	Initial release.
Revision 02 (February 12, 2009)	
Connection Diagrams	Added USON package.
Valid Combinations Table	Added Tray packing type.
Configuration Register	Added OTP description for BPNV bit.
Configuration Register Table	Corrected TBPARM description. Added “Default” setting information upon initial factory shipment.
Instruction Set	Separated Mode bit and Dummy bytes.
Product Group CFI Primary Vendor-Specific Extended Query	Corrected data of 45h bytes.
Read-ID (READ_ID)	Removed statement of 8-cycle buffer for Manufacturer ID and the Device ID.
Read Status Register	Corrected description for SRWD bit in the Status Register Table. Modified E_ERR and P_ERR descriptions.
Read Configuration Register	Updated figure.
Parameter Sector Erase (P4E, P8E)	Updated figure.
Release from Deep Power-Down and Read Electronic Signature (RES)	Updated figure.
OTP Regions	Modified description for the ACC function.
Power-up and Power-down	Changed specification for t_{PU}.
Absolute Maximum Ratings	Corrected the Table.
DC Characteristics	Changed maximum specifications for I_{CC1} and I_{CC3}. Modified Test Conditions for I_{SB1} and I_{PD}.
AC Characteristics	Changed maximum specifications for t_W and t_{PE}. Changed typical time for t_{EP}. Added note for max values assume 100k cycles. Changed Clock High/Low time.

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