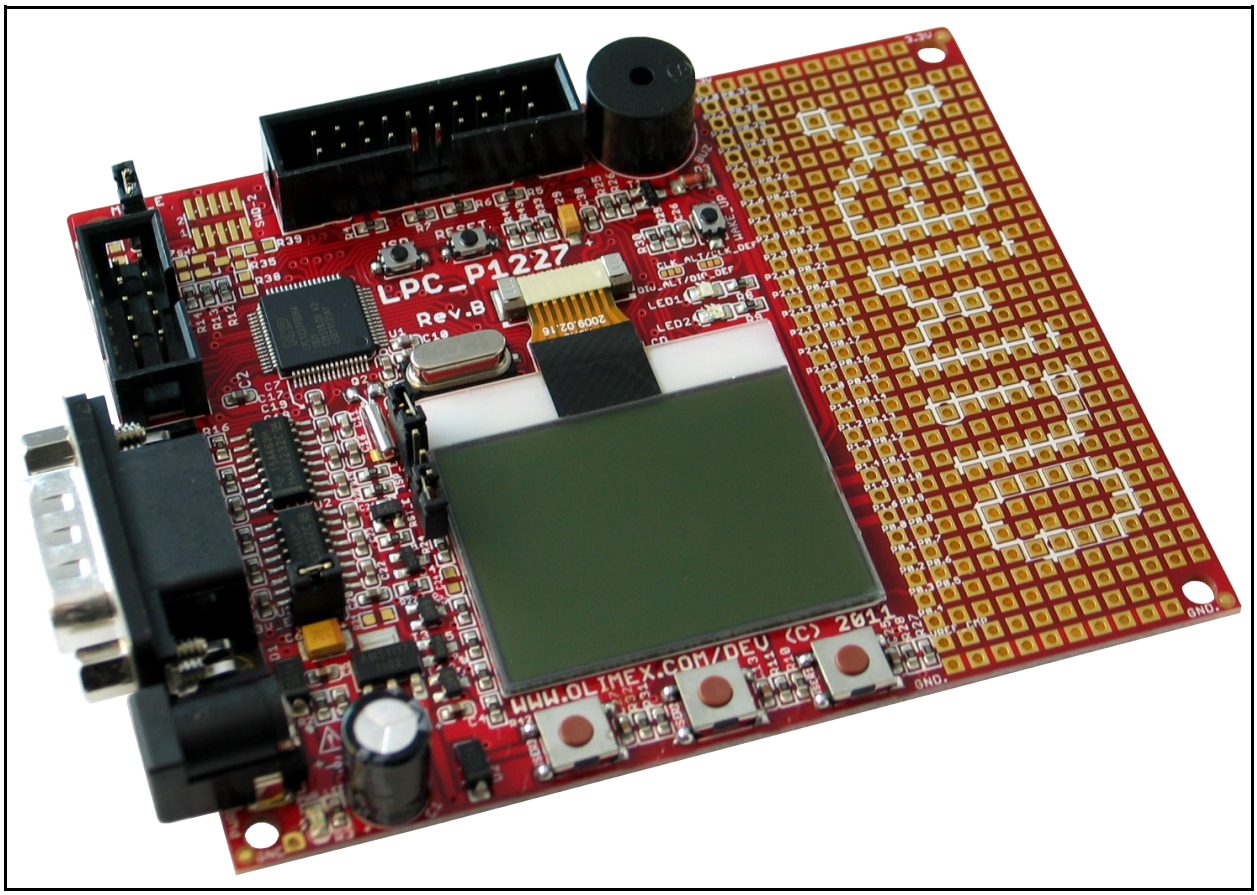

LPC-P1227 development board
USER'S MANUAL

Initial release, March 2012
Designed by OLIMEX Ltd, 2011

lead-free

All boards produced by Olimex LTD are ROHS compliant

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Thank you for purchasing LPC-P1227 development board assembled by OLIMEX LTD

Table of Contents

CHAPTER 1

OVERVIEW

1. Introduction to the chapter

Thank you for choosing the LPC-P1227 development board from Olimex! This document provides a User's Guide for the Olimex LPC-P1227 development board. As an overview, this chapter gives the scope of this document and lists the board's features. The document's organization is then detailed.

The LPC-P1227 development board enables code development of applications running on the LPC1227 Cortex-M0 microcontroller, manufactured by NXP Semiconductors.

1.1 Features

- MCU: LPC1227 Cortex-M0, up to 45Mhz, 128 kB Flash, 8kB SRAM, 2 UARTs , SPI, I2C, 10 bit ADC
- RS232
- Buzzer
- NOKIA 3310 LCD
- 12 MHz crystal resonator
- Power supply circuit
- Power-on LED
- Debug interface – SWD (Serial Wire Debug)
- UEXT connector
- Two user leds
- Three user buttons
- Reset button
- Prototype area
- FR-4, 1.5 mm, soldermask, component print
- Dimensions:80x50mm (3.15 x 1.97")

1.2 Organization

Each section in this document covers a separate topic, organized as follow:

- Chapter 1 is an overview of the board usage and features
- Chapter 2 provides a guide for quickly setting up the board
- Chapter 3 contains the general board diagram and layout
- Chapter 4 describes the component that is the heart of the board: the LPC1227FBD64 microcontroller
- Chapter 5 is an explanation of the control circuitry associated with the microcontroller to reset. Also shows the clocks on the board
- Chapter 6 covers the connector pinout, peripherals and jumper description
- Chapter 7 shows the processor diagram and memory map
- Chapter 8 provides the schematics
- Chapter 9 contains the revision history

CHAPTER 2

SETTING UP THE LPC-P1227 BOARD

2. Introduction to the chapter

This section helps you set up the LPC-P1227 development board for the first time.

Please consider first the electrostatic warning to avoid damaging the board, then discover the hardware and software required to operate the board.

The procedure to power up the board is given, and a description of the default board behavior is detailed.

2.1 Electrostatic warning

LPC-P1227 is shipped in a protective anti-static package. The board must not be exposed to high electrostatic potentials. A grounding strap or similar protective device should be worn when handling the board. Avoid touching the component pins or any other metallic element.

2.2 Requirements

In order to set up and program the LPC-P1227, the following items are required:

- A source of power – the board can be powered through the PWR jack or through the SWD-1 (SWD-2) interface

- In order to program the board you will need a programmer that supports SWD (Serial Wire Debug) interface

Also, a host-based software toolchain is required in order to program/debug the LPC-P1227 board. There are also a number of ready IDEs available like IAR Embedded Workbench, Rowley CrossWorks, Code Composer Studio, etc.

The only low cost Olimex option at the time writing this guide is available if you use Rowley's Crossworks IDE. You can get any of our ARM-USB debuggers + ARM-JTAG-SWD adapter. As of moment of writing this guide OpenOCD 0.5.0 doesn't support SWD flashing.

2.3 Powering the board

- Provide between 5V and 9V to the board's PWR jack

OR

- Connect your SWD debugger

2.4 Prebuilt software

On powering the board the PWR LED should turn on. LED1 and LED2 should start blinking alternatively. The LCD display shows 6 lines of text. You can connect the board to a PC via RS232 Null-modem interface. Then start your favourite terminal program at 115200, 8-N-1 and reset the board. A line with the statuses of 4 buttons (USER3, USER2, USER1, WAKE_UP) and ISP_E jumper appears. Press the buttons to see their state changing or change the jumper position. Pressing escape will disconnect the RS232.

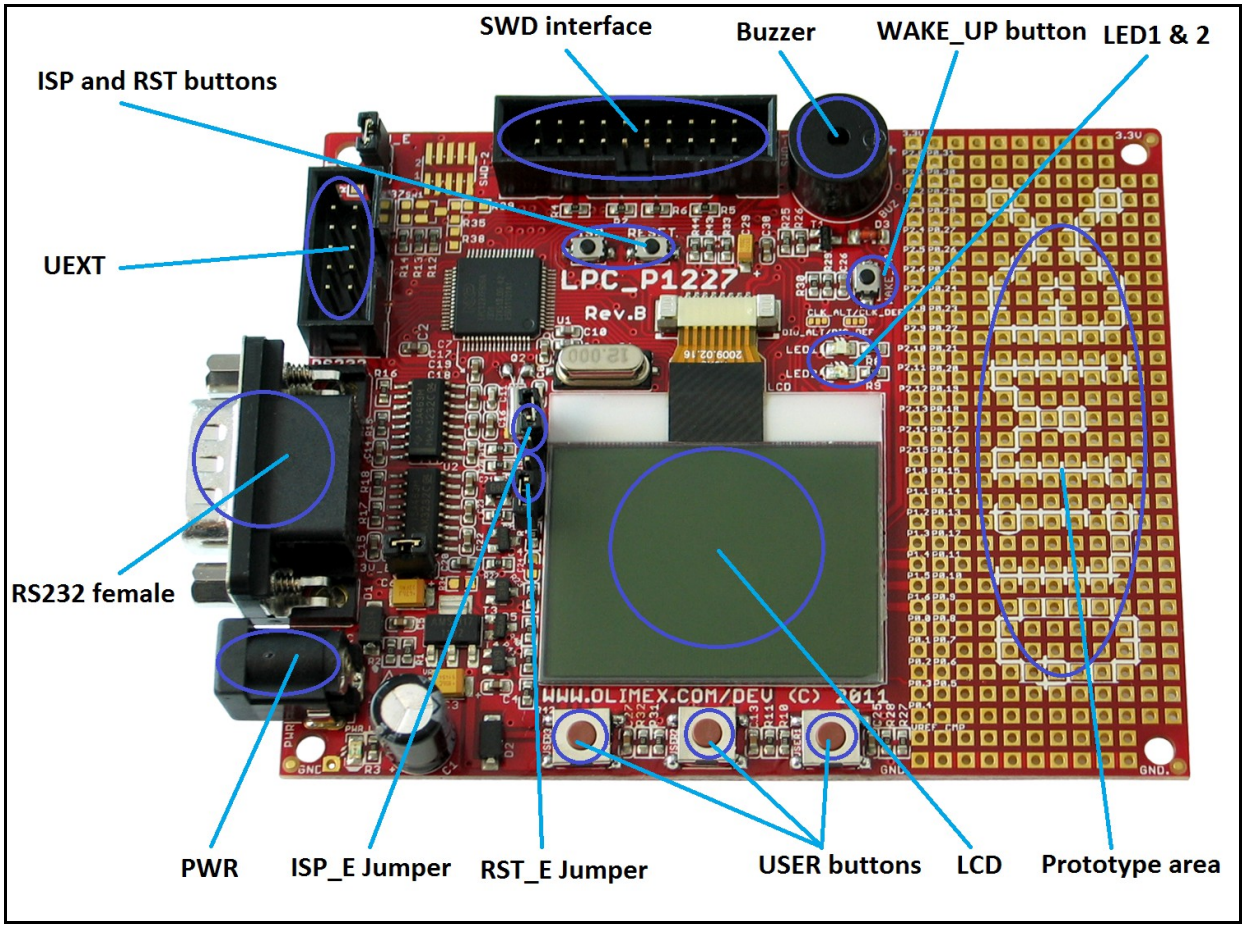
CHAPTER 3

LPC-P1227 BOARD DESCRIPTION

3. Introduction to the chapter

Here you get acquainted with the main parts of the board. Note the names used on the board differ from the names used to describe them. For the actual names check the LPC-P1227 board itself.

3.1 Layout (top view)



CHAPTER 4

THE LPC1227FBD64 MICROCONTROLLER

4. Introduction to the chapter

In this chapter is located the information about the heart of LPC-P1227 – its microcontroller. The information is a modified version of the datasheet provided by its manufacturers.

4.1 The microcontroller

Main processors features:

- Processor core
  - ✗ ARM Cortex-M0 processor, running at 45 MHz (one wait state from flash) or 30 MHz (zero wait states from flash). The LPC122x have a high score of over 45 in CoreMark CPU performance benchmark testing, equivalent to 1.51/MHz.
  - ✗ ARM Cortex-M0 built-in Nested Vectored Interrupt Controller (NVIC).
  - ✗ Serial Wire Debug (SWD).
  - ✗ System tick timer.
- Memory
  - ✗ 8 kB SRAM.
  - ✗ 128 kB on-chip flash programming memory.
  - ✗ In-System Programming (ISP) and In-Application Programming (IAP) via on-chip bootloader software.
  - ✗ Includes ROM-based 32-bit integer division routines.
- Clock generation unit
  - ✗ Crystal oscillator with an operating range of 1 MHz to 25 MHz.
  - ✗ 12 MHz Internal RC (IRC) oscillator trimmed to 1 % accuracy that can optionally be used as a system clock.
  - ✗ PLL allows CPU operation up to the maximum CPU rate without the need for a high-frequency crystal. May be run from the system oscillator or the internal RC oscillator.
  - ✗ Clock output function with divider that can reflect the system oscillator clock, IRC clock, main clock, and Watchdog clock.
  - ✗ Real-Time Clock (RTC).
- Digital peripherals
  - ✗ Micro DMA controller with 21 channels.

  - ✗ CRC engine.
  - ✗ Two UARTs with fractional baud rate generation and internal FIFO. One UART with RS-485 and modem support and one standard UART with IrDA.
  - ✗ SSP/SPI controller with FIFO and multi-protocol capabilities.
  - ✗ I2C-bus interface supporting full I2 C-bus specification and Fast-mode Plus with a data rate of 1 Mbit/s with multiple address recognition and monitor mode. I2C-bus pins have programmable glitch filter.
  - ✗ 55 General Purpose I/O (GPIO) pins with programmable pull-up resistor, open-drain mode, programmable digital input glitch filter, and programmable input inverter.
  - ✗ Programmable output drive on all GPIO pins. Four pins support high-current output drivers.
  - ✗ All GPIO pins can be used as edge and level sensitive interrupt sources.
  - ✗ Four general purpose counter/timers with four capture inputs and four match outputs (32-bit timers) or two capture inputs and two match outputs (16-bit timers).
  - ✗ Windowed WatchDog Timer (WWDT); IEC-60335 Class B certified.
- Analog peripherals
  - ✗ One 8-channel, 10-bit ADC.
  - ✗ Two highly flexible analog comparators. Comparator outputs can be programmed to trigger a timer match signal or can be used to emulate 555 timer behavior.
- Power
  - ✗ Three reduced power modes: Sleep, Deep-sleep, and Deep power-down.
  - ✗ Processor wake-up from Deep-sleep mode via start logic using 12 port pins.
  - ✗ Processor wake-up from Deep-power down and Deep-sleep modes via the RTC.
  - ✗ Brownout detect with three separate thresholds each for interrupt and forced reset.
  - ✗ Power-On Reset (POR).
  - ✗ Integrated PMU (Power Management Unit).
- Unique device serial number for identification.
- 3.3 V power supply

For comprehensive information on the microcontroller visit the NXP web page for a datasheet.

At the moment of writing the microcontroller datasheet can be found at the following link:
http://ics.nxp.com/products/lpc1000/datasheet/lpc122x.pdf

CHAPTER 5
CONTROL CIRCUITY

5. Introduction to the chapter

Here you can find information about reset circuit, power circuit and quartz crystal locations.

5.1 Reset

LPC-P1227 reset circuit includes R23 (10 KΩ), R24(330 Ω), LPC1227FB064 pin PIN40 (PIO0_13/RESET) and a RESET button.

5.2 Clocks

12 MHz quarz crystal Q1 is found at pins 1 and 2 of the processor.

Real time clock (RTC) Q2 is connected to pins 57 and 58 of the processor.

CHAPTER 6

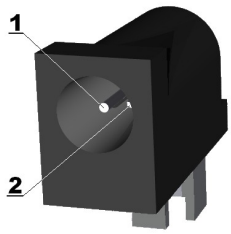
HARDWARE

6. Introduction to the chapter

In this chapter are presented the connectors that can be found on the board all together with their pinout. Proto area is shown. Jumpers functions are described. Notes and info on specific peripherals are presented. Notes regarding the interfaces are given.

6.1 PWR Connector

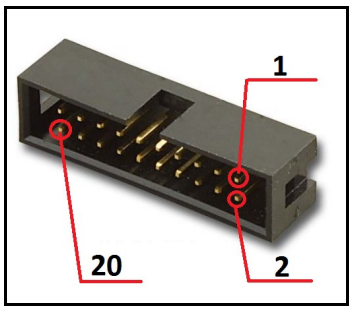
Pin #	Signal Name
1	PWR
2	GND



6.2 SWD1 connector

The 20 pin SWD (Serial Wire Debug) connector provides the interface for SWD programming/debugging. The pinout can be found in the table below.

SWD1 Connector			
Pin #	**Signal Name**	**Pin #**	**Signal Name**
1	VCC	11	GND
2	VCC	12	GND
3	Not connected	13	SWO
4	GND	14	GND
5	Not connected	15	RST



6	GND	**16**	GND
7	SWDIO	**17**	GND
8	GND	**18**	GND
9	SWCLK	**19**	+5V
10	GND	**20**	GND

6.3 SWD2 Header

Note! It doesn't have connector mounted, if you wish to use 20 pin SWD debugger you have to mount connector yourself. Signal between the two SWD interfaces is controlled by CLK_ALT/CLK_DEF and DIO_ALT/DIO_DEF. If you set them in _ALT positions the SWD2 would be enabled.

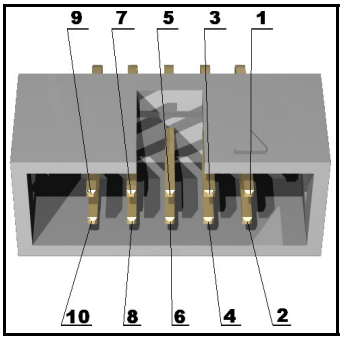
SWD2 Header			
Pin #	**Signal Name**	**Pin #**	**Signal Name**
1	+3.3V	**6**	SWO
2	SWDIO	**7**	Not connected
3	GND	**8**	Not connected
4	SWCLK	**9**	GND
5	GND	**10**	RST

6.4 UEXT

LPC-P1227 board has UEXT connector and can interface Olimex's UEXT modules.
For more information on UEXT please visit:

http://www.olimex.com/dev/OTHER/UEXT.pdf

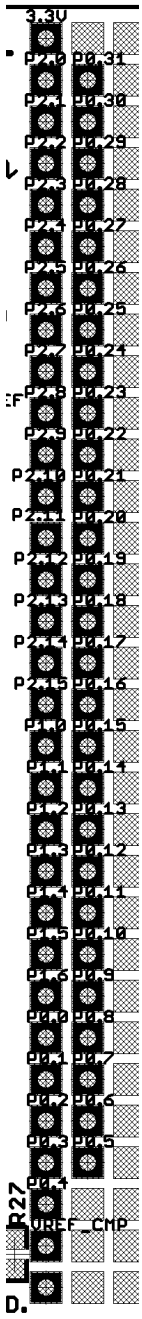
Pin #	Signal Name
1	+3.3V
2	GND
3	TXD1
4	RXD1
5	SCL
6	SDA
7	MISO
8	MOSI
9	SCK
10	SSEL



6.5 Pads on the proto area

For your convenience the pads are named individually near each of them. Please take extra care about the numbering but consider that there might be offset.

For full list of pin functions check on the processor data sheet.

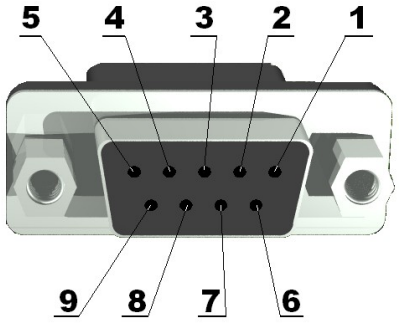


Pad Name	Signal	Pad Name	Signal
3.3V	3.3V row of pads	**3.3V**	3.3V row of pads
P2.0	PIO2_0	**P0.31**	PIO0_31
P2.1	PIO2_1	**P0.30**	PIO0_30
P2.2	PIO2_2	**P0.29**	PIO0_29
P2.3	PIO2_3	**P0.28**	PIO0_28
P2.4	PIO2_4	**P0.27**	PIO0_27
P2.5	PIO2_5	**P0.26**	**SWCLK_DEF**, PIO0_26
P2.6	PIO2_6	**P0.25**	**SWDIO_DEF**, PIO0_25
P2.7	PIO2_7	**P0.24**	PIO0_24
P2.8	PIO2_8	**P0.23**	PIO0_23
P2.9	PIO2_9	**P0.22**	PIO0_22
P2.10	**USER3**, PIO2_10	**P0.21**	PIO0_21
P2.11	**USER2**, PIO2_11	**P0.20**	PIO0_20
P2.12	**USER1**, PIO2_12	**P0.19**	PIO0_19
P2.13	**#RES**, PIO2_13	**P0.18**	**SWCLK_ALT**, PIO0_18
P2.14	**#SS**, PIO2_14	**P0.17**	**MOSI**, PIO0_17
P2.15	**D/#C**, PIO2_15	**P0.16**	**MISO**, PIO0_16
P1.0	PIO1_0	**P0.15**	**SSSL**, PIO0_15
P1.1	PIO1_1	**P0.14**	**SCK**, PIO0_14
P1.2	**SWDIO_OUT**, PIO1_2	**P0.13**	**RST**, PIO0_13

P1.3	**WAKE_UP**, PIO1_3	**P0.12**	**ISP_E**, PIO0_12
P1.4	PIO1_4	**P0.11**	**SDA**, PIO0_11
P1.5	PIO1_5	**P0.10**	**SCL**, PIO0_10
P1.6	**BUZZER**, PIO1_6	**P0.09**	**TXD1**, PIO0_9
P0.0	**#RTS0**, PIO0_0	**P0.08**	**RXD1**, PIO0_8
P0.1	**RXD0**, PIO0_1	**P0.07**	**#CTS0**, PIO0_7
P0.2	**TXD0**, PIO0_2	**P0.06**	**#RI0**, PIO0_6
P0.3	**DTR0**, PIO0_3	**P0.05**	**#DCD0**, PIO0_5
P0.4	**#DSR0**, PIO0_4	-	-
VREF CMP		-	-
GND	GND row of pads	**GND**	GND row of pads

6.6 RS232 Null-modem connector

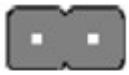
Pin #	Signal
1	DTE_CD
2	DTE_RD
3	DTE_TD
4	DTE_DTR
5	GND
6	DTE_DSR
7	DTE_RTS
8	DTE_CTS
9	DTE_RI



6.7 Jumper description

Note that the jumper configuration is also printed on the back of the board.

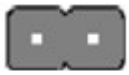
ISP_E



This jumper controlls the possibility of the ISP mode via UART0 (RS232) supported by the processor. It should be moved together with RST_E.

Default state is open.

RST_E



When closed together with ISP_E enables ISP programming via UART0

Default state is open.

CLK_ALT/CLK_DEF and DIO_ALT/DIO_DEF

These jumpers should be moved together and control whether SWD-1 or SWD-2 interface is used for programming. When in position ALT – SWD-2 will be used.

Default positions are CLK_DEF and DIO_DEF.

MCU_E

If open disables the supply on the processor.

Default state is closed.

3.3V_E

If open disables the board's 3.3V power supply.

Default state is closed.

6.8 LCD Display

Nokia 3310 LCD display 84x48 pixels (38x35 mm).

6.9 Additional hardware components

The components below are mounted on LPC-P1227 but are not discussed above. They are listed here for completeness:

Buzzer

5 buttons + RST button

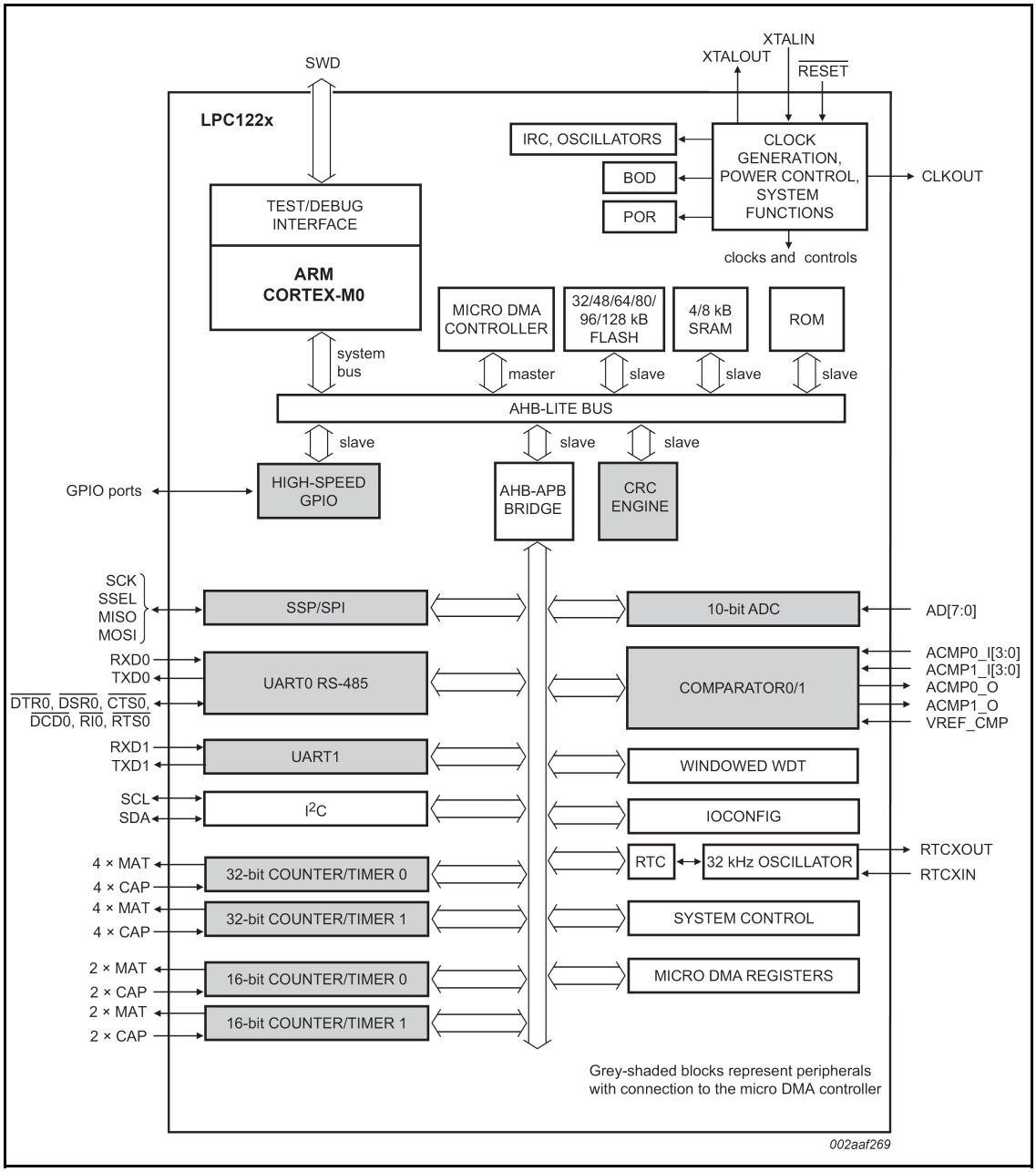
2LEDs + power-on LED

CHAPTER 7

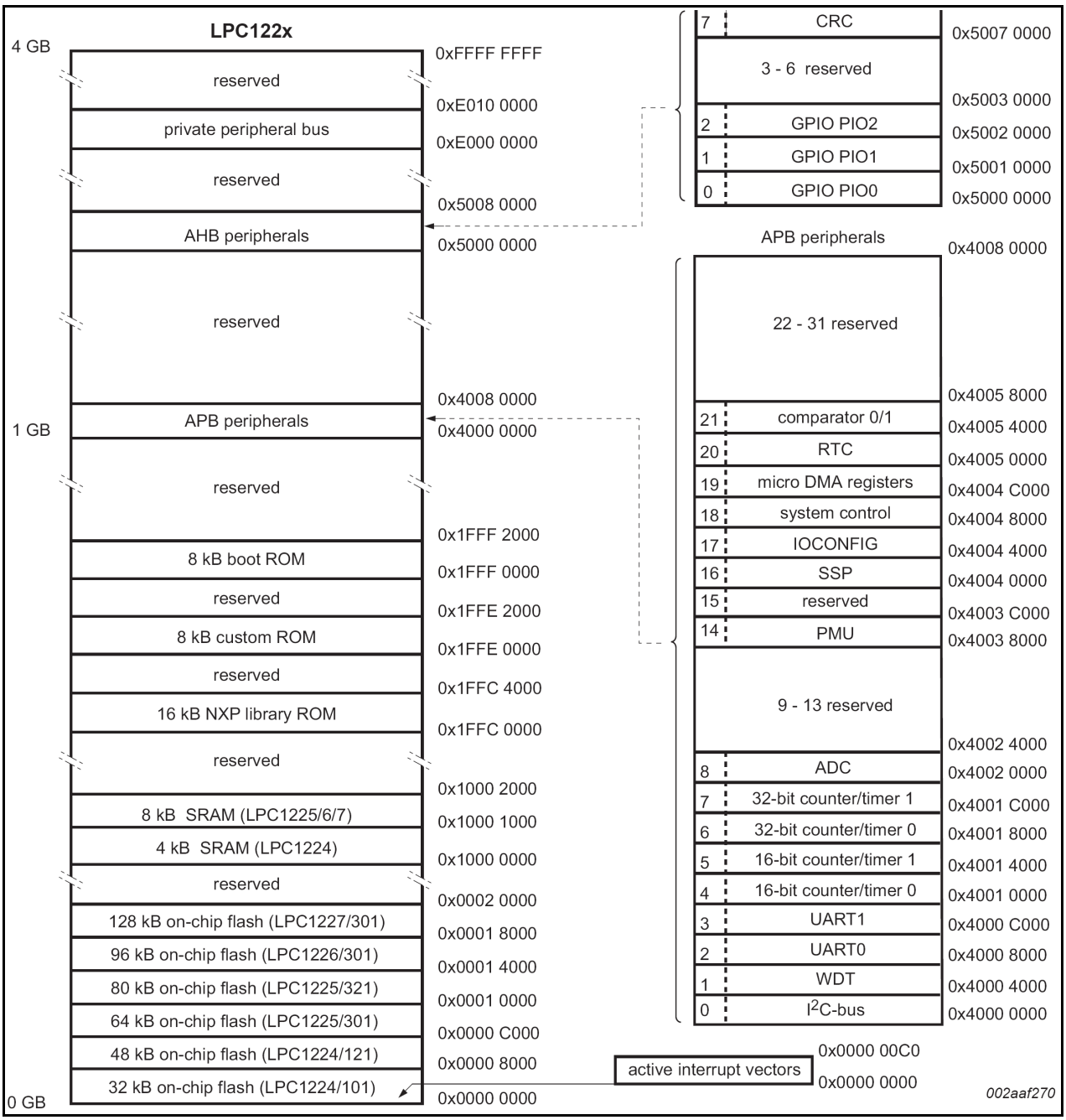
MEMORY AND BLOCK DIAGRAM

7. Introduction to the chapter

Below is located the block diagram of the processor and on the next page you can find a memory map for this family of processors. It is strongly recommended to refer to the original datasheet released by NXP for ones of higher quality.



7.1 Memory organization



CHAPTER 8

SCHEMATICS

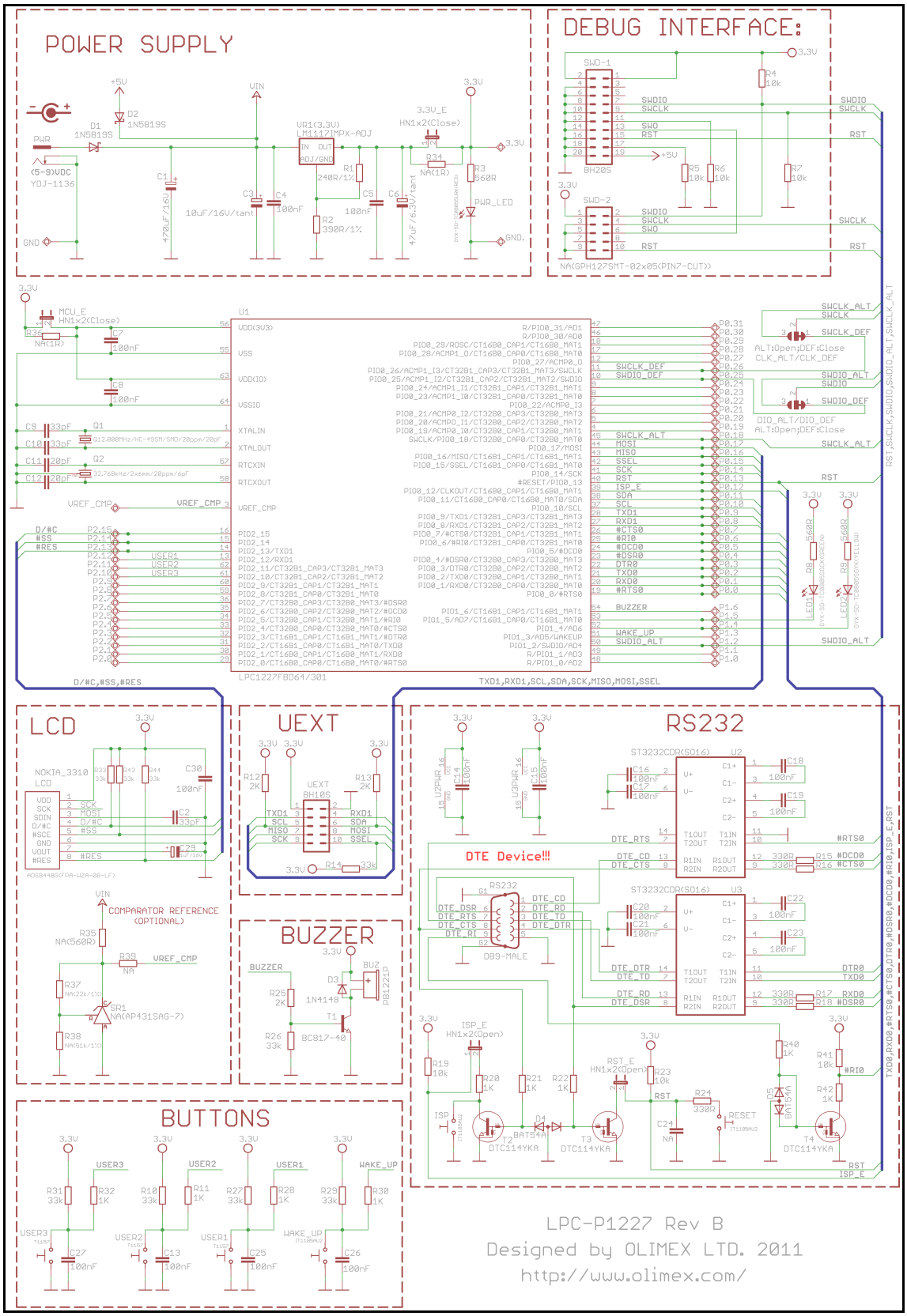
8. Introduction to the chapter

In this chapter are located the schematics describing logically and physically LPC-P1227.

8.1 Eagle schematic

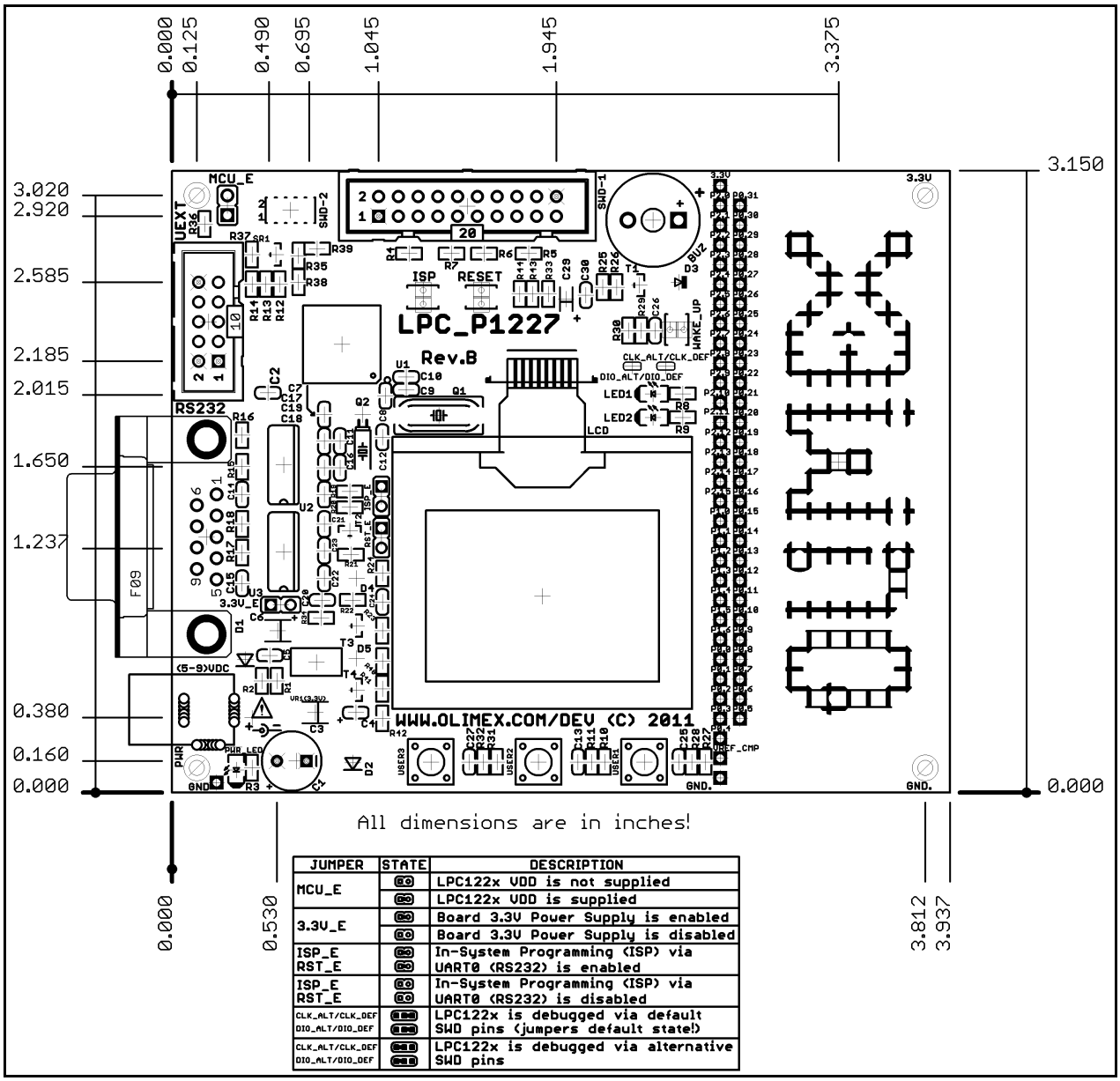
LPC-P1227 schematic is visible for reference here. You can also find them on the web page for LPC-P1227 at our site: http://www.olimex.com/dev/LPC-P1227.html. They are located in HARDWARE section.

The EAGLE schematic is situated on the next page for quicker reference.


POWER SUPPLY
DEBUG INTERFACE:
LCD
UEXT
RS232
BUZZER
BUTTONS
LPC-P1227 Rev B
Designed by OLIMEX LTD. 2011
http://www.olimex.com/

8.2 Physical dimensions

Note that all dimensions are in inches.



JUMPER	STATE	DESCRIPTION
MCU_E		LPC122x VDD is not supplied
		LPC122x VDD is supplied
3.3V_E		Board 3.3V Power Supply is enabled
		Board 3.3V Power Supply is disabled
ISP_E RST_E		In-System Programming (ISP) via UART0 (RS232) is enabled
ISP_E RST_E		In-System Programming (ISP) via UART0 (RS232) is disabled
CLK_ALT/CLK_DEF DIO_ALT/DIO_DEF		LPC122x is debugged via default SWD pins (jumpers default state!)
CLK_ALT/CLK_DEF DIO_ALT/DIO_DEF		LPC122x is debugged via alternative SWD pins

CHAPTER 9

REVISION HISTORY

9. Introduction to the chapter

In this chapter you will find the current and the previous version of the document you are reading. Also the web-page for your device is listed. Be sure to check it after a purchase for the latest available updates and examples.

9.1 Document revision

Revision	Changes	Modified Pages
A	Initial Creation	All

9.2 Web page of your device

The web page you can visit for more info on your device is http://www.olimex.com/dev/LPC-P1227.html. There you can find more info and some examples.

ORDER CODES:

LPC-P1227 - completely assembled and tested

How to order?
You can order to us directly or by any of our distributors.
Check our webpage http://www.olimex.com/ for more info.