Application Note AN-SS3

SGDR600P1: 6 A JFET Gate Driver Reference Design & Demoboard

Optimized for high-speed hard switching

SemiSouth

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Table of Contents

Features and Specifications

Overview: This 6 A gate driver reference design is optimized for driving SemiSouth's SJEP120R063 & SJEP120R050 vertical JFETs. Incorporating an opto isolator front end, this design enables fast turn-on and turn-off in "Isolated Bridge" topologies while maintaining low conduction losses. ***NOTE:*** *With a few resistor value changes, this driver can easily be modified to also drive the 100 mΩ and depletion mode devices (See page 13-16 for modification instructions).*

Features:

- **Dual Drive – switching & conduction**
- **Peak Gate Current +6/-3 A**
- **Very Fast Switching up to 250 kHz**
- **Opto Isolation 3750 VAC**
- **15 V to 6 V DCDC for lowered gate power**
- **Low BOM Cost**

Applications:

- **Hard Switched Bridge Topologies**
- **Solar Inverters**
- **IT/Telecom Power Supplies**
- **Medical and Laser Power Supplies**
- **Recommended for the following JFETs**

SJEP120R063 Eon + Eoff: 225 µJ

SJEP120R050 Eon + Eoff: 237 µJ

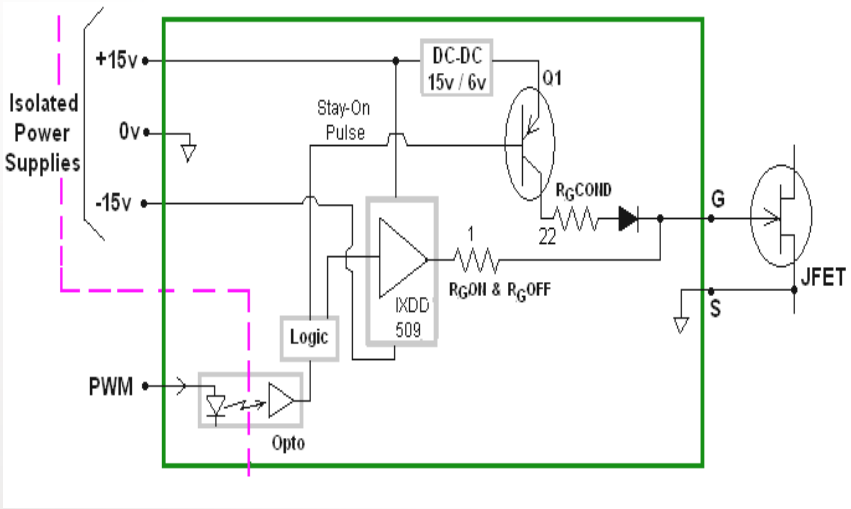
Gate Drive Specifications:

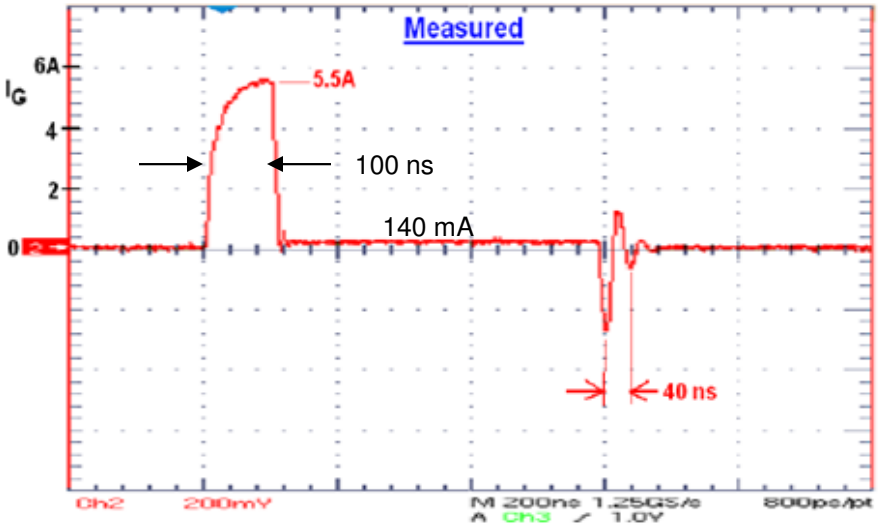
Max Gate Voltage Output	+15 V / -15 V
Peak Gate Current	+6/-3 A
Propagation Delay on/off	130 ns
Rise and Fall times	< 20 ns
Duty Cycle Range	0 to 100%
On-State Gate Current	140 mA (adjustable)

Maximum Ratings:

External Power Supplies	+15 V and -15 V
Power Supply Currents	+300 mA and -75 mA
On-State Gate Current	140 mA (50% D.C.)
Isolation voltage	3750 V (for 1 min)
Operating Temp Range	-0 C to +85 C

Functional Description





Opto Coupler: This reference design uses the Toshiba TLP715F high speed opto coupler enabling fast switching speeds while allowing layout spacing to meet safety isolation requirements.

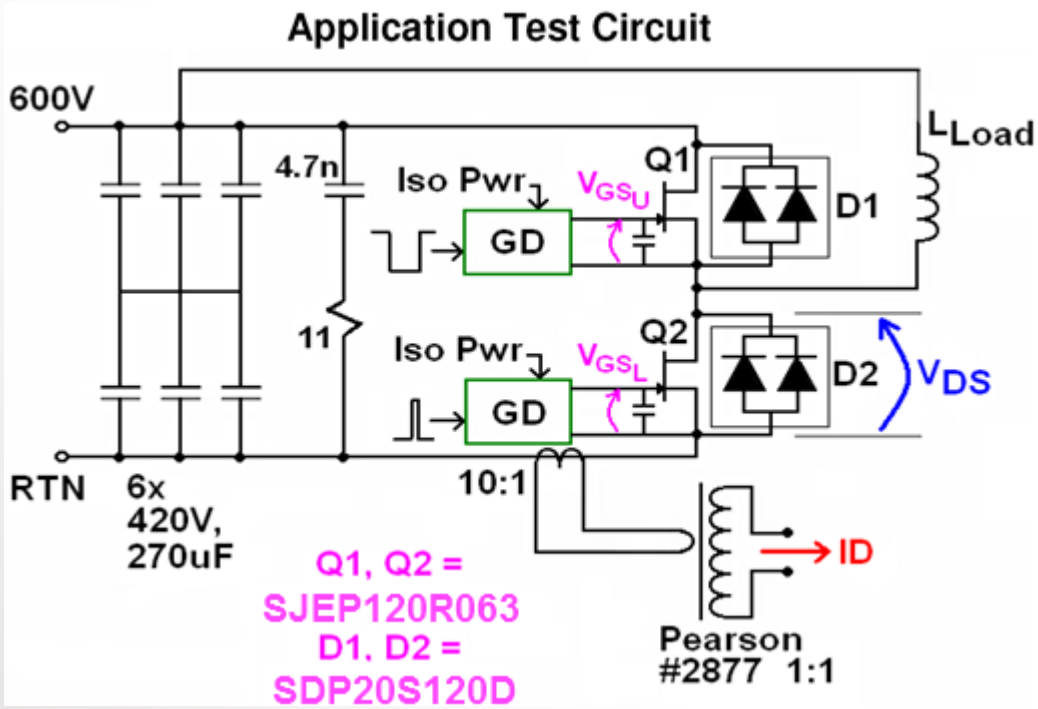
509 Gate Driver: The IXYS IXDD509 high-speed Driver is used to provide a high-current turn-on and turn-off gate pulse through $R_{G(on/off)}$ for fast switching and low switching losses. ***NOTE:*** *IXDD509 has since been discontinued by IXYS and replaced with the IXDD609 sold by Clare Electronics. The IXDD609 is not available as a DFN6 and so layout modifications will be necessary to accommodate a new footprint for the Clare replacement part.*

Q1 Conduction Driver: Q1 is a small PNP transistor used to provide the ON-state gate current of 140 mA to maintain a low $R_{DS(on)}$ during the conduction period.

15 V to 6 V DCDC: This step-down (80% eff) DCDC converter IC is used as the power source for Q1 and enables a reduction in gate power loss during the conduction period. (optional).

Timing Logic: The logic / timing circuit generates the required timing signal for the IXDD509 gate Driver and Q1. The timing is set to achieve a 100 ns turn on high I pulse and then maintain the 140 mA conduction pulse.

Switching Test Circuit



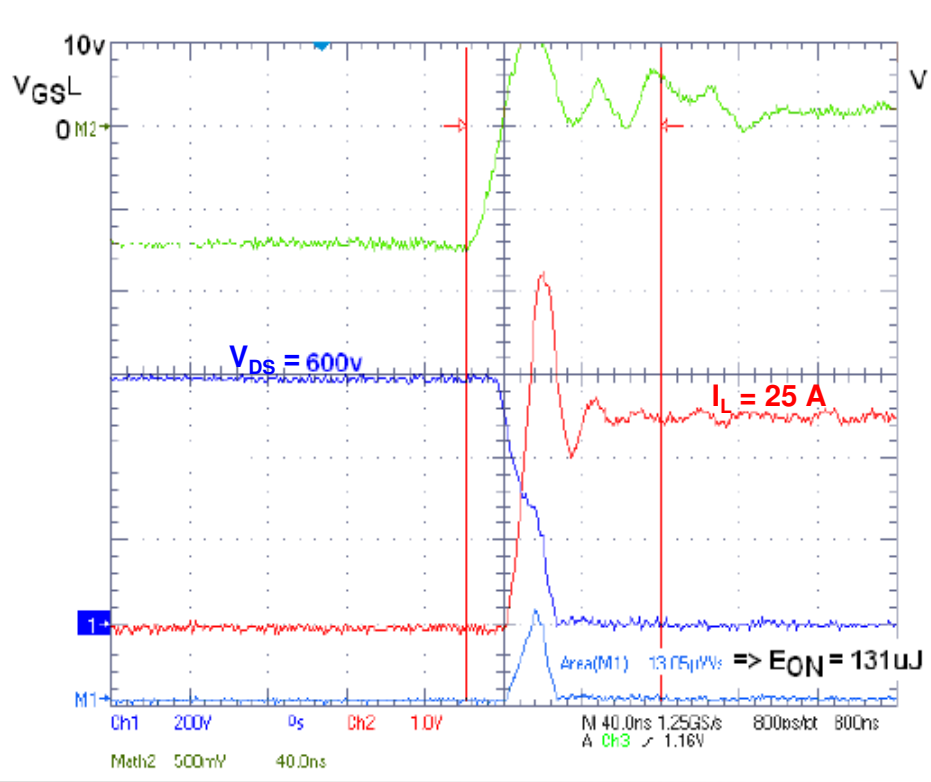
Test Conditions

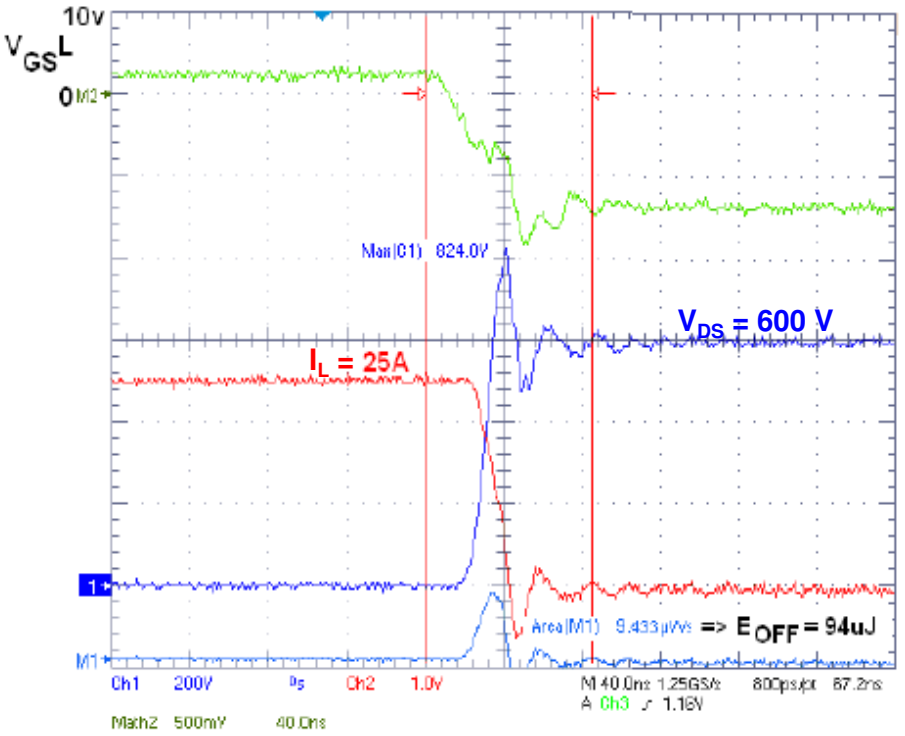
1. Results for SJEP120R063
2. Phase-leg configuration
3. V_{DC} = 600V; I_{LPK} = 25A, TA = 25°C
4. RC snubber equal to 11 ohms and 4.7nF
5. 400uH load inductance
6. Each device driven by separate SGDR600P1
7. Gate driver power supplies of +/- 15V
8. Gate driver approx. 5 mm from gate terminal
9. 3.3nF gate-source capacitive clamp

Comments:

1. It is recommended to use a snubber (4.7 nF and 11 Ω) across the DC Bus in the event there is ringing in the power circuit.
2. It is recommended to use a 3.3 nF capacitor connected tight across the gate-source terminals of Q1 and Q2 for added noise immunity in the bridge configuration.

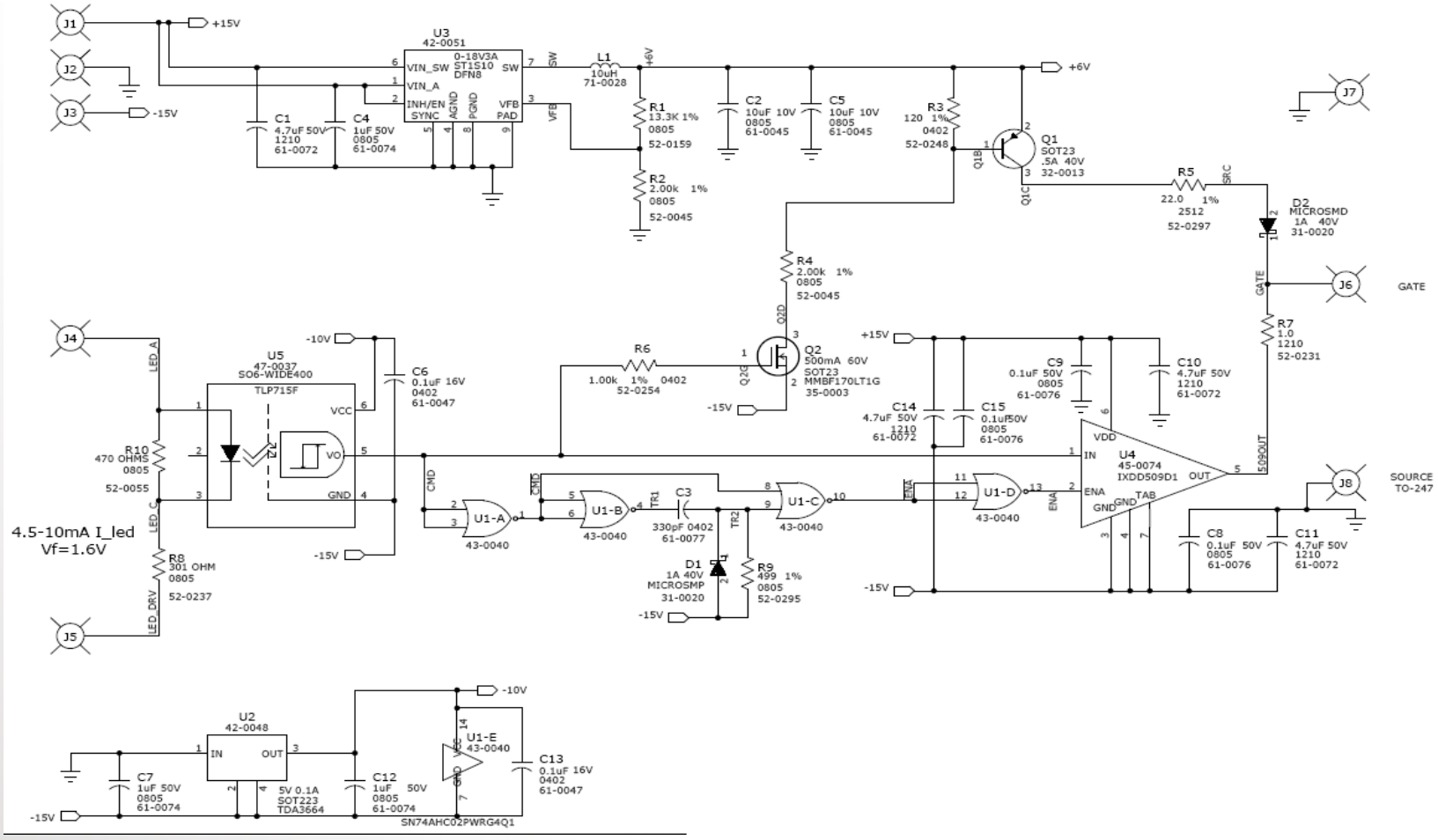
Typical Switching Waveforms for SJEP120R063 JFET





Eon + Eoff = 225 µJ

Detailed Driver Schematic



Comments:

1. A four-layer board is recommended with one layer dedicated to the ground plane to reduce inductance.
2. The bypass capacitors should be placed very close to the IXYS 509 gate driver IC.

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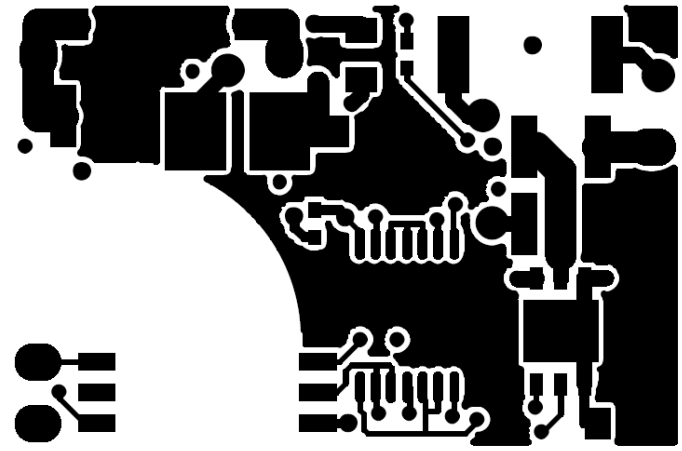
Bill of Materials

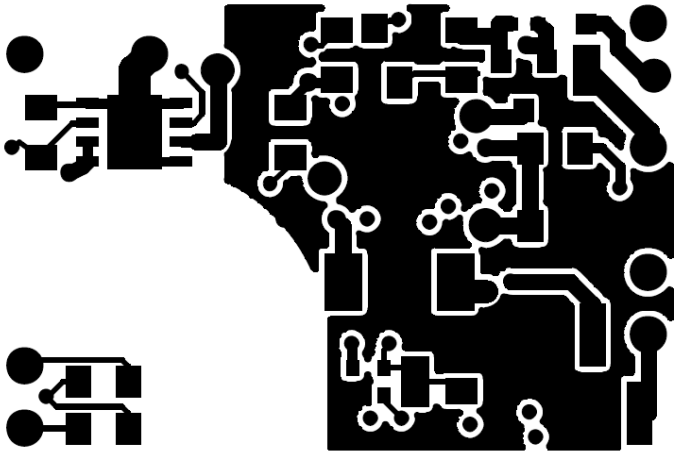
Item	Qty	Reference	Description	Mfr Name	Mfr P/N	Size
1	2	D1, D2	SCKY 40V 1A	VISHAY	MSS1P4-M3/89A	MicroSMP
2	1	Q1	XSTR DUAL PNP 65V 100mA	NXP Semiconductors	PBSS3540E,115	STO363
3	1	Q2	MOSFET N-CH 60V .5A	ON SEMI	MMBF170LT1G	SOT23
4	1	U2	IC REG TDA3664 5.0V	NXP Semiconductors	TDA3664	SOT223
5	1	U3	IC SMPS 3A 18V 900kHz SYNCBUCK	STMicro	ST1S10PUR	SO8
6	1	U1	IC 74AHC02-Q1 QUAD 2-IN NOR	TEXAS INST	SN74AHC02PWRG4Q1	TSSOP14
7	1	U4	IC GATE DRVR 9A IXDD509	IXYS CORP	IXDD509D1	SOIC8
8	1	U5	IC OPTO TLP715F HI-ISO	TOSHIBA	TLP715(F)	6-SDIP
9	2	R2, R4	RES 2.00K 1%	VISHAY	CRCW 0805 2001 FRT1	0805
10	1	R10	RES 470 OHM 5%	VISHAY	CRCW0805470RJNEA	0805
11	1	R1	RES 13.3k 1%	VISHAY	CRCW080513K3FKEA	0805
12	1	R7	RES 1 OHM 5%	PANASONIC	ERJ-P14J1R0U	1210
13	1	R8	RES 301 OHM 1%	VISHAY	CRCW0805301RFKEA	0805
14	1	R3	RES 120 OHM 1%	YAGEO	RC0402FR-07120RL	0402
15	1	R6	RES 1.00k 1%	ROHM	MCR01MZPF1001	0402
16	1	R9	RES 499 1%	ROHM	MCR10EZHF4990	0805
17	1	R5	RES 22 ohm 1%	PANASONIC	ERJ-1TNF22R0U	2512
18	2	C2, C5	CAP 10uF 10V X7R CER	MURATA	GRM21BR71A106KE51L	0805
19	2	C6, C13	CAP 0.1uF 16V X7R CER	MURATA	GRM155R71C104KA88D	0402
20	4	C1, C10, C11, C14	CAP 4.7uF 50V X7R CER 10%	MURATA	GRM32ER71H475KA88L	1210
21	3	C4, C7, C12	CAP 1uF 50V X7R CER 10%	MURATA	GRM21BR71H105KA12L	0805
22	3	C8, C9, C15	CAP 0.1uF 50V X7R CER	PANASONIC	ECJ-2FB1H104K	0805
23	1	C3	CAP 330pF 50V X7R CER	PANASONIC	ECJ-0EB1H331K	0402
24	1	L1	IND 10uH .65A SMT	MURATA	LQH43CN100K03L	1812

PCB Layers

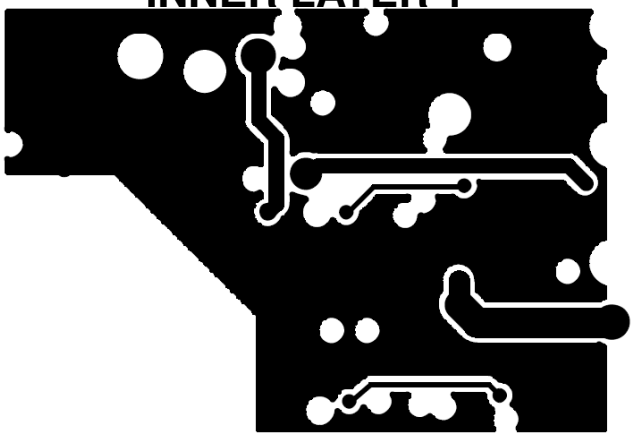
TOP LAYER



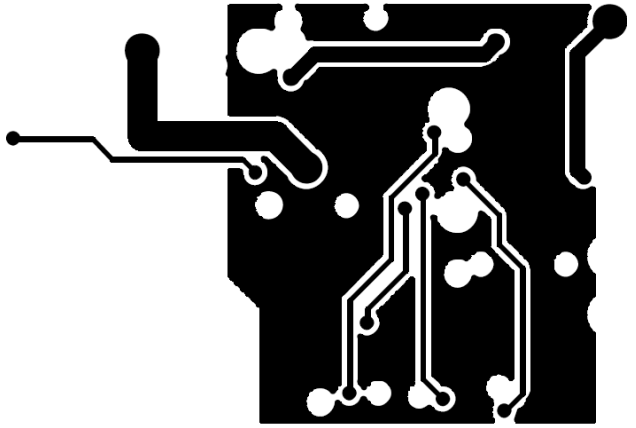
BOTTOM LAYER



INNER LAYER 1



INNER LAYER 2



NOTE: IXDD509 has been discontinued by IXYS and replaced with the IXDD609 sold by Clare Electronics. Clare did not release a replacement in the DFN6 package as used in this design. Gerbers available upon request; however, layout modifications would be necessary to accommodate a new footprint for the Clare replacement part.

Application Recommendations

- **External +15 V and -15 V power supplies** -The required power supplies must be sufficiently isolated from any source voltage that is accessible to human touch. This isolation requirement will depend upon the bus voltage used and the requirements set by the applicable regulatory agency. Here are some additional considerations:
  - ✓ Minimize the lead length between the output of these isolated power supplies and the input to the gate drive circuit
  - ✓ The voltage differential between the +15 V and -15 V must not exceed 30 V in order to protect the driver IC.
  - ✓ The -15 V must be constrained to be between -15V and -8V in order to ensure the 5 V regulator for the logic and opto coupler has enough head room.
  - ✓ If two gate driver circuits are used in a half-bridge configuration, the stray capacitance between the two sets of isolated outputs must be very low (<10 pF). Bench-top power supplies should not be used.
  - ✓ If a switching power supply is used to generate the supplies for both the upper and lower JFETs, the transformer should be segment-wound to minimize the stray capacitance.
- **Adjusting the gate current for $R_{DS(ON)}$ during conduction -** The gate current required by the JFET during its ON state is set by the resistor R5 in the schematic of page 6. In this reference design, the value of R5 was set for a gate current of 140 mA which is the recommendation for the SJEP120R063 and SJEP120R050 JFETs to maintain a low $R_{DS(ON)}$ over temperature while keeping the gate power loss to a reasonably low level. If a different JFET is being used, the value of R5 can be adjusted to reach the desired gate current. The designer should refer to the JFET data sheet for picking the proper gate current.

Application Recommendations

- **EMI issues and adjusting turn-on and turn-off switching speeds -** The turn-on and turn-off speeds are set by R7 in the schematic on page 6, where the default value is for minimum switching energies for the SJEP120R063 and SJEP120R050. If this default switching results in excessive EMI, R7 can be increased from 1 Ω to the 3 - 5 Ω range to slow down the switching speeds.
- **Techniques for reducing gate ringing -** Excessive ringing on the gate voltage waveform can be caused by the leakage inductance in either the main power circuit and/or in the gate circuit itself. Hence, the loop area composed of the JFET + freewheel diode + bus caps must be minimized and the physical distance from the gate driver to the JFET must be minimized. The use of a ferrite bead can also significantly reduce the ringing at the expense of slower turn on.
- **Recommendation for using a snubber across the DC Bus -** Further reductions in ringing can sometimes be achieved by the addition of a low power series R-C snubber circuit, as shown in the test circuit of page 5
- **Eliminating shoot-through in bridge configurations -** In bridge configurations, the act of turning on one of the JFETs often results in the a corresponding miller effect “glitch” on the gate of the other JFET such that it can be transiently turned on, resulting in excessive switching losses in both devices. Due to the very fast switching capability of the JFET, this reference design requires a -15 V power supply to suppress this phenomenon. To add more safety margin, a small (1 – 5 nF) capacitor placed across each JFET’s gate & source can be used.

Application Recommendations

- **Turn on pulse timing circuit and adjustments -** The logic / timing circuit (shown in the block diagram of page 4) generates the required high current pulse with a duration of approx. 100 ns (long enough for the turn-on transient). Changing C7 will adjust the duration of this pulse.

- **Cooling of the driver board -** The heat dissipated by the board will become significant when:
  1. The JFET's duty cycle is closer to 100 %.
  2. The power supplies are at or near their max rated +/- 15 V values.
  3. The PWM frequency is higher than 25 kHz.

  When one or more of the above conditions is met, care must be taken to ensure that none of the components on the PCB have surface temperatures in excess of 100 ^{o}C. Options to improve cooling include reducing the ambient temperature in the vicinity of the driver board, increasing airflow, and sinking some of the heat from the board by soldering the board's mounting pins to a suitable copper plane of another PCB.

- **Other layout recommendations -** Because of the relatively high amplitude gate currents involved, it is essential that the decoupling capacitors around the gate driver IC be in very close proximity to it. A 4 layer board is recommended where one layer is dedicated to the 0 volt ground plane. The gate driver IC and related gate resistors should be located to within 1 cm of the JFET gate and source pins. For the opto coupler, proper layout line spacing should be followed according to the specific regulatory agency and certification for safety isolation strike and creep.

- Additional information on the JFET and recommendations are in available in the SemiSouth White Paper WP-SS2 and “how to use” Applications Note AN-SS1 which can be found on the SemiSouth web site

Modification Instructions

Since the gate driver requirements of both the enhancement-mode and depletion-mode devices are similar, the SGDR600P1 can also be modified to drive the SJEP120R100, SJDP120R085, and the SJDP120R045. The modification for the depletion-mode devices included in this document will only allow for driving the gate at V_{GS} = 0V during the conduction phase. A V_{GS} = +2 V drive option is not yet available as a modification to the existing SGDR600P1. Below is a summary of the required modifications necessary for driving other enhancement-mode and depletion-mode devices using the SGDR600P1 demoboard.

Required modification for driving other enhancement-mode SiC JFETs:

1. Value change of resistor R5 to adjust the on-state gate current.
2. Value change of resistor R7 to optimally dampen any feedback of power circuit oscillations. This resistor also adjusts the turn-on and turn-off speeds.

Required modification for driving depletion-mode SiC JFETs:

1. Removal of resistor R5 to disconnect the second driver stage as on-state current is unnecessary during conduction.
2. Value change of resistor R7 to optimally dampen any feedback of power circuit oscillations. This resistor also adjusts the turn-on and turn-off speeds.
3. Addition of a pull-down resistor connected across the gate and source output pins of the PCB such that the gate will be held at V_{GS} = 0 V during the conduction period.
4. The +15 V supply can be decreased to +10 V if desired.

Modifications for Driving SJEP120R100

BOM Change

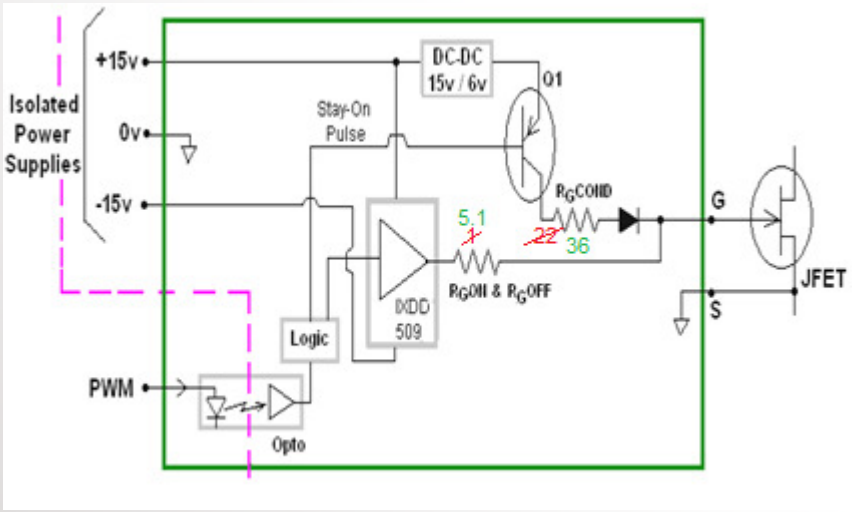
2	12	1	R7	RES 1 OHM 5%	PANASONIC	ERJ-P14J1R0U	1210
	13	1	R8	RES 301 OHM 1%	VISHAY	CRCW0805301RFKEA	0805
	14	1	R3	RES 120 OHM 1%	YAGEO	RC0402FR-07120RL	0402
	15	1	R6	RES 1.00k 1%	ROHM	MCR01MZPF1001	0402
	16	1	R9	RES 499 1%	ROHM	MCR10EZHF4990	0805
1	17	1	R5	RES 22 ohm 1%	PANASONIC	ERJ-1TNF22R0U	2512

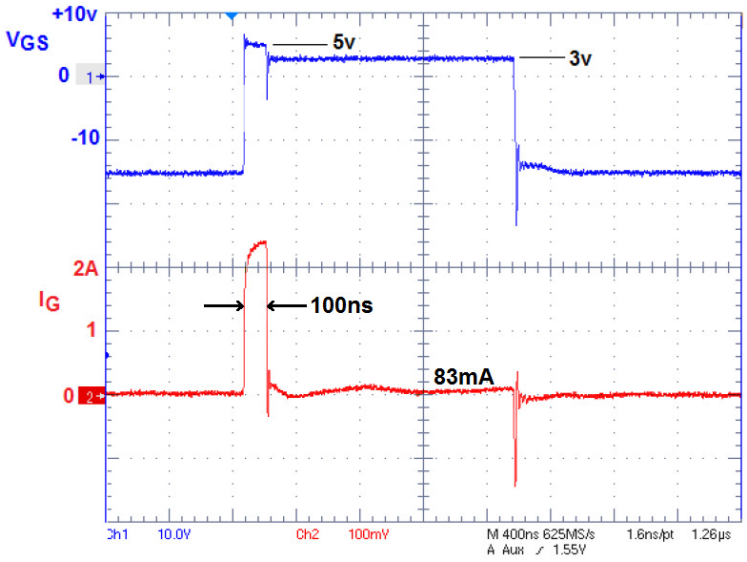
RES 5.1 OHM 5%

RES 36 OHM 1%

ERJ-P14J5R1U

ERJ-1TNF36R0U





Modifications for Driving SJDP120R085

BOM Change

2

12	1	R7	RES 1 OHM 5%	PANASONIC	ERJ-P14J1R0U	1210
13	1	R8	RES 301 OHM 1%	VISHAY	CRCW0805301RFKEA	0805
14	1	R3	RES 120 OHM 1%	YAGEO	RC0402FR-07120RL	0402
15	1	R6	RES 1.00k 1%	ROHM	MCR01MZPF1001	0402
16	1	R9	RES 499 1%	ROHM	MCR10EZHF4990	0805
17	1	R5	RES 22 ohm 1%	PANASONIC	ERJ-1TNF22R0U	2512
18	2	C2, C5	CAP 10uF 10V X7R CER	MURATA	GRM21BR71A106KE51L	0805

1

REMOVE

RES 5.1 OHM 5%

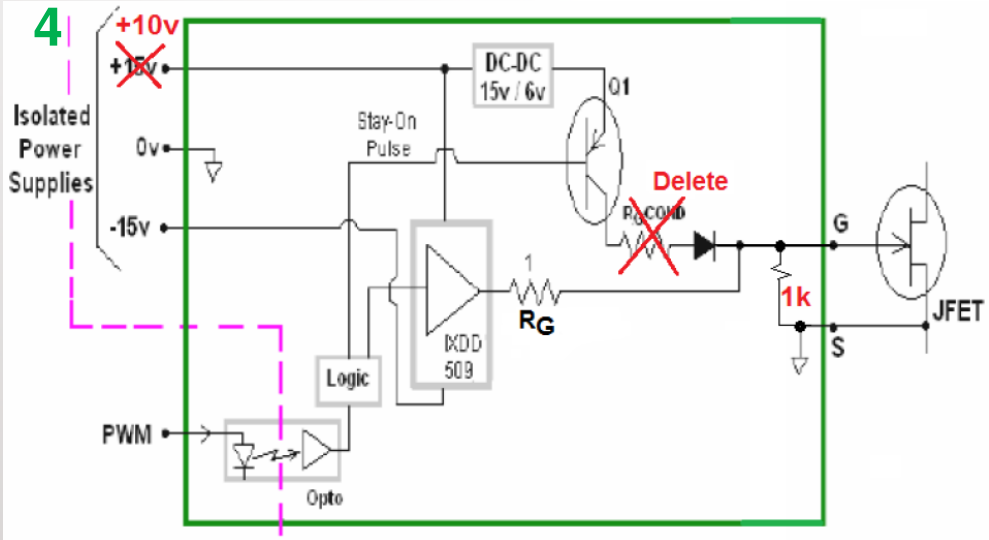
ERJ-P14J5R1U

ADD

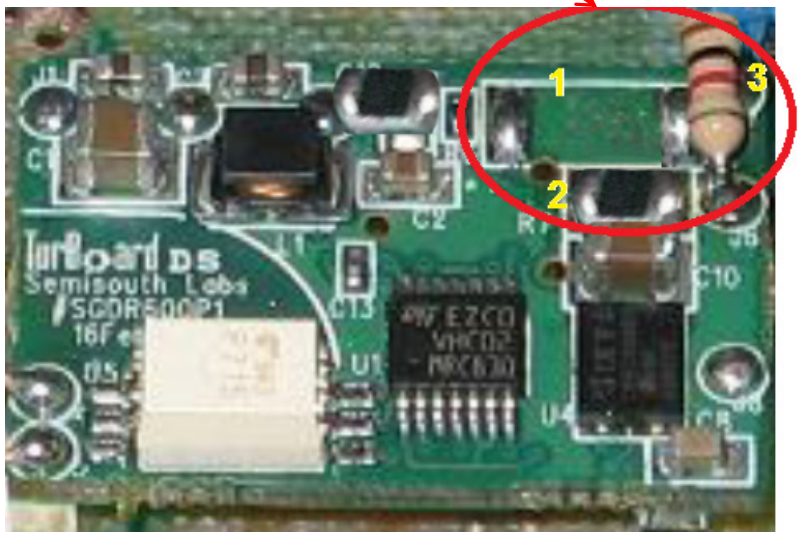
3

Item	Qty	Reference	Description
22	1	R11	RES 1K OHM 5%

4



Modifications numbered to the left



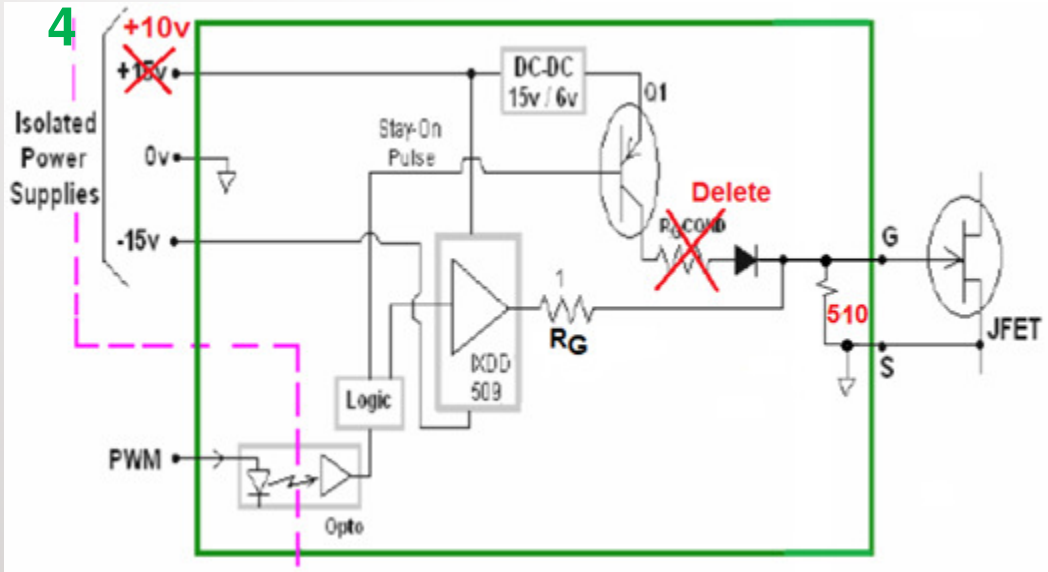
Modifications for Driving SJDP120R045

BOM Change

16	1	R9	RES 499 1%		ROHM	MCR10EZHF4990	0805
1	17	1	R5	RES 22 ohm 1%	REMOVE	PANASONIC	ERJ-1TNF22R0U	2512
	18	2	C2, C5	CAP 10uF 10V X7R CER		MURATA	GRM21BR71A106KE51L	0805

ADD

3	Item	Qty	Reference	Description
	22	1	R11	RES 510 OHM 5%



Modifications numbered to the left