Atmel AT45DB161E

16-Mbit DataFlash (with Extra 512-Kbits), 2.3V or 2.5V Minimum SPI Serial Flash Memory

DATASHEET

Features

- Single 2.3V - 3.6V or 2.5V - 3.6V supply
- Serial Peripheral Interface (SPI) compatible
  - Supports SPI modes 0 and 3
  - Supports Atmel® RapidS™ operation
- Continuous read capability through entire array
  - Up to 85MHz
  - Low-power read option up to 10MHz
  - Clock-to-output time (t_V) of 6ns maximum
- User configurable page size
  - 512 bytes per page
  - 528 bytes per page (default)
  - Page size can be factory pre-configured for 512 bytes
- Two fully independent SRAM data buffers (512/528 bytes)
  - Allows receiving data while reprogramming the main memory array
- Flexible programming options
  - Byte/Page Program (1 to 512/528 bytes) directly into main memory
  - Buffer Write
  - Buffer to Main Memory Page Program
- Flexible erase options
  - Page Erase (512/528 bytes)
  - Block Erase (4KB)
  - Sector Erase (128KB)
  - Chip Erase (16-Mbits)
- Program and Erase Suspend/Resume
- Advanced hardware and software data protection features
  - Individual sector protection
  - Individual sector lockdown to make any sector permanently read-only
- 128-byte, One-Time Programmable (OTP) Security Register
  - 64 bytes factory programmed with a unique identifier
  - 64 bytes user programmable
- Hardware and software controlled reset options
- JEDEC Standard Manufacturer and Device ID Read
- Low-power dissipation
  - 500nA Ultra-Deep Power-Down current (typical)
  - 3µA Deep Power-Down current (typical)
  - 25µA Standby current (typical at 20MHz)
  - 11mA Active Read current (typical)
- Endurance: 100,000 program/erase cycles per page minimum
- Data retention: 20 years
- Complies with full industrial temperature range
- Green (Pb/Halide-free/RoHS compliant) packaging options
  - 8-lead SOIC (0.150" wide and 0.208" wide)
  - 8-pad Ultra-thin DFN (5 x 6 x 0.6mm)
  - 9-ball Ultra-thin UBGA (6 x 6 x 0.6mm)

Description

The Atmel AT45DB161E is a 2.3V or 2.5V minimum, serial-interface sequential access Flash memory ideally suited for a wide variety of digital voice, image, program code, and data storage applications. The AT45DB161E also supports the RapidS serial interface for applications requiring very high speed operation. Its 17,301,504 bits of memory are organized as 4,096 pages of 512 bytes or 528 bytes each. In addition to the main memory, the AT45DB161E also contains two SRAM buffers of 512/528 bytes each. The buffers allow receiving of data while a page in the main memory is being reprogrammed. Interleaving between both buffers can dramatically increase a system's ability to write a continuous data stream. In addition, the SRAM buffers can be used as additional system scratch pad memory, and E^{2}PROM emulation (bit or byte alterability) can be easily handled with a self-contained three step read-modify-write operation.

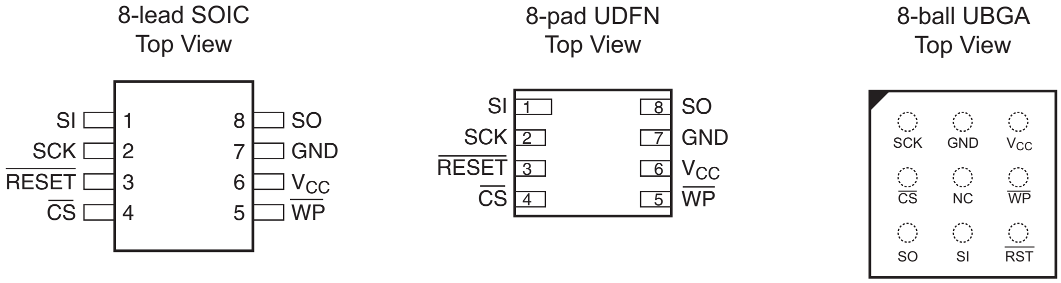
Unlike conventional Flash memories that are accessed randomly with multiple address lines and a parallel interface, the Atmel DataFlash® uses a serial interface to sequentially access its data. The simple sequential access dramatically reduces active pin count, facilitates simplified hardware layout, increases system reliability, minimizes switching noise, and reduces package size. The device is optimized for use in many commercial and industrial applications where high-density, low-pin count, low-voltage, and low-power are essential.

To allow for simple in-system re-programmability, the AT45DB161E does not require high input voltages for programming. The device operates from a single 2.3V to 3.6V or 2.5V to 3.6V power supply for the erase and program and read operations. The AT45DB161E is enabled through the Chip Select pin ($\overline{\text{CS}}$) and accessed via a 3-wire interface consisting of the Serial Input (SI), Serial Output (SO), and the Serial Clock (SCK).

All programming and erase cycles are self-timed.

1. Pin Configurations and Pinouts

Figure 1-1. Pinouts



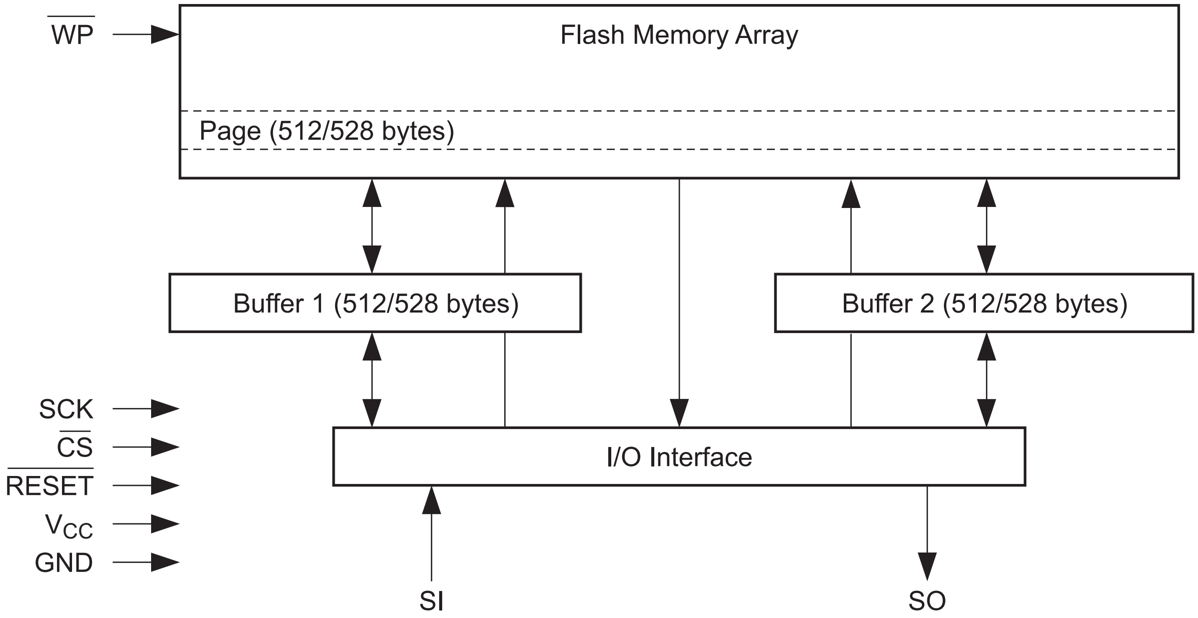
Note: 1. The metal pad on the bottom of the UDFN package is not internally connected to a voltage potential. This pad can be a "no connect" or connected to GND.

Table 1-1. Pin Configurations

Symbol	Name and Function	Asserted State	Type
$\overline{\text{CS}}$	**Chip Select:** Asserting the $\overline{\text{CS}}$ pin selects the device. When the $\overline{\text{CS}}$ pin is deasserted, the device will be deselected and normally be placed in the standby mode (not Deep Power-Down mode) and the output pin (SO) will be in a high-impedance state. When the device is deselected, data will not be accepted on the input pin (SI). A high-to-low transition on the $\overline{\text{CS}}$ pin is required to start an operation and a low-to-high transition is required to end an operation. When ending an internally self-timed operation such as a program or erase cycle, the device will not enter the standby mode until the completion of the operation.	Low	Input
SCK	**Serial Clock:** This pin is used to provide a clock to the device and is used to control the flow of data to and from the device. Command, address, and input data present on the SI pin is always latched on the rising edge of SCK, while output data on the SO pin is always clocked out on the falling edge of SCK.	—	Input
SI	**Serial Input:** The SI pin is used to shift data into the device. The SI pin is used for all data input including command and address sequences. Data on the SI pin is always latched on the rising edge of SCK. Data present on the SI pin will be ignored whenever the device is deselected ($\overline{\text{CS}}$ is deasserted).	—	Input
SO	**Serial Output:** The SO pin is used to shift data out from the device. Data on the SO pin is always clocked out on the falling edge of SCK. The SO pin will be in a high-impedance state whenever the device is deselected ($\overline{\text{CS}}$ is deasserted).	—	Output
$\overline{\text{WP}}$	**Write Protect:** When the $\overline{\text{WP}}$ pin is asserted, all sectors specified for protection by the Sector Protection Register will be protected against program and erase operations regardless of whether the Enable Sector Protection command has been issued or not. The $\overline{\text{WP}}$ pin functions independently of the software controlled protection method. After the $\overline{\text{WP}}$ pin goes low, the contents of the Sector Protection Register cannot be modified. If a program or erase command is issued to the device while the $\overline{\text{WP}}$ pin is asserted, the device will simply ignore the command and perform no operation. The device will return to the idle state once the $\overline{\text{CS}}$ pin has been deasserted. The Enable Sector Protection command and the Sector Lockdown command, however, will be recognized by the device when the $\overline{\text{WP}}$ pin is asserted. The $\overline{\text{WP}}$ pin is internally pulled-high and may be left floating if hardware controlled protection will not be used. However, it is recommended that the $\overline{\text{WP}}$ pin also be externally connected to V_{CC} whenever possible.	Low	Input
$\overline{\text{RESET}}$	**Reset:** A low state on the reset pin ($\overline{\text{RESET}}$) will terminate the operation in progress and reset the internal state machine to an idle state. The device will remain in the reset condition as long as a low level is present on the $\overline{\text{RESET}}$ pin. Normal operation can resume once the $\overline{\text{RESET}}$ pin is brought back to a high level. The device incorporates an internal power-on reset circuit, so there are no restrictions on the $\overline{\text{RESET}}$ pin during power-on sequences. If this pin and feature is not utilized, then it is recommended that the $\overline{\text{RESET}}$ pin be driven high externally.	Low	Input
V_{CC}	**Device Power Supply:** The V_{CC} pin is used to supply the source voltage to the device. Operations at invalid V_{CC} voltages may produce spurious results and should not be attempted.	—	Power
GND	**Ground:** The ground reference for the power supply. GND should be connected to the system ground.	—	Ground

2. Block Diagram

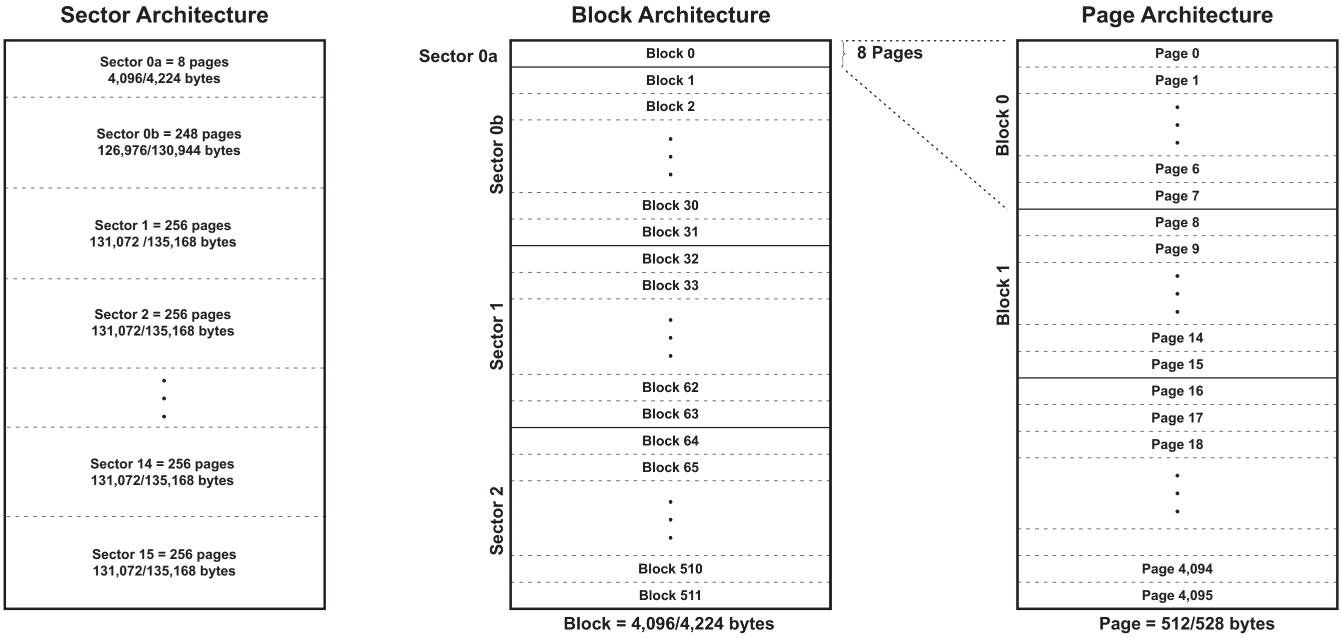
Figure 2-1. Block Diagram



3. Memory Array

To provide optimal flexibility, the AT45DB161E memory array is divided into three levels of granularity comprising of sectors, blocks, and pages. Figure 3-1, Memory Architecture Diagram illustrates the breakdown of each level and details the number of pages per sector and block. Program operations to the DataFlash can be done at the full page level or at the byte level (a variable number of bytes). The erase operations can be performed at the chip, sector, block, or page level.

Figure 3-1. Memory Architecture Diagram



4. Device Operation

The device operation is controlled by instructions from the host processor. The list of instructions and their associated opcodes are contained in Table 15-1 on page 40 through Table 15-4 on page 41. A valid instruction starts with the falling edge of $\overline{CS}$ followed by the appropriate 8-bit opcode and the desired buffer or main memory address location. While the $\overline{CS}$ pin is low, toggling the SCK pin controls the loading of the opcode and the desired buffer or main memory address location through the SI (Serial Input) pin. All instructions, addresses, and data are transferred with the Most Significant Bit (MSB) first.

Three address bytes are used to address memory locations in either the main memory array or in one of the SRAM buffers. The three address bytes will be comprised of a number of dummy bits and a number of actual device address bits, with the number of dummy bits varying depending on the operation being performed and the selected device page size. Buffer addressing for the standard DataFlash page size (528 bytes) is referenced in the datasheet using the terminology BFA9 - BFA0 to denote the 10 address bits required to designate a byte address within a buffer. The main memory addressing is referenced using the terminology PA11 - PA0 and BA9 - BA0, where PA11 - PA0 denotes the 12 address bits required to designate a page address, and BA9 - BA0 denotes the 10 address bits required to designate a byte address within the page. Therefore, when using the standard DataFlash page size, a total of 22 address bits are used.

For the “power of 2” binary page size (512 bytes), the buffer addressing is referenced in the datasheet using the conventional terminology BFA8 - BFA0 to denote the nine address bits required to designate a byte address within a buffer. Main memory addressing is referenced using the terminology A20 - A0, where A20 - A9 denotes the 12 address bits required to designate a page address, and A8 - A0 denotes the nine address bits required to designate a byte address within a page. Therefore, when using the binary page size, a total of 21 address bits are used.

5. Read Commands

By specifying the appropriate opcode, data can be read from the main memory or from either one of the two SRAM data buffers. The DataFlash supports RapidS protocols for Mode 0 and Mode 3. Please see Section 25., Detailed Bit-level Read Waveforms: Atmel RapidS Mode 0/Mode 3 diagrams in this datasheet for details on the clock cycle sequences for each mode.

5.1 Continuous Array Read (Legacy Command: E8h Opcode)

By supplying an initial starting address for the main memory array, the Continuous Array Read command can be utilized to sequentially read a continuous stream of data from the device by simply providing a clock signal; no additional addressing information or control signals need to be provided. The DataFlash incorporates an internal address counter that will automatically increment on every clock cycle, allowing one continuous read from memory to be performed without the need for additional address sequences. To perform a Continuous Array Read using the standard DataFlash page size (528 bytes), an opcode of E8h must be clocked into the device followed by three address bytes (which comprise the 22-bit page and byte address sequence) and four dummy bytes. The first 12 bits (PA11 - PA0) of the 22-bit address sequence specify which page of the main memory array to read and the last 10 bits (BA9 - BA0) of the 22-bit address sequence specify the starting byte address within the page. To perform a Continuous Array Read using the binary page size (512 bytes), an opcode of E8h must be clocked into the device followed by three address bytes and four dummy bytes. The first 12 bits (A20 - A9) of the 21-bit address sequence specify which page of the main memory array to read and the last nine bits (A8 - A0) of the 21-bit address sequence specify the starting byte address within the page. The dummy bytes that follow the address bytes are needed to initialize the read operation. Following the dummy bytes, additional clock pulses on the SCK pin will result in data being output on the SO (serial output) pin.

The $\overline{CS}$ pin must remain low during the loading of the opcode, the address bytes, the dummy bytes, and the reading of data. When the end of a page in the main memory is reached during a Continuous Array Read, the device will continue reading at the beginning of the next page with no delays incurred during the page boundary crossover (the crossover from the end of one page to the beginning of the next page). When the last bit in the main memory array has been read, the device will continue reading back at the beginning of the first page of memory. As with crossing over page boundaries, no delays will be incurred when wrapping around from the end of the array to the beginning of the array.

A low-to-high transition on the $\overline{CS}$ pin will terminate the read operation and tri-state the output pin (SO). The maximum SCK frequency allowable for the Continuous Array Read is defined by the f_{CAR1} specification. The Continuous Array Read bypasses the data buffers and leaves the contents of the buffers unchanged.

Warning: This command is not recommended for new designs.

5.2 Continuous Array Read (High Frequency Mode: 1Bh Opcode)

This command can be used to read the main memory array sequentially at the highest possible operating clock frequency up to the maximum specified by f_{CAR1}. To perform a Continuous Array Read using the standard DataFlash page size (528 bytes), the $\overline{CS}$ pin must first be asserted, and then an opcode of 1Bh must be clocked into the device followed by three address bytes and two dummy bytes. The first 12 bits (PA11 - PA0) of the 22-bit address sequence specify which page of the main memory array to read and the last 10 bits (BA9 - BA0) of the 22-bit address sequence specify the starting byte address within the page. To perform a Continuous Array Read using the binary page size (512 bytes), the opcode 1Bh must be clocked into the device followed by three address bytes (A20 - A0) and two dummy bytes. Following the dummy bytes, additional clock pulses on the SCK pin will result in data being output on the SO (Serial Output) pin.

The $\overline{CS}$ pin must remain low during the loading of the opcode, the address bytes, the dummy bytes, and the reading of data. When the end of a page in the main memory is reached during a Continuous Array Read, the device will continue reading at the beginning of the next page with no delays incurred during the page boundary crossover (the crossover from the end of one page to the beginning of the next page). When the last bit in the main memory array has been read, the device will continue reading back at the beginning of the first page of memory. As with crossing over page boundaries, no delays will be incurred when wrapping around from the end of the array to the beginning of the array.

A low-to-high transition on the $\overline{CS}$ pin will terminate the read operation and tri-state the output pin (SO). The maximum SCK frequency allowable for the Continuous Array Read is defined by the f_{CAR1} specification. The Continuous Array Read bypasses both data buffers and leaves the contents of the buffers unchanged.

5.3 Continuous Array Read (High Frequency Mode: 0Bh Opcode)

This command can be used to read the main memory array sequentially at higher clock frequencies up to the maximum specified by f_{CAR1}. To perform a Continuous Array Read using the standard DataFlash page size (528 bytes), the $\overline{CS}$ pin must first be asserted, and then an opcode of 0Bh must be clocked into the device followed by three address bytes and one dummy byte. The first 12 bits (PA11 - PA0) of the 22-bit address sequence specify which page of the main memory array to read and the last 10 bits (BA9 - BA0) of the 22-bit address sequence specify the starting byte address within the page. To perform a Continuous Array Read using the binary page size (512 bytes), the opcode 0Bh must be clocked into the device followed by three address bytes (A20 - A0) and one dummy byte. Following the dummy byte, additional clock pulses on the SCK pin will result in data being output on the SO pin.

The $\overline{CS}$ pin must remain low during the loading of the opcode, the address bytes, the dummy byte, and the reading of data. When the end of a page in the main memory is reached during a Continuous Array Read, the device will continue reading at the beginning of the next page with no delays incurred during the page boundary crossover (the crossover from the end of one page to the beginning of the next page). When the last bit in the main memory array has been read, the device will continue reading back at the beginning of the first page of memory. As with crossing over page boundaries, no delays will be incurred when wrapping around from the end of the array to the beginning of the array.

A low-to-high transition on the $\overline{CS}$ pin will terminate the read operation and tri-state the output pin (SO). The maximum SCK frequency allowable for the Continuous Array Read is defined by the f_{CAR1} specification. The Continuous Array Read bypasses both data buffers and leaves the contents of the buffers unchanged.

5.4 Continuous Array Read (Low Frequency Mode: 03h Opcode)

This command can be used to read the main memory array sequentially at lower clock frequencies up to maximum specified by f_{CAR2}. Unlike the previously described read commands, this Continuous Array Read command for the lower clock frequencies does not require the clocking in of dummy bytes after the address byte sequence. To perform a Continuous Array Read using the standard DataFlash page size (528 bytes), the $\overline{CS}$ pin must first be asserted, and then an opcode of 03h must be clocked into the device followed by three address bytes. The first 12 bits (PA11 - PA0) of the 22-bit address sequence specify which page of the main memory array to read and the last 10 bits (BA9 - BA0) of the 22-bit address sequence specify the starting byte address within the page. To perform a Continuous Array Read using the binary page size (512 bytes), the opcode 03h must be clocked into the device followed by three address bytes (A20 - A0). Following the address bytes, additional clock pulses on the SCK pin will result in data being output on the SO pin.

The $\overline{CS}$ pin must remain low during the loading of the opcode, the address bytes, and the reading of data. When the end of a page in the main memory is reached during a Continuous Array Read, the device will continue reading at the beginning of the next page with no delays incurred during the page boundary crossover (the crossover from the end of one page to the beginning of the next page). When the last bit in the main memory array has been read, the device will continue reading back at the beginning of the first page of memory. As with crossing over page boundaries, no delays will be incurred when wrapping around from the end of the array to the beginning of the array.

A low-to-high transition on the $\overline{CS}$ pin will terminate the read operation and tri-state the output pin (SO). The maximum SCK frequency allowable for the Continuous Array Read is defined by the f_{CAR2} specification. The Continuous Array Read bypasses both data buffers and leaves the contents of the buffers unchanged.

5.5 Continuous Array Read (Low Power Mode: 01h Opcode)

This command is ideal for applications that want to minimize power consumption and do not need to read the memory array at high frequencies. Like the 03h opcode, this Continuous Array Read command allows reading the main memory array sequentially without the need for dummy bytes to be clocked in after the address byte sequence. The memory can be read at clock frequencies up to maximum specified by f_{CAR3}. To perform a Continuous Array Read using the standard DataFlash page size (528 bytes), the $\overline{CS}$ pin must first be asserted, and then an opcode of 01h must be clocked into the device followed by three address bytes. The first 12 bits (PA11 - PA0) of the 22-bit address sequence specify which page of the main memory array to read and the last 10 bits (BA9 - BA0) of the 22-bit address sequence specify the starting byte address within the page. To perform a Continuous Array Read using the binary page size (512 bytes), the opcode 01h must be clocked into the device followed by three address bytes (A20 - A0). Following the address bytes, additional clock pulses on the SCK pin will result in data being output on the SO pin.

The $\overline{CS}$ pin must remain low during the loading of the opcode, the address bytes, and the reading of data. When the end of a page in the main memory is reached during a Continuous Array Read, the device will continue reading at the beginning of the next page with no delays incurred during the page boundary crossover (the crossover from the end of one page to the beginning of the next page). When the last bit in the main memory array has been read, the device will continue reading back at the beginning of the first page of memory. As with crossing over page boundaries, no delays will be incurred when wrapping around from the end of the array to the beginning of the array.

A low-to-high transition on the $\overline{CS}$ pin will terminate the read operation and tri-state the output pin (SO). The maximum SCK frequency allowable for the Continuous Array Read is defined by the f_{CAR3} specification. The Continuous Array Read bypasses both data buffers and leaves the contents of the buffers unchanged.

5.6 Main Memory Page Read

A Main Memory Page Read allows the reading of data directly from a single page in the main memory, bypassing both of the data buffers and leaving the contents of the buffers unchanged. To start a page read using the standard DataFlash page size (528 bytes), an opcode of D2h must be clocked into the device followed by three address bytes (which comprise the 22-bit page and byte address sequence) and four dummy bytes. The first 12 bits (PA11 - PA0) of the 22-bit address sequence specify the page in main memory to be read and the last 10 bits (BA9 - BA0) of the 22-bit address sequence specify the starting byte address within that page. To start a page read using the binary page size (512 bytes), the opcode D2h must be clocked into the device followed by three address bytes and four dummy bytes. The first 12 bits (A20 - A9) of the 21-bit address sequence specify which page of the main memory array to read, and the last nine bits (A8 - A0) of the 21-bit address sequence specify the starting byte address within that page. The dummy bytes that follow the address bytes are sent to initialize the read operation. Following the dummy bytes, the additional pulses on SCK result in data being output on the SO (serial output) pin.

The $\overline{CS}$ pin must remain low during the loading of the opcode, the address bytes, the dummy bytes, and the reading of data. Unlike the Continuous Array Read command, when the end of a page in main memory is reached, the device will continue reading back at the beginning of the same page rather than the beginning of the next page.

A low-to-high transition on the $\overline{CS}$ pin will terminate the read operation and tri-state the output pin (SO). The maximum SCK frequency allowable for the Main Memory Page Read is defined by the f_{SCK} specification. The Main Memory Page Read bypasses both data buffers and leaves the contents of the buffers unchanged.

5.7 Buffer Read

The SRAM data buffers can be accessed independently from the main memory array, and utilizing the Buffer Read command allows data to be sequentially read directly from either one of the buffers. Four opcodes, D4h or D1h for Buffer 1 and D6h or D3h for Buffer 2, can be used for the Buffer Read command. The use of each opcode depends on the maximum SCK frequency that will be used to read data from the buffers. The D4h and D6h opcode can be used at any SCK frequency up to the maximum specified by f_{CAR1} while the D1h and D3h opcode can be used for lower frequency read operations up to the maximum specified by f_{CAR2}.

To perform a Buffer Read using the standard DataFlash buffer size (528 bytes), the opcode must be clocked into the device followed by three address bytes comprised of 14 dummy bits and 10 buffer address bits (BFA9 - BFA0). To perform a Buffer Read using the binary buffer size (512 bytes), the opcode must be clocked into the device followed by three address bytes comprised of 15 dummy bits and nine buffer address bits (BFA8 - BFA0). Following the address bytes, one dummy byte must be clocked into the device to initialize the read operation if using opcodes D4h or D6h. The $\overline{CS}$ pin must remain low during the loading of the opcode, the address bytes, the dummy byte (if using opcodes D4h or D6h), and the reading of data. When the end of a buffer is reached, the device will continue reading back at the beginning of the buffer. A low-to-high transition on the $\overline{CS}$ pin will terminate the read operation and tri-state the output pin (SO).

6. Program and Erase Commands

6.1 Buffer Write

Utilizing the Buffer Write command allows data clocked in from the SI pin to be written directly into either one of the SRAM data buffers.

To load data into a buffer using the standard DataFlash buffer size (528 bytes), an opcode of 84h for Buffer 1 or 87h for Buffer 2 must be clocked into the device followed by three address bytes comprised of 14 dummy bits and 10 buffer address bits (BFA9 - BFA0). The 10 buffer address bits specify the first byte in the buffer to be written.

To load data into a buffer using the binary buffer size (512 bytes), an opcode of 84h for Buffer 1 or 87h for Buffer 2, must be clocked into the device followed by 15 dummy bits and nine buffer address bits (BFA8 - BFA0). The nine buffer address bits specify the first byte in the buffer to be written.

After the last address byte has been clocked into the device, data can then be clocked in on subsequent clock cycles. If the end of the data buffer is reached, the device will wrap around back to the beginning of the buffer. Data will continue to be loaded into the buffer until a low-to-high transition is detected on the $\overline{\text{CS}}$ pin.

6.2 Buffer to Main Memory Page Program with Built-In Erase

The Buffer to Main Memory Page Program with Built-In Erase command allows data that is stored in one of the SRAM buffers to be written into an erased or programmed page in the main memory array. It is not necessary to pre-erase the page in main memory to be written because this command will automatically erase the selected page prior to the program cycle.

To perform a Buffer to Main Memory Page Program with Built-In Erase using the standard DataFlash page size (528 bytes), an opcode of 83h for Buffer 1 or 86h for Buffer 2 must be clocked into the device followed by three address bytes comprised of two dummy bits, 12 page address bits (PA11 - PA0) that specify the page in the main memory to be written, and 10 dummy bits.

To perform a Buffer to Main Memory Page Program with Built-In Erase using the binary page size (512 bytes), an opcode of 83h for Buffer 1 or 86h for Buffer 2 must be clocked into the device followed by three address bytes comprised of three dummy bits, 12 page address bits (A20 - A9) that specify the page in the main memory to be written, and nine dummy bits.

When a low-to-high transition occurs on the $\overline{\text{CS}}$ pin, the device will first erase the selected page in main memory (the erased state is a Logic 1) and then program the data stored in the appropriate buffer into that same page in main memory. Both the erasing and the programming of the page are internally self-timed and should take place in a maximum time of t_{EP}. During this time, the RDY/$\overline{\text{BUSY}}$ bit in the Status Register will indicate that the device is busy.

The device also incorporates an intelligent erase and program algorithm that can detect when a byte location fails to erase or program properly. If an erase or programming error arises, it will be indicated by the EPE bit in the Status Register.

6.3 Buffer to Main Memory Page Program without Built-In Erase

The Buffer to Main Memory Page Program without Built-In Erase command allows data that is stored in one of the SRAM buffers to be written into a pre-erased page in the main memory array. It is necessary that the page in main memory to be written be previously erased in order to avoid programming errors.

To perform a Buffer to Main Memory Page Program without Built-In Erase using the standard DataFlash page size (528 bytes), an opcode of 88h for Buffer 1 or 89h for Buffer 2 must be clocked into the device followed by three address bytes comprised of two dummy bits, 12 page address bits (PA11 - PA0) that specify the page in the main memory to be written, and 10 dummy bits.

To perform a Buffer to Main Memory Page Program using the binary page size (512 bytes), an opcode of 88h for Buffer 1 or 89h for Buffer 2 must be clocked into the device followed by three address bytes comprised of three dummy bits, 12 page address bits (A20 - A9) that specify the page in the main memory to be written, and nine dummy bits.

When a low-to-high transition occurs on the $\overline{\text{CS}}$ pin, the device will program the data stored in the appropriate buffer into the specified page in the main memory. The page in main memory that is being programmed must have been previously erased using one of the erase commands (Page Erase, Block Erase, Sector Erase, or Chip Erase). The programming of the page is internally self-timed and should take place in a maximum time of t_P. During this time, the RDY/$\overline{\text{BUSY}}$ bit in the Status Register will indicate that the device is busy.

The device also incorporates an intelligent programming algorithm that can detect when a byte location fails to program properly. If a programming error arises, it will be indicated by the EPE bit in the Status Register.

6.4 Main Memory Page Program through Buffer with Built-In Erase

The Main Memory Page Program through Buffer with Built-In Erase command combines the Buffer Write and Buffer to Main Memory Page Program with Built-In Erase operations into a single operation to help simplify application firmware development. With the Main Memory Page Program through Buffer with Built-In Erase command, data is first clocked into either Buffer 1 or Buffer 2, the addressed page in memory is then automatically erased, and then the contents of the appropriate buffer are programmed into the just-erased main memory page.

To perform a Main Memory Page Program through Buffer using the standard DataFlash page size (528 bytes), an opcode of 82h for Buffer 1 or 85h for Buffer 2 must first be clocked into the device followed by three address bytes comprised of two dummy bits, 12 page address bits (PA11 - PA0) that specify the page in the main memory to be written, and 10 buffer address bits (BFA9 - BFA0) that select the first byte in the buffer to be written.

To perform a Main Memory Page Program through Buffer using the binary page size (512 bytes), an opcode of 82h for Buffer 1 or 85h for Buffer 2 must first be clocked into the device followed by three address bytes comprised of three dummy bits, 12 page address bits (A20 - A9) that specify the page in the main memory to be written, and nine buffer address bits (BFA8 - BFA0) that select the first byte in the buffer to be written.

After all address bytes have been clocked in, the device will take data from the input pin (SI) and store it in the specified data buffer. If the end of the buffer is reached, the device will wrap around back to the beginning of the buffer. When there is a low-to-high transition on the $\overline{\text{CS}}$ pin, the device will first erase the selected page in main memory (the erased state is a Logic 1) and then program the data stored in the buffer into that main memory page. Both the erasing and the programming of the page are internally self-timed and should take place in a maximum time of t_{EP}. During this time, the RDY/$\overline{\text{BUSY}}$ bit in the Status Register will indicate that the device is busy.

The device also incorporates an intelligent erase and programming algorithm that can detect when a byte location fails to erase or program properly. If an erase or program error arises, it will be indicated by the EPE bit in the Status Register.

6.5 Main Memory Byte/Page Program through Buffer 1 without Built-In Erase

The Main Memory Byte/Page Program through Buffer 1 without Built-In Erase command combines both the Buffer Write and Buffer to Main Memory Program without Built-In Erase operations to allow any number of bytes (1 to 512/528 bytes) to be programmed directly into previously erased locations in the main memory array. With the Main Memory Byte/Page Program through Buffer 1 without Built-In Erase command, data is first clocked into Buffer 1, and then only the bytes clocked into the buffer are programmed into the pre-erased byte locations in main memory. Multiple bytes up to the page size can be entered with one command sequence.

To perform a Main Memory Byte/Page Program through Buffer 1 using the standard DataFlash page size (528 bytes), an opcode of 02h must first be clocked into the device followed by three address bytes comprised of two dummy bits, 12 page address bits (PA11 - PA0) that specify the page in the main memory to be written, and 10 buffer address bits (BFA9 - BFA0) that select the first byte in the buffer to be written. After all address bytes are clocked in, the device will take data from the input pin (SI) and store it in Buffer 1. Any number of bytes (1 to 528) can be entered. If the end of the buffer is reached, then the device will wrap around back to the beginning of the buffer.

To perform a Main Memory Byte/Page Program through Buffer 1 using the binary page size (512 bytes), an opcode of 02h for Buffer 1 using must first be clocked into the device followed by three address bytes comprised of three dummy bits, 12 page address bits (A20 - A9) that specify the page in the main memory to be written, and nine buffer address bits (BFA8 - BFA0) that selects the first byte in the buffer to be written. After all address bytes are clocked in, the device will take data from the input pin (SI) and store it in Buffer 1. Any number of bytes (1 to 512) can be entered. If the end of the buffer is reached, then the device will wrap around back to the beginning of the buffer. When using the binary page size, the page and buffer address bits correspond to a 21-bit logical address (A20-A0) in the main memory.

After all data bytes have been clocked into the device, a low-to-high transition on the $\overline{\text{CS}}$ pin will start the program operation in which the device will program the data stored in Buffer 1 into the main memory array. Only the data bytes that were clocked into the device will be programmed into the main memory.

Example: If only two data bytes were clocked into the device, then only two bytes will be programmed into main memory and the remaining bytes in the memory page will remain in their previous state.

The $\overline{\text{CS}}$ pin must be deasserted on a byte boundary (multiples of eight bits); otherwise, the operation will be aborted and no data will be programmed. The programming of the data bytes is internally self-timed and should take place in a maximum time of t_P (the program time will be a multiple of the t_{BP} time depending on the number of bytes being programmed). During this time, the RDY/$\overline{\text{BUSY}}$ bit in the Status Register will indicate that the device is busy.

The device also incorporates an intelligent programming algorithm that can detect when a byte location fails to program properly. If a programming error arises, it will be indicated by the EPE bit in the Status Register.

6.6 Page Erase

The Page Erase command can be used to individually erase any page in the main memory array allowing the Buffer to Main Memory Page Program without Built-In Erase command or the Main Memory Byte/Page Program through Buffer 1 command to be utilized at a later time.

To perform a Page Erase with the standard DataFlash page size (528 bytes), an opcode of 81h must be clocked into the device followed by three address bytes comprised of two dummy bits, 12 page address bits (PA11 - PA0) that specify the page in the main memory to be erased, and 10 dummy bits.

To perform a Page Erase with the binary page size (512 bytes), an opcode of 81h must be clocked into the device followed by three address bytes comprised of three dummy bits, 12 page address bits (A20 - A9) that specify the page in the main memory to be erased, and nine dummy bits.

When a low-to-high transition occurs on the $\overline{\text{CS}}$ pin, the device will erase the selected page (the erased state is a Logic 1). The erase operation is internally self-timed and should take place in a maximum time of t_{PE}. During this time, the RDY/$\overline{\text{BUSY}}$ bit in the Status Register will indicate that the device is busy.

The device also incorporates an intelligent erase algorithm that can detect when a byte location fails to erase properly. If an erase error arises, it will be indicated by the EPE bit in the Status Register.

6.7 Block Erase

The Block Erase command can be used to erase a block of eight pages at one time. This command is useful when needing to pre-erase larger amounts of memory and is more efficient than issuing eight separate Page Erase commands.

To perform a Block Erase with the standard DataFlash page size (528 bytes), an opcode of 50h must be clocked into the device followed by three address bytes comprised of two dummy bits, nine page address bits (PA11 - PA3), and 13 dummy bits. The nine page address bits are used to specify which block of eight pages is to be erased.

To perform a Block Erase with the binary page size (512 bytes), an opcode of 50h must be clocked into the device followed by three address bytes comprised of three dummy bits, nine page address bits (A20 - A12), and 12 dummy bits. The nine page address bits are used to specify which block of eight pages is to be erased.

When a low-to-high transition occurs on the $\overline{\text{CS}}$ pin, the device will erase the selected block of eight pages. The erase operation is internally self-timed and should take place in a maximum time of t_{BE}. During this time, the RDY/$\overline{\text{BUSY}}$ bit in the Status Register will indicate that the device is busy.

The device also incorporates an intelligent erase algorithm that can detect when a byte location fails to erase properly. If an erase error arises, it will be indicated by the EPE bit in the Status Register.

Table 6-1. Block Erase Addressing

PA11/ A20	PA10/ A19	PA9/ A18	PA8/ A17	PA7/ A16	PA6/ A15	PA5/ A14	PA4/ A13	PA3/ A12	PA2/ A11	PA1/ A10	PA0/ A9	Block
0	0	0	0	0	0	0	0	0	X	X	X	0
0	0	0	0	0	0	0	0	1	X	X	X	1
0	0	0	0	0	0	0	1	0	X	X	X	2
0	0	0	0	0	0	0	1	1	X	X	X	3
• • •	• • •	• • •	• • •	• • •	• • •	• • •	• • •	• • •	• • •	• • •	• • •	• • •
1	1	1	1	1	1	1	0	0	X	X	X	508
1	1	1	1	1	1	1	0	1	X	X	X	509
1	1	1	1	1	1	1	1	0	X	X	X	510
1	1	1	1	1	1	1	1	1	X	X	X	511

6.8 Sector Erase

The Sector Erase command can be used to individually erase any sector in the main memory.

The main memory array is comprised of 17 sectors, and only one sector can be erased at a time. To perform an erase of Sector 0a or Sector 0b with the standard DataFlash page size (528 bytes), an opcode of 7Ch must be clocked into the device followed by three address bytes comprised of two dummy bits, nine page address bits (PA11 - PA3), and 13 dummy bits. To perform a Sector 1-15 erase, an opcode of 7Ch must be clocked into the device followed by three address bytes comprised of two dummy bits, four page address bits (PA11 - PA8), and 18 dummy bits.

To perform a Sector 0a or Sector 0b erase with the binary page size (512 bytes), an opcode of 7Ch must be clocked into the device followed by three address bytes comprised of three dummy bits, nine page address bits (A20 - A12), and 12 dummy bits. To perform a Sector 1-15 erase, an opcode of 7Ch must be clocked into the device followed by three dummy bits, four page address bits (A20 - A17), and 17 dummy bits.

The page address bits are used to specify any valid address location within the sector to be erased. When a low-to high transition occurs on the $\overline{\text{CS}}$ pin, the device will erase the selected sector. The erase operation is internally self-timed and should take place in a maximum time of t_{SE}. During this time, the RDY/$\overline{\text{BUSY}}$ bit in the Status Register will indicate that the device is busy.

The device also incorporates an intelligent algorithm that can detect when a byte location fails to erase properly. If an erase error arises, it will be indicated by the EPE bit in the Status Register.

Table 6-2. Sector Erase Addressing

PA11/ A20	PA10/ A19	PA9/ A18	PA8/ A17	PA7/ A16	PA6/ A15	PA5/ A14	PA4/ A13	PA3/ A12	PA2/ A11	PA1/ A10	PA0/ A9	Sector
0	0	0	0	0	0	0	0	0	X	X	X	0a
0	0	0	0	0	0	0	0	1	X	X	X	0b
0	0	0	1	X	X	X	X	X	X	X	X	1
0	0	1	0	X	X	X	X	X	X	X	X	2
• • •	• • •	• • •	• • •	• • •	• • •	• • •	• • •	• • •	• • •	• • •	• • •	• • •
1	1	0	0	X	X	X	X	X	X	X	X	12
1	1	0	1	X	X	X	X	X	X	X	X	13
1	1	1	0	X	X	X	X	X	X	X	X	14
1	1	1	1	X	X	X	X	X	X	X	X	15

6.9 Chip Erase

The Chip Erase command allows the entire main memory array to be erased can be erased at one time.

To execute the Chip Erase command, a 4-byte command sequence of C7h, 94h, 80h, and 9Ah must be clocked into the device. Since the entire memory array is to be erased, no address bytes need to be clocked into the device, and any data clocked in after the opcode will be ignored. After the last bit of the opcode sequence has been clocked in, the $\overline{CS}$ pin must be deasserted to start the erase process. The erase operation is internally self-timed and should take place in a time of t_{CE}. During this time, the RDY/$\overline{BUSY}$ bit in the Status Register will indicate that the device is busy.

The Chip Erase command will not affect sectors that are protected or locked down; the contents of those sectors will remain unchanged. Only those sectors that are not protected or locked down will be erased.

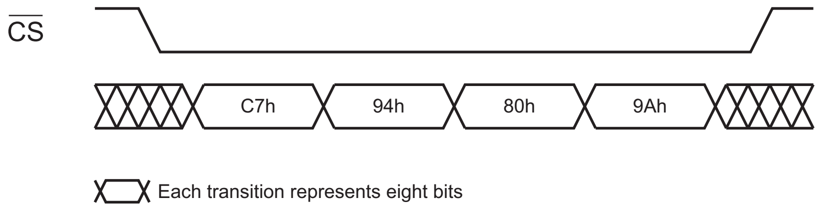
The $\overline{WP}$ pin can be asserted while the device is erasing, but protection will not be activated until the internal erase cycle completes.

The device also incorporates an intelligent algorithm that can detect when a byte location fails to erase properly. If an erase error arises, it will be indicated by the EPE bit in the Status Register.

Table 6-3. Chip Erase Command

Command	Byte 1	Byte 2	Byte 3	Byte 4
Chip Erase	C7h	94h	80h	9Ah

Figure 6-1. Chip Erase



6.10 Program/Erase Suspend

In some code and data storage applications, it may not be possible for the system to wait the milliseconds required for the Flash memory to complete a program or erase cycle. The Program/Erase Suspend command allows a program or erase operation in progress to a particular 128KB sector of the main memory array to be suspended so that other device operations can be performed.

Example: By suspending an erase operation to a particular sector, the system can perform functions such as a program or read operation within a different 128KB sector. Other device operations, such as Read Status Register, can also be performed while a program or erase operation is suspended.

To perform a Program/Erase Suspend, an opcode of B0h must be clocked into the device. No address bytes need to be clocked into the device, and any data clocked in after the opcode will be ignored. When the $\overline{\text{CS}}$ pin is deasserted, the program or erase operation currently in progress will be suspended within a time of t_{SUSP}. One of the Program Suspend bits (PS1 or PS2) or the Erase Suspend bit (ES) in the Status Register will then be set to the Logic 1 state. In addition, the RDY/$\overline{\text{BUSY}}$ bit in the Status Register will indicate that the device is ready for another operation.

Read operations are not allowed to a 128KB sector that has had its program or erase operation suspended. If a read is attempted to a suspended sector, then the device will output undefined data. Therefore, when performing a Continuous Array Read operation and the device's internal address counter increments and crosses the sector boundary to a suspended sector, the device will then start outputting undefined data continuously until the address counter increments and crosses a sector boundary to an unsuspended sector.

A program operation is not allowed to a sector that has been erase suspended. If a program operation is attempted to an erase suspended sector, then the program operation will abort.

During an Erase Suspend, a program operation to a different 128KB sector can be started and subsequently suspended. This results in a simultaneous Erase Suspend/Program Suspend condition and will be indicated by the states of both the ES and PS1 or PS2 bits in the Status Register being set to a Logic 1.

If a Reset command is performed, or if the $\overline{\text{RESET}}$ pin is asserted while a sector is erase suspended, then the suspend operation will be aborted and the contents of the sector will be left in an undefined state. However, if a reset is performed while a page is program or erase suspended, the suspend operation will abort but only the contents of the page that was being programmed or erased will be undefined; the remaining pages in the 128KB sector will retain their previous contents.

Table 6-4. Operations Allowed and Not Allowed During Suspend

Command	Operation During Program Suspend in Buffer 1 (PS1)	Operation During Program Suspend in Buffer 2 (PS2)	Operation During Erase Suspend (ES)
Read Commands			
Read Array (All Opcodes)	Allowed	Allowed	Allowed
Read Buffer 1 (All Opcodes)	Allowed	Allowed	Allowed
Read Buffer 2 (All Opcodes)	Allowed	Allowed	Allowed
Program and Erase Commands			
Buffer 1 Write	Not Allowed	Allowed	Allowed
Buffer 2 Write	Allowed	Not Allowed	Allowed
Buffer 1 to Memory Program w/ Erase	Not Allowed	Not Allowed	Not Allowed
Buffer 2 to Memory Program w/ Erase	Not Allowed	Not Allowed	Not Allowed
Buffer 1 to Memory Program w/o Erase	Not Allowed	Not Allowed	Allowed
Buffer 2 to Memory Program w/o Erase	Not Allowed	Not Allowed	Allowed
Memory Program through Buffer 1 w/ Erase	Not Allowed	Not Allowed	Not Allowed
Memory Program through Buffer 2 w/ Erase	Not Allowed	Not Allowed	Not Allowed
Memory Program through Buffer 1 w/o Erase	Not Allowed	Not Allowed	Allowed
Auto Page Rewrite	Not Allowed	Not Allowed	Not Allowed
Page Erase	Not Allowed	Not Allowed	Not Allowed
Block Erase	Not Allowed	Not Allowed	Not Allowed
Sector Erase	Not Allowed	Not Allowed	Not Allowed
Chip Erase	Not Allowed	Not Allowed	Not Allowed
Protection and Security Commands			
Enable Sector Protection	Not Allowed	Not Allowed	Not Allowed
Disable Sector Protection	Not Allowed	Not Allowed	Not Allowed
Erase Sector Protection Register	Not Allowed	Not Allowed	Not Allowed
Program Sector Protection Register	Not Allowed	Not Allowed	Not Allowed
Read Sector Protection Register	Allowed	Allowed	Allowed
Sector Lockdown	Not Allowed	Not Allowed	Not Allowed
Read Sector Lockdown	Allowed	Allowed	Allowed
Freeze Sector Lockdown State	Not Allowed	Not Allowed	Not Allowed
Program Security Register	Not Allowed	Not Allowed	Not Allowed
Read Security Register	Allowed	Allowed	Allowed
Additional Commands			
Main Memory to Buffer 1 Transfer	Not Allowed	Allowed	Allowed
Main Memory to Buffer 2 Transfer	Allowed	Not Allowed	Allowed
Main Memory to Buffer 1 Compare	Allowed	Allowed	Allowed
Main Memory to Buffer 2 Compare	Allowed	Allowed	Allowed
Enter Deep Power-Down	Not Allowed	Not Allowed	Not Allowed
Resume from Deep Power-Down	Not Allowed	Not Allowed	Not Allowed
Enter Ultra-Deep Power-Down mode	Not Allowed	Not Allowed	Not Allowed
Read Configuration Register	Allowed	Allowed	Allowed
Read Status Register	Allowed	Allowed	Allowed
Read Manufacturer and Device ID	Allowed	Allowed	Allowed
Reset (via Hardware or Software)	Allowed	Allowed	Allowed

6.11 Program/Erase Resume

The Program/Erase Resume command allows a suspended program or erase operation to be resumed and continue where it left off.

To perform a Program/Erase Resume, an opcode of D0h must be clocked into the device. No address bytes need to be clocked into the device, and any data clocked in after the opcode will be ignored. When the $\overline{\text{CS}}$ pin is deasserted, the program or erase operation currently suspended will be resumed within a time of t_{RES}. The PS1 bit, PS2 bit, or ES bit in the Status Register will then be reset back to a Logic 0 state to indicate that the program or erase operation is no longer suspended. In addition, the RDY/$\overline{\text{BUSY}}$ bit in the Status Register will indicate that the device is busy performing a program or erase operation.

During a simultaneous Erase Suspend/Program Suspend condition, issuing the Program/Erase Resume command will result in the program operation resuming first. After the program operation has been completed, the Program/Erase Resume command must be issued again in order for the erase operation to be resumed.

While the device is busy resuming a program or erase operation, any attempts at issuing the Program/Erase Suspend command will be ignored. Therefore, if a resumed program or erase operation needs to be subsequently suspended again, the system must either wait the entire t_{RES} time before issuing the Program/Erase Suspend command, or it must check the status of the RDY/$\overline{\text{BUSY}}$ bit or the appropriate PS1, PS2, or ES bit in the Status Register to determine if the previously suspended program or erase operation has resumed.

7. Sector Protection

Two protection methods, hardware and software controlled, are provided for protection against inadvertent or erroneous program and erase cycles. The software controlled method relies on the use of software commands to enable and disable sector protection while the hardware controlled method employs the use of the Write Protect ($\overline{\text{WP}}$) pin. The selection of which sectors that are to be protected or unprotected against program and erase operations is specified in the Nonvolatile Sector Protection Register. The status of whether or not sector protection has been enabled or disabled by either the software or the hardware controlled methods can be determined by checking the Status Register.

7.1 Software Sector Protection

Software controlled protection is useful in applications in which the $\overline{\text{WP}}$ pin is not or cannot be controlled by a host processor. In such instances, the $\overline{\text{WP}}$ pin may be left floating (the $\overline{\text{WP}}$ pin is internally pulled high) and sector protection can be controlled using the Enable Sector Protection and Disable Sector Protection commands.

If the device is power cycled, then the software controlled protection will be disabled. Once the device is powered up, the Enable Sector Protection command should be reissued if sector protection is desired and if the $\overline{\text{WP}}$ pin is not used.

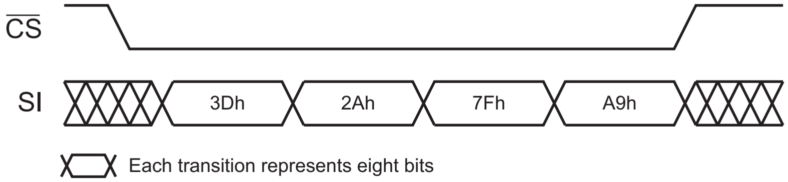
7.1.1 Enable Sector Protection

Sectors specified for protection in the Sector Protection Register can be protected from program and erase operations by issuing the Enable Sector Protection command. To enable the sector protection, a 4-byte command sequence of 3Dh, 2Ah, 7Fh, and A9h must be clocked into the device. After the last bit of the opcode sequence has been clocked in, the $\overline{\text{CS}}$ pin must be deasserted to enable the Sector Protection.

Table 7-1. Enable Sector Protection Command

Command	Byte 1	Byte 2	Byte 3	Byte 4
Enable Sector Protection	3Dh	2Ah	7Fh	A9h

Figure 7-1. Enable Sector Protection



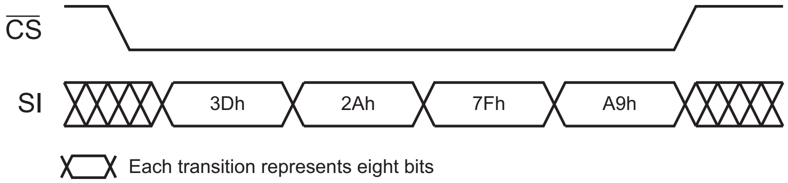
7.1.2 Disable Sector Protection

To disable the sector protection, a 4-byte command sequence of 3Dh, 2Ah, 7Fh, and 9Ah must be clocked into the device. After the last bit of the opcode sequence has been clocked in, the $\overline{\text{CS}}$ pin must be deasserted to disable the sector protection.

Table 7-2. Disable Sector Protection Command

Command	Byte 1	Byte 2	Byte 3	Byte 4
Disable Sector Protection	3Dh	2Ah	7Fh	9Ah

Figure 7-2. Disable Sector Protection



7.2 Hardware Controlled Protection

Sectors specified for protection in the Sector Protection Register and the Sector Protection Register itself can be protected from program and erase operations by asserting the $\overline{\text{WP}}$ pin and keeping the pin in its asserted state. The Sector Protection Register and any sector specified for protection cannot be erased or programmed as long as the $\overline{\text{WP}}$ pin is asserted. In order to modify the Sector Protection Register, the $\overline{\text{WP}}$ pin must be deasserted. If the $\overline{\text{WP}}$ pin is permanently connected to GND, then the contents of the Sector Protection Register cannot be changed. If the $\overline{\text{WP}}$ pin is deasserted or permanently connected to V_{CC}, then the contents of the Sector Protection Register can be modified.

The $\overline{\text{WP}}$ pin will override the software controlled protection method but only for protecting the sectors.

Example: If the sectors were not previously protected by the Enable Sector Protection command, then simply asserting the $\overline{\text{WP}}$ pin would enable the sector protection within the maximum specified t_{WPE} time. When the $\overline{\text{WP}}$ pin is deasserted, however, the sector protection would no longer be enabled (after the maximum specified t_{WPD} time) as long as the Enable Sector Protection command was not issued while the $\overline{\text{WP}}$ pin was asserted. If the Enable Sector Protection command was issued before or while the $\overline{\text{WP}}$ pin was asserted, then simply deasserting the $\overline{\text{WP}}$ pin would not disable the sector protection. In this case, the Disable Sector Protection command would need to be issued while the $\overline{\text{WP}}$ pin is deasserted to disable the sector protection. The Disable Sector Protection command is also ignored whenever the $\overline{\text{WP}}$ pin is asserted.

A noise filter is incorporated to help protect against spurious noise that may inadvertently assert or deassert the $\overline{\text{WP}}$ pin.

Figures 7-3 and Table 7-3 detail the sector protection status for various scenarios of the $\overline{\text{WP}}$ pin, the Enable Sector Protection command, and the Disable Sector Protection command.

Figure 7-3. $\overline{\text{WP}}$ Pin and Protection Status

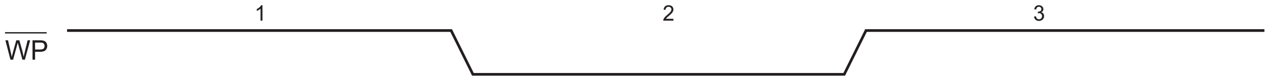


Table 7-3. $\overline{\text{WP}}$ Pin and Protection Status

Time Period	$\overline{\text{WP}}$ Pin	Enable Sector Protection Command	Disable Sector Protection Command	Sector Protection Status	Sector Protection Register
1	High	Command Not Issued Previously	X	Disabled	Read/Write
		—	Issue Command	Disabled	Read/Write
		Issue Command	—	Enabled	Read/Write
2	Low	X	X	Enabled	Read
3	High	Command Issued During Period 1 or 2	Not Issued Yet	Enabled	Read/Write
		—	Issue Command	Disabled	Read/Write
		Issue Command	—	Enabled	Read/Write

7.3 Sector Protection Register

The nonvolatile Sector Protection Register specifies which sectors are to be protected or unprotected with either the software or hardware controlled protection methods. The Sector Protection Register contains 16 bytes of data, of which byte locations 0 through 15 contain values that specify whether Sectors 0 through 15 will be protected or unprotected. The Sector Protection Register is user modifiable and must be erased before it can be reprogrammed. Table 7-4 illustrates the format of the Sector Protection Register.

Table 7-4. Sector Protection Register

Sector Number	0 (0a, 0b)	1 to 15
Protected	See Table 7-5	FFh
Unprotected		00h

Note: 1. The default values for bytes 0 through 15 are 00h when shipped from Atmel.

Table 7-5. Sector 0 (0a, 0b) Sector Protection Register Byte Value

	Bit 7:6	Bit 5:4	Bit 3:2	Bit 1:0	Data Value
	Sector 0a (Page 0-7)	Sector 0b (Page 8-255)	N/A	N/A	
Sectors 0a and 0b Unprotected	00	00	XX	XX	0xh
Protect Sector 0a	11	00	XX	XX	Cxh
Protect Sector 0b	00	11	XX	XX	3xh
Protect Sectors 0a and 0b	11	11	XX	XX	Fxh

Note: 1. x = Don't care

7.3.1 Erase Sector Protection Register

In order to modify and change the values of the Sector Protection Register, it must first be erased using the Erase Sector Protection Register command.

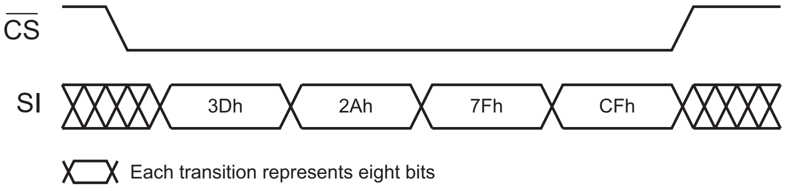
To erase the Sector Protection Register, a 4-byte command sequence of 3Dh, 2Ah, 7Fh, and CFh must be clocked into the device. After the last bit of the opcode sequence has been clocked in, the $\overline{\text{CS}}$ pin must be deasserted to initiate the internally self-timed erase cycle. The erasing of the Sector Protection Register should take place in a maximum time of t_{PE}. During this time, the RDY/$\overline{\text{BUSY}}$ bit in the Status Register will indicate that the device is busy. If the device is powered-down before the completion of the erase cycle, then the contents of the Sector Protection Register cannot be guaranteed.

The Sector Protection Register can be erased with sector protection enabled or disabled. Since the erased state (FFh) of each byte in the Sector Protection Register is used to indicate that a sector is specified for protection, leaving the sector protection enabled during the erasing of the register allows the protection scheme to be more effective in the prevention of accidental programming or erasing of the device. If for some reason an erroneous program or erase command is sent to the device immediately after erasing the Sector Protection Register and before the register can be reprogrammed, then the erroneous program or erase command will not be processed because all sectors would be protected.

Table 7-6. Erase Sector Protection Register Command

Command	Byte 1	Byte 2	Byte 3	Byte 4
Erase Sector Protection Register	3Dh	2Ah	7Fh	CFh

Figure 7-4. Erase Sector Protection Register



7.3.2 Program Sector Protection Register

Once the Sector Protection Register has been erased, it can be reprogrammed using the Program Sector Protection Register command.

To program the Sector Protection Register, a 4-byte command sequence of 3Dh, 2Ah, 7Fh, and FCh must be clocked into the device followed by 16 bytes of data corresponding to Sectors 0 through 15. After the last bit of the opcode sequence and data have been clocked in, the $\overline{CS}$ pin must be deasserted to initiate the internally self-timed program cycle. The programming of the Sector Protection Register should take place in a maximum time of t_P. During this time, the RDY/$\overline{BUSY}$ bit in the Status Register will indicate that the device is busy. If the device is powered-down before the completion of the erase cycle, then the contents of the Sector Protection Register cannot be guaranteed.

If the proper number of data bytes is not clocked in before the $\overline{CS}$ pin is deasserted, then the protection status of the sectors corresponding to the bytes not clocked in cannot be guaranteed.

Example: If only the first two bytes are clocked in instead of the complete 16 bytes, then the protection status of the last 14 sectors cannot be guaranteed. Furthermore, if more than 16 bytes of data is clocked into the device, then the data will wrap back around to the beginning of the register. For instance, if 17 bytes of data are clocked in, then the 17th byte will be stored at byte location 0 of the Sector Protection Register.

The data bytes clocked into the Sector Protection Register need to be valid values (0xh, 3xh, Cxh, and Fxh for Sector 0a or Sector 0b, and 00h or FFh for other sectors) in order for the protection to function correctly. If a non-valid value is clocked into a byte location of the Sector Protection Register, then the protection status of the sector corresponding to that byte location cannot be guaranteed.

Example: If a value of 17h is clocked into byte location 2 of the Sector Protection Register, then the protection status of Sector 2 cannot be guaranteed.

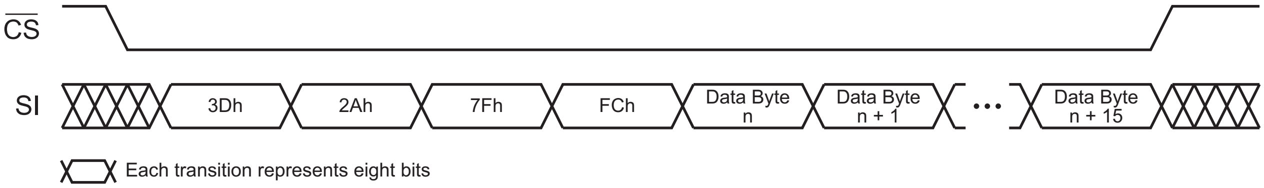
The Sector Protection Register can be reprogrammed while the sector protection is enabled or disabled. Being able to reprogram the Sector Protection Register with the sector protection enabled allows the user to temporarily disable the sector protection to an individual sector rather than disabling sector protection completely.

The Program Sector Protection Register command utilizes Buffer 1 for processing. Therefore, the contents of Buffer 1 will be altered from its previous state when this command is issued.

Table 7-7. Program Sector Protection Register Command

Command	Byte 1	Byte 2	Byte 3	Byte 4
Program Sector Protection Register	3Dh	2Ah	7Fh	FCh

Figure 7-5. Program Sector Protection Register



7.3.3 Read Sector Protection Register

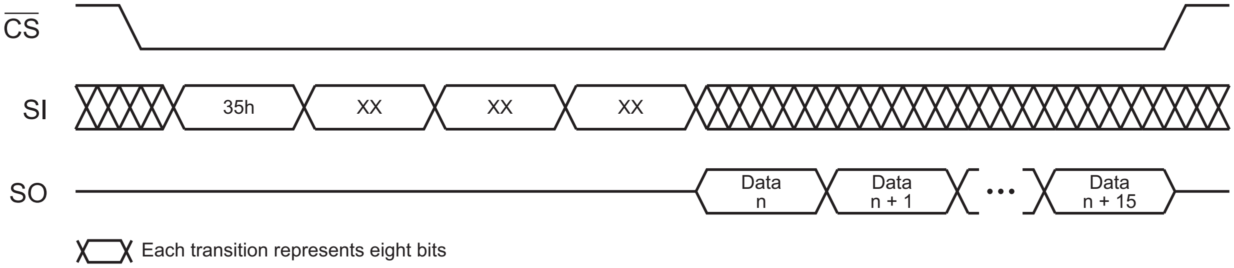
To read the Sector Protection Register, an opcode of 32h and three dummy bytes must be clocked into the device. After the last bit of the opcode and dummy bytes have been clocked in, any additional clock pulses on the SCK pin will result in the Sector Protection Register contents being output on the SO pin. The first byte (byte location 0) corresponds to Sector 0 (0a and 0b), the second byte corresponds to Sector 1, and the last byte (byte location 15) corresponds to Sector 15. Once the last byte of the Sector Protection Register has been clocked out, any additional clock pulses will result in undefined data being output on the SO pin. The $\overline{\text{CS}}$ pin must be deasserted to terminate the Read Sector Protection Register operation and put the output into a high-impedance state.

Table 7-8. Read Sector Protection Register Command

Command	Byte 1	Byte 2	Byte 3	Byte 4
Read Sector Protection Register	32h	XXh	XXh	XXh

Note: 1. XX = Dummy byte

Figure 7-6. Read Sector Protection Register



7.3.4 About the Sector Protection Register

The Sector Protection Register is subject to a limit of 10,000 erase/program cycles. Users are encouraged to carefully evaluate the number of times the Sector Protection Register will be modified during the course of the application's life cycle. If the application requires that the Security Protection Register be modified more than the specified limit of 10,000 cycles because the application needs to temporarily unprotect individual sectors (sector protection remains enabled while the Sector Protection Register is reprogrammed), then the application will need to limit this practice. Instead, a combination of temporarily unprotecting individual sectors along with disabling sector protection completely will need to be implemented by the application to ensure that the limit of 10,000 cycles is not exceeded.

8. Security Features

8.1 Sector Lockdown

The device incorporates a sector lockdown mechanism that allows each individual sector to be permanently locked so that it becomes read-only (ROM). This is useful for applications that require the ability to permanently protect a number of sectors against malicious attempts at altering program code or security information.

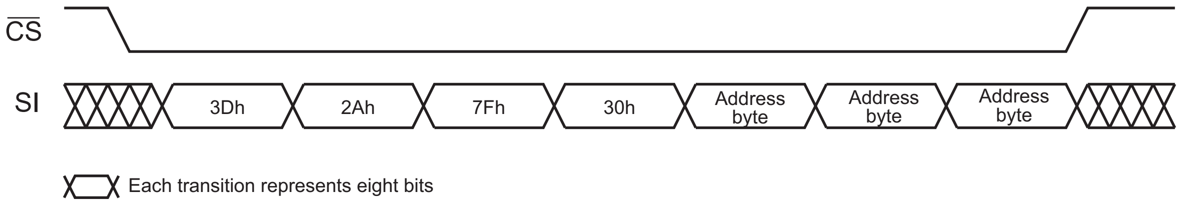
Warning: Once a sector is locked down, it can never be erased or programmed, and it can never be unlocked.

To issue the sector lockdown command, a 4-byte command sequence of 3Dh, 2Ah, 7Fh, and 30h must be clocked into the device followed by three address bytes specifying any address within the sector to be locked down. After the last address bit has been clocked in, the $\overline{CS}$ pin must be deasserted to initiate the internally self-timed lockdown sequence. The lockdown sequence should take place in a maximum time of t_P. During this time, the RDY/$\overline{BUSY}$ bit in the Status Register will indicate that the device is busy. If the device is powered-down before the completion of the lockdown sequence, then the lockdown status of the sector cannot be guaranteed. In this case, it is recommended that the user read the Sector Lockdown Register to determine the status of the appropriate sector lockdown bits or bytes and re-issue the Sector Lockdown command if necessary.

Table 8-1. Sector Lockdown Command

Command	Byte 1	Byte 2	Byte 3	Byte 4
Sector Lockdown	3Dh	2Ah	7Fh	30h

Figure 8-1. Sector Lockdown



8.1.1 Read Sector Lockdown Register

The nonvolatile Sector Lockdown Register specifies which sectors in the main memory are currently unlocked or have been permanently locked down. The Sector Lockdown Register is a read-only register and contains 16 bytes of data which correspond to Sectors 0 through 15. To read the Sector Lockdown Register, an opcode of 35h must be clocked into the device followed by three dummy bytes. After the last bit of the opcode and dummy bytes have been clocked in, the data for the contents of the Sector Lockdown Register will be clocked out on the SO pin. The first byte (byte location 0) corresponds to Sector 0 (0a and 0b), the second byte corresponds to Sector 1, and the last byte (byte location 15) corresponds to Sector 15. After the last byte of the Sector Lockdown Register has been read, additional pulses on the SCK pin will result in undefined data being output on the SO pin.

Deasserting the $\overline{CS}$ pin will terminate the Read Sector Lockdown Register operation and put the SO pin into a high-impedance state. Table 8-2 details the format the Sector Lockdown Register.

Table 8-2. Sector Lockdown Register

Sector Number	0 (0a, 0b)	1 to 15
Locked	See Table 8-3	FFh
Unlocked		00h

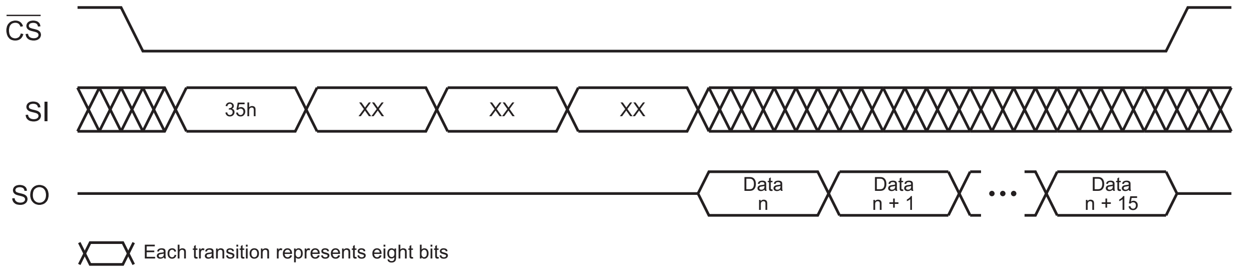
Table 8-3. Sector 0 (0a and 0b) Sector Lockdown Register Byte Value

	Bit 7:6	Bit 5:4	Bit 3:2	Bit 1:0	Data Value
	Sector 0a (Page 0-7)	Sector 0b (Page 8-255)	N/A	N/A	
Sectors 0a and 0b Unlocked	00	00	00	00	00h
Sector 0a Locked	11	00	00	00	C0h
Sector 0b Locked	00	11	00	00	30h
Sectors 0a and 0b Locked	11	11	00	00	F0h

Table 8-4. Read Sector Lockdown Register Command

Command	Byte 1	Byte 2	Byte 3	Byte 4
Read Sector Lockdown Register	35h	XXh	XXh	XXh

Figure 8-2. Read Sector Lockdown Register



8.1.2 Freeze Sector Lockdown

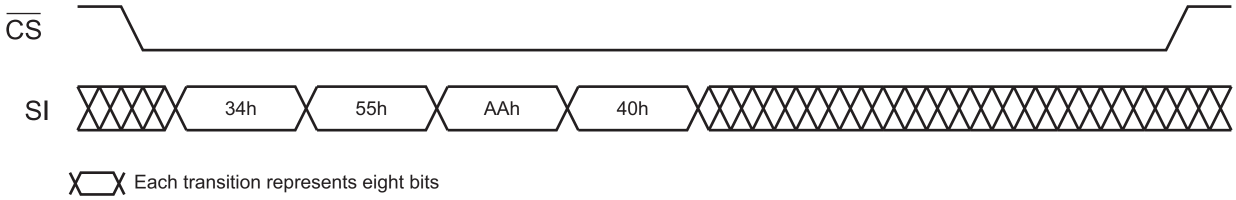
The Sector Lockdown command can be permanently disabled, and the current sector lockdown state can be permanently frozen so that no additional sectors can be locked down aside from those already locked down. Any attempts to issue the Sector Lockdown command after the Sector Lockdown State has been frozen will be ignored.

To issue the Freeze Sector Lockdown command, the $\overline{CS}$ pin must be asserted and the opcode sequence of 34h, 55h, AAh, and 40h must be clocked into the device. Any additional data clocked into the device will be ignored. When the $\overline{CS}$ pin is deasserted, the current sector lockdown state will be permanently frozen within a time of t_{LOCK}. In addition, the SLE bit in the Status Register will be permanently reset to a Logic 0 to indicate that the Sector Lockdown command is permanently disabled.

Table 8-5. Freeze Sector Lockdown

Command	Byte 1	Byte 2	Byte 3	Byte 4
Freeze Sector Lockdown	34h	55h	AAh	40h

Figure 8-3. Freeze Sector Lockdown



8.2 Security Register

The device contains a specialized Security Register that can be used for purposes such as unique device serialization or locked key storage. The register is comprised of a total of 128 bytes that is divided into two portions. The first 64 bytes (byte locations 0 through 63) of the Security Register are allocated as a One-Time Programmable space. Once these 64 bytes have been programmed, they cannot be erased or reprogrammed. The remaining 64 bytes of the register (byte locations 64 through 127) are factory programmed by Atmel and will contain a unique value for each device. The factory programmed data is fixed and cannot be changed.

Table 8-6. Security Register

	Security Register Byte Number							
	0	1	· · ·	63	64	65	· · ·	127
Data Type	One-Time User Programmable				Factory Programmed by Atmel			

8.2.1 Programming the Security Register

The user programmable portion of the Security Register does not need to be erased before it is programmed.

To program the Security Register, a 4-byte opcode sequence of 9Bh, 00h, 00h, and 00h must be clocked into the device. After the last bit of the opcode sequence has been clocked into the device, the data for the contents of the 64-byte user programmable portion of the Security Register must be clocked in.

After the last data byte has been clocked in, the $\overline{\text{CS}}$ pin must be deasserted to initiate the internally self-timed program cycle. The programming of the Security Register should take place in a time of t_P, during which time the RDY/$\overline{\text{BUSY}}$ bit in the Status Register will indicate that the device is busy. If the device is powered-down during the program cycle, then the contents of the 64-byte user programmable portion of the Security Register cannot be guaranteed.

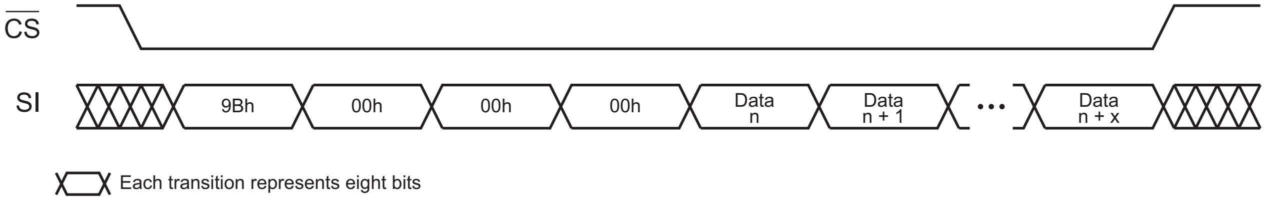
If the full 64 bytes of data are not clocked in before the $\overline{\text{CS}}$ pin is deasserted, then the values of the byte locations not clocked in cannot be guaranteed.

Example: If only the first two bytes are clocked in instead of the complete 64 bytes, then the remaining 62 bytes of the user programmable portion of the Security Register cannot be guaranteed. Furthermore, if more than 64 bytes of data is clocked into the device, then the data will wrap back around to the beginning of the register. For example, if 65 bytes of data are clocked in, then the 65th byte will be stored at byte location 0 of the Security Register.

Warning: **The user programmable portion of the Security Register can only be programmed one time.** Therefore, it is not possible, for example, to only program the first two bytes of the register and then program the remaining 62 bytes at a later time.

The Program Security Register command utilizes Buffer 1 for processing. Therefore, the contents of Buffer 1 will be altered from its previous state when this command is issued.

Figure 8-4. Program Security Register

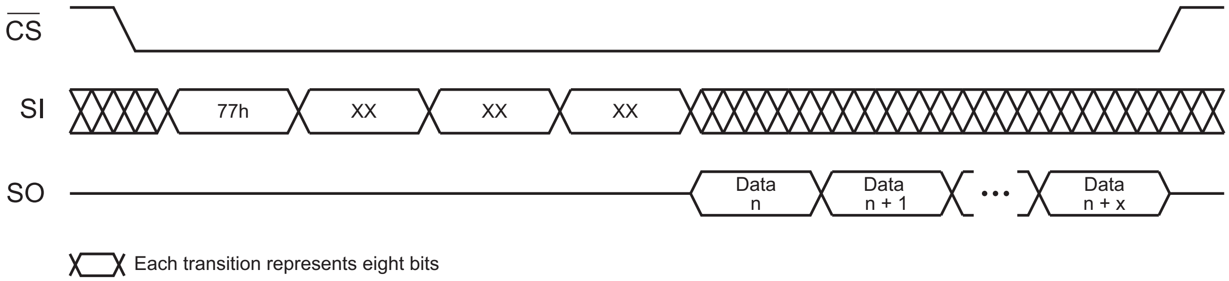


8.2.2 Reading the Security Register

To read the Security Register, an opcode of 77h and three dummy bytes must be clocked into the device. After the last dummy bit has been clocked in, the contents of the Security Register can be clocked out on the SO pin. After the last byte of the Security Register has been read, additional pulses on the SCK pin will result in undefined data being output on the SO pin.

Deasserting the $\overline{CS}$ pin will terminate the Read Security Register operation and put the SO pin into a high-impedance state.

Figure 8-5. Read Security Register



9. Additional Commands

9.1 Main Memory Page to Buffer Transfer

A page of data can be transferred from the main memory to either Buffer 1 or Buffer 2. To transfer a page of data using the standard DataFlash page size (528 bytes), an opcode of 53h for Buffer 1 or 55h for Buffer 2 must be clocked into the device followed by three address bytes comprised of two dummy bits, 12 page address bits (PA11 - PA0) which specify the page in main memory to be transferred, and 10 dummy bits. To transfer a page of data using the binary page size (512 bytes), an opcode of 53h for Buffer 1 and 55h for Buffer 2 must be clocked into the device followed by three address bytes comprised of three dummy bits, 12 page address bits (A20 - A9) which specify the page in the main memory to be transferred, and nine dummy bits.

The $\overline{\text{CS}}$ pin must be low while toggling the SCK pin to load the opcode and the three address bytes from the input pin (SI). The transfer of the page of data from the main memory to the buffer will begin when the $\overline{\text{CS}}$ pin transitions from a low to a high state. During the page transfer time (t_{XFR}), the RDY/$\overline{\text{BUSY}}$ bit in the Status Register can be read to determine whether or not the transfer has been completed.

9.2 Main Memory Page to Buffer Compare

A page of data in main memory can be compared to the data in Buffer 1 or Buffer 2 as a method to ensure that data was successfully programmed after a Buffer to Main Memory Page Program command. To compare a page of data with the standard DataFlash page size (528 bytes), an opcode of 60h for Buffer 1 or 61h for Buffer 2 must be clocked into the device followed by three address bytes comprised of two dummy bits, 12 page address bits (PA11 - PA0) which specify the page in the main memory to be compared to the buffer, and 10 dummy bits. To compare a page of data with the binary page size (512 bytes), an opcode of 60h for Buffer 1 or 61h for Buffer 2 must be clocked into the device followed by three address bytes comprised of three dummy bits, 12 page address bits (A20 - A9) which specify the page in the main memory to be compared to the buffer, and nine dummy bits.

The $\overline{\text{CS}}$ pin must be low while toggling the SCK pin to load the opcode and the address bytes from the input pin (SI). On the low-to-high transition of the $\overline{\text{CS}}$ pin, the data bytes in the selected Main Memory Page will be compared with the data bytes in Buffer 1 or Buffer 2. During the compare time (t_{COMP}), the RDY/$\overline{\text{BUSY}}$ bit in the Status Register will indicate that the part is busy. On completion of the compare operation, bit 6 of the Status Register will be updated with the result of the compare.

9.3 Auto Page Rewrite

This command only needs to be used if the possibility exists that static (non-changing) data may be stored in a page or pages of a sector and the other pages of the same sector are erased and programmed a large number of times. Applications that modify data in a random fashion within a sector may fall into this category. To preserve data integrity of a sector, each page within a sector must be updated/rewritten at least once within every 20,000 cumulative page erase/program operations within that sector. The Auto Page Rewrite command provides a simple and efficient method to “refresh” a page in the main memory array in a single operation.

The Auto Page Rewrite command is a combination of the Main Memory Page to Buffer Transfer and Buffer to Main Memory Page Program with Built-In Erase commands. With the Auto Page Rewrite command, a page of data is first transferred from the main memory to Buffer 1 or Buffer 2 and then the same data (from Buffer 1 or Buffer 2) is programmed back into the same page of main memory, essentially “refreshing” the contents of that page. To start the Auto Page Rewrite operation with the standard DataFlash page size (528 bytes), a 1-byte opcode, 58H for Buffer 1 or 59H for Buffer 2, must be clocked into the device followed by three address bytes comprised of two dummy bits, 12 page address bits (PA11-PA0) that specify the page in main memory to be rewritten, and 10 dummy bits.

To initiate an Auto Page Rewrite with the a binary page size (512 bytes), the opcode 58H for Buffer 1 or 59H for Buffer 2, must be clocked into the device followed by three address bytes consisting of three dummy bits, 12 page address bits (A20 - A9) that specify the page in the main memory that is to be rewritten, and nine dummy bits. When a low-to-high transition occurs on the $\overline{\text{CS}}$ pin, the part will first transfer data from the page in main memory to a buffer and then program the data from the buffer back into same page of main memory. The operation is internally self-timed and should take place in a maximum time of t_{EP}. During this time, the RDY/$\overline{\text{BUSY}}$ Status Register will indicate that the part is busy.

If a sector is programmed or reprogrammed sequentially page by page and the possibility does not exist that there will be a page or pages of static data, then the programming algorithm shown in Figure 26-1 on page 61 is recommended. Otherwise, if there is a chance that there may be a page or pages of a sector that will contain static data, then the programming algorithm shown in Figure 26-2 on page 62 is recommended.

Please contact Atmel for availability of devices that are specified to exceed the 20,000 cycle cumulative limit.

9.4 Status Register Read

The 2-byte Status Register can be used to determine the device's ready/busy status, page size, a Main Memory Page to Buffer Compare operation result, the sector protection status, Freeze Sector Lockdown status, erase/program error status, Program/Erase Suspend status, and the device density. The Status Register can be read at any time, including during an internally self-timed program or erase operation.

To read the Status Register, the $\overline{\text{CS}}$ pin must first be asserted and then the opcode D7h must be clocked into the device. After the opcode has been clocked in, the device will begin outputting Status Register data on the SO pin during every subsequent clock cycle. After the second byte of the Status Register has been clocked out, the sequence will repeat itself, starting again with the first byte of the Status Register, as long as the $\overline{\text{CS}}$ pin remains asserted and the clock pin is being pulsed. The data in the Status Register is constantly being updated, so each repeating sequence may output new data. The RDY/$\overline{\text{BUSY}}$ status is available for both bytes of the Status Register and is updated for each byte.

Deasserting the $\overline{\text{CS}}$ pin will terminate the Status Register Read operation and put the SO pin into a high-impedance state. The $\overline{\text{CS}}$ pin can be deasserted at any time and does not require that a full byte of data be read.

Table 9-1. Status Register Format – Byte 1

Bit	Name		Type[1]	Description	
7	RDY/$\overline{\text{BUSY}}$	Ready/Busy Status	R	0	Device is busy with an internal operation.
				1	Device is ready.
6	COMP	Compare Result	R	0	Main memory page data matches buffer data.
				1	Main memory page data does not match buffer data.
5:2	DENSITY	Density Code	R	1011	16-Mbit
1	PROTECT	Sector Protection Status	R	0	Sector protection is disabled.
				1	Sector protection is enabled.
0	PAGE SIZE	Page Size Configuration	R	0	Device is configured for standard DataFlash page size (528 bytes).
				1	Device is configured for “power of 2” binary page size (512 bytes).

Note: 1. R = Readable only

Table 9-2. Status Register Format – Byte 2

Bit	Name		Type[1]	Description	
7	RDY/$\overline{\text{BUSY}}$	Ready/Busy Status	R	0	Device is busy with an internal operation.
				1	Device is ready.
6	RES	*Reserved for Future Use*	R	0	*Reserved for future use.*
5	EPE	Erase/Program Error	R	0	Erase or program operation was successful.
				1	Erase or program error detected.
4	RES	*Reserved for Future Use*	R	0	*Reserved for future use.*
3	SLE	Sector Lockdown Enabled	R	0	Sector Lockdown command is disabled.
				1	Sector Lockdown command is enabled.
2	PS2	Program Suspend Status (Buffer 2)	R	0	No program operation has been suspended while using Buffer 2.
				1	A sector is program suspended while using Buffer 2.
1	PS1	Program Suspend Status (Buffer 1)	R	0	No program operation has been suspended while using Buffer 1.
				1	A sector is program suspended while using Buffer 1.
0	ES	Erase Suspend	R	0	No sectors are erase suspended.
				1	A sector is erase suspended.

Note: 1. R = Readable only

9.4.1 RDY/$\overline{\text{BUSY}}$ Bit

The RDY/$\overline{\text{BUSY}}$ bit is used to determine whether or not an internal operation, such as a program or erase, is in progress. To poll the RDY/$\overline{\text{BUSY}}$ bit to detect the completion of an internally timed operation, new Status Register data must be continually clocked out of the device until the state of the RDY/$\overline{\text{BUSY}}$ bit changes from a Logic 0 to a Logic 1.

9.4.2 COMP Bit

The result of the most recent Main Memory Page to Buffer Compare operation is indicated using the COMP bit. If the COMP bit is a Logic 1, then at least one bit of the data in the Main Memory Page does not match the data in the buffer.

9.4.3 DENSITY Bits

The device density is indicated using the DENSITY bits. For the AT45DB161E, the four bit binary value is 1011. The decimal value of these four binary bits does not actually equate to the device density; the four bits represent a combinational code relating to differing densities of DataFlash devices. The DENSITY bits are not the same as the density code indicated in the JEDEC Device ID information. The DENSITY bits are provided only for backward compatibility to older generation DataFlash devices.

9.4.4 PROTECT Bit

The PROTECT bit provides information to the user on whether or not the sector protection has been enabled or disabled, either by the software-controlled method or the hardware-controlled method.

9.4.5 PAGE SIZE Bit

The PAGE SIZE bit indicates whether the buffer size and the page size of the main memory array is configured for the “power of 2” binary page size (512 bytes) or the standard DataFlash page size (528 bytes).

9.4.6 EPE Bit

The EPE bit indicates whether the last erase or program operation completed successfully or not. If at least one byte during the erase or program operation did not erase or program properly, then the EPE bit will be set to the Logic 1 state. The EPE bit will not be set if an erase or program operation aborts for any reason, such as an attempt to erase or program a protected region or a locked down sector or an attempt to erase or program a suspended sector. The EPE bit is updated after every erase and program operation.

9.4.7 SLE Bit

The SLE bit indicates whether or not the Sector Lockdown command is enabled or disabled. If the SLE bit is a Logic 1, then the Sector Lockdown command is still enabled and sectors can be locked down. If the SLE bit is a Logic 0, then the Sector Lockdown command has been disabled and no further sectors can be locked down.

9.4.8 PS2 Bit

The PS2 bit indicates if a program operation has been suspended while using Buffer 2. If the PS2 bit is a Logic 1, then a program operation has been suspended while Buffer 2 was being used, and any command attempts that would modify the contents of Buffer 2 will be ignored.

9.4.9 PS1 Bit

The PS1 bit indicates if a program operation has been suspended while using Buffer 1. If the PS1 bit is a Logic 1, then a program operation has been suspended while Buffer 1 was being used, and any command attempts that would modify the contents of Buffer 1 will be ignored.

9.4.10 The ES bit

The ES bit indicates whether or not an erase has been suspended. If the ES bit is a Logic 1, then an erase operation (page, block, sector, or chip) has been suspended.

10. Deep Power-Down

During normal operation, the device will be placed in the standby mode to consume less power as long as the $\overline{\text{CS}}$ pin remains deasserted and no internal operation is in progress. The Deep Power-Down command offers the ability to place the device into an even lower power consumption state called the Deep Power-Down mode.

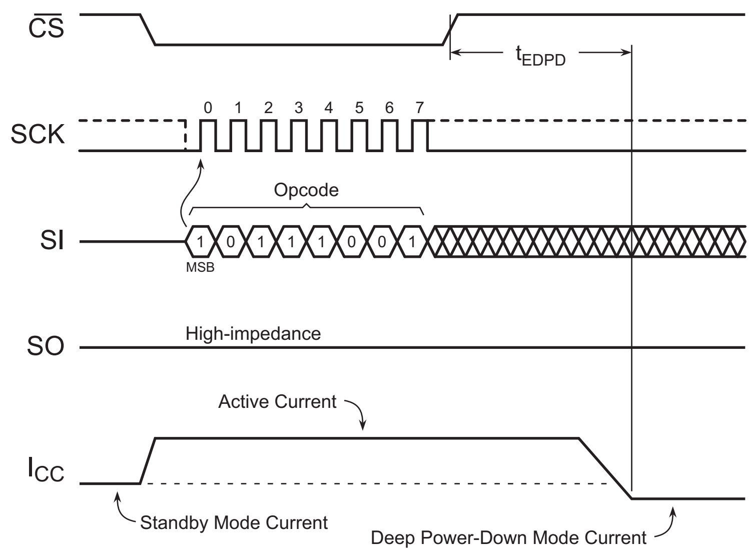
When the device is in the Deep Power-Down mode, all commands including the Status Register Read command will be ignored with the exception of the Resume from Deep Power-Down command. Since all commands will be ignored, the mode can be used as an extra protection mechanism against program and erase operations.

Entering the Deep Power-Down mode is accomplished by simply asserting the $\overline{\text{CS}}$ pin, clocking in the opcode B9h, and then deasserting the $\overline{\text{CS}}$ pin. Any additional data clocked into the device after the opcode will be ignored. When the $\overline{\text{CS}}$ pin is deasserted, the device will enter the Deep Power-Down mode within the maximum time of t_{EDPD}.

The complete opcode must be clocked in before the $\overline{\text{CS}}$ pin is deasserted, and the $\overline{\text{CS}}$ pin must be deasserted on an even byte boundary (multiples of eight bits); otherwise, the device will abort the operation and return to the standby mode once the $\overline{\text{CS}}$ pin is deasserted. In addition, the device will default to the standby mode after a power cycle.

The Deep Power-Down command will be ignored if an internally self-timed operation such as a program or erase cycle is in progress. The Deep Power-Down command must be reissued after the internally self-timed operation has been completed in order for the device to enter the Deep Power-Down mode.

Figure 10-1. Deep Power-Down



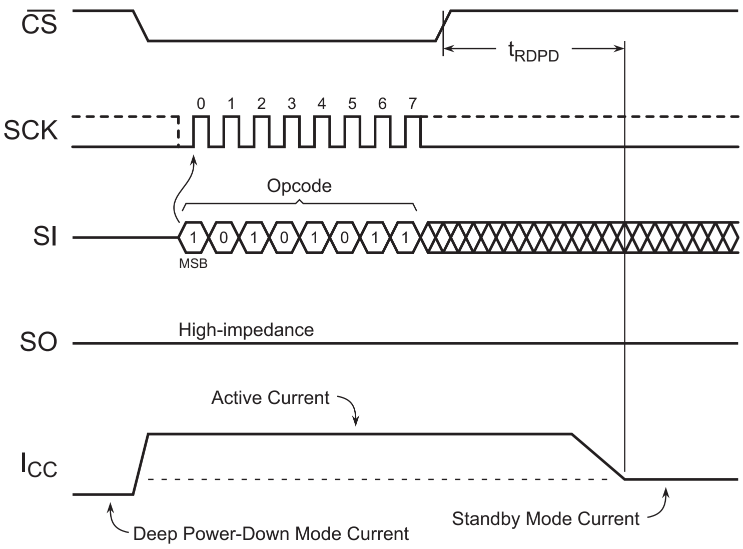
10.1 Resume from Deep Power-Down

In order to exit the Deep Power-Down mode and resume normal device operation, the Resume from Deep Power-Down command must be issued. The Resume from Deep Power-Down command is the only command that the device will recognize while in the Deep Power-Down mode.

To resume from the Deep Power-Down mode, the $\overline{\text{CS}}$ pin must first be asserted and then the opcode ABh must be clocked into the device. Any additional data clocked into the device after the opcode will be ignored. When the $\overline{\text{CS}}$ pin is deasserted, the device will exit the Deep Power-Down mode and return to the standby mode within the maximum time of t_{RDPD}. After the device has returned to the standby mode, normal command operations such as Continuous Array Read can be resumed.

If the complete opcode is not clocked in before the $\overline{\text{CS}}$ pin is deasserted, or if the $\overline{\text{CS}}$ pin is not deasserted on an even byte boundary (multiples of eight bits), then the device will abort the operation and return to the Deep Power-Down mode.

Figure 10-2. Resume from Deep Power-Down



10.2 Ultra-Deep Power-Down

The Ultra-Deep Power-Down mode allows the device to consume far less power compared to the standby and Deep Power-Down modes by shutting down additional internal circuitry. Since almost all active circuitry is shutdown in this mode to conserve power, the contents of the SRAM buffers cannot be maintained. Therefore, any data stored in the SRAM buffers will be lost once the device enters the Ultra-Deep Power-Down mode.

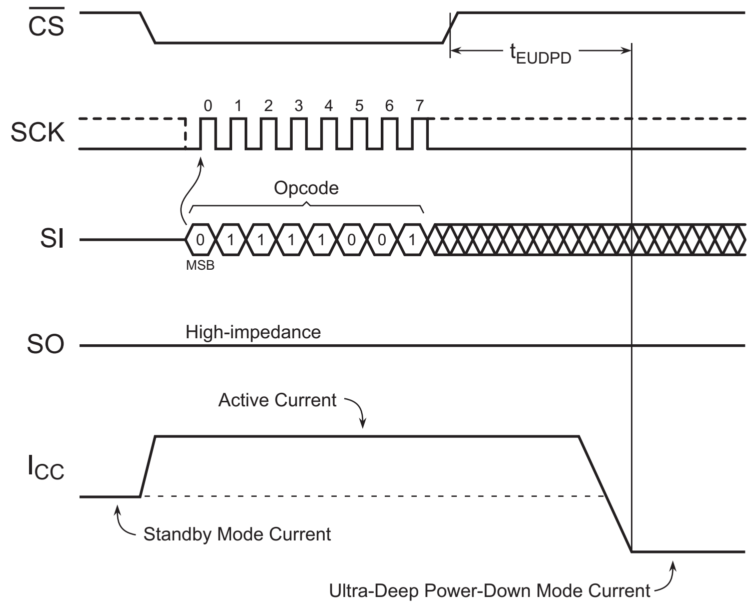
When the device is in the Ultra-Deep Power-Down mode, all commands including the Status Register Read and Resume from Deep Power-Down commands will be ignored. Since all commands will be ignored, the mode can be used as an extra protection mechanism against program and erase operations.

Entering the Ultra-Deep Power-Down mode is accomplished by simply asserting the $\overline{CS}$ pin, clocking in the opcode 79h, and then deasserting the $\overline{CS}$ pin. Any additional data clocked into the device after the opcode will be ignored. When the $\overline{CS}$ pin is deasserted, the device will enter the Ultra-Deep Power-Down mode within the maximum time of t_{EUDPD}.

The complete opcode must be clocked in before the $\overline{CS}$ pin is deasserted, and the $\overline{CS}$ pin must be deasserted on an even byte boundary (multiples of eight bits); otherwise, the device will abort the operation and return to the standby mode once the $\overline{CS}$ pin is deasserted. In addition, the device will default to the standby mode after a power cycle.

The Ultra-Deep Power-Down command will be ignored if an internally self-timed operation such as a program or erase cycle is in progress. The Ultra-Deep Power-Down command must be reissued after the internally self-timed operation has been completed in order for the device to enter the Ultra-Deep Power-Down mode.

Figure 10-3. Ultra-Deep Power-Down

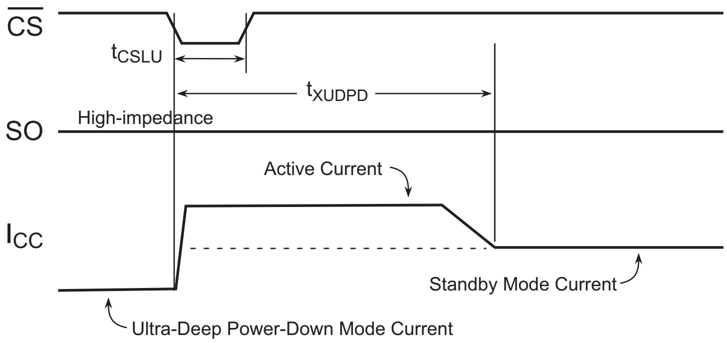


10.2.1 Exit Ultra-Deep Power-Down

To exit from the Ultra-Deep Power-Down mode, the $\overline{CS}$ pin must simply be pulsed by asserting the $\overline{CS}$ pin, waiting the minimum necessary t_{CSLU} time, and then deasserting the $\overline{CS}$ pin again. To facilitate simple software development, a dummy byte opcode can also be entered while the $\overline{CS}$ pin is being pulsed just as in a normal operation like the Program Suspend operation; the dummy byte opcode is simply ignored by the device in this case. After the $\overline{CS}$ pin has been deasserted, the device will exit from the Ultra-Deep Power-Down mode and return to the standby mode within a maximum time of t_{XUDPD}. If the $\overline{CS}$ pin is reasserted before the t_{XUDPD} time has elapsed in an attempt to start a new operation, then that operation will be ignored and nothing will be performed. The system must wait for the device to return to the standby mode before normal command operations such as Continuous Array Read can be resumed.

Since the contents of the SRAM buffers cannot be maintained while in the Ultra-Deep Power-Down mode, the SRAM buffers will contain undefined data when the device returns to the standby mode.

Figure 10-4. Exit Ultra-Deep Power-Down



11. Buffer and Page Size Configuration

The memory array of DataFlash devices is actually larger than other Serial Flash devices in that extra user-accessible bytes are provided in each page of the memory array. For the AT45DB161E, there are an extra 16 bytes of memory in each page for a total of an extra 64KB (512-Kbits) of user-accessible memory. Therefore, the device density is actually 16.5-Mbits instead of 16-Mbits.

Some applications, however, may not want to take advantage of this extra memory and instead architect their software to operate on a “power of 2” binary, logical addressing scheme. To allow this, the DataFlash can be configured so that the buffer and page sizes are 512 bytes instead of the standard 528 bytes. In addition, the configuration of the buffer and page sizes is reversible and can be changed from 528 bytes to 512 bytes or from 512 bytes to 528 bytes. The configured setting is stored in an internal nonvolatile register so that the buffer and page size configuration is not affected by power cycles. The nonvolatile register has a limit of 10,000 erase/program cycles; therefore, care should be taken to not switch between the size options more than 10,000 times.

Devices are initially shipped from Atmel with the buffer and page sizes set to 528 bytes. Devices can be ordered from Atmel pre-configured for the “power of 2” binary size of 512 bytes. For details, see Section 27., Ordering Information on page 63.

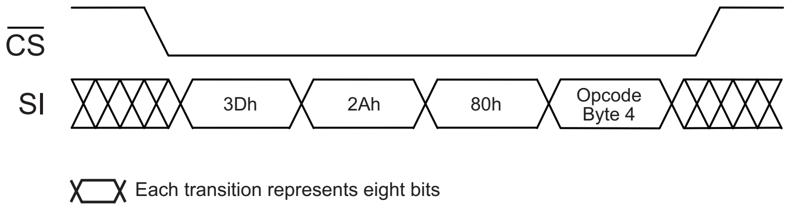
To configure the device for “power of 2” binary page size (512 bytes), a 4-byte opcode sequence of 3Dh, 2Ah, 80h, and A6h must be clocked into the device. After the last bit of the opcode sequence has been clocked in, the $\overline{\text{CS}}$ pin must be deasserted to initiate the internally self-timed configuration process and nonvolatile register program cycle. The programming of the nonvolatile register should take place in a time of t_{EP}, during which time the RDY/$\overline{\text{BUSY}}$ bit in the Status Register will indicate that the device is busy. The device does not need to be power cycled after the completion of the configuration process and register program cycle in order for the buffer and page size to be configured to 512 bytes.

To configure the device for standard DataFlash page size (528 bytes), a 4-byte opcode sequence of 3Dh, 2Ah, 80h, and A7h must be clocked into the device. After the last bit of the opcode sequence has been clocked in, the $\overline{\text{CS}}$ pin must be deasserted to initial the internally self-timed configuration process and nonvolatile register program cycle. The programming of the nonvolatile register should take place in a time of t_{EP}, during which time the RDY/$\overline{\text{BUSY}}$ bit in the Status Register will indicate that the device is busy. The device does not need to be power cycled after the completion of the configuration process and register program cycle in order for the buffer and page size to be configured to 528 bytes.

Table 11-1. Buffer and Page Size Configuration Commands

Command	Byte 1	Byte 2	Byte 3	Byte 4
“Power of 2” binary page size (512 bytes)	3Dh	2Ah	80h	A6h
DataFlash page size (528 bytes)	3Dh	2Ah	80h	A7h

Figure 11-1. Buffer and Page Size Configuration



12. Manufacturer and Device ID Read

Identification information can be read from the device to enable systems to electronically query and identify the device while it is in the system. The identification method and the command opcode comply with the JEDEC Standard for “Manufacturer and Device ID Read Methodology for SPI Compatible Serial Interface Memory Devices”. The type of information that can be read from the device includes the JEDEC-defined Manufacturer ID, the vendor-specific Device ID, and the vendor-specific Extended Device Information.

The Read Manufacturer and Device ID command is limited to a maximum clock frequency of f_{CLK}. Since not all Flash devices are capable of operating at very high clock frequencies, applications should be designed to read the identification information from the devices at a reasonably low clock frequency to ensure that all devices to be used in the application can be identified properly. Once the identification process is complete, the application can then increase the clock frequency to accommodate specific Flash devices that are capable of operating at the higher clock frequencies.

To read the identification information, the $\overline{CS}$ pin must first be asserted and then the opcode 9Fh must be clocked into the device. After the opcode has been clocked in, the device will begin outputting the identification data on the SO pin during the subsequent clock cycles. The first byte to be output will be the Manufacturer ID, followed by two bytes of the Device ID information. The fourth byte output will be the Extended Device Information (EDI) String Length, which will be 01h indicating that one byte of EDI data follows. After the one byte of EDI data is output, the SO pin will go into a high-impedance state; therefore, additional clock cycles will have no affect on the SO pin and no data will be output. As indicated in the JEDEC Standard, reading the EDI String Length and any subsequent data is optional.

Deasserting the $\overline{CS}$ pin will terminate the Manufacturer and Device ID Read operation and put the SO pin into a high-impedance state. The $\overline{CS}$ pin can be deasserted at any time and does not require that a full byte of data be read.

Table 12-1. Manufacturer and Device ID Information

Byte No.	Data Type	Value
1	Manufacturer ID	1Fh
2	Device ID (Byte 1)	26h
3	Device ID (Byte 2)	00h
4	[Optional to Read] Extended Device Information (EDI) String Length	01h
5	[Optional to Read] EDI Byte 1	00h

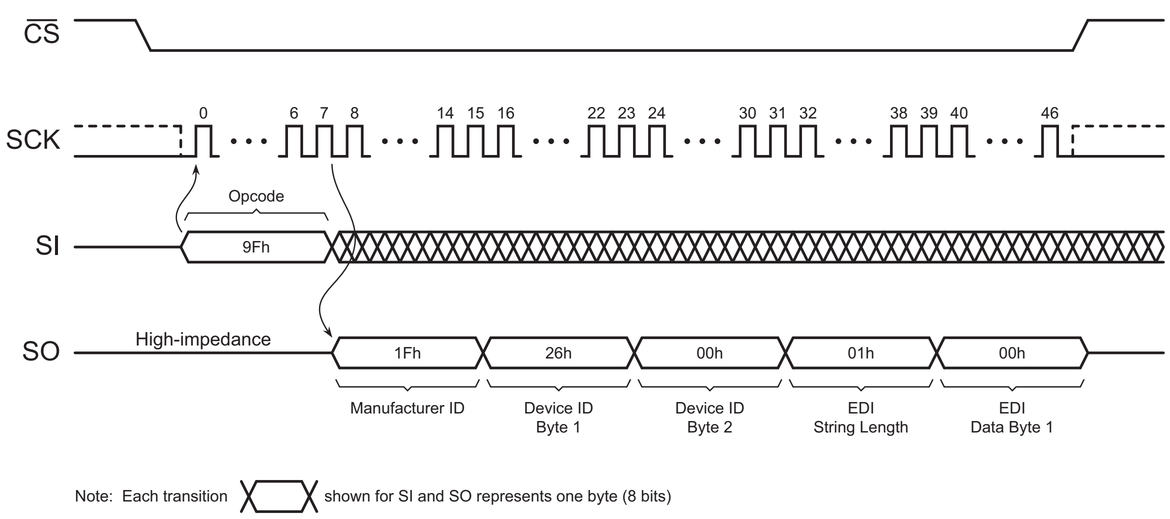
Table 12-2. Manufacturer and Device ID Details

Data Type	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Hex Value	Details
Manufacturer ID	JEDEC Assigned Code								1Fh	JEDEC code: 0001 1111 (1Fh for Atmel)
	0	0	0	1	1	1	1	1		
Device ID (Byte 1)	Family Code			Density Code					26h	Family code: 001 (AT45Dxxx Family) Density code: 00110 (16-Mbit)
	0	0	1	0	0	1	1	0		
Device ID (Byte 2)	Sub Code			Product Variant					00h	Sub code: 000 (Standard Series) Product variant: 00000
	0	0	0	0	0	0	0	0		

Table 12-3. EDI Data

Byte Number	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Hex Value	Details
1	RFU			Device Revision					00h	RFU: Reserved for Future Use Device revision: 00000 (Initial Version)
	0	0	0	0	0	0	0	0		

Figure 12-1. Read Manufacturer and Device ID



13. Software Reset

In some applications, it may be necessary to prematurely terminate a program or erase cycle early rather than wait the hundreds of microseconds or milliseconds necessary for the program or erase operation to complete normally. The Software Reset command allows a program or erase operation in progress to be ended abruptly and returns the device to an idle state.

To perform a Software Reset, the $\overline{CS}$ pin must be asserted and a 4-byte command sequence of F0h, 00h, 00h, and 00h must be clocked into the device. Any additional data clocked into the device after the last byte will be ignored. When the $\overline{CS}$ pin is deasserted, the program or erase operation currently in progress will be terminated within a time t_{SWRST}. Since the program or erase operation may not complete before the device is reset, the contents of the page being programmed or erased cannot be guaranteed to be valid.

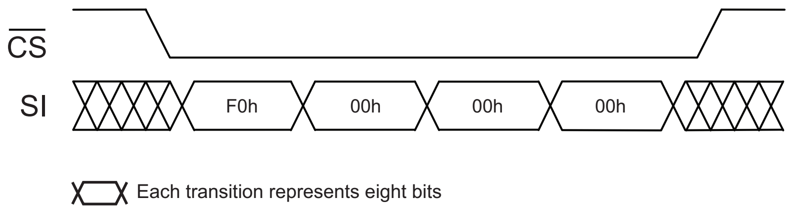
The Software Reset command has no effect on the states of the Sector Protection Register, the Sector Lockdown Register, or the buffer and page size configuration. The PS2, PS1, and ES bits of the Status Register, however, will be reset back to their default states. If a Software Reset operation is performed while a sector is erase suspended, the suspend operation will abort and the contents of the page or block being erased in the suspended sector will be left in an undefined state. If a Software Reset is performed while a sector is program suspended, the suspend operation will abort and the contents of the page that was being programmed and subsequently suspended will be undefined. The remaining pages in the sector will retain their previous contents.

The complete 4-byte opcode must be clocked into the device before the $\overline{CS}$ pin is deasserted, and the $\overline{CS}$ pin must be deasserted on a byte boundary (multiples of eight bits); otherwise, no reset operation will be performed.

Table 13-1. Software Reset

Command	Byte 1	Byte 2	Byte 3	Byte 4
Software Reset	F0h	00h	00h	00h

Figure 13-1. Software Reset



14. Operation Mode Summary

The commands described previously can be grouped into four different categories to better describe which commands can be executed at what times.

Group A commands consist of:

1. Main Memory Page Read
2. Continuous Array Read (SPI)
3. Read Sector Protection Register
4. Read Sector Lockdown Register
5. Read Security Register

Group B commands consist of:

1. Page Erase
2. Block Erase
3. Sector Erase
4. Chip Erase
5. Main Memory Page to Buffer 1 (or 2) Transfer
6. Main Memory Page to Buffer 1 (or 2) Compare
7. Buffer 1 (or 2) to Main Memory Page Program with Built-In Erase
8. Buffer 1 (or 2) to Main Memory Page Program without Built-In Erase
9. Main Memory Page Program through Buffer 1 (or 2) with Built-In Erase
10. Main Memory Byte/Page Program through Buffer 1 without Built-In Erase
11. Auto Page Rewrite

Group C commands consist of:

1. Buffer 1 (or 2) Read
2. Buffer 1 (or 2) Write
3. Status Register Read
4. Manufacturer and Device ID Read

Group D commands consist of:

1. Erase Sector Protection Register
2. Program Sector Protection Register
3. Sector Lockdown
4. Program Security Register
5. Buffer and Page Size Configuration
6. Freeze Sector Lockdown

If a Group A command is in progress (not fully completed), then another command in Group A, B, C, or D should not be started. However, during the internally self-timed portion of Group B commands, any command in Group C can be executed. The Group B commands using Buffer 1 should use Group C commands using Buffer 2 and vice versa. Finally, during the internally self-timed portion of a Group D command, only the Status Register Read command should be executed.

Most of the commands in Group B can be suspended and resumed, except the Buffer Transfer, Buffer Compare, and Auto Page Rewrite operations. If a Group B command is suspended, all of the Group A commands can be executed. See Table 6-4 to determine which of the Group B, Group C, and Group D commands are allowed.

15. Command Tables

Table 15-1. Read Commands

Command	Opcode
Main Memory Page Read	D2h
Continuous Array Read (Low Power Mode)	01h
Continuous Array Read (Low Frequency)	03h
Continuous Array Read (High Frequency)	0Bh
Continuous Array Read (High Frequency)	1Bh
Continuous Array Read (Legacy Command – Not Recommended for New Designs)	E8h
Buffer 1 Read (Low Frequency)	D1h
Buffer 2 Read (Low Frequency)	D3h
Buffer 1 Read (High Frequency)	D4h
Buffer 2 Read (High Frequency)	D6h

Table 15-2. Program and Erase Commands

Command	Opcode
Buffer 1 Write	84h
Buffer 2 Write	87h
Buffer 1 to Main Memory Page Program with Built-In Erase	83h
Buffer 2 to Main Memory Page Program with Built-In Erase	86h
Buffer 1 to Main Memory Page Program without Built-In Erase	88h
Buffer 2 to Main Memory Page Program without Built-In Erase	89h
Main Memory Page Program through Buffer 1 with Built-In Erase	82h
Main Memory Page Program through Buffer 2 with Built-In Erase	85h
Main Memory Byte/Page Program through Buffer 1 without Built-In Erase	02h
Page Erase	81h
Block Erase	50h
Sector Erase	7Ch
Chip Erase	C7h + 94h + 80h + 9Ah
Program/Erase Suspend	B0h
Program/Erase Resume	D0h

Table 15-3. Protection and Security Commands

Command	Opcode
Enable Sector Protection	3Dh + 2Ah + 7Fh + A9h
Disable Sector Protection	3Dh + 2Ah + 7Fh + 9Ah
Erase Sector Protection Register	3Dh + 2Ah + 7Fh + CFh
Program Sector Protection Register	3Dh + 2Ah + 7Fh + FCh
Read Sector Protection Register	32h
Sector Lockdown	3Dh + 2Ah + 7Fh + 30h
Read Sector Lockdown Register	35h
Freeze Sector Lockdown	34h + 55h + AAh + 40h
Program Security Register	9Bh + 00h + 00h + 00h
Read Security Register	77h

Table 15-4. Additional Commands

Command	Opcode
Main Memory Page to Buffer 1 Transfer	53h
Main Memory Page to Buffer 2 Transfer	55h
Main Memory Page to Buffer 1 Compare	60h
Main Memory Page to Buffer 2 Compare	61h
Auto Page Rewrite through Buffer 1	58h
Auto Page Rewrite through Buffer 2	59h
Deep Power-Down	B9h
Resume from Deep Power-Down	ABh
Ultra-Deep Power-Down	79h
Status Register Read	D7h
Manufacturer and Device ID Read	9Fh
Configure “Power of 2” (Binary) Page Size	3Dh + 2Ah + 80h + A6h
Configure Standard DataFlash Page Size	3Dh + 2Ah + 80h + A7h
Software Reset	F0h + 00h + 00h + 00h

Table 15-5. Detailed Bit-level Addressing Sequence for Binary Page Size (512 bytes)

Page Size = 512 bytes									Address Byte								Address Byte								Address Byte								Additional Dummy Bytes
Opcode	Opcode								Reserved	Reserved	Reserved	A20	A19	A18	A17	A16	A15	A14	A13	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0	
01h	0	0	0	0	0	0	0	1	X	X	X	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	N/A
02h	0	0	0	0	0	0	1	0	X	X	X	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	N/A
03h	0	0	0	0	0	0	1	1	X	X	X	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	N/A
0Bh	0	0	0	0	1	0	1	1	X	X	X	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	1
1Bh	0	0	0	1	1	0	1	1	X	X	X	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	2
32h	0	0	1	1	0	0	1	0	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	N/A
35h	0	0	1	1	0	1	0	1	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	N/A
50h	0	1	0	1	0	0	0	0	X	X	X	A	A	A	A	A	A	A	A	A	X	X	X	X	X	X	X	X	X	X	X	X	N/A
53h	0	1	0	1	0	0	1	1	X	X	X	A	A	A	A	A	A	A	A	A	A	A	A	X	X	X	X	X	X	X	X	X	N/A
55h	0	1	0	1	0	1	0	1	X	X	X	A	A	A	A	A	A	A	A	A	A	A	A	X	X	X	X	X	X	X	X	X	N/A
58h	0	1	0	1	1	0	0	0	X	X	X	A	A	A	A	A	A	A	A	A	A	A	A	X	X	X	X	X	X	X	X	X	N/A
59h	0	1	0	1	1	0	0	1	X	X	X	A	A	A	A	A	A	A	A	A	A	A	A	X	X	X	X	X	X	X	X	X	N/A
60h	0	1	1	0	0	0	0	0	X	X	X	A	A	A	A	A	A	A	A	A	A	A	A	X	X	X	X	X	X	X	X	X	N/A
61h	0	1	1	0	0	0	0	1	X	X	X	A	A	A	A	A	A	A	A	A	A	A	A	X	X	X	X	X	X	X	X	X	N/A
77h	0	1	1	1	0	1	1	1	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	N/A
79h	0	1	1	1	1	0	0	1	N/A								N/A								N/A								N/A
7Ch	0	1	1	1	1	1	0	0	X	X	X	A	A	A	A	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	N/A
81h	1	0	0	0	0	0	0	1	X	X	X	A	A	A	A	A	A	A	A	A	A	A	A	X	X	X	X	X	X	X	X	X	N/A
82h	1	0	0	0	0	0	1	0	X	X	X	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	N/A
83h	1	0	0	0	0	0	1	1	X	X	X	A	A	A	A	A	A	A	A	A	A	A	A	X	X	X	X	X	X	X	X	X	N/A
84h	1	0	0	0	0	1	0	0	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	A	A	A	A	A	A	A	A	A	N/A
85h	1	0	0	0	0	1	0	1	X	X	X	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	N/A
86h	1	0	0	0	0	1	1	0	X	X	X	A	A	A	A	A	A	A	A	A	A	A	A	X	X	X	X	X	X	X	X	X	N/A
87h	1	0	0	0	0	1	1	1	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	A	A	A	A	A	A	A	A	A	N/A
88h	1	0	0	0	1	0	0	0	X	X	X	A	A	A	A	A	A	A	A	A	A	A	A	X	X	X	X	X	X	X	X	X	N/A
89h	1	0	0	0	1	0	0	1	X	X	X	A	A	A	A	A	A	A	A	A	A	A	A	X	X	X	X	X	X	X	X	X	N/A
9Fh	1	0	0	1	1	1	1	1	N/A								N/A								N/A								N/A
B9h	1	0	1	1	1	0	0	1	N/A								N/A								N/A								N/A
ABh	1	0	1	0	1	0	1	1	N/A								N/A								N/A								N/A
B0h	1	0	1	1	0	0	0	0	N/A								N/A								N/A								N/A
D0h	1	1	0	1	0	0	0	0	N/A								N/A								N/A								N/A
D1h	1	1	0	1	0	0	0	1	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	A	A	A	A	A	A	A	A	A	N/A
D2h	1	1	0	1	0	0	1	0	X	X	X	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	4
D3h	1	1	0	1	0	0	1	1	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	A	A	A	A	A	A	A	A	A	N/A
D4h	1	1	0	1	0	1	0	0	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	A	A	A	A	A	A	A	A	A	1
D6h	1	1	0	1	0	1	1	0	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	A	A	A	A	A	A	A	A	A	1
D7h	1	1	0	1	0	1	1	1	N/A								N/A								N/A								N/A

Note: X = Dummy Bit

Table 15-6. Detailed Bit-level Addressing Sequence for Standard Atmel DataFlash Page Size (528 bytes)

Page Size = 528-bytes									Address Byte								Address Byte								Address Byte								Additional Dummy Bytes
Opcode	Opcode								Reserved	Reserved	PA11	PA10	PA9	PA8	PA7	PA6	PA5	PA4	PA3	PA2	PA1	PA0	BA9	BA8	BA7	BA6	BA5	BA4	BA3	BA2	BA1	BA0	
01h	0	0	0	0	0	0	0	1	X	X	P	P	P	P	P	P	P	P	P	P	P	P	B	B	B	B	B	B	B	B	B	B	N/A
02h	0	0	0	0	0	0	1	0	X	X	P	P	P	P	P	P	P	P	P	P	P	P	B	B	B	B	B	B	B	B	B	B	N/A
03h	0	0	0	0	0	0	1	1	X	X	P	P	P	P	P	P	P	P	P	P	P	P	B	B	B	B	B	B	B	B	B	B	N/A
0Bh	0	0	0	0	1	0	1	1	X	X	P	P	P	P	P	P	P	P	P	P	P	P	B	B	B	B	B	B	B	B	B	B	1
1Bh	0	0	0	1	1	0	1	1	X	X	P	P	P	P	P	P	P	P	P	P	P	P	B	B	B	B	B	B	B	B	B	B	2
32h	0	0	1	1	0	0	1	0	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	N/A
35h	0	0	1	1	0	1	0	1	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	N/A
50h	0	1	0	1	0	0	0	0	X	X	P	P	P	P	P	P	P	P	P	X	X	X	X	X	X	X	X	X	X	X	X	X	N/A
53h	0	1	0	1	0	0	1	1	X	X	P	P	P	P	P	P	P	P	P	P	P	P	X	X	X	X	X	X	X	X	X	X	N/A
55h	0	1	0	1	0	1	0	1	X	X	P	P	P	P	P	P	P	P	P	P	P	P	X	X	X	X	X	X	X	X	X	X	N/A
58h	0	1	0	1	1	0	0	0	X	X	P	P	P	P	P	P	P	P	P	P	P	P	X	X	X	X	X	X	X	X	X	X	N/A
59h	0	1	0	1	1	0	0	1	X	X	P	P	P	P	P	P	P	P	P	P	P	P	X	X	X	X	X	X	X	X	X	X	N/A
60h	0	1	1	0	0	0	0	0	X	X	P	P	P	P	P	P	P	P	P	P	P	P	X	X	X	X	X	X	X	X	X	X	N/A
61h	0	1	1	0	0	0	0	1	X	X	P	P	P	P	P	P	P	P	P	P	P	P	X	X	X	X	X	X	X	X	X	X	N/A
77h	0	1	1	1	0	1	1	1	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	N/A
79h	0	1	1	1	1	0	0	1	N/A								N/A								N/A								N/A
7Ch	0	1	1	1	1	1	0	0	X	X	P	P	P	P	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	N/A
81h	1	0	0	0	0	0	0	1	X	X	P	P	P	P	P	P	P	P	P	P	P	P	X	X	X	X	X	X	X	X	X	X	N/A
82h	1	0	0	0	0	0	1	0	X	X	P	P	P	P	P	P	P	P	P	P	P	P	B	B	B	B	B	B	B	B	B	B	N/A
83h	1	0	0	0	0	0	1	1	X	X	P	P	P	P	P	P	P	P	P	P	P	P	X	X	X	X	X	X	X	X	X	X	N/A
84h	1	0	0	0	0	1	0	0	X	X	X	X	X	X	X	X	X	X	X	X	X	X	B	B	B	B	B	B	B	B	B	B	N/A
85h	1	0	0	0	0	1	0	1	X	X	P	P	P	P	P	P	P	P	P	P	P	P	B	B	B	B	B	B	B	B	B	B	N/A
86h	1	0	0	0	0	1	1	0	X	X	P	P	P	P	P	P	P	P	P	P	P	P	X	X	X	X	X	X	X	X	X	X	N/A
87h	1	0	0	0	0	1	1	1	X	X	X	X	X	X	X	X	X	X	X	X	X	X	B	B	B	B	B	B	B	B	B	B	N/A
88h	1	0	0	0	1	0	0	0	X	X	P	P	P	P	P	P	P	P	P	P	P	P	X	X	X	X	X	X	X	X	X	X	N/A
89h	1	0	0	0	1	0	0	1	X	X	P	P	P	P	P	P	P	P	P	P	P	P	X	X	X	X	X	X	X	X	X	X	N/A
9Fh	1	0	0	1	1	1	1	1	N/A								N/A								N/A								N/A
B9h	1	0	1	1	1	0	0	1	N/A								N/A								N/A								N/A
ABh	1	0	1	0	1	0	1	1	N/A								N/A								N/A								N/A
B0h	1	0	1	1	0	0	0	0	N/A								N/A								N/A								N/A
D0h	1	1	0	1	0	0	0	0	N/A								N/A								N/A								N/A
D1h	1	1	0	1	0	0	0	1	X	X	X	X	X	X	X	X	X	X	X	X	X	X	B	B	B	B	B	B	B	B	B	B	N/A
D2h	1	1	0	1	0	0	1	0	X	X	P	P	P	P	P	P	P	P	P	P	P	P	B	B	B	B	B	B	B	B	B	B	4
D3h	1	1	0	1	0	0	0	1	X	X	X	X	X	X	X	X	X	X	X	X	X	X	B	B	B	B	B	B	B	B	B	B	N/A
D4h	1	1	0	1	0	1	0	0	X	X	X	X	X	X	X	X	X	X	X	X	X	X	B	B	B	B	B	B	B	B	B	B	1
D6h	1	1	0	1	0	1	1	0	X	X	X	X	X	X	X	X	X	X	X	X	X	X	B	B	B	B	B	B	B	B	B	B	1
D7h	1	1	0	1	0	1	1	1	N/A								N/A								N/A								N/A

Note: P = Page Address Bit B = Byte/Buffer Address Bit X = Dummy Bit

16. Power-On/Reset State

When power is first applied to the device, or when recovering from a reset condition, the device will default to SPI Mode 3. In addition, the output pin (SO) will be in a high impedance state, and a high-to-low transition on the $\overline{CS}$ pin will be required to start a valid instruction. The SPI mode (Mode 3 or Mode 0) will be automatically selected on every falling edge of $\overline{CS}$ by sampling the inactive clock state.

16.1 Initial Power-Up Timing Restrictions

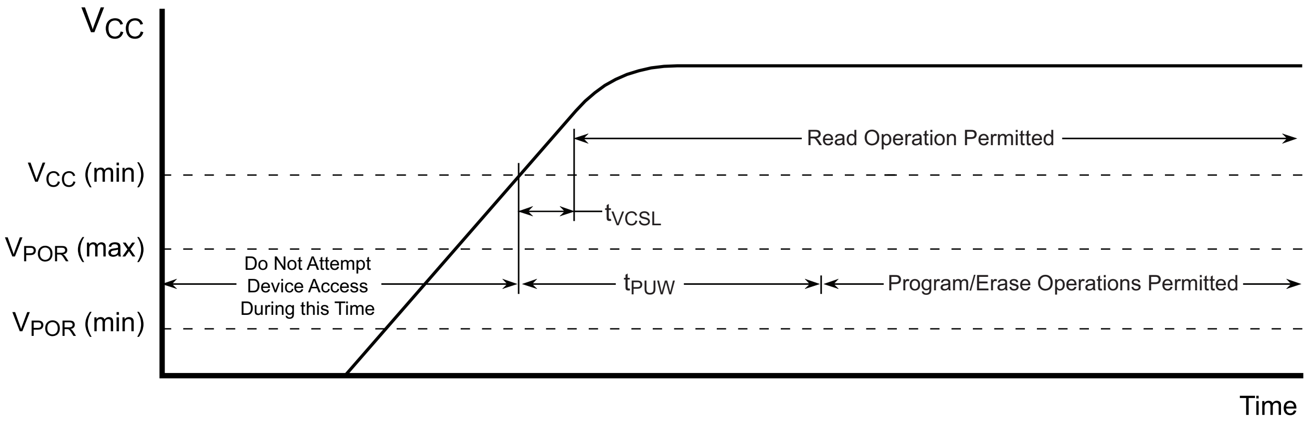
During power-up, the device must not be accessed for at least the minimum t_{VCSL} time after the supply voltage reaches the minimum V_{CC} level. While the device is being powered-up, the internal Power-On Reset (POR) circuitry keeps the device in a reset mode until the supply voltage rises above the maximum POR threshold value (V_{POR}). During this time, all operations are disabled and the device will not respond to any commands. After power-up, the device will be in the standby mode.

If the first operation to the device after power-up will be a program or erase operation, then the operation cannot be started until the supply voltage reaches the minimum V_{CC} level and an internal device delay has elapsed. This delay will be a maximum time of t_{PUW}.

Table 16-1. Power-Up Timing

Symbol	Parameter	Min	Max	Units
t_{VCSL}	Minimum V_{CC} to Chip Select Low Time	70		µs
t_{PUW}	Power-Up Device Delay Before Program or Erase Allowed		5	ms
V_{POR}	Power-On Reset (POR) Voltage	1.5	2.2	V

Figure 16-1. Power-Up Timing



VCC
VCC (min)
VPOR (max)
VPOR (min)
Read Operation Permitted
tVCSL
Do Not Attempt Device Access During this Time
tPUW
Program/Erase Operations Permitted
Time

17. System Considerations

The serial interface is controlled by the Serial Clock (SCK), Serial Input (SI), and Chip Select ($\overline{CS}$) pins. These signals must rise and fall monotonically and be free from noise. Excessive noise or ringing on these pins can be misinterpreted as multiple edges and cause improper operation of the device. PCB traces must be kept to a minimum distance or appropriately terminated to ensure proper operation. If necessary, decoupling capacitors can be added on these pins to provide filtering against noise glitches.

As system complexity continues to increase, voltage regulation is becoming more important. A key element of any voltage regulation scheme is its current sourcing capability. Like all Flash memories, the peak current for DataFlash devices occurs during the programming and erasing operations. The supply voltage regulator needs to be able to supply this peak current requirement. An under specified regulator can cause current starvation. Besides increasing system noise, current starvation during programming or erasing can lead to improper operation and possible data corruption.

18. Electrical Specifications

18.1 Absolute Maximum Ratings*

Temperature under Bias	-55°C to +125°C
Storage Temperature	-65°C to +150°C
All Input Voltages (except V_{CC} but including NC pins) with Respect to Ground	-0.6V to +6.25V
All Output Voltages with Respect to Ground	-0.6V to V_{CC} + 0.6V

*Notice: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. The "Absolute Maximum Ratings" are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Voltage extremes referenced in the "Absolute Maximum Ratings" are intended to accommodate short duration undershoot/overshoot conditions and does not imply or guarantee functional device operation at these levels for any extended period of time.

18.2 DC and AC Operating Range

		Atmel AT45DB161E 2.3V Version	Atmel AT45DB161E 2.5V Version
Operating Temperature (Case)	Industrial	-40°C to 85°C	-40°C to 85°C
V_{CC} Power Supply		2.3V to 3.6V	2.5V to 3.6V

18.3 DC Characteristics

Symbol	Parameter	Condition	Min	Typ	Max	Units
I_{UDPD}	Ultra-Deep Power-Down Current	All inputs at 0V or V_{CC}		0.4	1	µA
I_{DPD}	Deep Power-Down Current	$\overline{CS}$, $\overline{RESET}$, $\overline{WP}$ = V_{IH} All inputs at CMOS levels		3	10	µA
I_{SB}	Standby Current	$\overline{CS}$, $\overline{RESET}$, $\overline{WP}$ = V_{IH} All inputs at CMOS levels		25	50	µA
I_{CC1}	Active Current, Low Power Read (01h) Operation	f = 1MHz; I_{OUT} = 0mA; V_{CC} = 3.6V		6	8	mA
		f = 10MHz; I_{OUT} = 0mA; V_{CC} = 3.6V		6.5	9	mA
		f = 20MHz; I_{OUT} = 0mA; V_{CC} = 3.6V		7.5	10	mA
I_{CC2}[1][2]	Active Current, Read Operation	f = 20MHz; I_{OUT} = 0mA; V_{CC} = 3.6V		11	14	mA
		f = 33MHz; I_{OUT} = 0mA; V_{CC} = 3.6V		12	16	mA
		f = 50MHz; I_{OUT} = 0mA; V_{CC} = 3.6V		13	19	mA
		f = 85MHz; I_{OUT} = 0mA; V_{CC} = 3.6V		16	26	mA
I_{CC3}	Active Current, Program Operation	V_{CC} = 3.6V		12	18	mA
I_{CC4}	Active Current, Erase Operation	V_{CC} = 3.6V		14	20	mA
I_{LI}	Input Load Current	All inputs at CMOS levels			1	µA
I_{LO}	Output Leakage Current	All inputs at CMOS levels			1	µA
V_{IL}	Input Low Voltage				V_{CC} x 0.3	V
V_{IH}	Input High Voltage		V_{CC} x 0.7			V
V_{OL}	Output Low Voltage	I_{OL} = 1.6mA; V_{CC} = 2.5V			0.4	V
V_{OH}	Output High Voltage	I_{OH} = -100µA	V_{CC} - 0.2V			V

Notes:
1. Typical values measured at 3.0V at 25°C.
2. I_{CC2} during a Buffer Read is 20mA maximum @ 20MHz.
3. All inputs (SI, SCK, $\overline{CS}$, $\overline{WP}$, and $\overline{RESET}$) are guaranteed by design to be 5V tolerant.

18.4 AC Characteristics

Symbol	Parameter	Atmel AT45DB161E 2.3V Version		Atmel AT45DB161E 2.5V Version		Units
		Min	Max	Min	Max	
f_{SCK}	SCK Frequency		70		85	MHz
f_{CAR1}	SCK Frequency for Continuous Read		70		85	MHz
f_{CAR2}	SCK Frequency for Continuous Read (Low Frequency)		40		50	MHz
f_{CAR3}	SCK Frequency for Continuous Read (Low Power Mode – 01h Opcode)		20		20	MHz
t_{WH}	SCK High Time	6.4		5.2		ns
t_{WL}	SCK Low Time	6.4		5.2		ns
t_{SCKR}(1)	SCK Rise Time, Peak-to-peak	0.1		0.1		V/ns
t_{SCKF}(1)	SCK Fall Time, Peak-to-peak	0.1		0.1		V/ns
t_{CS}	Minimum $\overline{\text{CS}}$ High Time	30		30		ns
t_{CSS}	$\overline{\text{CS}}$ Setup Time	5		5		ns
t_{CSH}	$\overline{\text{CS}}$ Hold Time	5		5		ns
t_{SU}	Data In Setup Time	2		2		ns
t_{H}	Data In Hold Time	1		1		ns
t_{HO}	Output Hold Time	0		0		ns
t_{DIS}	Output Disable Time		7		6	ns
t_{V}	Output Valid		7		6	ns
t_{WPE}	$\overline{\text{WP}}$ Low to Protection Enabled		1		1	µs
t_{WPD}	$\overline{\text{WP}}$ High to Protection Disabled		1		1	µs
t_{LOCK}	Freeze Sector Lockdown Time (from $\overline{\text{CS}}$ High)		200		200	µs
t_{EUDPD}	$\overline{\text{CS}}$ High to Ultra-Deep Power-Down		3		3	µs
t_{CSLU}	Minimum $\overline{\text{CS}}$ Low Time to Exit Ultra-Deep Power-Down	20		20		ns
t_{XUDPD}	Exit Ultra-Deep Power-Down Time		120		120	µs
t_{EDPD}	$\overline{\text{CS}}$ High to Deep Power-Down		3		3	µs
t_{RDPD}	Resume from Deep Power-Down Time		35		35	µs
t_{XFR}	Page to Buffer Transfer Time		200		200	µs
t_{COMP}	Page to Buffer Compare Time		220		220	µs
t_{RST}	$\overline{\text{RESET}}$ Pulse Width	10		10		µs
t_{REC}	$\overline{\text{RESET}}$ Recovery Time		1		1	µs
t_{SWRST}	Software Reset Time		30		30	µs

Note: 1. Values are based on device characterization, not 100% tested in production.

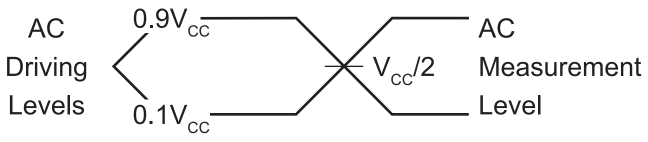
18.5 Program and Erase Characteristics

Symbol	Parameter		Min	Typ	Max	Units
t_{EP}	Page Erase and Programming Time (512/528 bytes)			15	40	ms
t_P	Page Programming Time			3	6	ms
t_{BP}	Byte Programming Time			8		µs
t_{PE}	Page Erase Time			12	35	ms
t_{BE}	Block Erase Time			45	100	ms
t_{SE}	Sector Erase Time			1.4	3.5	s
t_{CE}	Chip Erase Time			22	40	s
t_{SUSP}	Suspend Time	Program		10	20	µs
		Erase		20	40	
t_{RES}	Resume Time	Program		10	20	µs
		Erase		20	40	
t_{OTPP}	OTP Security Register Program Time			200	500	µs

Notes: 1. Values are based on device characterization, not 100% tested in production.

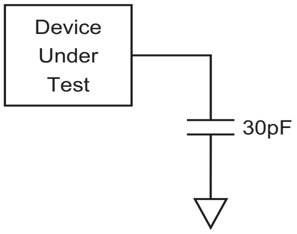
2. Not 100% tested (value guaranteed by design and characterization).

19. Input Test Waveforms and Measurement Levels



t_R, t_F < 2ns (10% to 90%)

20. Output Test Load

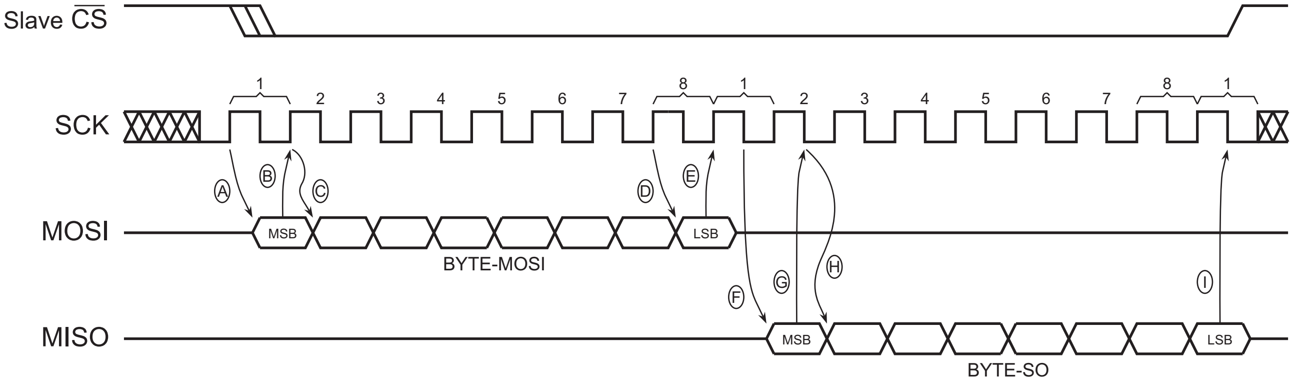


21. Utilizing the Atmel RapidS Function

To take advantage of the RapidS function's ability to operate at higher clock frequencies, a full clock cycle must be used to transmit data back and forth across the serial bus. The DataFlash is designed to always clock its data out on the falling edge of the SCK signal and clock data in on the rising edge of SCK.

For full clock cycle operation to be achieved, when the DataFlash is clocking data out on the falling edge of SCK, the host controller should wait until the next falling edge of SCK to latch the data in. Similarly, the host controller should clock its data out on the rising edge of SCK in order to give the DataFlash a full clock cycle to latch the incoming data in on the next rising edge of SCK.

Figure 21-1. Atmel RapidS Mode



MOSI = Master Out, Slave In
MISO = Master In, Slave Out
The Master is the host controller and the Slave is the Atmel DataFlash.

The Master always clocks data out on the rising edge of SCK and always clocks data in on the falling edge of SCK.
The Slave always clocks data out on the falling edge of SCK and always clocks data in on the rising edge of SCK.

A. Master clocks out first bit of BYTE-MOSI on the rising edge of SCK
B. Slave clocks in first bit of BYTE-MOSI on the next rising edge of SCK
C. Master clocks out second bit of BYTE-MOSI on the same rising edge of SCK
D. Last bit of BYTE-MOSI is clocked out from the Master
E. Last bit of BYTE-MOSI is clocked into the slave
F. Slave clocks out first bit of BYTE-SO
G. Master clocks in first bit of BYTE-SO
H. Slave clocks out second bit of BYTE-SO
I. Master clocks in last bit of BYTE-SO

Figure 21-2. Command Sequence for Read/Write Operations for Page Size 512 bytes
(Except Status Register Read, Manufacturer and Device ID Read)

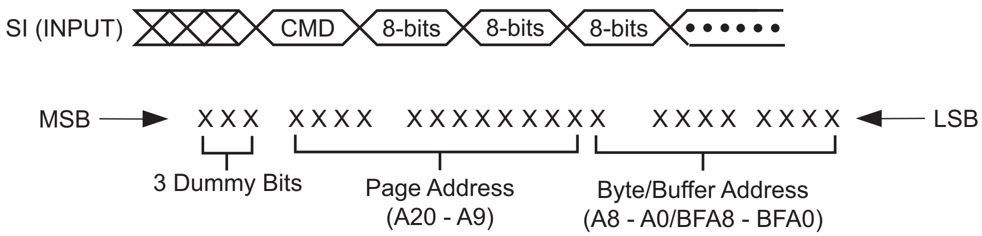
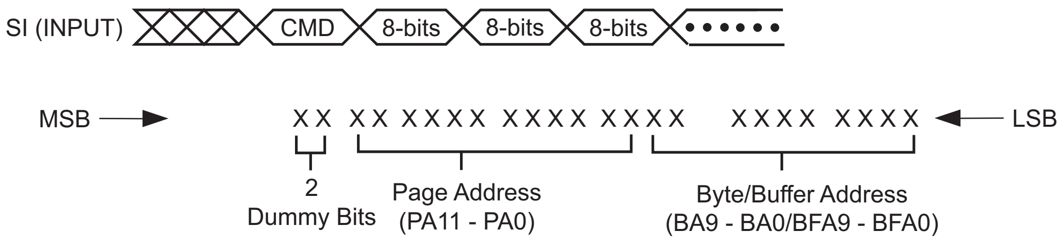


Figure 21-3. Command Sequence for Read/Write Operations for Page Size 528 bytes
(Except Status Register Read, Manufacturer and Device ID Read)



22. AC Waveforms

Four different timing waveforms are shown in Figure 22-1 through Figure 22-4. Waveform 1 shows the SCK signal being low when $\overline{CS}$ makes a high-to-low transition and Waveform 2 shows the SCK signal being high when $\overline{CS}$ makes a high-to-low transition. In both cases, output SO becomes valid while the SCK signal is still low (SCK low time is specified as t_{WL}). Timing Waveforms 1 and 2 conform to RapidS serial interface but for frequencies up to 85MHz. Waveforms 1 and 2 are compatible with SPI Mode 0 and SPI Mode 3, respectively.

Waveform 3 and 4 illustrate general timing diagram for RapidS serial interface. These are similar to Waveform 1 and 2, except that output SO is not restricted to become valid during the t_{WL} period. These timing waveforms are valid over the full frequency range (maximum frequency = 85MHz) of the RapidS serial case.

Figure 22-1. Waveform 1 = SPI Mode 0 Compatible

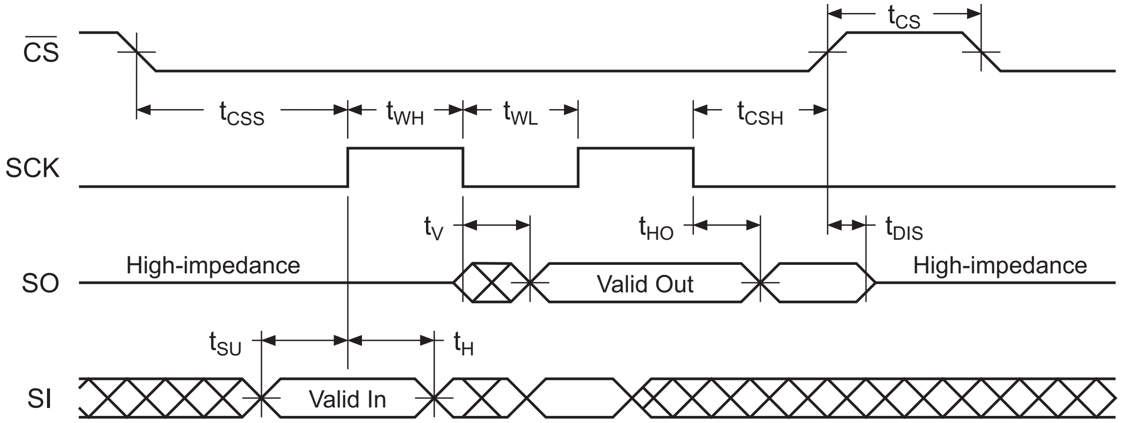


Figure 22-2. Waveform 2 = SPI Mode 3 Compatible

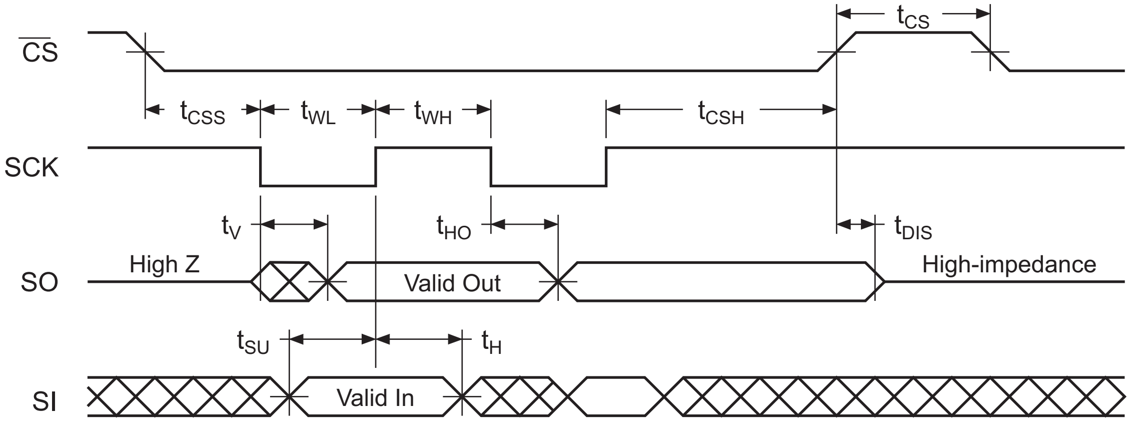


Figure 22-3. Waveform 3 = Atmel RapidS Mode 0

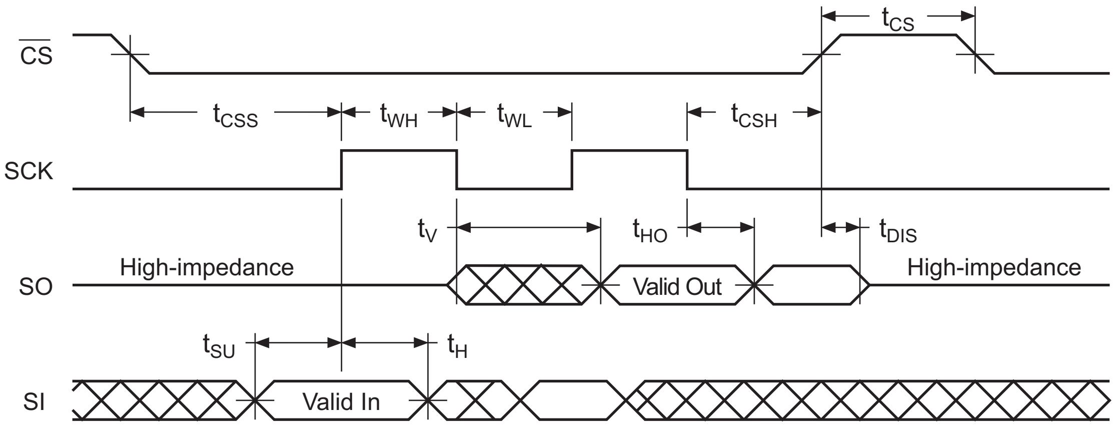
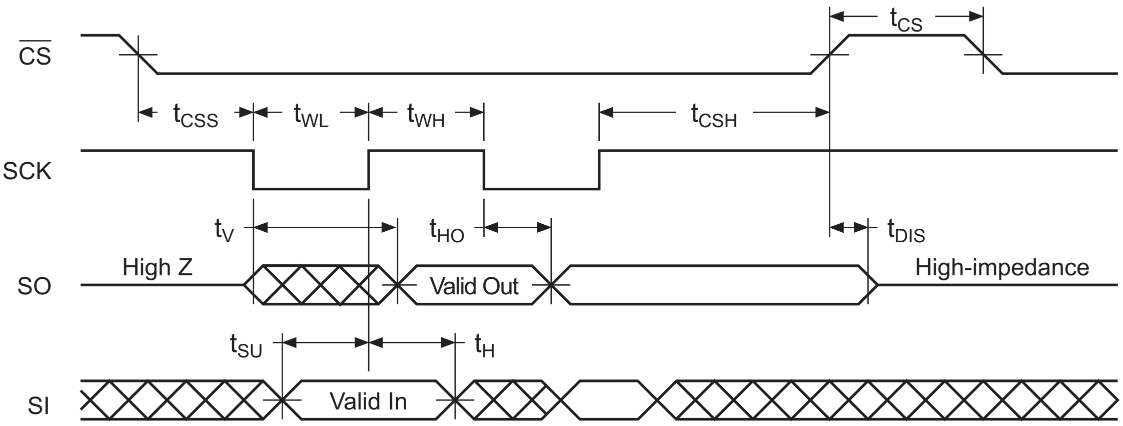


Figure 22-4. Waveform 4 = Atmel RapidS Mode 3



23. Write Operations

The following block diagram and waveforms illustrate the various write sequences available.

Figure 23-1. Block Diagram

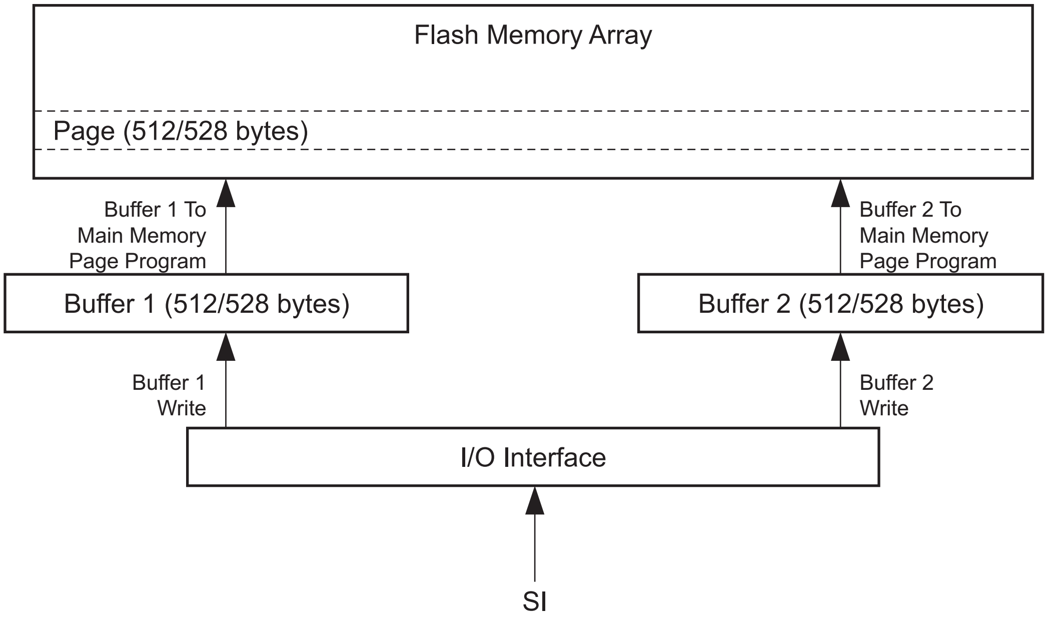


Figure 23-2. Buffer Write

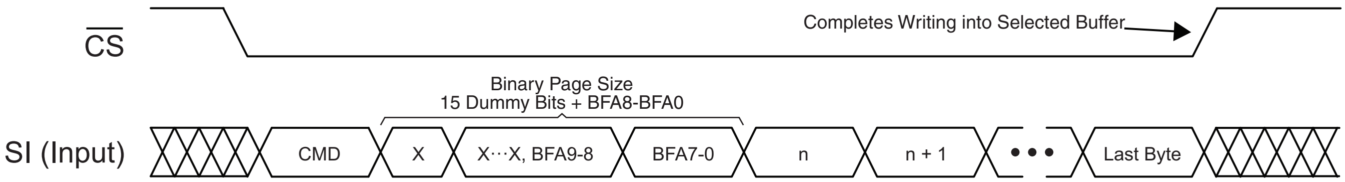
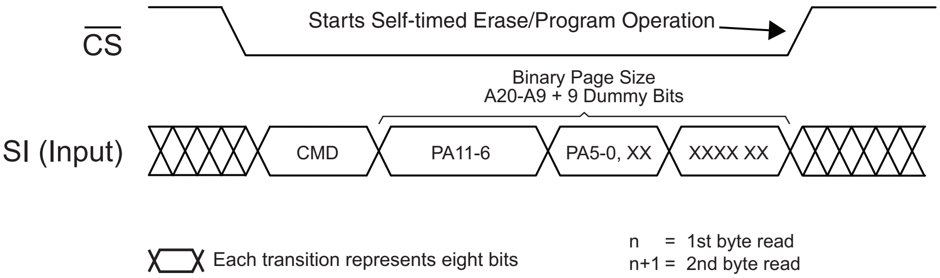


Figure 23-3. Buffer to Main Memory Page Program



24. Read Operations

The following block diagram and waveforms illustrate the various read sequences available.

Figure 24-1. Block Diagram

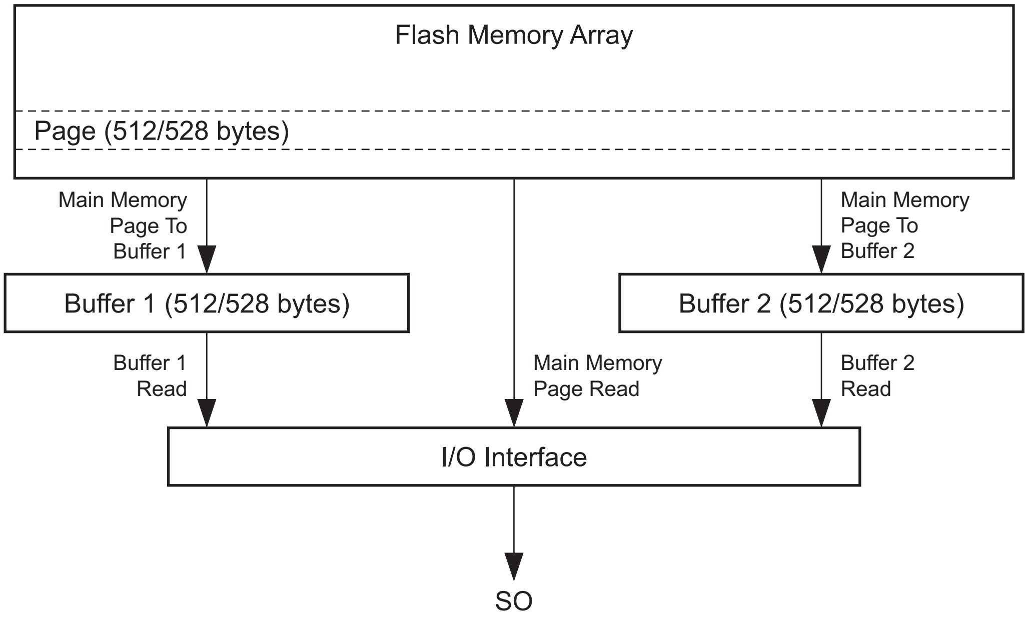


Figure 24-2. Main Memory Page Read

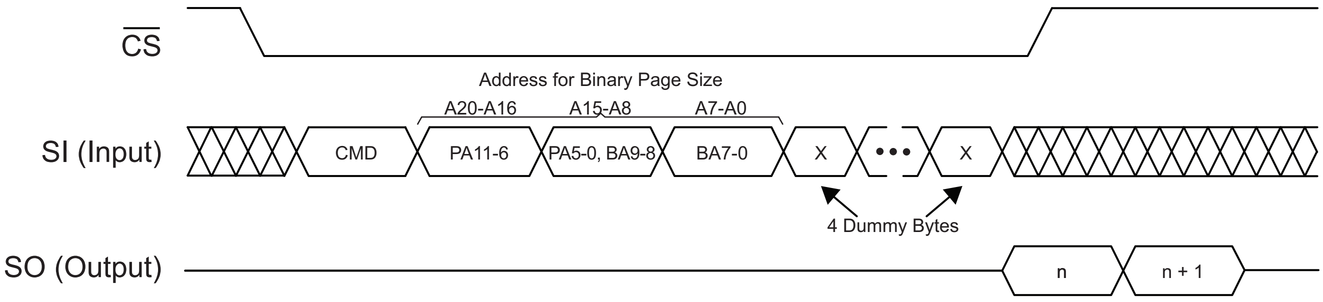


Figure 24-3. Main Memory Page to Buffer Transfer
Data From the selected Flash Page is read into either SRAM Buffer

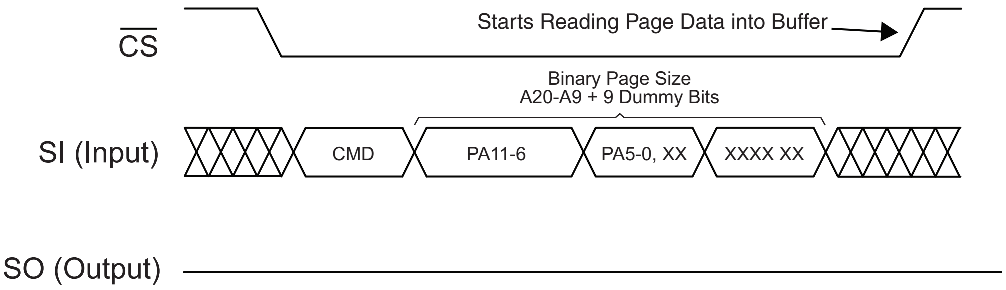
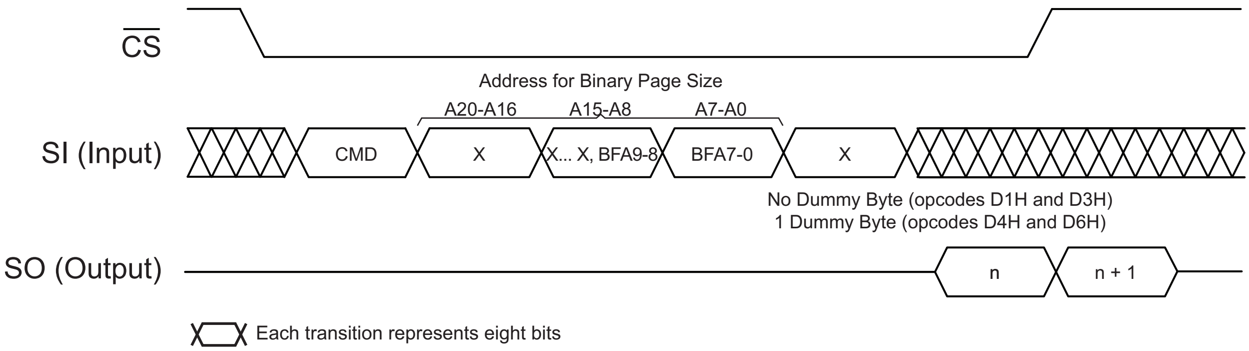


Figure 24-4. Buffer Read


CS
Address for Binary Page Size
A20-A16
A15-A8
A7-A0
SI (Input)
CMD
X
X... X, BFA9-8
BFA7-0
X
No Dummy Byte (opcodes D1H and D3H)
1 Dummy Byte (opcodes D4H and D6H)
SO (Output)
n
n + 1
Each transition represents eight bits

25. Detailed Bit-level Read Waveforms: Atmel RapidS Mode 0/Mode 3

Figure 25-1. Continuous Array Read (Legacy Opcode E8h)

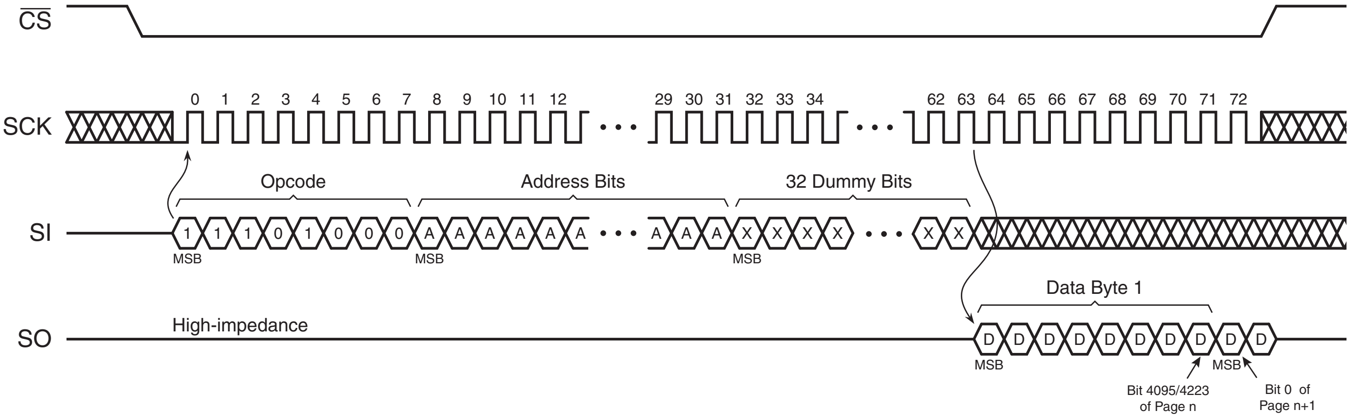


Figure 25-2. Continuous Array Read (Opcode 0Bh)

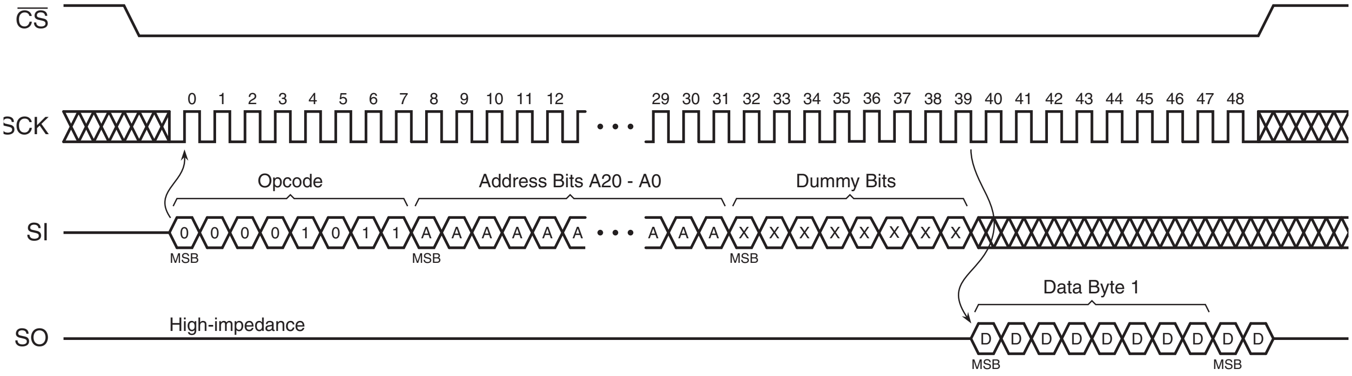


Figure 25-3. Continuous Array Read (Opcode 01h or 03h)

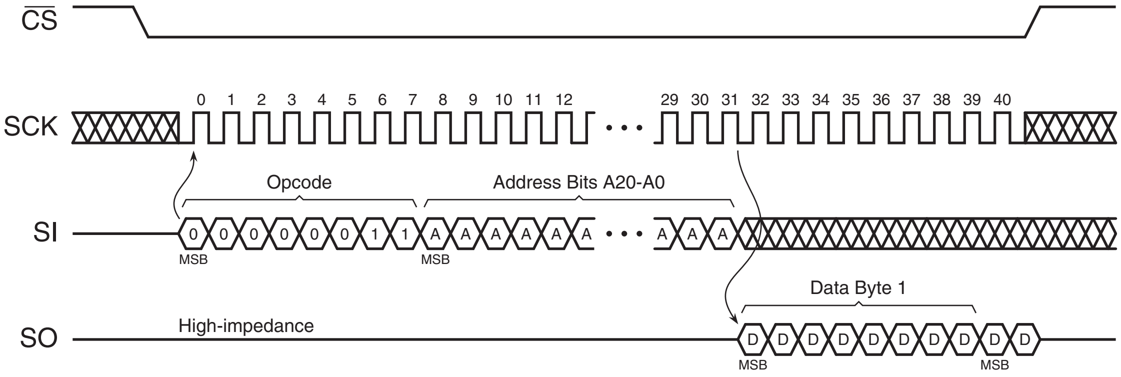


Figure 25-4. Main Memory Page Read (Opcode D2h)

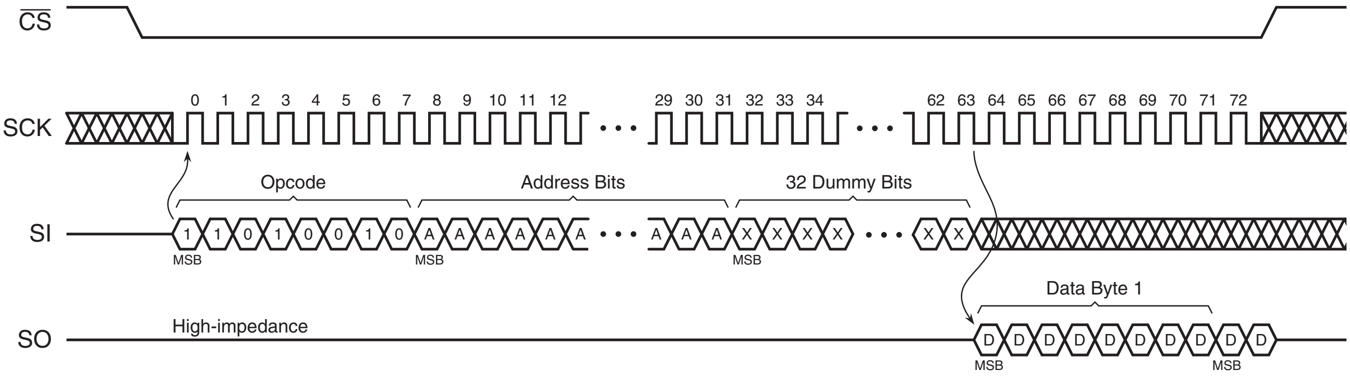


Figure 25-5. Buffer Read (Opcode D4h or D6h)

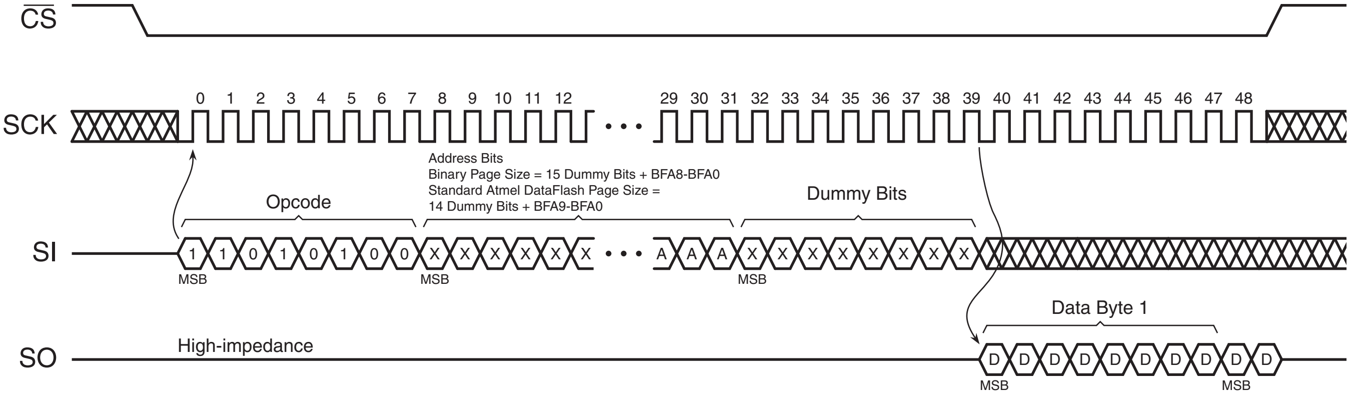


Figure 25-6. Buffer Read – Low Frequency (Opcode D1h or D3h)

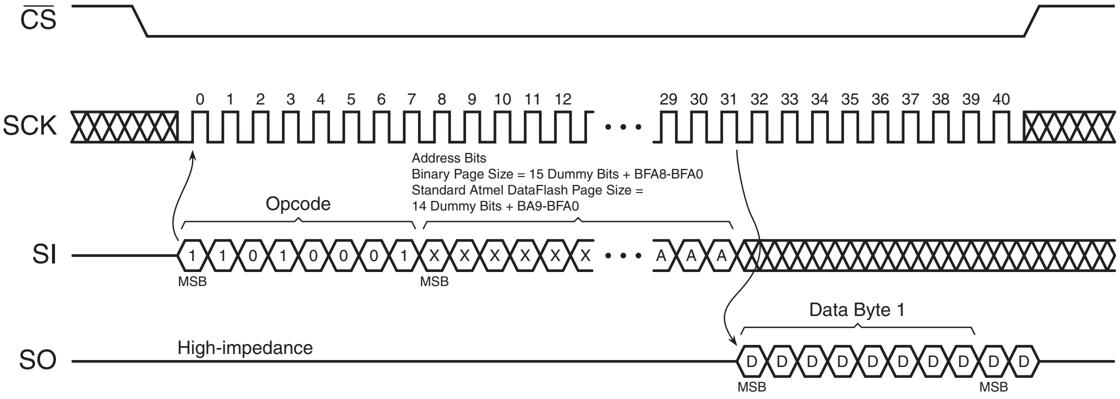


Figure 25-7. Read Sector Protection Register (Opcode 32h)

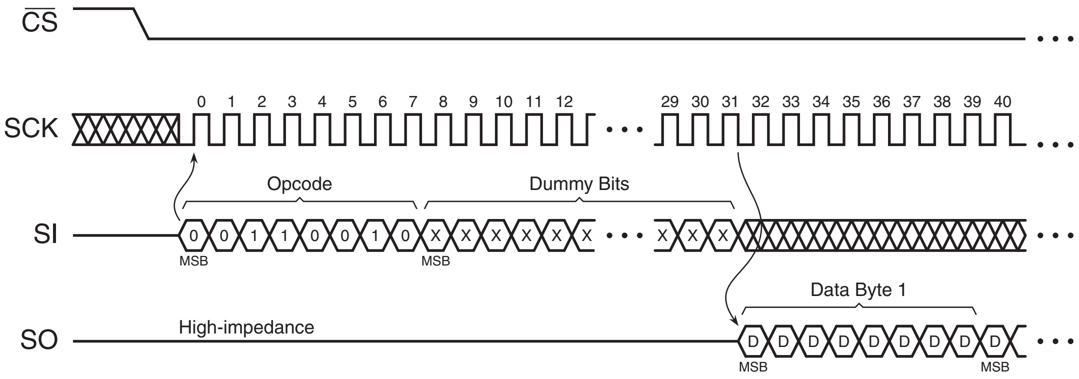


Figure 25-8. Read Sector Lockdown Register (Opcode 35h)

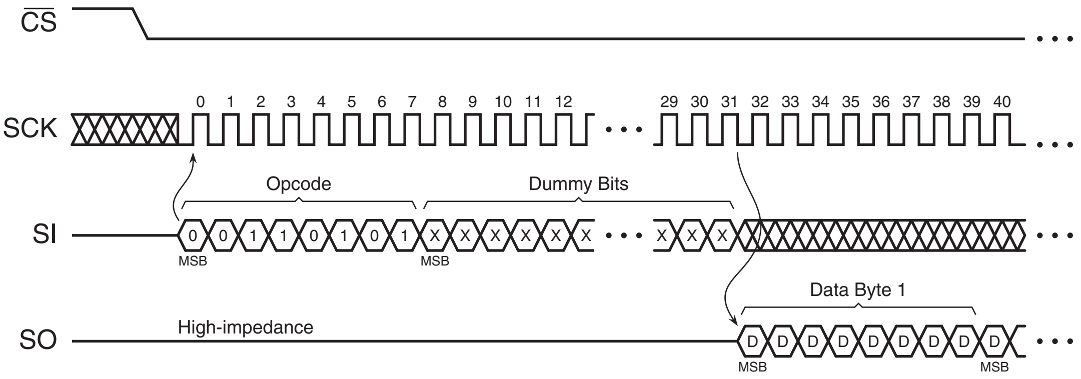


Figure 25-9. Read Security Register (Opcode 77h)

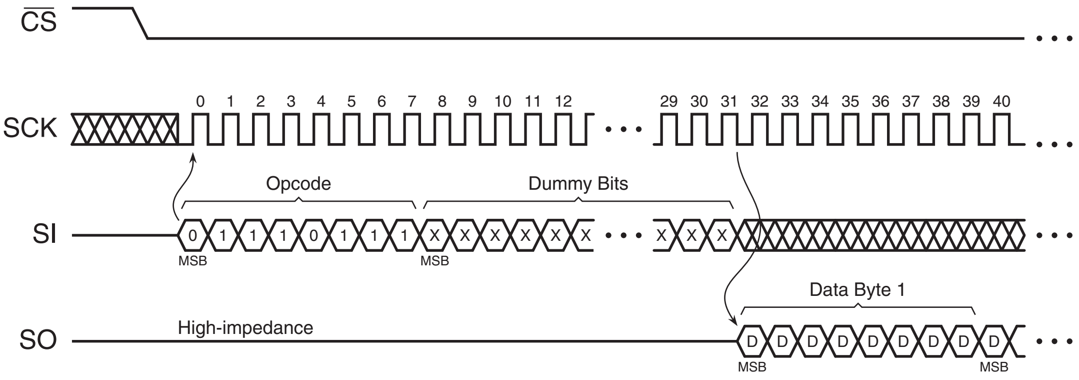


Figure 25-10. Status Register Read (Opcode D7h)

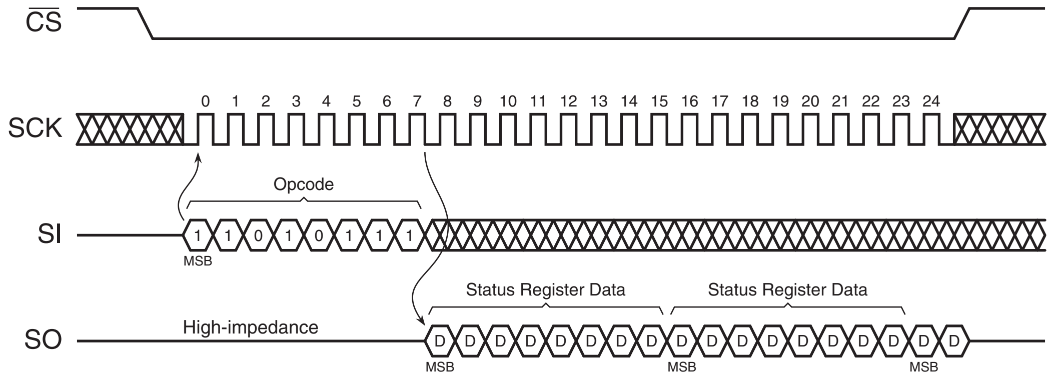
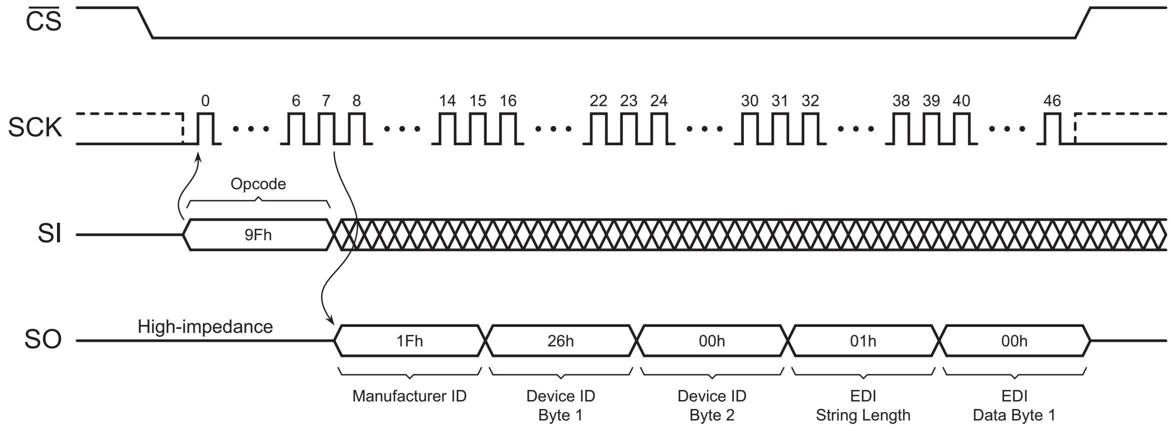
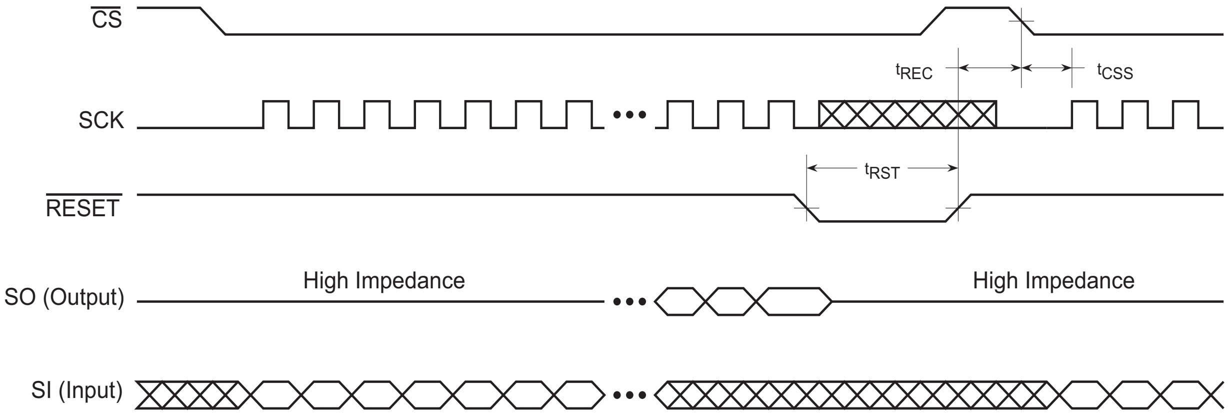


Figure 25-11. Manufacturer and Device Read (Opcode 9Fh)



Note: Each transition ⟩⟨ shown for SI and SO represents one byte (8 bits)

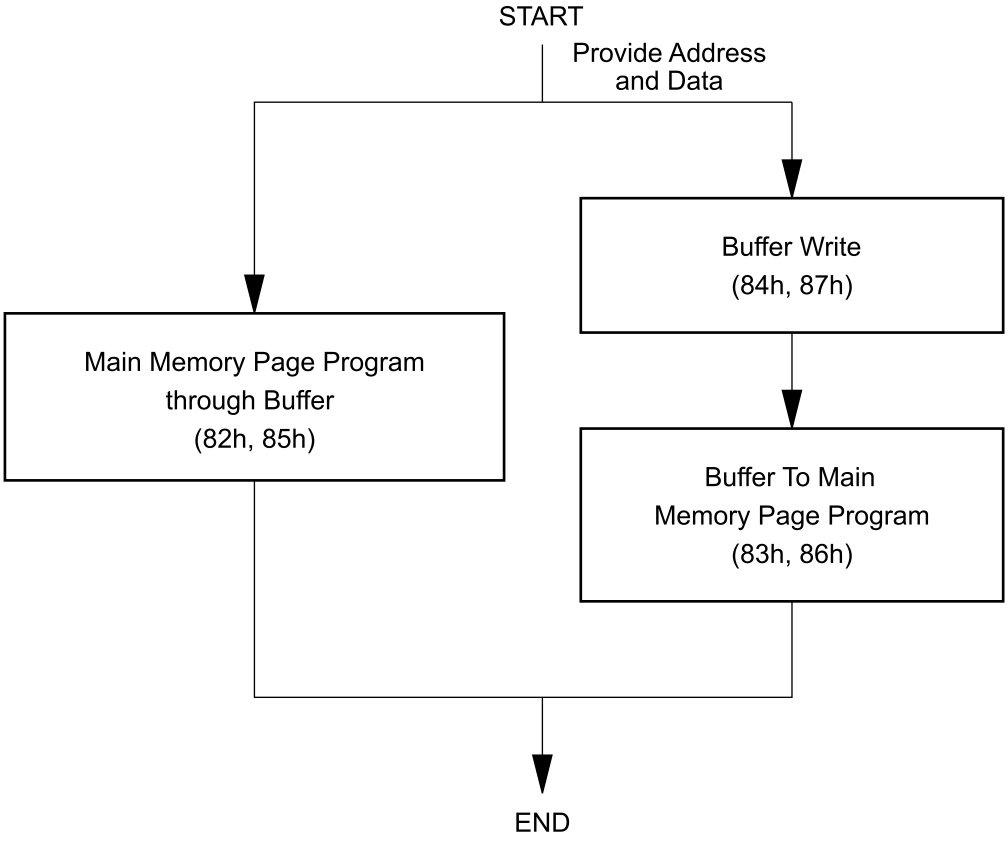
Figure 25-12.Reset Timing



Note: 1. The $\overline{CS}$ signal should be in the high state before the $\overline{RESET}$ signal is deasserted.

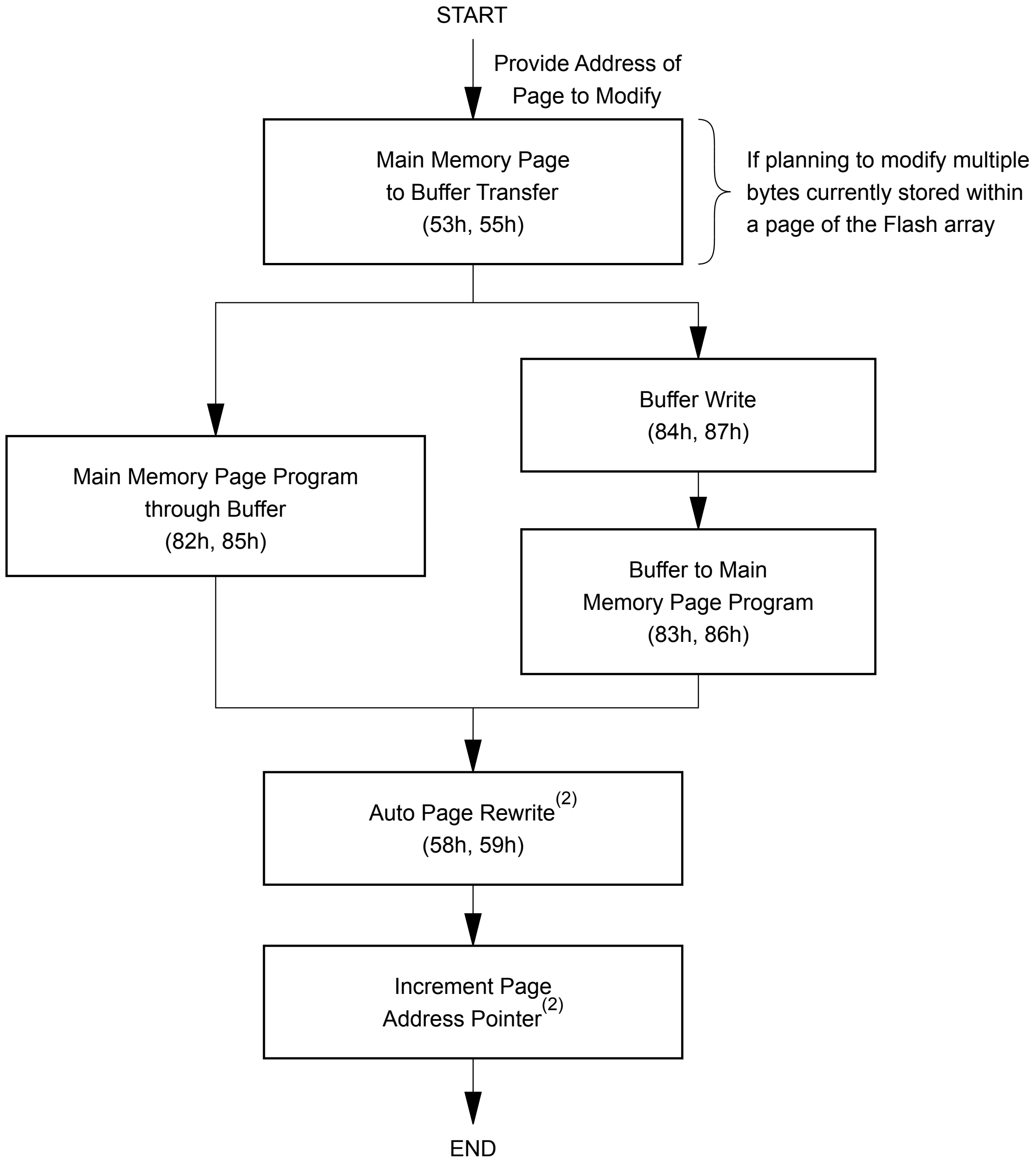
26. Auto Page Rewrite Flowchart

Figure 26-1. Algorithm for Programming or Re-programming of the Entire Array Sequentially


START
Provide Address and Data
Buffer Write (84h, 87h)
Main Memory Page Program through Buffer (82h, 85h)
Buffer To Main Memory Page Program (83h, 86h)
END

Notes:
1. This type of algorithm is used for applications in which the entire array is programmed sequentially, filling the array page-by-page
2. A page can be written using either a Main Memory Page Program operation or a buffer write operation followed by a buffer to Main Memory Page Program operation
3. The algorithm above shows the programming of a single page. The algorithm will be repeated sequentially for each page within the entire array

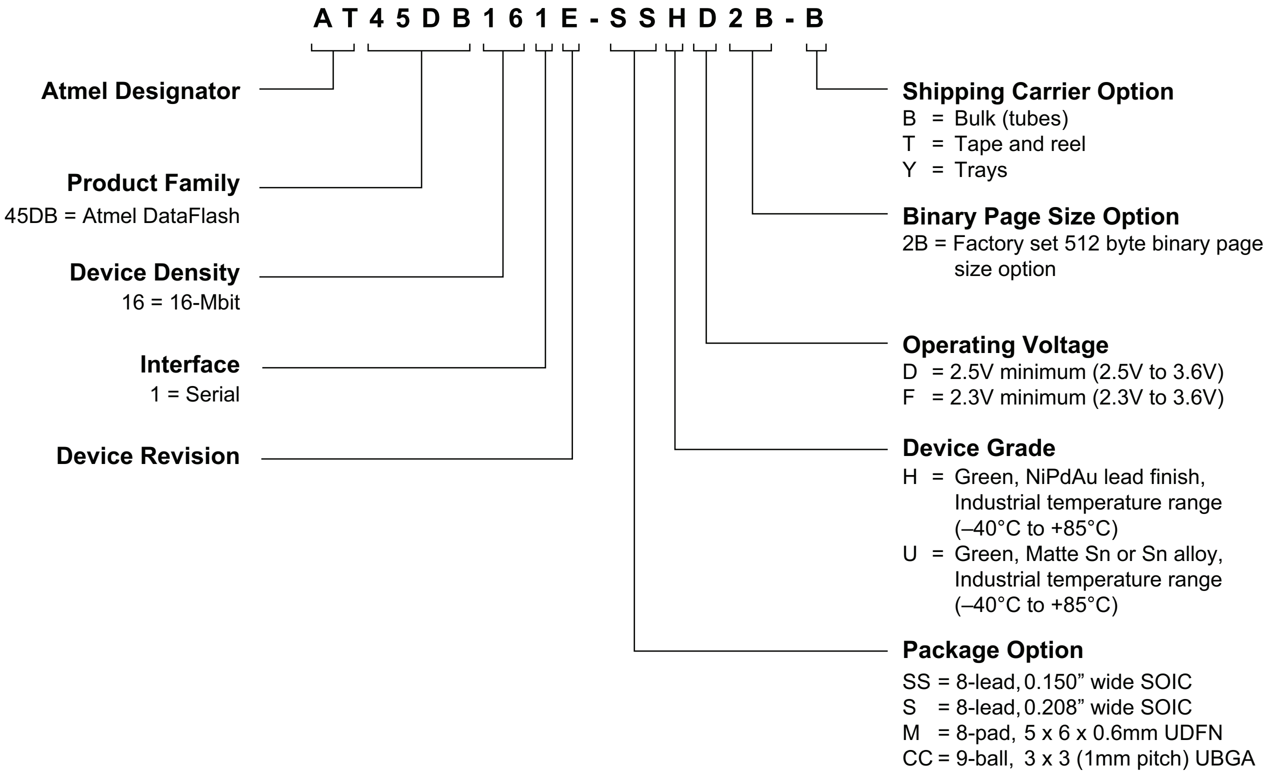
Figure 26-2. Algorithm for Programming or Re-programming of the Entire Array Randomly


START
Provide Address of Page to Modify
Main Memory Page to Buffer Transfer (53h, 55h)
If planning to modify multiple bytes currently stored within a page of the Flash array
Buffer Write (84h, 87h)
Main Memory Page Program through Buffer (82h, 85h)
Buffer to Main Memory Page Program (83h, 86h)
Auto Page Rewrite(2) (58h, 59h)
Increment Page Address Pointer(2)
END

Notes:
1. To preserve data integrity, each page of an Atmel DataFlash sector must be updated/rewritten at least once within every 20,000 cumulative page erase and program operations
2. A page address pointer must be maintained to indicate which page is to be rewritten. The auto page rewrite command must use the address specified by the page address pointer
3. Other algorithms can be used to rewrite portions of the Flash array. Low-power applications may choose to wait until 20,000 cumulative page erase and program operations have accumulated before rewriting all pages of the sector. See application note AN-4 (“Using Atmel’s Serial DataFlash”) for more details

27. Ordering Information

27.1 Ordering Detail



AT45DB161E-SSHD2B-B

Atmel Designator

Product Family
45DB = Atmel DataFlash

Device Density
16 = 16-Mbit

Interface
1 = Serial

Device Revision

Shipping Carrier Option
B = Bulk (tubes)
T = Tape and reel
Y = Trays

Binary Page Size Option
2B = Factory set 512 byte binary page size option

Operating Voltage
D = 2.5V minimum (2.5V to 3.6V)
F = 2.3V minimum (2.3V to 3.6V)

Device Grade
H = Green, NiPdAu lead finish, Industrial temperature range (–40°C to +85°C)
U = Green, Matte Sn or Sn alloy, Industrial temperature range (–40°C to +85°C)

Package Option
SS = 8-lead, 0.150” wide SOIC
S = 8-lead, 0.208” wide SOIC
M = 8-pad, 5 x 6 x 0.6mm UDFN
CC = 9-ball, 3 x 3 (1mm pitch) UBGA

27.2 Ordering Codes

Atmel Ordering Code	Package	Lead Finish	Operating Voltage	f_{SCK}	Device Grade
AT45DB161E-SSHD-B [1]	8S1	NiPdAu	2.5V to 3.6V	85MHz	Industrial (-40°C to 85°C)
AT45DB161E-SSHD-T[1]					
AT45DB161E-SHD-B[1][2]	8S2				
AT45DB161E-SHD-T[1][2]					
AT45DB161E-MHD-Y[1]	8MA1				
AT45DB161E-MHD-T[1]					
AT45DB161E-CCUD-T[1]	9CC1	SnAgCu			
AT45DB161E-SSHF-B[1]	8S1	NiPdAu	2.3V to 3.6V	85MHz	Industrial (-40°C to 85°C)
AT45DB161E-SSHF-T[1]					
AT45DB161E-MHF-Y[1]	8MA1				
AT45DB161E-MHF-T[1]					

Notes: 1. The shipping carrier suffix is not marked on the device.

2. Not recommended for new design. Use the 8S1 package option.

Package Type	
8S1	8-lead 0.150" wide, Plastic Gull Wing Small Outline (JEDEC SOIC)
8S2	8-lead 0.208" wide, Plastic Gull Wing Small Outline (EIAJ SOIC)
8MA1	8-pad (5 x 6 x 0.6mm body), Thermally Enhanced Plastic Ultra Thin Dual Flat No-lead (UDFN)
9CC1	9-ball (6 x 6 x 0.6mm body) 3 x 3 array x 1mm pitch, Ultra-thin Ball Grid Array (UBGA)

27.3 Ordering Codes (Binary Page Mode)

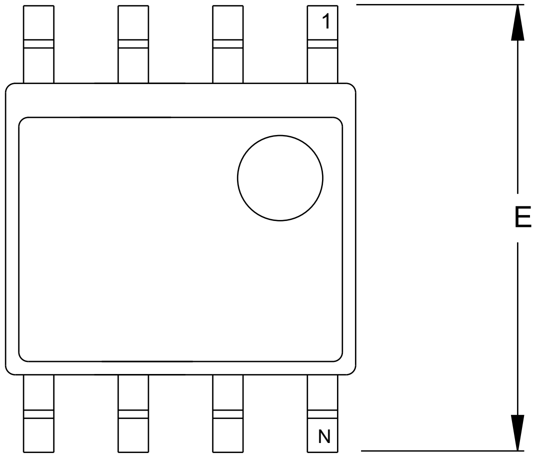
Atmel Ordering Code	Package	Lead Finish	Operating Voltage	f_{SCK}	Device Grade
AT45DB161E-SSHD2B-T(1)(3)	8S1	NiPdAu	2.5V to 3.6V	85MHz	Industrial (-40°C to 85°C)
AT45DB161E-SHD2B-T(1)(2)(3)	8S2				
AT45DB161E-MHD2B-T (1)(3)	8MA1				
AT45DB161E-SSHF2B-T(1)(3)	8S1	NiPdAu	2.3V to 3.6V	85MHz	Industrial (-40°C to 85°C)
AT45DB161E-MHF2B-T(1)(3)	8MA1				

Notes:
1. The shipping carrier suffix is not marked on the device.
2. Not recommended for new design. Use the 8S1 package option.
3. Parts ordered with suffix code ‘2B’ are shipped in tape and reel (T&R) with the page size set to 512 bytes. This option is only available for shipping in T&R (-T).

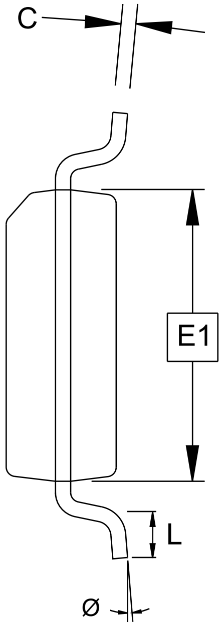
Package Type	
8S1	8-lead 0.150" wide, Plastic Gull Wing Small Outline (JEDEC SOIC)
8S2	8-lead 0.208" wide, Plastic Gull Wing Small Outline (EIAJ SOIC)
8MA1	8-pad (5 x 6 x 0.6mm body), Thermally Enhanced Plastic Ultra Thin Dual Flat No-lead (UDFN)

28. Packaging Information

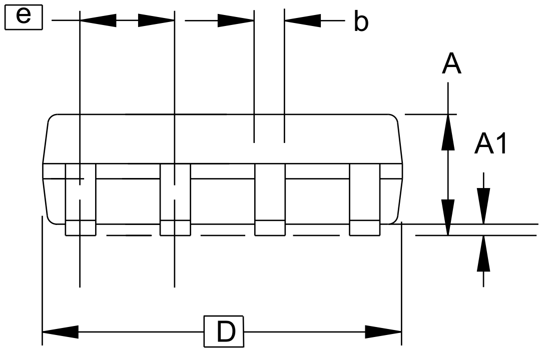
28.1 8S1 – 8-lead JEDEC SOIC



TOP VIEW



END VIEW



SIDE VIEW

Notes: This drawing is for general information only. Refer to JEDEC Drawing MS-012, Variation AA for proper dimensions, tolerances, datums, etc.

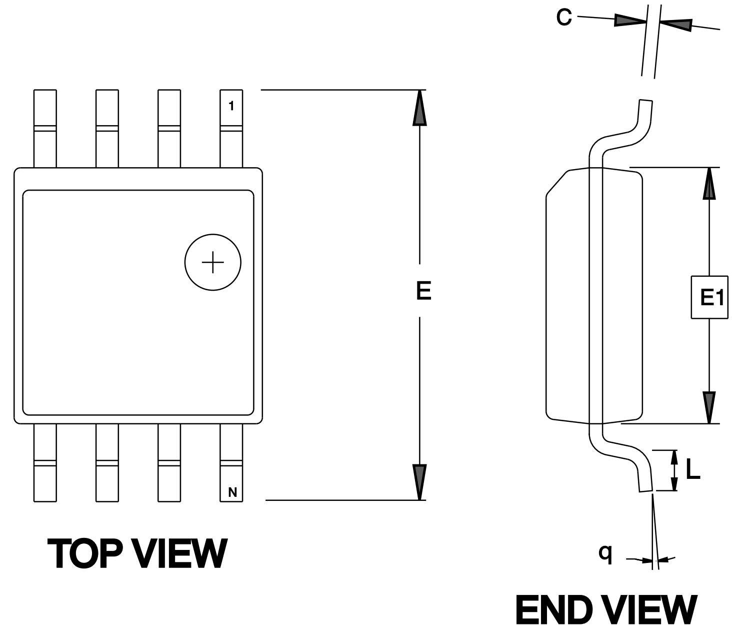
COMMON DIMENSIONS
(Unit of Measure = mm)

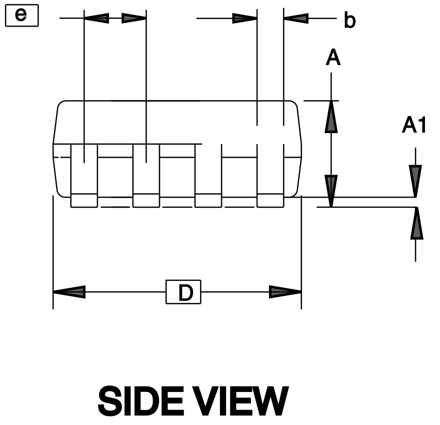
SYMBOL	MIN	NOM	MAX	NOTE
A	1.35	–	1.75	
A1	0.10	–	0.25	
b	0.31	–	0.51	
C	0.17	–	0.25	
D	4.80	–	5.05	
E1	3.81	–	3.99	
E	5.79	–	6.20	
e	1.27 BSC			
L	0.40	–	1.27	
Ø	0°	–	8°	

6/22/11

Atmel Package Drawing Contact: packagedrawings@atmel.com	**TITLE** 8S1, 8-lead (0.150” Wide Body), Plastic Gull Wing Small Outline (JEDEC SOIC)	**GPC** SWB	**DRAWING NO.** 8S1	**REV.** G

28.2 8S2 – 8-lead EIAJ SOIC





COMMON DIMENSIONS
(Unit of Measure = mm)

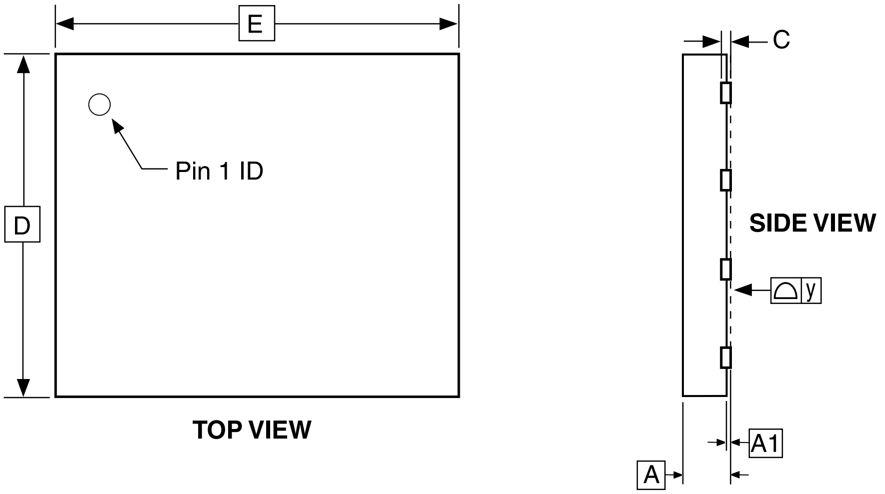
SYMBOL	MIN	NOM	MAX	NOTE
A	1.70		2.16	
A1	0.05		0.25	
b	0.35		0.48	4
C	0.15		0.35	4
D	5.13		5.35	
E1	5.18		5.40	2
E	7.70		8.26	
L	0.51		0.85	
q	0°		8°	
e	1.27 BSC			3

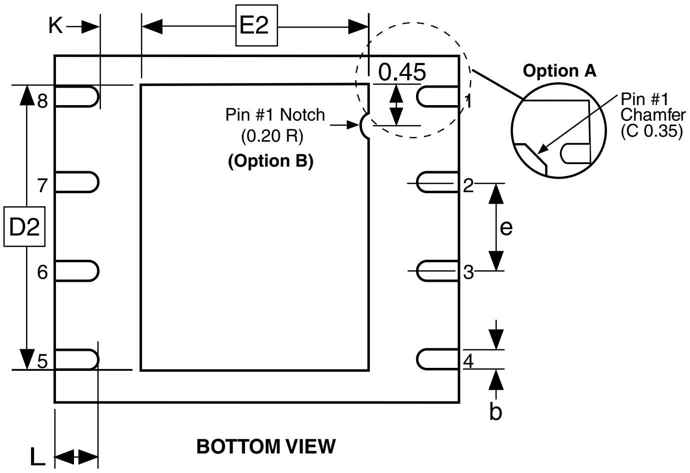
Notes: 1. This drawing is for general information only; refer to EIAJ Drawing EDR-7320 for additional information.
2. Mismatch of the upper and lower dies and resin burrs aren't included.
3. Determines the true geometric position.
4. Values b,C apply to plated terminal. The standard thickness of the plating layer shall measure between 0.007 to .021 mm.

4/15/08

	TITLE	GPC	DRAWING NO.	REV.
Atmel Package Drawing Contact: packagedrawings@atmel.com	**8S2,** 8-lead, 0.208" Body, Plastic Small Outline Package (EIAJ)	STN	8S2	F

28.3 8MA1 – 8-pad UDFN





COMMON DIMENSIONS
(Unit of Measure = mm)

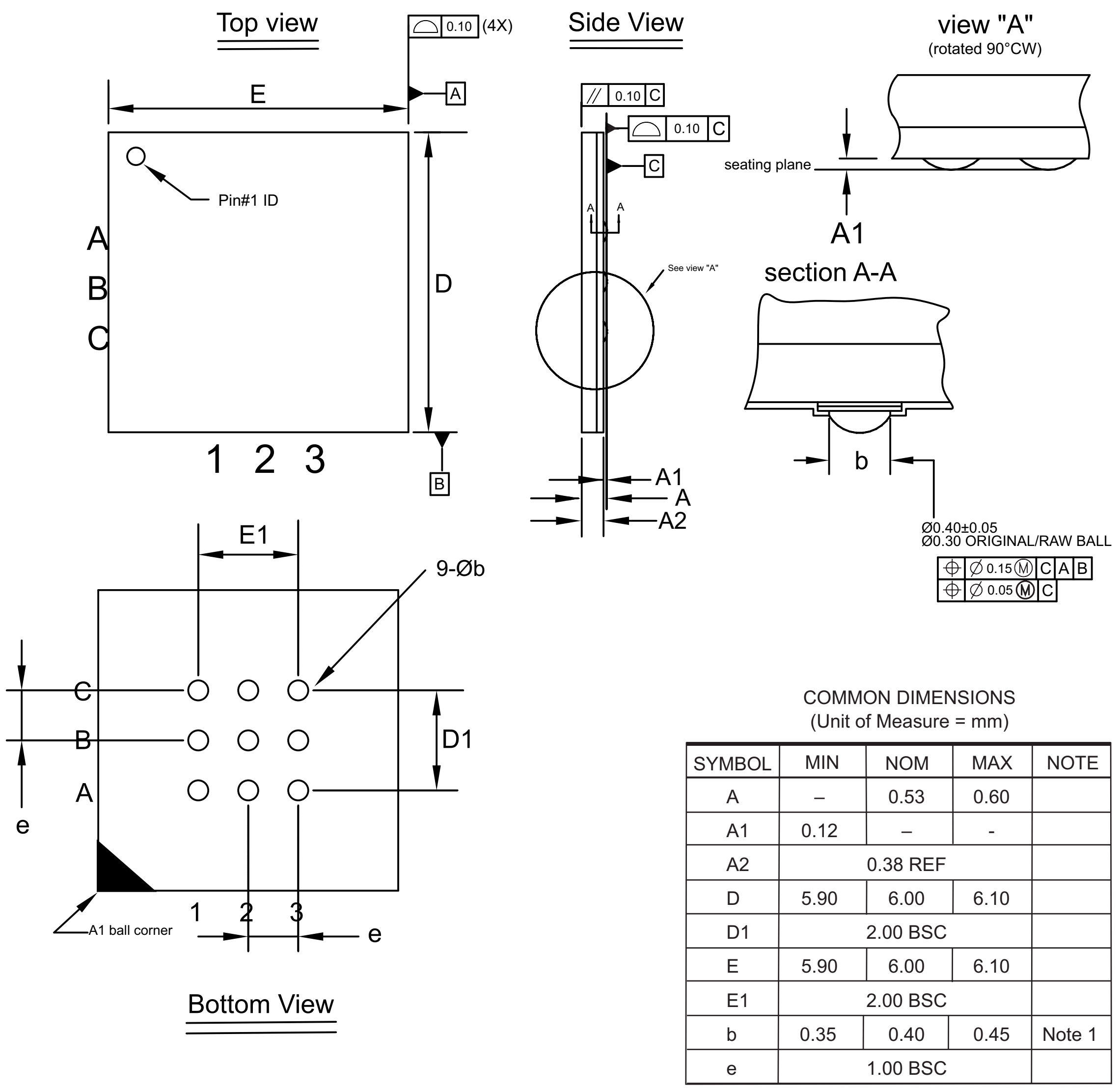
SYMBOL	MIN	NOM	MAX	NOTE
A	0.45	0.55	0.60	
A1	0.00	0.02	0.05	
b	0.35	0.40	0.48	
C	0.152 REF			
D	4.90	5.00	5.10	
D2	3.80	4.00	4.20	
E	5.90	6.00	6.10	
E2	3.20	3.40	3.60	
e	1.27			
L	0.50	0.60	0.75	
y	0.00	–	0.08	
K	0.20	–	–	

Notes: 1. This package conforms to JEDEC reference MO-229, Saw Singulation.
2. The terminal #1 ID is a Laser-marked Feature.

4/15/08

	TITLE	GPC	DRAWING NO.	REV.
Atmel Package Drawing Contact: packagedrawings@atmel.com	**8MA1,** 8-pad (5 x 6 x 0.6 mm Body), Thermally Enhanced Plastic Ultra Thin Dual Flat No Lead Package (UDFN)	YFG	8MA1	D

28.4 9CC1 – 9-ball UBGA



COMMON DIMENSIONS
(Unit of Measure = mm)

SYMBOL	MIN	NOM	MAX	NOTE
A	–	0.53	0.60	
A1	0.12	–	-	
A2		0.38 REF		
D	5.90	6.00	6.10	
D1		2.00 BSC		
E	5.90	6.00	6.10	
E1		2.00 BSC		
b	0.35	0.40	0.45	Note 1
e		1.00 BSC		

Notes: 1. Dimension "b" is measured at the maximum ball diameter, in a plane parallel to the seating plane.

6/30/09

	TITLE	GPC	DRAWING NO.	REV.
Atmel Package Drawing Contact: packagedrawings@atmel.com	**9CC1**, 9-ball, 6 x 6 x 0.6mm Body, 1.0mm ball pitch (3x3 Array), Ultra-thin Ball Grid Array Package(UBGA)	CAA	9CC1	A

29. Revision History

Doc. Rev.	Date	Comments
8782C	07/2012	Update preliminary to complete datasheet status. Correct pinout drawings to state top view. Increase t_{XUDPD} maximum from 70µs to 120µs. Update ordering detail to add 2B equals factory set 512 byte binary page size option.
8782B	06/2012	Update “Enable Sector Protection”, “Disable Sector Protection”, “Erase Sector Protection Register”, “Program Sector Protection Register”, and “Read Sector Lockdown Register” figures. Correct descriptions for PAGE SIZE, bit 0 in “Status Register Format – Byte 1” table. Insert 1Bh opcode in “Detailed Bit-level Addressing Sequence for Binary Page Size (512 bytes)” and “Detailed Bit-level Addressing Sequence for Standard Atmel DataFlash Page Size (528 bytes)” tables. DC Characterisitcs: ● Add I_{CC1} condition of f = 20MHz; I_{OUT} = 0mA; V_{CC} = 3.6V with typical 7.5mA and maximum 10mA. ● Add I_{CC4} – Active Current, Erase Operation, V_{CC} = 3.6V, typical 14mA and maximum 20mA. ● Update I_{ZP} to I_{UDPD} – decrease typical from 0.5µA to 0.4µA and maximum from 2µA to 1µA. ● Update I_{DP} to I_{DPD} and I_{SP} to I_{SB}. ● Update I_{CC0} to I_{CC1} – decrease typical 7mA to 6.5mA. ● Update I_{CC1} to I_{CC2} – 33MHZ, increase maximum from 17mA to 19mA; 50MHz, decrease maximum from 20mA to 19mA; and at 85MHz, increase typical 14mA to 16mA and maximum 23mA to 26mA. ● Update I_{CC2} to I_{CC3} – remove erase operation, decrease typical from 15mA to 12mA and maximum from 20mA to 18mA. AC Characterisitics: ● Remove typical columns, t_{SECP}, and t_{SECUP}. ● f_{CAR3} – increase 2.3V/2.5V maximum 10MHz to 20MHz. ● t_{WH} – decrease 2.3V minimum from 6.8ns to 6.4ns and 2.5V minimum from 6.8ns to 5.2ns. ● t_{WL} – decrease 2.3V minimum from 6.8ns to 6.4ns and 2.5V minimum from 6.8ns to 5.2ns. ● t_{CS} – decrease 2.3V/2.5V minimum from 50ns to 30ns. ● t_{H} – decrease 2.3V/2.5V minimum from 3ns to 1ns. ● t_{DIS} – decrease 2.3V maximum from 35ns to 7ns and 2.5V from 35ns to 6ns. ● t_{V} – decrease 2.3V maximum from 8ns to 7ns. ● t_{COMP} – decrease 2.3V/2.5V maximum from 250µs to 220µs. Program and Erase Characteristics: ● Remove 2.3V minimum, typical, and maximum columns. ● t_{EP} – decrease typical from 17ms to 15ms and maximum from 50ms to 40ms. ● t_{PE} – decrease typical from 15ms to 12ms and maximum from 50ms to 35ms. ● t_{SE} – decrease typical from 1.6s to 1.4s and maximum from 5s to 3.5s. ● t_{CE} – decrease typical from 25s to 22s and maximum from 60s to 40s. Update ordering code detail. Replace package option from 9C1-CBGA to 9CC1-UBGA. Various topographical edits throughout document. Update template.
8782A	03/2012	Initial document release.

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Atmel Corporation
1600 Technology Drive
San Jose, CA 95110
USA
Tel: (+1) (408) 441-0311
Fax: (+1) (408) 487-2600
www.atmel.com

Atmel Asia Limited
Unit 01-5 & 16, 19F
BEA Tower, Millennium City 5
418 Kwun Tong Roa
Kwun Tong, Kowloon
HONG KONG
Tel: (+852) 2245-6100
Fax: (+852) 2722-1369

Atmel Munich GmbH
Business Campus
Parkring 4
D-85748 Garching b. Munich
GERMANY
Tel: (+49) 89-31970-0
Fax: (+49) 89-3194621

Atmel Japan G.K.
16F Shin-Osaki Kangyo Bldg
1-6-4 Osaki, Shinagawa-ku
Tokyo 141-0032
JAPAN
Tel: (+81) (3) 6417-0300
Fax: (+81) (3) 6417-0370

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