

PRODUCT BULLETIN

Generic Copy

18-Apr-2012 **ISSUE DATE:**

15150 **NOTIFICATION:**

TITLE: **ERRATA UPDATE FOR KINETIS**

EFFECTIVE

19-Apr-2012 DATE:

DEVICE(S)

MPN	
MK10DN512VLK10	
MK10DN512VLL10	
MK10DN512VLQ10	
MK10DN512VMD10	
MK10DN512ZAB10R	
MK10DN512ZVLK10	
MK10DN512ZVLL10	
MK10DN512ZVLL10R	
MK10DN512ZVLQ10	
MK10DN512ZVMB10	
MK10DN512ZVMC10	
MK10DN512ZVMC10R	
MK10DN512ZVMD10	
MK10DX256VLQ10	
MK10DX256VMD10	
MK10DX256ZVLQ10	
MK10DX256ZVLQ10R	
MK10DX256ZVMD10	
MK20DN512VLK10	
MK20DN512ZAB10R	
MK20DN512ZVLK10	
MK20DN512ZVLL10	
MK20DN512ZVLQ10	
MK20DN512ZVLQ10R	
MK20DN512ZVMB10	
MK20DN512ZVMC10	
MK20DN512ZVMD10	
MK20DX128ZVLQ10	
MK20DX256VLK10	

IK20DX256ZVLK10	
IK20DX256ZVLL10	
IK20DX256ZVLQ10	
IK20DX256ZVMC10	
IK20DX256ZVMD10	
IK30DN512ZVLK10	
IK30DN512ZVLL10	
IK30DN512ZVLQ10	
IK30DN512ZVLQ10R	
IK30DN512ZVMD10	
IK30DX256ZVLQ10	
IK30DX256ZVMD10	
K40DN512VLK10	
IK40DN512VLL10	
K40DN512VLQ10	
K40DN512ZVLL10	
IK40DN512ZVLQ10	
K40DN512ZVMD10	
K40DX128ZVLQ10	
K40DX256VLQ10	
K40DX256VMD10	
K40DX256ZVLQ10	
K40DX256ZVMB10	
K40DX256ZVMD10	
K50DN512ZCLL10	
IK50DN512ZCLQ10	
K50DX256ZCLL10	
K50DX256ZCLQ10	
K51DN512CLL10	
K51DN512ZCLQ10	
K51DX256ZCLL10	
K51DX256ZCMC10	
K52DN512ZCLQ10	
K52DN512ZCMD10	
K53DN512CMD10	
K53DN512ZCLQ10	
K53DN512ZCMD10	
K53DX256CLQ10	
K60DN256ZVLL10	
K60DN256ZVLQ10	
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IK60DN512VLQ10
IK60DN512VMD10
IK60DN512ZAB10R
IK60DN512ZCAB10R
IK60DN512ZVLL10
IK60DN512ZVLQ10
IK60DN512ZVLQ10R
IK60DN512ZVMC10
IK60DN512ZVMD10
IK60DX256VLL10
IK60DX256VLQ10
IK60DX256VMD10
IK60DX256ZVLL10
IK60DX256ZVLQ10
IK60DX256ZVMC10
IK60DX256ZVMD10

AFFECTED CHANGE CATEGORIES

• DEVICE SPECIFICATION / ERRATA

DESCRIPTION OF CHANGE

The Kinetis 100 MHz devices (4N30D mask set) errata documentation has been updated to include additional errata that have been identified. The updated version has been added to the freescale.com website at: http://cache.freescale.com/files/microcontrollers/doc/errata/KINETIS_4N30D.pdf.

4482	PMC: STOP mode recovery unstable
3981	SDHC: ADMA fails when data length in the last descriptor is less or equal to 4 bytes
3982	SDHC: ADMA transfer error when the block size is not a multiple of four
4624	SDHC: AutoCMD12 and R1b polling problem
3977	SDHC: Does not support Infinite Block Transfer Mode
4627	SDHC: Erroneous CMD CRC error and CMD Index error may occur on sending new CMD during data transfer
3980	SDHC: Glitch is generated on card clock with software reset or clock divider change
3983	SDHC: Problem when ADMA2 last descriptor is LINK or NOP
3978	SDHC: Software can not clear DMA interrupt status bit after read operation
3984	SDHC: eSDHC misses SDIO interrupt when CINT is disabled
2793	I2C: MCU does not wake from STOP mode on subsequent address matches if previous address is mismatched

REASON FOR CHANGE

The errata documentation for the Kinetis 100 MHz devices has been updated.

ANTICIPATED IMPACT OF PRODUCT CHANGE(FORM, FIT, FUNCTION, OR RELIABILITY)

There have been no changes made to the current production device. The errata describe existing conditions identified on current production devices. There are potential software and/or hardware implications to customers.

NOTE:

THE CHANGE(S) SPECIFIED IN THIS NOTIFICATION WILL BE IMPLEMENTED ON THE EFFECTIVE DATE LISTED ABOVE. To request further data or inquire about the notification, please enter a Service Request

For sample inquiries - please go to www.freescale.com

QUAL DATA AVAILABILITY DATE: 08-Apr-2012

QUALIFICATION STATUS: COMPLETED

QUALIFICATION PLAN:

N/A

RELIABILITY DATA SUMMARY:

N/A

ELECTRICAL CHARACTERISTIC SUMMARY:

N/A

CHANGED PART IDENTIFICATION:

N/A

ATTACHMENT(S):

External attachment(s) FOR this notification can be viewed AT: 15150 KINETIS 4N30D 3-29-12.pdf