# AFBR-5972Z

Industrial Fast Ethernet Fiber Optic Design

## Application Note 5523

### Introduction

The AFBR-5972Z fiber optic transceiver provides the system designer with the ability to implement a cost optimized Fast Ethernet (100 Mbps) over standard plastic optical fiber (POF). This product is lead free and compliant with RoHS. The AFBR-5972Z is UL listed and is a laser class 1 product. The transceiver also supports proprietary protocols up to 125 Mbps depending on the coding.

### Industrial Fast Ethernet

Industrial Fast Ethernet is defined as the use of the Ethernet protocol in an industrial environment, such as for automation and production machine control, or in power generation and distribution applications. Until recently, an industrial controller would communicate with a slave machine using one of several possible open or proprietary protocols such as Profibus, Foundation™ Fieldbus, and SERCOS. Increasingly, Ethernet is used as the link layer protocol (layer 2 in the Open Systems Interconnection or OSI model) with proprietary protocols riding on top in the network to application layers (layer 3 and up in the OSI model). The advantages are increased speed, better interoperability, easy integration with TCP/IP based networks, such as the Internet, and the ability to use standard routers, switches, and hubs. Examples of protocols based on industrial Fast Ethernet are ProfiNet, Fieldbus High Speed Ethernet and SERCOS III. While the Ethernet standard permits network nodes to be connected via central hubs with Carrier Sense Multiple Access with Collision Detection (CSMA/CD), current low cost switching technology allows industrial Fast Ethernet deployment in a dedicated point-to-point topology. This topology supports time critical applications like motion control.

Industrial Fast Ethernet over optical fiber has many advantages over copper solutions. While copper based communication links are susceptible to EM (electromagnetic) fields and emit EM noise which may interfere with other instrumentation, fiber optic links are immune to EM fields and do not generate them. Other advantages fiber has over copper are: low weight, complete galvanic separation between link partners, easy field termination and maintenance, easier installation due to short bending radius and better performance over temperature.

### Fiber Optic (FO) Network Components

The typical components used in an industrial Fast Ethernet fiber optic link, shown in Figure 1, are:

- **Network interface controller (NIC):** The Media Access Controller (MAC), which handles link control and makes the data available to higher network layer functions, and a Physical Layer Device (PHY) which serializes the data and performs clock and data recovery on the incoming data stream.
- **Fiber optic transceiver:** Converts the serial data from the NIC to an optical signal and vice versa.
- **Optical fiber:** Transport medium between the link partners. With the Avago AFBR-5972Z transceiver, the maximum link distance at 100 Mbps is 50 m POF with a 0.5 NA and 70 m POF with a 0.3 NA.

## Physical Layer Definitions

Industrial Fast Ethernet has three signal types or classiifcations: optical, electrical and electrical data.

The optical signal is defined as the optical signal into, and out of, the fiber. See callout A in Figure 1. The optical signal is serial binary data between two optical light levels. The serial binary stream is encoded to keep the DC balance of optical signal within limits. The AFBR-5972Z can be used with fast ethernet (100 Mbps with 4B/5B encoding, resulting in 125 MBd) and ethernet (10 Mbps, Manchester encoding, resulting in 20 MBd), or 10 Mbps with a Bi-phase coding. The auto-negotiation signals cannot be handled by the AFBR-5972Z. The AFBR-5972Z was characterized using PRBS $2^7$-1 pattern corresponding to a BER < 2.5 x $10^{-10}$. In addition, an evaluation of 10 MBd was performed using a Bi-phase coding.

The electrical signal is defined as the differential signal between the fiber optic transceiver and the NIC. See callout B in Figure 1. The differential serial binary electrical signal is between two PECL levels referenced to 3.3 V (also known as Low Voltage Pseudo Emitter-Coupled Logic or LVPECL). Because the electrical signal is the quantized, amplitude limited conversion of the optical signal, the encoding is the same as the optical signal. The electrical data is defined as the framed and clocked data between the PHY and the MAC and is also known as the Media Independent Interface (MII). See callout C in Figure 1. The clock is recovered from the incoming binary signal stream by the PHY and subsequently used to sample the data. On the transmitter side of the PHY, callout B in Figure 1, the data is encoded and transmitted based on the local clock. The AFBR-5972Z transceiver can be easily integrated into new and existing industrial ethernet system as shown in Figure 2.

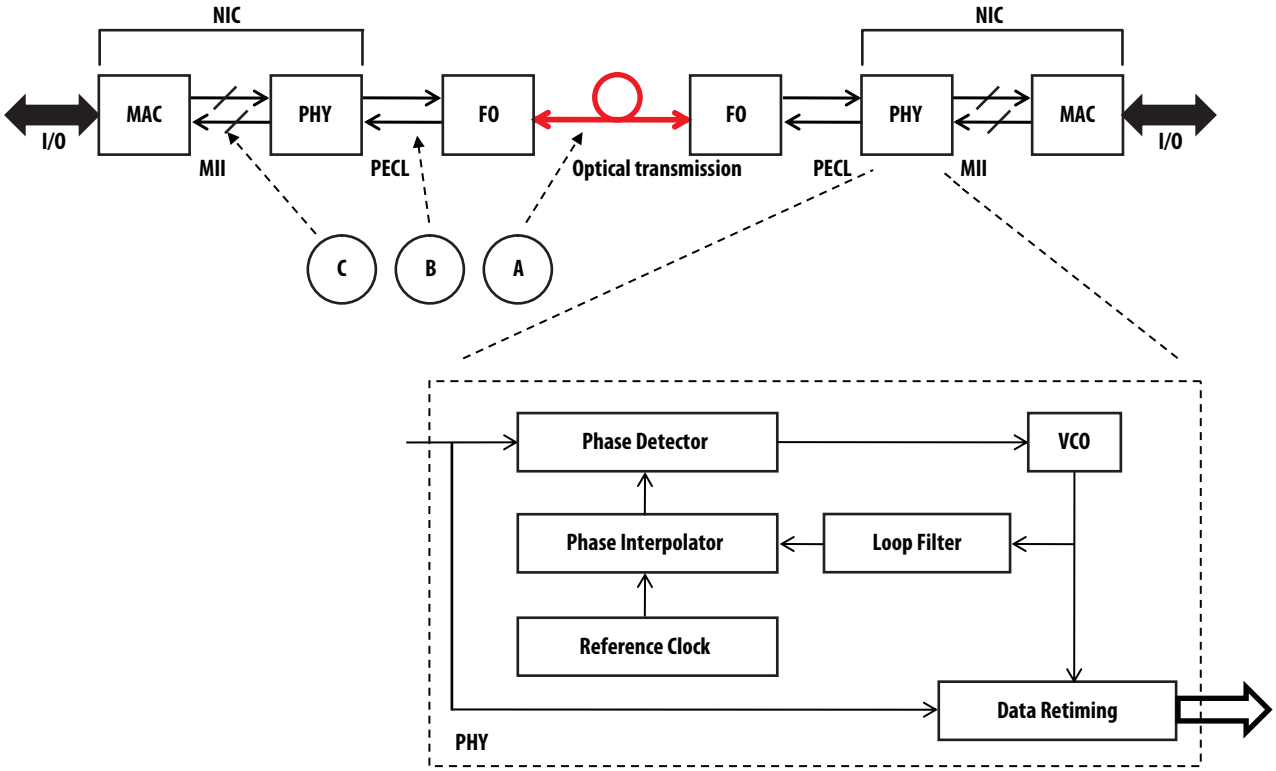


**Figure 1. The optical (A), electrical (B) and data (C) signal types in an industrial Ethernet link. The insert shows a block diagram of a typical clock/data recovery circuit in the receiver section of the PHY**

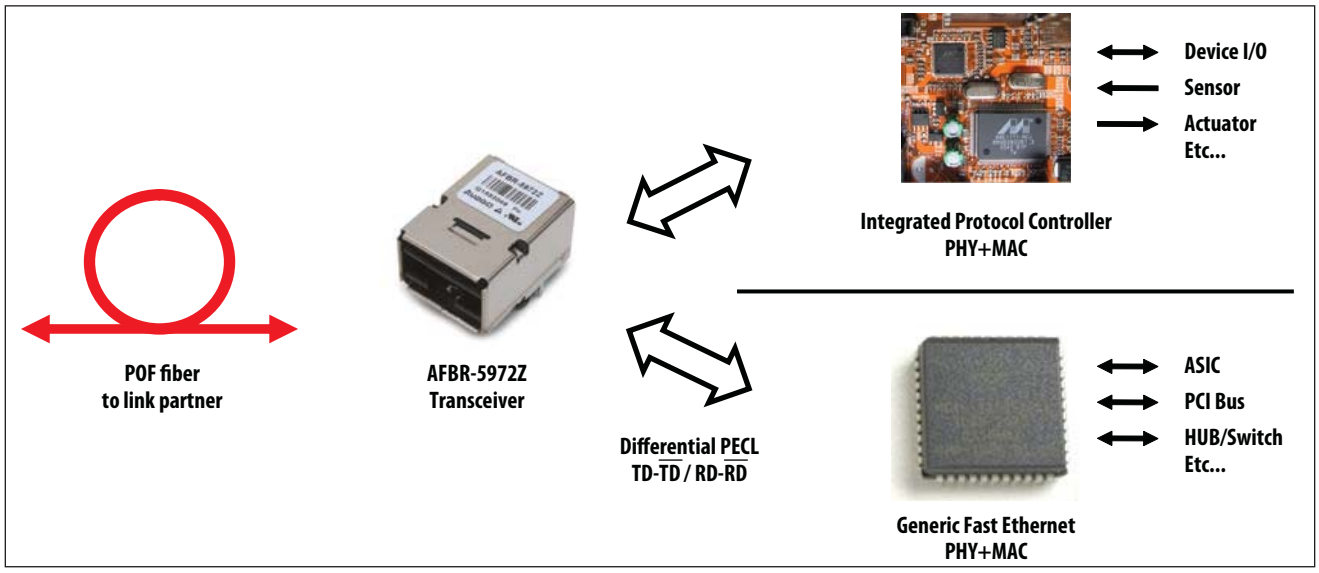


**Figure 2. Industrial Fast Ethernet link with an optical transceiver and a PHY+MAC**

## Recommended AFBR-5972Z Termination

- LVDS - The transmitter is LVDS compatible without any change. If the LVPECL output of the receiver is too high for the LVDS input of the PHY IC, then use the circuit as shown in Figure 3.
- LVPECL - The recommended termination of the AFBR-5972Z, the LVPECL interface to the PHY IC and the three different NIC configurations are illustrated in Figure 4 to 7.

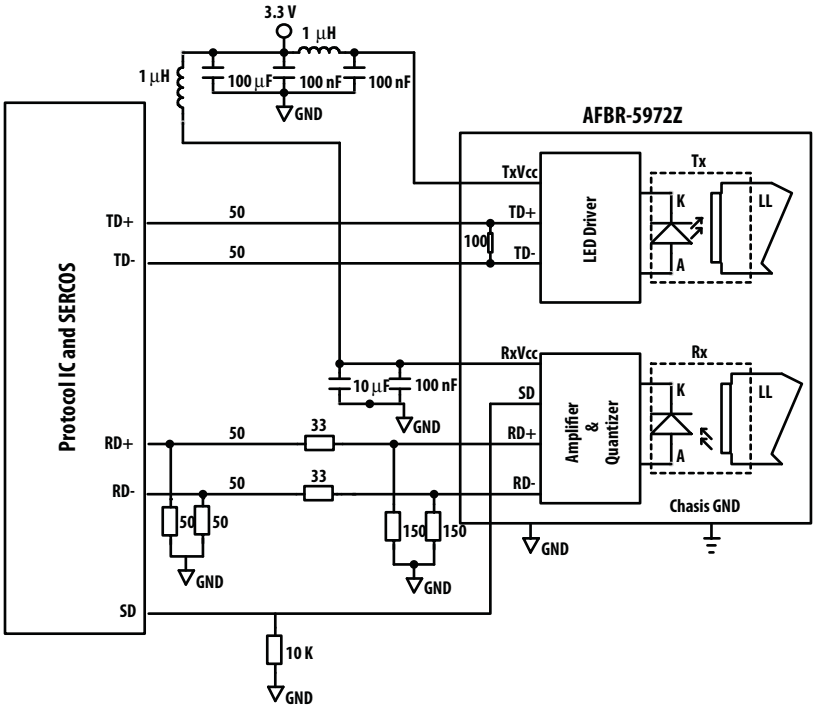


**Figure 3. AFBR-5972Z interface for DC-LVDS scheme**

## Application: Media Converter

Ethernet uses different encoding schemes for signals on copper and fiber links. A media converter converts between the two encoding schemes. A media converter application using an AFBR-5972Z transceiver requires an interface IC with a LVPECL PHY connected to the AFBR-5972Z and a twisted-pair PHY connected to the RJ-45 interface. See Figure 4 for details. The LVPECL PHY needs to be compatible with one or more of the following Ethernet standards: 100 BASE-FX, 100 BASE-SX and 10 BASE-FL. Example interface ICs are the MicroLinear ML6652 (now available from RF Micro Devices, Inc.) and the DaviCom DM9301.

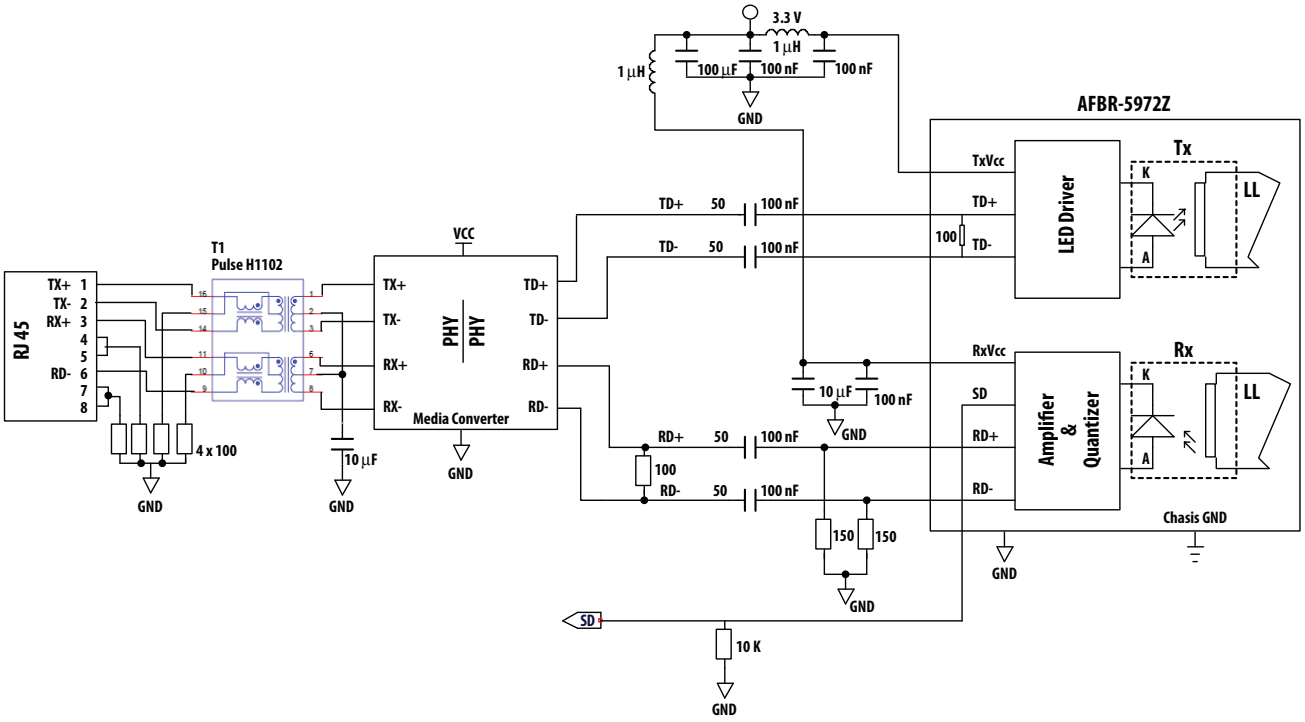


**Figure 4. General AFBR-5972Z termination and interface schematic for a media converter application**

## Application: Industrial Network Device

An industrial network device based on the Ethernet protocol (like ProfiNet, Fieldbus HSE or SERCOS III) typically uses a protocol specific ASIC with an MII interface. An industrial network application using the AFBR-5972Z transceiver therefore requires a PHY which translates between the LVPECL signals of the AFBR-5972Z and the MII signals of the protocol ASIC. Figure 5 shows a typical circuit.

The LVPECL PHY must be compatible with 100BASE-FX. Examples of suitable PHY ICs are the Micrel KSZ8001 and the Intel LXT971A.

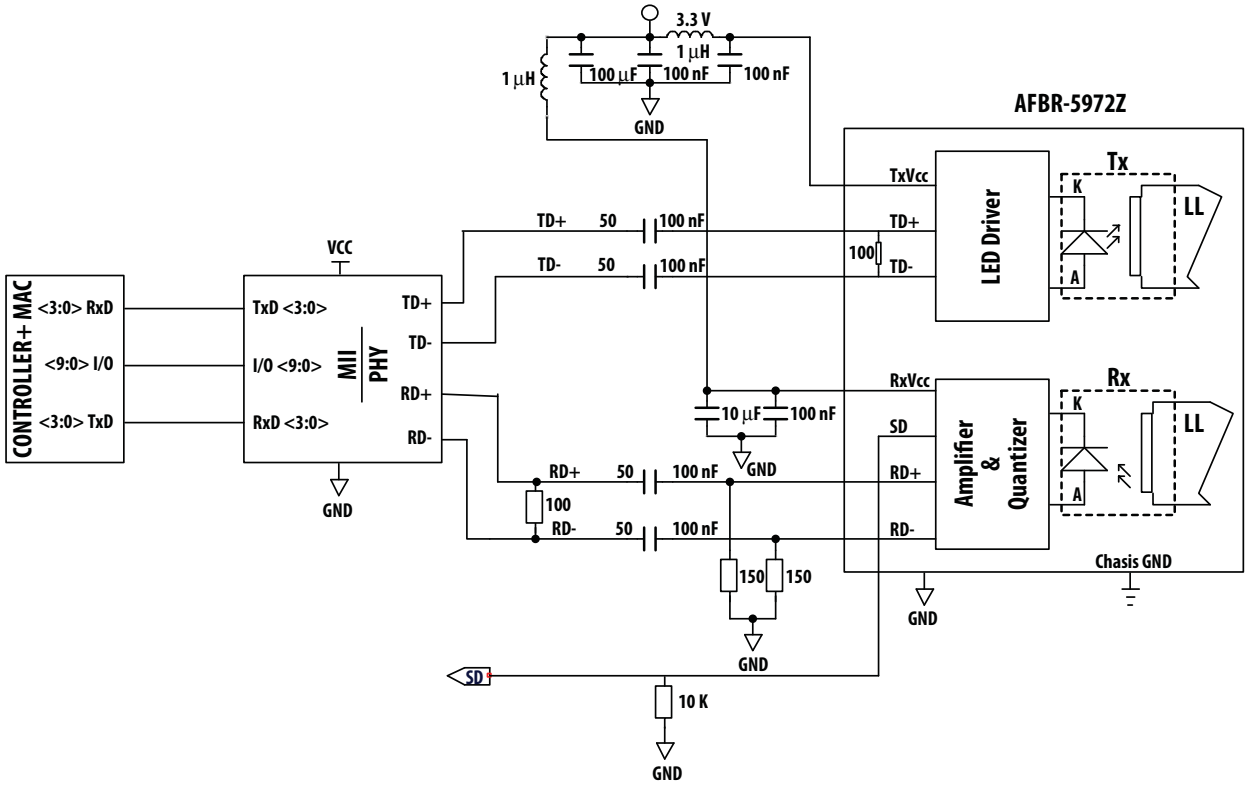


**Figure 5. General AFBR-5972Z termination and interface schematic for an industrial network application**

## Application: Communication Network Device

A communication network device for Ethernet and Fast Ethernet, like a PC motherboard, router or switch, requires a specialized IC with a LVPECL PHY connected to the AFBR-5972Z and a bus interface connected to the host system. Figure 6 shows a typical circuit.

The LVPECL PHY needs to be compatible with one or more of the following Ethernet standards: 100BASE-FX, 100BASE-SX and 10BASE-FL. Examples of such specialized ICs for the PCI bus are the Micrel KS8695P.

## Evaluation Kit

To see the performance of AFBR-5972Z, please use the evalution kit AFBR-0544Z.

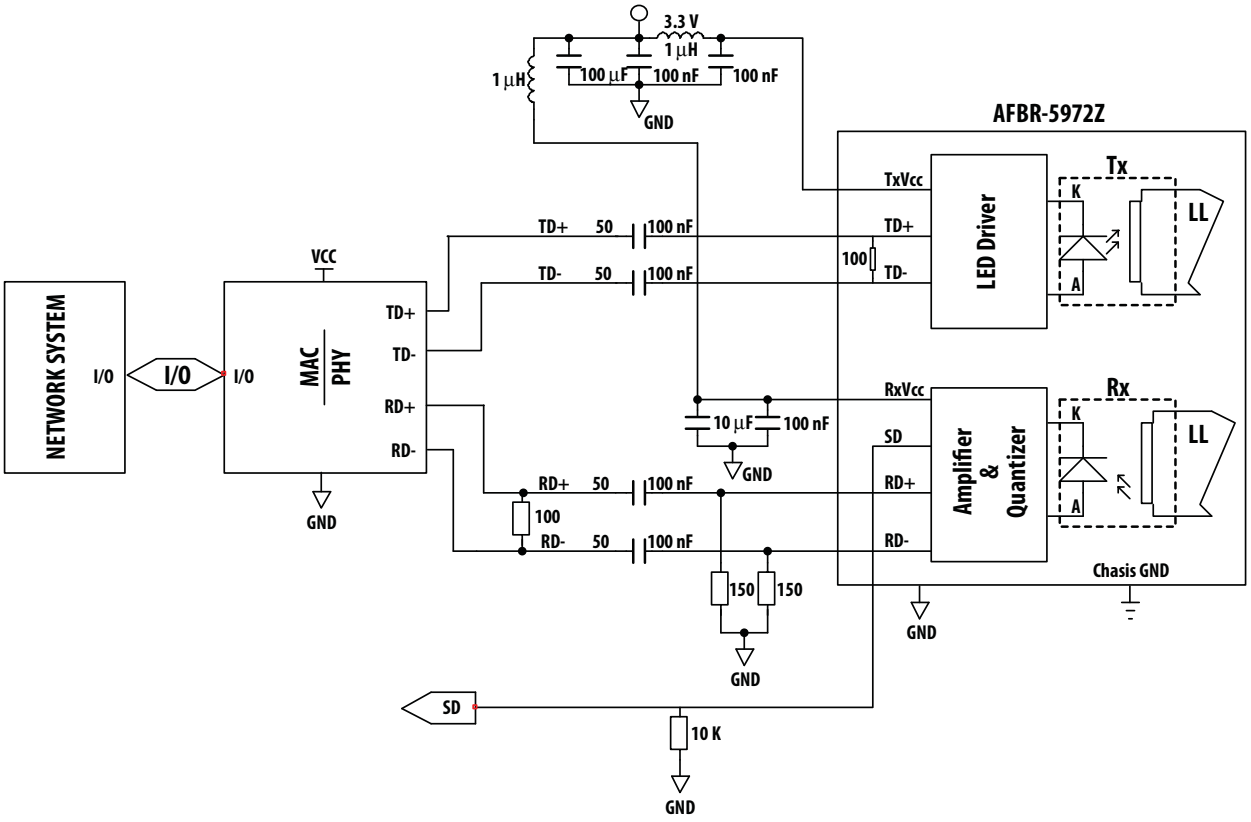


**Figure 6. General AFBR-5972Z termination and interface schematic for a communication network device**

## Receiver

The LVPECL (RD+ and RD-) output uses a differential pair of source followers. The output source followers should operate in the active region such that DC current flows at all times. If the AFBR-5972Z is DC-coupled to the NIC, the proper output termination is 50 Ω to Vcc - 2 V. For a system operating at 3.3 V, the LVPECL outputs should be pulled up to Vcc with a 130 Ω resistor and pulled down with an 82 Ω resistor. See figure 7. Data sheet values have been verified by characterization with this termination.

If AC-coupling is required for the PECL input structure of the NIC, due to supply voltage for example, the transceiver PECL output needs to be biased by coupling it to ground with a resistor. Because the PECL output common-mode voltage is fixed at approximately Vcc - 1.3 V, the value of the resistor is calculated as 142 Ω (assuming a 14 mA DC current). However, It is recommended to increase this resistor slightly to 150 Ω to compensate for the AC component of the signal that is transmitted to the PECL receiver side and that therefore lowers the termination resistance as seen from the transceiver side. On the NIC side, PECL termination recommended by the NIC manufacturer should be used.

For the AFBR-5972Z transceiver in an industrial Fast Ethernet application the recommended coupling capacitance is 100 nF.

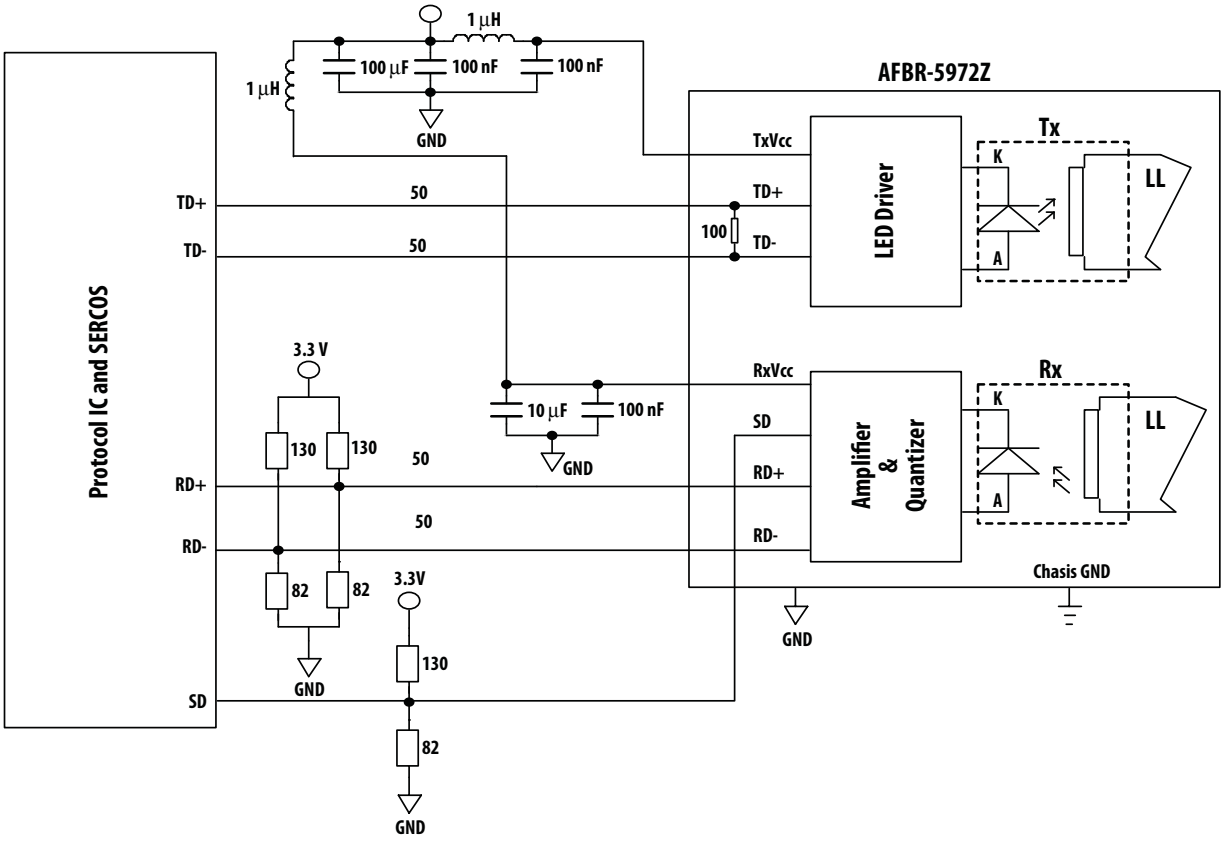


**Figure 7. An alternative interface DC-LVPECL circuits**

## Application of SD

The SD output can be used for e.g wake up of the network node from sleep mode, or for control of a status LED, or open link detection.

## Transmitter

The LVPECL (TD+ and TD-) input of the AFBR-5972Z is terminated internally with a 100 Ω resistor across the data lines. The differential input is self-biased with current switching. The recommended coupling capacitance is 100 nF. If external biasing of the NIC's PECL output is needed, this is typically detailed in the NIC datasheet or vendor application information.

## Power Budget – Example

| Fiber: POF | 50 m, NA = 0.5 | Unit |
|---|---|---|
| Tx average launched power (min.) | -10 | dBm |
| Link attenuation: -0.25 dB/m x 50 m | -12.5 | dB |
| Margin | -3 | dB |
| **Sum** | **-25.5** | **dBm** |
| Rx sensitivity (max.) | -26 | dBm |

## General Design and Layout Rules

When the AFBR-5972Z is used, the following PCB design considerations should be followed.

The AFBR-5972Z board mounting clips have been optimized for a PCB thickness of 1.57 mm. When thicker PCBs are used, which is possible due to the length of the electrical pins, the user must ensure that the bores for the board mounting clips allow proper mating and mechanical stability. This can be achieved by thinning the board around the board mounting clips by a stud hole that leaves the remaining board thickness of approximately 1.57 mm (see Figure 8).

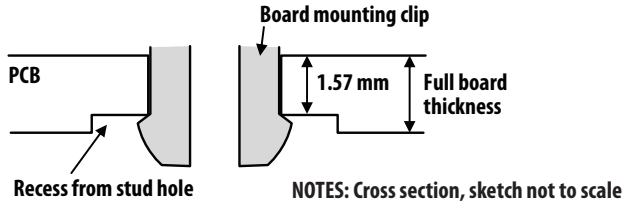


**Figure 8. Example AFBR-5972Z PCB design with thicker PCB**

- The 10 µF and 100 nF decoupling capacitors and the ferrite inductors must be placed as close as possible to the transceiver. Tantalum or ceramic chip capacitors are recommended.
- When in the operating state, the transceiver induces relatively large current transients and therefore the power supply design needs to have sufficient capacity and output stability.
- The ground pins of the transceiver must be directly connected to a contiguous ground plane provided by the circuit board to give a low inductance power supply ground.
- To ensure the best possible performance of the (typically bandwidth limited) industrial fiber optic link, it is good practice to optimize the electrical path between the transceiver and NIC. Therefore, the transmitter and receiver signal lines between the transceiver and NIC must be differential pairs that are equal in length, as short as possible, on one signal layer (no vias), and impedance matched to 50 Ω.
- The differential signal lines are best placed in a signal layer directly above a ground layer. The ground plane must not be interrupted or cut by a trace over the entire length of the differential signal lines. This ensures a low inductance signal return path and continuous impedance along the trace.
- The bias resistors in the receiver signal line need to be as close as possible to the NIC. This is recommended for both DC and AC coupling.
- If required by the NIC, any bias resistors in the transmitter signal line must be as close as possible to the transceiver.
- A solid Vcc and ground plane under/around the transceiver that helps the transceiver dissipate thermal energy through the two Vcc and two ground pins is recommended.
- When the signal detect pin (SD in Figure 4) of the transceiver is connected to LVPECL compatible logic, it is recommended to use a 10 kΩ pull-down resistor. Alternatively, a LVPECL termination (130 Ω to VCC and 82 Ω to GND as shown in Figure 7) can be used. Data sheet values have been verified by characterization with this LVPECL termination. If signal detect is not used, the SD pin of the transceiver should be left floating.

## Packing

As shown in Figure 9, the AFBR-5972Z transceiver is shipped in trays with 25 pieces. To keep the devices protected against humidity, each tray is put into a moisture barrier bag (MBB) together with desiccant and indicator according to JEDEC J-STD-33. Each packed tray is put into a carton box (size: 275 mm x 44 mm x 320 mm).

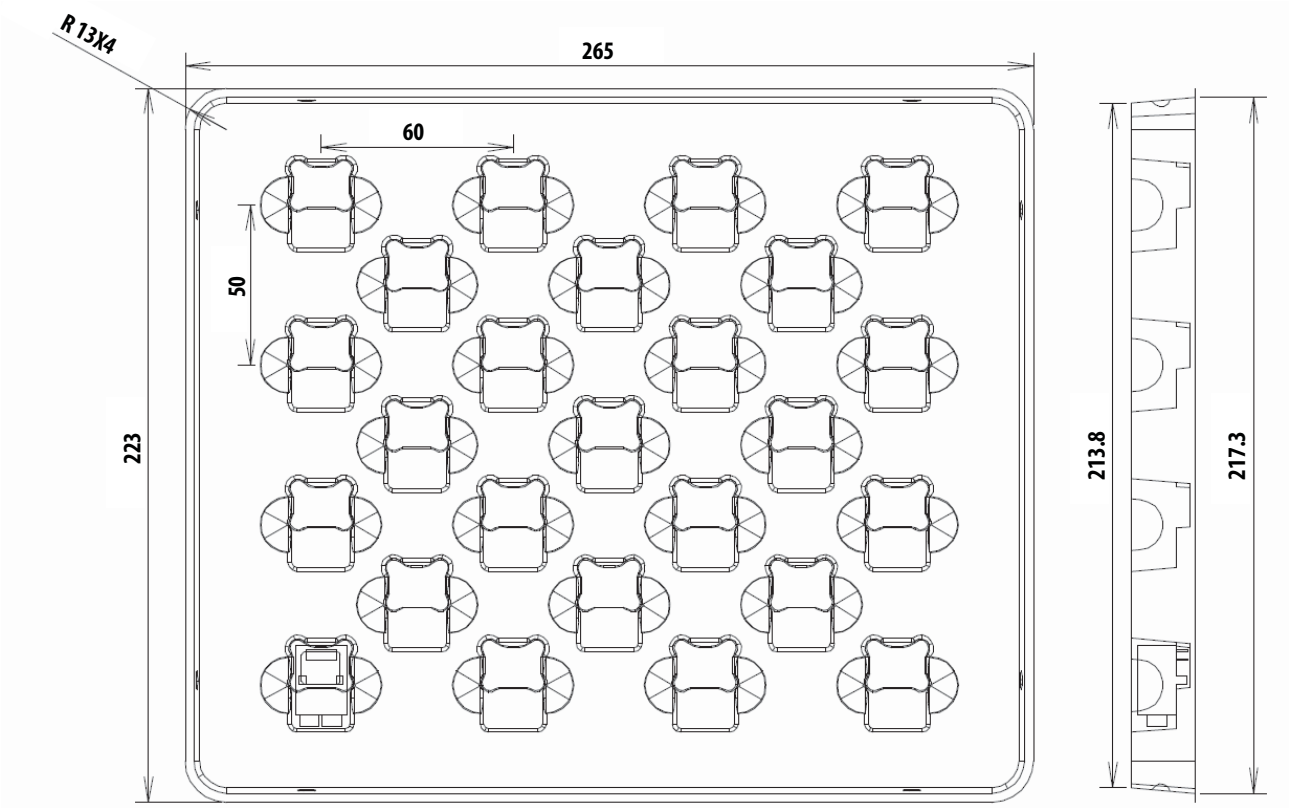


**Figure 9. Packing tray of the AFBR-5972Z (dimension are in mm)**

## Electrostatic Discharge (ESD) Protection

The AFBR-5972Z is sensitive to electrostatic discharges and therefore must be handled with care in an ESD protected area, indicated with the sign as shown in Figure 10.

An ESD event may damage or degrade device performance. The DIN EN61340-5-1 standard has to be considered. The following ESD prevention measures should be applied. Any smaller ESD prevention program might be unsuitable to prevent ESD damage.

- ESD floors
- ESD tables, ESD work surfaces and ESD storage facilities (e.g. trolleys and carts)
- ESD wrist straps/connectors for wrist straps
- ESD footwear and garments (cotton or special released materials)
- ESD gloves or finger cots
- ESD chairs
- ESD tools (e.g. nippers)
- ESD preventions at equipment parts (Equipment parts which may directly contact the device leads must be made of dissipative materials, wherever possible. If dissipative materials cannot be used for technical reasons, metals must be used whose natural nonconductive surface layer is sufficiently thin (breakdown voltage < 10 V).
- Conducting machine parts which may contact the device leads directly must be connected to ground without a series resistor.
- ESD packing materials

## ESD Classification

AFBR-5972Z devices passed the following ESD tests:

- Human body model (HBM) with U = 2 kV according to JEDEC standard JESD22-A114(Electrostatic discharge (ESD) sensitivity testing HBM)
- Machine model (MM) with U = 500 V according to JEDEC standard JESD22-A115(Machine model (MM) sensitivity testing MM)


**Figure 10. Warning sign for an ESD protected area**

## Floor Life and Maximum Storage Time

The AFBR-5972Z moisture sensitivity classification is MSL2a according to JEDEC J-STD-020. Unopened moisture barrier bagged devices can be stored up to 12 months in an environment with a temperature between 5° C and 50° C and a relative humidity (RH) not exceeding 90%. Unpacked devices can be kept in a production environment up to four weeks provided a temperature not exceeding 30° C and a relative humidity (RH) not exceeding 60%. Table 1 summaries MSL2a floor life time.

**Table 1. MSL2a floor life[1]**

| |
|---|
| 4 weeks |
| ≤ 30° C |
| 60% RH |

Note:
1. Maximum storage time without humidity protection pack after opening moisture barrier bag

## Baking

When AFBR-5972Z devices are inserted and soldered into a system up to four weeks after they have been taken out of the moisture barrier bag, then the moisture level in the mold material is low enough to ensure minimum mechanical stress while soldering. If the devices are kept on the production floor for more than four weeks, Avago recommends to bake the devices before soldering.

Baking is done by removing the devices from the tray and placing them in a shallow container so that the package bodies do not touch each other. Then the devices are placed in the bake oven, heating the devices to 100° C for 24 hours. After this procedure, the moisture content of the devices is low and the moisture-induced stress during soldering is reduced. As a general guideline baking is recommended before every soldering attempt.

## Solderability/ Soldering Process

The leads of the devices are tin plated for good solderability. The recommended soldering method for the AFBR-5972Z transceiver devices is wave soldering.

The preconditioning for the qualification tests "Temperature Shock (TS)" and "Temperature Humidity Bias (THB)" was done by dip soldering with a solder temperature of 260° C for 10 seconds according to JEDEC standard J-STD-020. The qualification test "Resistance to soldering heat – Standard soldering technique (RSH-ST)" was done by dip soldering with a solder temperature of 260° C for 10 seconds according to JEDEC standard JESD22-B106C.

The AFBR-5972Z devices are not suitable for reflow soldering. If SMD components are assembled on the same PCB as the AFBR-5972Z, the AFBR-5972Z devices must be assembled afterwards. They must not be subjected to reflow solder stress.

## Eye safety

The transmitter device emits light with a wavelength of 650 nm (red). This product is designed to avoid damage to the unprotected eye. To indicate the classification of the light source, a label as depicted in Figure 11 can be used. However these labels are not mandatory on the product according to IEC 60825 version 1.2 paragraph 1.1.

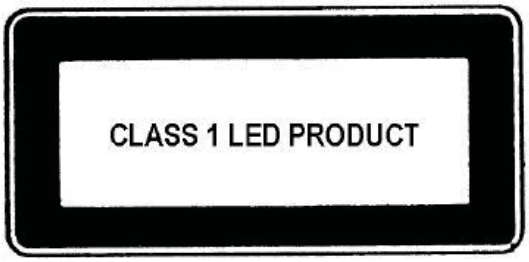


**Figure 11. LED source label**

## Product label

The AFBR-5972Z product label dimensions and code explanation are shown in Figure 12.


**Figure 12. The AFBR-5972Z product label contains lot, year, work week and serial number and country of origin information**

Label dimensions: 10 mm x 12 mm

Explanation of product code (in Figure 12, the product code example is AA110001):

AA110001

LLYWWSSS

⇩

LL lot number (2 digits)

Y last digit of the calender year (1 digit)

WW work week (2 digits)

SSS serial number (3 digits)

For product information and a complete list of distributors, please go to our web site: **www.avagotech.com**


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