

BUK7K6R8-40E

Dual N-channel TrenchMOS standard level FET

23 July 2012

Product data sheet

1. Product profile

1.1 General description

Dual standard level N-channel MOSFET in a LFPAK56D package using TrenchMOS technology. This product has been designed and qualified to AEC Q101 standard for use in high performance automotive applications.

1.2 Features and benefits

- Q101 compliant
- Repetitive avalanche rated
- Suitable for thermally demanding environments due to 175 °C rating
- True standard level gate with $V_{GS(th)} > 1 \text{ V @ } 175 \text{ °C}$

1.3 Applications

- 12 V Automotive systems
- Motors, lamps and solenoid control
- Start-stop micro-hybrid applications
- Transmission control
- Ultra high performance power switching

1.4 Quick reference data

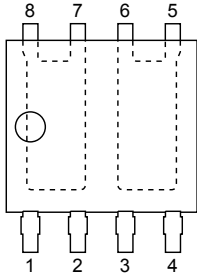
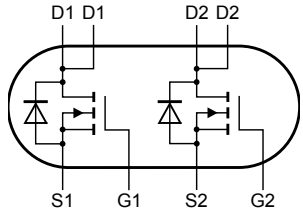
Table 1. Quick reference data

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|--|----------------------------------|---|-----|-----|-----|------------|
| V_{DS} | drain-source voltage | $T_j \geq 25 \text{ °C}; T_j \leq 175 \text{ °C}$ | - | - | 40 | V |
| I_D | drain current | $V_{GS} = 5 \text{ V}; T_{mb} = 25 \text{ °C}; \text{Fig. 1}$ | - | - | 40 | A |
| P_{tot} | total power dissipation | $T_{mb} = 25 \text{ °C}; \text{Fig. 2}$ | - | - | 64 | W |
| Static characteristics FET1 and FET2 | | | | | | |
| R_{DSon} | drain-source on-state resistance | $V_{GS} = 10 \text{ V}; I_D = 20 \text{ A}; T_j = 25 \text{ °C}; \text{Fig. 12}$ | - | 5.8 | 6.8 | m Ω |
| Dynamic characteristics FET1 and FET2 | | | | | | |
| Q_{GD} | gate-drain charge | $I_D = 20 \text{ A}; V_{DS} = 32 \text{ V}; V_{GS} = 20 \text{ V}; T_j = 25 \text{ °C}; \text{Fig. 14}; \text{Fig. 15}$ | - | 9.1 | - | nC |



2. Pinning information

Table 2. Pinning information

| Pin | Symbol | Description | Simplified outline | Graphic symbol |
|-----|--------|-------------|--|--|
| 1 | S1 | source1 |  <p>LFPAK56D (SOT1205)</p> |  <p><i>mbk725</i></p> |
| 2 | G1 | gate1 | | |
| 3 | S2 | source2 | | |
| 4 | G2 | gate2 | | |
| 5 | D2 | drain2 | | |
| 6 | D2 | drain2 | | |
| 7 | D1 | drain1 | | |
| 8 | D1 | drain1 | | |

3. Ordering information

Table 3. Ordering information

| Type number | Package | | Version |
|--------------|----------|--|---------|
| | Name | Description | |
| BUK7K6R8-40E | LFPAK56D | Plastic single ended surface mounted package (LFPAK56D); 8 leads | SOT1205 |

4. Limiting values

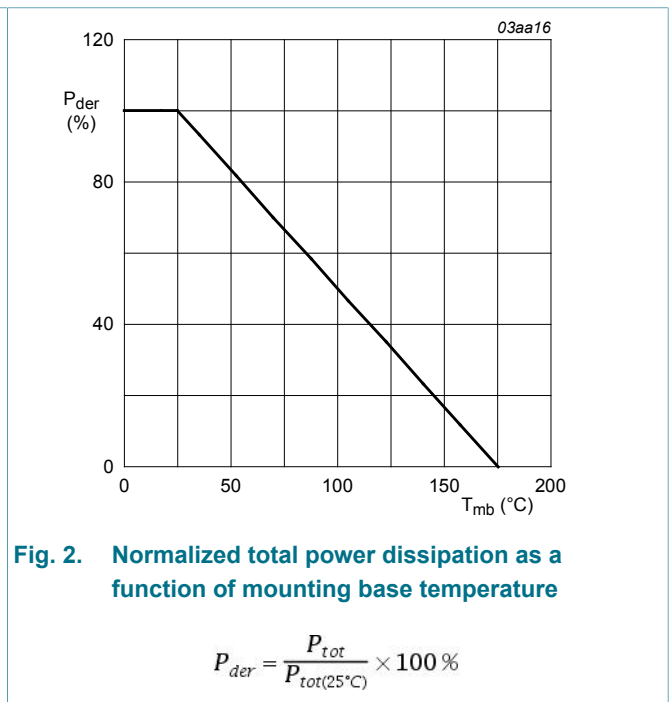
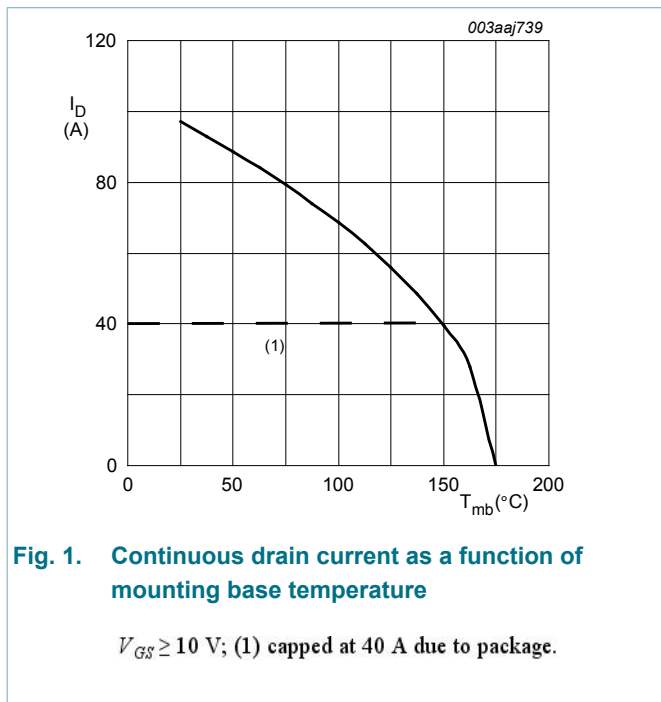
Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

| Symbol | Parameter | Conditions | Min | Max | Unit |
|---|----------------------------|---|-----|-----|------|
| V_{DS} | drain-source voltage | $T_j \geq 25\text{ °C}; T_j \leq 175\text{ °C}$ | - | 40 | V |
| V_{DGR} | drain-gate voltage | $R_{GS} = 20\text{ k}\Omega; T_j \geq 25\text{ °C}; T_j \leq 175\text{ °C}$ | - | 40 | V |
| V_{GS} | gate-source voltage | | -20 | 20 | V |
| I_D | drain current | $V_{GS} = 5\text{ V}; T_{mb} = 25\text{ °C}; \text{Fig. 1}$ | - | 40 | A |
| | | $T_{mb} = 100\text{ °C}; V_{GS} = 5\text{ V}; \text{Fig. 1}$ | - | 40 | A |
| I_{DM} | peak drain current | $T_{mb} = 25\text{ °C}; \text{pulsed}; t_p \leq 10\text{ }\mu\text{s}; \text{Fig. 4}$ | - | 291 | A |
| P_{tot} | total power dissipation | $T_{mb} = 25\text{ °C}; \text{Fig. 2}$ | - | 64 | W |
| T_{stg} | storage temperature | | -55 | 175 | °C |
| T_j | junction temperature | | -55 | 175 | °C |
| $T_{sld(M)}$ | peak soldering temperature | | - | 260 | °C |
| Source-drain diode FET1 and FET2 | | | | | |
| I_S | source current | | - | 40 | A |

| Symbol | Parameter | Conditions | Min | Max | Unit |
|---|--|---|---|-----|--------|
| I_{SM} | peak source current | pulsed; $t_p \leq 10 \mu s$; $T_{mb} = 25^\circ C$ | - | 291 | A |
| Avalanche Ruggedness FET1 and FET2 | | | | | |
| $E_{DS(AL)S}$ | non-repetitive drain-source avalanche energy | $I_D = 40 A$; $V_{sup} \leq 40 V$; $V_{GS} = 10 V$; $T_{j(init)} = 25^\circ C$; Fig. 3 | [1] [2] | - | 130 mJ |

- [1] Refer to application note AN10273 for further information
- [2] Single-pulse avalanche rating limited by maximum junction temperature of 175 °C



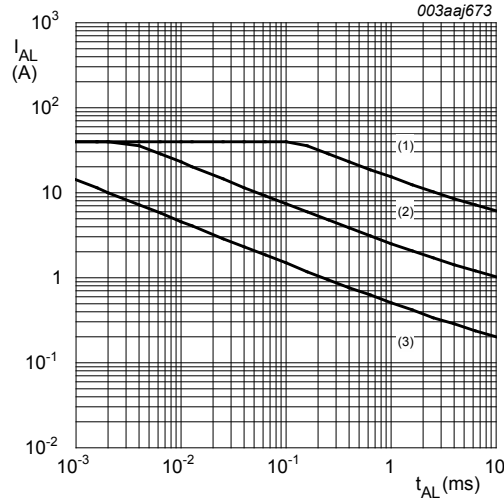


Fig. 3. Single-pulse and repetitive avalanche rating; avalanche current as a function of avalanche time, FET1 and FET2

- (1) Single-pulse; $T_j = 25\text{ }^\circ\text{C}$.
- (2) Single-pulse; $T_j = 175\text{ }^\circ\text{C}$.
- (3) Repetitive.

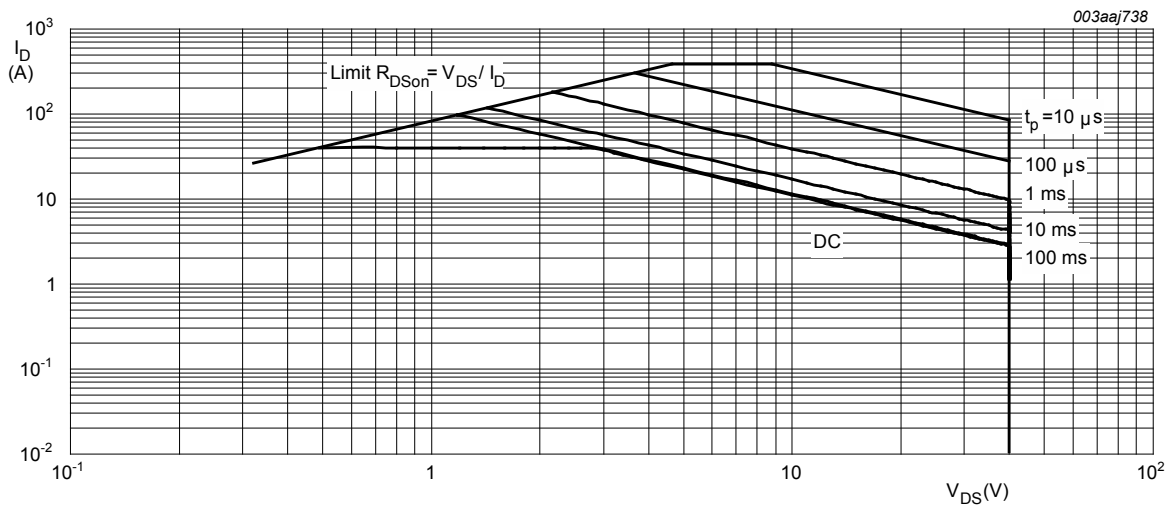


Fig. 4. Safe operating area; continuous and peak drain currents as a function of drain-source voltage

$T_{mb} = 25\text{ }^\circ\text{C}$; I_{DM} is a single pulse; (1) Capped at 40 A due to package

5. Thermal characteristics

Table 5. Thermal characteristics

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|----------------|---|------------|-----|-----|------|------|
| $R_{th(j-mb)}$ | thermal resistance from junction to mounting base | Fig. 5 | - | - | 2.36 | K/W |

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---------------|---|---|-----|-----|-----|------|
| $R_{th(j-a)}$ | thermal resistance from junction to ambient | Minimum footprint; mounted on a printed circuit board | - | 95 | - | K/W |

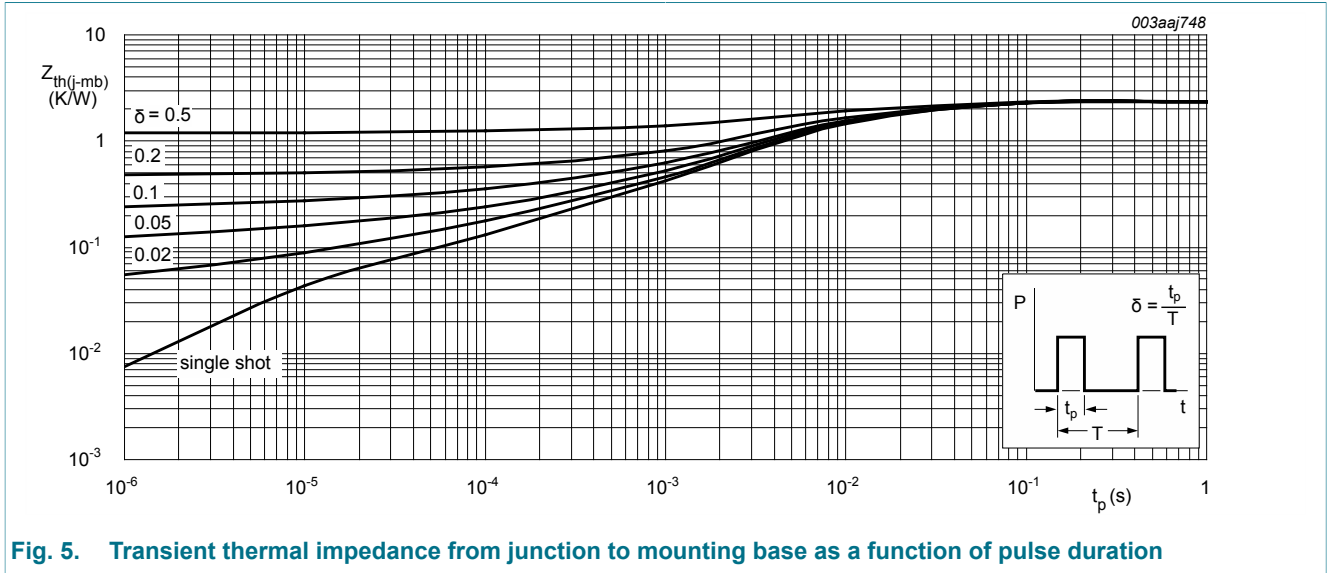


Fig. 5. Transient thermal impedance from junction to mounting base as a function of pulse duration

6. Characteristics

Table 6. Characteristics

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|----------------------------------|--|-----|-------|-----|------------|
| Static characteristics FET1 and FET2 | | | | | | |
| $V_{(BR)DSS}$ | drain-source breakdown voltage | $I_D = 250 \mu A; V_{GS} = 0 V; T_j = -55 \text{ }^\circ C$ | 36 | - | - | V |
| | | $I_D = 250 \mu A; V_{GS} = 0 V; T_j = 25 \text{ }^\circ C$ | 40 | - | - | V |
| $V_{GS(th)}$ | gate-source threshold voltage | $I_D = 1 \text{ mA}; V_{DS} = V_{GS}; T_j = 25 \text{ }^\circ C;$ Fig. 10; Fig. 11 | 2.4 | 3 | 4 | V |
| | | $I_D = 1 \text{ mA}; V_{DS} = V_{GS}; T_j = 175 \text{ }^\circ C;$ Fig. 10; Fig. 11 | 1 | - | - | V |
| | | $I_D = 1 \text{ mA}; V_{DS} = V_{GS}; T_j = -55 \text{ }^\circ C;$ Fig. 10; Fig. 11 | - | - | 4.5 | V |
| I_{DSS} | drain leakage current | $V_{DS} = 40 \text{ V}; V_{GS} = 0 \text{ V}; T_j = 175 \text{ }^\circ C$ | - | - | 500 | μA |
| | | $V_{DS} = 40 \text{ V}; V_{GS} = 0 \text{ V}; T_j = 25 \text{ }^\circ C$ | - | 0.02 | 1 | μA |
| I_{GSS} | gate leakage current | $V_{GS} = -20 \text{ V}; V_{DS} = 0 \text{ V}; T_j = 25 \text{ }^\circ C$ | - | 2 | 100 | nA |
| | | $V_{GS} = 20 \text{ V}; V_{DS} = 0 \text{ V}; T_j = 25 \text{ }^\circ C$ | - | 2 | 100 | nA |
| R_{DSon} | drain-source on-state resistance | $V_{GS} = 10 \text{ V}; I_D = 20 \text{ A}; T_j = 25 \text{ }^\circ C;$ Fig. 12 | - | 5.8 | 6.8 | m Ω |
| | | $V_{GS} = 10 \text{ V}; I_D = 20 \text{ A}; T_j = 175 \text{ }^\circ C;$ Fig. 12; Fig. 13 | - | 10.27 | 12 | m Ω |

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|--|-----------------------------------|---|-----|------|------|------|
| Dynamic characteristics FET1 and FET2 | | | | | | |
| $Q_{G(tot)}$ | total gate charge | $I_D = 20\text{ A}; V_{DS} = 32\text{ V}; V_{GS} = 10\text{ V};$ $T_j = 25\text{ }^\circ\text{C};$ Fig. 14 ; Fig. 15 | - | 28.9 | - | nC |
| Q_{GS} | gate-source charge | | - | 7 | - | nC |
| Q_{GD} | gate-drain charge | $I_D = 20\text{ A}; V_{DS} = 32\text{ V}; V_{GS} = 20\text{ V};$ $T_j = 25\text{ }^\circ\text{C};$ Fig. 14 ; Fig. 15 | - | 9.1 | - | nC |
| $Q_{GS(th)}$ | pre-threshold gate-source charge | $I_D = 20\text{ A}; V_{DS} = 32\text{ V}; V_{GS} = 10\text{ V};$ $T_j = 25\text{ }^\circ\text{C};$ Fig. 14 ; Fig. 15 | - | 4.5 | - | nC |
| $Q_{GS(th-pl)}$ | post-threshold gate-source charge | | - | 2.5 | - | nC |
| $V_{GS(pl)}$ | gate-source plateau voltage | $I_D = 20\text{ A}; V_{DS} = 32\text{ V}; T_j = 25\text{ }^\circ\text{C};$ Fig. 14 ; Fig. 15 | - | 4.7 | - | V |
| C_{iss} | input capacitance | $V_{GS} = 0\text{ V}; V_{DS} = 25\text{ V}; f = 1\text{ MHz};$ $T_j = 25\text{ }^\circ\text{C};$ Fig. 16 | - | 1460 | 1947 | pF |
| C_{oss} | output capacitance | | - | 324 | 389 | pF |
| C_{rss} | reverse transfer capacitance | | - | 197 | 270 | pF |
| $t_{d(on)}$ | turn-on delay time | $V_{DS} = 32\text{ V}; R_L = 1.6\text{ }\Omega; V_{GS} = 10\text{ V};$ $R_{G(ext)} = 5\text{ }\Omega; T_j = 25\text{ }^\circ\text{C}; I_D = 20\text{ A}$ | - | 8.9 | - | ns |
| t_r | rise time | | - | 15.4 | - | ns |
| $t_{d(off)}$ | turn-off delay time | | - | 19.4 | - | ns |
| t_f | fall time | | - | 16.5 | - | ns |
| Source-drain diode FET1 and FET2 | | | | | | |
| V_{SD} | source-drain voltage | $I_S = 10\text{ A}; V_{GS} = 0\text{ V}; T_j = 25\text{ }^\circ\text{C};$ Fig. 17 | - | 0.78 | 1.2 | V |
| t_{rr} | reverse recovery time | $I_S = 20\text{ A}; di_S/dt = -100\text{ A}/\mu\text{s}; V_{GS} = 0\text{ V};$ $V_{DS} = 20\text{ V}; T_j = 25\text{ }^\circ\text{C}$ | - | 20.6 | - | ns |
| Q_r | recovered charge | | - | 11.3 | - | nC |

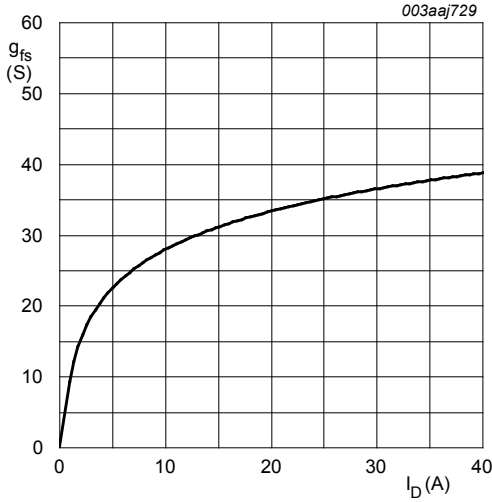


Fig. 6. Forward transconductance as a function of drain current; typical values

$T_j = 25\text{ }^\circ\text{C}; V_{DS} = 15\text{ V}$

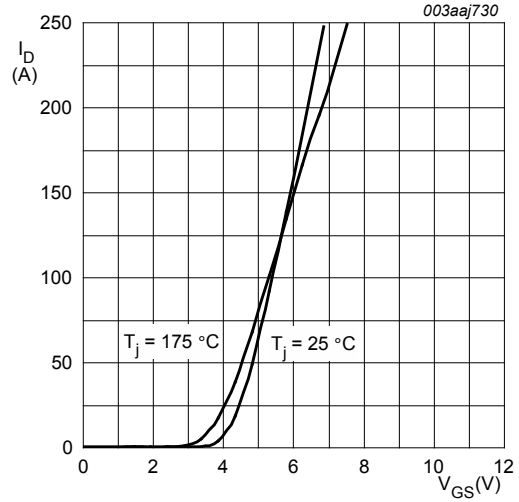


Fig. 7. Transfer characteristics: drain current as a function of gate-source voltage; typical values

$V_{DS} > I_D \times R_{DS(on)}$

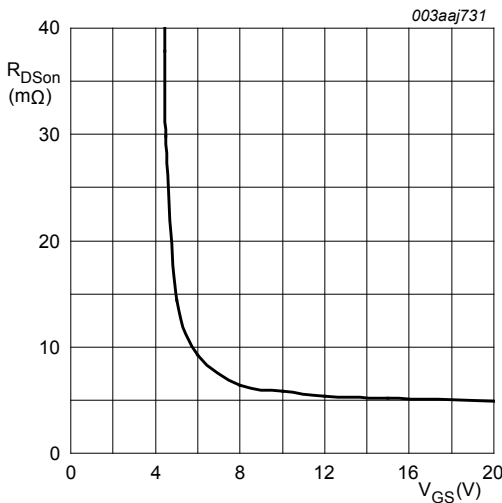


Fig. 8. Drain-source on-state resistance as a function of gate-source voltage; typical values

$T_j = 25\text{ }^\circ\text{C}; I_D = 20\text{ A}$

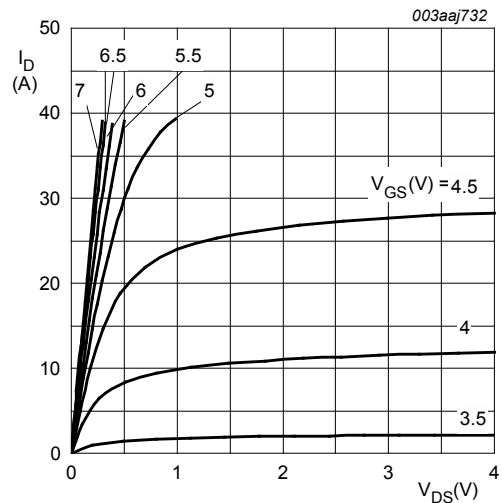


Fig. 9. Output characteristics: drain current as a function of drain-source voltage; typical values

$T_j = 25\text{ }^\circ\text{C}$

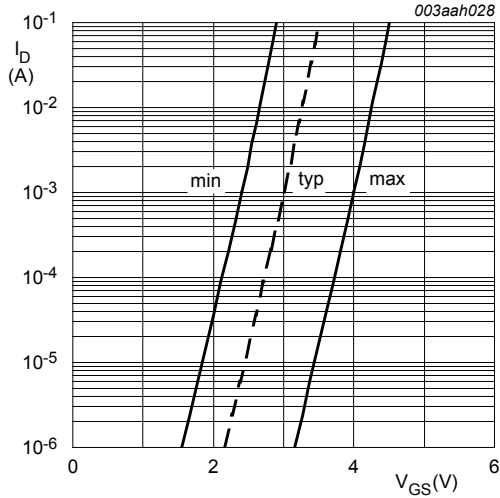


Fig. 10. Sub-threshold drain current as a function of gate-source voltage

$$T_j = 25^\circ\text{C}; V_{DS} = 5\text{V}$$

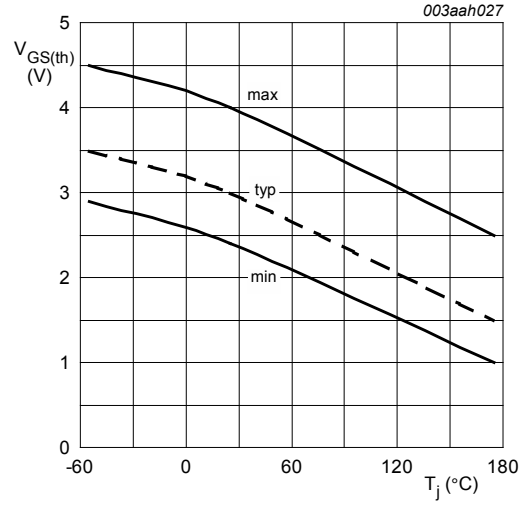


Fig. 11. Gate-source threshold voltage as a function of junction temperature

$$I_D = 1\text{ mA}; V_{DS} = V_{GS}$$

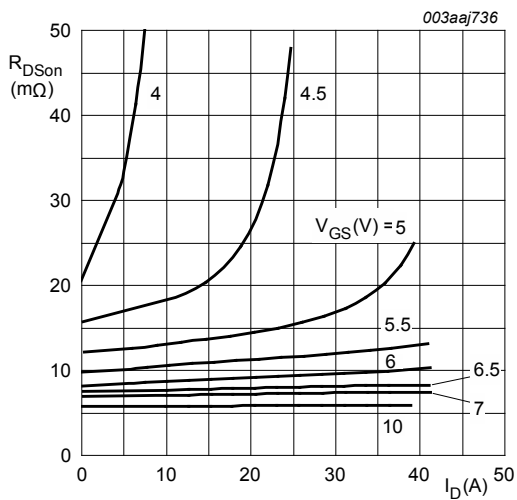


Fig. 12. Drain-source on-state resistance as a function of drain current; typical values

$$T_j = 25^\circ\text{C}$$

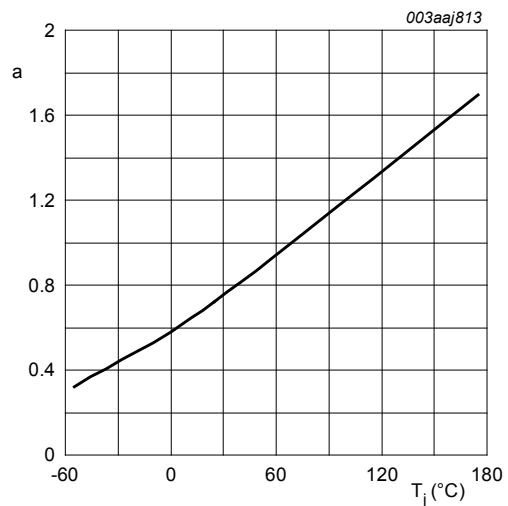


Fig. 13. Normalized drain-source on-state resistance factor as a function of junction temperature

$$a = \frac{R_{DS(on)}}{R_{DS(on)}(25^\circ\text{C})}$$

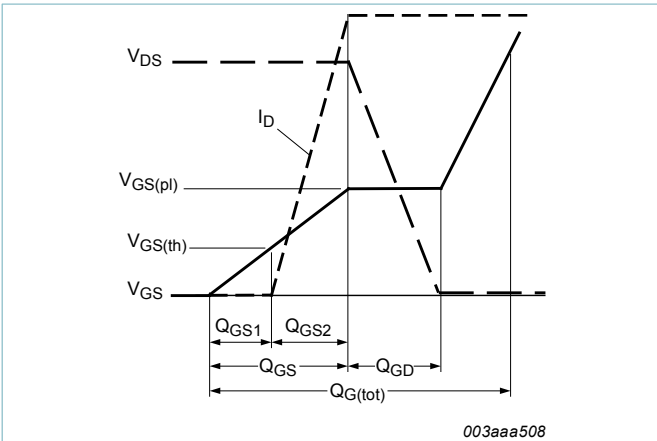


Fig. 14. Gate charge waveform definitions

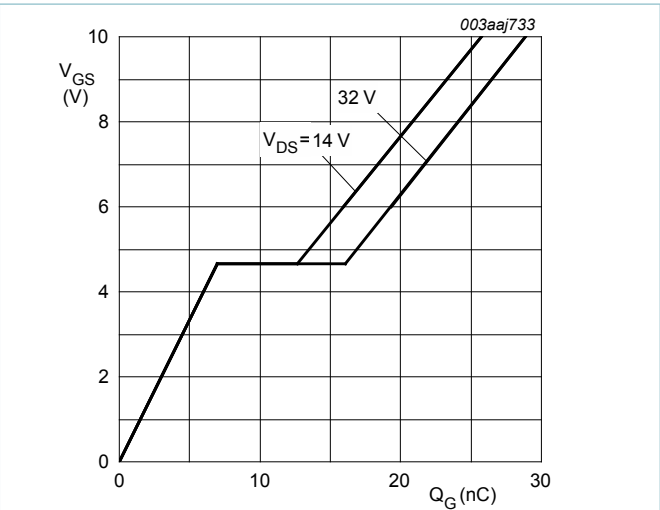


Fig. 15. Gate-source voltage as a function of gate charge; typical values

$T_j = 25^\circ\text{C}; I_D = 20\text{A}$

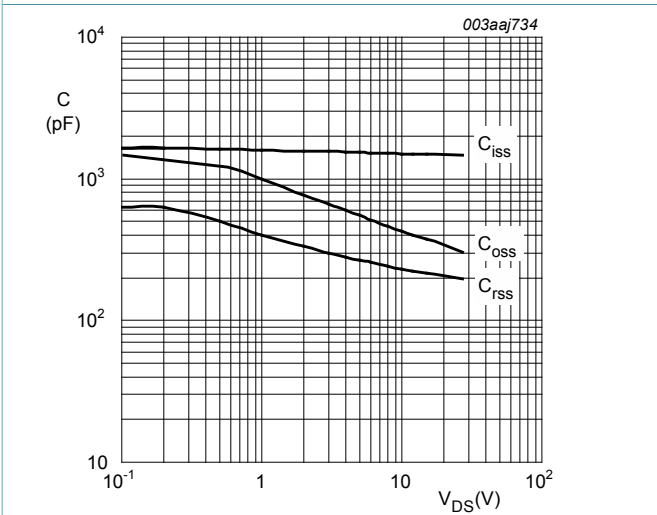


Fig. 16. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values

$V_{GS} = 0\text{V}; f = 1\text{MHz}$

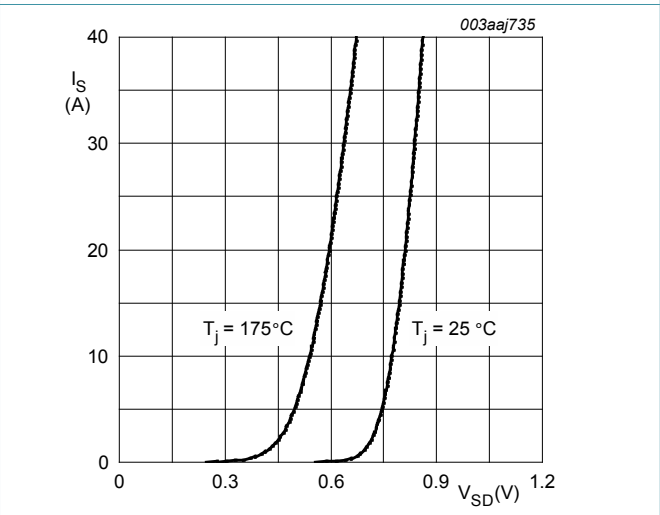


Fig. 17. Source current as a function of source-drain voltage; typical values

$V_{GS} = 0\text{V}$

7. Package outline

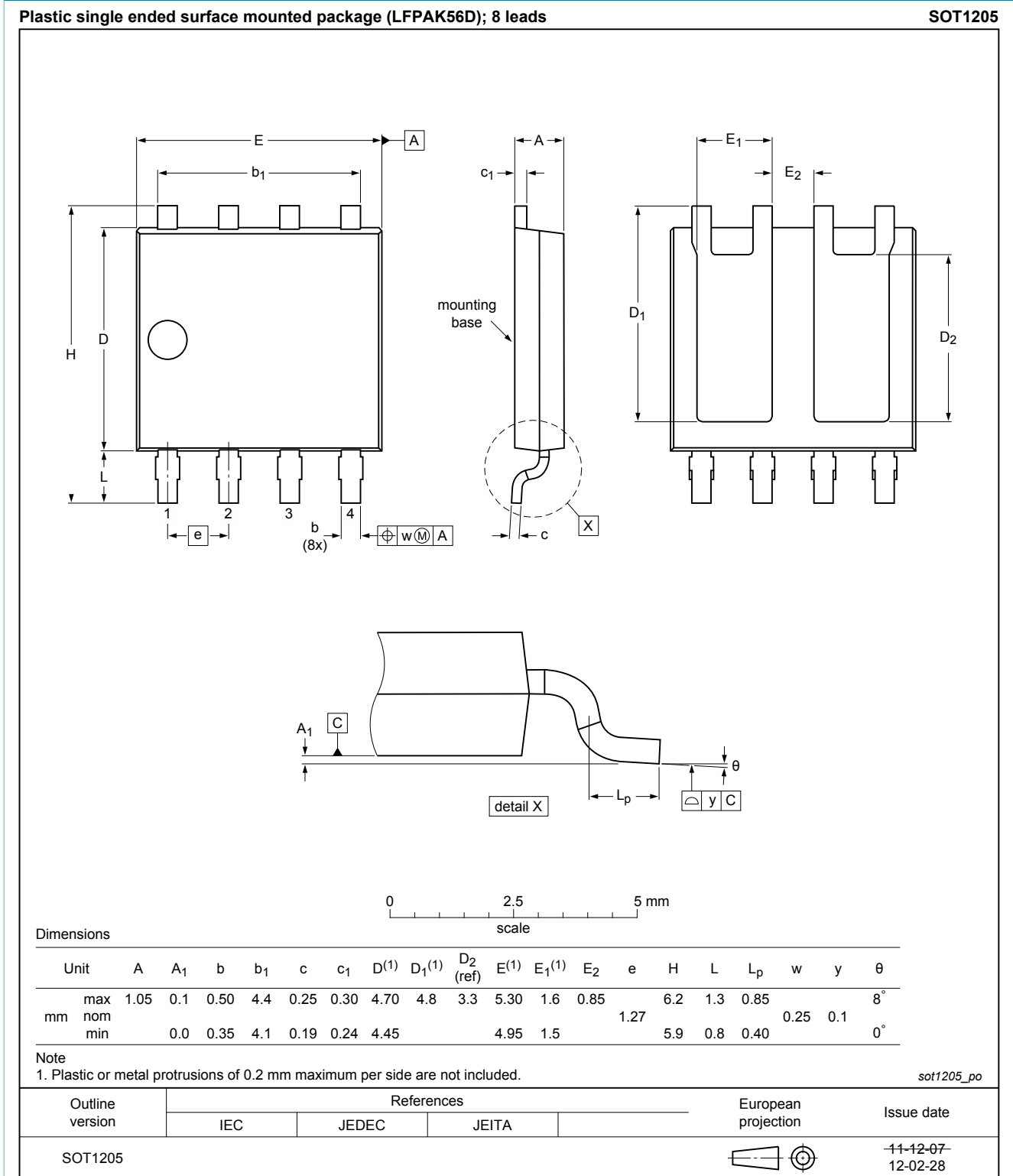


Fig. 18. LPAK56D (SOT1205)

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|--------------------------------|--------------------|---|
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