USER MANUAL

MCIMX6Q-SL: Development Platform for i.MX 6Quad

Board built to Freescale® SABRE Lite design

From element14

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1 Board Overview

1.1 Product Introduction

The development platform for i.MX 6Quad from element14 (built to the Freescale® SABRE Lite design) is an evaluation platform featuring the powerful i.MX 6Q, a multimedia application processor with Quad ARM Cortex-A9 cores at 1.2 GHz from Freescale Semiconductor. The platform helps evaluate the rich set of peripherals and includes a 10/100/Gb Ethernet port, SATA-II, HDMI v1.4, LVDS, parallel RGB interface, touch screen interface, analog headphone/microphone, micro TF and SD card interface, USB, serial port, JTAG, camera interface, and input keys for Android, as shown in Figure 1-1.

The SABRE Lite can be used in the following applications:

- Netbooks (web tablets)
- Nettops (Internet desktop devices)
- High-end mobile Internet devices (MID)
- High-end PDAs
- High-end portable media players (PMP) with HD video capability
- Portable navigation devices (PNDs)
- Industrial control and Test and measurement (T&M)
- Single board computers (SBCs)

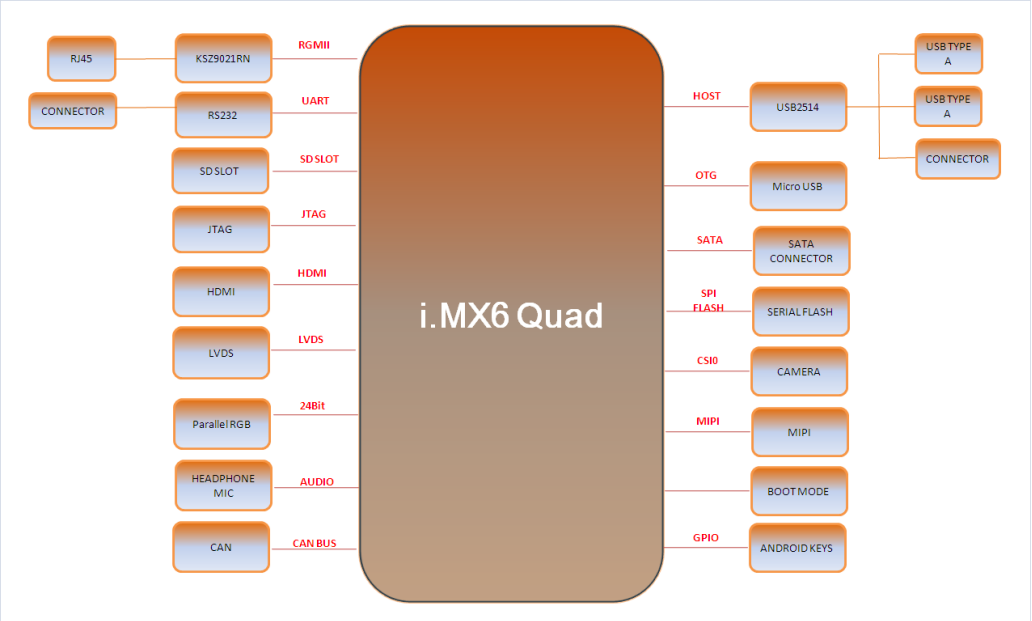
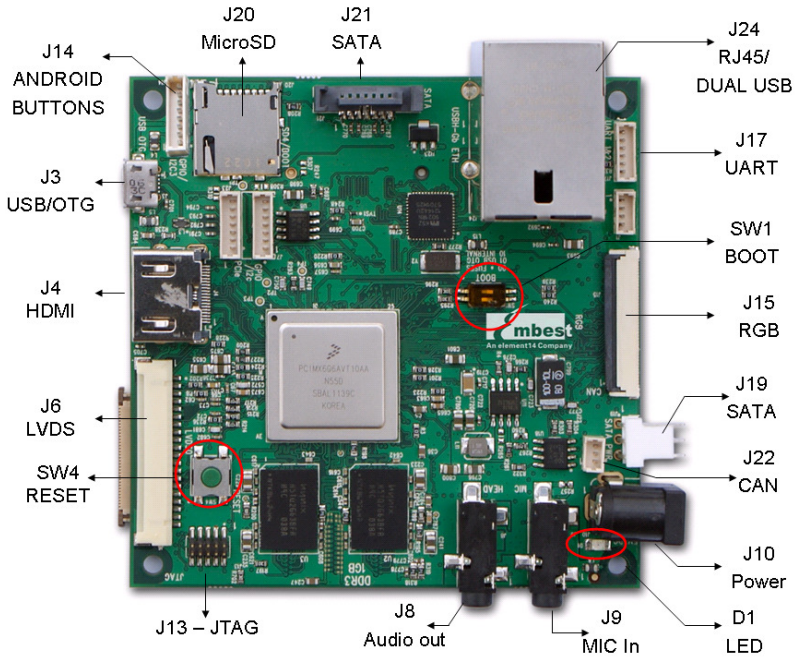


Figure 1-1 Functional Block Diagram of SABRE Lite Board

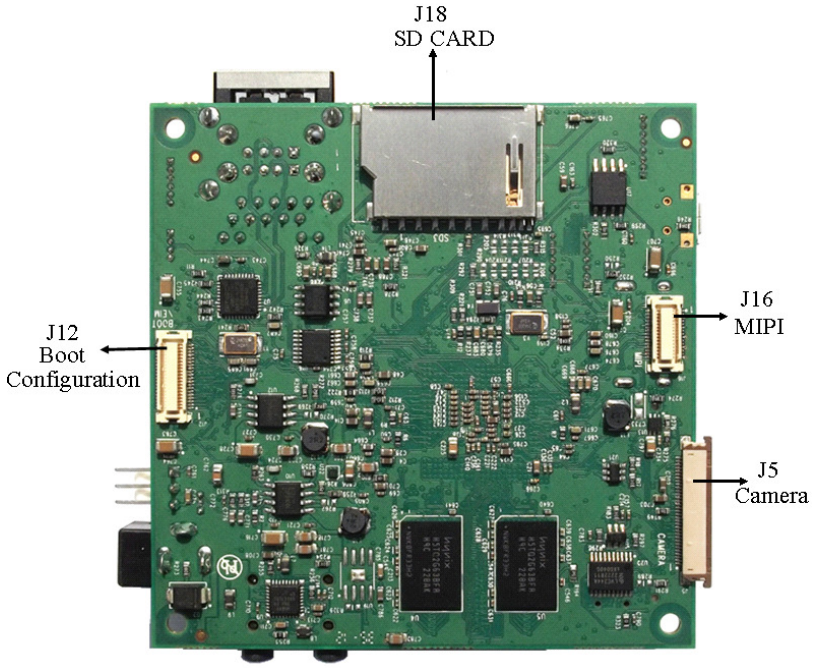
1.2 Features

The SABRE Lite Board is based on the i.MX 6Quad-core processor from Freescale integrating all the functionalities of this multimedia application processor with the following features:

- Mechanical Parameters
  - Working Temperature: 0°C - 70°C
  - Humidity Range: 20% - 90%
  - Dimensions: 82.55mm x 82.55mm
  - Input Voltage: +5V
- Processor
  - ARM Cortex A9 MPCore™ 4xCPU Processor at 1GHz
  - Multi-stream-capable HD video engine delivering H.264 1080p60 decode, 1080p30 encode, and 3-D video playback in HD
  - Triple Play Graphics System consisting of a Quad-shader 3D unit capable of 200MT/s, and a separate 2-D and separate OpenVG Vertex acceleration engines for superior 3D, 2D, and user interface acceleration
- Memories
  - 1GByte of 64-bit wide DDR3 @ 532MHz
  - 2MB SPI FLASH



- Media Interfaces
  - Analog headphone/microphone, 3.5mm audio jack
  - LVDS interface
  - HDMI interface
  - Parallel RGB interface
  - Camera interface (Support CCD or CMOS camera)
  - MIPI lanes at 1 Gbps



- Data Transfer Interfaces
  - Serial Ports
    - UART1, 3 line serial port, RS232 Logic
    - UART2, 3 line serial port, RS232 Logic
  - USB Ports:
    - 1 x USB2.0 OTG, micro USB, high-speed, 480Mbps
    - 2 x USB2.0 HOST, Type A, high-speed, 480Mbps
    - 1 x USB2.0 HOST, connector, high-speed, 480Mbps
  - TF card interface
  - SD card interface
  - SATA II interface, 3.0 Gbps
  - 10M/100M/Gb Ethernet Interface (RJ45 jack)
  - 1 channel I2C interface
  - 1 channel PCIE X1 interface
  - CAN bus
- Input Interfaces
  - Android keyboard interface
  - 10-pin JTAG interface
  - 2 bit DIP switch for boot mode selection
  - Boot configuration interface
- Others
  - 1 Power LED
  - 1 DC Jack
  - 1 Reset button

2 Quick Start Guide

This section describes how to use the SABRE Lite and associated components.

2.1 Unpacking the Kit

The SABRE Lite development kit is shipped with the items listed in Table 2-1. Remove the circuit board from the conductive bag and perform a visual inspection.

Table 2-1 SABRE Lite Kit Contents

Item	Description
Circuit Board	SABRE Lite board
USB cable	Micro-B to standard-A cable
RS-232 cable	Custom serial cable
Serial Cable	Crossover cable – DB9 female to DB9 female
Ethernet cable	Crossover cable to connect the board to host computer
Power Supply	5Vdc @ 4 A power supply
Documentation	Quick-Start Guide
MicroSD Card	The kit includes a MicroSD Card pre-loaded with the Linux BSP from TimeSys

2.2 Web-Based Contents

Please refer to www.element14.com/iMX6 for the latest documents and software, including:

- Schematics
- Board layout
- Bill of Materials (BOM)
- Board Support Packages (BSPs)

2.3 Setting Up the System

2.3.1 Insert MicroSD Card

Insert the supplied MicroSD card into the board's MicroSD card socket J20.
Note: MicroSD Card is included if ready at the date your kit was shipped.
For the latest version of the BSP, please visit www.element14.com/iMX6

2.3.2 Connect RS-232 cable

Connect the custom serial cable provided to serial port J17, and then use cross serial cable to connect to the host computer.
Open a terminal window on the host (eg. Hyperterminal) with serial port configuration: 115.2 kbaud, 8 data bits, 1 stop bit, with no parity.

2.3.3 Connect USB OTG (optional)

Connect the cable from the kit to micro USB connector J3 on the board.

2.3.4 Connect the Power Supply

Plug in the 5Vdc supply to power jack J10, the power LED (D1) should illuminate.
To re-boot, press the reset button SW4.

3 Hardware Description

3.1 Processor

The i.MX 6Dual/6Quad processors represents Freescale Semiconductor's latest achievement in integrated multimedia applications processors, which are part of a growing family of multimedia-focused products that offer high performance processing and are optimized for lowest power consumption.

The processor features Freescale's advanced implementation of the quad ARM™ Cortex-A9 core, which operates at speeds up to 1GHz. They include 2D and 3D graphics processors, 3D 1080p video processing, and integrated power management. Each processor provides a 64-bit DDR3/LVDDR3-1066 memory interface and a number of other interfaces for connecting peripherals, such as WLAN, Bluetooth™, GPS, hard drive, displays, and camera sensors.

3.1.1 Core Features

The i.MX 6Dual/6Quad processors are based on the ARM Cortex A9 MPCore™ platform with the following features:

- ARM Cortex A9 MPCore™ 4xCPU Processor (with TrustZone)
- The core configuration is symmetric, where each core includes:
  - 32 KByte L1 Instruction Cache
  - 32 KByte L1 Data Cache
  - Private Timer and Watchdog
  - Cortex-A9 NEON MPE (Media Processing Engine) Co-processor
- The ARM Cortex A9 MPCore™ complex includes:
  - General Interrupt Controller (GIC) with 128 interrupt support
  - Global Timer
  - Snoop Control Unit (SCU)
  - 1 MB unified I/D L2 cache, shared by two/four cores
  - Two Master AXI (64-bit) bus interfaces output of L2 cache
  - Target frequency of the core (including Neon and L1 cache) is:
    - 1 GHz overdrive over the specified temperature rang
    - 900 MHz non-overdrive over the specified temperature range
  - NEON MPE coprocessor
    - SIMD Media Processing Architecture
    - NEON register file with 32x64bit general-purpose registers
    - NEON Integer execute pipeline (ALU, Shift, MAC)
    - NEON dual, single-precision floating point execute pipeline (FADD, FMUL)
    - NEON load/store and permute pipeline
- The memory system consists of the following components:
  - Level 1 Cache--32 KB Instruction, 32 KB Data cache per core
  - Level 2 Cache--Unified instruction and data (1 MByte)
  - On-Chip Memory:
    - Boot ROM, including HAB (96 KB)
    - Internal multimedia / shared,fast access RAM (OCRAM, 256 KB)
    - Secure/non-secure RAM (16 KB)

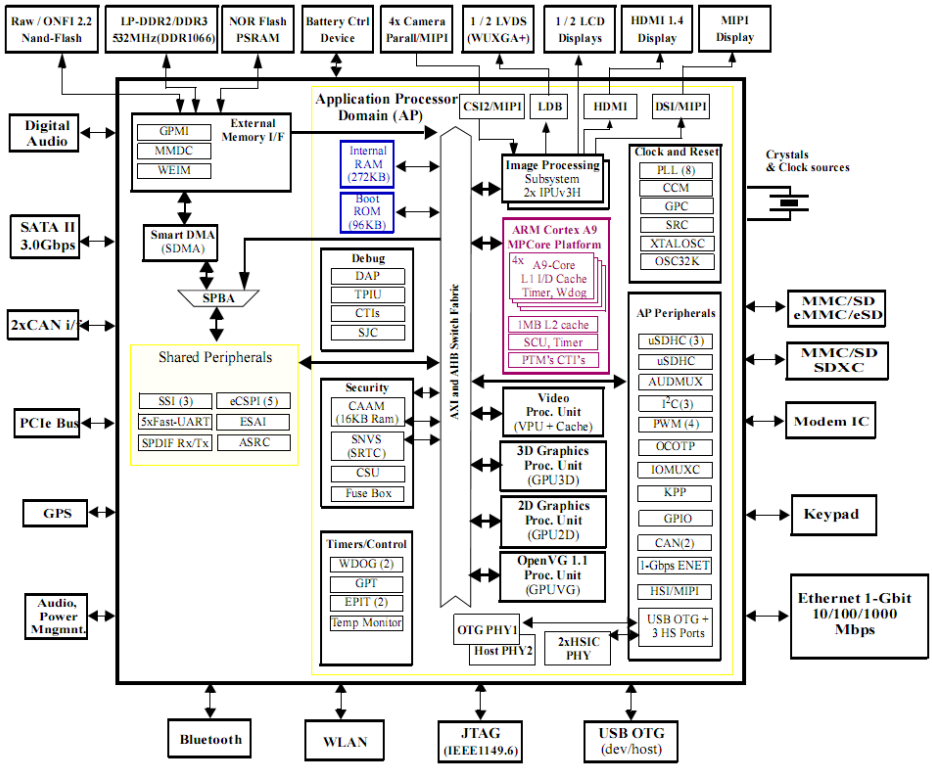


Figure 3-1 Block Diagram of i.MX 6Dual/6Quad

3.1.2 External memory interfaces:

- 16-bit, 32-bit, and 64-bit DDR3-1066,LV-DDR3-1066, and 1/2 LPDDR2-1066 channels, supporting DDR interleaving mode, for 2x32 LPDDR2-1066
- 8-bit NAND-Flash, including support for Raw MLC/SLC, 2 KB, 4 KB, and 8 KB page size, BA-NAND, PBA-NAND, LBA-NAND, OneNAND™ and others. BCH ECC up to 32 bit.
- 16-bit NOR Flash. All WEIMv2 pin are muxed on other interfaces.
- 16-bit PSRAM, Cellular RAM

3.1.3 Interface to external devices

Each i.MX 6Dual/6Quad processor enables the following interfaces to external devices (some of them are muxed and not available simultaneously):

- Hard Disk Drives--SATA II, 3.0 Gbps
- Displays--Total five interfaces available. Total raw pixel rate of all interfaces is up to 450 Mpixels/sec, 24 bpp. Up to four interfaces may be active in parallel.
  - One Parallel 24-bit display port, up to 225 Mpixes/sec (for example, WUXGA at 60 Hz or dual HD1080 and WXGA at 60 Hz)
  - LVDS serial ports!aOne port up to 165 Mpixels/seor two ports up to 85 MP/sec (for example, WUXGA at 60 Hz) each
  - HDMI 1.4 port
  - MIPI/DSI, two lanes at 1 Gbps
  -

- Camera sensors:
  - Parallel Camera port (up to 20 bit and up to 240 MHz peak)
  - MIPI CSI-2 serial camera port, supporting up to 1000 Mbps/lane in 1/2/3-lane mode and up to

800 Mbps/lane in 4-lane mode. The CSI-2 Receiver core can manage one clock lane and up to four data lanes. Each i.MX 6Dual/6Quad processor has four lanes.

- Expansion cards:
  - Four MMC/SD/SDIO card ports all supporting:
  - 1-bit or 4-bit transfer mode specifications for SD and SDIO cards up to UHS-I SDR-104 mode (104 MB/s max)
  - 1-bit, 4-bit, or 8-bit transfer mode specifications for MMC cards up to 52 MHz in both SDR and DDR modes (104 MB/s max)
- USB
  - High Speed (HS) USB 2.0 OTG (Up to 480 Mbps), with integrated HS USB PHY
  - Three USB 2.0 (480 Mbps) hosts
  - One HS host with integrated High Speed PHY
  - Two HS hosts with integrated HS-IC USB (High Speed Inter-Chip USB) PHY
- Expansion PCI Express port (PCIe) v2.0 one lane
  - PCI Express (Gen 2.0) dual mode complex, supporting Root complex operations and Endpoint operations. Uses x1 PHY configuration.
- Miscellaneous IPs and interfaces:
  - Three I2S/SSI/AC97,up to 1.4 Mbps each
  - Enhanced Serial Audio Interface ESAI), up to 1.4 Mbps per channel
  - Five UARTs, up to 4.0 Mbps each
  - Providing RS232 interface
  - Supporting 9-bit RS485 multidrop mode
  - One of the five UARTs (UART1) supports 8-wir while others four supports 4-wire. This is due to the SoC IOMUX limitation, since all UART IPs are identical.
  - Five eCSPI (Enhanced CSI), up to 52 Mbps each
  - Three I2C, supporting 400 kbps
  - Gigabit Ethernet Controller(IEEE1588 compliant), 10/100/1000 Mbps
  - Four Pulse Width Modulators (PWM)
  - System JTAG Controller (SJC)
  - GPIO with interrupt capabilities
  - 8x8 Key Pad Port (KPP)
  - Sony Philips Digital Interface (SPDIF), Rx and Tx
  - Two Controller Area Network (FlexCAN), 1 Mbps each
  - Two Watchdog timers (WDOG)
  - Audio MUX (AUDMUX)

3.1.4 Advanced Power Management unit

The i.MX 6Dual/6Quad processors integrate advanced power management unit and controllers:

- Provide PMU, including DCDC and LDO supplies, for on-chip resources
- Use Temperature Sensor for monitoring the die temperature
- Support DVFS techniques for low power modes
- Use SW State Retention and Power Gating for ARM and MPE
- Support various levels of system power modes
- Use flexible clock gating control scheme

3.1.5 Hardware Accelerators

The i.MX 6Dual/6Quad processors use dedicated HW accelerators to meet the targeted multimedia performance. The use of HW accelerators is a key factor in obtaining high performance at low power consumption numbers, while having the CPU core relatively free for performing other tasks.

The i.MX 6Dual/6Quad processors incorporate the following hardware accelerators:

- VPU--Video Processing Unit
- IPUv3H--Image Processing Unit version 3H (2 IPUs)
- GPU3Dv4--3D Graphics Processing Unit (OpenGL ES 2.0) version
- GPU2Dv2--2D Graphics Processing Unit (BitBlt)
- GPUVG—Open VG 1.1 Graphics Processing Unit
- ASRC--Asynchronous Sample Rate Converter
- Security functions are enabled and accelerated by the following hardware:
- ARM TrustZone including the TZ architecture (separation of interrupts, memory mapping, etc.)
- SJC--System JTAG Controller. Protecting JTAG from debug port attacks by regulating or blocking the access to the system debug features.
- CAAM--Cryptographic Acceleration and Assurance Module, containing 16 KB secure RAM and True and Pseudo Random Number Generator (NIST certified)
- SNVS--Secure Non-Volatile Storage, including Secure Real Time Clock
- CSU--Central Security Unit. Enhancement for the IC Identification Module (IIM). Will be configured during boot and by eFUSEs and will determine the security level operation mode as well as the TZ policy.
- A-HAB Advanced High Assurance Boot--Hv4 with the new embedded enhancements:
- SHA-256, 2048-bit RSA key, version control mechanism, warm boot, CSU, and TZ initialization.

3.2 Expanded Chip Introduction

3.2.1 H5TQ2G63BFR-H9C

The board has 1GB of SDRAM (4x256MB). The H5TQ2G63BFR is a 256MB DDR3 Synchronous DRAM, ideally suited for the main memory applications which require large memory density and high bandwidth.

3.2.2 SST25VF016B

The serial EPROM SST25VF016B is a 16Mb SPI Serial Flash used for boot code storage. Booting from serial EPROM is recommended.

3.2.3 KSZ9021RN

The KSZ9021RN is a single-port 10/100/1000Base-T Gigabit transceiver in industry's smallest footprint, supporting data transfer over standard CAT-5 unshielded twisted pair cable. This device offers robust performance and low power consumption. On-chip integration of termination resistors and LDO controller, along with built-in diagnostic features, significantly reduces the cost and the complexity of Gigabit Ethernet applications. This device is ideal for enabling Gigabit Ethernet performance in SOHO and SMB networking applications, such as SOHO media center, wired/wireless Gigabit SOHO/SMB router, and VoIP gateway.

The SABRE Lite can be connected to a network hub directly through a cable. It also can be directly connected with a computer through a crossover cable which is provided with the kit.

3.2.4 USB2514B-AEZG for USB 2.0 High Speed 4-Port Hub

The USB2514 hub is a family of low-power, OEM configurable, MTT (multi transaction translator) hub controller IC with 4 downstream ports for embedded USB solutions. The SMSC hub supports low-speed, full-speed, and hi-speed (if operating as a hi-speed hub) downstream devices on all of the enabled downstream ports.

3.2.5 SGTL5000

The SGTL5000 is a low power stereo Codec with Headphone Amp from Freescale, and is designed to provide a complete audio solution for portable products needing line-in, mic-in, line-out, headphone-out, and digital I/O. Deriving its architecture from best-in-class Freescale-integrated products currently on the market, the SGTL5000 is able to achieve ultra low-power with very high performance and functionality, all in one of the smallest footprints available.

Designed with features such as capless headphone and an integrated PLL to allow clock reuse within the system, it helps customers achieve a lower overall system cost.

3.2.6 ICL3232CVZ

The Intersil ICL32XX X interface ICs operate from a single +3V to +5.5V supply, guarantee a 250kbps minimum data rate, require only four small external 0.1µF capacitors, feature low power consumption, and meet all EIA RS-232C and V.28 specifications. Targeted applications are PDAs, Palmtops, and notebook and laptop computers where the low operational and even lower standby, power consumption is critical.

3.2.7 TJA1040T

The TJA1040, a High Speed CAN transceiver is the interface between the Controller Area Network (CAN) protocol controller and the physical bus. It is primarily intended for high speed applications, up to 1MBaud, in passenger cars. The device provides differential transmit capability to the bus and differential receive capability to the CAN controller.

3.3 Hardware Interface

3.3.1 Power Input Jack

The 5V/4A AC-to-DC power supply that comes with the board is plugged into the Power Jack (J10) on the board. *It is not recommended to use a higher voltage since possible damage to the board may result due to failure of the protection circuitry.*

Figure 3-2 Power input jack

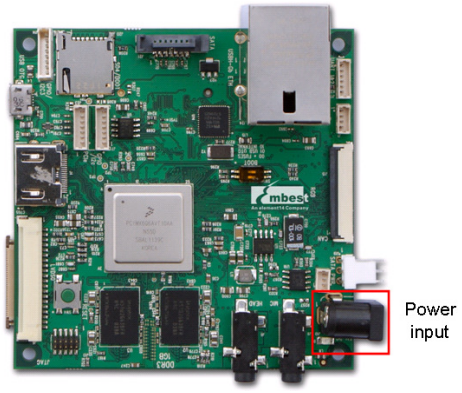


Table 3-1 Power Interface

J10		
Pin	Signal	Function
1	GND	GND
2	NC	NC
3	+5V	Power supply (+5V) 2A (Type)

3.3.2 SATA Power Interface

A 3-pin SATA power connector for 2.5 inch SATA hard disk is shown in Figure 3-3 below.

Figure 3-3 SATA Power Interface

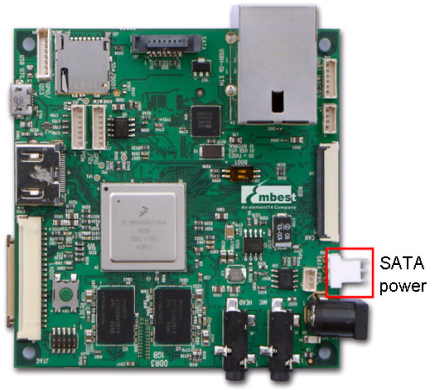


Table 3-2 SATA Power Interface

J19		
Pin	Signal	Function
1	+3.3V	3.3V output
2	GND	GND
3	+5V	5V output

3.3.3 SATA Data Interface

A SATA 7-pin data connector (J21) is provided on the Quick Start Board and is connected to the SATA module of the i.MX6 processor. The SABRE Lite board is capable of communicating with any standard SATA device, such as a hard drive or optical DVD/CD reader. The SATA data cable is plugged into the SABRE Lite board at the location shown in Figure 3-4.

Figure 3-4 SATA connector

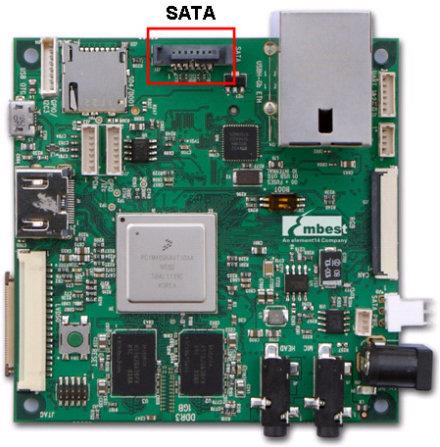


Table 3-3 SATA Connector

J21		
Pin	Signal	Function
1	GND	GND
2	SATA_TXP	SATA receive data(positive)
3	SATA_TXN	SATA receive data(negative)
4	GND	GND
5	SATA_RXN	SATA transmit data(negative)
6	SATA_RXP	SATA transmit data(positive)
7	GND	GND

3.3.4 CAN Interface

Figure 3-5 CAN Interface

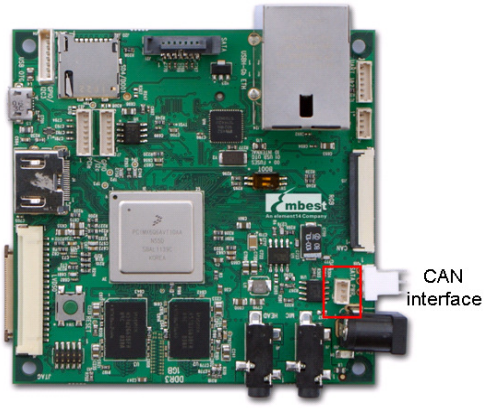


Table 3-4 CAN Interface

J22		
Pin	Signal	Function
1	CANH	CAN differential pairs high level
2	GND	GND
3	CANL	CAN differential pairs low level

3.3.5 Parallel RGB Interface

Figure 3-6 Parallel RGB Interface

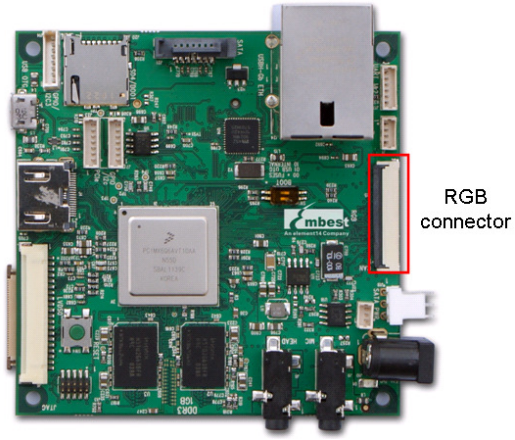


Table 3-5 Parallel RGB interface

J15		
Pin	Signal	Function
1	GND	GND
2	GND	GND
3	GND	GND
4	DISP0_CNTRST	GPIO
5	R0	DISP0 data bit16
6	R1	DISP0 data bit17
7	R2	DISP0 data bit18
8	R3	DISP0 data bit19
9	R4	DISP0 data bit 20
10	R5	DISP0 data bit 21
11	R6	DISP0 data bit 22
12	R7	DISP0 data bit 23
13	G0	DISP0 data bit 8
14	G1	DISP0 data bit 9
15	G2	DISP0 data bit10
16	G3	DISP0 data bit 11
17	G4	DISP0 data bit 12
18	G5	DISP0 data bit 13
19	G6	DISP0 data bit 14
20	G7	DISP0 data bit 15
21	B0	DISP0 data bit 0
22	B1	DISP0 data bit 1
23	B2	DISP0 data bit 2
24	B3	DISP0 data bit 3
25	B4	DISP0 data bit 4
26	B5	DISP0 data bit 5
27	B6	DISP0 data bit6
28	B7	DISP0 data bit 7
29	GND	GND
30	DISP0_CLK	Pixel Clock
31	GND	GND
32	DISP0_HSYNC	DISP0 HSYNC
33	DISP0_VSYNC	DISP0 VSYNC
34	DISP0_DRDY	DISP0 enable chip select
35	I2C3_SCL	IIC master serial clock,

36	I2C3_SDA	IIC serial bidirectional data,
37	PWM1	Backlight brightness control
38	5VIN	+5V
39	5VIN	+5V
40	5VIN	+5V

3.3.6 Audio Output Jack

A headphone with a standard 3.5mm stereo jack can be connected to the Audio Output jack at the point shown in Figure3-7.

Figure 3-7 Audio Output Jack

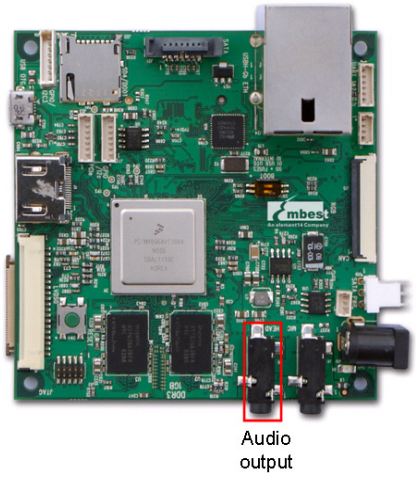


Table 3-6 Audio Output Jack

J8		
Pin	Signal	Function
1	GND_ANALOG	ANALOG GND
2	HP_L	Left output
3	HP_R	Right output
10	Default set	Pull down 10k resister

3.3.7 Microphone Input Jack

The SABRE Lite board provides a 3.5mm stereo connector for a microphone input, as shown in Figure 3-8. A mono microphone will input its signal though the tip of the 3.5mm plug.

Figure 3-8 MIC In Jack

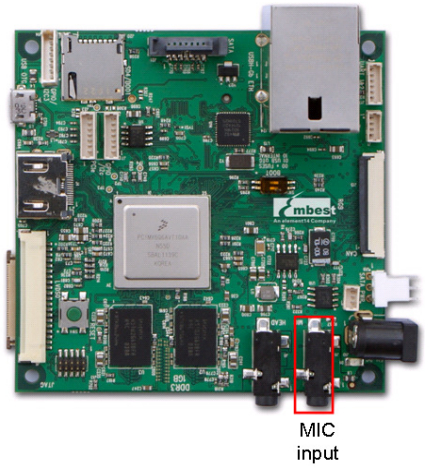


Table 3-7 MIC In Jack

J9		
Pin	Signal	Function
1	GND_ANALOG	ANALOG GND
2	MIC_IN_P	MIC input
3	NC	NC
10	MIC_DET	MIC input Jack detect

3.3.8 Camera Interface

Table 3-8 Camera Interface

J5		
Pin	Signal	Function
1	GND	GND
2	CSI0_DAT19	CSI0 capture data bit 19
3	CSI0_DAT18	CSI0 capture data bit 18
4	CSI0_DAT17	CSI0 capture data bit 17
5	CSI0_DAT16	CSI0 capture data bit 16
6	CSI0_DAT15	CSI0 capture data bit 15
7	CSI0_DAT14	CSI0 capture data bit 14
8	CSI0_DAT13	CSI0 capture data bit 13

9	CSI0_DAT12	CSI0 capture data bit 12
10	CSI0_DAT11	CSI0 capture data bit 11
11	CSI0_DAT10	CSI0 capture data bit 10
12	CSI0_DAT9	CSI0 capture data bit 9
13	CSI0_DAT8	CSI0 capture data bit 8
14	I2C2_SCL	I2C2 serial clock
15	I2C2_SDA	I2C2 serial data
16	GND	GND
17	GPIO_3_CLKO2	GPIO
18	GND	GND
19	2P5V	2P5V
20	2P5V	2P5V
21	2P5V	2P5V
22	2P5V	2P5V
23	GND	GND
24	CSI0_DATA_EN	CSI0 DATA enable
25	GND	GND
26	CSI0_RST	CSI0 Reset
27	CSI0_VSYNC	CSIO VSYNC
28	CSI0_HSYNC	CSIO HSYNC
29	GND	GND
30	CSI0_PIXCLK	CSI0 pixel clock
31	GPIO6	GPIO
32	GND	GND
33	GPIO1_16	GPIO

3.3.9 RS232 Serial Port

Figure 3-9 RS232 Serial Port

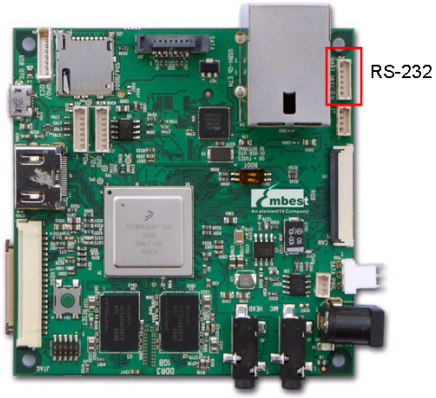


Table 3-9 RS-232 Serial Port

J17		
Pin	Signal	Function
1	UART1_TXD	UART1 Transmit data
2	5VIN	5V
3	GND	GND
4	UART2_TXD	UART2 Transmit data
5	UART2_RXD	UART2 Receive data
6	UART1_RXD	UART1 Receive data

3.3.10 RGMII LAN Interface

A standard CAT-V Ethernet cable is attached to the Quick Start board at the Ethernet/Dual USB connector J24. The connector contains integrated magnetic which allows the Ethernet IC to auto configure the port for the correct connection to either a switch or directly to a host PC on a peer-to-peer network. It is not necessary to use a crossover cable when connecting directly to another computer. The Ethernet/Dual USB connector is shown in Figure 3-10.

Figure 3-10 RGMII LAN Interface

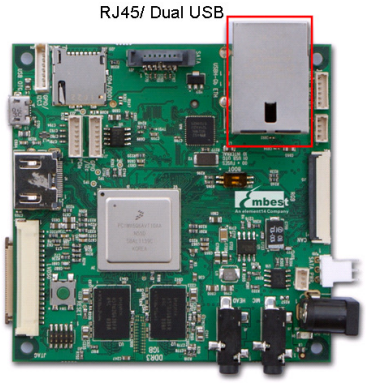


Table 3-10 RGMII LAN interface

J24A		
Pin	Signal	Function
9	NC	NC
10	TXRXP_A	differential pair TXRX+
11	TXRXM_A	differential pair TXRX-
12	TXRXP_B	differential pair TXRX+
13	TXRXM_B	differential pair TXRX+
14	TXRXP_C	differential pair TXRX+
15	TXRXM_C	differential pair TXRX+
16	TXRXP_D	differential pair TXRX+
17	TXRXP_D	differential pair TXRX+
18	YEL	Link LED
19	GRN	Speed LED
20	3P3V	3.3V
21	YEL	Link LED
22	3P3V	3.3V
23	GND_DVI	GND

3.3.11 USB Host Interface

Table 3-11 USB Host Interface

J24B		
Pin	Signal	Function
1	USB1_VBUS	+5V
2	USB1_D-	USB Data-
3	USB1_D+	USB Data+
4	GND	GND

5	USB2_VBUS	+5V
6	USB2_D-	USB Data-
7	USB2_D+	USB Data+
8	GND	GND

Table 3-12 USB Host Interface

J1		
Pin	Signal	Function
1	5VIN	+5V
2	USBDN_DM3	USB Data-
3	USBDN_DP3	USB Data+
4	GND	GND

3.3.12 Micro USB Interface

The micro connector is connected to the high-speed (HS) USB 2.0 OTG module of the i.MX 6 processor and is cross connected with the lower USB Host port on J3. When a 5V supply is seen on the micro connector (from the USB Host), the i.MX 6Q processor will configure the OTG module for device mode, which will prevent the lower USB Host port from operating correctly.

Figure 3-11 Micro USB Interface

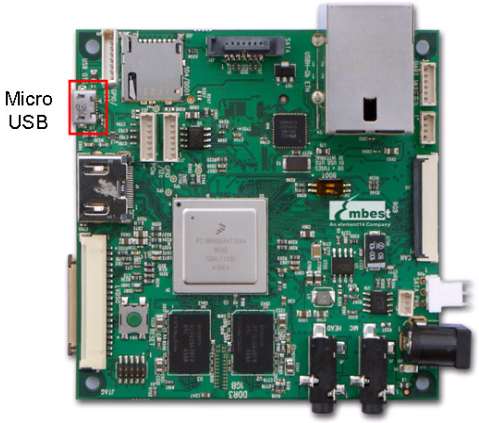


Table 3-13 Micro USB Interface

J3		
Pin	Signal	Function
1	USB0_VBUS	+5V
2	USB0_D-	USB Data-
3	USB0_D+	USB Data+
4	ID	USB ID
5	GND	GND

3.3.13 SD Card Interface

Table 3-14 SD Card Interface

J18		
Pin	Signal	Function
1	SD3_DAT3	Card data 3
2	SD3_CMD	Command Signal
3	GND	GND
4	3P3V	3P3V
5	SD3_CLK	Clock
6	VSS	GND
7	SD3_DAT0	Card data 0
8	SD3_DAT1	Card data 1
9	SD3_DAT2	Card data 2
10	SD3_CD	Card detect
11	SD3_WP	Card write protected
12	GND	GND
13	GND	GND
14	GND	GND
15	GND	GND

3.3.14 JTAG Interface

Table 3-15 JTAG Interface

J13		
Pin	Signal	Function
1	3P3V	3.3V
2	JTAG_TMS	Test mode select
3	GND	GND
4	JTAG_TCK	Test clock
5	GND	GND
6	JTAG_TDO	Test data output
7	JTAG_MOD	Test mode
8	JTAG_TDI	Test data input
9	JTAG_nTRST	Test system reset
10	RESET_N	RESET for TPS3808

3.3.15 Expansion Interface

Table 3-16 IIC expansion interface

J7		
Pin	Signal	Function
1	5VIN	5V
2	5VIN	5V
3	5VIN	5V
4	GPIO9	GPIO
5	I2C3_SCL	IIC3 serial clock
6	I2C3_SDA	IIC3 serial data
7	GND	GND

3.3.16 Boot Configuration Select

Table 3-17 Boot Configuration Select

J12		
Pin		Function
1	EIM_A23	BOOT_CFG3[7]
2	EIM_DA0	BOOT_CFG1[0]
3	EIM_A22	BOOT_CFG3[6]
4	EIM_DA1	BOOT_CFG1[1]
5	EIM_A21	BOOT_CFG3[5]
6	EIM_DA2	BOOT_CFG1[2]
7	EIM_A20	BOOT_CFG3[4]
8	EIM_DA3	BOOT_CFG1[3]
9	EIM_A19	BOOT_CFG3[3]
10	EIM_DA4	BOOT_CFG1[4]
11	EIM_A18	BOOT_CFG3[2]
12	EIM_DA5	BOOT_CFG1[5]
13	EIM_A17	BOOT_CFG3[1]
14	EIM_DA6	BOOT_CFG1[6]
15	EIM_A16	BOOT_CFG3[0]
16	EIM_DA7	BOOT_CFG1[7]
17	EIM_EB3	BOOT_CFG4[7]
18	EIM_DA8	BOOT_CFG2[0]]
19	EIM_EB2	BOOT_CFG4[6]
20	EIM_DA9	BOOT_CFG2[1]

21	EIM_RW	BOOT_CFG4[5]
22	EIM_DA10	BOOT_CFG2[2]
23	EIM_EB1	BOOT_CFG4[4]
24	EIM_DA11	BOOT_CFG2[3]
25	EIM_EB0	BOOT_CFG4[3]
26	GND	GND
27	EIM_LBA	BOOT_CFG4[2]
28	EIM_DA12	BOOT_CFG2[4]
29	GND	GND
30	GND	GND
31	EIM_WAIT	BOOT_CFG4[1]
32	EIM_DA13	BOOT_CFG2[5]
33	GND	GND
34	GND	GND
35	EIM_A24	BOOT_CFG4[0]
36	EIM_DA14	BOOT_CFG2[6]
37	3P3V	3.3V
38	GND	GND
39	3P3V	3.3V
40	EIM_DA15	BOOT_CFG2[7]

3.3.17 ANDROID KEYBOARD INTERFACE

Table 3-18 ANDROID BUTTONS

J14		
Pin		Function
1	ON_OFF	GPIO
2	KEY_VOL_UP	GPIO
3	HOME	GPIO
4	SEARCH	GPIO
5	BACK	GPIO
6	MENU	GPIO
7	KEY_VOL_DN	GPIO
8	GND	GPIO

3.3.18 LED

Table 3-19 LED

LED		
Pin	Signal	Function
D1	Power led	5V power indicator

3.3.19 Switch

Table 3-20 Reset Switch

SW4		
Pin	Signal	Function
1	NC	NC
2	GND	GND
3	RESET_N	System Reset
4	NC	GND

Table 3-21 Boot Switch

SW1		
Pin	Signal	Function
1	BOOT_MODE1	Boot mode detect
2	BOOT_MODE0	Boot mode detect
3	3P3V	3.3V
4	3P3V	3.3V

3.3.20 TF/MMC Card Interface

The micro SD Card Connector (J20) connects a 4-bit parallel data bus to the SD4 port of the i.MX 6 processor. The micro SD Card is inserted facing up at the location shown in Figure 3-12.

Figure 3-12 TF/MMC Card Interface

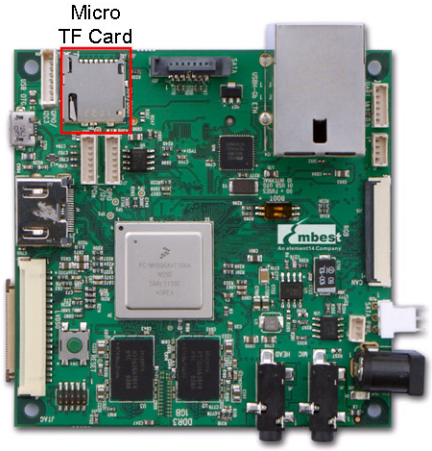


Table 3-22 TF/MMC Card Interface

J20		
Pin	Signal	Function
1	SD4_DAT2	Card data 2
2	SD4_DAT3	Card data 3
3	CMD	Card command signal
4	3P3V	3P3V
5	SD4_CLK	Card clock
6	VSS	GND
7	SD4_DAT0	Card data 0
8	SD4_DAT1	Card data 1
9	NC	NC
11	GND	GND
12	SD4_CD	Card detect

3.3.21 HDMI Interface

Table 3-23 HDMI Interface

J4		
Pin	Signal	Function
1	HDMI_D2P	HDMI differential pairs data2+

2	GND	GND
3	HDMI_D2M	HDMI differential pairs data2-
4	HDMI_D1P	HDMI differential pairs data1+
5	GND	GND
6	HDMI_D1M	HDMI differential pairs data1-
7	HDMI_D0P	HDMI differential pairs data0+
8	GND	GND
9	HDMI_D0M	HDMI differential pairs data0-
10	HDMI_CLKP	HDMI differential pairs clock+
11	GND	GND
12	HDMI_CLKM	HDMI differential pairs clock-
13	NC	NC
14	NC	NC
15	BI2C2_SCL	IIC2 serial clock
16	BI2C2_SDA	IIC2 serial data
17	GND	GND
18	5Vin	5V
19	HDMI_HPD	HDMI detect
20	GNF_DVI	GND

3.3.22 LVDS Interface

Table 3-24 LVDS Interface

J6		
Pin	Signal	Function
1	3P3V	3.3V
2	3P3V	3.3V
3	GND	GND
4	GND	GND
5	LVDS0_TX0_N	LVDS0 transmit differential pairs data0-
6	LVDS0_TX0_P	LVDS0 transmit differential pairs data0+
7	GND	GND
8	LVDS0_TX1_N	LVDS0 transmit differential pairs data1-
9	LVDS0_TX1_P	LVDS0 transmit differential pairs data1+
10	GND	GND
11	LVDS0_TX2_N	LVDS0 transmit differential pairs data2-
12	LVDS0_TX2_P	LVDS0 transmit differential pairs data2+

13	GND	GND
14	LVDS0_CLK_N	LVDS0 transmit differential pairs clock-
15	LVDS0_CLK_P	LVDS0 transmit differential pairs clock+
16	GND	GND
17	LVDS0_TX3_N	LVDS0 transmit differential pairs data3-
18	LVDS0_TX3_P	LVDS0 transmit differential pairs data3+
19	DISP0_CONTRAST	GPIO
20	PWM4	Backlight brightness control

3.3.23 MIPI Interface

Table 3-25 MIPI Interface

J16		
Pin	Signal	Function
1	CSI_D0M	CSI differential pairs data0-
2	5VIN	5V
3	CSI_D0P	CSI differential pairs data0+
4	5VIN	5V
5	GND	GND
6	I2C2_SDA	IIC2 serial data
7	CSI_D1M	CSI differential pairs data1-
8	I2C2_SCL	IIC2 serial clock
9	CSI_D1P	CSI differential pairs data1+
10	PWM3	PWM3
11	GND	GND
12	MIPI_BAKLGT_ON	backlight power enable
13	CSI_D2M	CSI differential pairs data2-
14	NANDF_D5	GPIO
15	CSI_D2P	CSI differential pairs data2+
16	DSI_D0P	DSI differential pairs data0+
17	GND	GND
18	DSI_D0M	DSI differential pairs data0-
19	CSI_D3M	CSI differential pairs data3-
20	GND	GND
21	CSI_D3P	CSI differential pairs data3+
22	DSI_CLK0P	DSI differential pairs clock0+
23	GND	GND

24	DSI_CLK0M	DSI differential pairs clock0-
25	CSI_CLK0M	CSI differential pairs clock0-
26	GND	GND
27	CSI_CLK0P	CSI differential pairs clock0+
28	DSI_D1P	DSI differential pairs data1+
29	GND	GND
30	DSI_D1M	DSI differential pairs data1-

3.3.24 PCIe Interface

Table 3-26 PCIe Interface

J23		
Pin	Signal	Function
1	3P3V	3.3V
2	PCIE_RXM	PCIE receive differential pairs data-
3	PCIE_RXP	PCIE receive differential pairs data+
4	PCIE_TXM	PCIE transmit differential pairs data-
5	PCIE_TXP	PCIE transmit differential pairs data+
6	GND	GND
7	GND	GND

4 Software Description

4.1 Software Overview- Linux

4.1.1 Overview

Timesys has developed a board support package (BSP) for the element14 i.MX 6Q SABRE-Lite platform. The BSP comes pre-loaded on the MicroSD card provided with the board.

This BSP demonstrates a number of features on i.MX 6Q - based platforms, including hardware video acceleration, 3D graphics, GUI software, camera support, and Web use.

4.1.2 Software Features

Items		Notes
OS	Linux	Version 3.0.15
Device Driver	Serial	Series driver
	RTC	Hardware clock driver
	Network	10/100/Gb IEEE1588 Ethernet
	Flash	SPI flash driver
	Display	Three display ports (RGB, LVDS, and HDMI 1.4a)
	MMC/SD	Dual SD 3.0/SDXC card slots
	SATA	Serial ATA 2.5 (SATA) at 3Gbps
	USB	3 High speed USB ports (2xHost, 1xOTG)
	Audio	Analog (headphone/mic) and Digital (HDMI)
	Camera	Two camera ports (1xParallel, 1x MIPI CSI-2)
	PCIe	PCIe port (1 lane)
	CAN	1xCAN2 port
	Keypad	GPIO keyboard driver
	LED	User LEDs driver

4.1.3 System Development

The instructions below assist the user with setting up the i.MX 6Q SABRE-Lite platform distributed with the Timesys BSP, including how to navigate and operate the BSP demo programs.

4.1.3.1 Preparing the Board

To benefit from using the demos, at a minimum you must have:

1. element14 SABRE-Lite for i.MX 6Q board
2. Power supply
3. Video display
4. USB mouse

The following additional peripherals can be used to enhance your experience:

5. Ethernet cord
6. Camera
7. RS-232 serial cable
8. USB keyboard

Connect the display, USB mouse, and optionally the ethernet cord, camera and serial cable to your SABRE-Lite board. Then insert the power supply plug into the power port on your board.

4.1.3.2 Booting your Board

Several seconds after supplying power to the SABRE-Lite, you will see the Timesys logo displayed on your video display. Wait for around 30 seconds for the boot process to complete.

At the conclusion of the boot, the Qt demo launcher application will begin, characterized by a number of application thumbnails arranged in a horizontal line, with a mouse positioned at center-screen.

NOTE: A number of displays are supported as defaults for the BSP distributed with your board. If you are using a non-default display, then you may have to manually set the U-Boot environment for your board in order to see the desired graphical output. For information on how to do this, sign up for your free LinuxLink account at http://linuxlink.timesys.com , and see the SABRE-Lite Getting Started Guide at https://linuxlink.timesys.com/docs/gsg/i.MX6QSABRELite .

4.1.3.3 Using the Demo

The demo begins in the Qt application called 'fluidlauncher'. A number of demos can be launched from here.

In order to navigate through the menu, click on with the USB mouse on a side of the window in the direction you wish to cycle the application thumbnails. For instance, if you wish to access an application whose thumbnail is to the left of center, position your mouse on the left side of the screen over black space and click several times until the thumbnail for your application is moved to center.

Once the thumbnail for the desired application is centered, click on it to launch the demo.

Demo applications

1. **Timesys Theatre**

   Timesys theatre showcases a number of the unique capabilites of the i.MX 6Q hardware, most notably:

   - Hardware video acceleration
   - Multi-core processing
   - Video streaming from camera

   The main menu for the theatre provides four options:

   - Accelerated Video: Play a video using Freescale accelerated codecs
   - Non-accelerated Video: Play same video with standard, unaccelerated gstreamer and ffmpeg codecs
   - Camera: see the video capture stream from an attached camera. Includes non-accelerated gstreamer pipeline elements
   - Exit: leave this demo

   When selecting any of the first three menu options, you may stress-test the video pipeline to see the impact of additional computational work on video that is accelerated and non-accelerated. In order to do this:

   - Select "Accelerated Video," "Non-accelerated Video," or "Camera"
   - Click anywhere on the screen to bring up the Qt GUI overlay
   - Add additional computational load with the "Add CPU Load" button
   - View the per-core CPU usage in the top-left corner of the screen

   Note that you will see notable video slowdown when adding CPU load for the non-accelerated video pipeline. Alternatively, you should see nearly no slowdown, if any, for the accelerated pipeline.

   To return to the main menu from any of the video streams, hit the "Stop" button in the lower-right corner of the Qt GUI overlay.

2. **Vivante GPU demos**

   Vivante provides a binary package of OpenGLES libraries to make 3D graphics acceleration available to the developer on an i.MX 6Q - based platform.

   Two Vivante-developed demos, "3D Spinning Orb" and "3D Spinning Block," show the SABRE-Lite's 3D graphics acceleration capabilities in a number of simple tests with texturized 3D objects.

3. **Timesys website**

   If your element14 i.MX 6Q SABRE-Lite is connected to a DHCP and DNS server through an ethernet cable, you can access the Web via the Qt application called 'fancybrowser.'

   This demo will route you to the Timesys website, after which you may navigate about the Web as you would with a standard Web browser.

4. Qt applications

Two Qt demos, "Vector Deformation" and "Path Stroking," have been included to demonstrate the capabilities of Qt software for this platform.

Qt is a toolkit that provides the ability to construct complex and rich GUI environments for your applications. The two demos above show a wide range of GUI elements available to the Qt developer.

4.1.4 For More Information

The Linux kernel and software for this BSP was built using the Timesys Factory.

The Factory provides a toolchain, sources, and build infrastructure that can be used for rapid development and customization of an embedded Linux OS for your target platform. At this time, over 100 reference boards and 1300 packages are integrated into the Factory build system.

To build your own free Linux BSP for your element14 i.MX 6Q SABRE-Lite, visit http://www.timesys.com/embedded-linux/resources/dev-center/element14-sabrelite. From here, you can find further instructions on building a custom Linux distribution using Timesys's LinuxLink, documentation on booting your board, and other materials to help you support Linux for your platform.

5 ESD PRECAUTIONS AND PROPER HANDLING PROCEDURES

This section includes the precautions for mechanical handling and static precautions to be taken to avoid ESD damage:

- Avoid carpets in cool, dry areas. Leave development kits in their anti-static packaging until ready to be installed.
- Dissipate static electricity before handling any system components (development kits) by touching a grounded metal object, such as the system unit unpainted metal chassis.
- If possible, use antistatic devices, such as wrist straps and floor mats.
- Always hold a evaluation board by its edges. Avoid touching the contacts and components on the board.
- Take care when connecting or disconnecting cables. A damaged cable can cause a short in the electrical circuit.
- Prevent damage to the connectors by aligning connector pins before you connect the cable. Misaligned connector pins can cause damage to system components at power-on.
- When disconnecting a cable, always pull on the cable connector or strain-relief loop, not on the cable itself.

6 APPENDIX A: SCHEMATICS

The schematics for the development platform for i.MX 6Q can be found at
http://www.element14.com/community/docs/DOC-51148