

FPGAView™ Software for Debugging Altera FPGA Devices with Tektronix Logic Analyzers and Mixed Signal Scopes

FPGAView™ software works with the Tektronix® TLA series of logic analyzers and MSO4000 series of mixed signal oscilloscopes to enable real-time debugging of Altera FPGAs. Using FPGAView software, you can quickly and easily measure signals inside the Altera® FPGA design and select which group of internal signals to probe without having to recompile the design. FPGAView software simplifies logic analyzer use by automatically updating channel names with the internal signal names selected and providing a mechanism to auto-select channel groupings from the same selection view.

Altera Logic Analyzer Interface Editor

The FPGAView software package is enabled by the Logic Analyzer Interface (LAI), introduced in the Quartus® II 5.1 software release. The LAI allows a large set of internal signals to be mapped to a small number of output pins via a user-configurable multiplexer. The Altera LAI Editor Window provides an easy to use environment for setting up the number of multiplexer input banks, defining the number of channels per bank, setting timing or state acquisition modes, and wiring internal logic signals to the appropriate input banks.

Hardware Probe Control

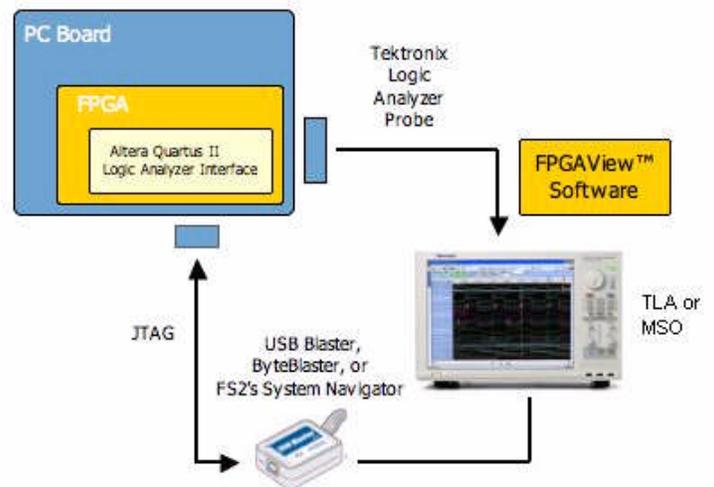
The same JTAG port that is used for programming the FPGA device or the Nios II processor core is used to select the signal bank in the Altera FPGA. Any one of three different probes can control the JTAG port –USB Blaster, ByteBlaster, or the FS2 System Navigator Probe.

System Overview

The diagram below shows the complete interconnection of target, JTAG probe, Tektronix TLA or MSO, and FPGAView software. The TLA or MSO probe or probes plug into the target board for accessing the on-chip signals that are brought out to probe connectors. The TLA, a PC in itself can host the JTAG probe which is connected to the JTAG target connector. The TLA also can run the Quartus software used to program the FPGA device. FPGAView software also runs on the TLA to control bank selection and update its channel names.

MSO4000 Support

FPGAView supports the Tektronix MSO (Mixed-Signal Oscilloscope) product family. The FPGAView software must run on a separate host PC along with the Quartus software.



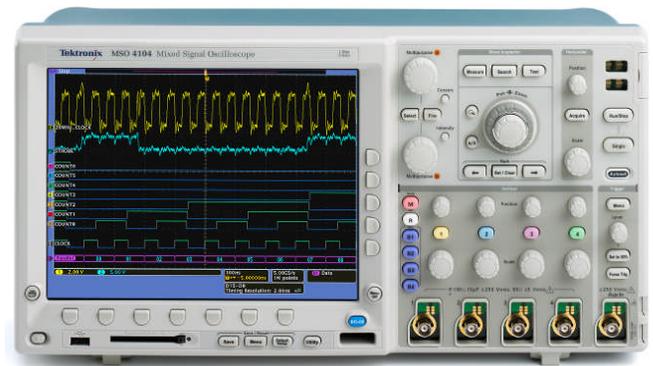
Features Summary

- Convenient control of the Altera FPGA Logic Analyzer Interface (LAI) logic block bank selection
- Identify and map LAI output pins to external logic analyzer or MSO probe connector quickly and easily
- Automatic update of TLA or MSO channel names when selecting a different signal bank
- Complete flexibility in hardware probe use
- FPGA control can use Altera USB Blaster, ByteBlaster or FS2 System Navigator probes
- Supports the Altera Cyclone and Stratix families of FPGAs
- Handles multiple LAI instantiations in one device for multiple clock domain support
- Supports multiple FPGA devices through JTAG chaining
- PC Windows user interface
- User can define and assign a TLA setup file for each bank, making it easy to reconfigure channel groupings



Target Connection

The photo (above right) shows the Tektronix TLA 7000 Logic Analyzer with its two connections to the target – the acquisition probe plugged into the Mictor 38-pin connector of the Altera evaluation board, and a USB Blaster plugged into the USB port of the TLA and into the JTAG header on the evaluation board. The photo to the right is the Tektronix MSO which has 16 logic analyzer input channels.



Getting Started with FPGAView

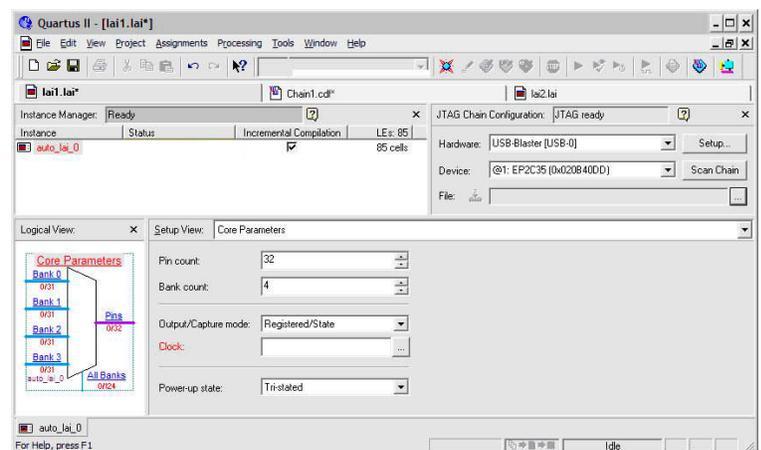
Step 1: Create an LAI core and make the connection

Use the Quartus II LAI Editor to select **Core Parameters**, fill in the **Pin** and **Bank** counts, select **Output/Capture** mode (state or timing), **Clock**, and **Power-up** state to create an LAI debug core that best fits your debug needs.

Next, select the **Pins** that will be analyzed, by double clicking on each **Pin Name** which brings up the **Pin Planner** where the associated pin to the logic analyzer connector header is selected.

Next, click on each **Bank**, then double click on each **Node Alias** which brings up the **Node Finder** where you select the signal name to wire up to each **Bank** input.

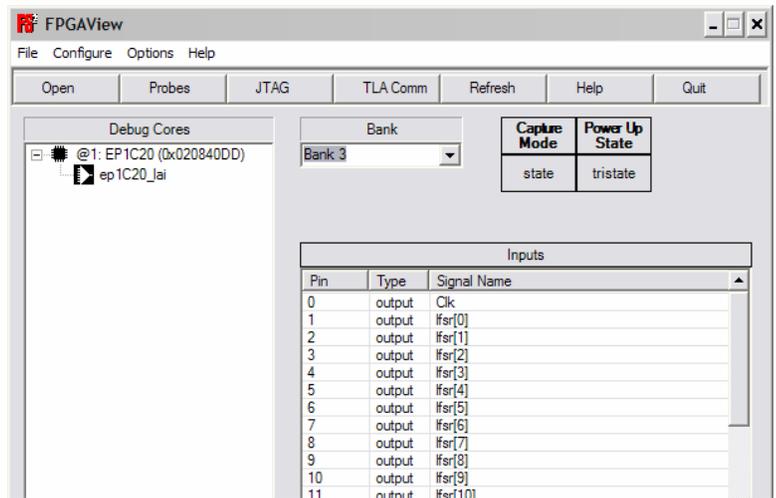
When the setup is completed, go to **File > Save as** to enter the desired name of the LAI block and save all the configuration information in a .lai file.



Step 2: Run the FPGAView Software

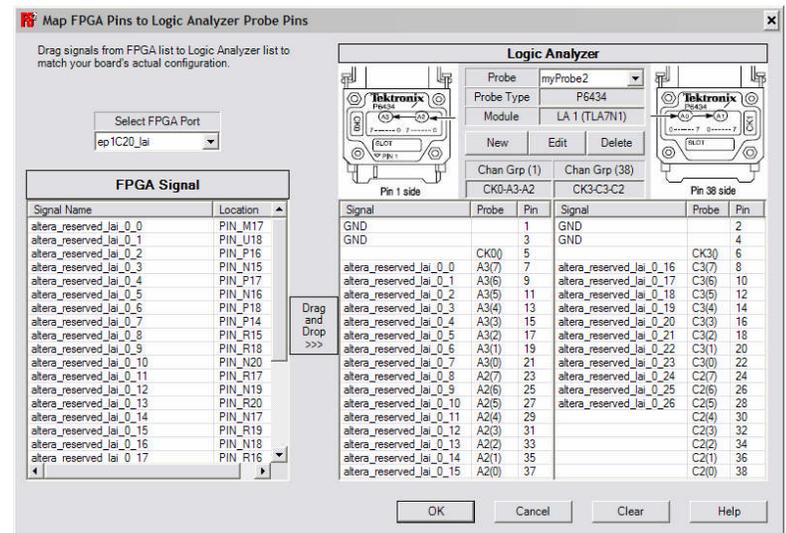
From the FPGAView window you establish the network connection to the TLA with the **TLA Comm** toolbar button or to the MSO with the **MSO** toolbar button.

The **Open** toolbar button brings up a file browser where you select the Altera Logic Analyzer Interface (.lai) file previously generated by the Quartus LAI Editor software. This loads all the information about the LAI core including the number of signals per bank, number of banks, signal names, and timing or state mode of acquisition. It also includes information on each LAI core in the device if there is more than one.



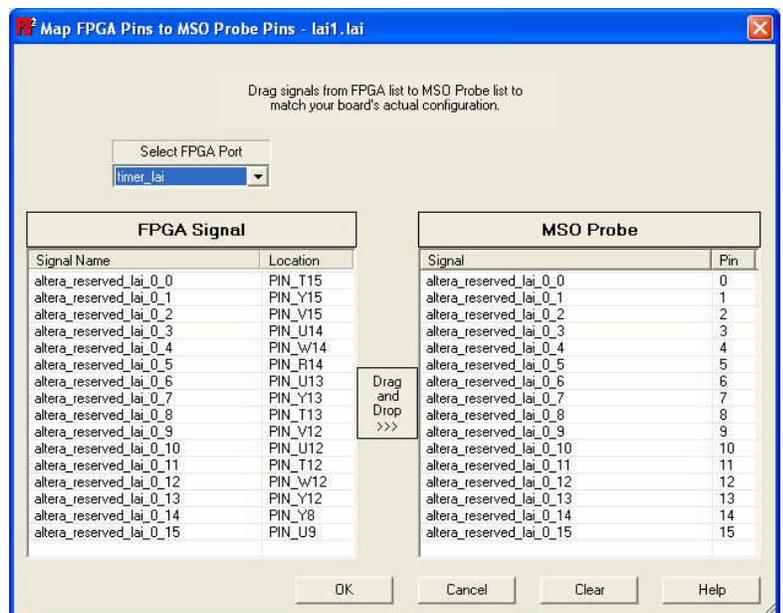
Step 3 (for TLA): Assign FPGA pins to TLA channels

Click on the **Probes** button to bring up the dialog for connecting LAI core output signal names and pin assignments to TLA probe channels. Drag and drop signal names to the desired channels to make the assignments. More than one signal can be selected at a time. Note that the left column assigns odd numbered probe pins and the right side, even numbered. The assignment process is only necessary once for a given target connection.



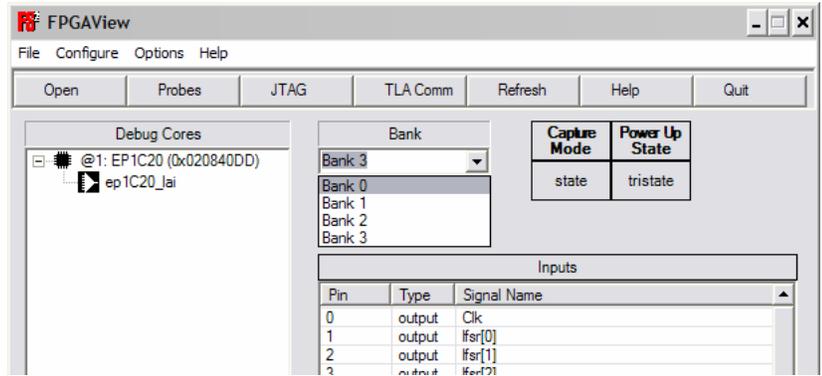
Step 3 (for MSO): Assign FPGA pins to digital channels

Click on the **Probes** button to bring up the dialog on the right. For the MSO there is only one probe type (16 channels) so there are no probe choices. Select an FPGA Port file, then select all the FPGA Signals of interest, and drag and drop them onto the MSO Probe list on the right.



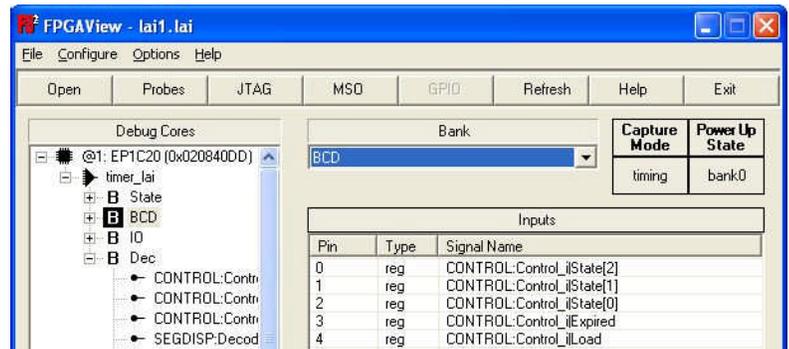
Step 4 (for TLA): Select the desired signal bank and program the TLA channel names

The **Bank** list pull-down contains all the banks defined previously in the Quartus LAI edit window. Selecting a **Bank** updates the **Inputs** list below it, and then programs the Tektronix Logic Analyzer with the names into their assigned channels.



Step 4 (for MSO): Select the desired signal bank and program the TLA channel names

The screen capture on the right is the MSO home page that shows the MSO button across the top. Note that the logic analyzer input signals to the MSO only operate in timing acquisition mode.



PC Workstation Configurations for the TLA

There are two basic configurations for the FPGAView software and its control over the Altera FPGA target board and the Tektronix Logic Analyzer.

Tektronix logic analyzer only—in this configuration the TLA controls the FPGA JTAG probe and runs the FPGAView software and standard logic analyzer control software. Quartus II can also be installed and run on the TLA although it is more likely to be run on a separate PC. In that case the LAI core setup file (.lai) can be copied into the TLA – physically or over its Ethernet connection, or access the .lai file remotely over the network.

PC in office, TLA and target in the lab—in this configuration, the majority of the operating software runs on a PC workstation and the TLA is controlled remotely. Quartus II and FPGAView software run on the PC as well as the Tektronix logic analyzer software, remotely. The TLA does not require a screen in this configuration. The user develops the FPGA logic design using Quartus II tools then creates the LAI core and attaches it to the signals to be traced. The Tek logic analyzer control software is started and linked to the TLA over the network. FPGAView software is then started; it controls the TLA over the same network connection. A minimal copy of Quartus II is installed on the TLA in order to run the JTAG probe remotely.

The user sets up the TLA with the trace probe(s) plugged into the target connector(s) – most commonly to one or more Mictor38 headers - and the USB Blaster (or other

compatible JTAG probe) to the TLA and its JTAG end plugged into the target JTAG header.

When FPGAView software runs, the user loads the .lai file first, makes the connections between the FPGA pins and the TLA channels (only once), then proceeds to select the bank of signals to trace and trigger on. FPGAView software copies the signal names into the TLA assigned channels. The user operates the TLA software on the PC workstation, with the actual target and TLA hardware set up in the lab.

PC Workstation Configurations for the MSO

There is only one PC configuration for the Tektronix MSO. The host PC runs the Quartus II software to define and configure the Altera LAI core, and it also runs FPGAView software to control the LAI core mux and program signal names for the digital input channels of the MSO.

Altera LAI Configuration Choices

The selectable attributes of the LAI are:

- Pin count: number of output channels 1-256
- Bank count: number of input banks 1-256
- Output/capture modes: 1) Registered/State or 2) Combinational/Timing. If mode 1, the user must select a clock source.

Hardware Requirements

- Tektronix Logic Analyzer Series supported are: TLA600, TLA5000, TLA700, TLA7000
- Tektronix MSO4000 Series
- Windows based PC if using MSO4000 or networked TLA
- Target board with at least one Altera FPGA, JTAG connection, and at least one TLA or MSO probe connection

Software Requirements

- Quartus II 5.1 or later which includes the Logic Analyzer Interface Editor
- Tektronix TLA software version 4.3, 5.0, 5.1 or later
- Tektronix MSO4000 series oscilloscope
- Windows XP/2000 on TLA or host PC

Product Codes

FPGAVIEW-A-TLA	FPGAVIEW, Altera FPGA, TLA or PC NIC host license
FPGAVIEW-A-TLA-F	FPGAVIEW, Xilinx FPGA, TLA, floating network server license
FPGAVIEW-A-MSO	FPGAVIEW, Altera FPGA, MSO serial number license
FPGAVIEW-A-MSO-PC	FPGAVIEW, Altera FPGA, MSO, PC NIC license



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