TSW4200 Demonstration Kit

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1 Introduction

1.1 Overview

This is the user's guide for the TSW4200 Demonstration Kit. The kit includes two EVMs: TSW4200-DAC and TSW4200-ADC, and they provide evaluation to TI's DAC3283 and ADS62P49, respectively. Through the included FMC adapter boards, the EVMs are ideally suited for mating with a FPGA development board to evaluate the DAC and the ADC as a basic transmitter and receiver system. For more information regarding the individual device or EVM, refer to Table 1 for the respective device's datasheet and EVM user's guide.

Table 1. TSW4200 Demonstration Kit Reference Materials

	Device	Data Sheet	EVM	User's Guide
TSW4200-DAC	DAC3283	SLAS693	DAC328xEVM	SLAU311
TSW4200-ADC	ADS62P49	SLAS635	ADS62PxxEVM	SLAU237

The included FMC adapters are the FMC-DAC-Adapter and the FMC-ADC-Adapter. They are a type of passive interconnect board that enables the output of TI's LVDS high speed DACs or ADCs to be directly connected to a standard FMC interconnect header. The FMC interconnect header is a typical input on the latest Xilinx FPGA EVMs. The TSW4200-DAC EVM uses the FMC-DAC-Adapter, and the TSW4200-ADC uses the FMC-ADC-Adapter.

1.2 TSW2400 Demonstration Kit Block Diagram

Figure 1 shows the configurations of the TSW4200-DAC and TSW4200-ADC EVM with the FPGA development board. Section 3 covers the setup information of the EVMs.

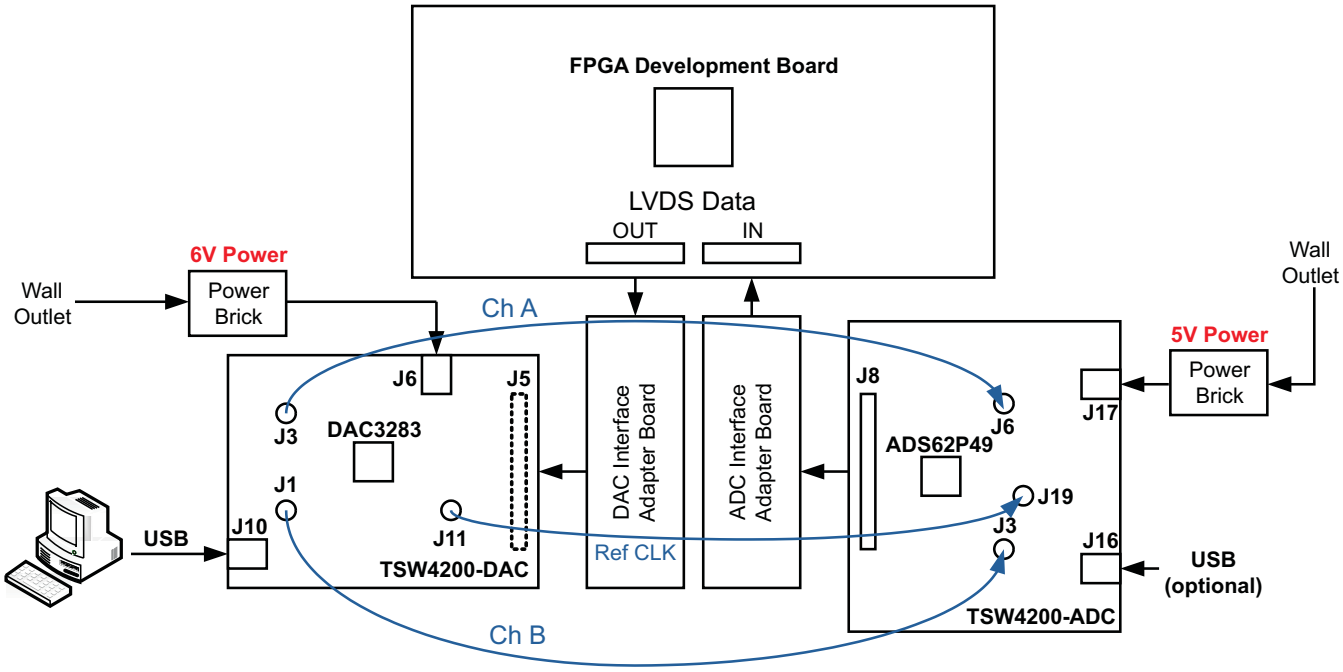

Figure 1. TSW4200 Demonstration Kit

1.3 TSW4200-DAC Configuration

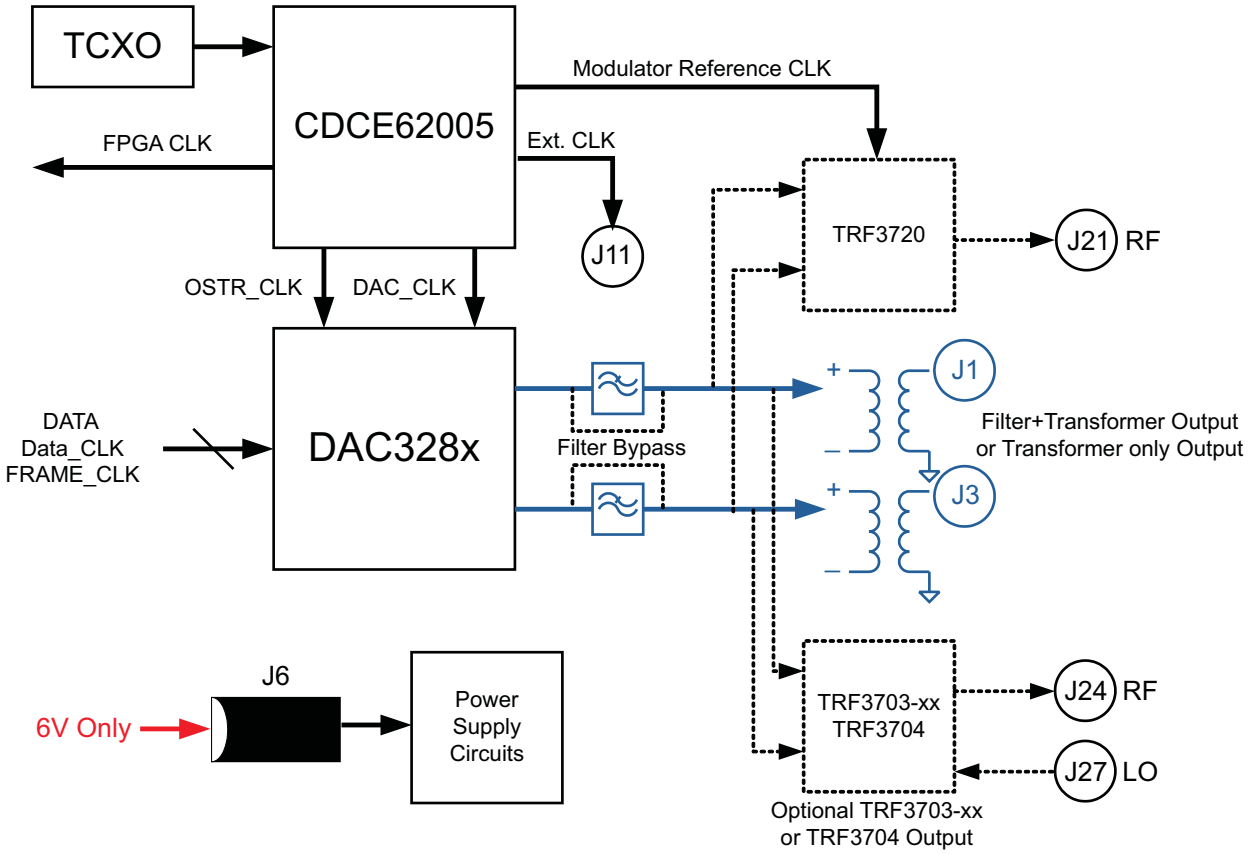

Figure 2. DAC3283 EVM Block Diagram

1. The TSW4200-DAC kit is a DAC3283EVM configured as follow:
   (a) Power Supply Option: The kit includes a **6V power supply** input to power supply jack J6. Be sure to use 6V power supply only for proper operation of the EVM and to prevent damage.
   (b) Analog Output Option: The on-board DAC3283 has dual channel outputs that go through filter network and transformer to J3 (Ch. A) and J1 (Ch. B).
   (c) Clock Option: The on-board CDCDE62005 provides clocks to all the on-board devices.
      (i) The default DAC clock is configured at 614.4MHz. The DAC interpolation, FPGA clock (TSW3100 CLK), and the FIFO OSTR clock can be configured based on the data rate, FPGA configuration, and system requirement. For more information, please refer to the DAC3283 datasheet.
      (ii) The TSW4200-DAC has a clock output at J11 that provides the reference clock for the CDCE72010 on the TSW4200-ADC at J19. The default reference clock should be configured as 19.2MHz.
2. The EVM has the default jumper setting listed on Table 2.
3. For more details, refer to DAC3283EVM User's Guide (SLAU311).

Table 2. TSW4200-DAC Default Jumper Setting

Jumper	Default Position	Purpose
JP22	2-3	CDCE62005 (U4) External Reference Clock Bias
JP19	Shorted	Enable TCXO (U7)
JP9	1-2	DAC3283 (U1) TXENABLE
JP20	1-2	CDCE62005 (U4) Power Down
JP21	1-2	CDCE62005 (U4) Reference Select
JP13	2-3	TRF3720 (U3) Power Save
JP17	1-2 (TRF3720)	TRF3720 (U3) or TRF3703 (U10) Power Path

1.4 TSW4200-ADC Configuration

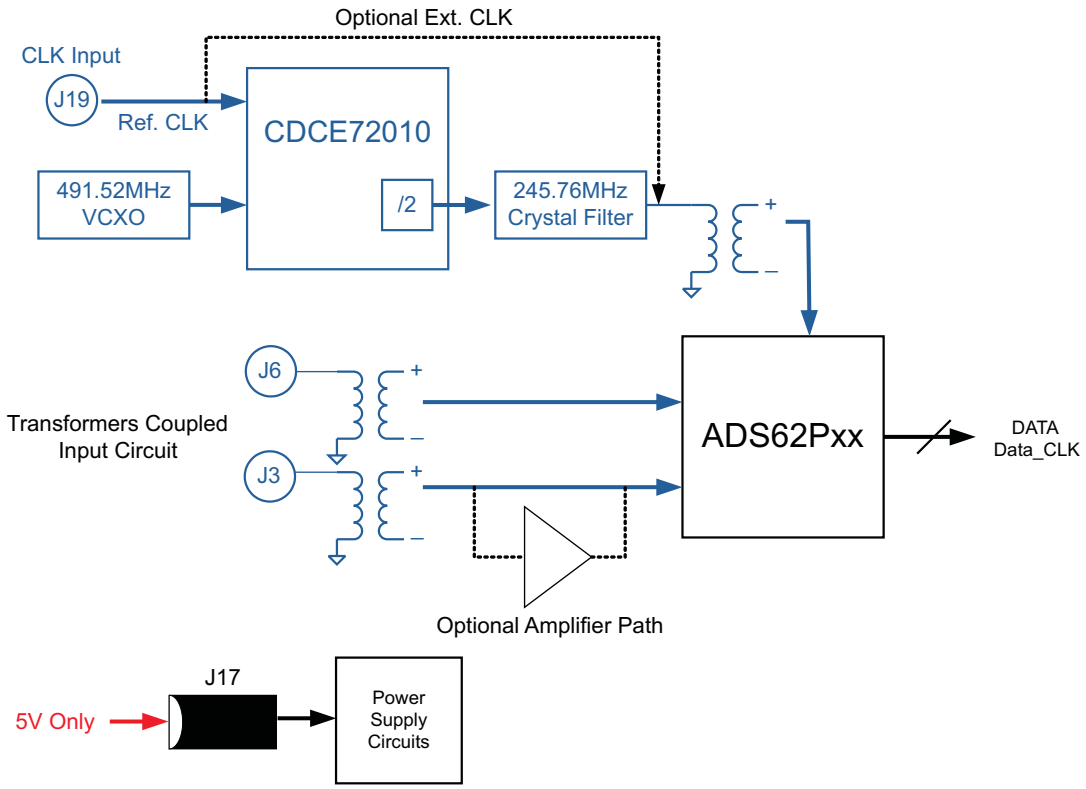

Figure 3. ADS62P49 EVM Block Diagram

1. TSW4200-ADC Configuration:
   (a) Power Supply Option: The kit includes a **5V power supply** input to power supply jack J17. Please be sure to use 5V power supply only for proper operation of the EVM and to prevent damage.
   (b) Analog Input Option: The on-board ADS62P49 has dual channel transformer-coupled inputs from J3 (Ch. A) and J6 (Ch. B).
   (c) Clock Option: The on-board CDCE72010 provides crystal filtered LVCMOS clock at 245.76MHz to the on-board ADS62P49. The reference clock input of 19.2MHz to the TSW4200-ADC is at J19. The CDCE72010 is configured in PLL mode by default using the on-board 491.52MHz VCXO. The CDCE72010's output has divider configured to be divide-by-2 to divide the 491.52MHz VCXO clock to the required 245.76MHz clock.
2. The EVM has the default jumper setting listed on Table 3.
3. For more details, refer to ADS62PXXEVM User's Guide (SLAU237).

Table 3. TSW4200-ADC Default Jumper Setting

Jumper	Default Position	Purpose
JP11	1-2 (Parallel)	ADS62P49 (U2) Parallel or Serial Mode Option
JP8	1-2 (Parallel)	SCLK Parallel or Serial Mode Option
JP12	1-2 (0dB Gain, Int. Ref.)	SCLK Parallel Mode Select
JP9	1-2 (Parallel)	SDATA Parallel or Serial Mode Option
JP13	Open	SDATA Parallel Mode Option
JP10	1-2 (Parallel)	SEN Parallel or Serial Mode Select
JP14	1-2 (2's com & DDR LVDS)	SEN Parallel Mode Option
JP20	1-2	CDCE72010 (U10) AUX Select
JP21	1-2	CDCE72010 (U10) MODE Select
J14	Open	CDCE72010 (U10) Power Down
J15	Open	CDCE72010 (U10) Reset
JP3	2-3 (Off)	THS4509 (U1) Power Down
JP23	1-2	USB Microcontroller (U6) Power Select
J18	Open	VCXO (VCXO1) Enable
JP16	1-2	Power Option (see schematic or ADS62PXX EVM User's Guide)
JP17	Open	Power Option (see schematic or ADS62PXX EVM User's Guide)
JP19	1-2	Power Option (see schematic or ADS62PXX EVM User's Guide)
JP15	1-2	Power Option (see schematic or ADS62PXX EVM User's Guide)
JP18	1-2	Power Option (see schematic or ADS62PXX EVM User's Guide)
JP22	1-2	FPGA SDOUT path
JP5	1-2 (Low)	ADS62P49 (U2) CTRL3
JP6	1-2 (Low)	ADS62P49 (U2) CTRL2
JP7	1-2 (Low)	ADS62P49 (U2) CTRL1

2 Software

See the DAC3283 and the ADS62P49 EVM User’s Guide for more detailed explanations of the EVM setup and operation. This document assumes that EVM software applications are installed and functioning properly.

Be sure to use the latest EVM software available at www.ti.com. For the TSW4200 Demonstration Kit evaluation, only the DAC3283 EVM software is needed. The ADS62P49 EVM software is optional since the on-board jumpers will provide sufficient control of the ADC.

3 Quick Setup

1. For the DAC EVM, connect 6V supply to J6. Connect the EVM to a PC through a USB cable to utilize the EVM software.

   (a) Start the DAC3283 EVM software. Select the Top Level Tab and press the *Reset USB Port* button.
   (b) Configure the Top Level Tab to be the same as Figure 4. Set *Test Port Div* to be *32* to set the reference frequency of 19.2MHz. All other settings should be default. The DAC interpolation, FPGA clock (TSW3100 CLK), and the FIFO OSTR clock can be configured based on the data rate, FPGA configuration, and system requirement. For more information, please refer to the DAC3283 datasheet.

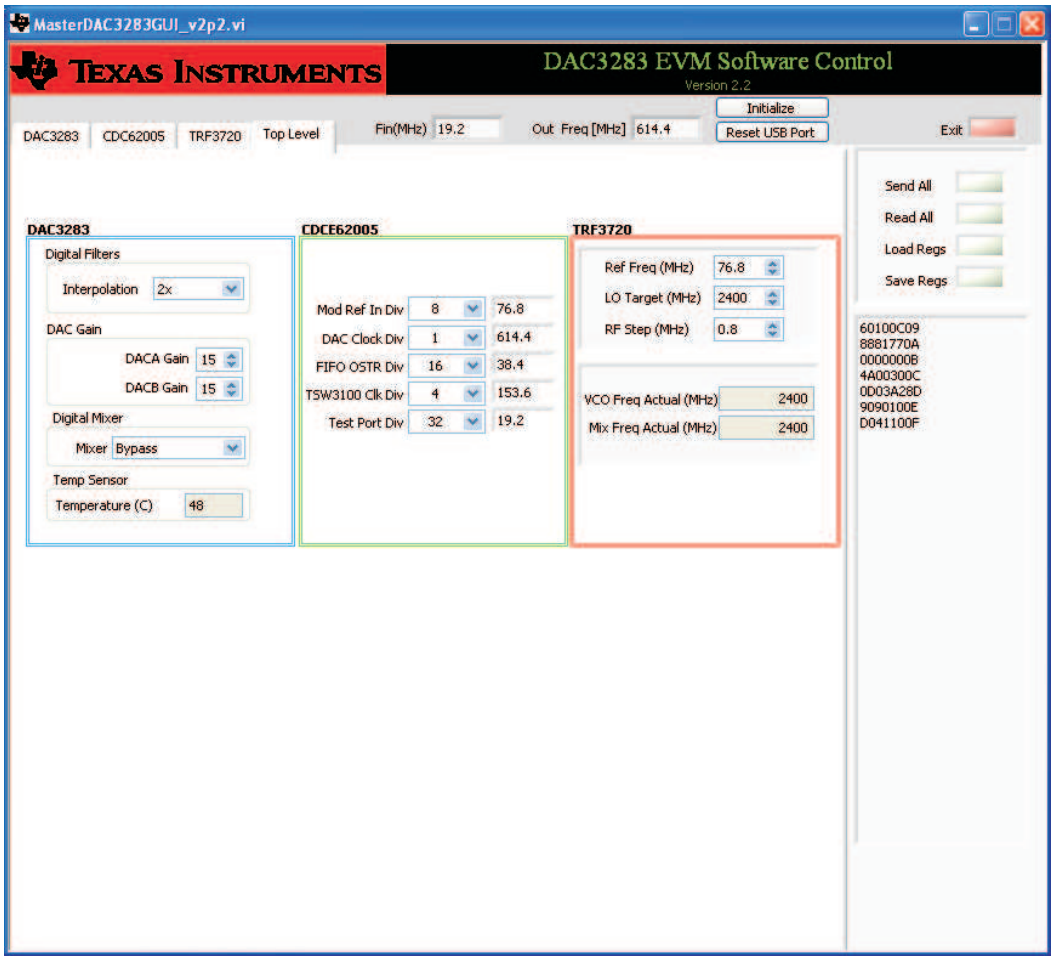

Figure 4. DAC3283 EVM Software Configuration

   (c) Press "send all" to send all the instructions to the DAC3283 EVM.
   (d) Toggle the *Initialize* button. This initializes the CDCE62005 clock.
   (e) Verify that the CDCE62005 LED (D4) is illuminated, indicating lock.
2. For the ADC EVM, connect 5V supply to J17. USB connection to ADC EVM is optional. The default ADS62P49 operates with internal reference and has 2s complement, LVDS output.
3. Connect the ADC and DAC EVMs to the FPGA solution through the provided adapter boards. See Adapter Reference section for detail.
4. Connect the external reference clock output of the DAC EVM at J11 to the reference clock input of the ADC EVM at J19. The reference clock should be at 19.2MHz.
5. Connect the DAC EVM output at J1 and J3 to the ADC EVM input at J3 and J6. See Figure 1 for detail.
6. Start evaluating the TSW4200 Demonstration Kit by configuring the FPGA to transmit data to the DAC EVM and receive data from the ADC EVM.

4 Adapter Reference

Visit www.ti.com for more information on the following adapter board options.

- FMC-ADC-Adapter, http://focus.ti.com/docs/toolsw/folders/print/fmc-adc-adapter.html
- FMC-DAC-Adapter, http://focus.ti.com/docs/toolsw/folders/print/fmc-dac-adapter.html
- HSMC-ADC-Bridge, http://focus.ti.com/docs/toolsw/folders/print/hsmc-adc-bridge.html

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