



A New Direction in Mixed-Signal

September 2012

XRP7724EVB-DEMO-1

Quad Channel Digital PWM/PFM Demo Board

Programmable Power Management System

Rev. 1.0.0

GENERAL DESCRIPTION

The XRP7724EVB-DEMO-1 board is a complete, four channel, power system. It provides 3.3V, 2.5V 1.5V and 1V at a maximum of 3A, 3A, 5A and 10A loads respectively. The 1.5V and 1V supplies can be adjusted in 2.5mV increments, the 2.5V supply in 5mV increments, and the 3.3V supply is adjustable in 10mV increments. The order and ramp rates for each supply can be programmed to accommodate any sequencing requirement. All power supply operations can be controlled over an I²C interface. Faults, output voltages and currents can also be monitored. Two GPIO and three PSIO signals are available and can be programmed to provide a variety of functions. Unused GPIO/PSIO pins can be programmed as I/O expansion for a microcontroller. The board is supported by PowerArchitect™ 5.0 and plugs directly onto the Exar Communications Module (XRP77xxEVB-XCM).

EVALUATION BOARD MANUAL



XRP7724EVB-DEMO-1

FEATURES

- **XRP7724 Programmable Controller**
- **4 Channel Power System**
- **Wide Input Voltage Range: 5.5V-25V**
- **I²C Interface**
 - Programming
 - Monitoring
 - Control

EVALUATION BOARD SCHEMATICS

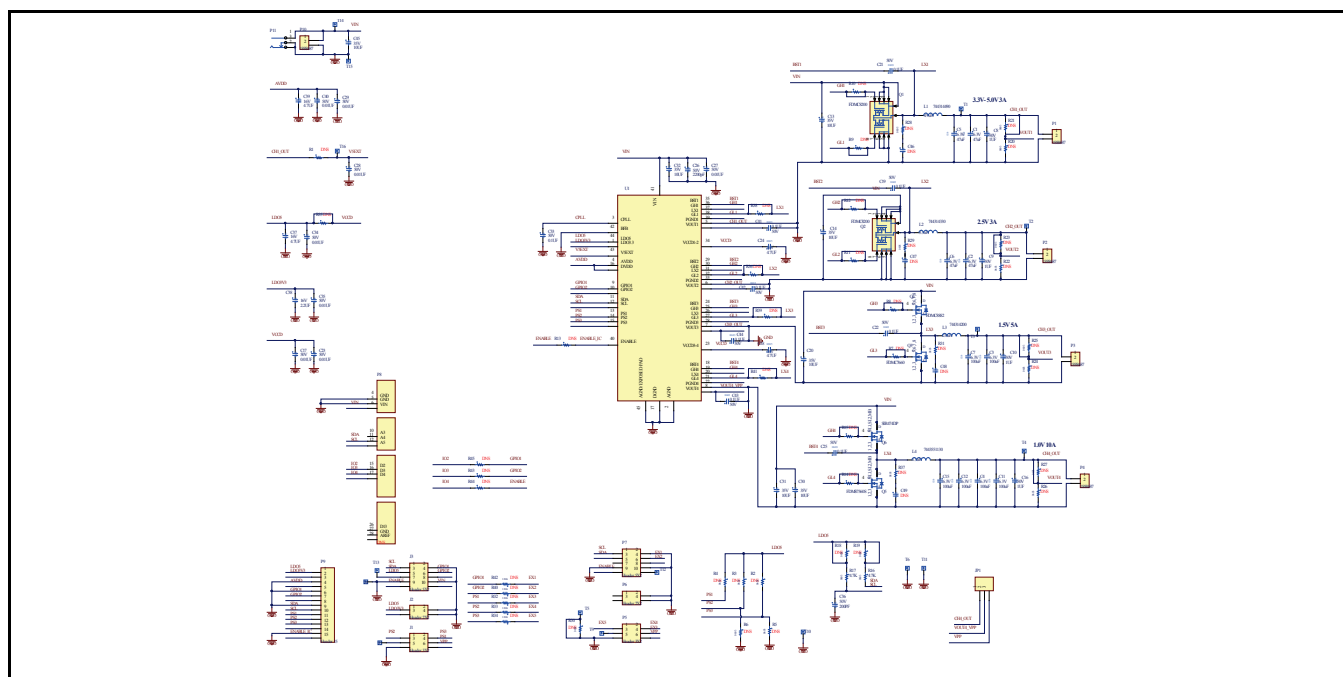


Fig. 1: XRP7724 Evaluation Board Schematics

PIN ASSIGNMENT

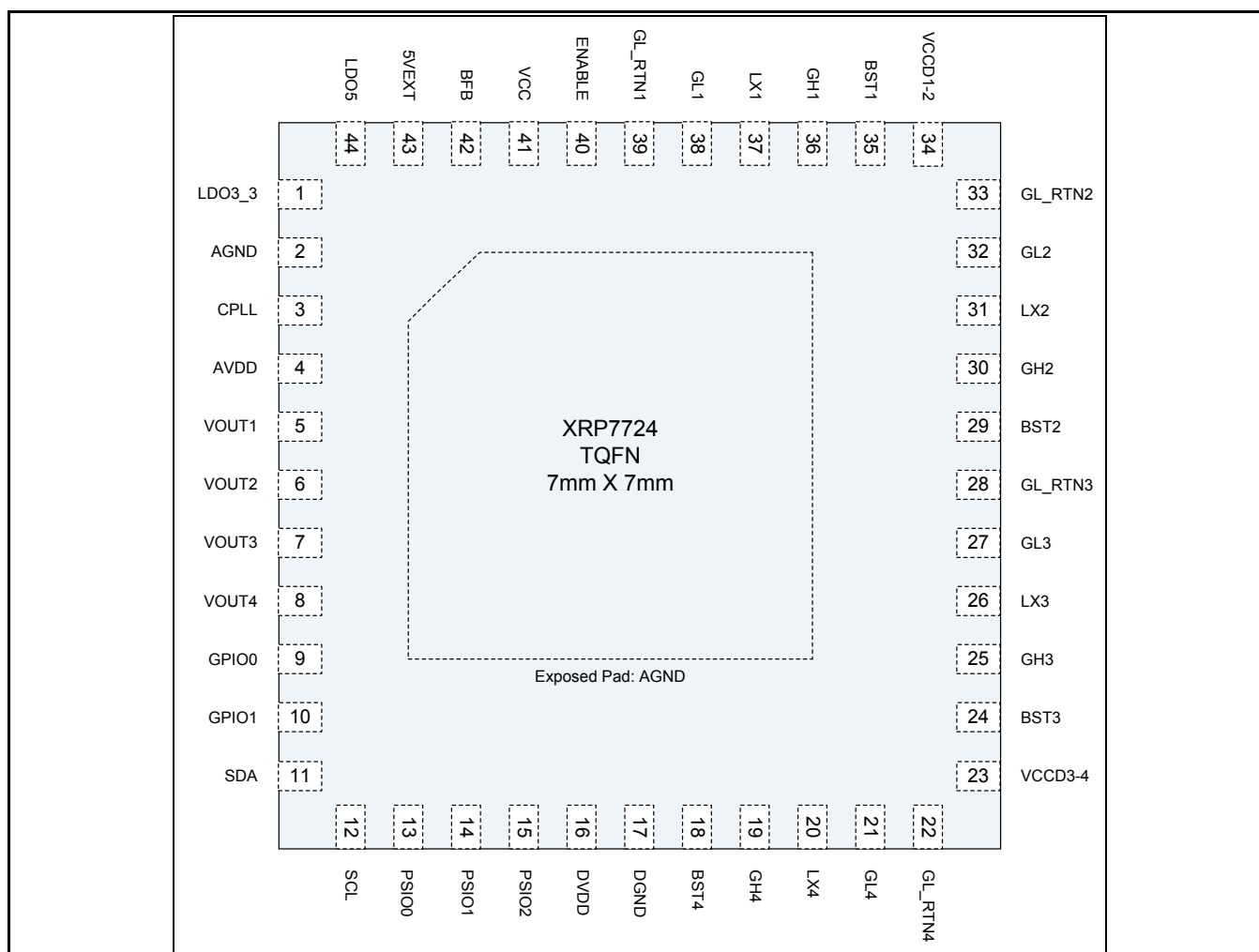


Fig. 2: XRP7724 Pin Assignment

PIN DESCRIPTION

Name	Pin Number	Description
VCC	41	Input voltage. Place a decoupling capacitor close to the controller IC. This input is used in UVLO fault generation.
DVDD	16	1.8V supply for digital circuitry. Connect pin to AVDD. Place a decoupling capacitor close to the controller IC.
VCCD1-2 VCCD3-4	23,34	Gate Drive supply. Two independent gate drive supply pins where pin 34 supplies drivers 1 and 2 and pin 23 supplies drivers 3 & 5. One of the two pins must be connected to the LDO5 pin to enable two power rails initially. It is recommended that the other VCCD pin be connected to the output of a 5V switching rail (for improved efficiency or for driving larger external FETs), if available, otherwise this pin may also be connected to the LDO5 pin. A bypass capacitor (>1uF) to PAD is recommended for each VCCD pin with the pin(s) connected to LDO5 with shortest possible length of etch.
AGND	2	Analog ground pin. This is the small signal ground connection.
GL_RTNA1-4	39,33, 28,22	Ground connection for the low side gate driver. This should be routed as a signal trace with GL. Connect to the source of the low side MOSFET.
GL1-GL4	38,32, 27,21	Output pin of the low side gate driver. Connect directly to the gate of an external N-channel MOSFET.

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Name	Pin Number	Description
GH1-GH4	36,30, 25,19	Output pin of the high side gate driver. Connect directly to the gate of an external N-channel MOSFET.
LX1-LX4	37,31, 26,20	Lower supply rail for the GH high-side gate driver. Connect this pin to the switching node at the junction between the two external power MOSFETs and the inductor. These pins are also used to measure voltage drop across bottom MOSFETs in order to provide output current information to the control engine.
BST1-BST4	35,29, 24,18	High side driver supply pin(s). Connect BST to the external capacitor as shown in the Typical Application Circuit on page 5. The high side driver is connected between the BST pin and LX pin and delivers the BST pin voltage to the high side FET gate each cycle.
GPIO-GPIO1	9,10	These pins can be configured as inputs or outputs to implement custom flags, power good signals, enable/disable controls and synchronization to an external clock.
PSIO0-PSIO2	13,14,15	Open drain, these pins can be used to control external power MOSFETs to switch loads on and off, shedding the load for fine grained power management. They can also be configured as standard logic outputs or inputs just as any of the GPIOs can be configured, but as open drains require an external pull-up when configured as outputs.
SDA, SCL	11,12	SMBus/I ² C serial interface communication pins. These pins can be configured open drain or pseudo-TTL requiring a pull-up resistor.
VOUT1-VOUT4	5,6,7,8	Connect to the output of the corresponding power stage. The output is sampled at least once every switching cycle
LDO5	44	Output of a 5V LDO. This is a micro power LDO that can remain active while the rest of the IC is in shutdown. This LDO is also used to power the internal Analog Blocks.
LDO3_3	1	Output of the 3.3V standby LDO. This is a micro power LDO that can remain active while the rest of the IC is in shutdown.
ENABLE	40	If ENABLE is pulled high or allowed to float high, the chip is powered up (logic is reset, registers configuration loaded, etc.). The pin must be held low for the XRP7724 to be placed into shutdown. Active channels will automatically be ramped down, if desired, prior to the disabling of the chip.
BFB	42	Input from the 15V output created by the external boost supply. When this pin goes below a pre-defined threshold, a pulse is created on the low side drive to charge this output back to the original level. If not used, this pin should be connected to GND.
DGND	17	Digital ground pin. This is the logic ground connection, and should be connected to the ground plane close to the PAD.
CPLL	3	PLL compensation capacitor

ORDERING INFORMATION

Refer to XRP7724's datasheet and/or www.exar.com for exact and up to date ordering information.

USING THE EVALUATION BOARD

INPUT VOLTAGE RANGE

The input voltage range of XRP7724EVB-DEMO-1 board is from 5.5V to 25V. The Input voltage components are rated at 35V. The power components have been optimized for a 12V input rail. When running the board at an input voltage other than 12V, use PowerArchitect™ 5 to evaluate the system performance.

I²C INTERFACE

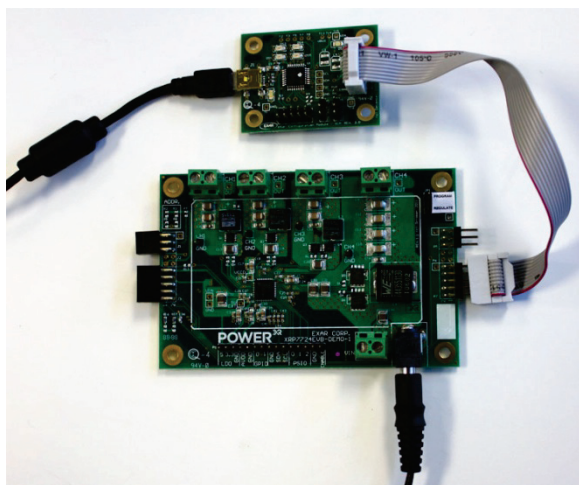
The XRP7724 controller employs a standard I2C interface. Pull-ups for the I2C signals are included on the demo board.

OPERATING THE EVALUATION BOARD

The XRP7724EVB-DEMO-1, is designed to be powered from either an AC/DC wall wart (the output voltage must be in the range of XRP7724 Vcc specification – 5.5V to 25V) connected to the barrel connector, or a test bench DC power supply (the voltage must be in the range of XRP7724 Vcc specification – 5.5V to 25V) connected to the Vin phoenix connector (the positive side is indicated by a purple dot. The proper connection is indicated in Figure 3).

BRING UP PROCEDURE

Plug the XRP7724EVB-DEMO-1 evaluation board to the XCM as shown below.



Load the PowerArchitect™ 5 software.

Select the "Get Started with the EVB-DEMO-1" option when prompted as shown below.



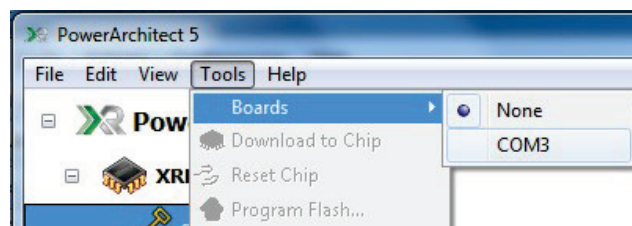
PowerArchitect™ 5 will load the default XRP7724EVB-DEMO-1 configuration automatically.

Apply Power to the board: Please refer to the sections above on how to properly supply power to the board and what voltage range to use.

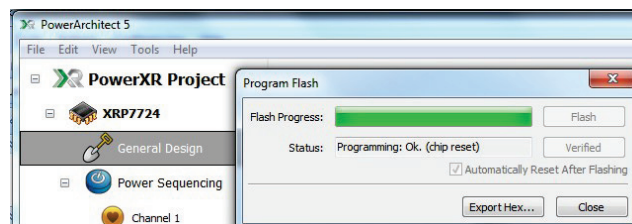
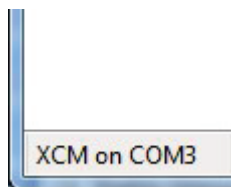
Turn on the Power supply.

Insert the USB cable into the computer and the XCM board.

Go to the Tools tab in PowerArchitect™ 5 and select Boards. The software will identify communication ports where it found the XCM board. Select the port.

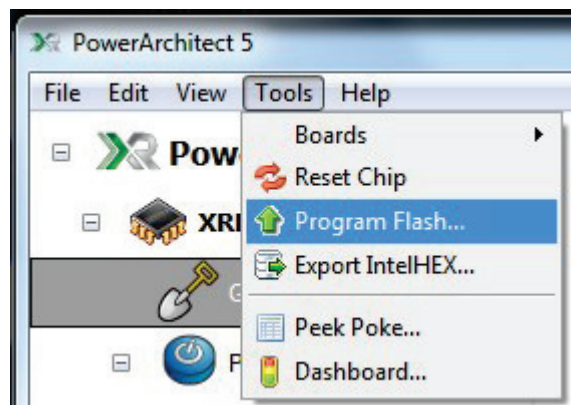


PowerArchitect™ 5 is now communicating with XCM which is indicated in the lower left corner.

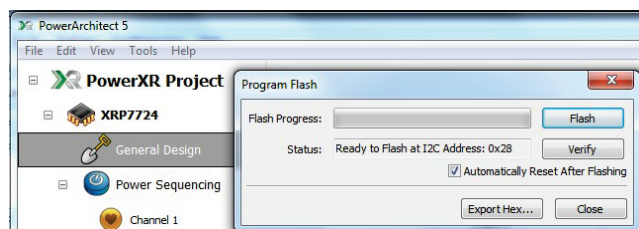


Programming the Configuration onto XRP7724

The next step is to program the default XRP7724EVB-DEMO-1 configuration onto the controller. Go to the Tools tab in PowerArchitect™ 5 and select Program Flash.



The program Flash window will appear.



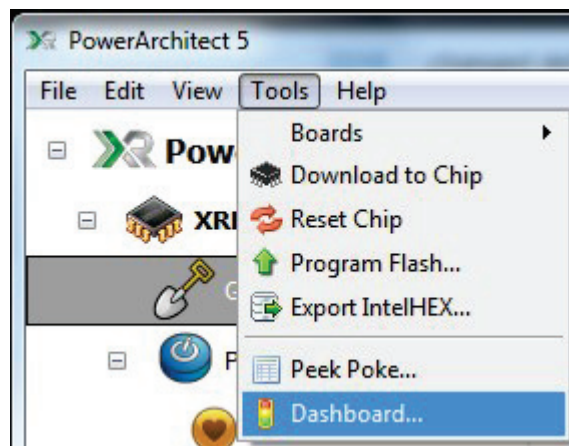
Click the Flash button.

The XRP7724 controller is now configured and ready to go.

Close the window.

Regulation

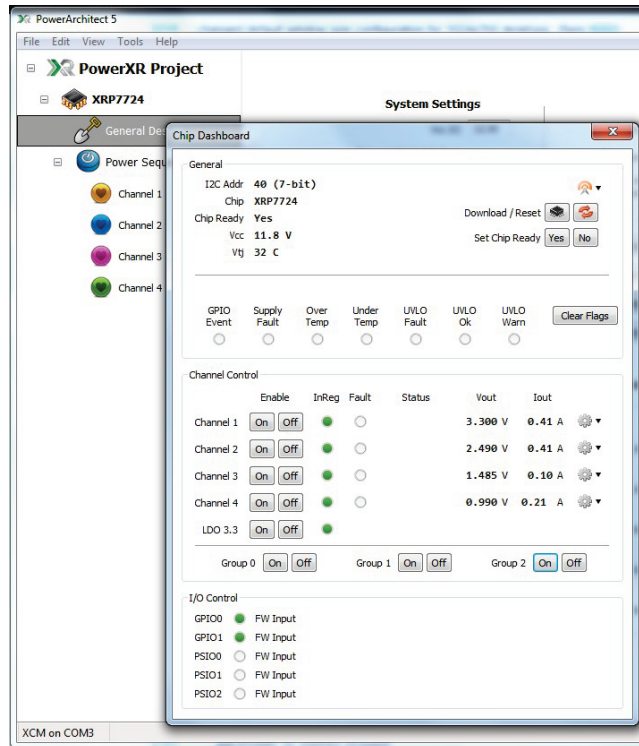
Now when we have the controller configured the way we intended, we are ready to start regulation. Go to the Tools tab in PowerArchitect™ 5 and select Dashboard.



In Dashboard turn Group 1 and Group 2 on. The configuration groups channel 1, channel 2, and LDO3.3 into Group 1, and channels 3 and 4 into Group 2. The channels are now in regulation as indicated by Vout readings as well as the in-regulation indicators.

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Channels can be turned on individually if desired.

Note: Make sure there is a jumper shorting JP1 pins 1 and 2 installed on your board. Channel 4 will regulate without it.

EVALUATION BOARD CONNECTIONS

The following picture illustrates how Vin supplied from a test bench DC power supply and instruments attached to the outputs would be connected to the XRP7724EVB-DEMO-1 board.

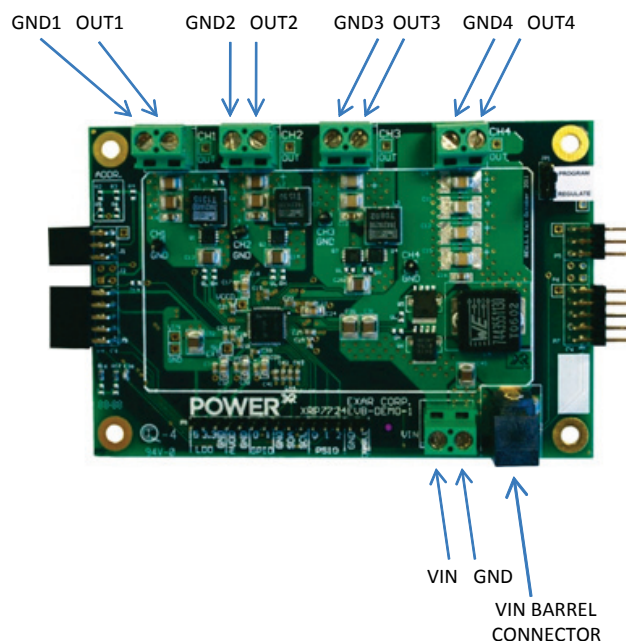
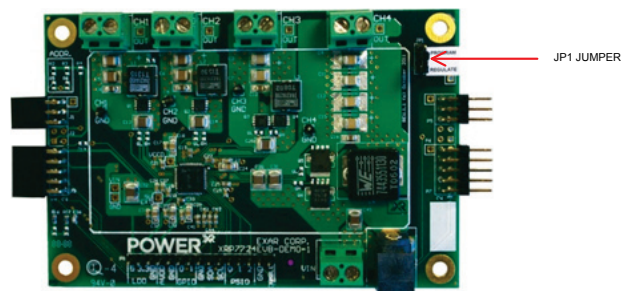
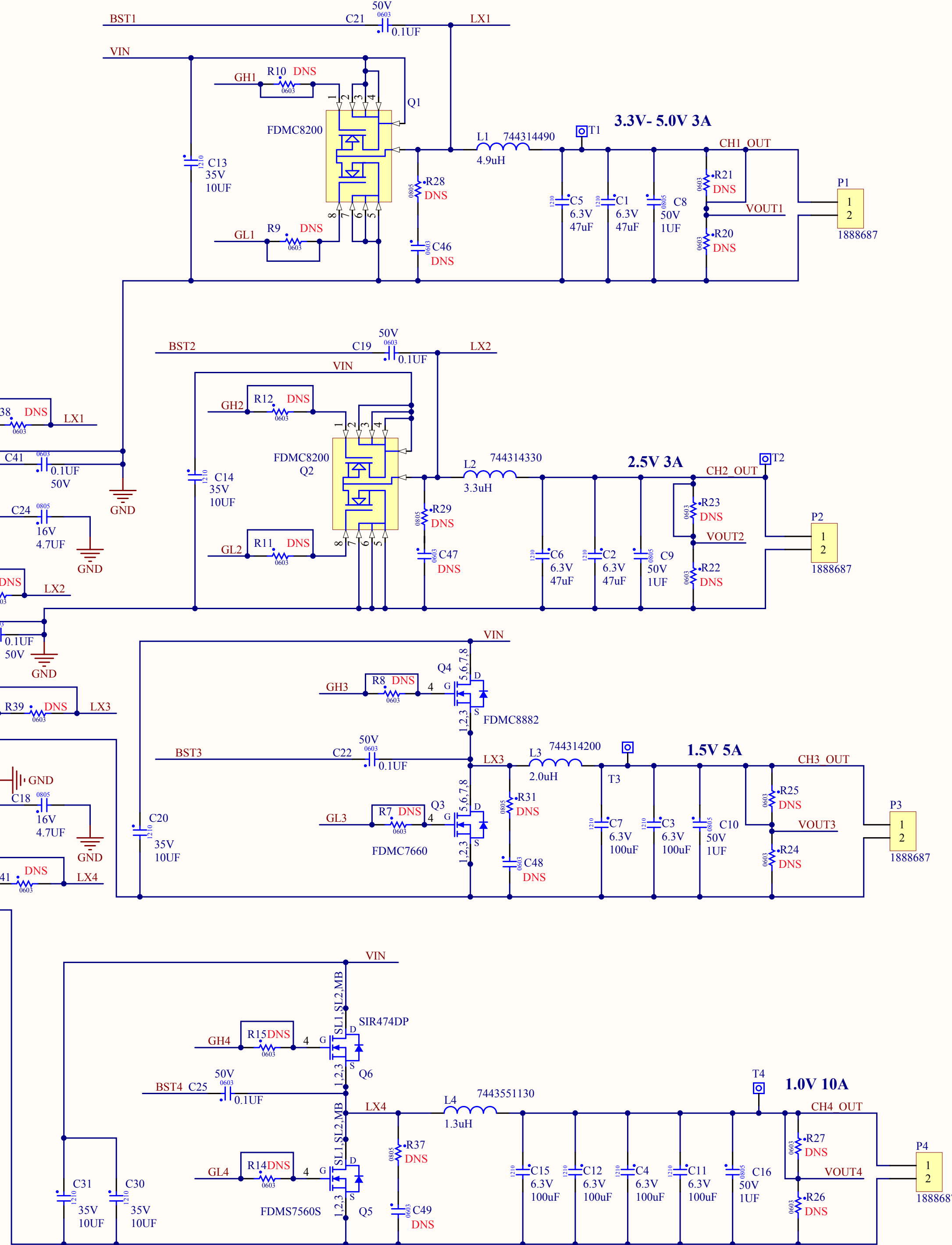
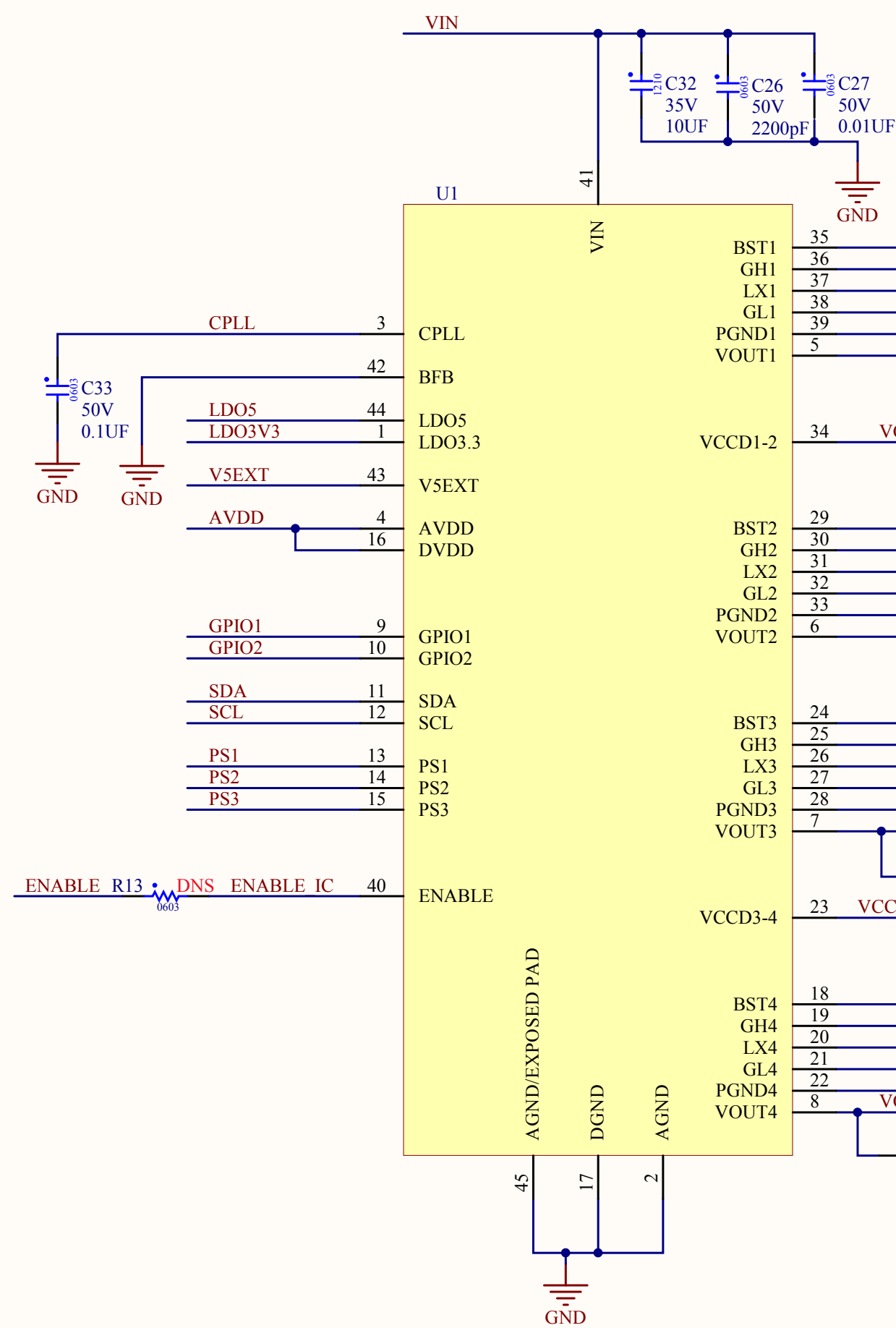
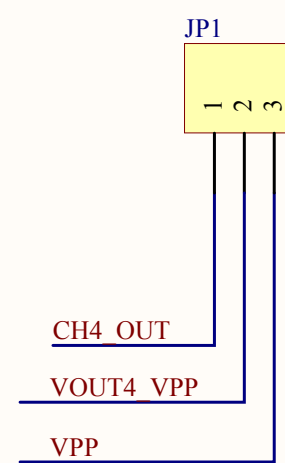
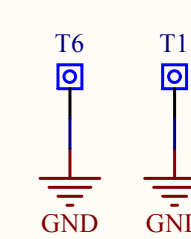
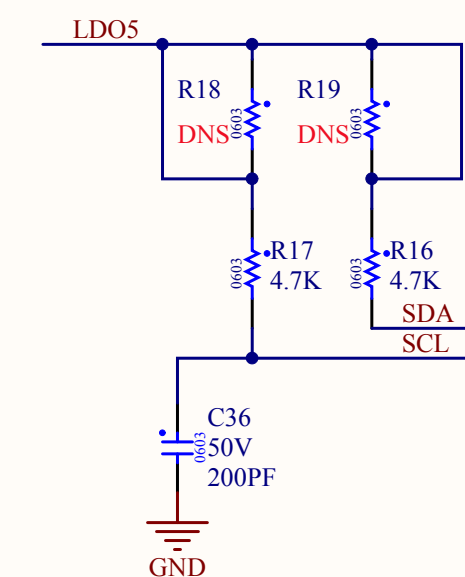
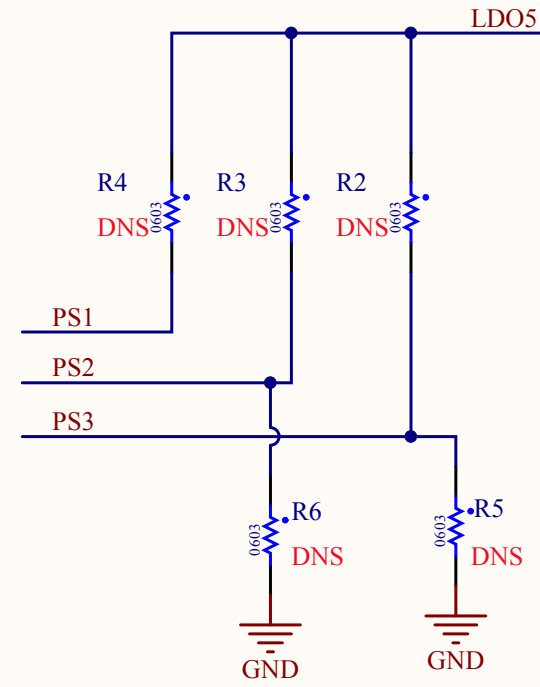
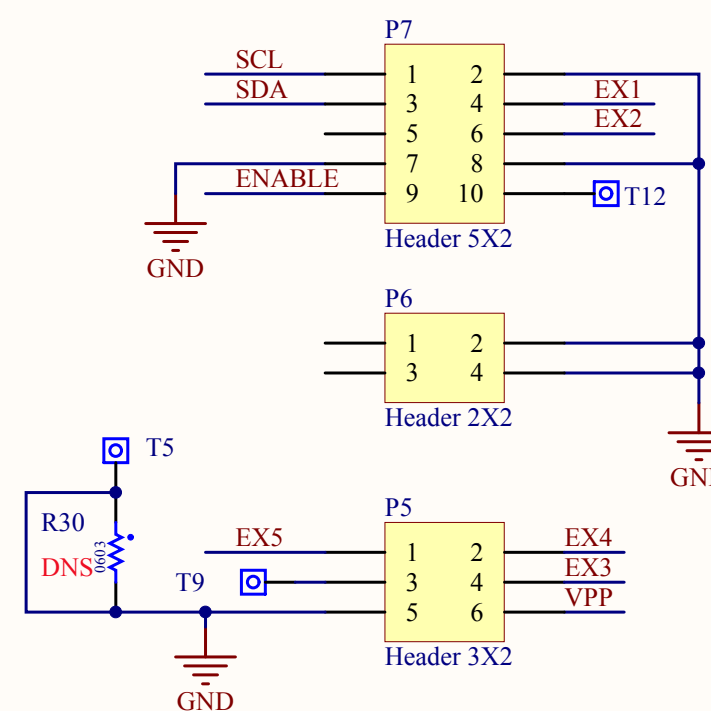
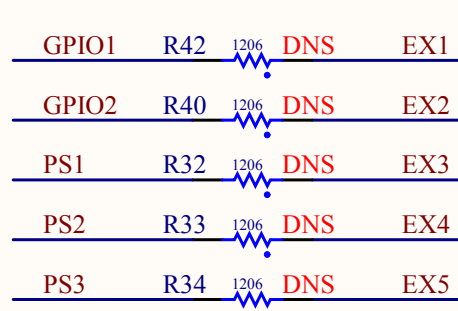
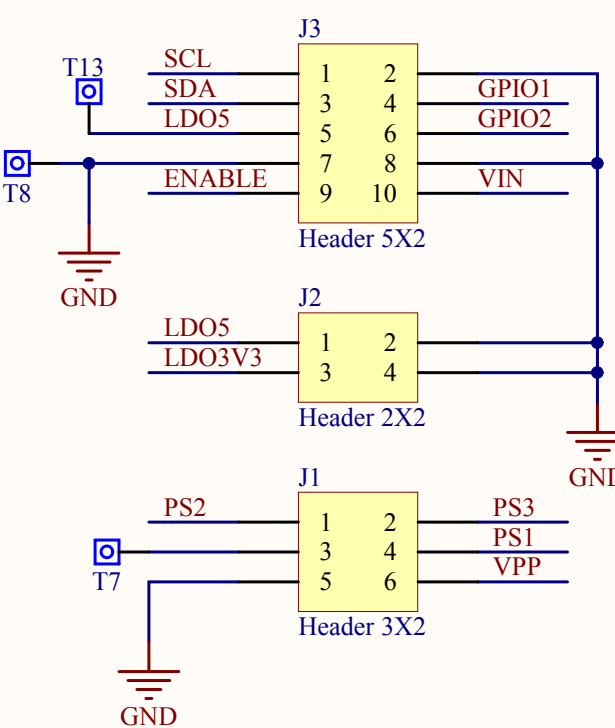
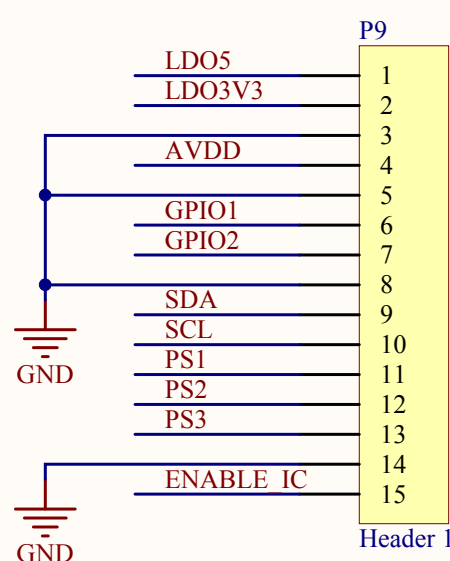
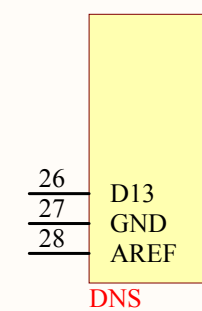
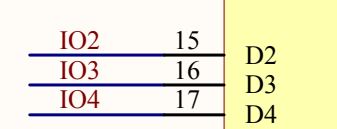
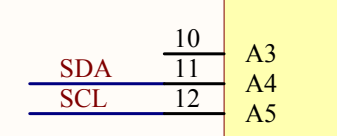
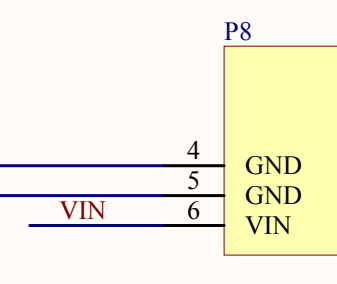
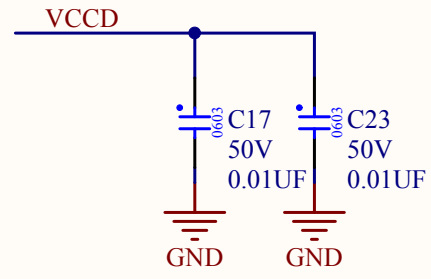
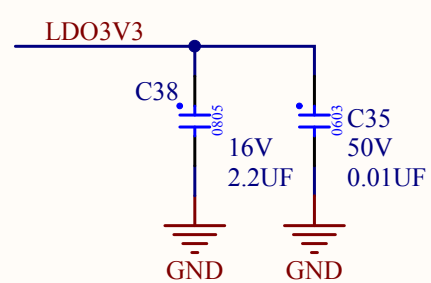
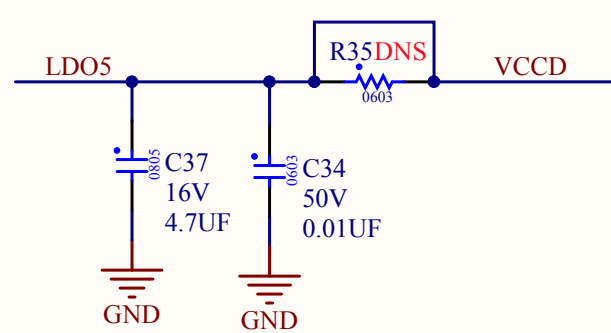
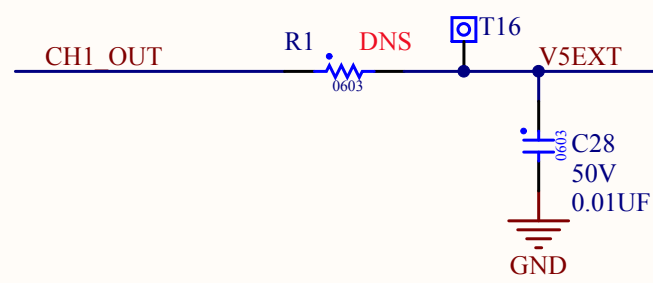
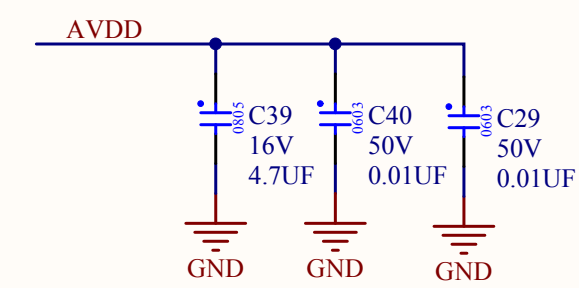
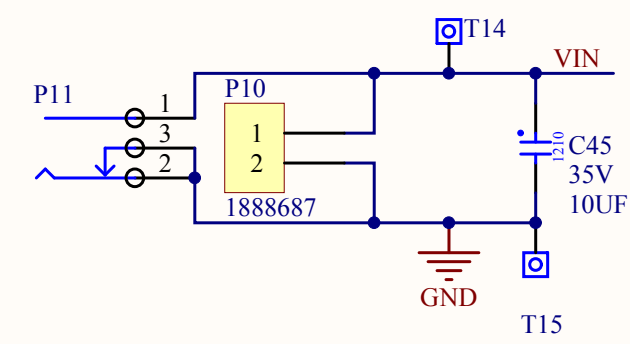


Fig. 3: XRP7724EVB-DEMO-1 Board Connections





BILL OF MATERIAL

Ref.	Qty	Manufacturer	Part Number	Size	Component
U1	1	Exar Corp.	XRP7724	TQFN44	2nd Generation 4Ch. Sw. Controller
Q1,Q2	2	FAIRCHILD	FDMC8200	Power 33	Dual N-Channel Power Trench MOSFET
Q3	1	FAIRCHILD	FDMC7660	Power 33	N-Channel Power Trench MOSFET
Q4	1	FAIRCHILD	FDMC8882	MLP 3.3X3.3	N-Channel Power Trench MOSFET
Q5	1	FAIRCHILD	FDMS7560S	Power 56	N-Channel Power Trench SyncFET
Q6	1	Vishay Siliconix	SIR474DP	PowerPAK SO-8	N-Ch. 30-V (D-S) MOSFET
L1	1	WURTH ELECTRONK	744314490	7.0x6.9mm	Inductor 4.9uH, 14.5mΩ, 6.5A
L2	1	WURTH ELECTRONK	744314330	7.0x6.9mm	Inductor 3.3uH, 9.0mΩ, 9.0A
L3	1	WURTH ELECTRONK	744314200	7.0x6.9mm	Inductor 2.0uH, 5.85mΩ, 11.5A
L4	1	WURTH ELECTRONK	7443551130	13.2X12.8mm	Inductor 1.3uH, 1.8mΩ, 25A
C1,C2,C5,C6	4	MURATA CORP.	GRM32ER70J476KE20L	1210	CAP CER 47uF, 6.3V, X7R, 10%
C3,C4,C7,C11,C12,C15	6	MURATA CORP.	GRM32ER60J107M20L	1210	CAP CER 100uF, 6.3V, X5R, 20%
C8,C9,C10,C16	4	MURATA CORP.	GRM21BR71H105KA12L	0805	CAP CER 1.0uF, 50V, X7R, 10%
C13,C14,C20,C30,C31,C32,C45	7	MURATA CORP.	GRM32ER7YA106KA12L	1210	CAP CER 10uF, 35V, X7R, 10%
C17,C23,C27-C29,C34,C35,C40	8	MURATA CORP.	GRM188R71H103KA01D	0603	CAP CER 0.01uF, 50V, X7R, 10%
C18,C24,C37,C39	4	MURATA CORP.	GRM21BR71C475KA73	0805	CAP CER 4.7uF, 16V, X7R, 10%
C19,C21,C22,C25,C33,C41-C44	9	MURATA CORP.	GRM188R71H104KA93D	0603	CAP CER 0.1uF, 50V, X7R, 10%
C26	1	MURATA CORP.	GRM188R71H222KA01D	0603	CAP CER 2200pF, 50V, X7R, 10%

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Ref.	Qty	Manufacturer	Part Number	Size	Component
C36	1	MURATA CORP.	GRM1885C1H201JA01D	0603	CAP CER 200pF, 50V,X7R,10%
R16,R17	2	PANASONIC	ERJ-3EKF4701V	0603	RES 4.7K OHM, 1/10W, 1%, SMD
J1	1	WURTH ELECTRONK	61300624321	2.54mm Angled Dual Socket	2.54mm dual Pin Socket Header WR-PHD
J3	1	WURTH ELECTRONK	613 010 243 121	2.54mm Angled Dual Socket	2.54mm dual Pin Socket Header WR-PHD
JP1	1	WURTH ELECTRONK	61300311121	2.54mm Pin Header	2.54mm Pin Header WR-PHD, 3 Pins
JP1(jumper)	1	609 002 115 121	WURTH ELECTRONK	2.54mm Pin Jumper	2.54mm Pin Jumper w/Test Point
P1, P2,P3,P4,P10	5	Phoenix Contact	1888687	9.5x5.08mm	CONN.TERM. BLOCK 2POS
P5	1	WURTH ELECTRONK	61300621021	2.54mm Dual Pin Header	2.54mm Dual Pin Header Wr-PHD
P7	1	WURTH ELECTRONK	61301021021	2.54mm Dual Pin Header	2.54mm Dual Pin Header Wr-PHD
P9	1	WURTH ELECTRONK	61301511121	2.54mm Pin Header	2.54mm Pin Header WR-PHD, 15 Pins
P11	1	Switchcraft Corp.	RAPC722X	2.1mmID, 5.5mmOD	Conn. Powerjack Mini R/A, T/H
T6,T8,T10,T11	4	WURTH ELECTRONK	61304011121	2.54mm Pin Header	2.54mm Pin Header WR-PHD, 40 Pins

EVALUATION BOARD LAYOUT

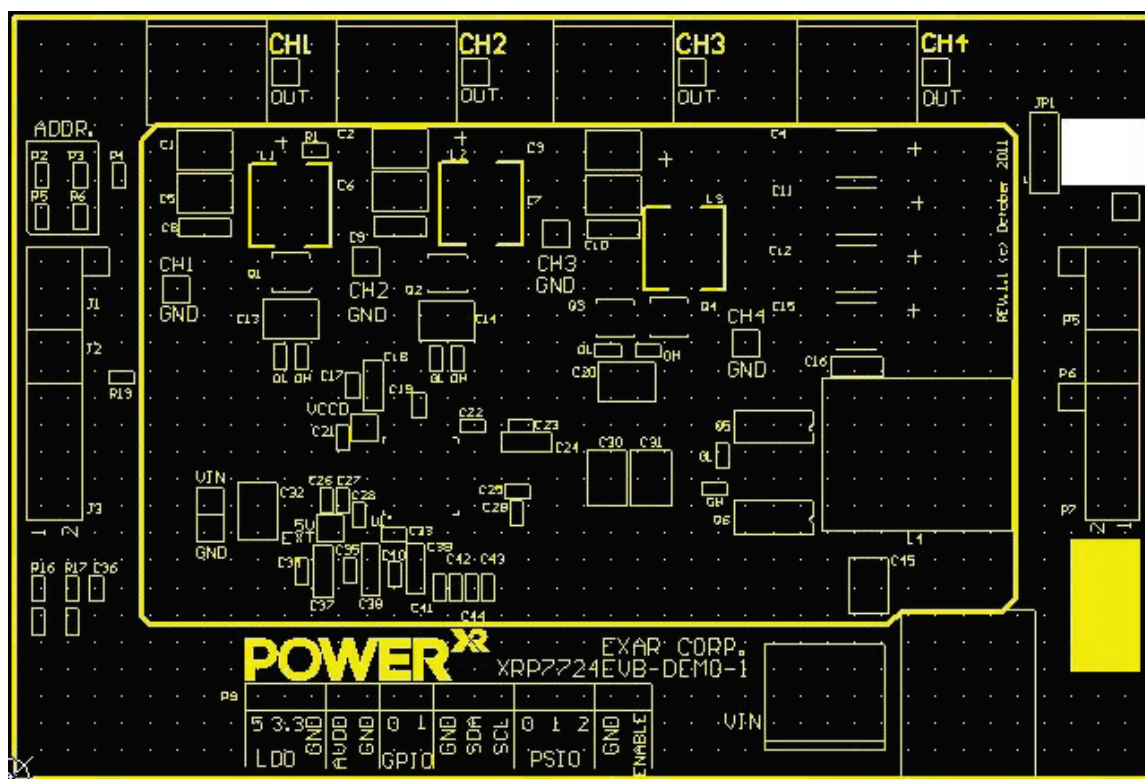


Fig. 4: Component Placement – Top Side

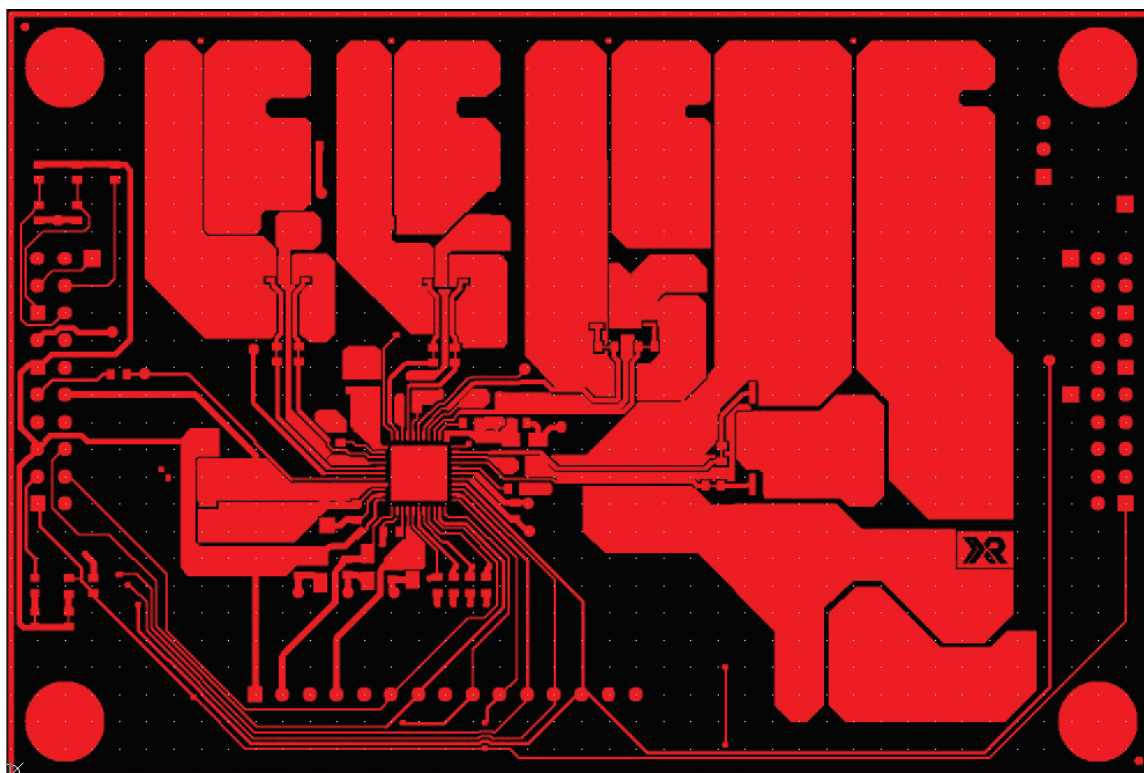


Fig. 5: Layout – Top Side

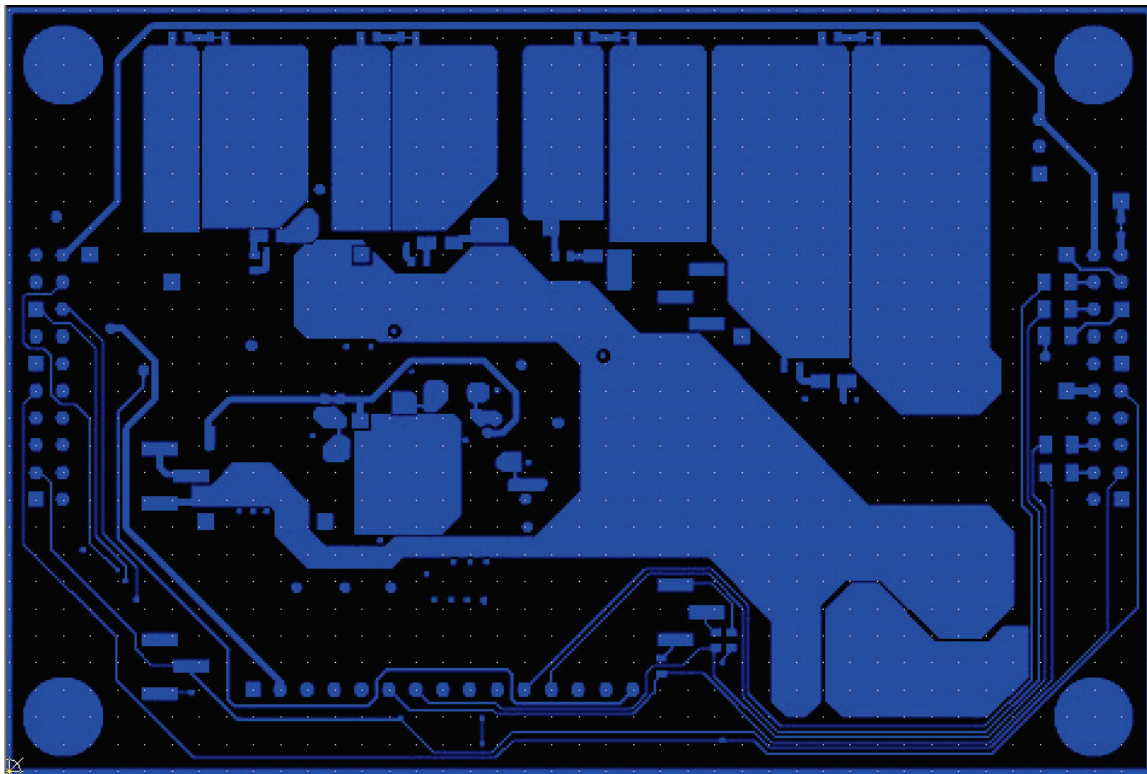


Fig. 6: Layout - Bottom

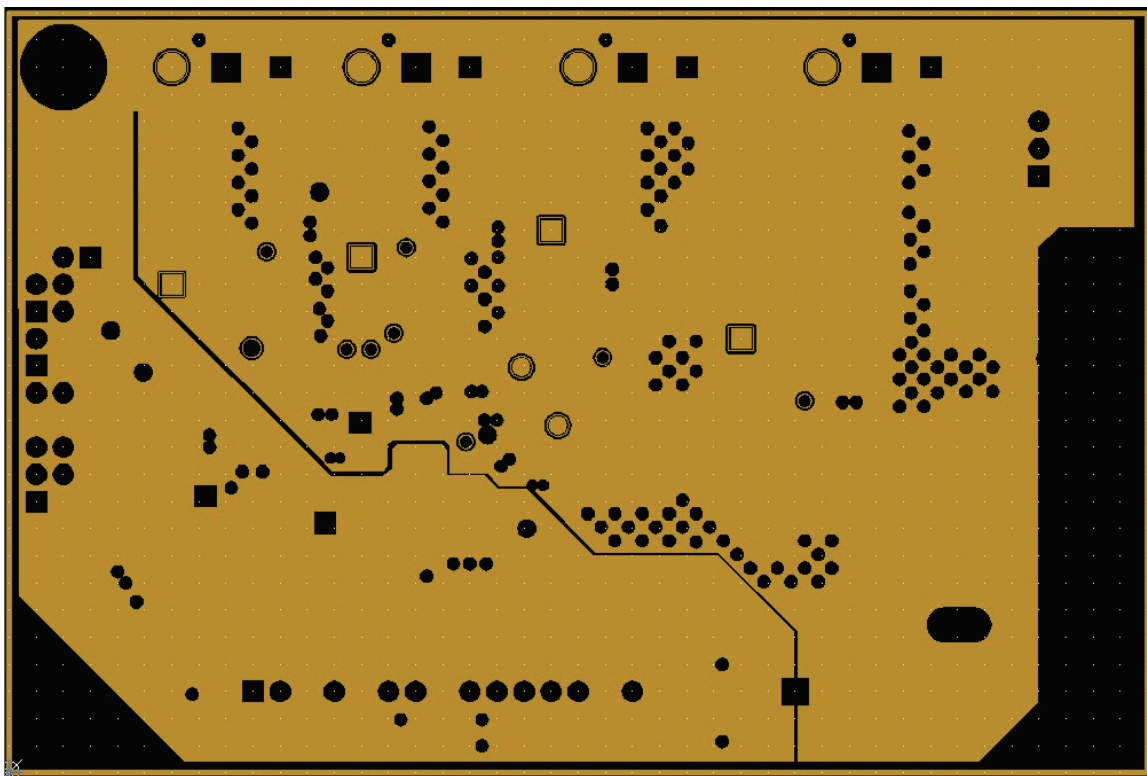


Fig. 7: Layout – Middle Layer 1

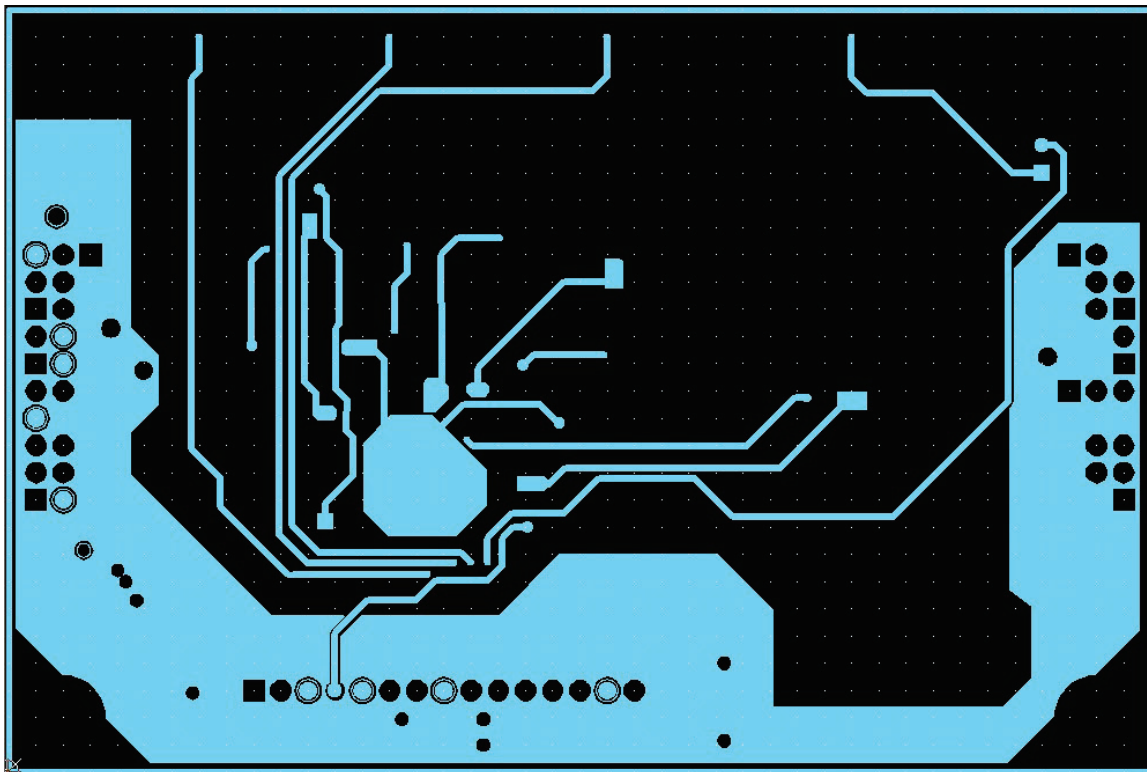


Fig. 8: Layout – Internal Plane

DOCUMENT REVISION HISTORY

Revision	Date	Description
1.0.0	09/28/12	Initial release of document

BOARD REVISION HISTORY

Board Revision	Date	Description
XRP7724EVB-DEMO-1-01	10/01/12	Initial release of evaluation board

FOR FURTHER ASSISTANCE

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