


MCIMX6SLEVK board

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Revision History

Rev. Code	Date	Description
A	2012/05/11	Rev A
B	2012/09/27	<p>ENGR00225877. Replaced D24 with BAT54C-7-F ENGR00225876. DNP standoffs H1, H2, H3 and H4 ENGR00225878. Replaced R11, R129 and R130 with SH14, SH15 and SH16 respectively ENGR00225879.</p> <ol style="list-style-type: none"> 1. Replaced U3 - MMPF0100NPEP with MMPF0100F1EP 2. Replaced C23 (0.1uF, 0402) with 0.22uF, 0201 3. Added C410, C412 per PMIC datasheet 4. Replaced C40 (0.1uF, 0402) with 0.22uF, 0201 5. Replaced C27, C28 and C32 (0.1uF) with 0.22uF 6. Replaced C70 (22uF, 0603, 6.3V) with 47uF, 0805, 10V <p>ENGR00226044. Replaced P4 - WM-64PNT with WM-64PCT ENGR00226043. Replaced U2 - K4P8G304EB-AGC1 with MT42L256M32D2LG-25WT ENGR00225880.</p> <ol style="list-style-type: none"> 1. Replaced C146 (10uF) with 47uF 2. Replaced C159 and C160 (0402, 6.3V) with 0603, 10V <p>ENGR00225881.</p> <ol style="list-style-type: none"> 1. Move PMIC SW1AB feedback to the load side of SH2 to compensate for SH2 voltage drops during current measurement. 2. Move PMIC SW1C feedback to the load side of SH3 to compensate for SH3 voltage drops during current measurement. 3. Move PMIC SW2 feedback to the load side of SH1 to compensate for SH1 voltage drops during current measurement. 4. Move PMIC SW3 feedback to the load side of SH5 to compensate for SH5 voltage drops during current measurement. <p>ENGR00225088. Connected J12.117 to POR_B ENGR00226215. Renamed PFUSE_VIN net to PF0100_VIN ENGR00227037. Replaced all capacitors in PF0100_VIN net whose voltage rating is less than 10V with 10V capacitors: C46, C47, C66, C41, C48, C63, C58. ENGR00227038. Flipped the capacitors whose polarity was inverted: C4, C2, C11, C21, C36, C46, C47, C58, C66, C156, C166, C178, C218, C200. ENGR00223967:</p> <ol style="list-style-type: none"> 1. Added test points TP42, 43, 44 and 45 2. The following pins were changed to NC in J8: CLKREQ#, UIM_C8, UIM_C4W, SMB_CLK, SMB_DATA, LED_WLAN#, LED_WPAN#, Reserved1-8, Reserved10 3. DNP C140, C191, C192 and C210 <p>ENGR00229277: Y1 (CC7V-T1A) 9pF is selected as default/preferred part. However, 12pF version may be used for production board. ENGR229701:</p> <ol style="list-style-type: none"> 1. Removed R195. 2. Replaced C152 (150uF) with 2.2uF

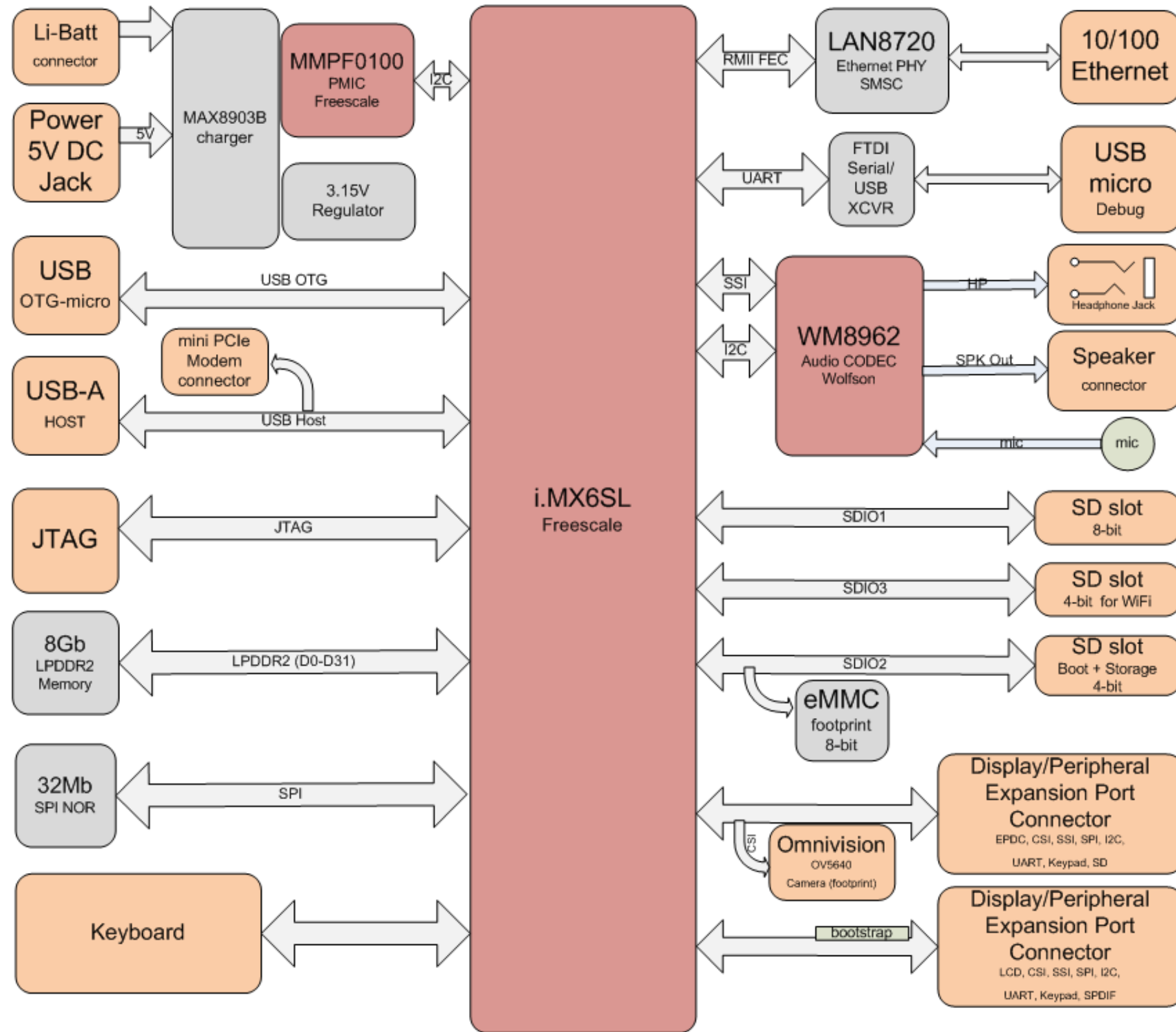


ICAP Classification: FCP: _____ FILE: X PUBL: _____
 Drawing Title: **MCIMX6SLEVK board**
 Page Title: **Title and Rev History**

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Date: Monday, October 15, 2012 | Sheet 1 of 16

MCIMX6SLEVK board Diagram



ICAP Classification: FCP: ___ FIUO: X PUBL: ___

Drawing Title: **MCIMX6SLEVK board**

Page Title: **Block Diagram**

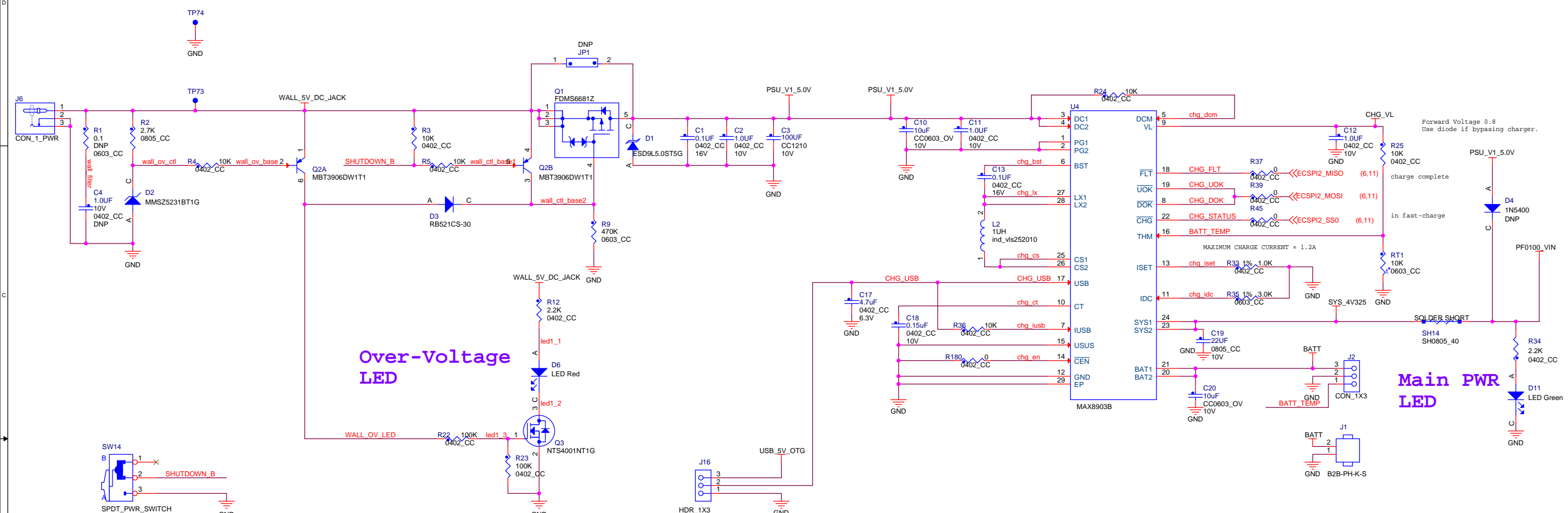
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Date: Wednesday, October 10, 2012 | Sheet 2 of 16

DC JACK 5V

Over Voltage Protection

Lithium Charger



Over-Voltage
LED

Main PWR
LED

PWR Cut Switch For SW Development

Secondary Charge Source USB or Wireless Charger

Lithium single cell battery connectors

Note:
Shunt 2-3 to experiment with USB charging.
Use cable to pins 1 and 2 to experiment with wireless charging

NEED TO FIGURE OUT THIS BETTER
PWRCTRL3 is the capacitive touch interrupt.
MISO and SSO might be OK.
must permanently decide to eliminate ability to use
Also should use pullups inside the processor

freescale

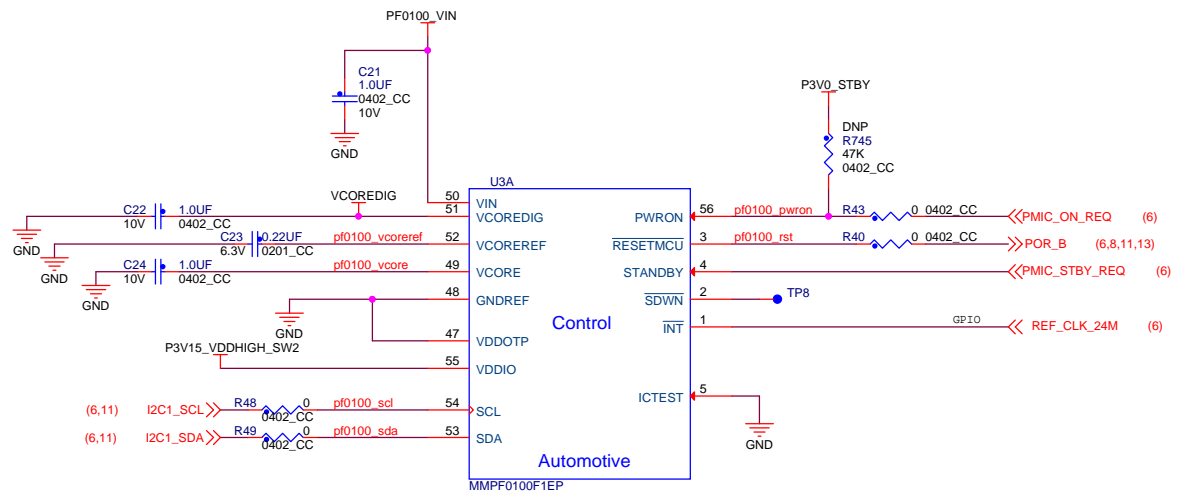
ICAP Classification: FCP: _____ FIUC: X PUBI: _____
 Drawing Title: **MCIMX6SLEVK board**
 Page Title: **SYS Power**

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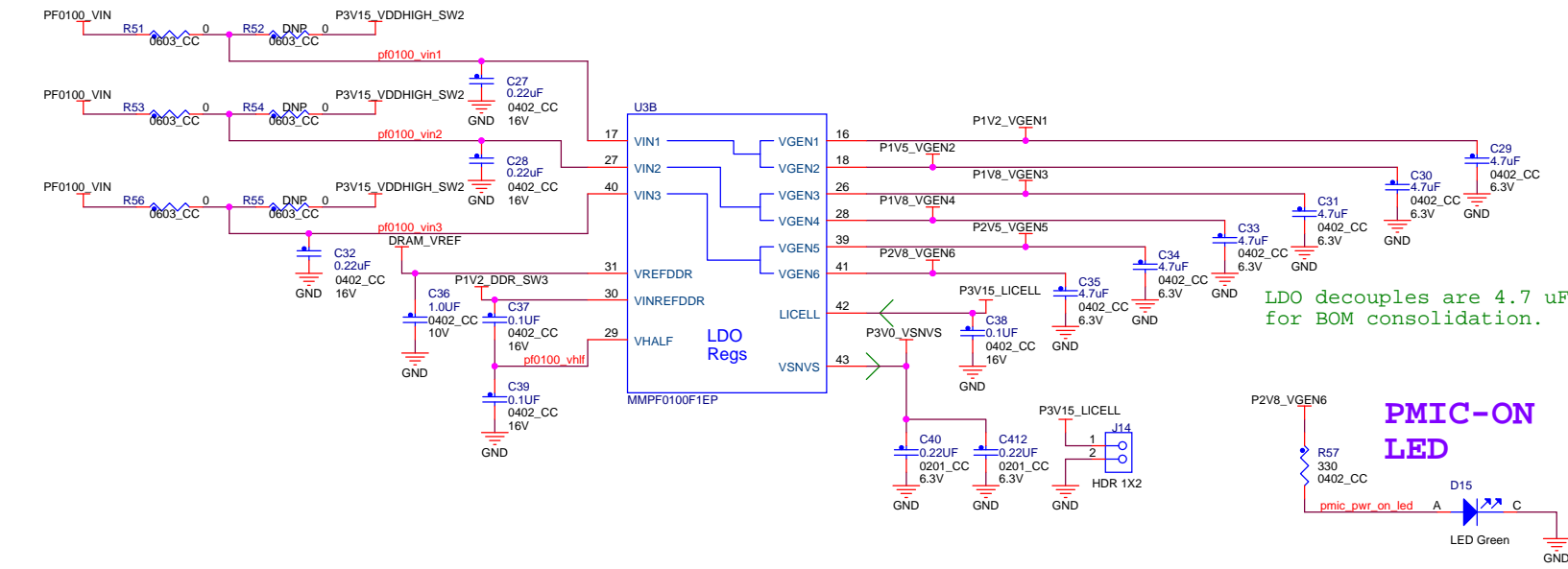
Freescale MMPF0100NPEP PMIC

Note:
This device is factory configurable for voltage and timings.
This reference design is configured to run from factory pre-programmed parts.
Ordering selections with common i.MX6SL voltages/timings are available.
Please check the device datasheet for latest ordering info.

Note:
MMPF0100 erratum ER19 can affect some of the systems, depending on the system characteristics. Please check this erratum and its workaround to see if applies.

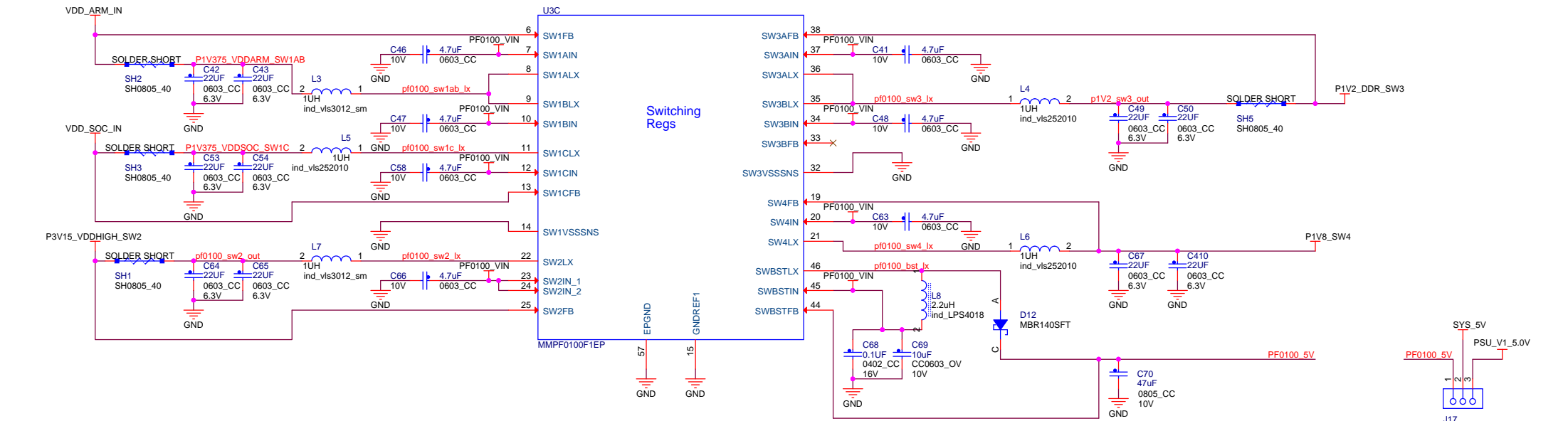
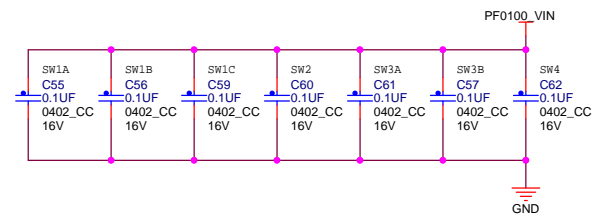


With low-inductive paths between VIN the voltage sources, either 0.22 uF or 0.47 uF may be used.



PMIC output rails				
PF0100	Voltage(V)	Current(A)	Power up sequence	Note
SW1A/B	1.375	2.5	1	
SW1C	1.375	1.7	1	
SW2	3.15	2	2	
SW3A/B	1.2	2.5	4	
SW4	1.8	1	3	
SWBST	5	0.6		
VGEN1	1.2	0.1	4	
VGEN2	1.5	0.25		
VGEN3	1.8	0.1		
VGEN4	1.8	0.35	3	
VGEN5	2.5	0.1	5	LED
VGEN6	2.8	0.2		
VSNVS	3	0.0002	0	
VREFDDR	0.6	0.01	4	

SW1A/B = 1.375 V for boot-up at ~800 MHz.
Recommend that software increase SW1A/B to 1.425 V for 1 GHz operation.



Note:
Switcher currents and optimum inductor sizes vary depending on application.
Please refer to the latest part datasheet for inductor recommendations.

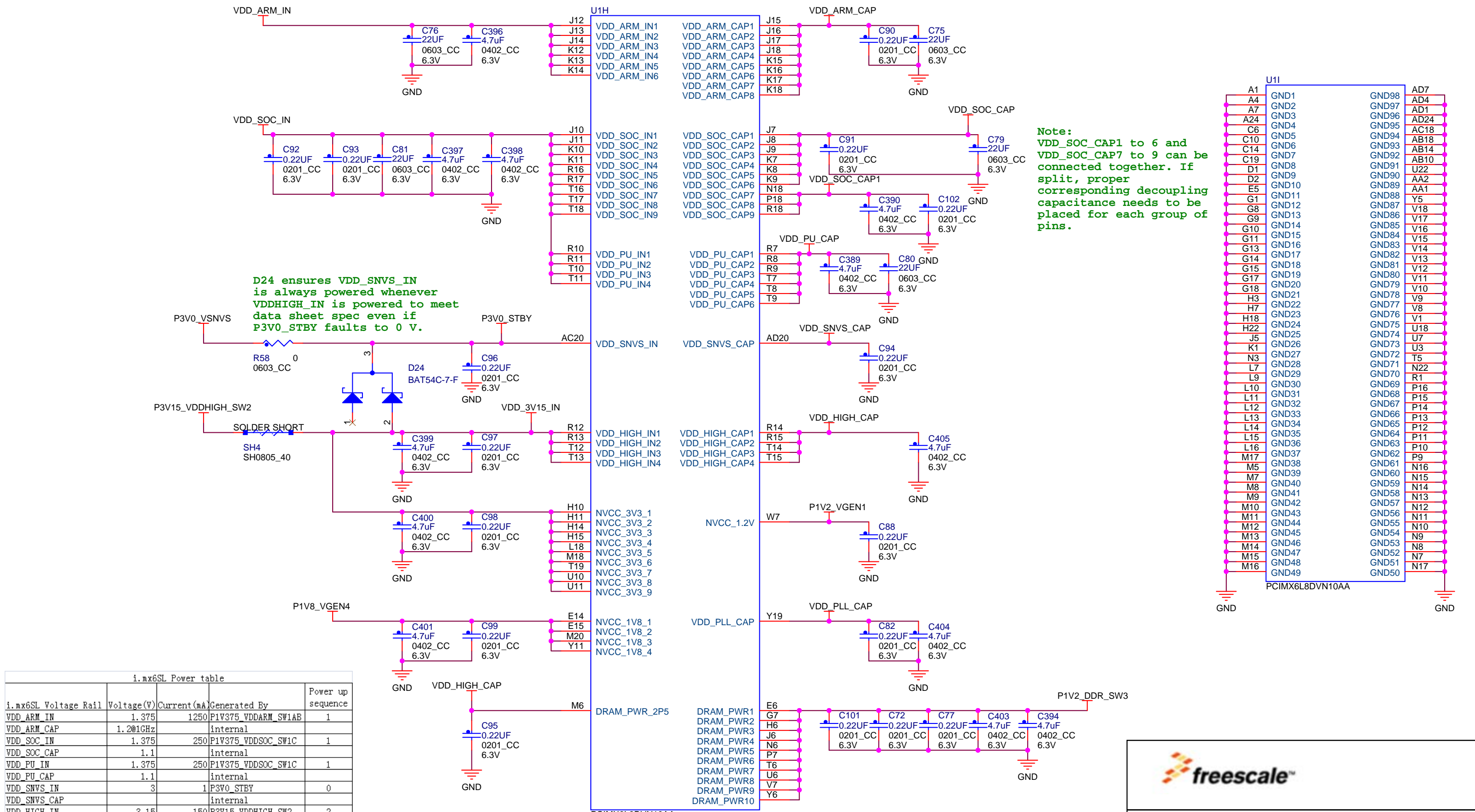
Note: J17
Shunt 1-2 for SYS_5V from PMIC: 600mA limited
Shunt 2-3 for SYS_5V from wall adapter

freescale

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Page Title: **PMIC**

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D24 ensures VDD_SNVS_IN is always powered whenever VDDHIGH_IN is powered to meet data sheet spec even if P3V0_STBY faults to 0 V.

Note:
VDD_SOC_CAP1 to 6 and VDD_SOC_CAP7 to 9 can be connected together. If split, proper corresponding decoupling capacitance needs to be placed for each group of pins.

i.mx6SL Power table				
i.mx6SL Voltage Rail	Voltage(V)	Current(mA)	Generated By	Power up sequence
VDD_ARM_IN	1.375	1250	P1V375_VDDARM_SW1AB	1
VDD_ARM_CAP	1.2@1GHz		internal	
VDD_SOC_IN	1.375	250	P1V375_VDDSOC_SW1C	1
VDD_SOC_CAP	1.1		internal	
VDD_PU_IN	1.375	250	P1V375_VDDSOC_SW1C	1
VDD_PU_CAP	1.1		internal	
VDD_SNVS_IN	3	1	P3V0_STBY	0
VDD_SNVS_CAP			internal	
VDD_HIGH_IN	3.15	150	P3V15_VDDHIGH_SW2	2
VDD_HIGH_CAP	2.5		internal	
NVCC_3V3	3.15	150	P3V15_VDDHIGH_SW2	2
NVCC_1V8	1.8	125	P1V8_VGEN4	3
NVCC_1.2V	1.2		P1V2_VGEN1	4
VDD_PLL_CAP	1.1		internal	
VDD_USB_CAP	3		internal	
DARM_PWR_2P5	2.5		VDD_HIGH_CAP	2
DRAM_PWR	1.2	200	P1V2_DDR_SW3	4
DRAM_VREF	0.6		POW6_VREFDDR	4

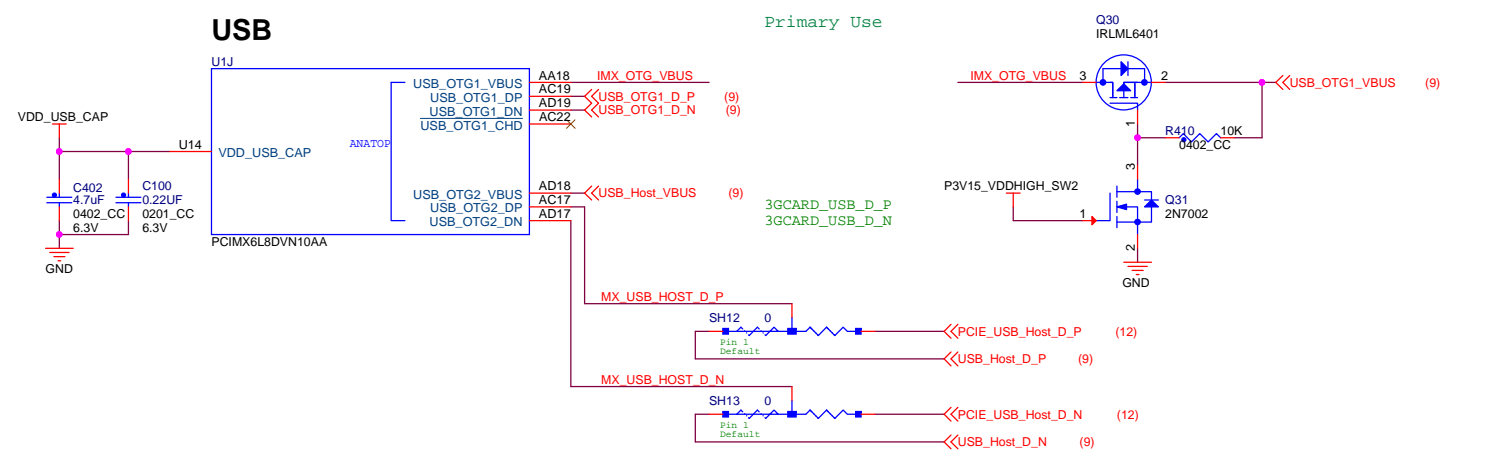
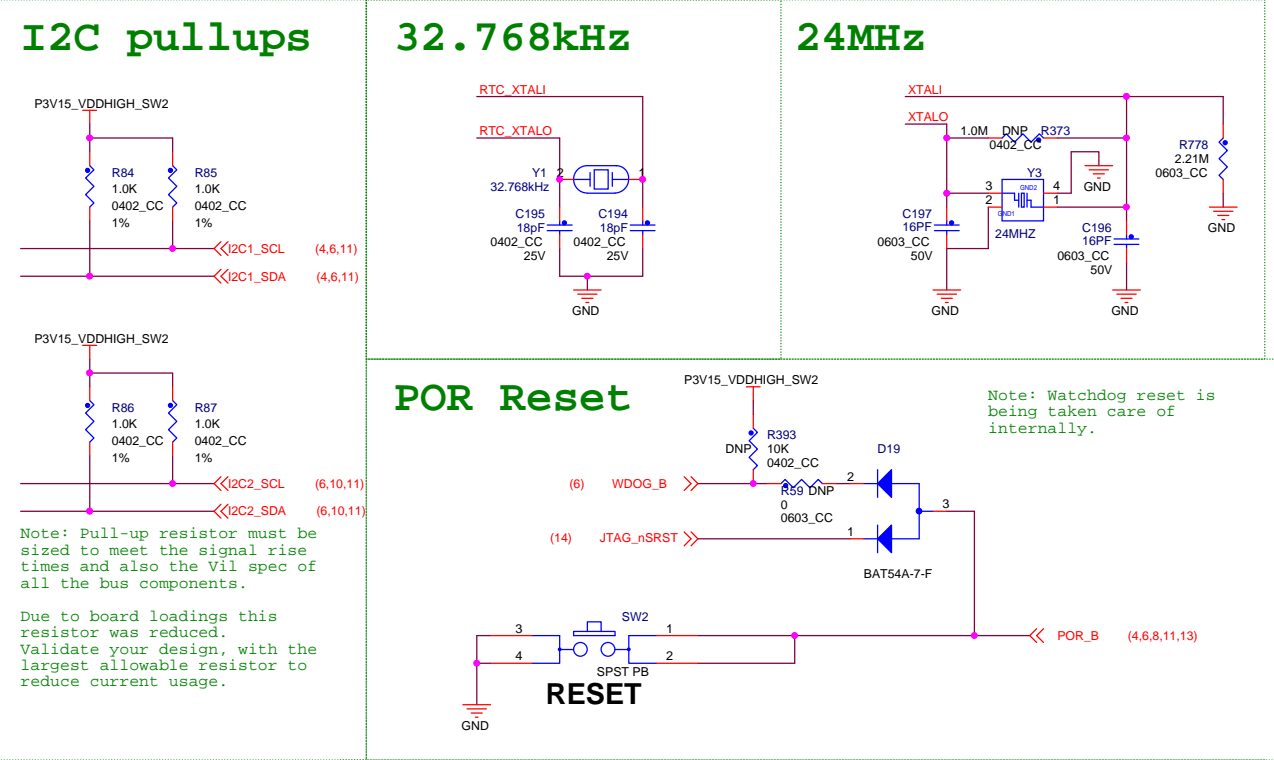
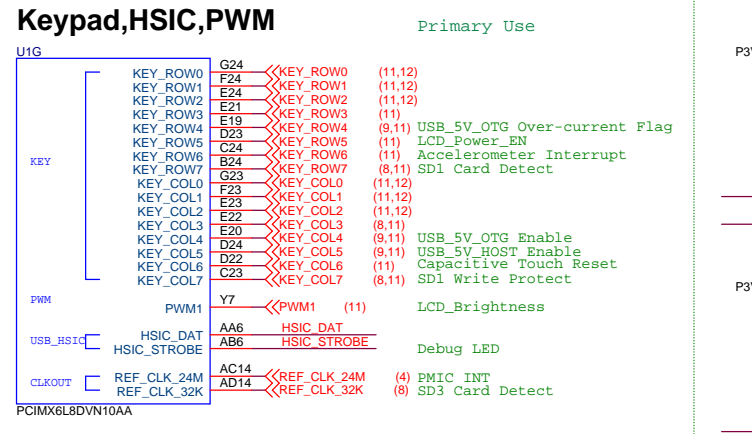
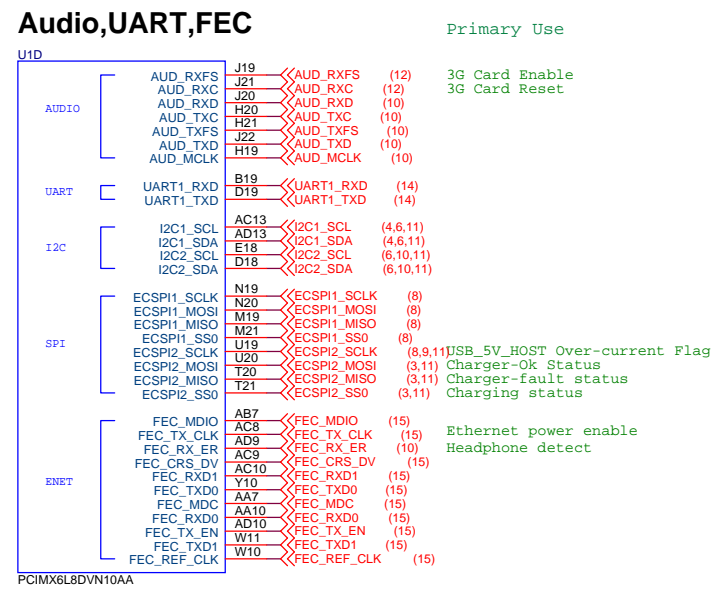
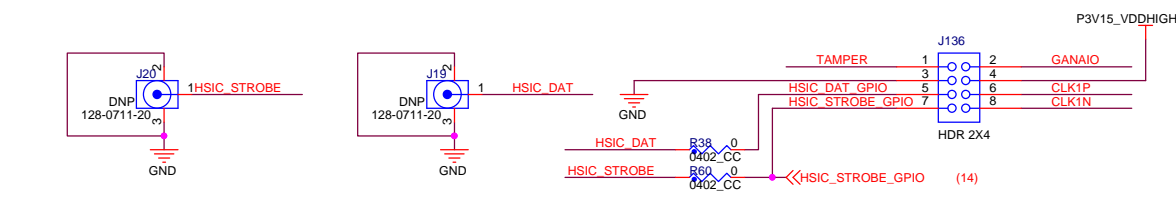
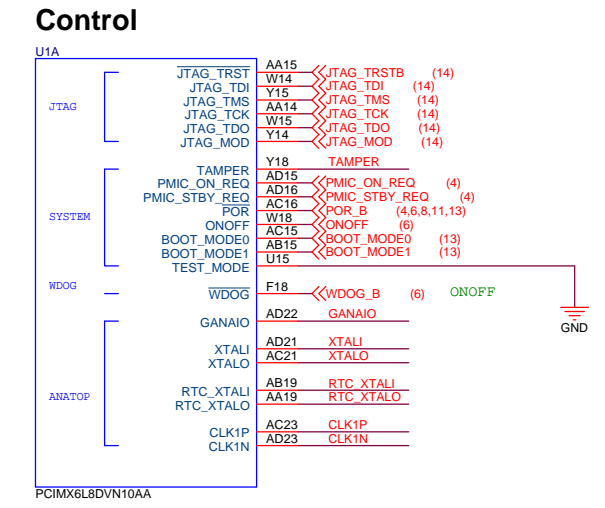
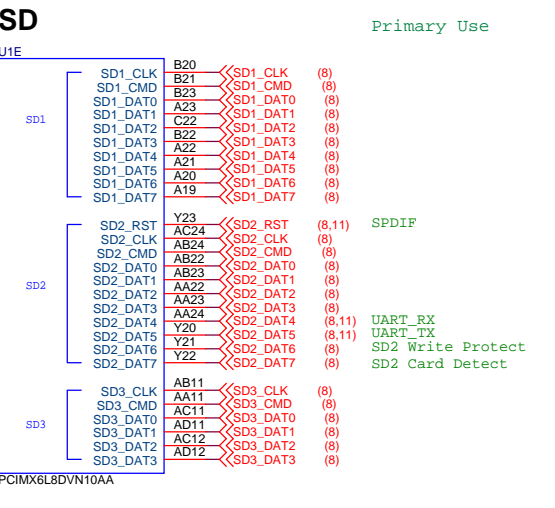
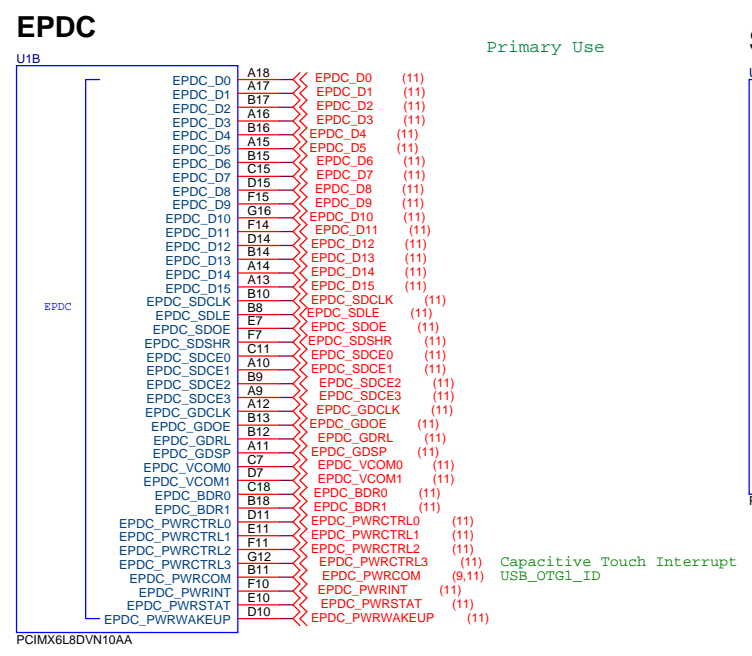
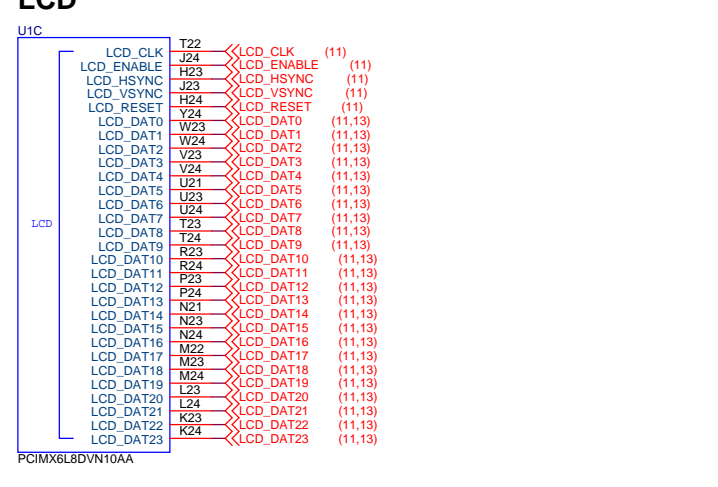


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 Page Title: **IMX6SL_Power**

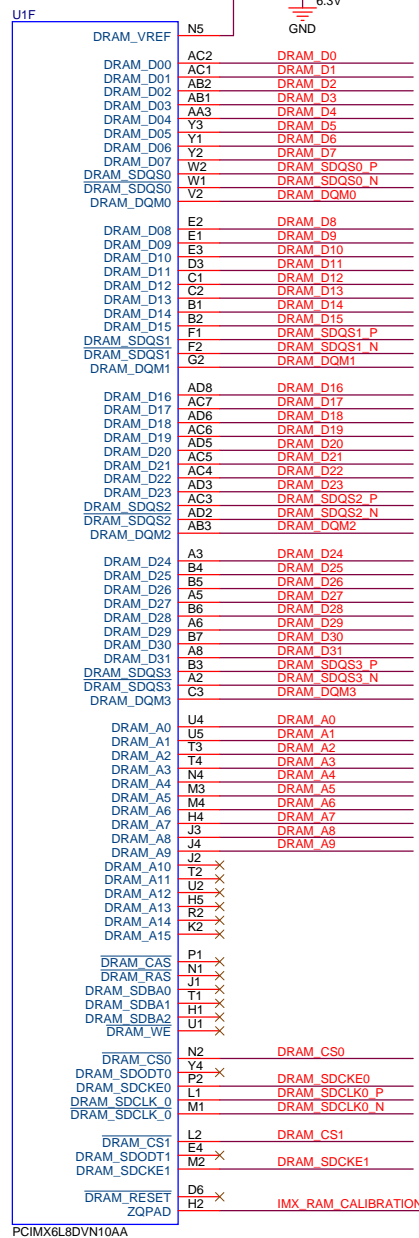
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i.MX6SL LCD

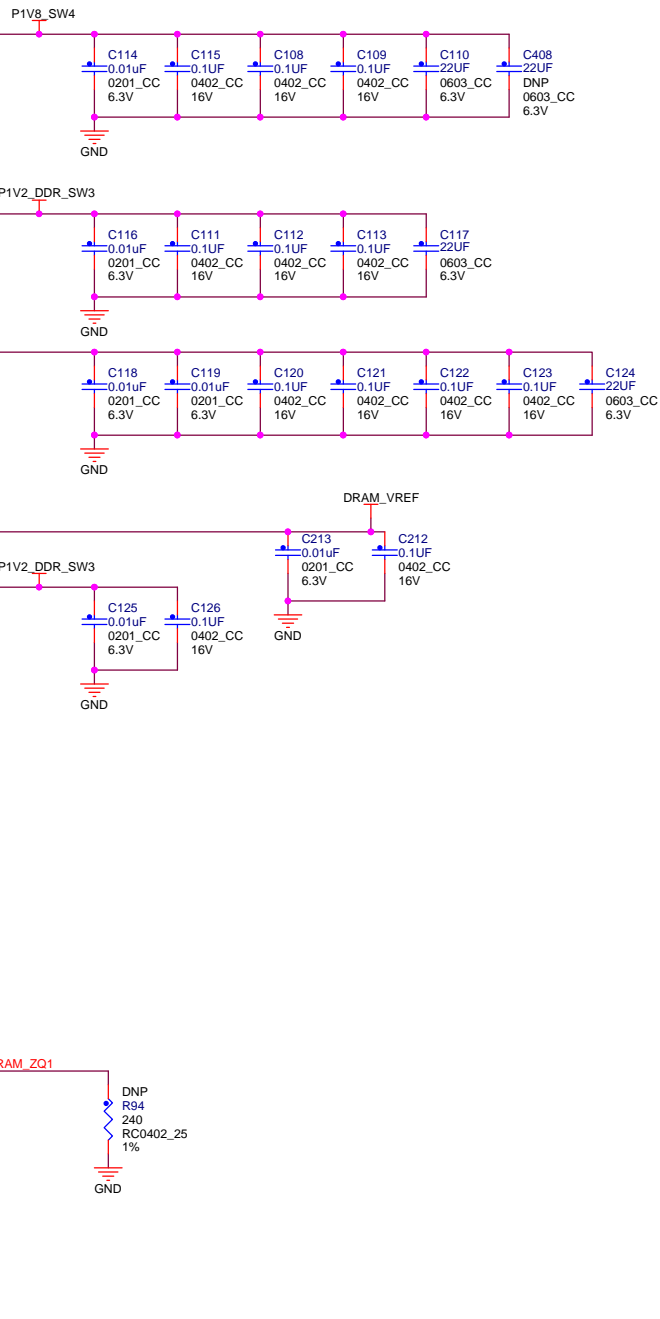
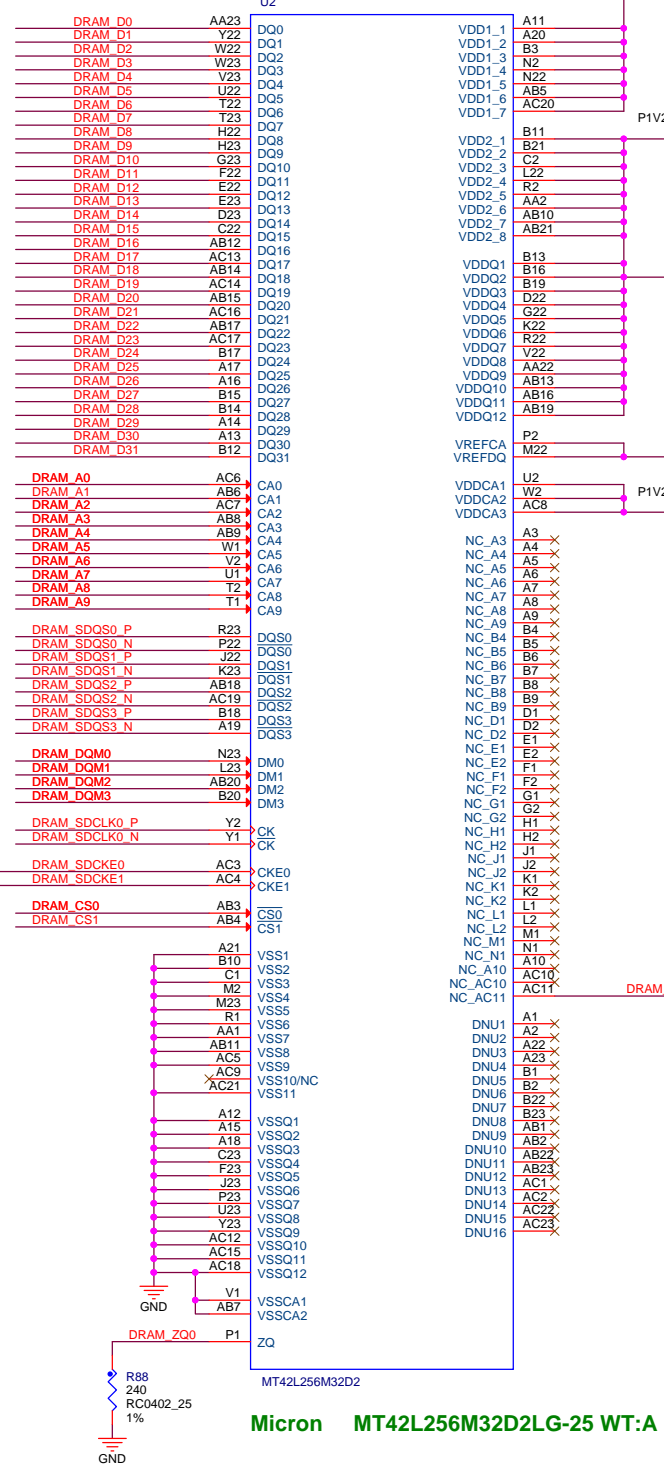


i.MX6SL
DDR



PCIMX6L8DVN10AA

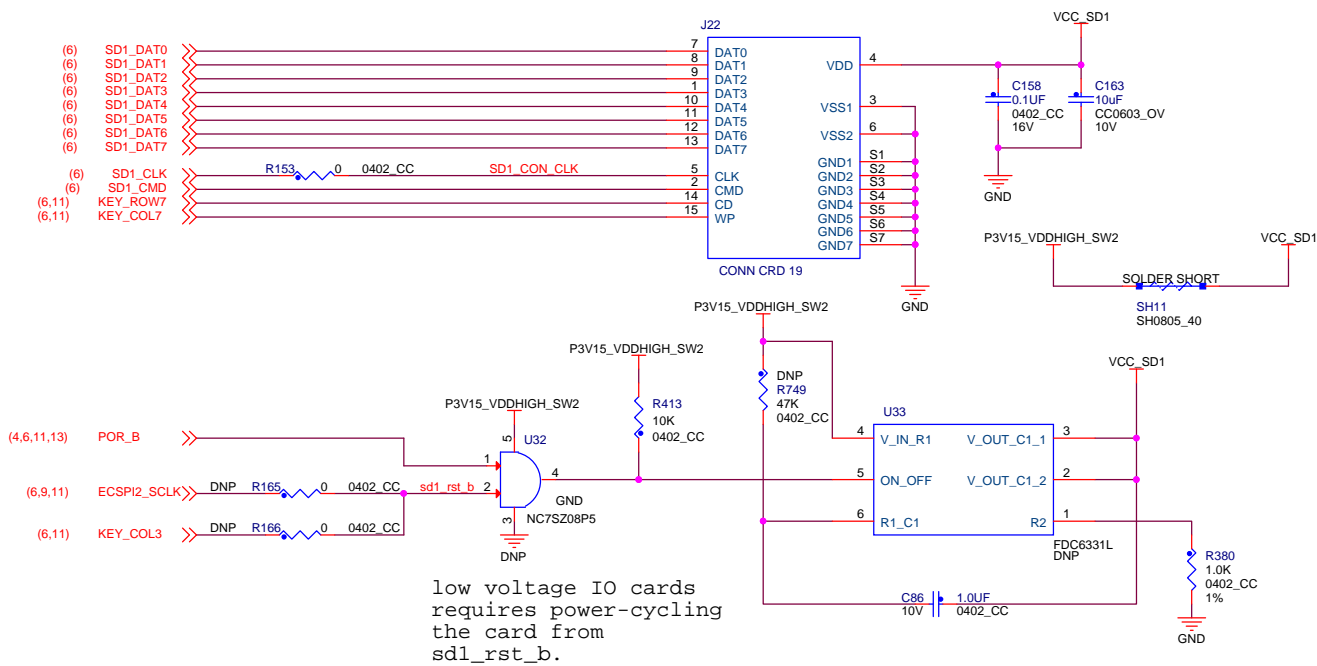
LPDDR2
8Gb 400MHz clock



Note:
Some dual-die LPDDR2 packages
require a separate ZQ at pin AC11.

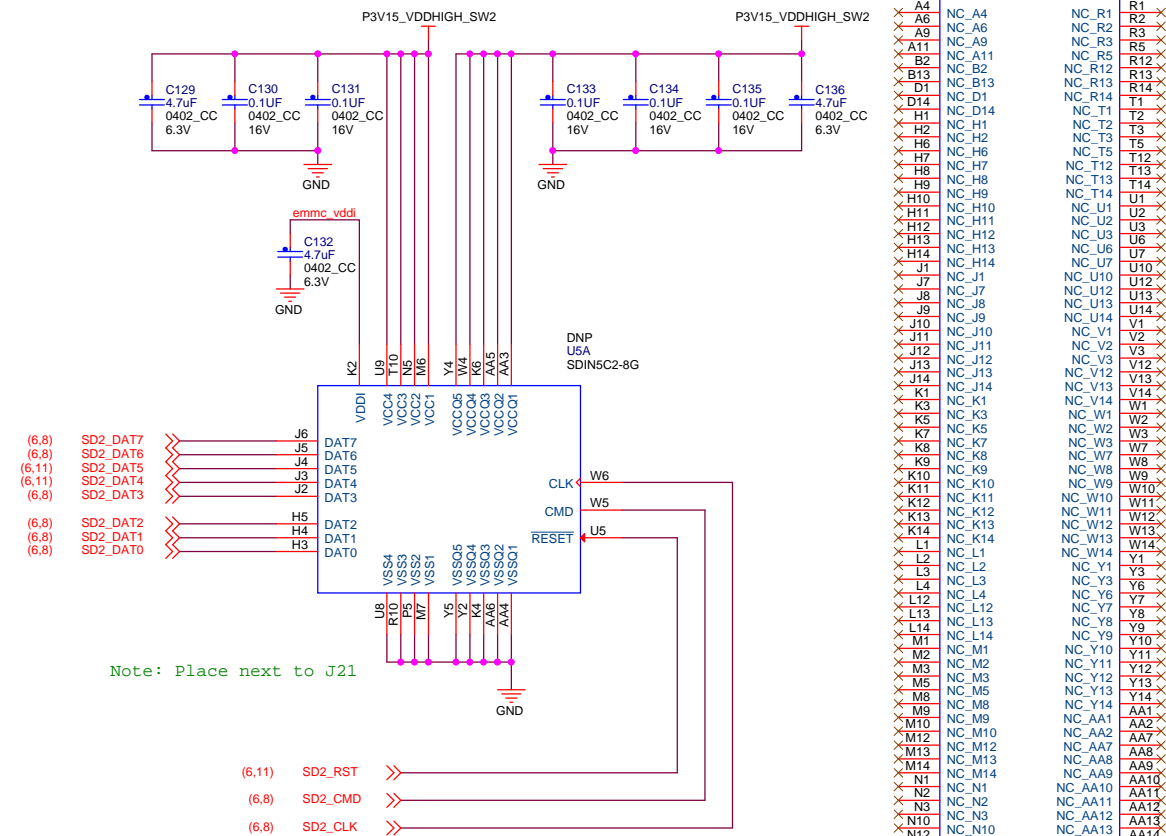
SD1 - For Primary External Card Slot

8-bit SD



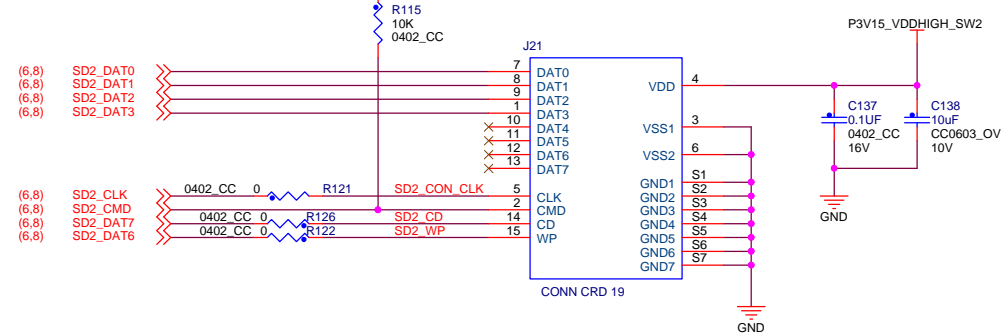
eMMC Footprint

8GB eMMC

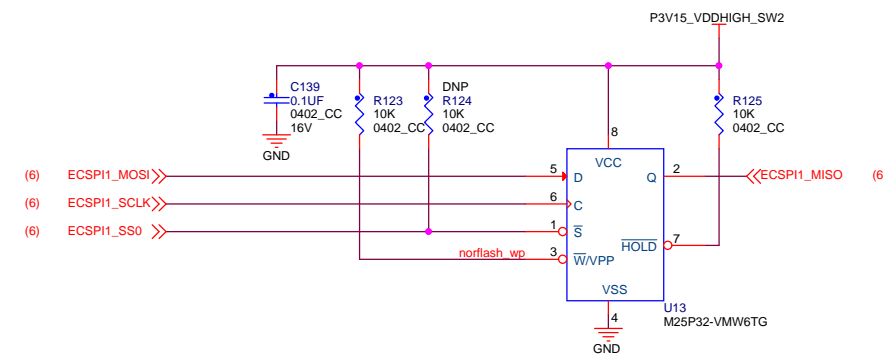


SD2 - For Boot Code

4-bit BOOT SD

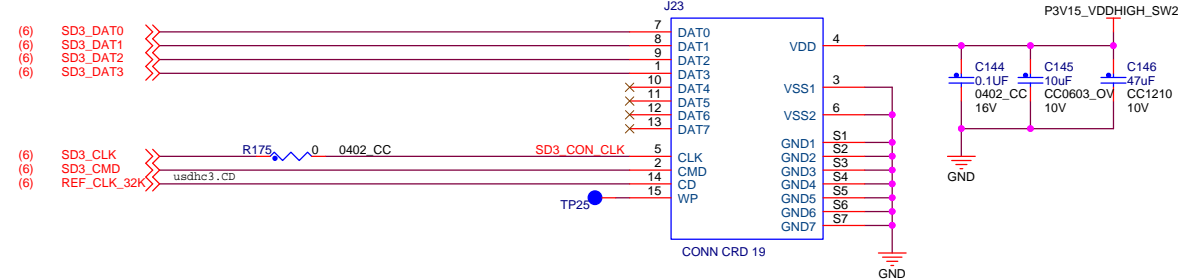


4MB SPI NOR FLASH



SD3 - for WiFi and SD Accessories

For WiFi

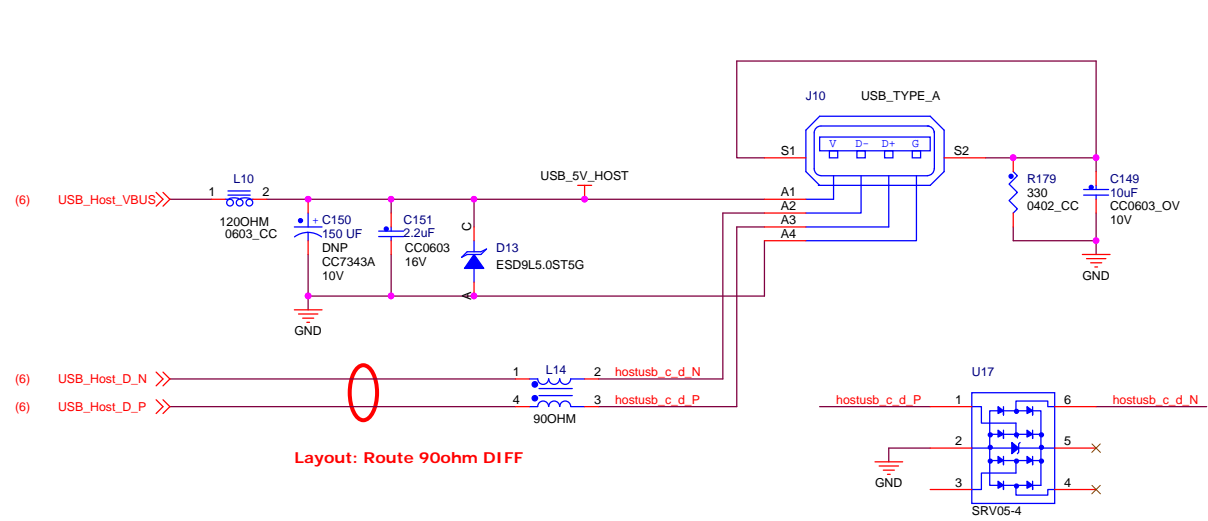


freescale

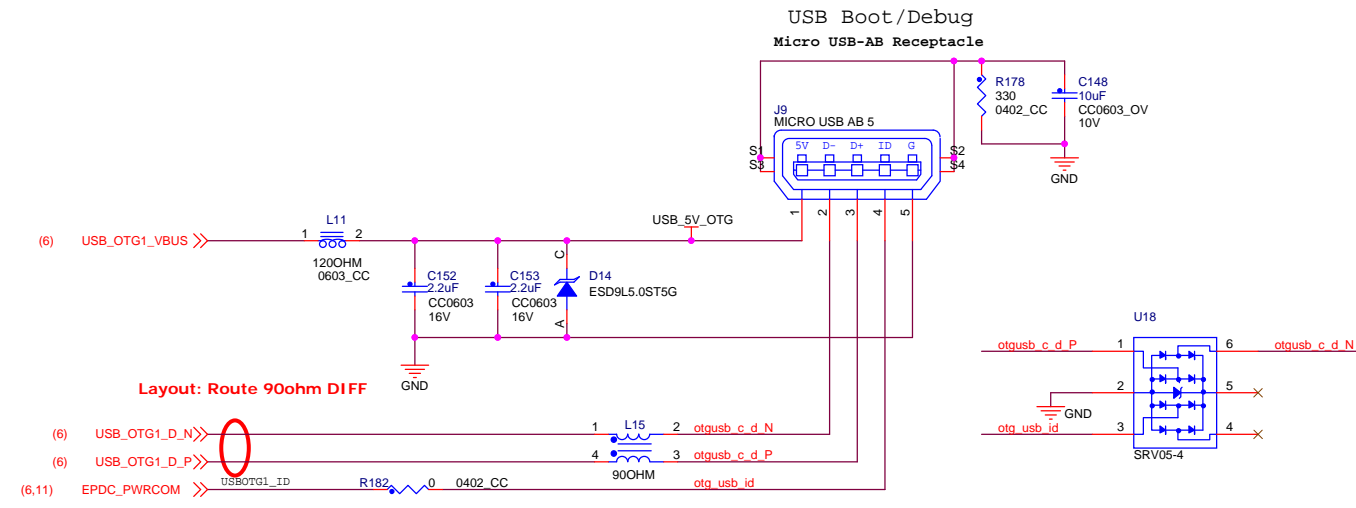
ICAP Classification: FCP: _____ FIUC: X PUBI: _____
 Drawing Title: **MCIMX6SLEVK board**
 Page Title: **EMMC, SD and SPI NOR**

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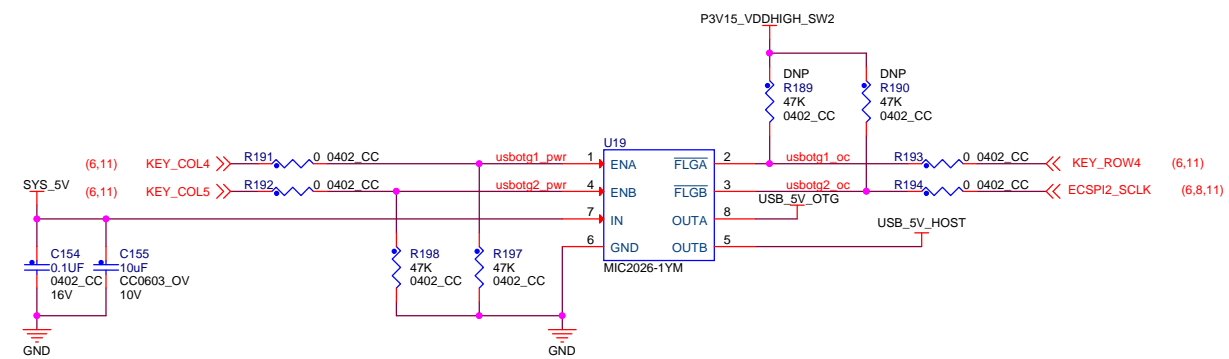
USB Host Port



USB Boot/Host/Device Port

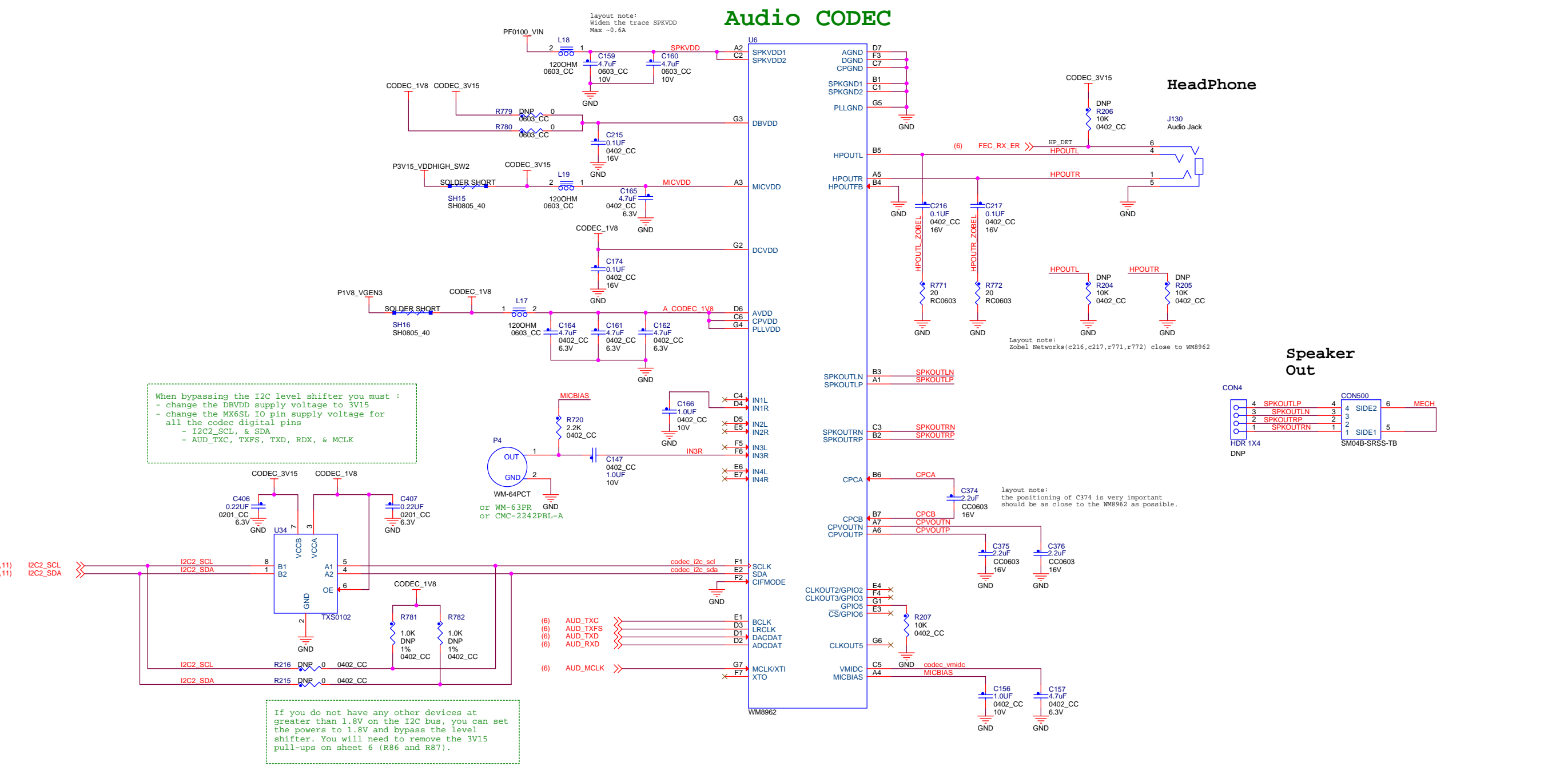


USB 5V Control



Audio CODEC

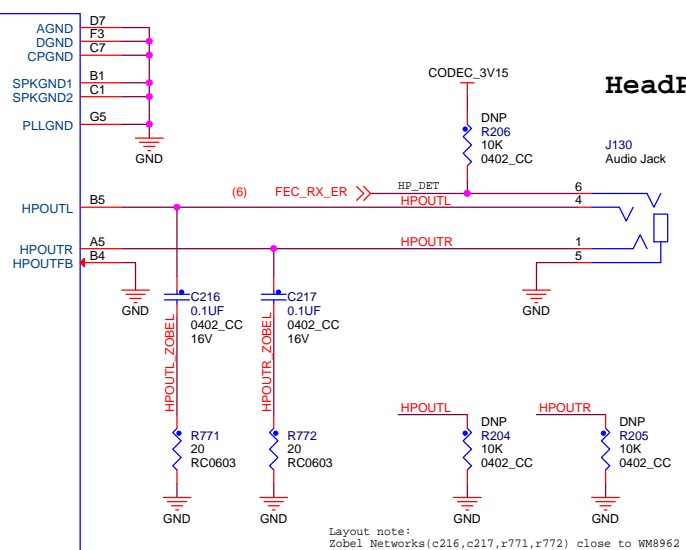
layout note:
Widen the trace SPKVDD
Max -0.6A



When bypassing the I2C level shifter you must :
 - change the DBVDD supply voltage to 3V15
 - change the MX6SL IO pin supply voltage for all the codec digital pins
 - I2C2_SCL, & SDA
 - AUD_TXC, TXFS, TXD, RDX, & MCLK

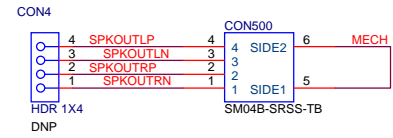
If you do not have any other devices at greater than 1.8V on the I2C bus, you can set the powers to 1.8V and bypass the level shifter. You will need to remove the 3V15 pull-ups on sheet 6 (R86 and R87).

HeadPhone



Layout note:
Zobel Networks(c216,c217,r771,r772) close to WM8962

Speaker Out



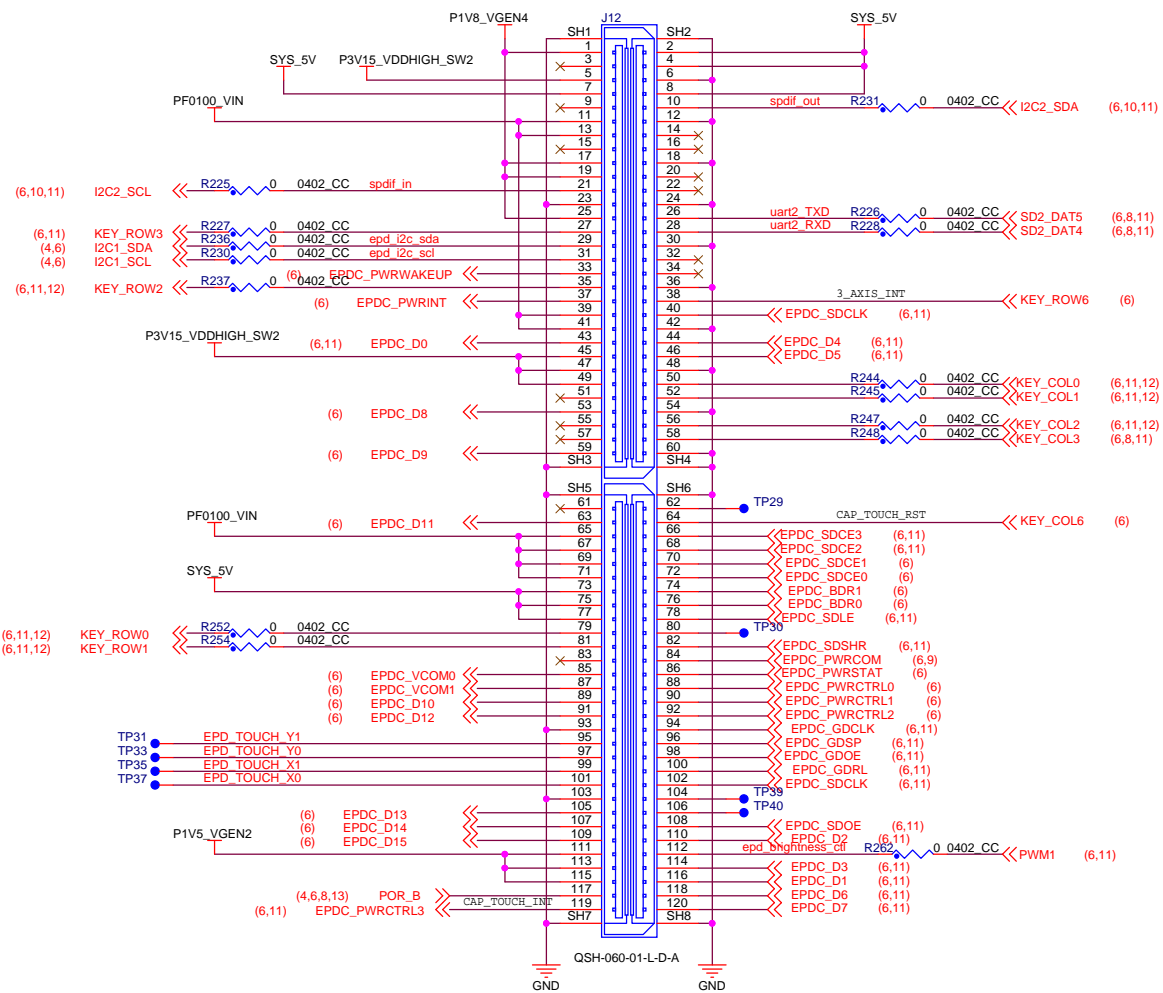
Layout note:
the positioning of C374 is very important should be as close to the WM8962 as possible.

freescale

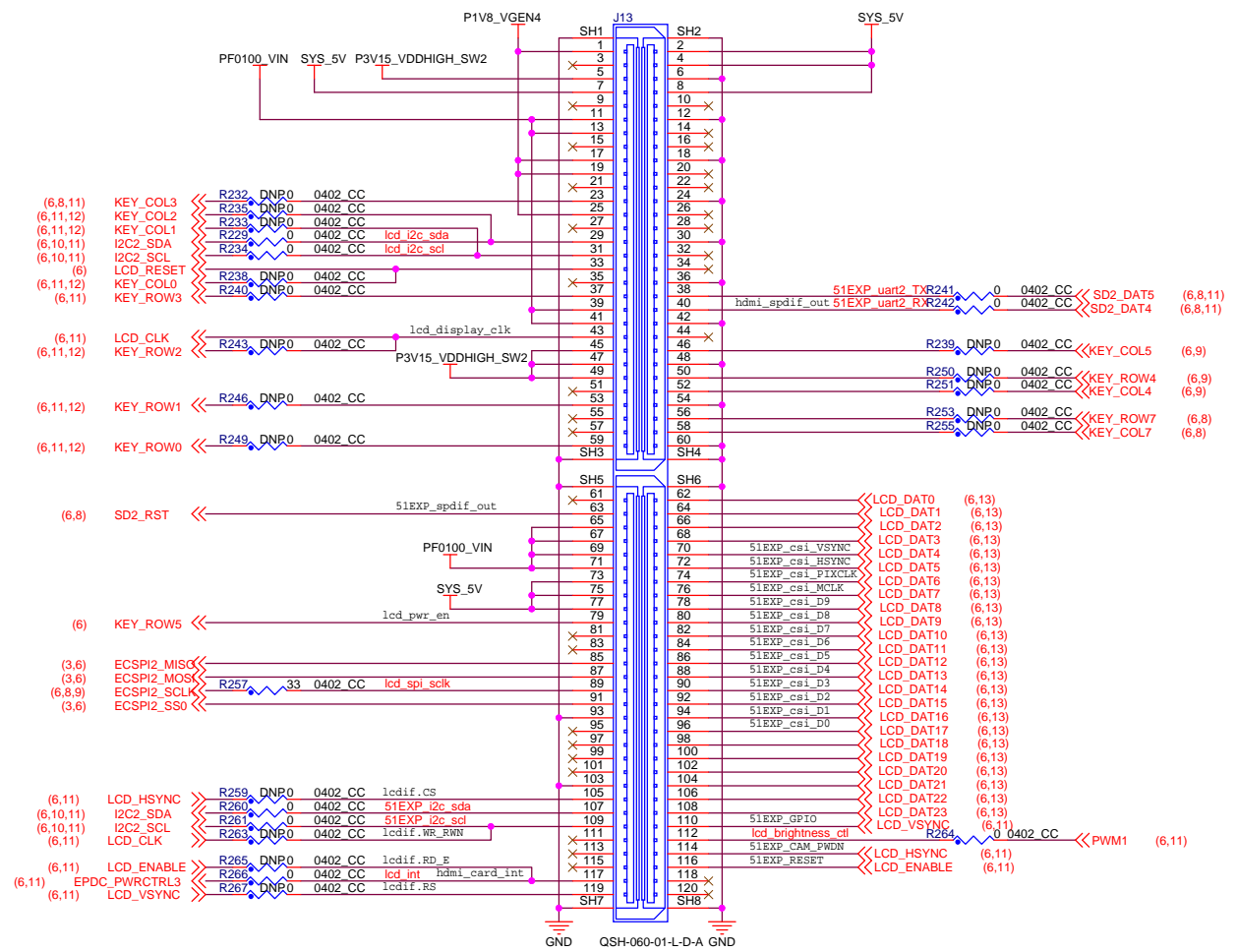
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 Drawing Title: **MCIMX6SLEVK board**
 Page Title: **Audio**

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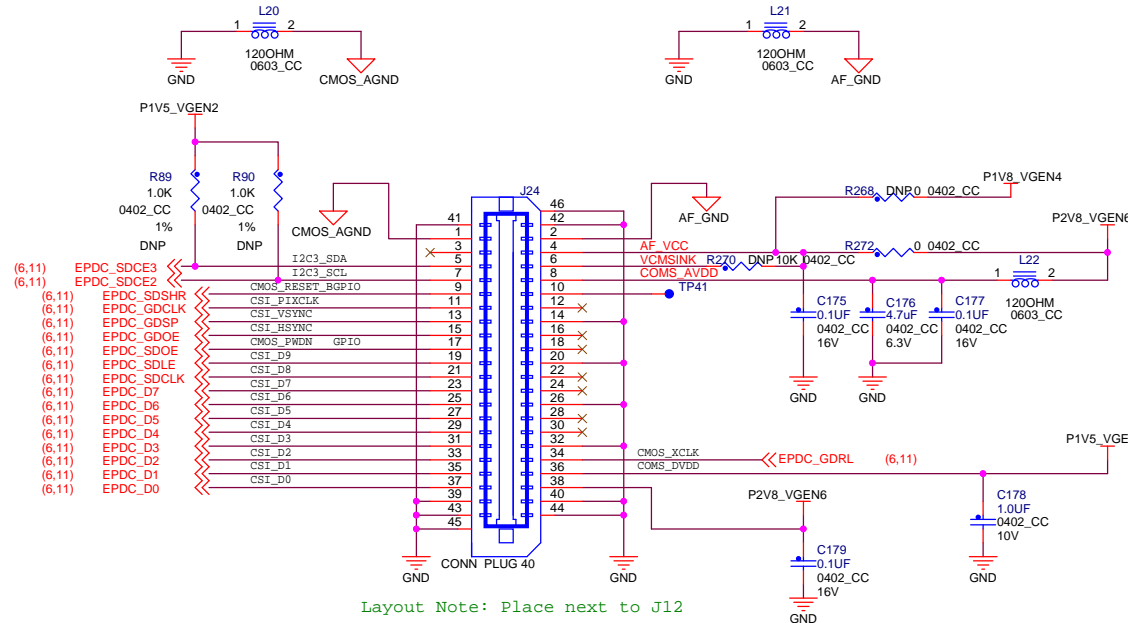
EPDC Expansion Port



LCD Expansion Port



Camera Expansion Connector



Layout Note: Place next to J12
 Use Omnivision OV5642 5M Pixel Sensor with this connector (not included)

Important Note:

The camera connector (J24) and the EPDC connector (J12) share the same signals and CANNOT be used at the same time.

One of these two peripherals MUST BE REMOVED when a developer wishes to use the other.

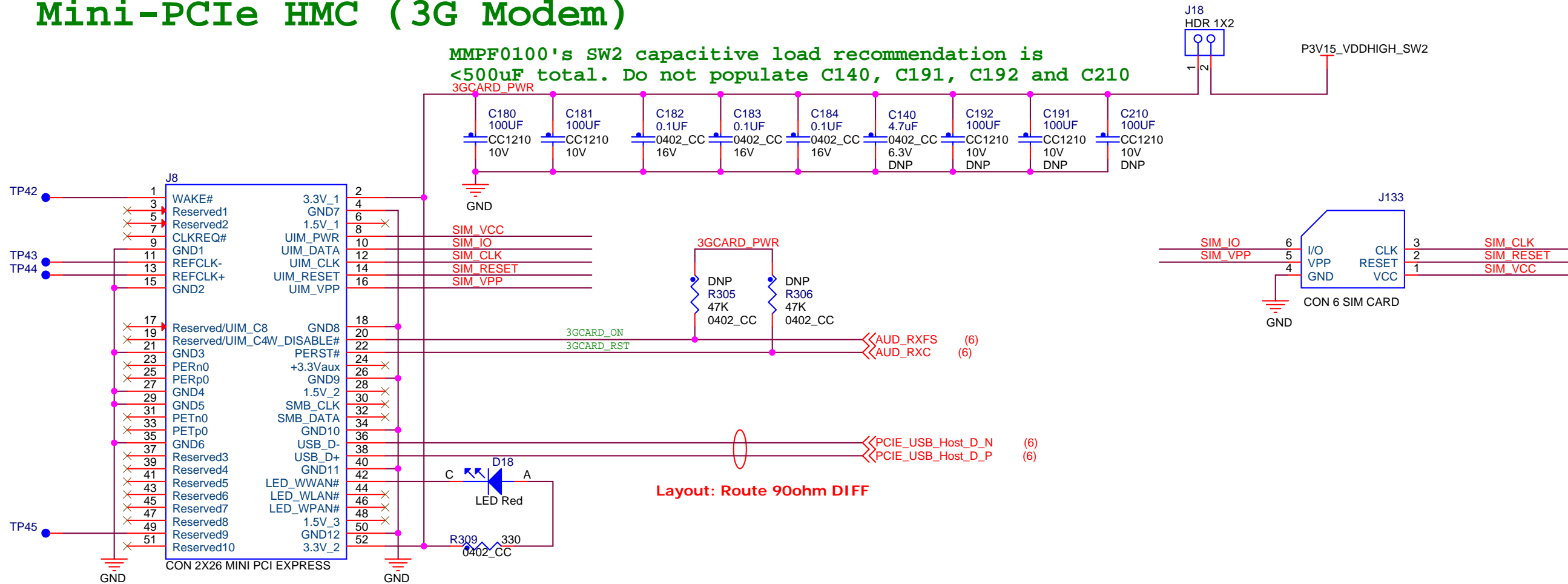
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ICAP Classification: FCP: _____ FIUC: X PUBI: _____
 Drawing Title: **MCIMX6SLEVK board**
 Page Title: **Video**

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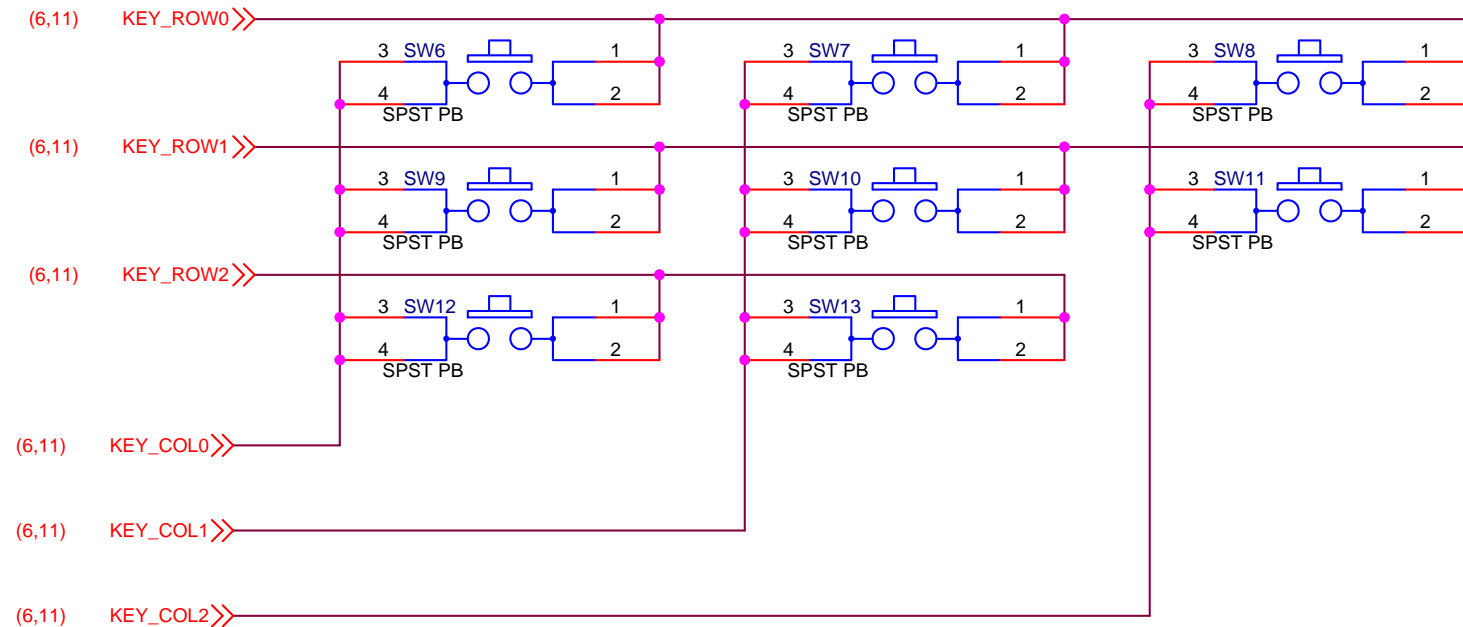
Mini-PCIE HMC (3G Modem)

MMPF0100's SW2 capacitive load recommendation is <500uF total. Do not populate C140, C191, C192 and C210



Layout: Route 90ohm DIFF

Button Matrix



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Drawing Title: **MCIMX6SLEVK board**

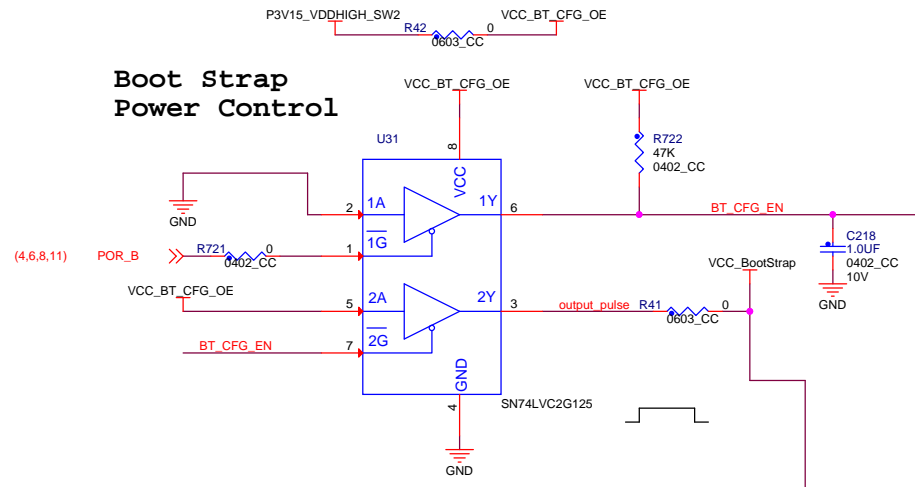
Page Title: **Wireless**

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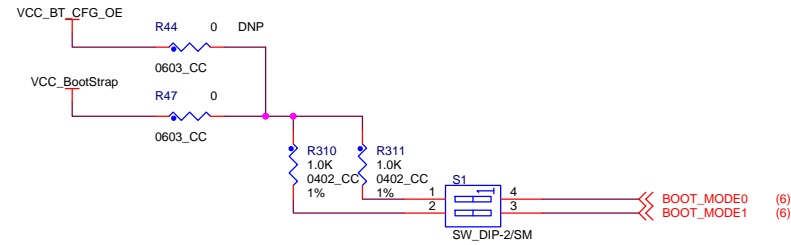
Boot Strap

Boot Strap Power Control

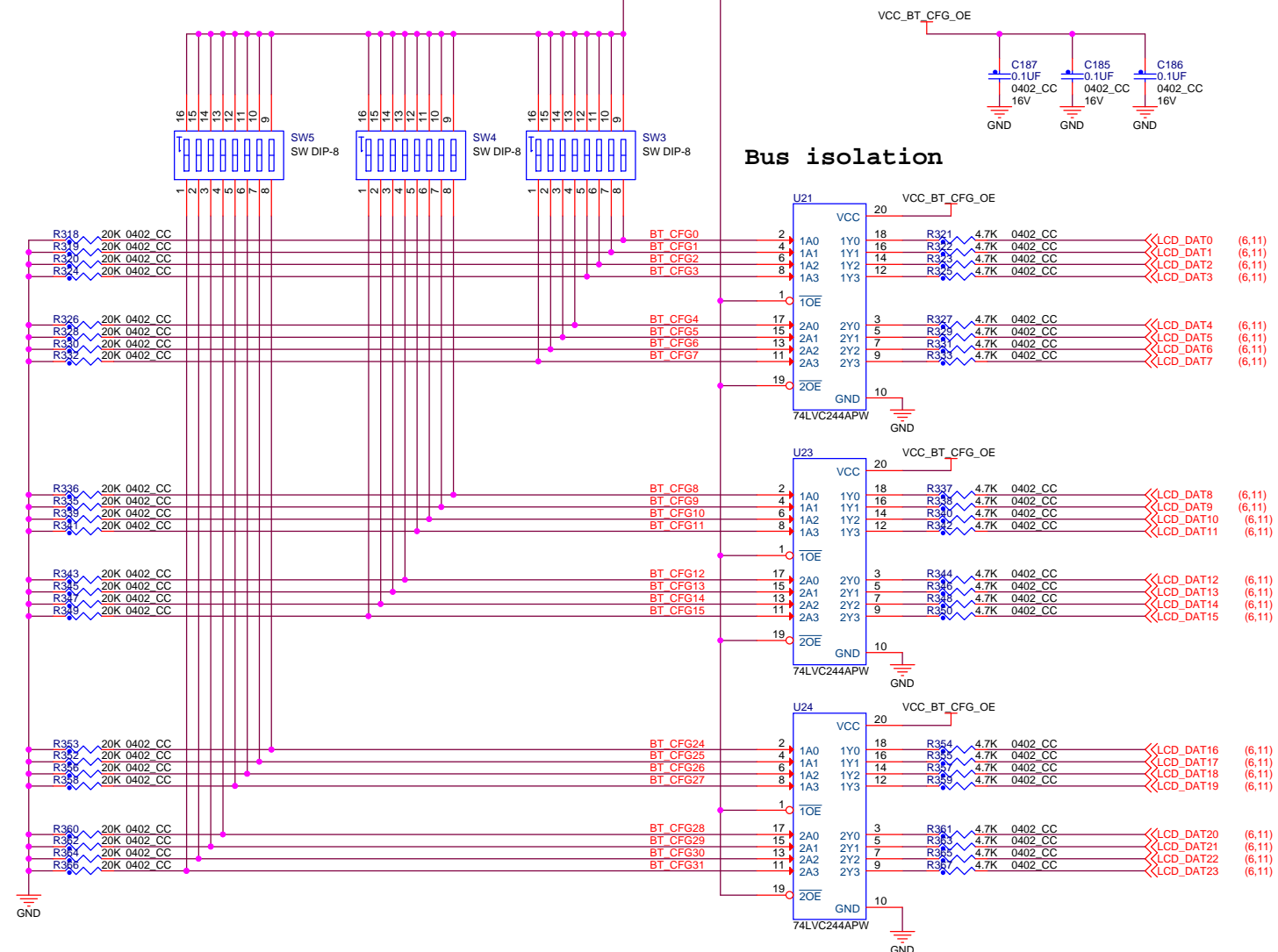


Note:
i.MX6SL reads values approximately 300us to 1ms after reset released. Buffers are active while unit is in reset and lms-10ms after reset is released.

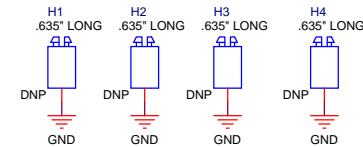
Boot Strap Primary Switches



Bus isolation

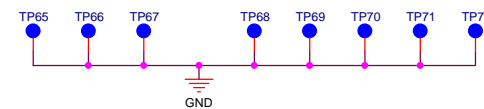


Board Mounting Holes for 4-40 Screws



IMPORTANT NOTE :
Use non metallic or non conducting standoff to avoid board damage due to GND potential difference with chassis.

GND TEST POINTS



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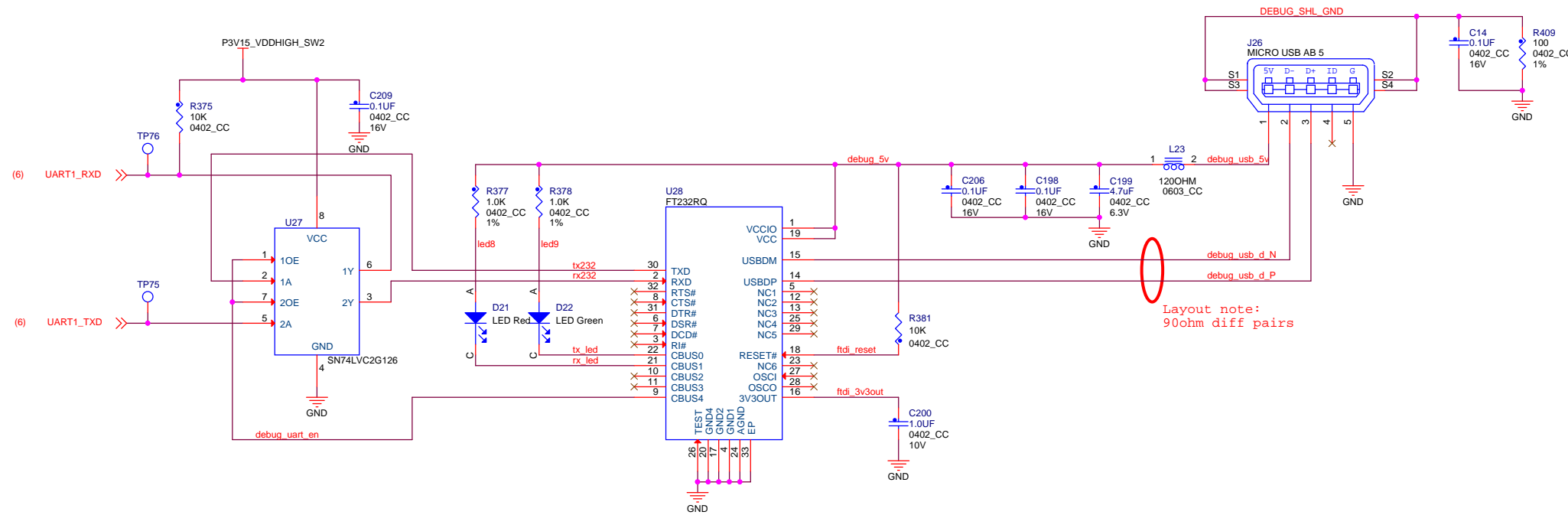
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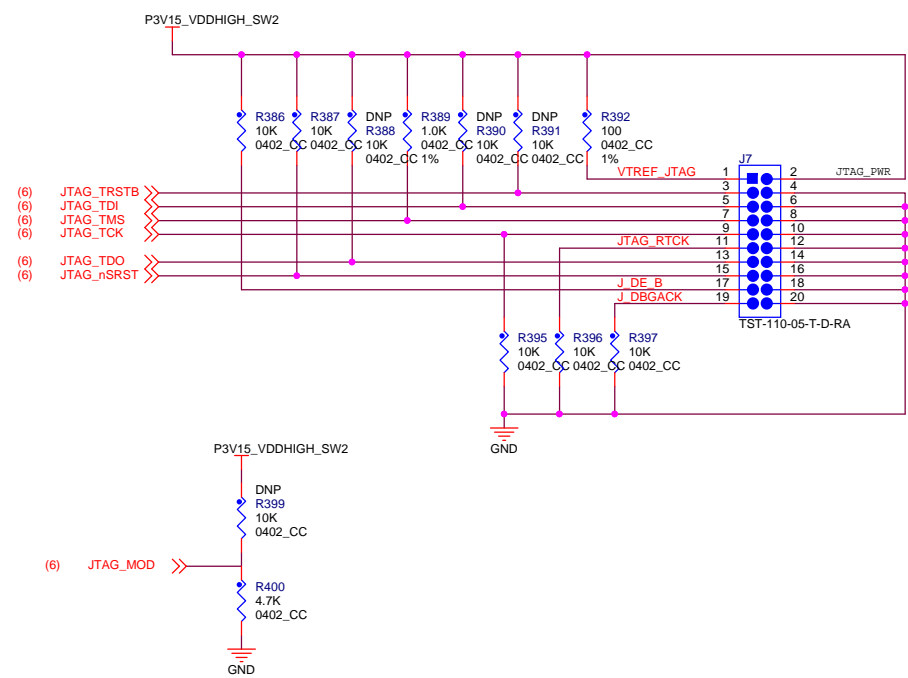
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Debug UART2USB Converter

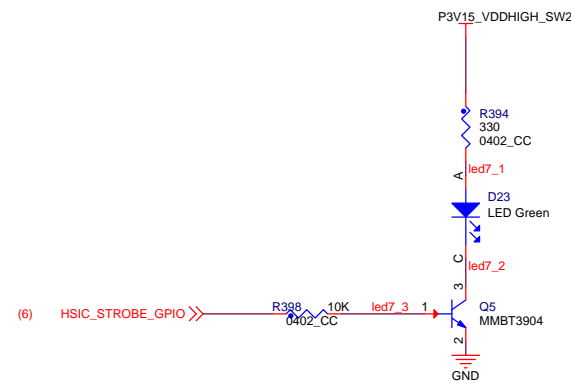


For driver installation, please refer to <http://www.ftdichip.com/Documents/InstallGuides.htm>

JTAG



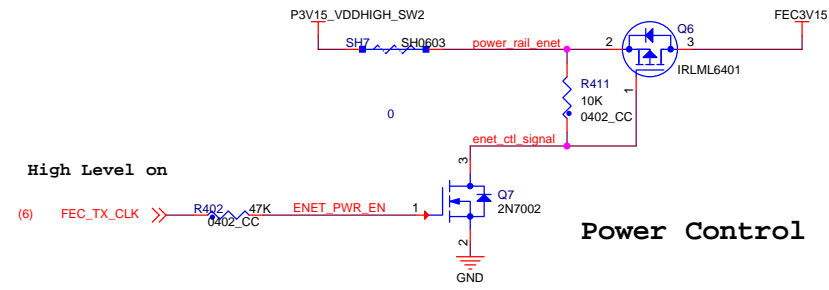
Debug LED



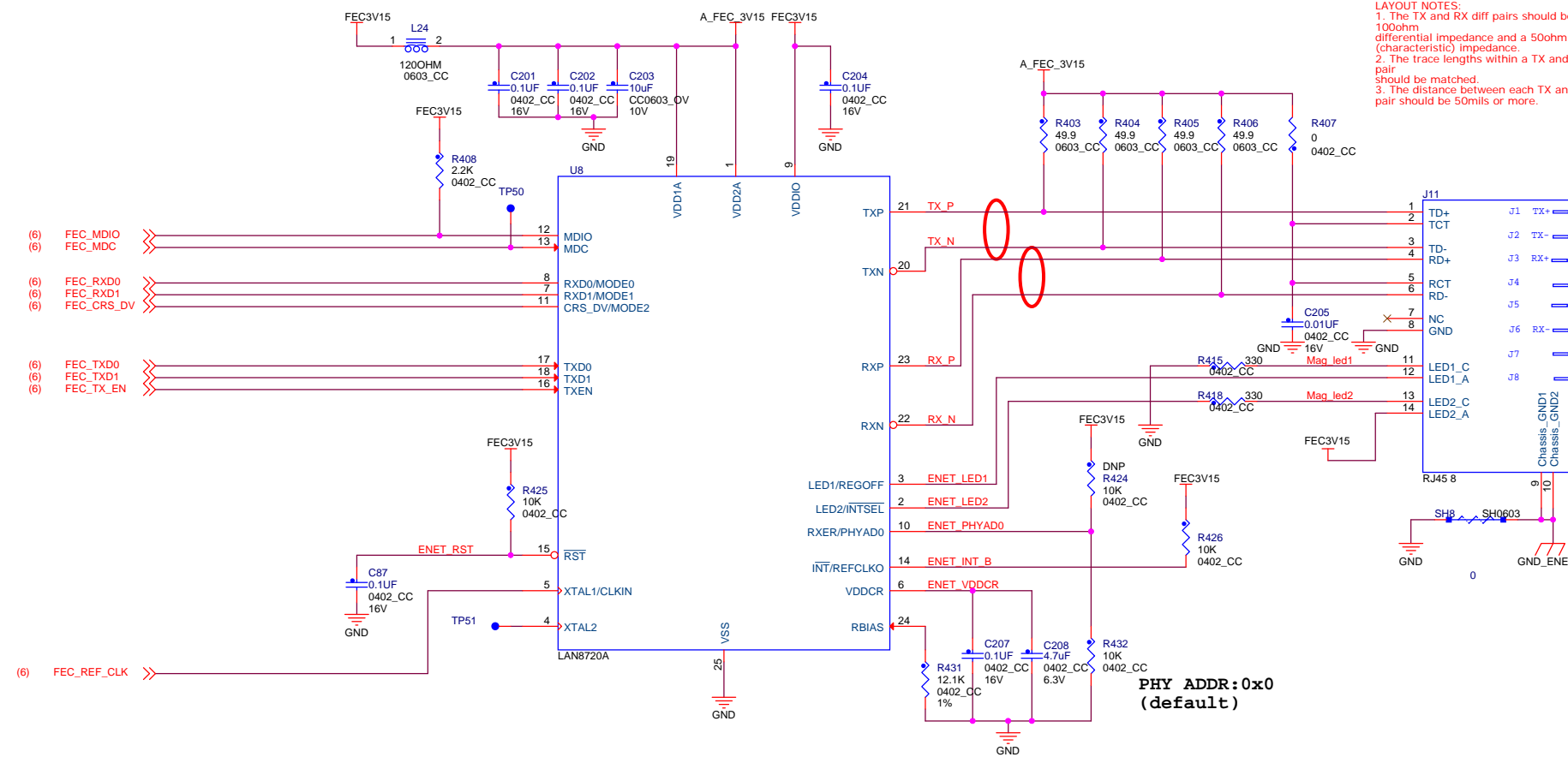
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 Page Title: **UART & JTAG**

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Ethernet



IOMUX Table

Table with 7 columns (PIN NAME, ALT0 to ALT7) listing various IOMUX pins and their alternate functions across different configurations. Pins include WDOG_B, HSDC_DAT, REF_CLK_24M, and many others, with functions ranging from WDOG1_WDOG_B to various peripheral controls.

