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Specification

MCCOG42005A6W-BNMLWI

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1. Revision History

DATE	VERSION	REVISED PAGE NO.	Note
2011/12/12	1		First issue

2. General Specification

The Features of the Module is description as follow:

- Module dimension: 74.3x 36.4 x 6.0 (max.) mm^3
- View area: 60.5 x 22.18 mm^2
- Active area: 58.5 x 20.18 mm^2
- Dot size: 0.45 x0.54 mm2
- Dot pitch: 0.5 x 0.59 mm2
- Character size: 2.45 x 4.67
- Character pitch: 2.95 x 5.17
- LCD type: STN Negative, Blue Transmissive,
- Duty: 1/33DUTY,1/6BIAS
- View direction: 6 o'clock
- Backlight Type: LED White

MIDAS DISPLAYS

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Midas LCD Part Number System

MC	COG	132033	A	*	6	W	*	*	-	S	N	T	L	W	*	*
1	2	3	4	5	6	7	8	9	-	10	11	12	13	14	15	16

1 = **MC:** Midas Components

2 = **Blank:** COB (chip on board) **COG**: chip on glass

3 = **No of dots** (e.g. 240064 = 240 x 64 dots) (e.g. 21605 = 2 x 16 5mm C.H.)

4 = **Series**

5 = **Series Variant:** A to Z – **see addendum**

6 = **3:** 3 o'clock **6:** 6 o'clock **9**: 9 o'clock **12**: 12 o'clock

7 = S: Normal (0 to + 50 deg C) **W:** Wide temp. (-20 to + 70 deg C) **X:** Extended temp (-30 + 80 Deg C)

8 = **Character Set**

Blank: Standard (English/Japanese)
C: Chinese Simplified (Graphic Displays only)
CB: Chinese Big 5 (Graphic Displays only)
H: Hebrew
K: European (std) (English/German/French/Greek)
L: English/Japanese (special)
M: European (English/Scandinavian)
R: Cyrillic
W: European (English/Greek)
U: European (English/Scandinavian/Icelandic)

9 = **Bezel Height** (where applicable / available)

	Top of Bezel to Top of PCB	Common (via pins 1 and 2)	Array or Edge Lit
Blank	9.5mm / not applicable	Common	Array
2	8.9 mm	Common	Array
3	7.8 mm	Separate	Array
4	7.8 mm	Common	Array
5	9.5 mm	Separate	Array
6	7 mm	Common	Array
7	7 mm	Separate	Array
8	6.4 mm	Common	Edge
9	6.4 mm	Separate	Edge
A	5.5 mm	Common	Edge
B	5.5 mm	Separate	Edge
D	6.0mm	Separate	Edge
E	5.0mm	Separate	Edge
F	4.7mm	Common	Edge
G	3.7mm	Separate	EL

10 = **T:** TN S: STN **B:** STN Blue **G:** STN Grey **F:** FSTN **F2:** FFSTN

11 = **P:** Positive **N**: Negative

12 = **R:** Reflective **M**: Transmissive **T:** Transflective

13 = **Backlight: Blank:** Reflective **L:** LED

14 = **Backlight Colour: Y:** Yellow-Green **W:** White **B:** Blue **R:** Red **A:** Amber **O:** Orange **G:** Green **RGB:** R.G.B.

15 = **Driver Chip: Blank:** Standard **I:** I²C **T:** Toshiba T6963C **A:** Avant SAP1024B **R:** Raio RA8835

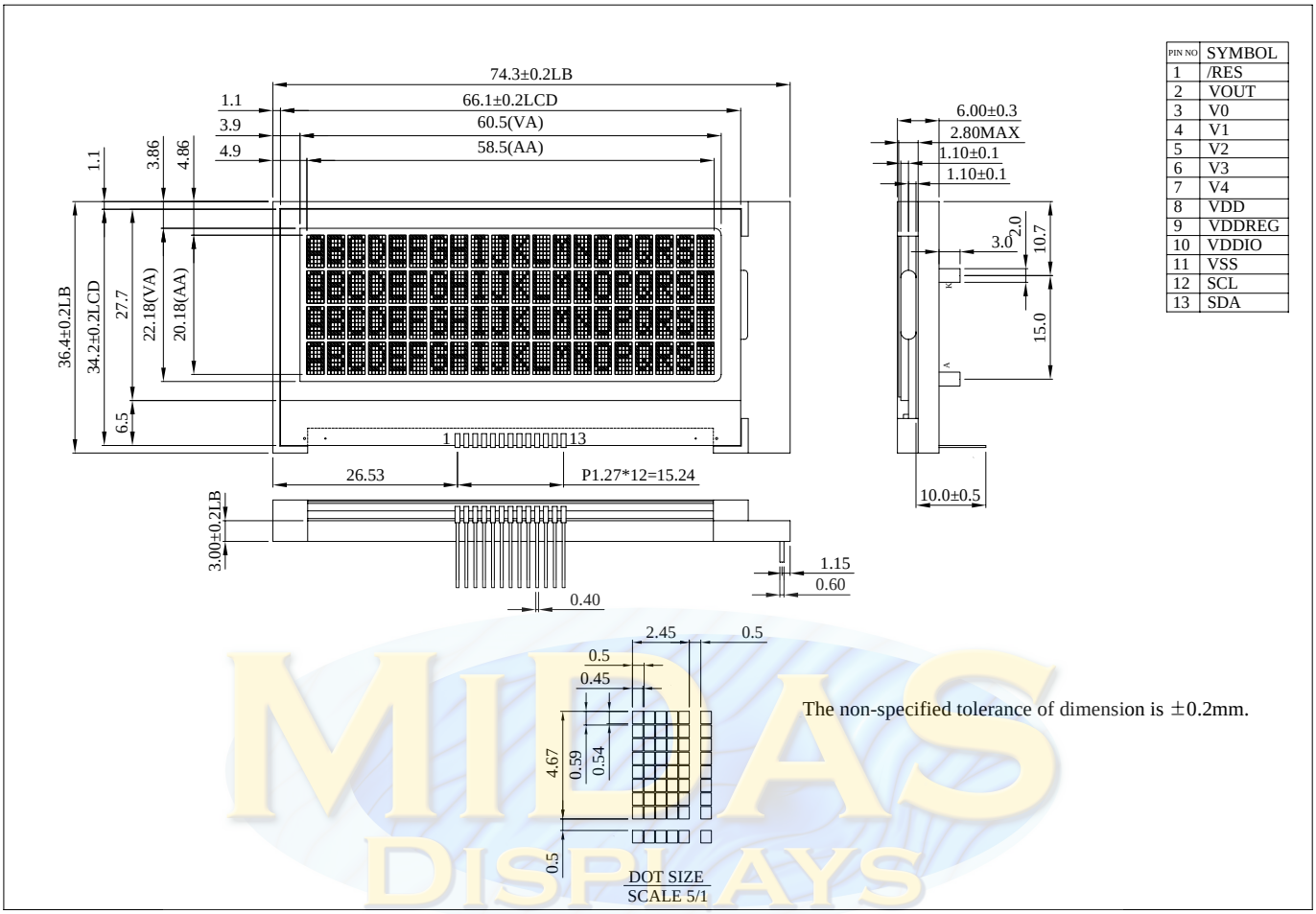
16 = **Voltage Variant**: e.g. **3** = 3v

4. Interface Pin Function

<table>
<tr><th>Pin No.</th><th>Symbol</th><th>Description</th></tr>
<tr><td>1</td><td>/RES</td><td>Reset Pin</td></tr>
<tr><td>2</td><td>VOUT</td><td>Output of the voltage converter</td></tr>
<tr><td>3</td><td>V0</td><td>Regulated voltage from voltage converter for LCD driving</td></tr>
<tr><td>4</td><td>V1</td><td rowspan="4">Bias voltage levels for LCD driving</td></tr>
<tr><td>5</td><td>V2</td></tr>
<tr><td>6</td><td>V3</td></tr>
<tr><td>7</td><td>V4</td></tr>
<tr><td>8</td><td>VDD</td><td>This pin is the power supply for logic circuit (VDD should rise within 10ms).
In 3V IO application (VDDREG pulled low), this is a power input pin.
In 5V IO application (VDDREG pulled high), this pin outputs 3V and should be connected with a capacitor to VSS.</td></tr>
<tr><td>9</td><td>VDDREG</td><td>This pin is used to enable VDD regulator in 5V I/O Application:
<table>
<tr><th>VDDREG</th><th>Mode</th></tr>
<tr><td>H</td><td>5V I/O Application</td></tr>
<tr><td>L</td><td>Low Voltage I/O Application</td></tr>
</table></td></tr>
<tr><td>10</td><td>VDDIO</td><td>This pin is the power supply for bus IO buffer in both Low Voltage I/O and 5V I/O application.</td></tr>
<tr><td>11</td><td>VSS</td><td>Ground</td></tr>
<tr><td>12</td><td>SCL</td><td>This pin is used as clock input pin in I2C mode.</td></tr>
<tr><td>13</td><td>SDA</td><td>This pin is used as data/ acknowledge response output pin in I2C mode.</td></tr>
</table>

MIDAS DISPLAYS

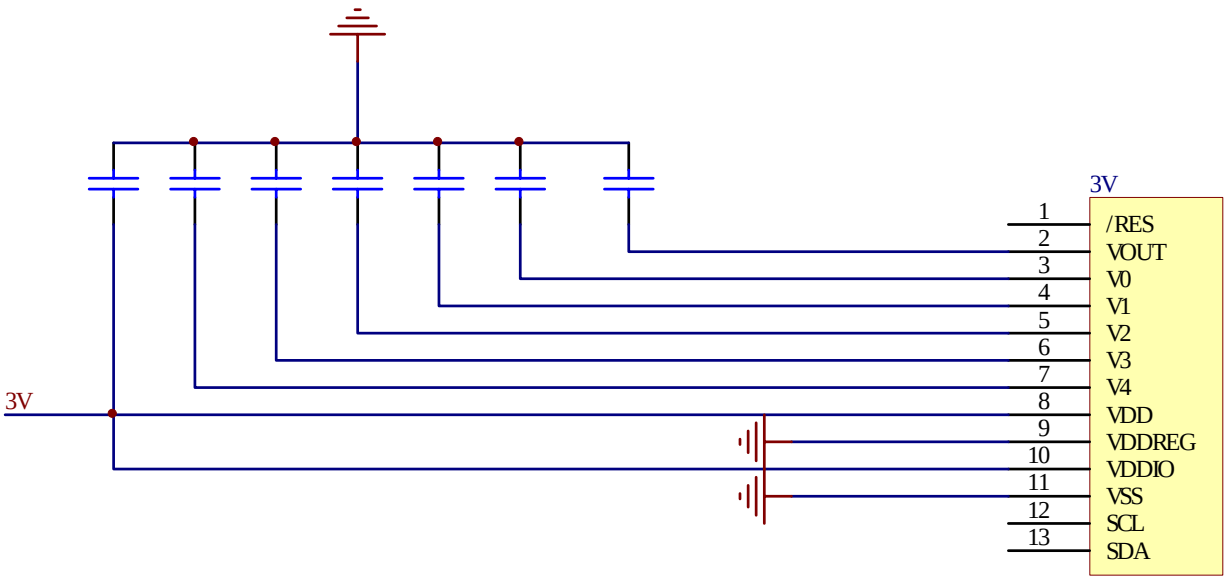
5. Outline Dimension & Block Diagram



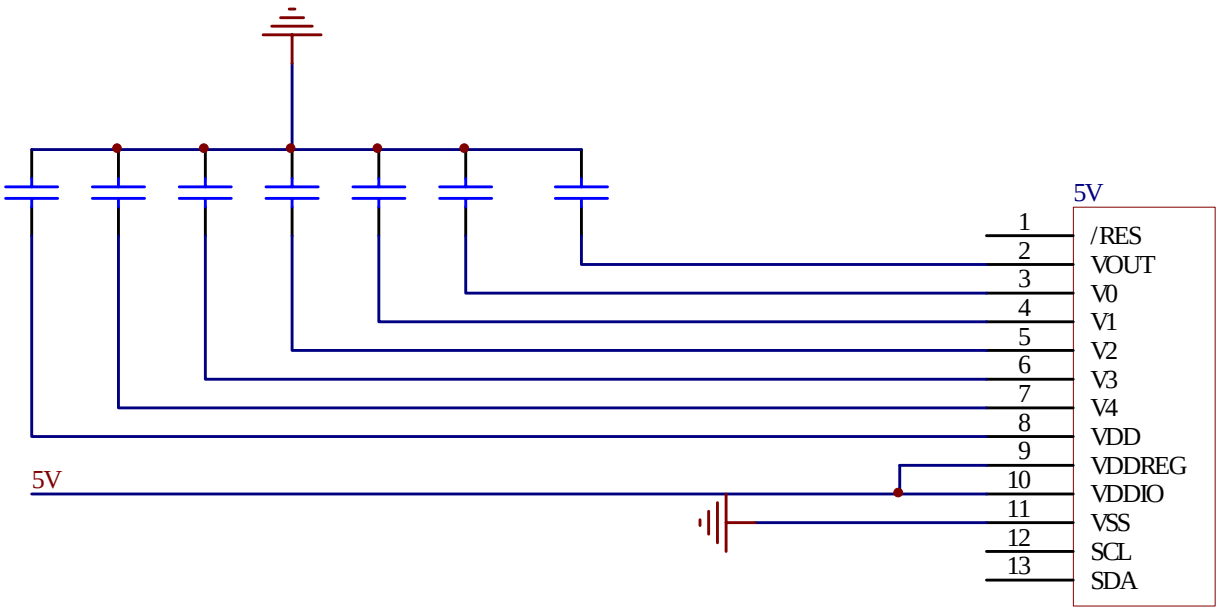
PIN NO	SYMBOL
1	/RES
2	VOUT
3	V0
4	V1
5	V2
6	V3
7	V4
8	VDD
9	VDDREG
10	VDDIO
11	VSS
12	SCL
13	SDA

5.1 APPLICATION EXAMPLES

1.Application Example I (I2C interface, 3V VDDIO mode)



2.Application Example II (I2C interface, 5V IO mode)



Capacitance =1μF

MIDAS DISPLAYS

6.Function Block Descriptions

6.1 Busy Flag (BF)

When BF = "High", it indicates that the internal operation is being processed. So during this time the next instruction cannot be accepted. BF can be read, when RS = Low and R/W = High (Read Instruction Operation), through DB7. Before executing the next instruction, be sure that BF is not high.

6.2 Display Data Ram (DDRAM)

DDRAM stores display data of maximum 80 x 8 bits (80 characters). DDRAM address is set in the address counter (AC) as a hexadecimal number. (Refer to Figure 9-1)

Figure 6-1: DDRAM Address

MSB						LSB
AC6	AC5	AC4	AC3	AC2	AC1	AC0

Display of 5-Dot Font Width Character

5-dot 4-line Display

In case of 4-line display with 5-dot font, the address range of DDARM is 00H-13H, 20H-33H, 40H-53H, 60H-73H (refer to Figure 9-5).

Figure 6-2: 4-line x 20ch. Display (5-dot Font Width)

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	
COM1 COM8	00	01	02	03	04	05	06	07	08	09	0A	0B	0C	0D	0E	0F	10	11	12	13	← Disp DDR
COM9 COM16	20	21	22	23	24	25	26	27	28	29	2A	2B	2C	2D	2E	2F	30	31	32	33	
COM17 COM24	40	41	42	43	44	45	46	47	48	49	4A	4B	4C	4D	4E	4F	50	51	52	53	
COM25 COM32	60	61	62	63	64	65	66	67	68	69	6A	6B	6C	6D	6E	6F	70	71	72	73	
	SEG1																			SEG100	

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20
COM1 COM8	01	02	03	04	05	06	07	08	09	0A	0B	0C	0D	0E	0F	10	11	12	13	00
COM9 COM16	21	22	23	24	25	26	27	28	29	2A	2B	2C	2D	2E	2F	30	31	32	33	20
COM17 COM24	41	42	43	44	45	46	47	48	49	4A	4B	4C	4D	4E	4F	50	51	52	53	40
COM25 COM32	61	62	63	64	65	66	67	68	69	6A	6B	6C	6D	6E	6F	70	71	72	73	60

(After Shift Left)

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20
COM1 COM8	13	00	01	02	03	04	05	06	07	08	09	0A	0B	0C	0D	0E	0F	10	11	12
COM9 COM16	33	20	21	22	23	24	25	26	27	28	29	2A	2B	2C	2D	2E	2F	30	31	32
COM17 COM24	53	40	41	42	43	44	45	46	47	48	49	4A	4B	4C	4D	4E	4F	50	51	52
COM25 COM32	73	60	61	62	63	64	65	66	67	68	69	6A	6B	6C	6D	6E	6F	70	71	72

(After Shift Right)

6.3 Timing Generation Circuit

Timing generation circuit generates clock signals for the internal operations.

6.4 Address Counter (AC)

Address Counter (AC) stores DDRAM/ CGRAM/ SEGRAM address, transferred from Instruction Register (IR). After writing into (reading from) DDRAM/ CGRAM/ SEGRAM, AC is automatically increased (decreased) by 1. In parallel and serial mode, when RS = "Low" and R/W = "High", AC can be read through DB0-DB6.

6.5 Cursor/Blink Control Circuit

It controls cursor/blink ON/OFF and black/white inversion at cursor position.

6.6 LCD Driver Circuit

LCD Driver circuit has 34 common and 100 segment signals for LCD driving. Data from SEGRAM/ CGRAM/ CGROM is transferred to 100-bit segment latch serially, and then it is stored to 100-bit shift latch. When each com is selected by 34-bit common register, segment data also output through segment driver from 100-bit segment latch. In case of 1-line display mode, ICON1/ICON2 and COM1-COM8 have 1/9 duty ratio; and in 4-line mode, ICON1/ICON2 and COM1-COM32 have 1/33 duty ratio.

6.7 CGROM (Character Generator ROM)

There is 3 optional CGROMs in SSD1803A in P.66-68 , which is selected by ROM1 and ROM2 pins. CGROM has 5 x 8 dots 256 Character Pattern.

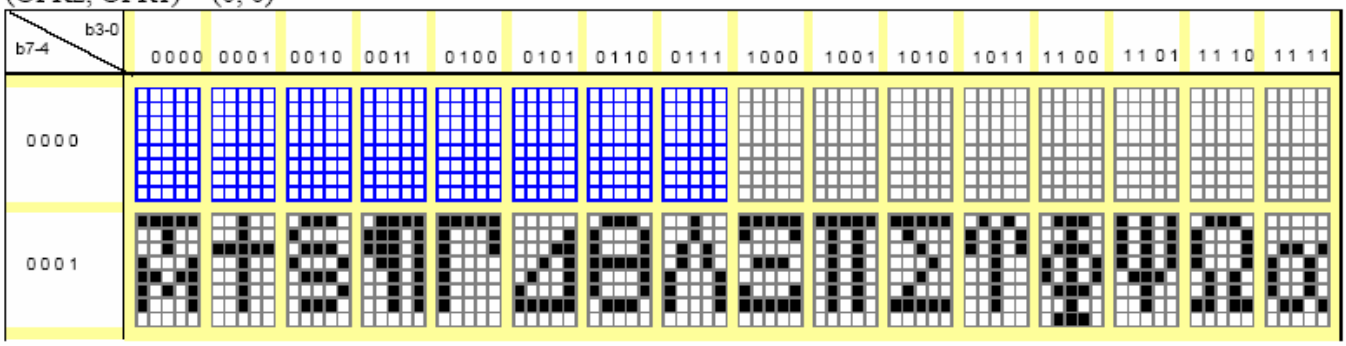
6.8 CGRAM (Character Generator RAM)

CGRAM has up to 8 characters of 5 x 8 dots, selectable by OPR2 and OPR1 pins (refer to Table 6-1).

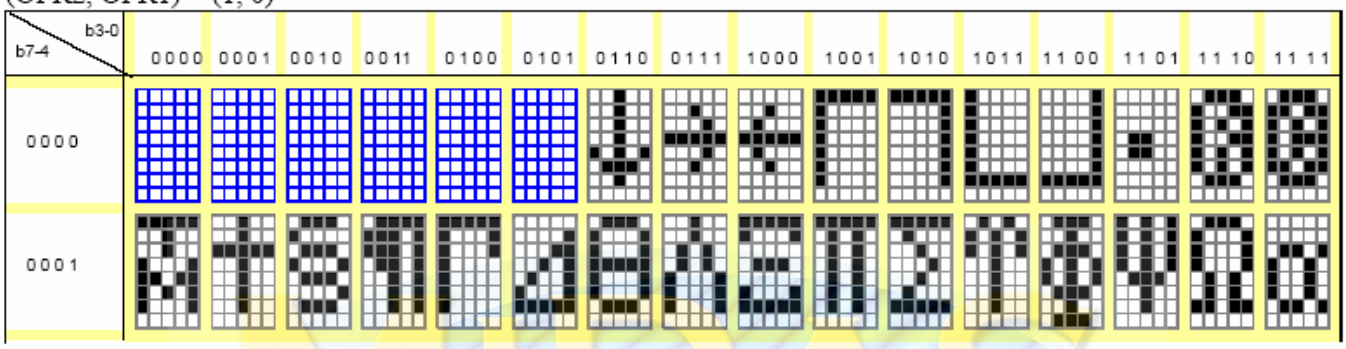
MIDAS DISPLAYS

Table 6-1: CGRAM and CGROM arrangement with

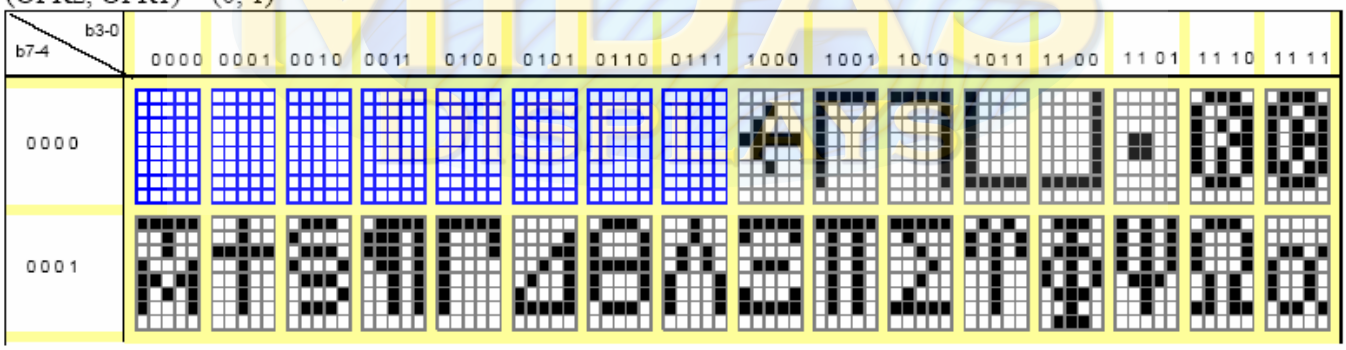
(OPR2, OPR1) = (0, 0)



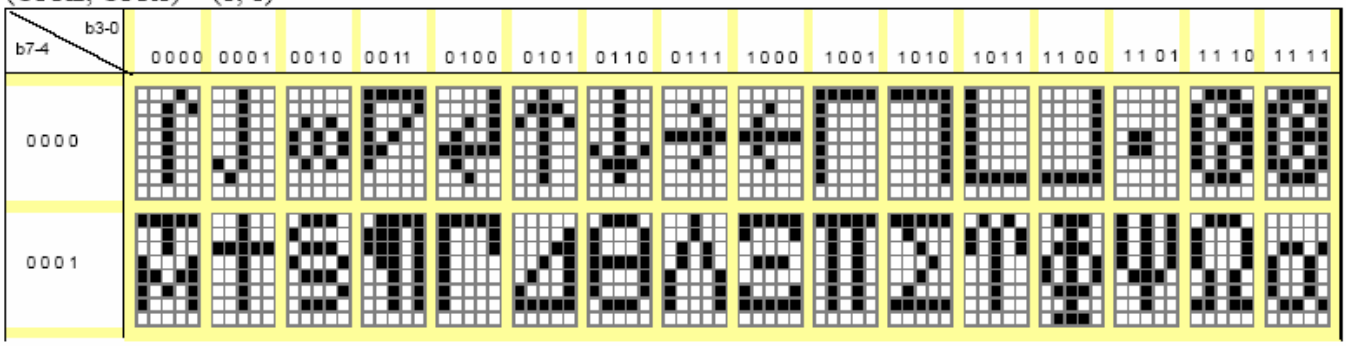
(OPR2, OPR1) = (1, 0)



(OPR2, OPR1) = (0, 1)



(OPR2, OPR1) = (1, 1)



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By writing font data to CGRAM, user defined character can be used (refer to Table 6-2).

Table 6-2: Relationship between Character Code (DDRAM) and Character Pattern (CGRAM)

5x8 dots Character Pattern

Character Code (DDRAM Data)								CGRAM Address						CGRAM Daata								Pattern Number
D7	D6	D5	D4	D3	D2	D1	D0	A5	A4	A3	A2	A1	A0	P7	P6	P5	P4	P3	P2	P1	P0	
0	0	0	0	x	0	0	0	0	0	0	0	0	0	B1	B0	x	0	1	1	1	0	Pattern1
											0	0	1				1	0	0	0	1	
				.							0	1	0				1	0	0	0	1	
				.					.		0	1	1		.		1	1	1	1	1	
				.					.		1	0	0		.		1	0	0	0	1	
				.					.		1	0	1		.		1	0	0	0	1	
											1	1	0		.		1	0	0	0	1	
											1	1	1				0	0	0	0	0	
				.					.			.						.				.
				.					.			.						.				.
0	0	0	0	x	1	1	1	1	1	1	0	0	0	B1	B0	x	1	0	0	0	1	Pattern8
											0	0	1				1	0	0	0	1	
				.					.		0	1	0		.		1	0	0	0	1	
				.					.		0	1	1		.		1	1	1	1	1	
				.					.		1	0	0		.		1	0	0	0	1	
				.					.		1	0	1		.		1	0	0	0	1	
											1	1	0				1	0	0	0	1	
											1	1	1				0	0	0	0	0	

6.9 SEGRAM (Segment Icon RAM)

SEGRAM has segment control data and segment pattern data. During display mode, ICON1 (ICON2) makes the data of SEGRAM enable to display icons. Its higher 2-bit are blinking control data, and lower 6-bits are pattern data (refer to Table 6-3 and Figure 6-3).

Table 6-3: Relationship between SEGRAM Address and Display Pattern

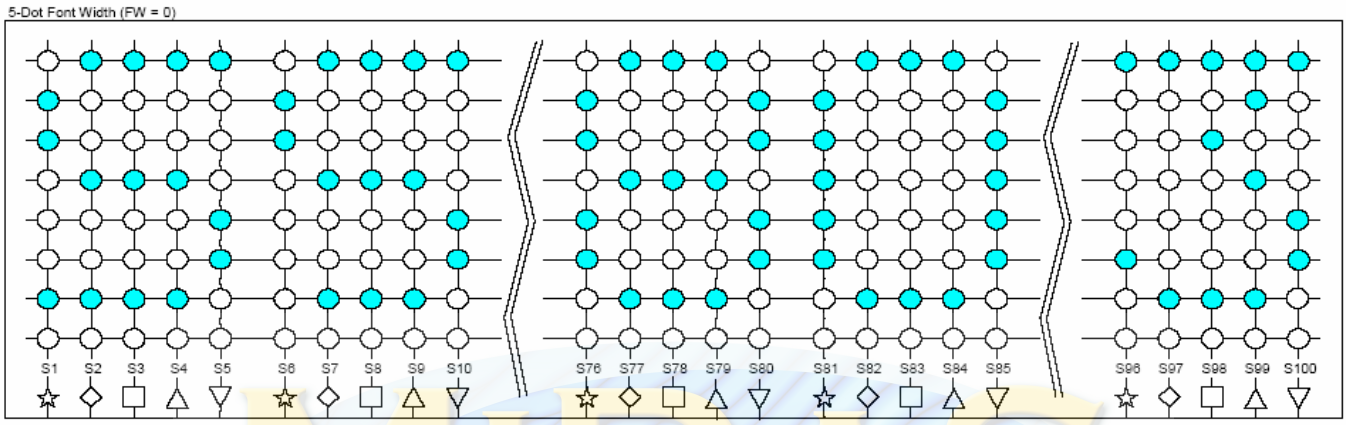
SEGRAM Address				SEGRAM Data Display Pattern															
				5-dot Font Width								6-dot Font Width							
A3	A2	A1	A0	D7	D6	D5	D4	D3	D2	D1	D0	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	B1	B0	X	S1	S2	S3	S4	S5	B1	B0	S1	S2	S3	S4	S5	S6
0	0	0	1	B1	B0	X	S6	S7	S8	S9	S10	B1	B0	S7	S8	S9	S10	S11	S12
0	0	1	0	B1	B0	X	S11	S12	S13	S14	S15	B1	B0	S13	S14	S15	S16	S17	S18
0	0	1	1	B1	B0	X	S16	S17	S18	S19	S20	B1	B0	S19	S20	S21	S22	S23	S24
0	1	0	0	B1	B0	X	S21	S22	S23	S24	S25	B1	B0	S25	S26	S27	S28	S29	S30
0	1	0	1	B1	B0	X	S26	S27	S28	S29	S30	B1	B0	S31	S32	S33	S34	S35	S36
0	1	1	0	B1	B0	X	S31	S32	S33	S34	S35	B1	B0	S37	S38	S39	S40	S41	S42
0	1	1	1	B1	B0	X	S36	S37	S38	S39	S40	B1	B0	S43	S44	S45	S46	S47	S48
1	0	0	0	B1	B0	X	S41	S42	S43	S44	S45	B1	B0	S49	S50	S51	S52	S53	S54
1	0	0	1	B1	B0	X	S46	S47	S48	S49	S50	B1	B0	S55	S56	S57	S58	S59	S60
1	0	1	0	B1	B0	X	S51	S52	S53	S54	S55	B1	B0	S61	S62	S63	S64	S65	S66
1	0	1	1	B1	B0	X	S56	S57	S58	S59	S60	B1	B0	S67	S68	S69	S70	S71	S72
1	1	0	0	B1	B0	X	S61	S62	S62	S64	S65	B1	B0	S73	S74	S75	S76	S77	S78
1	1	0	1	B1	B0	X	S66	S67	S68	S69	S70	B1	B0	S79	S80	S81	S82	S83	S84
1	1	1	0	B1	B0	X	S71	S72	S73	S74	S75	B1	B0	S85	S86	S87	S88	S89	S90
1	1	1	1	B1	B0	X	S76	S77	S78	S79	S80	B1	B0	S91	S92	S93	S94	S95	S96

1. B1, B0: Blinking control bit

Control Bit	Blinking Port	
BE B1 B0	5-dot font width	6-dot font width
0 X X	No blink	No blink
1 0 0	No blink	No blink
1 0 1	D4	D5
1 1 X	D4 - D0	D5 - D0

1. S1-S80 : Icon pattern ON/OFF in 5-dot font width
   S1-S96 : Icon pattern ON/OFF in 6-dot font width
2. "X": Don't care.

Figure 6-3 Relationship between SEGRAM and Segment Display



MIDAS DISPLAYS

6.10 System Interface

This chip has all four kinds of interface type with MPU: I2C, serial, 4-bit bus and 8-bit bus. I2C, Serial and bus (4-bit/8-bit) is selected by IM1 and IM2 inputs, and 4-bit bus and 8-bit bus is selected
by DL bit in the instruction register.

6.10.1 I2C interface

SSD1803A supports I2C interface with a bit rate up to 400 kbits/s. It enables write/ read data or busy flag and supports only the mandatory slave feature showed below.

Slaver address could be set to “011 1100” or “011 1101” by SA0 pin.

The I2C interface send RAM data and executes the commands sent via the I2C Interface. It could send data in to the RAM. The I2C Interface is two-line communication between different ICs or modules. The two lines are a Serial Data line (SDA) and a Serial Clock line (SCL). Both lines must be connected to a positive supply via a pull-up resistor. Data transfer may be initiated only when the bus is not busy. (Note: SDAin and SDAout are short together and forms SDA in SSD1803A)

Bit Transfer

One data bit is transferred during each clock pulse. The data on the SDA line must remain stable during the HIGH period of the clock pulse because changes in the data line at this time will be interpreted as a control signal. Bit transfer is illustrated in Figure 6-4.

Start and Stop conditions

Both data and clock lines remain HIGH when the bus is not busy. A HIGH-to-LOW transition of

the data line, while the clock is HIGH is defined as the START condition (S). A LOW-to-HIGH transition of the data line while the clock is HIGH is defined as the STOP condition (P). The START and STOP conditions are illustrated in Figure 6-5.

System Configuration

The system configuration consists of

• Transmitter: the device, which sends the data to the bus

• Master: the device, which initiates a transfer, generates clock signals and terminates a transfer

• Slave: the device addressed by a master

• Multi-Master: more than one master can attempt to control the bus at the same time without corrupting the message

• Arbitration: procedure to ensure that, if more than one master simultaneously tries to control the bus, only one is allowed to do so and the message is not corrupted

• Synchronization: procedure to synchronize the clock signals of two or more devices.

Acknowledge

Each byte of eight bits is followed by an acknowledge bit. The acknowledge bit is a HIGH signal put on the bus by the transmitter during which time the master generates an extra acknowledge related clock pulse. A slave receiver which is addressed must generate an acknowledge after the reception of each byte. A master receiver must also generate an acknowledge after the reception of each byte that has been clocked out of the slave transmitter. The device that acknowledges must pull-down the SDA line during the acknowledge clock pulse, so that the SDA line is stable LOW during the HIGH period of the acknowledge related clock pulse (set-up and hold times must be taken into consideration). A master receiver must signal an end-of-data to the transmitter by not generating an acknowledge on the last byte that has been clocked out of the slave. In this event the transmitter must leave the data line HIGH to enable the master to generate a STOP condition. Acknowledgement on the I2C Interface is illustrated in Figure 6-6.

Figure 6-4: Bit transfer on the I2C-bus

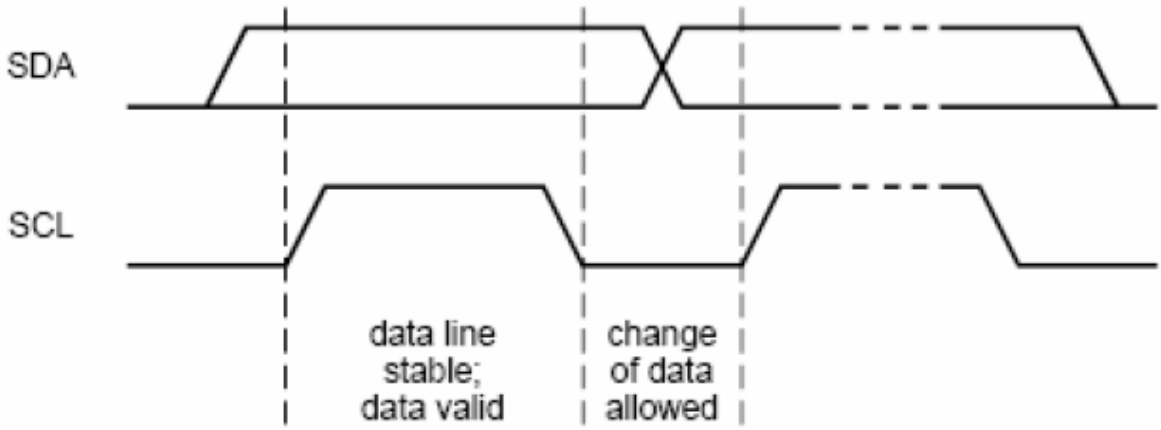
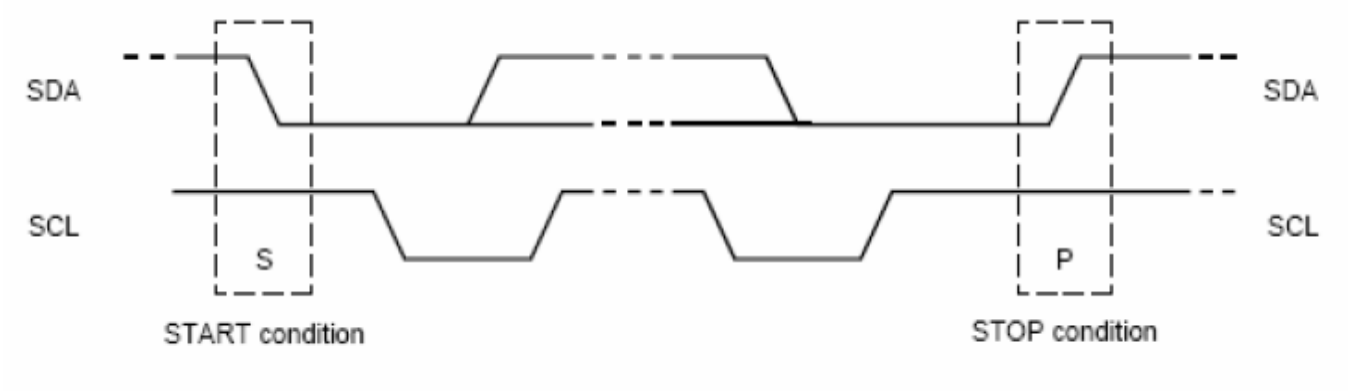


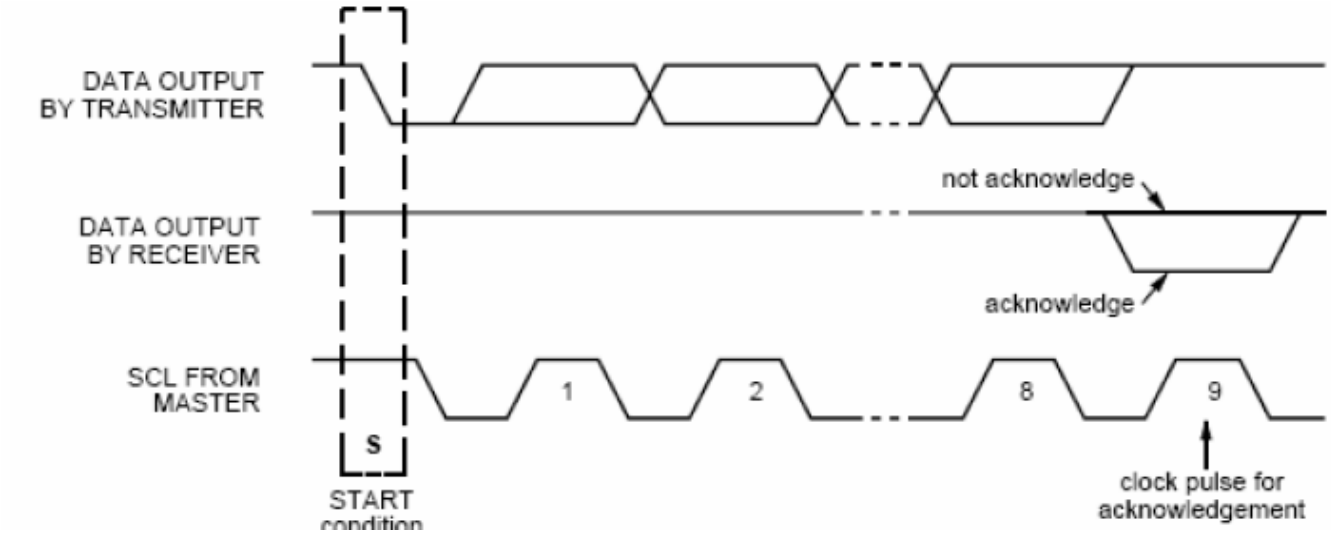
Figure 6-5: START and STOP conditions




```
//Note on I2C pull up resistors.
//These should not be too low otherwise the display will
//not pull the SDA line low enough to register an ACK.
//Suggest 10K.
// LCD initialize procedure VALUES FOR 3.3V 4x20 SSD1803A
void LCD_Init(void)
{
  //set reset low
  //wait 10ms
  //set reset high
  delay(5);
  send_command(0x3a);  //8bit,4line,IS=0,RE=1
  send_command(0x1e);  //Set BS1 (1/6 bias)
  send_command(0x39);  //8bit,4line,IS=1,RE=0
  send_command(0x1c);  //Set BS0 (1/6 bias) + osc
  send_command(0x79);  //Set contrast lower 4 bits
  send_command(0x5d);  //Set ION, BON, contrast bits 4&5
  send_command(0x6d);  //Set DON and amp ratio.
  send_command(0x0c);  //Set display on
  send_command(0x01);  //Clear display
}
```

MIDAS DISPLAYS

Figure 6-6: Acknowledge on the I2C bus



I2C Interface Protocol

The SSD1803A supports command, data read/ write addressed slaves on the bus. Before any data is transmitted on the I2C Interface, the device, which should respond, is addressed first. Two 7-bit slave addresses (0111100 to 0111101) are reserved for the SSD1803A. The R/W# is assigned to 0 for Write and 1 for Read. The I2C Interface protocol is illustrated in Figure 6-7 to 6-9.

The sequence is initiated with a START condition (S) from the I2C Interface master, which is followed by the slave address. All slaves with the corresponding address acknowledge in parallel, all the others will ignore the I2C Interface transfer. After acknowledgement, one or more command words follow which define the status of the addressed slaves.

A command word consists of control byte, which defines C0 and D/C#, plus a data byte. The last control byte is tagged with a cleared most significant bit (i.e. the continuation bit Co). After the last control byte with a cleared Co bit, only data bytes will follow. The state of the D/C# bit defines whether the data byte is interpreted as a command or as RAM data. All addressed slaves on the bus also acknowledge the control and data bytes. After the last control byte, depending on the D/C# bit setting; either a series of display data bytes or command data bytes may follow. If the D/C# bit is set to logic 1, these display bytes are stored in the display RAM at the address specified by the data pointer. The data pointer is automatically updated and the data is directed to the intended SSD1803A device. If the D/C# bit of the last control byte is set to logic 0, these command bytes will be decoded and the setting of the device will be changed according to the received commands. Only the addressed slave makes the acknowledgement after each byte. At the end of the transmission the I2C INTERFACE-bus master issues a STOP condition (P).

Figure 6-7: I2C write mode

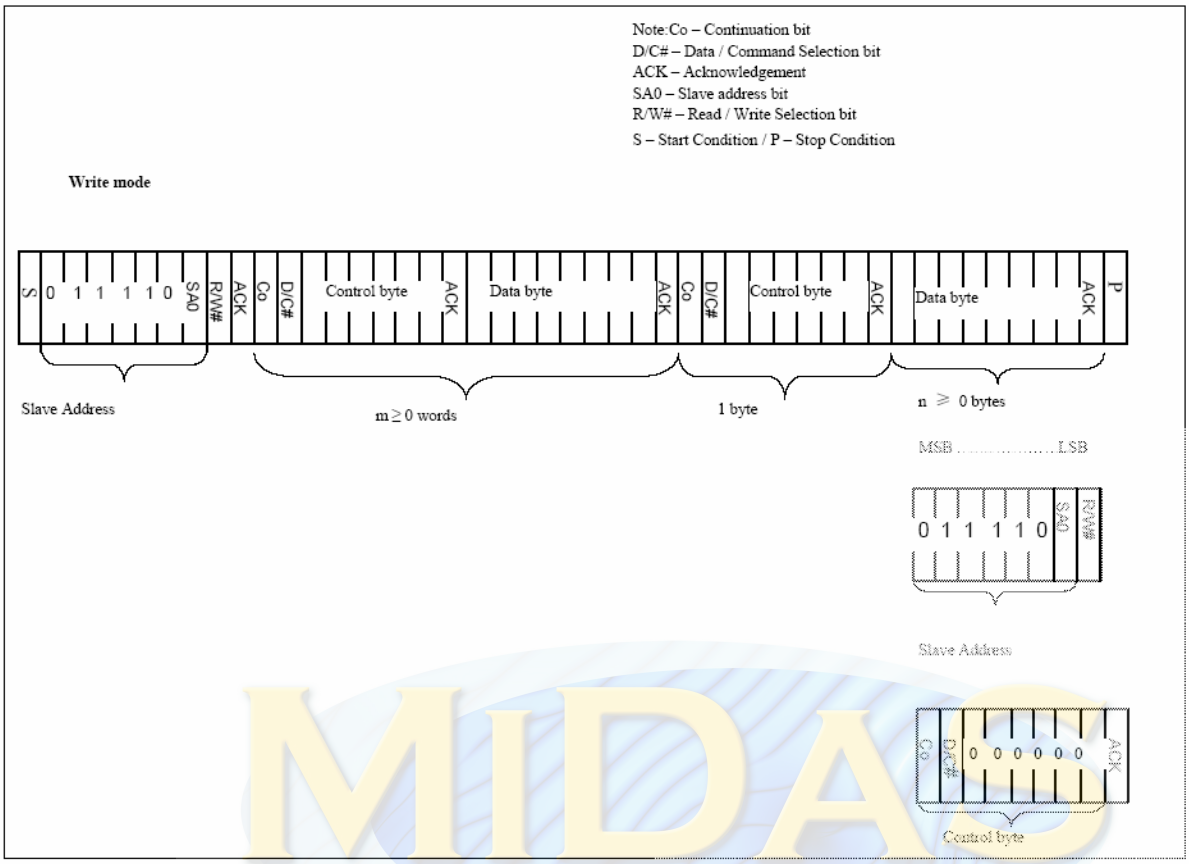
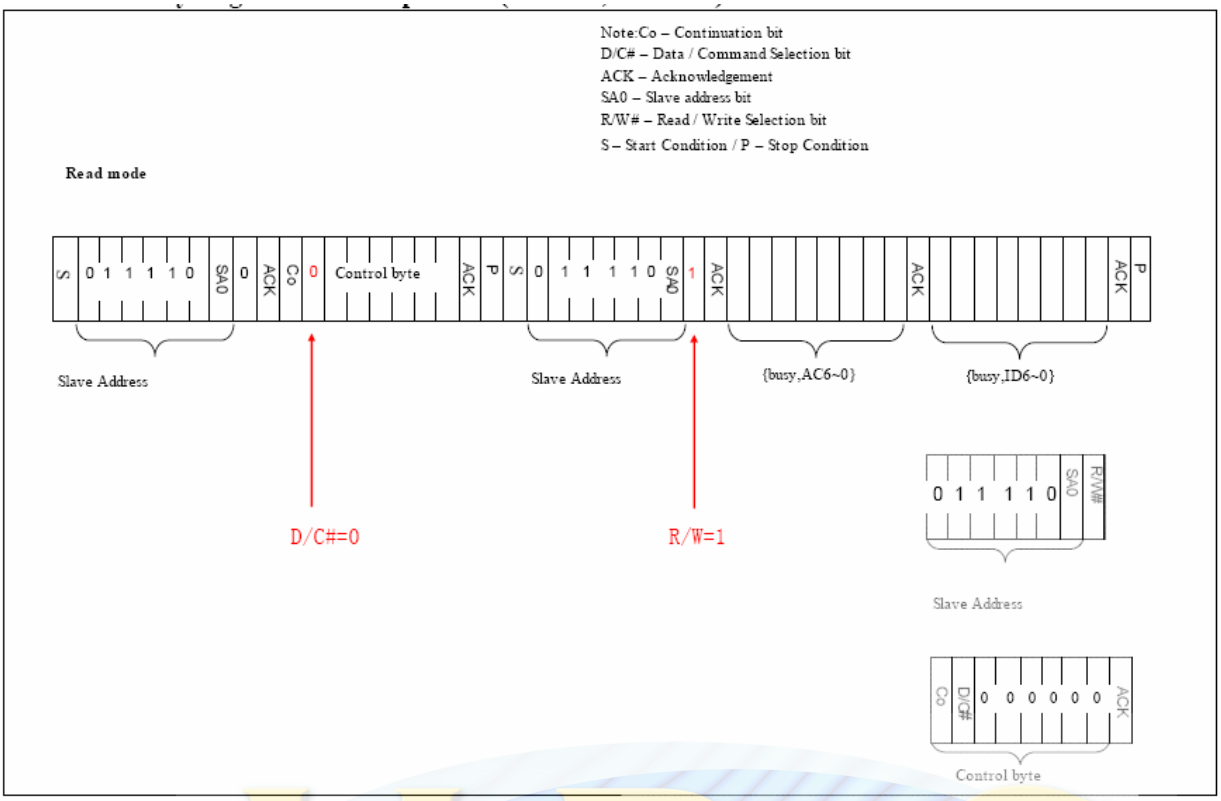


Figure 6-8: I2C read mode

Read busy flag and address/part ID (D/C#=0, R/W#=1)

MIDAS DISPLAYS



Read ram (D/C#=1, R/W#=1)

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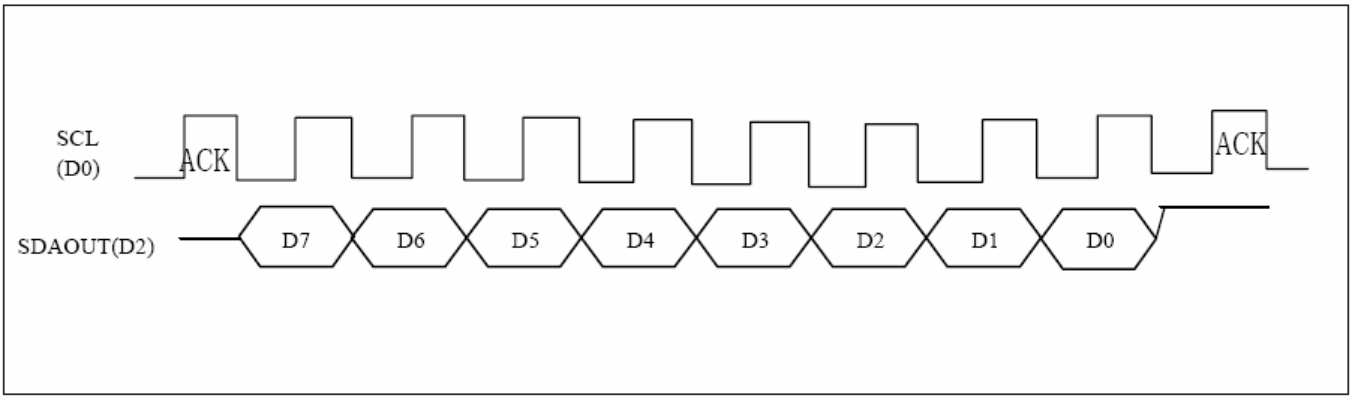
Figure 6-9: Read Timing



During read or write operation, two 8-bit registers are used. One is data register (DR), the other is instruction register (IR). The data register (DR) is used as temporary data storage place for being written into or read from DDRAM/ CGRAM/SEGRAM, target RAM is selected by RAM address setting instruction. Each internal operation, reading from or writing into RAM, is done automatically.

So to speak, after MPU reads DR data, the data in the next DDRAM/ CGRAM/ SEGRAM address is transferred into DR automatically. Also after MPU writes data to DR, the data in DR is transferred into DDRAM/ CGRAM/ SEGRAM automatically. The Instruction register (IR) is used only to store instruction code transferred from MPU. MPU cannot use it to read instruction data. To select register, use D/C# I2C mode.

Table 6-5: Bus interface operations according to D/C# and R/W# inputs

D/C#	R/W#	Operation
0	0	Instruction write operation (MPU writes Instruction code into IR)
0	1	Read busy flag (DB7) and address counter (DB0 - DB6)
1	0	Data write operation (MPU writes data into DR)
1	1	Data read operation (MPU reads data from DR/ Part ID)

6.11 5V IO regulator

SSD1803A accepts two power supply range:

2.4-3.6V **[Low Voltage I/O Application]** and

4.5-5.5V **[5V I/O Application]**

5V IO Regulator is enabled to regulate 5V I/O input to 3V for power supply of internal circuit blocks.

Note: In 5V I/O Application, VOUT should not be lower than VDDIO.

Table 6-6 summarizes the input/ output connection of 5V IO regulator in normal application.

Table 9-6: 5V IO regulator pin description

Pin Name	Low Voltage I/O Application	5V I/O Application
VDDREG	Low, disable 5V IO regulator	High, enable 5V IO regulator
VCI	Short to VDD	Short to VDD
VDD	2.4 -3.6V	NC with stabilizing capacitor It outputs 3V
VDDIO	2.4 -VCI	4.5 -5.5V

MIDAS DISPLAYS

6.12 LCD Driving Voltage Generator and Regulator

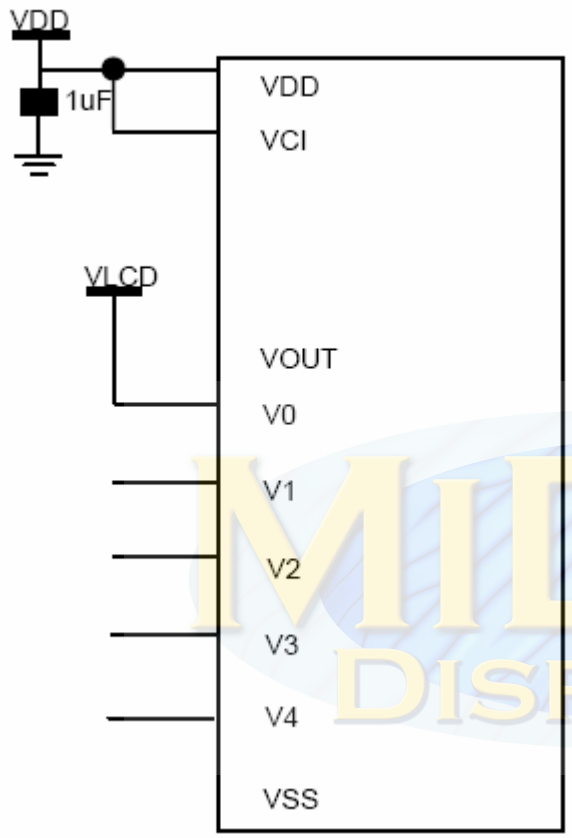
This module generates the LCD voltage required for display driving output.

6.12.1 External VLCD mode

When on-chip booster is turned off, VLCD can be supplied externally to V0 for display driving.

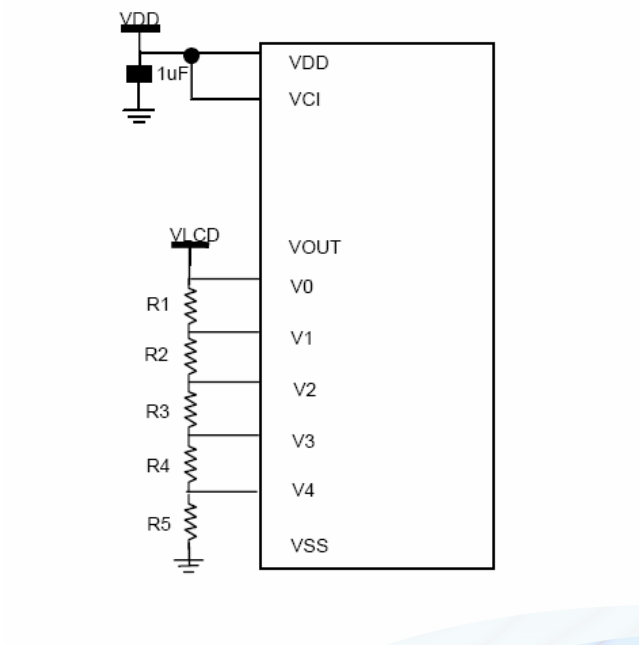
Figure 6-10: On-chip voltage converter application set up

When booster is off and voltage follower is on (Bon=0; Don=1)



MIDAS DISPLAYS

Figure 6-11: On-chip voltage converter application set up
When both booster and voltage follower is off (Bon=0; Don=0)



R1, R2, R3, R4, R5: 20K
VLCD: 10V (max)
*** Recommanded values for 1/5 bias application**

6.12.2 Internal voltage mode

a) On-chip DC-DC voltage converter

Voltage converter is available when Bon=1. Figure 6-21 shows the circuits boosting up the electric
potential between VDD – VSS toward positive side and boosted voltage is output at VOUT.

Figure 6-12: On-chip voltage converter application set up
When both booster and voltage follower is on (Bon=1; Don=1)

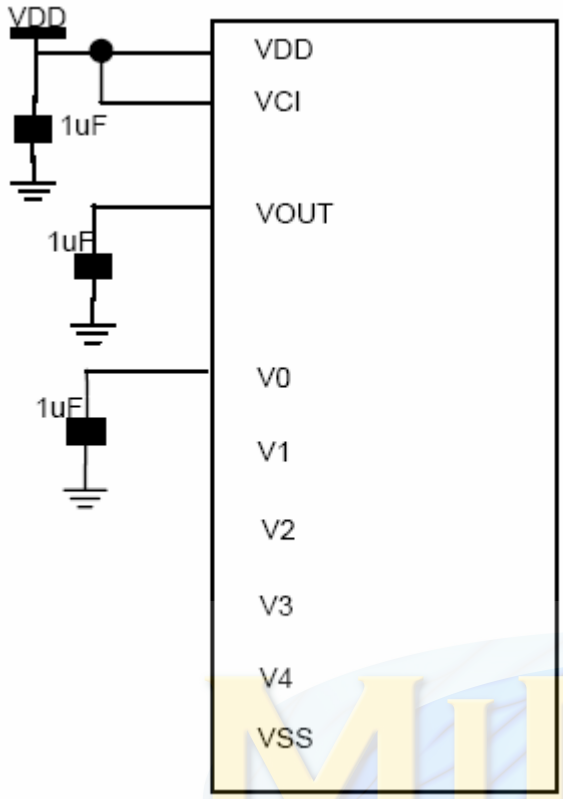
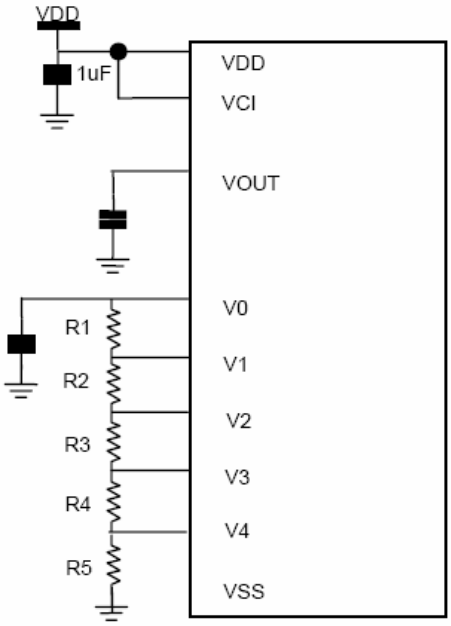


Figure 6-13: On-chip voltage converter application set up
When both booster is on and voltage follower is off (Bon=1; Don=0)

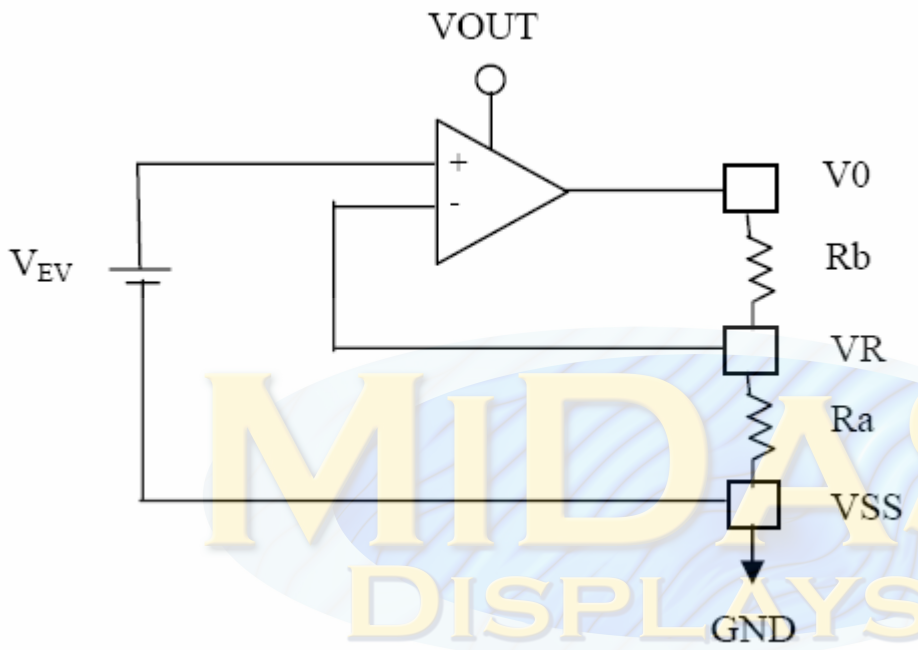


R1, R2, R3, R4, R5: 20K
*** Recommanded values for 1/5 bias application**

b) Voltage regulator circuits (Gain) and Contrast Control

There is a voltage regulator circuits to determine liquid crystal operating voltage, V0, by adjusting resistors, Ra and Rb, within the range of |V4| < |V0| . The circuits which are turned on with voltage converter consist of an operational-amplifier circuits and a feedback gain control. VOUT is the operating voltage for the op-amp, it is required to supply internally or externally. It consists of a feedback gain control for LCD driving contrast curves, eight settings can be selected through software command (Internal resistor ratio Rab2~0).

Figure 6-14: Voltage regulator circuit



Also, software command (C1-5) is used to adjust the 64 contrast voltage levels at each voltage regulator feedback gain. The equation of calculating the LCD driving voltage is given as:

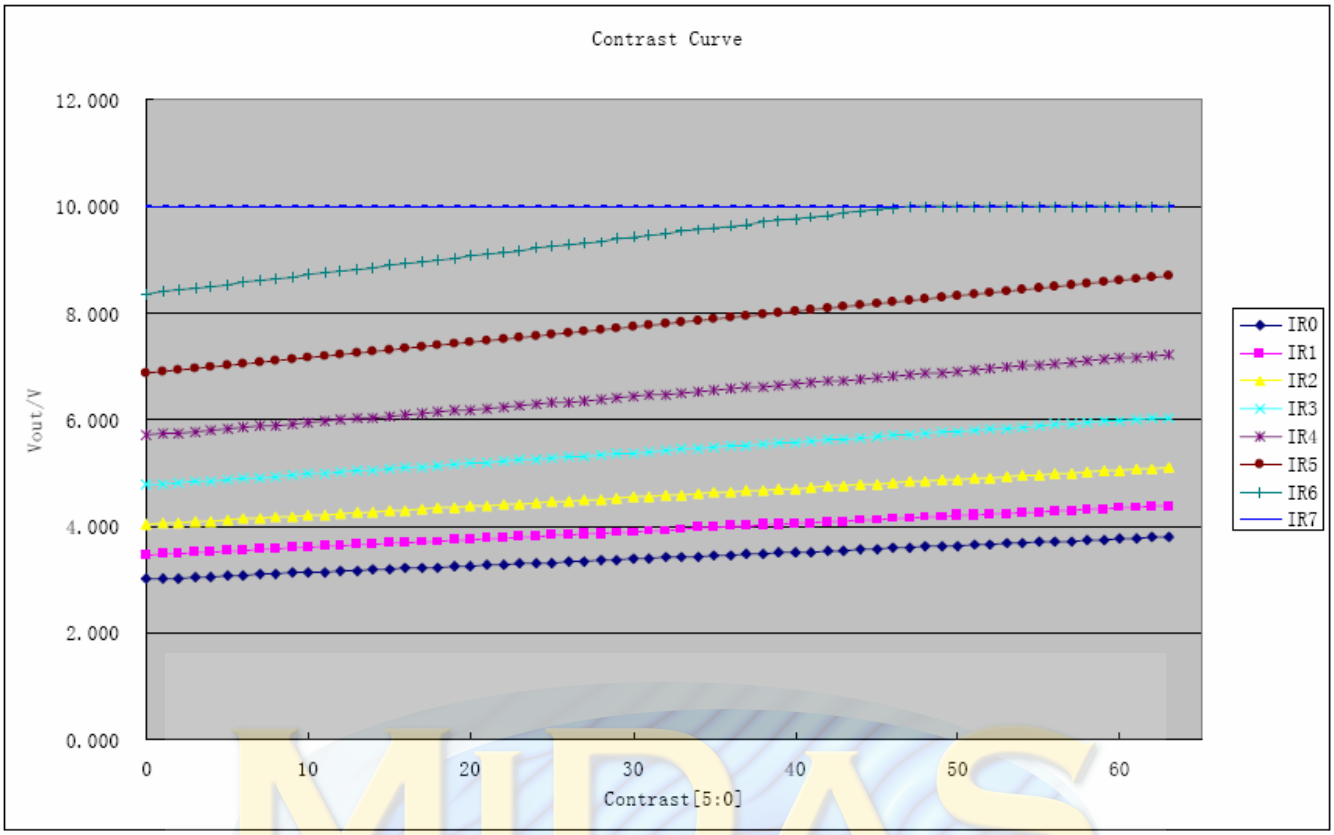
$$V0 = (1 + \frac{Rb}{Ra}) \times V_{EV} [V] \text{ ----------(Equation 1)}$$

$$V_{EV} = [1 - \frac{(63 - \alpha)}{300}) \times V_{REF}][V] \text{--(Equation 2)}$$

, where VREF = 2 and α= contrast setting (d)

Please refer to Figure 6-24 for the contrast curve with 8 sets of internal resistor network gain.

Figure 6-15: Contrast curve



c) Bias Divider

If the Don command is enabled, this circuit block will divide the voltage regulator circuit output (V0) to give the LCD driving levels. External stabilizing capacitors for the divider are optional to reduce the external hardware and pin counts.

d) Bias Ratio Selection circuitry

The software control circuit of 1/4 to 1/7 bias ratio in order to match the characteristic of LCD panel.

e) Self adjust temperature compensation circuitry

Provide 4 different compensation grade selections to satisfy the various liquid crystal temperature grades (-0.05%, -0.10%, -0.15%, -0.20%). The grading can be selected by software control. Defaulted temperature coefficient (TC) value is –0.05%/°C.

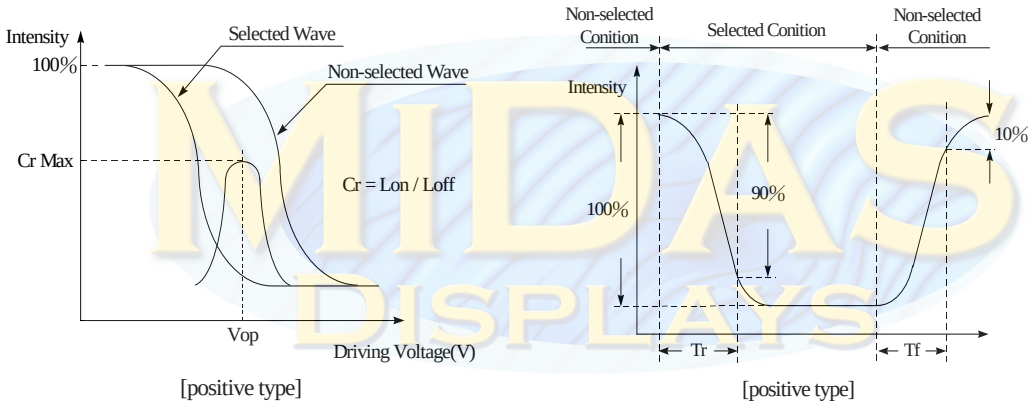
7.13 Oscillator Circuit

This module is an On-Chip low power temperature compensation oscillator circuitry. The oscillator generates the clock for the DC-DC voltage converter and the Display Timing Generator. User may choose to use internal oscillator clock or supply external clock by CLS pin.

7. Optical Characteristics

Item	Symbol	Condition	Min	Typ	Max	Unit
View Angle	(V)θ	CR≧2	20	—	40	deg
	(H)φ	CR≧2	-30	—	30	deg
Contrast Ratio	CR	—	—	3	—	—
Response Time	T rise	—	—	350	500	ms
	T fall	—	—	150	200	ms

Definition of Operation Voltage, Vop. **Definition of Response Time, Tr and Tf.**

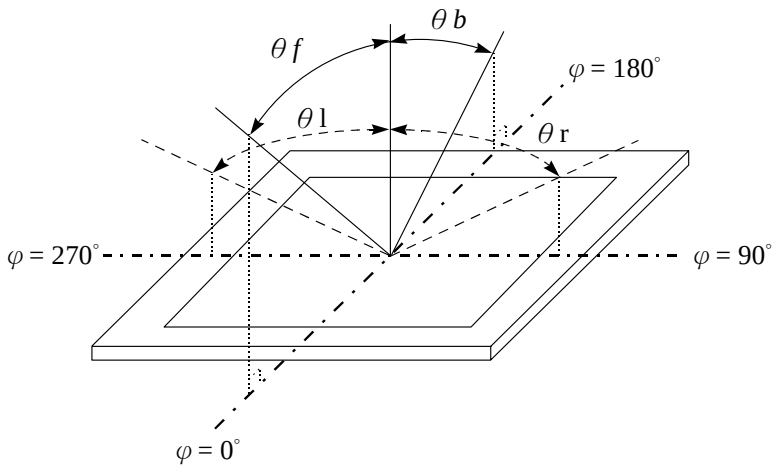


Conditions:

Operating Voltage : Vop Viewing Angle(θ，φ) : 0°， 0°

Frame Frequency: 64 HZ Driving Waveform: 1/N duty, 1/a bias

Definition of viewing angle (CR≧2)



8. Absolute Maximum Ratings

Item	Symbol	Min	Typ	Max	Unit
Operating Temperature	T_{OP}	-20	—	+70	℃
Storage Temperature	T_{ST}	-30	—	+80	℃
Power Supply Voltage	V_{DD}	-0.3	—	6.0	V
LCD Driver Voltage	VLCD	-0.3	—	15.0	V
Input Voltage	VIN	-0.3	—	V_{DD}+0.3	V

9. Electrical Characteristics

Item	Symbol	Condition	Min	Typ	Max	Unit
Supply Voltage For Logic	V_{DDIO}	Low Voltage I/O App.	2.4	3.0	V_{DD}	V
		5V I/O App.	4.5	5.0	5.5	V
	V_{DD}	—	2.4	3.0	3.6	V
Supply Voltage For LCD	V_O-V_{SS}	Ta=-20℃	—	—	—	V
		Ta=25℃	—	7.8	—	V
		Ta=70℃	—	—	—	V
Input High Volt.	V_{IH}	—	0.8 V_{DDIO}	—	V_{DDIO}	V
Input Low Volt.	V_{IL}	—	—	—	0.2 V_{DDIO}	V
Output High Volt.	V_{OH}	—	0.8 V_{DDIO}	—	V_{DDIO}	V
Output Low Volt.	V_{OL}	—	—	—	0.2 V_{DDIO}	V
Supply LCM current	IDD	VDD=5.0V	—	1.0	—	mA

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10. Backlight Information

Specification

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT	TEST CONDITION
Supply Current	ILED	43.2	48	60	mA	V= 3.5 V
Supply Voltage	V	3.4	3.5	3.6	V	—
Reverse Voltage	VR	—	—	5	V	—
Luminous Intensity (Without LCD)	IV	400	500	—	CD/M^2	ILED=48 mA
Chromaticity	x	—	0.30	—	—	—
	y	—	0.29	—	—	—
LED Life Time	—		50K		Hr.	$I_{LED} \leqq 48$ mA
Color	White					

Note: The LED of B/L is drive by current only；driving voltage is only for reference
To make driving current in safety area (waste current between minimum and maximum).

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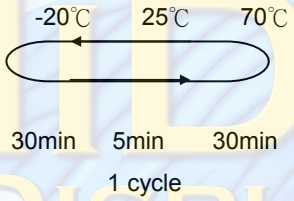
11. Reliability

Content of Reliability Test (wide temperature, -20℃~70℃)

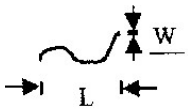
Environmental Test			
Test Item	**Content of Test**	**Condition**	**Note**
High Temperature storage	Endurance test applying the high storage temperature for a long time.	80℃ 200hrs	2
Low Temperature storage	Endurance test applying the high storage temperature for a long time.	-30℃ 200hrs	1,2
High Temperature Operation	Endurance test applying the electric stress (Voltage & Current) and the thermal stress to the element for a long time.	70℃ 200hrs	-
Low Temperature Operation	Endurance test applying the electric stress under low temperature for a long time.	-20℃ 200hrs	1
High Temperature/ Humidity Operation	The module should be allowed to stand at 60℃,90%RH max For 96hrs under no-load condition excluding the polarizer, Then taking it out and drying it at normal temperature.	60℃,90%RH 96hrs	1,2
Thermal shock resistance	The sample should be allowed stand the following 10 cycles of operation  	-20℃/70℃ 10 cycles	-
Vibration test	Endurance test applying the vibration during transportation and using.	fixed amplitude: 15mm Vibration. Frequency: 10~55Hz. One cycle 60 seconds to 3 directions of X,Y,Z for Each 15 minutes	3
Static electricity test	Endurance test applying the electric stress to the terminal.	VS=800V,RS=1.5kΩ CS=100pF 1 time	——

Note1: No dew condensation to be observed.

Note2: The function test shall be conducted after 4 hours storage at the normal temperature and humidity after remove from the test chamber.

Note3: Vibration test will be conducted to the product itself without putting it in a container.

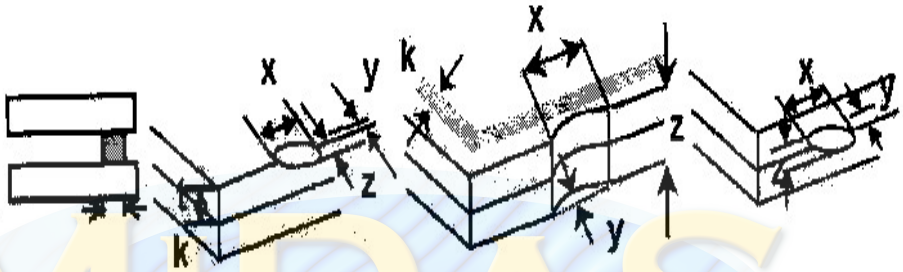
12. Inspection specification

<table>
<tr><th>NO</th><th>Item</th><th>Criterion</th><th>AQL</th></tr>
<tr><td>01</td><td>Electrical Testing</td><td>1.1 Missing vertical, horizontal segment, segment contrast defect.
1.2 Missing character, dot or icon.
1.3 Display malfunction.
1.4 No function or no display.
1.5 Current consumption exceeds product specifications.
1.6 LCD viewing angle defect.
1.7 Mixed product types.
1.8 Contrast defect.</td><td>0.65</td></tr>
<tr><td>02</td><td>Black or white spots on LCD (display only)</td><td>2.1 White and black spots on display ≦0.25mm, no more than three white or black spots present.
2.2 Densely spaced: No more than two spots or lines within 3mm</td><td>2.5</td></tr>
<tr><td rowspan="2">03</td><td rowspan="2">LCD black spots, white spots, contamination (non-display)</td><td>3.1 Round type : As following drawing
Φ=(x + y) / 2</td><td>2.5</td></tr>
<tr><td>3.2 Line type : (As following drawing)
 

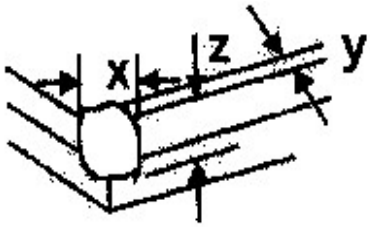
<table>
<tr><th>Length</th><th>Width</th><th>Acceptable Q TY</th></tr>
<tr><td>---</td><td>W≦0.02</td><td>Accept no dense</td></tr>
<tr><td>L≦3.0</td><td>0.02＜W≦0.03</td><td rowspan="2">2</td></tr>
<tr><td>L≦2.5</td><td>0.03＜W≦0.05</td></tr>
<tr><td>---</td><td>0.05＜W</td><td>As round type</td></tr>
</table></td><td>2.5</td></tr>
<tr><td>04</td><td>Polarizer bubbles</td><td>If bubbles are visible, judge using black spot specifications, not easy to find, must check in specify direction.
<table>
<tr><th>Size Φ</th><th>Acceptable Q TY</th></tr>
<tr><td>Φ≦0.20</td><td>Accept no dense</td></tr>
<tr><td>0.20＜Φ≦0.50</td><td>3</td></tr>
<tr><td>0.50＜Φ≦1.00</td><td>2</td></tr>
<tr><td>1.00＜Φ</td><td>0</td></tr>
<tr><td>Total Q TY</td><td>3</td></tr>
</table></td><td>2.5</td></tr>
</table>

MIDAS DISPLAYS

<table>
<tr><th>NO</th><th>Item</th><th>Criterion</th><th>AQL</th></tr>
<tr><td>05</td><td>Scratches</td><td>Follow NO.3 LCD black spots, white spots, contamination</td><td></td></tr>
<tr><td>06</td><td>Chipped glass</td><td>
Symbols Define:
x: Chip length y: Chip width z: Chip thickness
k: Seal width t: Glass thickness a: LCD side length
L: Electrode pad length:

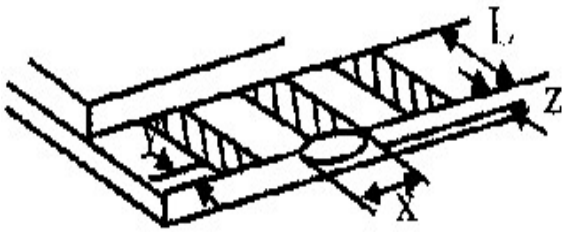
6.1 General glass chip :
6.1.1 Chip on panel surface and crack between panels:


<table>
<tr><th>z: Chip thickness</th><th>y: Chip width</th><th>x: Chip length</th></tr>
<tr><td>Z≦1/2t</td><td>Not over viewing area</td><td>x≦1/8a</td></tr>
<tr><td>1/2t＜z≦2t</td><td>Not exceed 1/3k</td><td>x≦1/8a</td></tr>
</table>
⊙If there are 2 or more chips, x is total length of each chip.

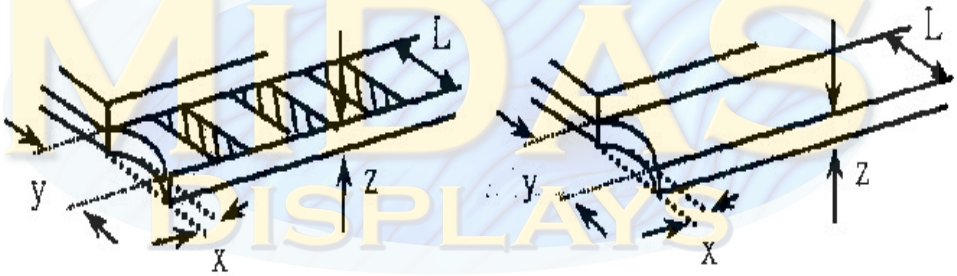
6.1.2 Corner crack:


<table>
<tr><th>z: Chip thickness</th><th>y: Chip width</th><th>x: Chip length</th></tr>
<tr><td>Z≦1/2t</td><td>Not over viewing area</td><td>x≦1/8a</td></tr>
<tr><td>1/2t＜z≦2t</td><td>Not exceed 1/3k</td><td>x≦1/8a</td></tr>
</table>
⊙If there are 2 or more chips, x is the total length of each chip.
</td><td>2.5</td></tr>
</table>

NO	Item	Criterion	AQL
06	Glass crack	Symbols : x: Chip length y: Chip width z: Chip thickness k: Seal width t: Glass thickness a: LCD side length L: Electrode pad length 6.2 Protrusion over terminal : 6.2.1 Chip on electrode pad :	2.5



y: Chip width	x: Chip length	z: Chip thickness
y≦0.5mm	x≦1/8a	0 ＜ z ≦ t

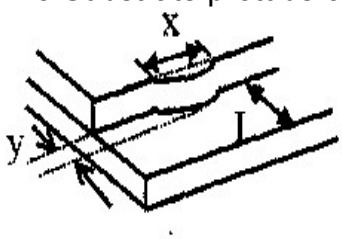


y≦ L	x≦1/8a	0 ＜ z ≦ t

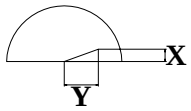
⊙If the chipped area touches the ITO terminal, over 2/3 of the ITO must remain and be inspected according to electrode terminal specifications.

⊙If the product will be heat sealed by the customer, the alignment mark not be damaged.

6.2.3 Substrate protuberance and internal crack.



y: width	x: length
y≦1/3L	x ≦ a

NO	Item	Criterion	AQL
07	Cracked glass	The LCD with extensive crack is not acceptable.	2.5
08	Backlight elements	8.1 Illumination source flickers when lit. 8.2 Spots or scratched that appear when lit must be judged. Using LCD spot, lines and contamination standards. 8.3 Backlight doesn't light or color wrong.	0.65 2.5 0.65
09	Bezel	9.1 Bezel may not have rust, be deformed or have fingerprints, stains or other contamination. 9.2 Bezel must comply with job specifications.	2.5 0.65
10	PCB、COB	10.1 COB seal may not have pinholes larger than 0.2mm or contamination. 10.2 COB seal surface may not have pinholes through to the IC. 10.3 The height of the COB should not exceed the height indicated in the assembly diagram. 10.4 There may not be more than 2mm of sealant outside the seal area on the PCB. And there should be no more than three places. 10.5 No oxidation or contamination PCB terminals. 10.6 Parts on PCB must be the same as on the production characteristic chart. There should be no wrong parts, missing parts or excess parts. 10.7 The jumper on the PCB should conform to the product characteristic chart. 10.8 If solder gets on bezel tab pads, LED pad, zebra pad or screw hold pad, make sure it is smoothed down. 10.9 The Scraping testing standard for Copper Coating of PCB  **X * Y<=2mm^2**	2.5 2.5 0.65 2.5 2.5 0.65 0.65 2.5 2.5
11	Soldering	11.1 No un-melted solder paste may be present on the PCB. 11.2 No cold solder joints, missing solder connections, oxidation or icicle. 11.3 No residue or solder balls on PCB. 11.4 No short circuits in components on PCB.	2.5 2.5 2.5 0.65

NO	Item	Criterion	AQL
12	General appearance	12.1 No oxidation, contamination, curves or, bends on interface Pin (OLB) of TCP. 12.2 No cracks on interface pin (OLB) of TCP. 12.3 No contamination, solder residue or solder balls on product. 12.4 The IC on the TCP may not be damaged, circuits. 12.5 The uppermost edge of the protective strip on the interface pin must be present or look as if it causes the interface pin to sever. 12.6 The residual rosin or tin oil of soldering (component or chip component) is not burned into brown or black color. 12.7 Sealant on top of the ITO circuit has not hardened. 12.8 Pin type must match type in specification sheet. 12.9 LCD pin loose or missing pins. 12.10 Product packaging must the same as specified on packaging specification sheet. 12.11 Product dimension and structure must conform to product specification sheet.	2.5 0.65 2.5 2.5 2.5 2.5 2.5 0.65 0.65 0.65 0.65

MIDAS DISPLAYS

13. Precautions in use of LCD Modules

1. Avoid applying excessive shocks to the module or making any alterations or modifications to it.
2. Don’t make extra holes on the printed circuit board, modify its shape or change the components of LCD module.
3. Don’t disassemble the LCM.
4. Don’t operate it above the absolute maximum rating.
5. Don’t drop, bend or twist LCM.
6. Soldering: only to the I/O terminals.
7. Storage: please storage in anti-static electricity container and clean environment.
8. Midas have the right to change the passive components
   (Resistors,capacitors and other passive components will have different appearance and color caused by the different supplier.)
9. Midas have the right to change the PCB Rev.

14. Material List of Components for RoHs

1. Midas Components Ltd. hereby declares that all of or part of products, including, but not limited to, the LCM, accessories or packages, manufactured and/or delivered to your company (including your subsidiaries and affiliated company) directly or indirectly by our company (including our subsidiaries or affiliated companies) do not intentionally contain any of the substances listed in all applicable EU directives and regulations, including the following substances.

   Exhibit A：The Harmful Material List

Material	(Cd)	(Pb)	(Hg)	(Cr6+)	PBBs	PBDEs
Limited Value	100 ppm	1000 ppm	1000 ppm	1000 ppm	1000 ppm	1000 ppm
Above limited value is set up according to RoHS.						

2. Process for RoHS requirement：
   (1) Use the Sn/Ag/Cu soldering surface；the surface of Pb-free solder is rougher than we used before.
   (2) Heat-resistance temp.：
   Reflow：250℃, 30 seconds Max.；
   Connector soldering wave or hand soldering：320℃, 10 seconds max.
   (3) Temp. curve of reflow, max. Temp.：235±5℃；
   Recommended customer's soldering temp. of connector：280℃, 3 seconds.

15. Recommendable storage

1. Place the panel or module in the temperature 25°C±5°C and the humidity below 65% RH
2. Do not place the module near organics solvents or corrosive gases.
3. Do not crush, shake, or jolt the module