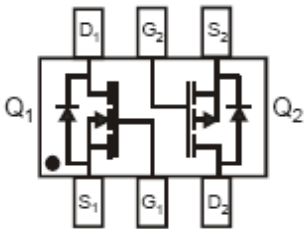
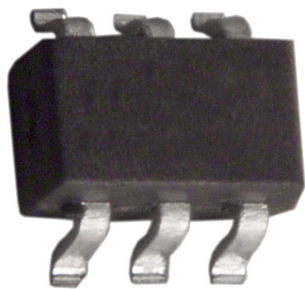


Complementary Pair Enhancement Mode Field Effect Transistor



SOT-363

Features:

- Low On-Resistance
- Low Gate Threshold Voltage
- Low Input Capacitance
- Fast Switching Speed
- Low Input / Output Leakage
- Complementary Pair

Maximum Ratings: Total Device
Ratings at 25°C unless otherwise specified.

Parameter	Symbol	Value	Units
Power Dissipation	P _D	200	mW
Thermal resistance, junction-to-ambient	R _{θJA}	625	°C/W
Junction and storage temperature	T _J , T _{stg}	-55 to +150	°C

N-Channel –Q₁, 2N7002 Section

Drain-source voltage	V _{DSS}	60	V
Drain-gate voltage(R _{GS} ≤1MΩ)	V _{DGR}	60	V
Gate -source voltage continuous Pulsed	V _{GSS}	±20 ±40	V
Drain current continuous Continuous at 100°C Pulsed	I _D	115 73 800	mA

N-Channel –Q₂, BSS84 Section

Drain-source voltage	V _{DSS}	-50	V
Drain-gate voltage (R _{GS} ≤1MΩ)	V _{DGR}	-50	V
Gate -Source voltage continuous	V _{GSS}	±20	V
Drain current continuous	I _D	-130	mA



Complementary Pair Enhancement Mode Field Effect Transistor



Electrical Characteristics:

Ratings at 25°C unless otherwise specified
Q1, 2N7002 Section

Parameter	Symbol	Test conditions	Min.	Typ.	Max.	Unit
Drain-source breakdown voltage	$V_{(BR)DSS}$	$V_{GS}=0V, I_D=10\mu A$	60	70	-	V
Gate threshold voltage	$V_{GS(th)}$	$V_{DS}=V_{GS}, I_D=250\mu A$	1	-	2.5	
Gate-body leakage Forward Reverse	I_{GSS}	$V_{DS}=0V, V_{GS}=20V$ $V_{DS}=0V, V_{GS}=-20V$	- -	- -	100 -100	nA
Zero gate voltage drain current	I_{DSS}	$V_{DS}=60V, V_{GS}=0V$	-	-	1	μA
		$V_{DS}=60V, V_{GS}=0V, T_J=125^\circ C$	-	-	500	
On-state drain current	$I_{D(on)}$	$V_{GS}=10V, V_{DS}=7.5V$	0.5	1	-	A
Drain-source on-voltage	$V_{DS(on)}$	$V_{GS}=10V, I_D=500mA$	-	0.6	3.75	V
		$V_{GS}=5V, I_D=50mA$	-	0.09	1.5	
Forward transconductance	g_{FS}	$V_{DS}=10V, I_D=200mA$	80	-	-	mS
Static drain-source on-resistance	$R_{DS(on)}$	$V_{GS}=5V, I_D=50mA$	-	3.2	7.5	Ω
		$V_{GS}=10V, I_D=500mA, T_J=125^\circ C$	-	4.4	13.5	
Input capacitance	C_{iss}	$V_{DS}=25V, V_{GS}=0V, f=1MHz$	-	22	50	pF
Output capacitance	C_{oss}		-	11	25	
Reverse transfer capacitance	C_{rss}		-	2	5	
Turn-on delay time	$t_{d(on)}$	$V_{DD}=30V, I_D=0.2A,$ $R_L=150\Omega, V_{GS}=10V,$ $R_{GEN}=25\Omega$	-	7	20	ns
Turn-Off Delay Time	$t_{d(off)}$		-	11		

Complementary Pair Enhancement Mode Field Effect Transistor



Electrical Characteristics:

Ratings at 25°C unless otherwise specified
Q2, BSS84 Section

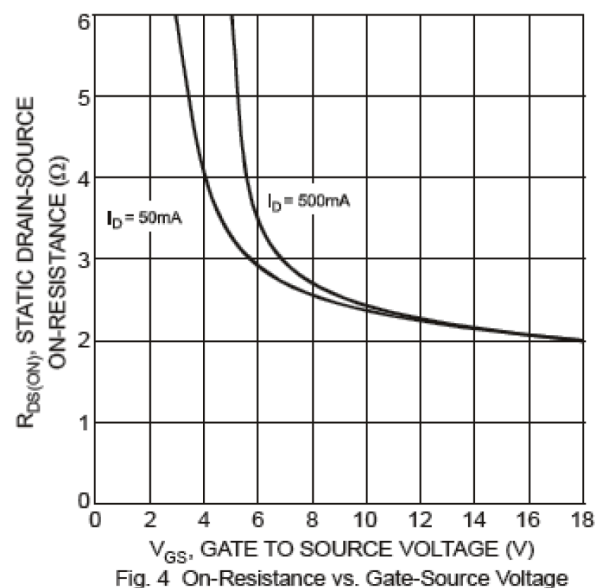
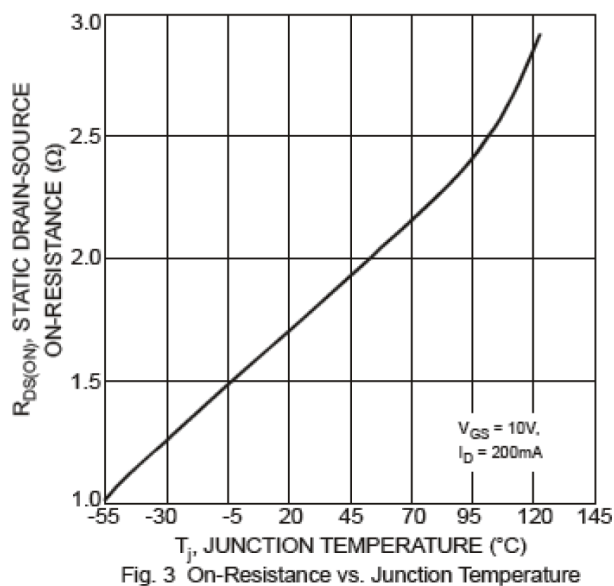
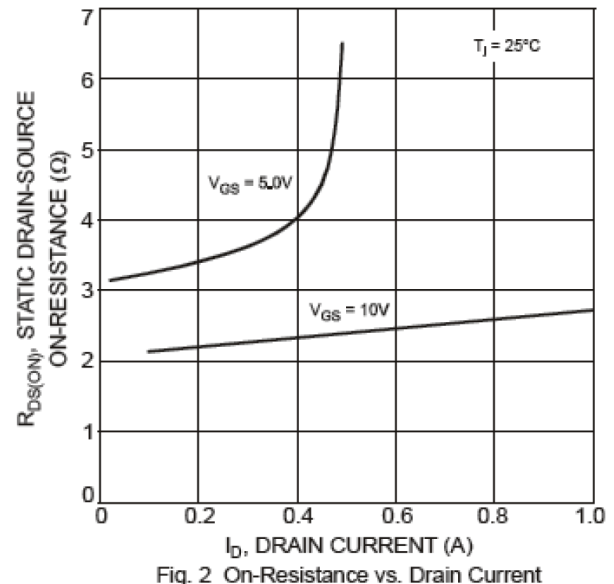
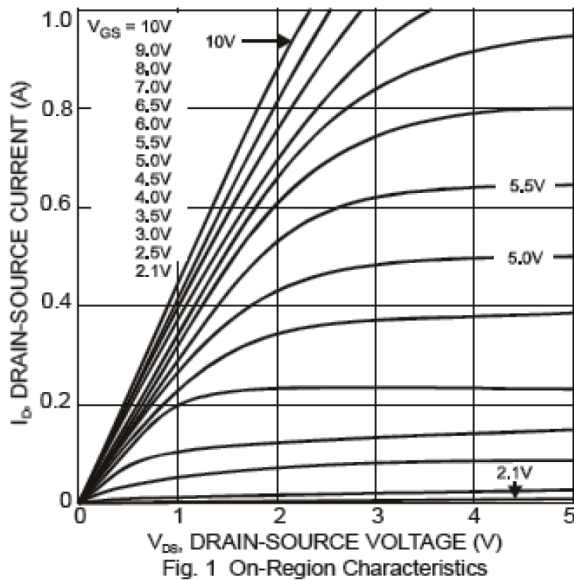
Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
Drain-source breakdown voltage	$V_{(BR)DSS}$	$V_{GS}=0V, I_D=-250\mu A$	-50	-	-	V
Gate threshold voltage	$V_{GS(th)}$	$V_{DS}=V_{GS}, I_D=-1mA$	-0.8	-	-2	
Gate-body leakage Forward Reverse	I_{GSS}	$V_{DS}=0V, V_{GS}=20V$ $V_{DS}=0V, V_{GS}=-20V$	- -	- -	100 -100	nA
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS}=-50V, V_{GS}=0V, T_J=25^\circ C$	-	-	-15	nA
		$V_{DS}=-50V, V_{GS}=0V, T_J=125^\circ C$	-	-	-60	
		$V_{DS}=-25V, V_{GS}=0V, T_J=25^\circ C$	-	-	-100	
Forward transconductance	g_{FS}	$V_{DS}=-25V, I_D=-0.1A$	0.05	-	-	S
Static drain-Source on-resistance	$R_{DS(ON)}$	$V_{GS}=-5V, I_D=-0.1A$	-	-	10	Ω
On-state drain current	$I_{D(ON)}$	$V_{GS}=10V, V_{DS}=7.5V$	0.5	1	-	A
Input capacitance	C_{ISS}	$V_{DS}=-25V, V_{GS}=0V, f=1MHz$	-	-	45	pF
Output capacitance	C_{OSS}		-	-	25	
Reverse transfer capacitance	C_{RSS}		-	-	12	
Turn-on delay time	$t_{D(ON)}$	$V_{DD}=-30V, I_D=-0.27A,$ $V_{GS}=-10V, R_{GEN}=50\Omega$	-	10	-	ns
Turn-off delay time	$t_{D(OFF)}$		-	18	-	

Complementary Pair Enhancement Mode Field Effect Transistor



Typical Characteristics:

$T_A = 25^\circ\text{C}$ unless otherwise specified



Complementary Pair Enhancement Mode Field Effect Transistor

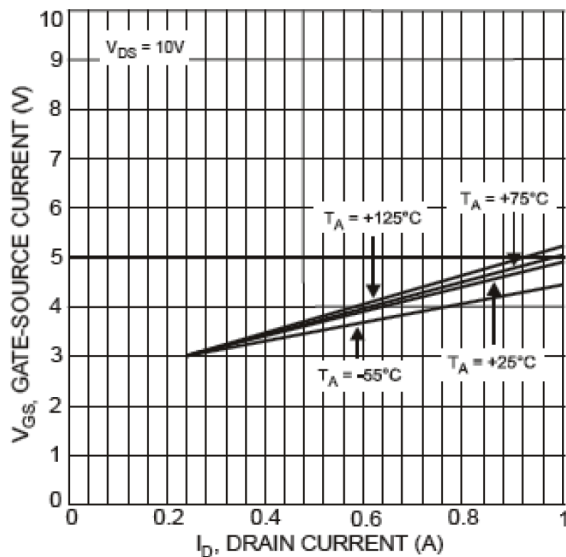


Fig. 5 Typical Transfer Characteristics

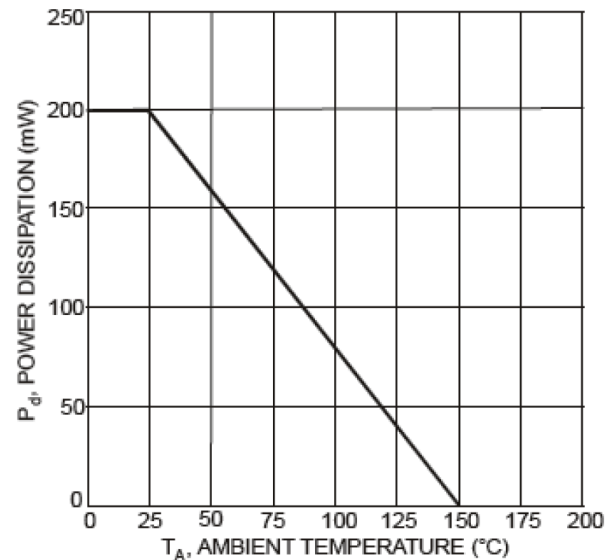


Fig. 6 Max Power Dissipation vs. Ambient Temperature

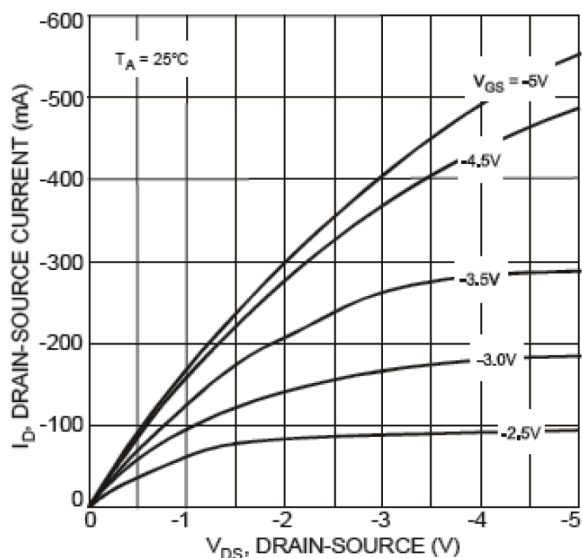


Fig. 7 Drain-Source Current vs. Drain-Source Voltage

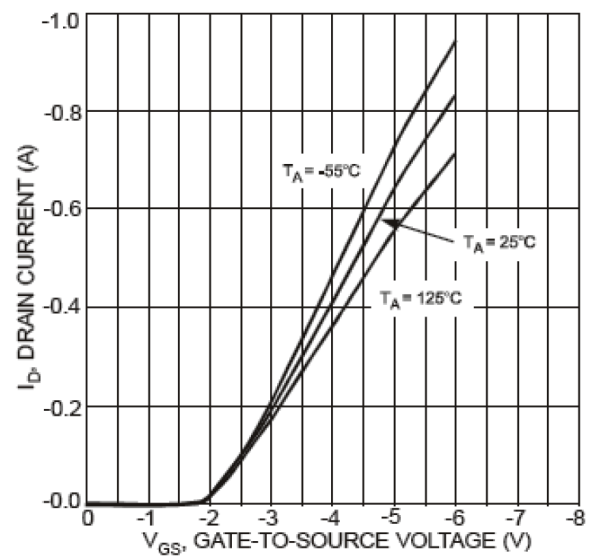


Fig. 8 Drain Current vs. Gate-Source Voltage

Complementary Pair Enhancement Mode Field Effect Transistor



Fig. 7 Drain-Source Current vs. Drain-Source Voltage

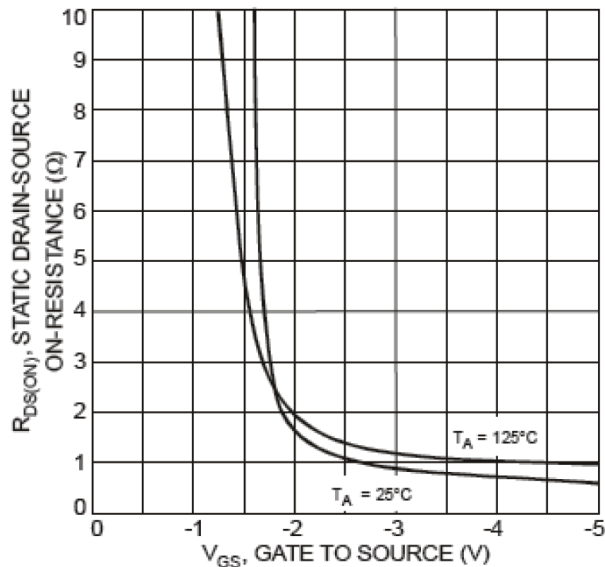


Fig. 9 On-Resistance vs. Gate-Source Voltage

Fig. 8 Drain Current vs. Gate-Source Voltage

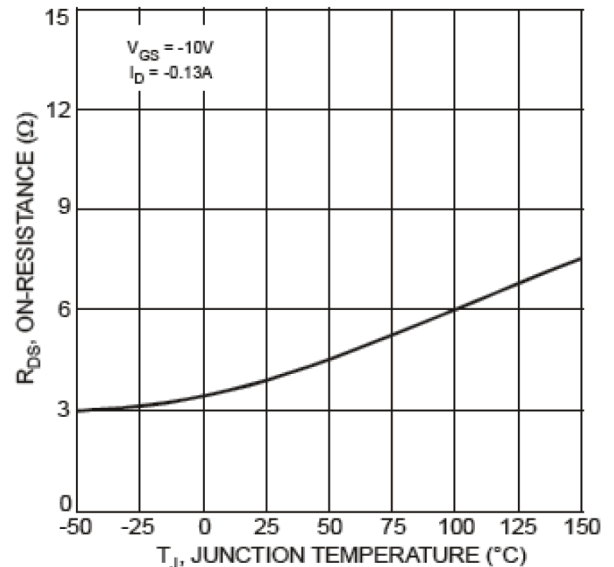


Fig. 10 On-Resistance vs. Junction Temperature

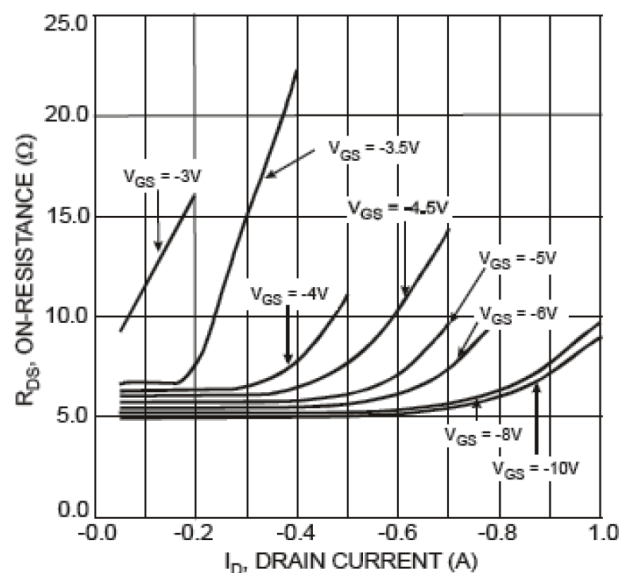


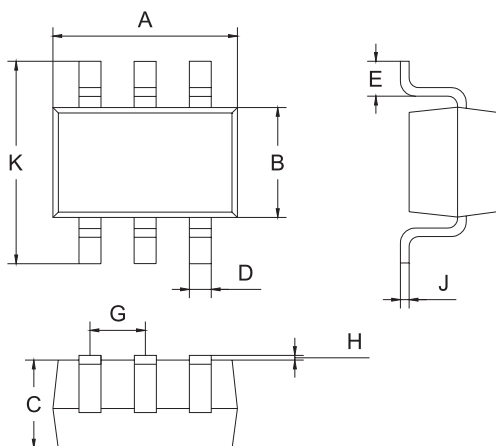
Fig. 11 On-Resistance vs. Drain Current

Complementary Pair Enhancement Mode Field Effect Transistor



Package Outline:

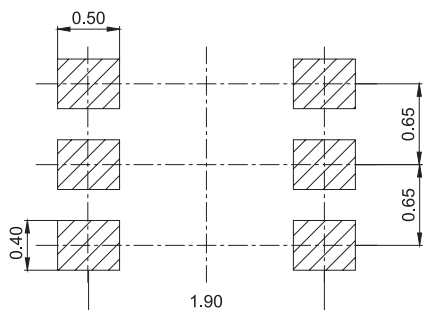
Plastic surface mounted package



SOT-363		
Dim.	Min.	Max.
A	2	2.2
B	1.15	1.35
C	0.95 Typ.	
D	0.25 Typ.	
E	0.25	0.4
G	0.6	0.7
H	0.02	0.1
J	0.1 Typ.	
K	2.2	2.4

Dimensions : Millimetres

Soldering Footprint:



Dimensions : Millimetres

Package Information:

Device	Package	Shipping
BSS8402DW-7-F	SOT-363	3,000 / Tape & Reel

Part Number Table

Description	Part Number
Complementary Pair Enhancement Mode Field Effect Transistor	BSS8402DW-7-F

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