CS8422

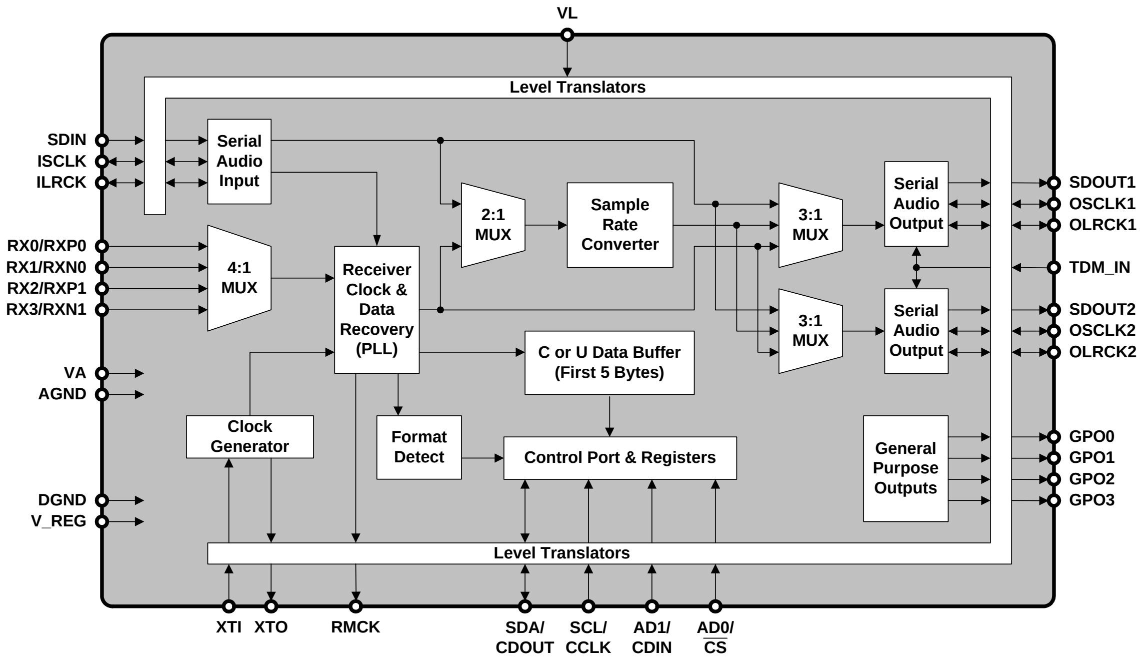
24-bit, 192 kHz, Asynchronous Sample Rate Converter with Integrated Digital Audio Interface Receiver

Sample Rate Converter Features

- 140 dB Dynamic Range
- -120 dB THD+N
- No External Master Clock Required
- Supports Sample Rates up to 211 kHz
- Input/Output Sample Rate Ratios from 6:1 to 1:6
- Master Mode Master Clock/Sample Rate Ratio Support: 64, 96, 128, 192, 256, 384, 512, 768, 1024
- 16, 18, 20, or 24-bit Data I/O
- Dither Automatically Applied and Scaled to Output Resolution
- Multiple Device Outputs are Phase Matched

Digital Audio Interface Receiver Features

- Complete EIAJ CP1201, IEC-60958, AES3, S/PDIF Compatible Receiver
- 28 kHz to 216 kHz Sample Rate Range
- 2:1 Differential AES3 or 4:1 S/PDIF Input Mux
- De-emphasis Filtering for 32 kHz, 44.1 kHz, and 48 kHz
- Recovered Master Clock Output: 64 x Fs, 96 x Fs, 128 x Fs, 192 x Fs, 256 x Fs, 384 x Fs, 512 x Fs, 768 x Fs, 1024 x Fs
- 49.152 MHz Maximum Recovered Master Clock Frequency
- Ultra-low-jitter Clock Recovery
- High Input Jitter Tolerance
- No External PLL Filter Components Required
- Selectable and Automatic Clock Switching
- AES3 Direct Output and AES3 TX Pass-through
- On-chip Channel Status Data Buffering
- Automatic Detection of Compressed Audio Streams
- Decodes CD Q Sub-Code


VL
Level Translators
SDIN
ISCLK
ILRCK
Serial Audio Input
RX0/RXP0
RX1/RXN0
RX2/RXP1
RX3/RXN1
4:1 MUX
Receiver Clock & Data Recovery (PLL)
2:1 MUX
Sample Rate Converter
3:1 MUX
3:1 MUX
Serial Audio Output
Serial Audio Output
SDOUT1
OSCLK1
OLRCK1
TDM_IN
SDOUT2
OSCLK2
OLRCK2
C or U Data Buffer (First 5 Bytes)
VA
AGND
Clock Generator
Format Detect
Control Port & Registers
General Purpose Outputs
GPO0
GPO1
GPO2
GPO3
DGND
V_REG
Level Translators
XTI
XTO
RMCK
SDA/ CDOUT
SCL/ CCLK
AD1/ CDIN
AD0/ $\overline{\text{CS}}$

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SEP '08
DS692PP1

System Features

- SPI™ or I²C® Software Mode and Stand-Alone Hardware Mode
- Flexible 3-wire Digital Serial Audio Input Port
- Dual Serial Audio Output Ports with Independently Selectable Data Paths
- Master or Slave Mode Operation for all Serial Audio Ports
- Time Division Multiplexing (TDM) Mode
- Integrated Oscillator for use with External Crystal
- Four General-purpose Output Pins (GPO)
- +3.3 V Analog Supply (VA)
- +1.8 V to 5.0 V Digital Interface (VL)
- Space-saving 32-pin QFN Package

General Description

The CS8422 is a 24-bit, high-performance, monolithic CMOS stereo asynchronous sample rate converter with an integrated digital audio interface receiver that decodes audio data according to the EIAJ CP1201, IEC-60958, AES3, and S/PDIF interface standards.

Audio data is input through the digital interface receiver or a 3-wire serial audio input port. Audio is output through one of two 3-wire serial audio output ports. Serial audio data outputs can be set to 24, 20, 18, or 16-bit word-lengths. Data into the digital interface receiver and serial audio input port can be up to 24-bits long. Input and output data can be completely asynchronous, synchronous to an external clock through XTI, or synchronous to the recovered master clock.

The CS8422 can be controlled through the control port in Software Mode or in a Stand-Alone Hardware Mode. In Software Mode, the user can control the device through an SPI or I²C control port.

Target applications include digital recording systems (DVD-R/RW, CD-R/RW, PVR, DAT, MD, and VTR), digital mixing consoles, high-quality D/A, effects processors, computer audio systems, and automotive audio systems.

The CS8422 is available in a space-saving QFN package in both Commercial (-40° C to +85° C) and Automotive (-40° C to +105° C) grades. The CDB4822 is also available for device evaluation and implementation suggestions. Please refer to "Ordering Information" on page 80 for complete details.

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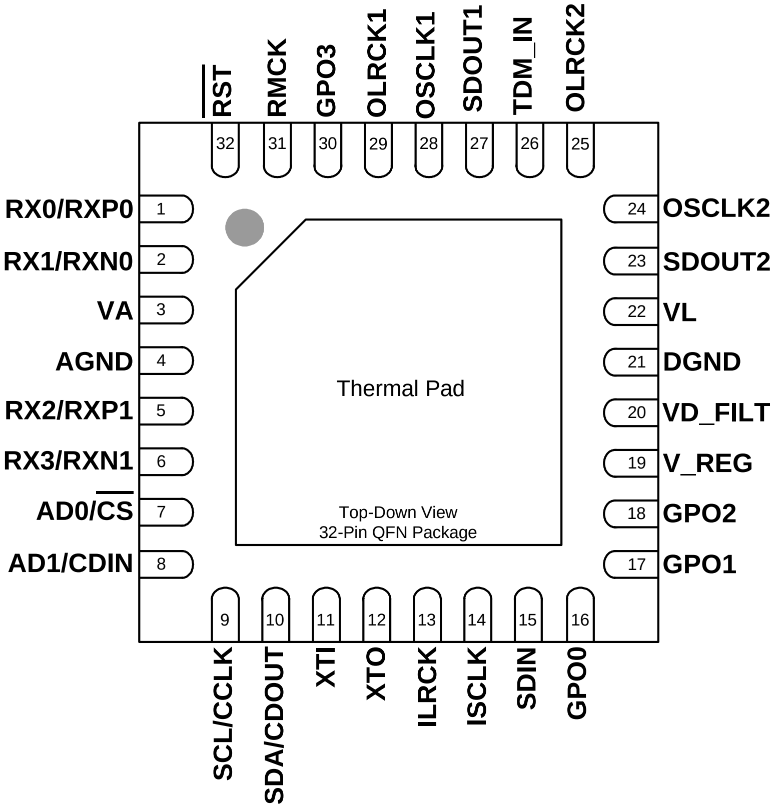
1. PIN DESCRIPTION

1.1 Software Mode


$\overline{RST}$ 32
RMCK 31
GPO3 30
OLRCK1 29
OSCLK1 28
SDOUT1 27
TDM_IN 26
OLRCK2 25
RX0/RXP0 1
RX1/RXN0 2
VA 3
AGND 4
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21 DGND
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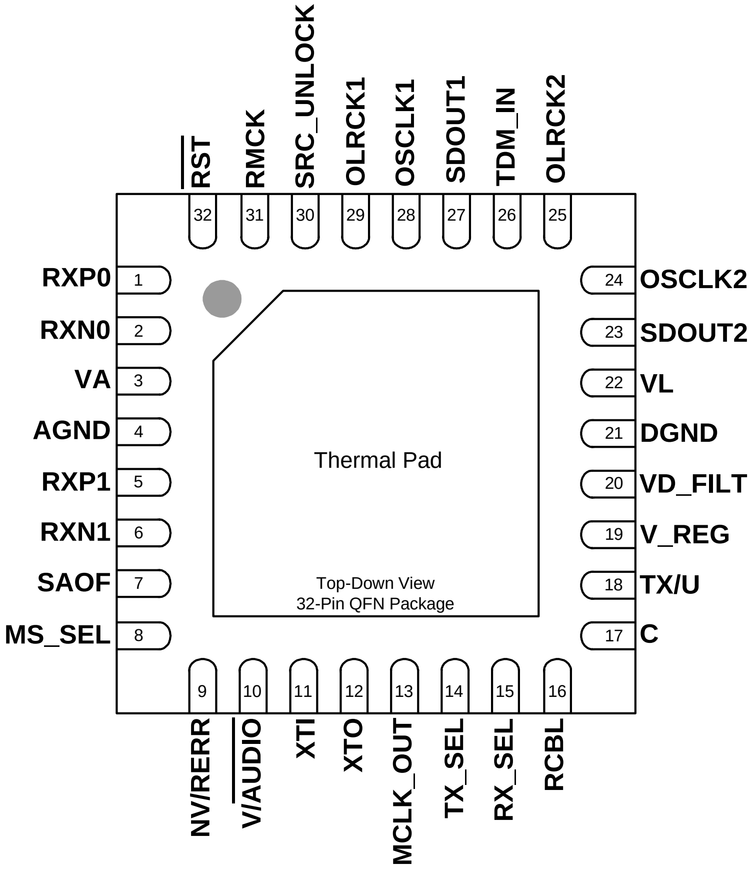
19 V_REG
18 GPO2
17 GPO1
9 SCL/CCLK
10 SDA/CDOUT
11 XTI
12 XTO
13 ILRCK
14 ISCLK
15 SDIN
16 GPO0

Pin Name	Pin #	Pin Description
RX[3:0], RXP/RXN[1:0]	1 2 5 6	**AES3/SPDIF Input** *(Input)* - Single-ended or differential receiver inputs carrying AES3 or S/PDIF encoded digital data. RX[3:0] comprise the single-ended input multiplexer. RXP[1:0] comprise the non-inverting inputs of the differential input multiplexer and RXN[1:0] comprise the inverting inputs of the differential input multiplexer. Unused inputs should be tied to AGND/DGND.
VA	3	**Analog Power** *(Input)* - Analog power supply, nominally +3.3 V. Care should be taken to ensure that this supply is as noise-free as possible, as noise on this pin will directly affect the jitter performance of the recovered clock.
AGND	4	**Analog Ground** *(Input)* - Ground for the analog circuitry in the chip. AGND and DGND should be connected to a common ground area under the chip.
AD0/$\overline{CS}$	7	**Address Bit 0 (I^{2}C) / Software Chip Select (SPI)** *(Input)* - A falling edge on this pin puts the CS8422 into SPI Control Port Mode. With no falling edge, the CS8422 defaults to I^{2}C Mode. In I^{2}C Mode, AD0 is a chip address pin. In SPI Mode, $\overline{CS}$ is used to enable the control port interface on the CS8422. See “Control Port Description” on page 42.
AD1/CDIN	8	**Address Bit 1 (I^{2}C) / Serial Control Data in (SPI)** *(Input)* - In I^{2}C Mode, AD1 is a chip address pin. In SPI Mode, CDIN is the input data line to the control port interface. See “Control Port Description” on page 42.
SCL/CCLK	9	**Software Clock** *(Input)* - Serial control interface clock used to clock control data bits into and out of the CS8422.
SDA/CDOUT	10	**Serial Control Data I/O (I^{2}C) / Data Out (SPI)** *(Input/Output)* - In I^{2}C Mode, SDA is the control I/O data line. In SPI Mode, CDOUT is the output data from the control port interface on the CS8422.

Pin Name	Pin #	Pin Description
XTI	11	**Crystal/Oscillator In** *(Input)* - Crystal or digital clock input for Master clock. See "SRC Master Clock" on page 38 for more details.
XTO	12	**Crystal Out** *(Output)* - Crystal output for Master clock. See "SRC Master Clock" on page 38 for more details.
ILRCK	13	**Serial Audio Input Left/Right Clock** (*Input*/*Output*) - Word rate clock for the audio data on the SDIN pin.
ISCLK	14	**Serial Audio Input Bit Clock** (*Input*/*Output*) - Serial bit clock for audio data on the SDIN pin.
SDIN	15	**Serial Audio Input Data Port** (*Input*) - Audio data serial input pin.
GPO[3:0]	16 17 18 30	**General Purpose Outputs** *(Output)* - See page 50 for details. In I²C Mode, a 20 kΩ pull-up resistor to VL on GPO2 will set AD2 chip address bit to 1, otherwise AD2 will be 0.
V_REG	19	**Voltage Regulator In** (*Input*) - Regulator power supply input, nominally +3.3 V.
VD_FILT	20	**Digital Voltage Regulator** *(Output)* - Digital core voltage regulator output. Should be connected to digital ground through a 10 µF capacitor. Typically +2.5 V. Cannot be used as an external voltage source.
DGND	21	**Digital & I/O Ground** *(Input)* - Ground for the I/O and core logic. AGND and DGND should be connected to a common ground area under the chip.
VL	22	**Logic Power** (*Input*) - Input/Output power supply, typically +1.8 V, +2.5 V, +3.3 V, or +5.0 V.
SDOUT2	23	**Serial Audio Output 2 Data Port** *(Output)* - Audio data serial output 2 pin.
OSCLK2	24	**Serial Audio Output 2 Bit Clock** *(Input/Output)* - Serial bit clock for audio data on the SDOUT2 pin.
OLRCK2	25	**Serial Audio Output 2 Left/Right Clock** (*Input*/*Output*) - Word rate clock for the audio data on the SDOUT2 pin.
TDM_IN	26	**Serial Audio Output 1 TDM Input** (*Input*) - Time Division Multiplexing serial audio data input. Should remain grounded when not used. See "Time Division Multiplexing (TDM) Mode" on page 27.
SDOUT1	27	**Serial Audio Output 1 Data Port** (*Output*) - Audio data serial output 1 pin.
OSCLK1	28	**Serial Audio Output 1 Bit Clock** (*Input*/*Output*) - Serial bit clock for audio data on the SDOUT 1 pin.
OLRCK1	29	**Serial Audio Output 1 Left/Right Clock** (*Input*/*Output*) - Word rate clock for the audio data on the SDOUT 1 pin.
RMCK	31	**Recovered Master Clock** *(Output)* - Recovered master clock from the PLL. Frequency is 128x, 192x, 256x, 384x, 512x, 768x, or 1024x Fs, where Fs is the sample rate of the incoming AES3-compatible data, or ISCLK/64.
$\overline{\text{RST}}$	32	**Reset** *(Input)* - When $\overline{\text{RST}}$ is low the CS8422 enters a low power mode and all internal states are reset. On initial power up $\overline{\text{RST}}$ must be held low until the power supply is stable and all input clocks are stable in frequency and phase.
THERMAL PAD	-	**Thermal Pad** - Thermal relief pad. Should be connected to the ground plane for optimized heat dissipation.

1.2 Hardware Mode


$\overline{\text{RST}}$
RMCK
SRC_UNLOCK
OLRCK1
OSCLK1
SDOUT1
TDM_IN
OLRCK2
32
31
30
29
28
27
26
25
RXP0
RXN0
VA
AGND
RXP1
RXN1
SAOF
MS_SEL
1
2
3
4
5
6
7
8
24
23
22
21
20
19
18
17
OSCLK2
SDOUT2
VL
DGND
VD_FILT
V_REG
TX/U
C
Thermal Pad
Top-Down View
32-Pin QFN Package
9
10
11
12
13
14
15
16
NV/RERR
V/$\overline{\text{AUDIO}}$
XTI
XTO
MCLK_OUT
TX_SEL
RX_SEL
RCBL

Pin Name	Pin #	Pin Description
RXP/RXN[1:0]	1 2 5 6	**AES3/SPDIF Input** *(Input)* - Differential receiver inputs carrying AES3 or S/PDIF encoded digital data. RXP[1:0] comprise the non-inverting inputs of the differential input multiplexer; and RXN[1:0] comprise the inverting inputs of the input multiplexer. Unused inputs should be tied to AGND.
VA	3	**Analog Power** *(Input)* - Analog power supply, nominally +3.3 V. Care should be taken to ensure that this supply is as noise-free as possible, as noise on this pin will directly affect the jitter performance of the recovered clock.
AGND	4	**Analog Ground** *(Input)* - Ground for the analog circuitry in the chip. AGND and DGND should be connected to a common ground area under the chip.
SAOF	7	**Serial Audio Output Format Select** *(Input)* - Used to select the serial audio output format after reset. See Table 4 on page 41 for format settings.
MS_SEL	8	**Master/Slave Select** *(Input)* - Used to select Master or Slave settings for the input and output serial audio ports after reset. See Table 5 on page 41 for format settings.
NV/RERR	9	**Non-Validity Receiver Error/Receiver Error** *(Output)* - Receiver error indicator. NVERR is output by default, RERR is selected by a 20 kΩ resistor to VL.
V/$\overline{\text{AUDIO}}$	10	**Validity Data/$\overline{\text{AUDIO}}$** (*Output*) - If a 20 kΩ pull-down is present on this pin, it will output serial Validity data from the AES3 receiver, clocked by the rising and falling edges of OLRCK2 in master mode. If a 20 kΩ pull-up is present, the pin will be low when valid linear PCM data is present at the AES3 input.
XTI	11	**Crystal/Oscillator In** *(Input)* - Crystal or digital clock input for Master clock. See "SRC Master Clock" on page 38.
XTO	12	**Crystal Out** *(Output)* - Crystal output for Master clock. See "SRC Master Clock" on page 38.

Pin Name	Pin #	Pin Description
MCLK_OUT	13	**Buffered MCLK** *(Output)* **-** Buffered output of XTI clock. If a 20 kΩ pull-up resistor to VL is present on this pin, the SRC MCLK source will be the PLL clock, otherwise it will be the ring oscillator.
TX_SEL	14	**TX Pin MUX Selection** *(Input)* - Used to select the AES3-compatible receiver input for pass-through to the TX pin.
RX_SEL	15	**Receiver MUX Selection** *(Input)* - Used to select the active AES3-compatible receiver input.
RCBL	16	**Receiver Channel Status Block** *(Output)* -Indicates the beginning of a received channel status block. Will go high for one subframe during each Z preamble following the first detected Z preamble. If no Z preamble is detected, output is indeterminate. See Figure 19 on page 36 for more detail.
C	17	**Channel Status Data** (*Output*) - Serial channel status data output from the AES3-compatible receiver, clocked by the rising and falling edges of OLRCK2 in master mode. A 20 kΩ pull-up resistor to VL must be present on this pin to put the part in Hardware Mode.
TX/U	18	**Receiver MUX Pass-through/User Data** (*Output*) - If no 20 kΩ pull-up resistor is present on this pin it will output a copy of the receiver mux input selected by the TX_SEL pin. If a 20 kΩ pull-up resistor to VL is present on this pin, it will output serial User data from the AES3 receiver, clocked by the rising and falling edges of OLRCK2 in master mode.
V_REG	19	**Voltage Regulator In** (*Input*) - Regulator power supply input, nominally +3.3 V.
VD_FILT	20	**Digital Voltage Regulator Out** *(Output)* - Digital core voltage regulator output. Should be connected to digital ground through a 10 µF capacitor. Cannot be used as an external voltage source.
DGND	21	**Digital & I/O Ground** *(Input)* - Ground for the I/O and core logic. AGND and DGND should be connected to a common ground area under the chip.
VL	22	**Logic Power** (*Input*) - Input/Output power supply, typically +1.8 V, +2.5 V, +3.3 V, or +5.0 V.
SDOUT2	23	**Serial Audio Output 2 Data Port** *(Output)* - Audio data serial output 2 pin.
OSCLK2	24	**Serial Audio Output 2 Bit Clock** *(Input/Output)* - Serial bit clock for audio data on the SDOUT2 pin.
OLRCK2	25	**Serial Audio Output 2 Left/Right Clock** *(Input/Output)* - Word rate clock for the audio data on the SDOUT2 pin.
TDM_IN	26	**Serial Audio Output 1 TDM Input** *(Input)* - Time Division Multiplexing serial audio data input. Grounded when not used. See “Time Division Multiplexing (TDM) Mode” on page 27 for details.
SDOUT1	27	**Serial Audio Output 1 Data Port** *(Output)* - Audio data serial output 1 pin. A 20 kΩ pull-up to VL present on this pin will disable de-emphasis auto detect.
OSCLK1	28	**Serial Audio Output 1 Bit Clock** *(Input/Output)* - Serial bit clock for audio data on the SDOUT1 pin.
OLRCK1	29	**Serial Audio Output 1 Left/Right Clock** *(Input/Output)* - Word rate clock for the audio data on the SDOUT1 pin.
SRC_UNLOCK	30	**SRC Unlock Indicator** (*Output*) - Indicates when the SRC is unlocked. See “SRC Locking” on page 37 for more details.
RMCK	31	**Recovered Master Clock** *(Output)* **-** Recovered master clock from the PLL. Frequency is 128 x, 256 x, or 512 x Fs, where Fs is the sample rate of the incoming AES3-compatible data or ISCLK/64. If a 20 kΩ pull-up to VL is present on this pin, the SDOUT2 MCLK source will be RMCK, otherwise it will be the clock input through XTI-XTO.
$\overline{\text{RST}}$	32	**Reset** *(Input)* - When $\overline{\text{RST}}$ is low the CS8422 enters a low power mode and all internal states are reset. On initial power up $\overline{\text{RST}}$ must be held low until the power supply is stable and all input clocks are stable in frequency and phase.
THERMAL PAD	-	**Thermal Pad** - Thermal relief pad. Should be connected to the ground plane for optimized heat dissipation.

2. CHARACTERISTICS AND SPECIFICATIONS

(All Min/Max characteristics and specifications are guaranteed over the Specified Operating Conditions. Typical performance characteristics and specifications are derived from measurements taken at nominal supply voltages and T_A = 25° C.)

RECOMMENDED OPERATING CONDITIONS

GND = 0 V, all voltages with respect to 0 V.

Parameter		Symbol	Min	Nominal	Max	Units
Power Supply Voltage		VL VA V_REG	1.71 3.135 3.135	3.3 3.30 3.30	5.25 3.465 3.465	V V V
Ambient Operating Temperature:	Commercial Grade Automotive Grade	T_A	-40 -40	- -	+85 +105	°C °C

ABSOLUTE MAXIMUM RATINGS

DGND = AGND = 0 V; all voltages with respect to 0 V. Operation beyond these limits may result in permanent damage to the device. Normal operation is not guaranteed at these extremes.

Parameter	Symbol	Min	Max	Units
Power Supply Voltage	VL VA V_REG	-0.3 -0.3 -0.3	6.0 4.3 4.3	V V V
Input Current, Any Pin Except Supplies (Note 1)	I_{in}	-	±10	mA
Input Voltage, Any Pin Except RXP[1:0], RXN[1:0], or RX[3:0]	V_{in}	-0.3	VL+0.4	V
Input Voltage, RXP[1:0], RXN[1:0], or RX[3:0]	V_{in}	-0.3	VA+0.4	V
Ambient Operating Temperature (power applied)	T_A	-55	+125	°C
Storage Temperature	T_{stg}	-65	+150	°C

Notes:

1. Transient currents of up to 100 mA will not cause SCR latch-up.

PERFORMANCE SPECIFICATIONS - SAMPLE RATE CONVERTER

XTI-XTO = 24.576 MHz; Input signal = 1.000 kHz, Measurement Bandwidth = 20 to Fso/2 Hz, and Word Width = 24-Bits. (Note 2)

Parameter		Min	Typ	Max	Units
Resolution		16	-	24	bits
Sample Rate	Slave Master	XTI/2048 XTI/512	- -	XTI/128 XTI/128	kHz kHz
Sample Rate Ratio - Upsampling		-	-	1:6	Fsi:Fso
Sample Rate Ratio - Downsampling		-	-	6:1	Fsi:Fso
Interchannel Gain Mismatch		-	0.0	-	dB
Interchannel Phase Deviation		-	0.0	-	Degrees
Gain Error		-0.2	-	0	dB
Peak Idle Channel Noise Component		-	-	-144	dBFS
Dynamic Range - Unweighted (20 Hz to Fso/2, -60 dBFS Input)					
32 kHz:48 kHz		-	140	-	dB
44.1 kHz:48 kHz		-	141	-	dB
44.1 kHz:192 kHz		-	138	-	dB
48 kHz:44.1 kHz		-	140	-	dB
48 kHz:96 kHz		-	141	-	dB
96 kHz:48 kHz		-	140	-	dB
192 kHz:32 kHz		-	141	-	dB
Total Harmonic Distortion + Noise (20 Hz to Fso/2, 0 dBFS Input)					
32 kHz:48 kHz		-	-134	-	dB
44.1 kHz:48 kHz		-	-134	-	dB
44.1 kHz:192 kHz		-	-133	-	dB
48 kHz:44.1 kHz		-	-131	-	dB
48 kHz:96 kHz		-	-135	-	dB
96 kHz:48 kHz		-	-136	-	dB
192 kHz:32 kHz		-	-137	-	dB

Notes:

2. Fsi indicates the input sample rate. Fso indicates the output sample rate. Numbers separated by a colon indicate the ratio of Fsi to Fso.

DIGITAL FILTER CHARACTERISTICS

Parameter	Min	Typ	Max	Units
Passband (Upsampling or Downsampling)	-	-	0.4535* min(Fsi,Fso)	Fs
Passband Ripple	-	-	± 0.05	dB
Stopband (Downsampling)	0.5465*Fso	-	-	Fs
Stopband Attenuation	125	-	-	dB
Group Delay	See "Group Delay" on page 69			

DC ELECTRICAL CHARACTERISTICS

AGND = DGND = 0 V; all voltages with respect to 0 V.

Parameter		Min	Typ	Max	Units
Power-Down Mode (Note 3)					
Supply Current in power down	VA	-	4.7	-	µA
	V_REG	-	1	-	µA
	VL = 1.8 V	-	0.3	-	µA
	VL = 2.5 V	-	7.1	-	µA
	VL = 3.3 V	-	16.9	-	µA
	VL = 5.0 V	-	102.6	-	µA
Normal Operation (Note 4)					
Supply Current at 48 kHz Fsi and Fso	VA	-	7.6	-	mA
	V_REG	-	9.4	-	mA
	VL = 1.8 V	-	2.7	-	mA
	VL = 2.5 V	-	3.8	-	mA
	VL = 3.3 V	-	5.2	-	mA
	VL = 5.0 V	-	24	-	mA
Supply Current at 192 kHz Fsi and Fso	VA	-	32.4	-	mA
	V_REG	-	18.9	-	mA
	VL = 1.8 V	-	6.2	-	mA
	VL = 2.5 V	-	8.8	-	mA
	VL = 3.3 V	-	12	-	mA
	VL = 5.0 V	-	50.4	-	mA

Notes:

3. Power-Down Mode is defined as $\overline{\text{RST}}$ = LOW with all clocks and data lines held static and no crystal attached across XTI - XTO.
4. Normal operation is defined as $\overline{\text{RST}}$ = HIGH. The typical values shown were measured with the digital interface receiver in differential mode, serial audio output port 1 in master mode sourced by the SRC, and serial audio output port 2 in master mode sourced by the AES3 receiver output.

DIGITAL INTERFACE SPECIFICATIONS

AGND = DGND = 0 V; all voltages with respect to 0 V.

Parameter	Symbol	Min	Typ	Max	Units
Input Leakage Current (Note 5)	I_{in}	-	-	+32	µA
Input Capacitance	I_{in}	-	8	-	pF
Digital Interface Receiver - RXP[1:0], RXN[1:0], RX[3:0]					
Differential Input Sensitivity, RXP to RXN (Note 6)		-	-	200	mVpp
Differential Input Impedance, RXP and RXN to GND		-	11	-	kΩ
Single-Ended Input Sensitivity, RX pins, Receiver Input Mode 1 (Note 6)		-	-	200	mVpp
Single-Ended Input Impedance, RX pins, Receiver Input Mode 1		-	11	-	kΩ
High-Level Input Voltage, RX pins in Digital mode	V_{IH}	0.55xVA	-	VA+0.3	V
Low-Level Input Voltage, RX pins in Digital mode	V_{IL}	-0.3	-	0.8	V
Digital I/O					
High-Level Output Voltage (I_{OH} = -4 mA)	V_{OH}	.77xVL	-	-	V
Low-Level Output Voltage (I_{OL} = 4 mA)	V_{OL}	-	-	0.6	V
High-Level Input Voltage	V_{IH}	0.65xVL	-	-	V
Low-Level Input Voltage	V_{IL}	-	-	0.3xVL	V
Input Hysteresis		-	0.2	-	V

Notes:

5. When a digital signal is sent to the AES RX pins, the pins will draw approximately 730 µA from the digital signal's supply from the time reset is de-asserted until the RX_MODE, RX_SEL, and INPUT_TYPE bits in register 03h are properly configured to allow a digital input signal on the driven pins, see Section 11.3 on page 48.
6. Maximum sensitivity in accordance with AES3-2003 section 8.3.3. Measured with eye diagram height at the specified voltage and width of at least 50% of one-half the biphase symbol period.

SWITCHING SPECIFICATIONS

Inputs: Logic 0 = 0 V, Logic 1 = VL; C_L = 20 pF.

Parameter	Symbol	Min	Typ	Max	Units
$\overline{\text{RST}}$ pin Low Pulse Width (Note 7)		1	-	-	ms
PLL Clock Recovery Sample Rate Range (Note 8)		28	-	216	kHz
RMCK Output Jitter (Note 9) Differential RX Mode Single-Ended RX Mode		- -	200 475	- -	ps RMS ps RMS
RMCK Output Duty Cycle		45	50	55	%
XTI Frequency Crystal Digital Clock Source		12 1.024	- -	27.000 49.152	MHz MHz
XTI Pulse Width High/Low		9	-	-	ns
MCLK_OUT Duty Cycle		45	-	55	%
VL = 3.3 V, 5 V					
RMCK Output Frequency		-	-	49.152	MHz
MCLK_OUT Frequency		-	-	49.152	MHz
Slave Mode					
ISCLK Frequency		-	-	49.152	MHz
ISCLK High Time	t_{sckh}	9.2	-	-	ns
ISCLK Low Time	t_{sckl}	9.2	-	-	ns
OSCLK Frequency		-	-	26.9	MHz
OSCLK High Time	t_{sckh}	16.7	-	-	ns
OSCLK Low Time	t_{sckl}	16.7	-	-	ns
I/OLRCK Edge to I/OSCLK Rising Edge	t_{lcks}	5.7	-	-	ns
I/OSCLK Rising Edge to I/OLRCK Edge	t_{lckd}	4.2	-	-	ns
OSCLK Falling Edge/OLRCK Edge to SDOUT Output Valid	t_{dpd}	-	-	13.7	ns
SDIN/TDM_IN Setup Time Before I/OSCLK Rising Edge	t_{ds}	2.2	-	-	ns
SDIN/TDM_IN Hold Time After I/OSCLK Rising Edge	t_{dh}	5.5	-	-	ns
TDM Mode OLRCK High Time (Note 10)	t_{lrckh}	20	-	-	ns
TDM Mode OLRCK Rising Edge to OSCLK Rising Edge	t_{fss}	5.3	-	-	ns
TDM Mode OSCLK Rising Edge to OLRCK Falling Edge	t_{fsh}	4.2	-	-	ns
Master Mode					
I/OSCLK Frequency (non-TDM Mode)		48*Fsi/o	-	128*Fsi/o	MHz
I/OLRCK Duty Cycle		49.5	-	50.5	%
I/OSCLK Duty Cycle		45	-	55	%
I/OSCLK Falling Edge to I/OLRCK Edge	t_{lcks}	-	-	4.2	ns
OSCLK Falling Edge to SDOUT Output Valid	t_{dpd}	-	-	4.6	ns

Parameter	Symbol	Min	Typ	Max	Units
SDIN/TDM_IN Setup Time Before I/OSCLK Rising Edge	t_{ds}	2.2	-	-	ns
SDIN/TDM_IN Hold Time After I/OSCLK Rising Edge	t_{dh}	5.5	-	-	ns
TDM Mode OSCLK Frequency (Note 11)		-	-	49.152	MHz
TDM Mode OSCLK Falling Edge to OLRCK Edge	t_{fsm}	-	-	4.2	ns
VL = 1.8 V, 2.5 V					
RMCK Output Frequency		-	-	31	MHz
MCLK_OUT Frequency		-	-	31	MHz
Slave Mode					
ISCLK Frequency		-	-	49.152	MHz
ISCLK High Time	t_{sckh}	9.2	-	-	ns
ISCLK Low Time	t_{sckl}	9.2	-	-	ns
OSCLK Frequency		-	-	15.7	MHz
OSCLK High Time	t_{sckh}	28.7	-	-	ns
OSCLK Low Time	t_{sckl}	28.7	-	-	ns
I/OLRCK Edge to I/OSCLK Rising Edge	t_{lcks}	7.4	-	-	ns
I/OSCLK Rising Edge to I/OLRCK Edge	t_{lckd}	6.2	-	-	ns
OSCLK Falling Edge/OLRCK Edge to SDOUT Output Valid	t_{dpd}	-	-	25.6	ns
SDIN/TDM_IN Setup Time Before I/OSCLK Rising Edge	t_{ds}	4.7	-	-	ns
SDIN/TDM_IN Hold Time After I/OSCLK Rising Edge	t_{dh}	7.3	-	-	ns
TDM Mode OLRCK High Time (Note 10)	t_{lrckh}	20	-	-	ns
TDM Mode OLRCK Rising Edge to OSCLK Rising Edge	t_{fss}	7.0	-	-	ns
TDM Mode OSCLK Rising Edge to OLRCK Falling Edge	t_{fsh}	6.2	-	-	ns
Master Mode					
I/OSCLK Frequency (non-TDM Mode)		48*Fsi/o	-	128*Fsi/o	MHz
I/OLRCK Duty Cycle		45	-	55	%
I/OSCLK Duty Cycle		45	-	55	%
I/OSCLK Falling Edge to I/OLRCK Edge	t_{lcks}	-	-	5.7	ns
OSCLK Falling Edge to SDOUT Output Valid	t_{dpd}	-	-	5.4	ns
SDIN/TDM_IN Setup Time Before I/OSCLK Rising Edge	t_{ds}	4.7	-	-	ns
SDIN/TDM_IN Hold Time After I/OSCLK Rising Edge	t_{dh}	7.3	-	-	ns
TDM Mode OSCLK Frequency (Note 11)		-	-	31	MHz
TDM Mode OSCLK Falling Edge to OLRCK Edge	t_{fsm}	-	-	5.7	ns

Notes:

7. After powering up the CS8422, $\overline{\text{RST}}$ should be held low until the power supplies and clocks are settled.
8. If ISCLK is selected as the clock source for the PLL, then the Sample Rate = ISCLK/64.

9. Typical base band jitter in accordance with AES-12id-2006 section 3.4.2. Measurements are Time Interval Error (TIE) taken with 3rd order 100 Hz to 40 kHz band-pass filter. Measured with Sample Rate = 48 kHz.
10. OLRCK must remain high for at least 1 OSCLK period and at most 255 OSCLK periods in TDM Mode.
11. In TDM formatted master mode, the OSCLK frequency is fixed at 256*OLRCK.

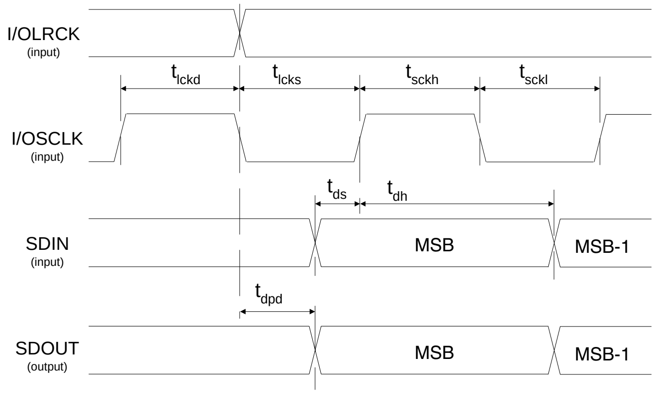

I/OLRCK
(input)
t_{lckd}
t_{lcks}
t_{sckh}
t_{sckl}
I/OSCLK
(input)
t_{ds}
t_{dh}
SDIN
(input)
MSB
MSB-1
t_{dpd}
SDOUT
(output)
MSB
MSB-1

Figure 1. Non-TDM Slave Mode Timing

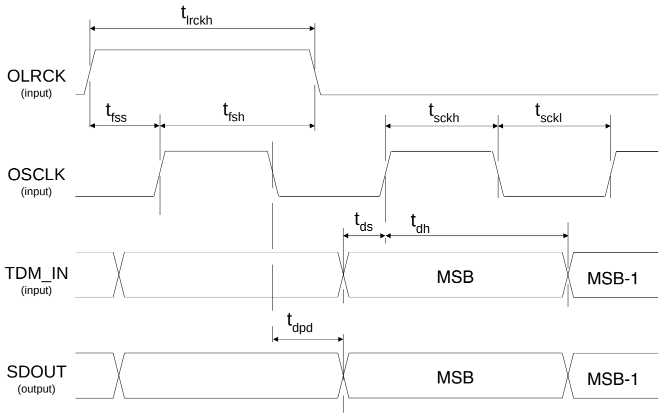

t_{lrckh}
OLRCK
(input)
t_{fss}
t_{fsh}
t_{sckh}
t_{sckl}
OSCLK
(input)
t_{ds}
t_{dh}
TDM_IN
(input)
MSB
MSB-1
t_{dpd}
SDOUT
(output)
MSB
MSB-1

Figure 2. TDM Slave Mode Timing

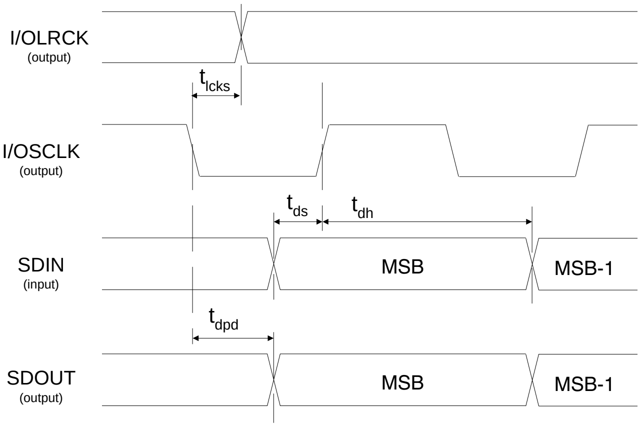

I/OLRCK
(output)
t_{lcks}
I/OSCLK
(output)
t_{ds}
t_{dh}
SDIN
(input)
MSB
MSB-1
t_{dpd}
SDOUT
(output)
MSB
MSB-1

Figure 3. Non-TDM Master Mode Timing

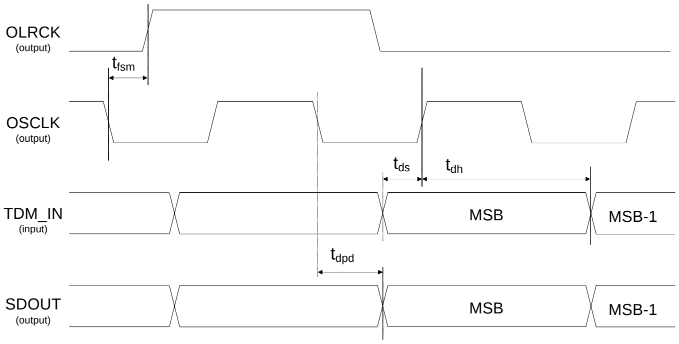

OLRCK
(output)
t_{fsm}
OSCLK
(output)
t_{ds}
t_{dh}
TDM_IN
(input)
MSB
MSB-1
t_{dpd}
SDOUT
(output)
MSB
MSB-1

Figure 4. TDM Master Mode Timing

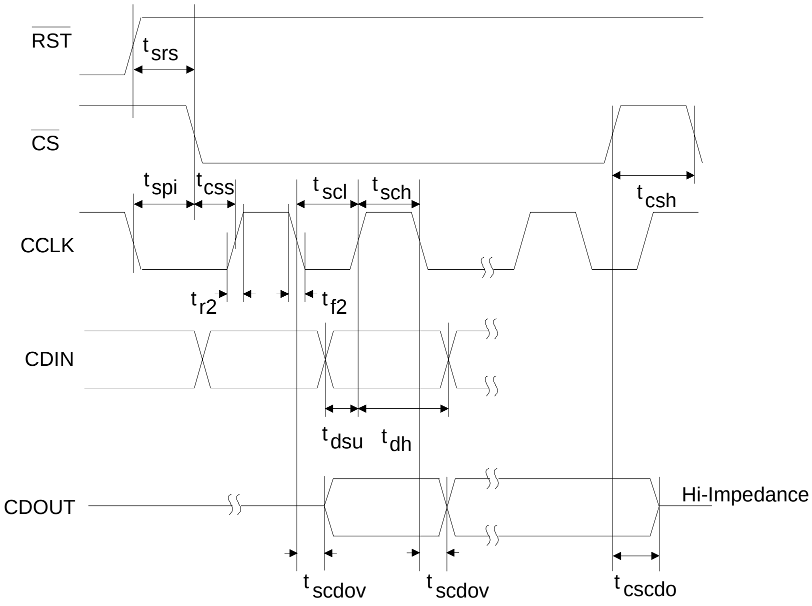
SWITCHING CHARACTERISTICS - CONTROL PORT - SPI MODE

Inputs: Logic 0 = 0 V, Logic 1 = VL; C_L = 20 pF.

Parameter	Symbol	Min	Max	Unit
CCLK Clock Frequency	f_{sck}	0	6.0	MHz
$\overline{\text{RST}}$ Rising Edge to $\overline{\text{CS}}$ Falling	t_{srs}	500	-	µs
CCLK Edge to $\overline{\text{CS}}$ Falling (Note 12)	t_{spi}	500	-	ns
$\overline{\text{CS}}$ High Time Between Transmissions	t_{csh}	1.0	-	µs
$\overline{\text{CS}}$ Falling to CCLK Edge	t_{css}	20	-	ns
CCLK Low Time	t_{scl}	66	-	ns
CCLK High Time	t_{sch}	66	-	ns
CDIN to CCLK Rising Setup Time	t_{dsu}	40	-	ns
CCLK Rising to DATA Hold Time (Note 13)	t_{dh}	15	-	ns
CCLK Falling to CDOUT Valid (Note 14)	t_{scdov}	-	100	ns
Time from $\overline{\text{CS}}$ Rising to CDOUT High-Z	t_{cscdo}	-	100	ns
CDOUT Rise Time	t_{r1}	-	25	ns
CDOUT Fall Time	t_{f1}	-	25	ns
CCLK and CDIN Rise Time (Note 15)	t_{r2}	-	100	ns
CCLK and CDIN Fall Time (Note 15)	t_{f2}	-	100	ns

Notes:

12. t_{spi} only needed before first falling edge of $\overline{\text{CS}}$ after $\overline{\text{RST}}$ rising edge. t_{spi} = 0 at all other times.
13. Data must be held for sufficient time to bridge the transition time of CCLK.
14. CDOUT should *not* be sampled during this time.
15. For f_{sck} < 1 MHz.



$\overline{\text{RST}}$
t_{srs}
$\overline{\text{CS}}$
t_{spi}
t_{css}
t_{scl}
t_{sch}
t_{csh}
CCLK
t_{r2}
t_{f2}
CDIN
t_{dsu}
t_{dh}
CDOUT
Hi-Impedance
t_{scdov}
t_{scdov}
t_{cscdo}

Figure 5. SPI Mode Timing

SWITCHING CHARACTERISTICS - CONTROL PORT - I²C MODE

Inputs: Logic 0 = 0 V, Logic 1 = VL; C_L = 20 pF.

Parameter	Symbol	Min	Max	Unit
SCL Clock Frequency	f_{scl}	-	100	kHz
$\overline{\text{RST}}$ Rising Edge to Start	t_{irs}	500	-	µs
Bus Free Time Between Transmissions	t_{buf}	4.7	-	µs
Start Condition Hold Time (prior to first clock pulse)	t_{hdst}	4.0	-	µs
Clock Low time	t_{low}	4.7	-	µs
Clock High Time	t_{high}	4.0	-	µs
Setup Time for Repeated Start Condition	t_{sust}	4.7	-	µs
SDA Hold Time from SCL Falling (Note 16)	t_{hdd}	10	-	ns
SDA Setup time to SCL Rising	t_{sud}	250	-	ns
Rise Time of SCL and SDA	t_{rc}, t_{rd}	-	1000	ns
Fall Time SCL and SDA	t_{fc}, t_{fd}	-	300	ns
Setup Time for Stop Condition	t_{susp}	4.7	-	µs
Acknowledge Delay from SCL Falling	t_{ack}	300	1000	ns

Notes:

16. Data must be held for sufficient time to bridge the transition time, t_{fc}, of SCL.

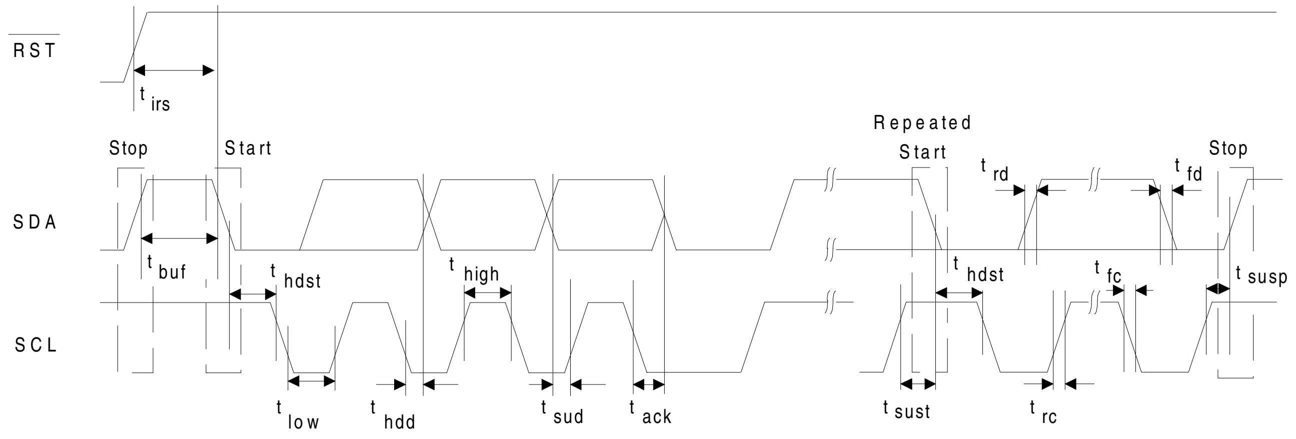

RST
t irs
Stop
Start
SDA
SCL
t buf
t hdst
t high
t low
t hdd
t sud
t ack
Repeated Start
t rd
t fd
Stop
t hdst
t fc
t susp
t sust
t rc

Figure 6. I²C Mode Timing

3. TYPICAL CONNECTION DIAGRAMS

3.1 Software Mode

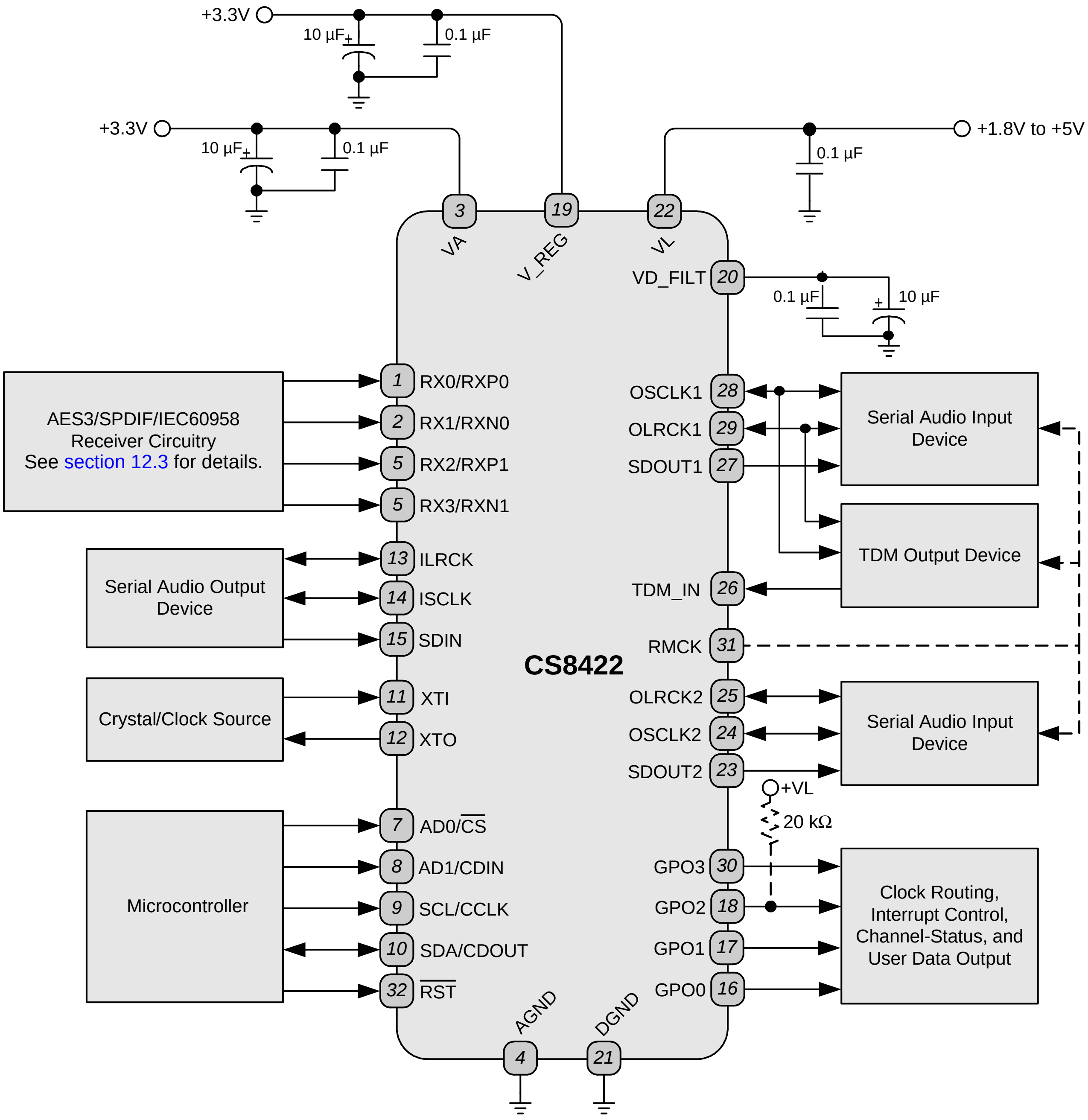

+3.3V
10 µF
+
0.1 µF
+3.3V
10 µF
+
0.1 µF
+1.8V to +5V
0.1 µF
3
19
22
VA
V_REG
VL
VD_FILT
20
0.1 µF
+
10 µF
AES3/SPDIF/IEC60958
Receiver Circuitry
See section 12.3 for details.
1 RX0/RXP0
2 RX1/RXN0
5 RX2/RXP1
5 RX3/RXN1
OSCLK1 28
OLRCK1 29
SDOUT1 27
Serial Audio Input
Device
TDM Output Device
Serial Audio Output
Device
13 ILRCK
14 ISCLK
15 SDIN
TDM_IN 26
RMCK 31
CS8422
Crystal/Clock Source
11 XTI
12 XTO
OLRCK2 25
OSCLK2 24
SDOUT2 23
Serial Audio Input
Device
+VL
20 kΩ
Microcontroller
7 AD0/CS
8 AD1/CDIN
9 SCL/CCLK
10 SDA/CDOUT
32 RST
GPO3 30
GPO2 18
GPO1 17
GPO0 16
Clock Routing,
Interrupt Control,
Channel-Status, and
User Data Output
AGND
DGND
4
21

Figure 7. Typical Connection Diagram, Software Mode

3.2 Hardware Mode

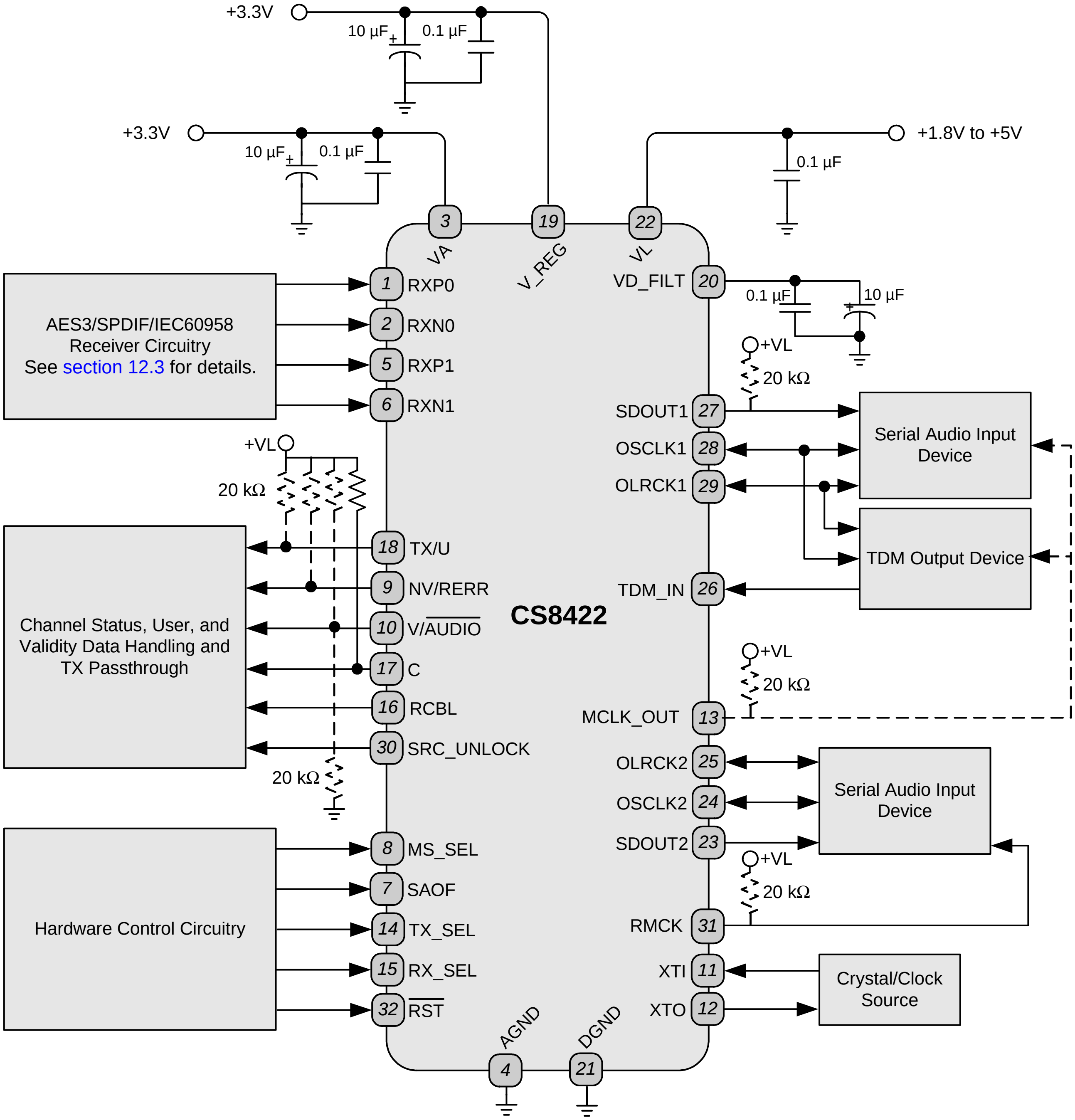

+3.3V
10 µF
0.1 µF
+3.3V
10 µF
0.1 µF
+1.8V to +5V
0.1 µF
3
19
22
VA
V_REG
VL
VD_FILT
20
0.1 µF
10 µF
AES3/SPDIF/IEC60958
Receiver Circuitry
See section 12.3 for details.
1 RXP0
2 RXN0
5 RXP1
6 RXN1
+VL
20 kΩ
SDOUT1 27
OSCLK1 28
OLRCK1 29
Serial Audio Input Device
TDM Output Device
TDM_IN 26
+VL
20 kΩ
18 TX/U
9 NV/RERR
10 V/AUDIO
17 C
16 RCBL
30 SRC_UNLOCK
20 kΩ
Channel Status, User, and Validity Data Handling and TX Passthrough
CS8422
+VL
20 kΩ
MCLK_OUT 13
OLRCK2 25
OSCLK2 24
SDOUT2 23
Serial Audio Input Device
+VL
20 kΩ
RMCK 31
XTI 11
XTO 12
Crystal/Clock Source
Hardware Control Circuitry
8 MS_SEL
7 SAOF
14 TX_SEL
15 RX_SEL
32 RST
AGND
DGND
4
21

Figure 8. Typical Connection Diagram, Hardware Mode

4. OVERVIEW

The CS8422 is a 24-bit, high performance, monolithic CMOS stereo asynchronous sample rate converter with integrated digital audio interface receiver that decodes audio data according to EIAJ CP1201, IEC-60958, AES3, and S/PDIF interface standards.

Audio data is input through either a 3-wire serial audio port or the AES3-compatible digital interface receiver. Audio data is output through one of two 3-wire serial audio output ports. The serial audio ports are capable of 24, 20, 18, or 16-bit word lengths. Data in to the digital interface receiver can be up to 24-bit. Input and output data can be completely asynchronous, synchronous to an external data clock through XTI, or synchronous to the master clock recovered from the incoming S/PDIF or AES3 data.

CS8422 can be controlled either in Software Mode or in a stand-alone Hardware Mode. In Software Mode, the user can control the device through either a SPI or I²C control port.

Target applications include digital recording systems (DVD-R/RW, CD-R/RW, PVR, DAT, MD, and VTR), digital mixing consoles, high quality D/A, effects processors, computer audio systems, and automotive audio systems.

Figure 7 and Figure 8 show typical connections to the CS8422.

5. THREE-WIRE SERIAL INPUT/OUTPUT AUDIO PORT

The CS8422 provides two independent 3-wire serial audio output ports, and a 3-wire serial audio input (only available in Software Mode). The interface format should be chosen to suit the attached device either through the control port in Software Mode, or through the MS_SEL and SAOF pins in Hardware Mode. The following parameters are adjustable:

Hardware Mode

- Master or slave mode operation
- Master-mode MCLK-to-OLRCK (OLRCK1 and OLRCK2) ratios: 128, 256, and 512
- Audio data resolution of 16, 20, or 24-bits
- Left-Justified, I²S, or Right-Justified serial data formats
- Multi-channel TDM serial audio format (Serial Audio Output 1 only)

Software Mode

- Master or slave mode operation
- Master-mode MCLK-to-ILRCK and MCLK-to-OLRCK (OLRCK1 and OLRCK2) ratios: 64, 128, 192, 256, 384, 512, 768, and 1024
- Audio data resolution of 16, 18, 20, or 24-bits
- Left-Justified, I²S, or Right-Justified serial data formats
- Multi-channel TDM serial audio format
- AES3 Direct Output format

Figures 9, 10, 11, and 12 show the standard input/output formats available. The TDM serial audio format is described in Section 5.1.5 on page 27. For more information about serial audio formats, refer to the Cirrus Logic applications note AN282, “The 2-Channel Serial Audio Interface: A Tutorial”, available at *www.cirrus.com.*

5.1 Serial Port Clock Operation

5.1.1 Master Mode

When a serial port is set to master mode, its left/right clock (ILRCK, OLRCK1, or OLRCK2), and its serial bit-clock (ISCLK, OSCLK1, or OSCLK2) are outputs. If a serial output is sourced directly by the AES3 receiver, then that serial port's left/right clock and serial bit-clock will be synchronous with RMCK. If a serial port is routed to or from the sample rate converter (SRC), then that serial port's left/right clock and serial bit-clock can be synchronous with either the XTI-XTO or RMCK when it is in master mode.

If a serial output is source directly by the serial input port without the use of the SRC, then all associated clocks must be synchronous, so both serial ports must use the same master clock source. It is for this reason that, when in this mode, the serial output clock control is done through the Serial Audio Input Clock Control (07h) register.

5.1.2 Slave Mode

When a serial port is in slave mode, its left/right clock (ILRCK, OLRCK1, or OLRCK2), and its serial bit-clock (ISCLK, OSCLK1, or OSCLK2) are inputs. If the serial input or a serial output has the SRC in its data path, then the serial port's LRCK and SCLK may be asynchronous to all other serial ports. The left/right clock should be continuous, but the duty cycle can be less than 50% if enough serial clocks are present in each associated LRCK phase to clock all of the data bits.

If there are fewer SCLK periods than required to clock all the bits present in one half LRCK period in Left-Justified and I²S Modes, data will be truncated beginning with the LSB. In Right-Justified Modes, the data will be invalid.

If a serial audio output is operated in slave mode and sourced directly by the AES3 receiver or the serial input port without the use of the sample rate converter, then the OLRCK supplied to the serial audio output should be synchronous to Fsi or ILRCK to avoid skipped or repeated samples. The OSLIP bit ("Interrupt Status (14h)" on page 59) is provided to indicate when skipped or repeated samples occur.

If the input sample rate, Fsi or ILRCK, is greater than the slave-mode OLRCK frequency, then dropped samples will occur. If Fsi or ILRCK is less than the slave-mode OLRCK frequency, then samples will be repeated. In either case the OSLIP bit will be set to 1 and will not be cleared until read through the control port.

5.1.3 Hardware Mode Control

In Hardware Mode, the serial audio input port is not available. SDOUT1 is the serial data output from the sample rate converter, and SDOUT2 is the serial audio output directly from the AES3-compatible receiver. Because there is no serial audio input available in Hardware Mode, all audio data input is done through the AES3-compatible receiver. In Hardware Mode, the serial output ports are controlled through the SAOF and MS_SEL pins. See "Hardware Mode Serial Audio Port Control" on page 40 for more details.

In Hardware Mode, there are always 64 SCLK periods per LRCK period when a serial port is set to master mode.

5.1.4 Software Mode Control

In Software Mode, the CS8422 provides a serial audio input port and two serial audio output ports. Each serial port's clocking and data routing options are fully configurable as shown in Serial Audio Input Data Format (0Bh), Serial Audio Output Data Format - SDOUT1 (0Ch), and Serial Audio Output Data Format - SDOUT2 (0Dh) registers, found on pages 53, 54, and 55.

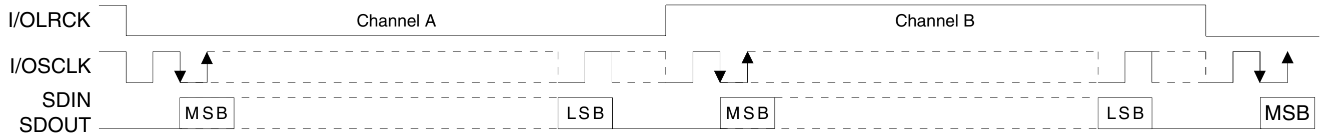

I/OLRCK
Channel A
Channel B
I/OSCLK
SDIN
SDOUT
MSB
LSB
MSB
LSB
MSB

Figure 9. Serial Audio Interface Format – I²S

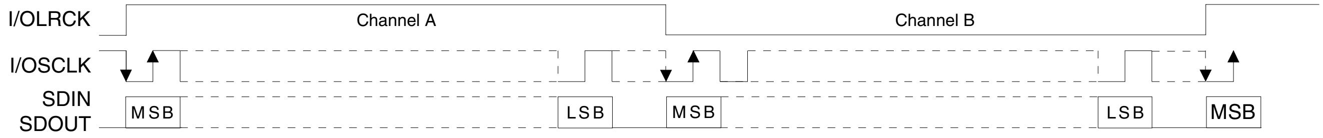

I/OLRCK
Channel A
Channel B
I/OSCLK
SDIN
SDOUT
MSB
LSB
MSB
LSB
MSB

Figure 10. Serial Audio Interface Format – Left-Justified

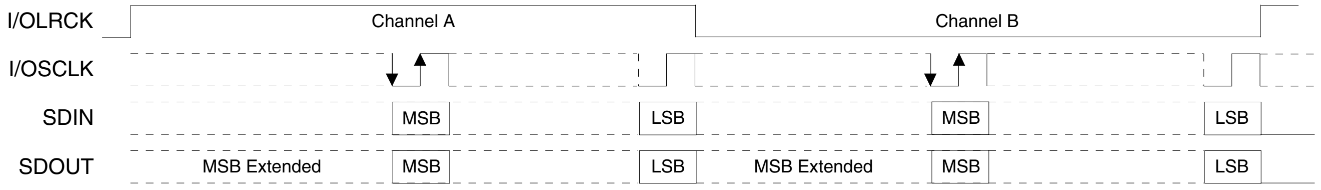

I/OLRCK
Channel A
Channel B
I/OSCLK
SDIN
MSB
LSB
MSB
LSB
SDOUT
MSB Extended
MSB
LSB
MSB Extended
MSB
LSB

Figure 11. Serial Audio Interface Format – Right-Justified (Master Mode only)

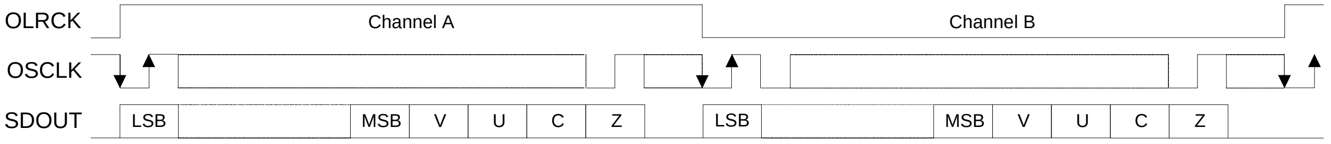

OLRCK
Channel A
Channel B
OSCLK
SDOUT
LSB
MSB
V
U
C
Z
LSB
MSB
V
U
C
Z

Figure 12. Serial Audio Interface Format – AES3 Direct Output

5.1.5 Time Division Multiplexing (TDM) Mode

TDM Mode allows several TDM-compatible devices to be serially connected together allowing their corresponding serial output data to be multiplexed onto one line for input into a DSP or other TDM capable input device.

In TDM Mode, the TDM_IN pin is used to input TDM-formatted data while the SDOUT1 or SDOUT2 (Software Mode only) pin is used to output TDM data. If the CS8422 is the first TDM device in the chain, it should have its TDM_IN connected to GND. Data is transmitted from SDOUTx (SDOUT1 or SDOUT2) most significant bit first on the first falling OSCLKx edge after an OLRCKx rising edge and is valid on the rising edge of OSCLKx.

5.1.5.1 TDM Master Mode

In TDM master mode, OSCLKx frequency is fixed at 256*OLRCKx (where x = 1 or x = 2 depending on which serial output port is selected as being in TDM Mode). Each sample time slot is 32 bit-clock periods long; providing 8 channels of digital audio multiplexed together, with the first two channels being supplied by the CS8422 which has been placed in master mode. An OSCLKx-wide OLRCKx pulse identifies the start of a new frame, with the valid data sample beginning one OSCLKx after the OLRCKx rising edge. In TDM master mode, the master clock source for the TDM serial port must be 256, 512, or 1024*Fso. Valid data lengths are 16, 18, 20, or 24 bits. Figure 13 shows the interface format for TDM master mode.

5.1.5.2 TDM Slave Mode

In TDM slave mode, the number of channels that can by multiplexed to one serial data line depends on the output sample rate. For slave mode, OSCLKx must operate at N*64*Fso, where N is the number of CS8422's in the TDM chain. For example, if Fso = 96 kHz, N = 4 (8 channels of serial audio data), OSCLKx frequency must be 24.576 MHz. Note that the maximum OSCLKx frequency in slave mode is a function of the VL supply voltage, as shown in "Switching Specifications" on page 17. Figure 14 shows the interface format for TDM slave mode.

5.1.5.3 Hardware Mode Control

In Hardware Mode, TDM Mode is selected through the SAOF pin. See Section 8.1 on page 40 for more details.

5.1.5.4 Software Mode Control

In Software Mode, TDM Mode is selected through the Serial Audio Output Data Format - SDOUT1 (0Ch) register, found on page 54.

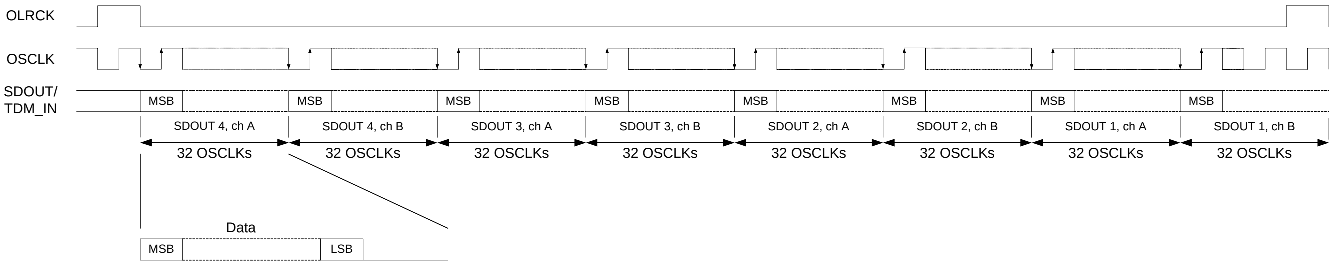

OLRCK
OSCLK
SDOUT/
TDM_IN
MSB
SDOUT 4, ch A
SDOUT 4, ch B
SDOUT 3, ch A
SDOUT 3, ch B
SDOUT 2, ch A
SDOUT 2, ch B
SDOUT 1, ch A
SDOUT 1, ch B
32 OSCLKs
Data
MSB
LSB

Figure 13. TDM Master Mode Timing Diagram

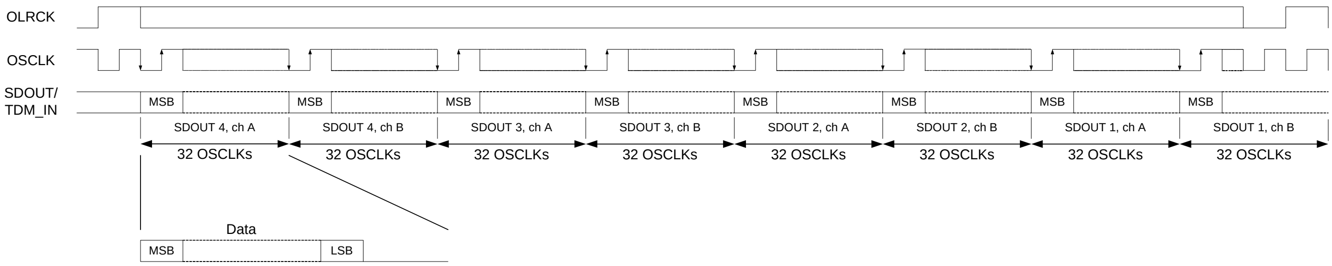

OLRCK
OSCLK
SDOUT/
TDM_IN
MSB
SDOUT 4, ch A
SDOUT 4, ch B
SDOUT 3, ch A
SDOUT 3, ch B
SDOUT 2, ch A
SDOUT 2, ch B
SDOUT 1, ch A
SDOUT 1, ch B
32 OSCLKs
Data
MSB
LSB

Figure 14. TDM Slave Mode Timing Diagram

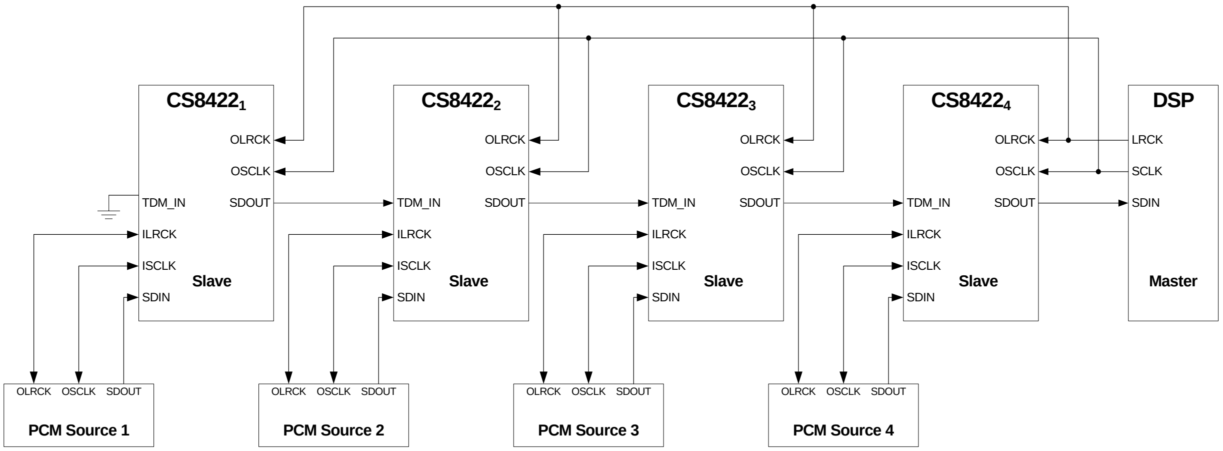

CS8422₁
CS8422₂
CS8422₃
CS8422₄
DSP
OLRCK
OSCLK
TDM_IN
SDOUT
ILRCK
ISCLK
SDIN
Slave
LRCK
SCLK
SDIN
Master
OLRCK OSCLK SDOUT
PCM Source 1
PCM Source 2
PCM Source 3
PCM Source 4

Figure 15. TDM Mode Configuration (All CS8422 outputs are slave)

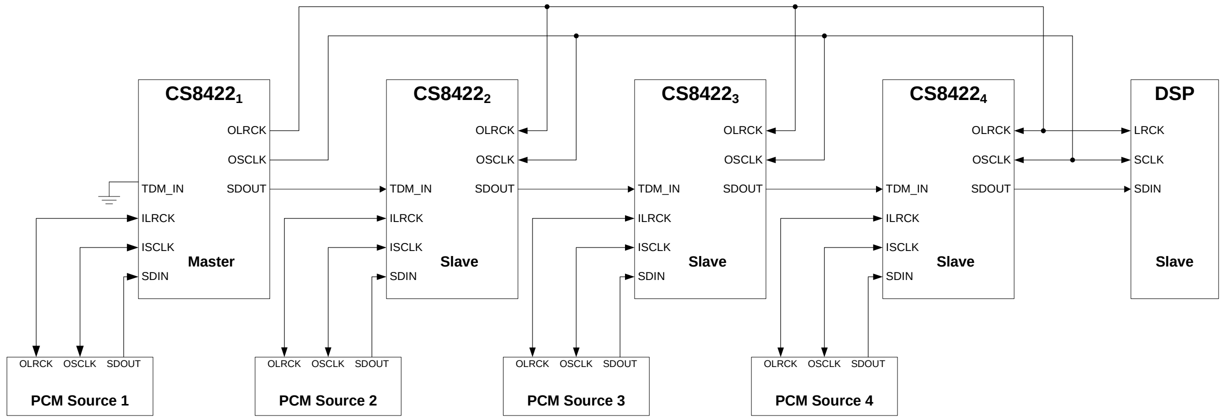

CS8422₁
CS8422₂
CS8422₃
CS8422₄
DSP
OLRCK
OSCLK
TDM_IN
SDOUT
ILRCK
ISCLK
SDIN
Master
Slave
LRCK
SCLK
SDIN
Slave
OLRCK OSCLK SDOUT
PCM Source 1
PCM Source 2
PCM Source 3
PCM Source 4

Figure 16. TDM Mode Configuration (First CS8422 output is master, all others are slave)

6. DIGITAL INTERFACE RECEIVER

The CS8422 includes a digital interface receiver that can receive and decode audio data according to the AES3, IEC60958, S/PDIF, and EIJ CP1201 interface standards.

The CS8422 uses either a 4:1 single-ended or 2:1 differential input mux to select the input pin(s) that will receive input data to be decoded. A low-jitter clock (RMCK) is recovered using a PLL, which provides the digital interface receiver with a master clock. The decoded audio data can either be routed through the SRC for sample rate conversion, or can be an output on one of two serial audio output ports. The channel status and Q-subcode data portion of the user data are assembled and buffered in Channel Status Registers (23h - 2Ch) and Q-Channel Subcode (19h - 22h), and may be accessed through the control port in either SPI or I²C Mode.

6.1 AES3 and S/PDIF Standards

This document assumes that the user is familiar with the AES3 and S/PDIF data formats. It is advisable to have current copies of the AES3, IEC60958, IEC61937, and EIJ CP1201 specifications on hand for easy reference.

The latest AES3 standard is available from the Audio Engineering Society at www.aes.org. The latest IEC60958/61937 standard is available from the International Electrotechnical Commission at www.iec.ch. The latest EIAJ CP-1201 standard is available from the Japanese Electronics Bureau at www.jeita.or.jp/eiaj/.

Application Note 22: *Overview of Digital Audio Interface Data Structures*, available at www.cirrus.com*,* contains a useful tutorial on digital audio specifications, but it should not be considered a substitute for the standards.

The paper titled *An Understanding and Implementation of the SCMS Serial Copy Management System for Digital Audio Transmission*, by Clifton Sanchez, is an excellent tutorial on SCMS. It is available from the AES as reprint 3518.

6.2 Receiver Input Multiplexer

The CS8422's receiver input multiplexer allows input of data compatible with AES3, S/PDIF, IEC60958, and EIAJ CP-1201 standards. For information about recommended receiver input circuits, see "External Receiver Components" on page 64.

6.2.1 Hardware Mode Control

In Hardware Mode, the receiver input multiplexer is limited to a selection between two differential inputs, RXP0/RXN0 and RXP1/RXN1. The receiver input multiplexer will decode data present at the differential input selected by the RX_SEL pin. See Section 8. "Hardware Mode Control" on page 39 for more details.

Multiplexer inputs are floating when not selected. Unused inputs should be tied to AGND/DGND

6.2.2 Software Mode Control

In Software Mode, CS8422 offers either a 4:1 single-ended, or a 2:1 differential input multiplexer to accommodate switching between up to four channels of AES3 or S/PDIF-compatible data input. In Single-Ended Mode, the CS8422 can switch between four single-ended signals present at RX[3:0]. In differential mode, the CS8422 can switch between two differential signals, present on RXP0/RXN0 and RXP1/RXN1.

Multiplexer inputs are floating when not selected. Unused inputs should be tied to AGND/DGND

In Software Mode, the receiver input multiplexer is controlled through the register described in Section 11.3 "Receiver Input Control (03h)" on page 48.

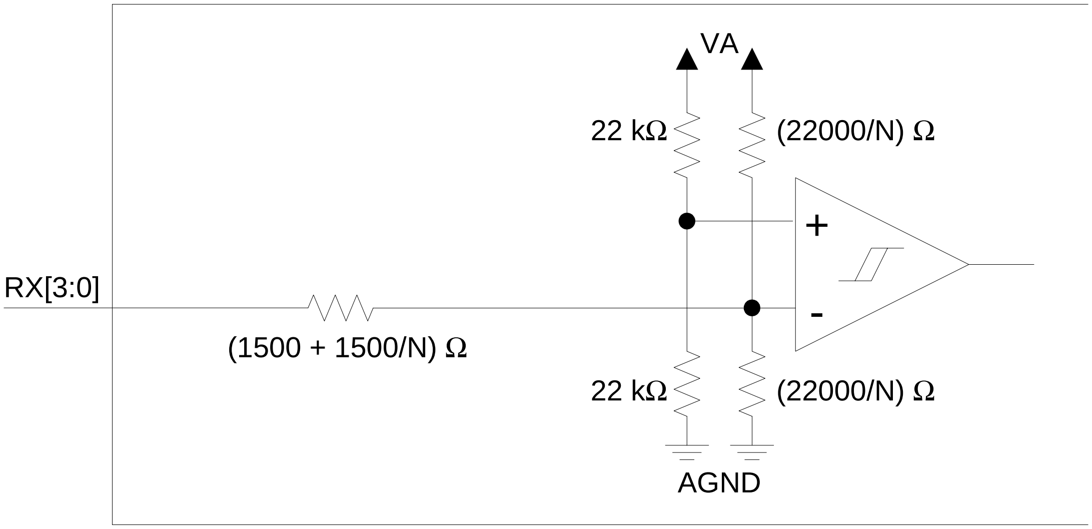
6.2.2.1 Single-Ended Input Mode

When the receiver input multiplexer is set to Single-Ended Mode, the receiver inputs can be switched between operation as comparator inputs or digital inputs.

Receiver Input Mode 1 (Analog Sensitivity Mode)

If Mode 1 is selected, the inputs are biased at VA/2 and should be coupled through a capacitor. The recommended value for the AC coupling capacitors is 0.01 µF to 0.1 µF. The recommended dielectrics for the AC coupling capacitors are C0G or X7R.

When the receiver input multiplexer is in Mode 1, the receiver input pins allow very low amplitude signals to be decoded reliably. In this mode, the maximum allowable input amplitude is determined by VA, which is nominally 3.3 volts. If input amplitudes greater than 3.3 Volts to a single pin of the receiver input multiplexer are required, then attenuation is necessary prior to the receiver input to avoid damage to the part (See “Attenuating Input signals” on page 65 for more details). Figure 17 shows the input structure of the receiver in Single-Ended Mode.



Note:
1. If RX[3:0] is selected by either the receiver MUX or the TX pass-through MUX, N=1.
2. If RX[3:0] is selected by both the receiver MUX and the TX pass-through MUX, N=2.
3. If RX[3:0] is not selected at all, N=0 (i.e. high impedance).

Figure 17. Single-Ended Receiver Input Structure, Receiver Mode 1

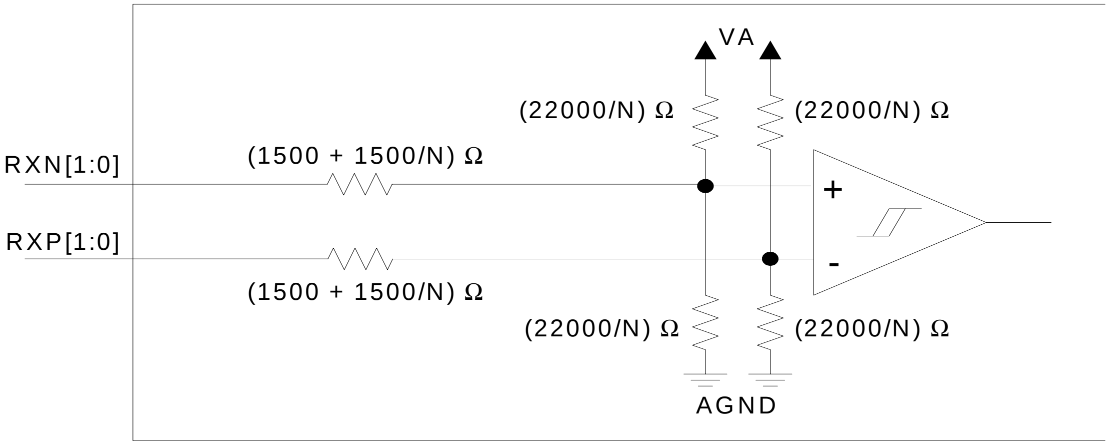
Receiver Input Mode 2 (Digital Sensitivity Mode)

If Mode 2 is selected, the receiver inputs should be driven by a digital signal referenced to VA. In this mode, the selected receiver input is not biased, and does not require the use of an AC coupling capacitor (as with the use of a typical optical receiver output).

When the receiver input multiplexer is in Mode 2 the specifications for V_{IH}/V_{IL} apply (see “Switching Specifications” on page 17 for more details).

6.2.2.2 Differential Input Mode

When the receiver input multiplexer is set to differential input mode, the inputs are biased at VA/2, and require the use of AC coupling capacitors, as mentioned in Section 6.2.2.1. Figure 18 shows the structure of the receiver in differential mode.



Note:

1. If RXP/N[1:0] is selected by either the receiver MUX or the TX pass-through MUX, N=1.
2. If RXP/N[1:0] is selected by both the receiver MUX and the TX pass-through MUX, N=2.
3. If RXP/N[1:0] is not selected at all, N=0 (i.e. high impedance).

Figure 18. Differential Receiver Input Structure

6.3 Recovered Master Clock - RMCK

The CS8422 has an internal PLL which recovers a high-frequency system clock, referred to as the recovered master clock (RMCK). RMCK can be generated by incoming AES3-compatible data or the ISCLK (slave mode and Software Mode only). This clock is used as the master clock source for the AES3 receiver and the master-mode serial port that it directly supplies data to, and is available as an output on the RMCK pin. In addition, the user can set the RMCK as the master clock of either of the two remaining serial ports.

6.3.1 Hardware Mode Control

In Hardware Mode, the RMCK frequency is determined by the incoming AES3 frame rate and the MS_SEL pin. RMCK can be routed for use as the master clock for the serial audio output associated with SDOUT1 by connecting a 20 kΩ resistor from the RMCK pin to VL. See “Hardware Mode Control” on page 39 for more details.

6.3.2 Software Mode Control

In Software Mode, The RMCK frequency is determined by the incoming AES3 frame rate or ISCLK/64 (slave mode only). The RMCK frequency is configured in the register described in Section 11.9 “Recovered Master Clock Ratio Control & Misc. (09h)” on page 52. If the ISCLK is chosen as the source for RMCK, then the ratios in the “Recovered Master Clock Ratio Control & Misc. (09h)” register reflect the ratio of 64*RMCK/ISCLK.

6.4 XTI System Clock Mode

A special clock switching mode is available that allows the clock present at the XTI-XTO clock input to automatically replace RMCK when the PLL becomes unlocked. This is accomplished without spurious transitions or glitches on RMCK.

When clock switching is enabled, the PLL’s loss of lock will cause the XTI-XTO clock input to be output on RMCK. If a serial port is set master mode and has RMCK as its master clock source, it’s LRCK and SCLK frequencies will be derived from the XTI-XTO clock when clock switching has taken place and the RMCK-to-LRCK ratio will be maintained.

When clock switching is not enabled and the PLL has lost lock, RMCK will be derived from the VCO idle frequency. The frequency of the RMCK output will be still be determined by the ratio selected by the RMCK[2:0] bits in register 09h, or the MS_SEL pin in Hardware Mode. When the PLL has lost lock, the VCO idle frequency is equivalent to AES3 input data with Fs ≅ 54 kHz ± 5% (or ISCLK ≅ 3.456 MHz ± 5%).

6.4.1 Hardware Mode Control

In Hardware Mode, XTI System Clock Mode is always enabled.

6.4.2 Software Mode Control

In Software Mode, XTI System Clock Mode is controlled through the register described in Section 11.2 “Clock Control (02h)” on page 47.

6.5 AES11 Behavior

When an AES3-derived OLRCK is configured as a master, the rising or falling edge of OLRCK (depending on the serial port interface format setting) will be within -1.5%(1/Fs) to 1.5%(1/Fs) from the start of the preamble X/Z. In master mode, the latency through the receiver depends on the input sample frequency. In master mode the latency of the audio data will be 3 frames in AES3 direct mode, and 4 frames in all other cases.

When an AES3-derived OLRCK is configured as a slave, any synchronized input within +/-25% of an AES3 frame from the positive or negative edge of OLRCK (depending on the serial port interface format setting) will be treated as being sampled at the same time. Since the CS8422 has no control of the OLRCK in slave mode, the latency of the data through the part will be a multiple of 1/Fs plus the intrinsic delay between OLRCK and the preambles also present in master mode.

Both of these conditions are within the tolerance range set forth in the AES11 standard.

6.6 Error and Status Reporting

While decoding the incoming bi-phase encoded data stream, the CS8422 has the ability to identify various error conditions. Refer to Sections 6.6.1 and 6.6.2 for details.

6.6.1 Software Mode

Software Mode allows the most flexibility in reading errors. When unmasked, bits in the Receiver Error register (0Ch) indicate the following errors:

1. QCRC – CRC error in Q subcode data.
2. CCRC – CRC error in channel status data.
3. UNLOCK – PLL is not locked to incoming bi-phase data stream, or 2 valid Z preambles have not yet been detected.
4. V – Data Validity bit is set.
5. CONF – The input data stream may be near error condition due to jitter degradation.
6. BIP – Bi-phase encoding error.
7. PAR – Parity error in incoming data.

The error bits are “sticky”, meaning that they are set on the first occurrence of the associated error and will remain set until the user reads the register through the control port. This enables the register to log all unmasked errors that occurred since the last time the register was read.

As a result of the bits “stickiness”, it is necessary to perform two reads on these registers to see if the error condition still exists.

The Receiver Error Mask register (0Eh) allows masking of individual errors. The bits in this register default to 00h and serve as masks for the corresponding bits of the Receiver Error register. If a mask bit is set to 1, the error is unmasked, which implies the following: its occurrence will be reported in the receiver error register, induce a pulse on RERR, invoke the occurrence of a RERR interrupt, and affect the current audio sample according to the status of the HOLD bits. The exceptions are the QCRC and CCRC errors, which do not affect the current audio sample, even if unmasked.

The HOLD bits allow a choice of:

- Holding the previous sample
- Replacing the current sample with zero (mute)
- Not changing the current audio sample

For more details, refer to “Receiver Error Unmasking (0Eh)” on page 56, “Interrupt Unmasking (0Fh)” on page 56, “Interrupt Mode (10h)” on page 57, “Receiver Error (13h)” on page 58, and “Interrupt Status (14h)” on page 59.

6.6.2 Hardware Mode Control

In Hardware Mode, the user may choose to output either the Non-Validity Receiver Error (NVERR) or the Receiver Error (RERR) on the NV/RERR pin. By default the pin will output the NRERR signal. If upon startup a 20 kΩ resistor is connected between the pin and VL, the NV/RERR pin will output the RERR error signal. Both RERR and NVERR are updated on AES3 subframe boundaries. See “Hardware Mode Control” on page 39 for more details.

NVERR – The previous audio sample is held and passed to the serial audio output port if a parity, bi-phase, confidence or PLL lock error occurs during the current sample.

RERR – The previous audio sample is held and passed to the serial audio output port if the validity bit is high, or a parity, bi-phase, confidence or PLL lock error occurs during the current sample.

6.7 Non-Audio Detection

An AES3 data stream may be used to convey non-audio data, thus it is important to know whether the incoming AES3 data stream is digital audio or not. This information is typically conveyed in channel status bit 1, which is extracted automatically by the CS8422. However, certain non-audio sources, such as AC-3® or MPEG encoders, may not adhere to this convention and the bit may not be properly set. The CS8422 AES3 receiver can detect such non-audio data through the use of an auto-detect module. The auto-detect module is similar to auto-detect software used in Cirrus Logic DSPs.

If the AES3 stream contains sync codes in the proper format for IEC61937 or DTS® data transmission, an internal AUTODETECT signal will be asserted. If the sync codes no longer appear after a certain amount of time, auto-detection will time-out and AUTODETECT will be de-asserted until another format is detected. The $\overline{\text{AUDIO}}$ signal is the logical OR of AUTODETECT and the received channel status bit 1.

In Software Mode $\overline{\text{AUDIO}}$ is available through the GPO pins. If non-audio data is detected, the data is still processed exactly as if it were normal audio. The exception is the use of de-emphasis auto-select feature which will bypass the de-emphasis filter if the input stream is detected to be non-audio. It is up to the user to mute the outputs as required.

6.7.1 *Hardware Mode Control*

In Hardware Mode, $\overline{\text{AUDIO}}$ is output on the V/$\overline{\text{AUDIO}}$ pin when a 20 kΩ resistor is connected from the V/$\overline{\text{AUDIO}}$ pin to VL.

6.7.2 *Software Mode Control*

In Software Mode, the $\overline{\text{AUDIO}}$ signal is available through the GPO pins. See "GPO Control 1 (05h)" on page 50 for more details.

6.8 Format Detection (Software Mode Only)

In Software Mode, the CS8422 can automatically detect various serial audio input formats. The Format Detect Status register (12h) is used to indicate a detected format. The register will indicate if uncompressed PCM data, IEC61937 data, DTS_LD data, DTS_CD data, or digital silence was detected. Additionally, the IEC61937 Pc/Pd burst preambles are available in registers 2Dh-30h. See the register descriptions for more information.

6.9 Interrupts (Software Mode Only)

The INT signal, available in Software Mode, indicates when an interrupt condition has occurred and may be output on one of the GPOs. It can be set through bits INT[1:0] in the Control1 register (02h) to be active low, active high, or open-drain active low. This last mode is used for active low, wired-OR hook-ups, with multiple peripherals connected to the microcontroller interrupt input pin.

Many conditions can cause an interrupt, as listed in the interrupt status register descriptions. Each source may be masked off through mask register bits. In addition, some sources may be set to rising edge, falling edge, or level sensitive. Combined with the option of level sensitive or edge sensitive modes within the microcontroller, many different configurations are possible, depending on the needs of the equipment designer. Refer to the register descriptions for the Interrupt Unmasking (0Fh), Interrupt Mode (10h), and Interrupt Status (14h) registers

6.10 Channel Status and User Data Handling

"Channel Status Buffer Management" on page 66 describes the overall handling of Channel Status and User data.

6.10.1 *Hardware Mode Control*

In Hardware Mode, Received Channel Status (C), and User (U) bits are output on the C and TX/U pins (U data output must be selected on the TX/U pin, see "Hardware Mode Control" on page 39 for details). OLRCK2 and RCBL are made available to qualify the C and U data output. Figure 19 illustrates timing of the C and U data and their related signals.

6.10.2 *Software Mode Control*

In Software Mode, several options are available for accessing the Channel Status and User data that is encoded in the received AES3 or SPDIF data.

The first option allows access directly through registers. The first 5 bytes of the Channel Status block are decoded into the "Channel Status Registers (23h - 2Ch)". Registers 23h-27h contain the A channel status data. Registers 28h-2Ch contain the B channel status data.

Received Channel Status (C), User (U), and $\overline{\text{EMPH}}$ bits may also be serial outputs to the GPO pins by appropriately setting the GPOxSEL bits in the "GPO Control 1 (05h)" registers. OLRCK and RCBL can be made available to qualify the C and U data output. In serial port slave mode, VLRCK and RCBL can be made available to qualify the C and U data output. VLRCK is a virtual word clock, equal to the receiver recovered sample rate, that can be used to frame the C/U output. VLRCK and RCBL are available through the GPO pins. Figure 19 illustrates timing of the C and U data, and their related signals. To recover serial C-data or U-data with either OLRCK1 or OLRCK2, the corresponding serial port must be directly sourced by the AES3 receiver (not the SRC).

To source an SDOUT signal directly from the RX receiver, the receiver should be set in master mode in order to recover the received data. In this configuration, the SDOUT signal sourced from the receiver will toggle at the AES frame rate. If the RX receiver is set to slave mode, the user must ensure that its associated input OLRCK signal is externally synchronized to the input S/PDIF stream in order to recover the received data. In both configurations, VLRCK is equal to the OLRCK signal associated with the serial port used to clock the recovered receiver data.

When both SDOUTs are sourced from the RX receiver, VLRCK will equal OLRCK1. When both SDOUTs are sourced from the SRC, then VLRCK will equal the recovered AES frame rate, not OLRCK.

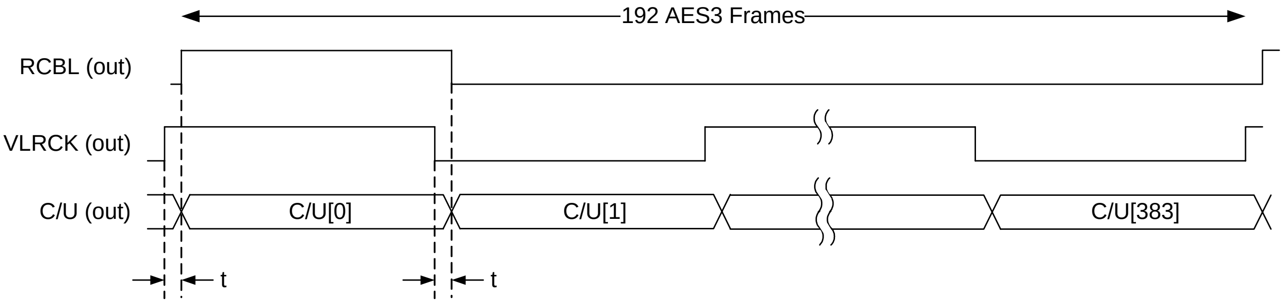
SDOUT1	SDOUT2	VLRCK	COMMENT
RX	RX	OLRCK1	see (Note 4)
RX	SRC	OLRCK1	see (Note 4)
SRC	RX	OLRCK2	see (Note 4)
SRC	SRC	AES FRAMES	see (Note 6)

Table 1. VLRCK Behavior

The user may also access all of the C and U bits directly from the output data stream (SDOUT) by setting bits SOFSELx[1:0]=11 (AES3 Direct mode) in “Serial Audio Output Data Format - SDOUT1 (0Ch)” or “Serial Audio Output Data Format - SDOUT2 (0Dh)”. The appropriate bits can be stripped from the SDOUT signal by external control logic such as a DSP or microcontroller. AES3 Direct mode is only valid if the serial port in question is directly sourced by the AES3 receiver (not the SRC).

If the incoming User data bits have been encoded as Q-channel subcode, the data is decoded, buffered, and presented in 10 consecutive register locations located in “Q-Channel Subcode (19h - 22h)” register. An interrupt may be enabled to indicate the decoding of a new Q-channel block, which may be read through the “Interrupt Status (14h)” register.

The encoded Channel Status bits which indicate sample word length are decoded according to AES3-2003 or IEC 60958. The number of auxiliary bits are reported in bits 7 through 4 of the “Receiver Channel Status (11h)”.



Note:

1. RCBL will go high on the transition of the first output C/U data bit (C/U[0]) and will remain high until the C/U[0] - C/U[1] transition.
2. VLRCK is a virtual word clock that is available through the GPO pins, and can be used to frame the C/U output.
3. VLRCK frequency is always equal to the incoming frame rate of the AES3-compatible data. If there are an even number of OSCLK periods per OLRCK, then the VLRCK duty cycle is 50%, otherwise it is 50% ± one OSCLK period.
4. If a serial audio output port is sourced directly by the AES3-compatible receiver VLRCK = $\overline{\text{OLRCK}}$ in I²S Mode, and VLRCK = OLRCK in left-justified and Right-Justified Modes.
5. If a serial port is sourced directly by the AES3-compatible receiver, the data will transition on the fourth OSCLK falling edge after a VLRCK edge and will be valid on VLRCK edges (t = 4 OSCLK period).
6. If a serial port is not sourced directly by the AES3-compatible receiver (as in a sample rate conversion application), the data will transition 1/64*Fsi after a VLRCK edge, and will be valid on VLRCK edges (t = 1/64*Fsi).

Figure 19. C/U Data Outputs

7. SAMPLE RATE CONVERTER (SRC)

Multirate digital signal processing techniques are used to conceptually upsample the incoming data to a very high rate and then downsample to the outgoing rate. Internal filtering is designed so that a full input audio bandwidth of 20 kHz is preserved if the input sample and output sample rates are greater than or equal to 44.1 kHz. When the output sample rate becomes less than the input sample rate, the input is automatically band limited to avoid aliasing artifacts in the output signal. Any jitter in the incoming signal has little impact on the dynamic performance of the rate converter and has no influence on the output clock.

7.1 SRC Data Resolution and Dither

When using the serial audio input port in left justified and I²S Modes, all input data is treated as 24-bits wide. Any truncation that has been done prior to the CS8422 to less than 24-bits should have been done using an appropriate dithering process. If the serial audio input port is in Right-Justified Mode, the input data will be truncated to the bit depth set through the “Serial Audio Input Data Format (0Bh)” register. If the bit depth is set to 16 bits, and the input data is 24-bits wide, then truncation distortion will occur. Similarly, in any serial audio input port mode, if an inadequate number of bit clocks are entered (i.e. 16 clocks instead of 20 clocks), then the input words will be truncated, causing truncation distortion at low levels. In summary, there is no dithering mechanism on the input side of the CS8422, and care must be taken to ensure that no truncation occurs.

The output side of the SRC can be set to 16, 18, 20, or 24. Dithering is applied and is automatically scaled to the selected output word length. This dither is not correlated between left and right channel.

7.1.1 Hardware Mode Control

In Hardware Mode, the SRC is the data source for SDOUT1, and its serial output port data resolution is controlled through the SAOF pin. See Section 8.1 on page 40 for more details.

7.1.2 Software Mode Control

In Software Mode, the serial port data resolution is controlled through the “Serial Audio Input Data Format (0Bh)”, “Serial Audio Output Data Format - SDOUT1 (0Ch)”, and “Serial Audio Output Data Format - SDOUT2 (0Dh)” registers.

7.2 SRC Locking

The SRC calculates the ratio between the input sample rate and the output sample rate, and uses this information to set up various parameters inside the SRC block. The SRC takes some time to make this calculation (approximately ~100 ms when Fso = 48 kHz).

The SRC_UNLOCK signal is used to indicate when the SRC is not locked. When $\overline{\text{RST}}$ is asserted, or if there is a change in Fsi or Fso, SRC_UNLOCK will be set high. The SRC_UNLOCK pin will continue to be high until the SRC has reacquired lock and settled, at which point it will transition low. When the SRC_UNLOCK pin is set low, SDOUT is outputting valid audio data. This can be used to signal a DAC to unmute its output.

The SRC_UNLOCK signal is available through the control port register 15h, or through the SRC_UNLOCK pin in Hardware Mode.

7.3 SRC Muting

The SDOUT pin sourced by the SRC (SDOUT1 or SDOUT2 in Software Mode, SDOUT1 in Hardware Mode) is set to all zero output (full mute) immediately after the $\overline{\text{RST}}$ pin is set high. While the output from the SRC becomes valid, SDOUT will be unmuted over a period of approximately 4096/Fso (soft unmuted). When the output becomes invalid the SRC's SDOUT is immediately set to all zero output (hard muted). After all invalid states have been cleared, the SRC will soft unmute SDOUT.

7.4 SRC Master Clock

The CS8422 can use the clock signal supplied through XTI-XTO, the PLL, or an internal ring oscillator as its master clock (MCLK). If the SRC MCLK source is selected as being XTI-XTO, care must be taken to ensure that the SRC MCLK source does not exceed 33 MHz. If the SRC MCLK source exceeds 33 MHz, an internal clock divider can be enabled to divide the SRC MCLK source by 2, allowing the use of higher frequency clocks. See Section 7.4.1 and Section 7.4.2 for more details.

If the SRC MCLK is applied through XTI then it can be supplied from a digital clock source, a crystal oscillator, or a fundamental mode crystal. If XTO is not used, such as with a digital clock source or crystal oscillator, XTO should be left unconnected or pulled low through a 20 kΩ resistor to GND.

If a crystal in conjunction with the internal oscillator is used to supply the SRC MCLK, the crystal circuit should be connected as shown in Figure 20. If VL < 2.5 Volts, it is recommended that the crystal attached across XTI and XTO should be specified as operating with a load capacitance of 10pF (capacitors in Figure 20 should be 20 pF). If VL ≥ 2.5 Volts, it is recommended that the crystal attached across XTI and XTO should be specified as operating with a series capacitance of at 20pF (capacitors in Figure 20 should be at 40 pF). Please refer to the crystal manufacturer's specifications for more information about external capacitor recommendations.

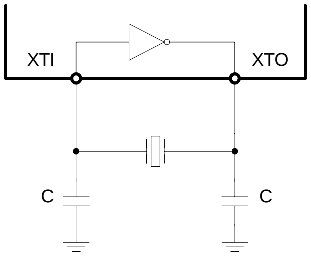


Figure 20. Typical Connection Diagram for Crystal Circuit

If the PLL clock is selected as the SRC MCLK, the SRC MCLK will be synchronous to incoming AES3-compatible data or ISCLK. Unlike RMCK, the user does not control PLL clock's relationship to the sampling rate of incoming AES3-compatible data (Fsi), or ISCLK. See Table 2 for the relationship between the Fsi or ISCLK/64, and the PLL clock.

Fsi (or ISCLK/64)	PLL/Fsi
Fsi ≤ 49 kHz	512
60 kHz ≤ Fsi ≤ 98 kHz	256
120 kHz ≤ Fsi	128

Table 2. PLL Clock Ratios

The CS8422 has the ability to operate without a master clock input through XTI. This benefits the design by not requiring extra external clock components (lowering production cost) and not requiring a master clock to be routed to the CS8422, resulting in lowered noise contribution in the system. In this mode, an internal oscillator provides the clock to run all of the internal logic. See Section 7.4.1 and Section 7.4.2 for explanation of how the SRC MCLK can be selected.

7.4.1 *Hardware Mode Control*

In Hardware Mode, the default master clock source for the SRC is the internal ring oscillator. Therefore, it is not necessary to apply an external MCLK source for the SRC. Optionally the user may select the PLL clock as the SRC MCLK source by connecting a 20 kΩ pull-up resistor between MCLK_OUT and VL.

7.4.2 *Software Mode Control*

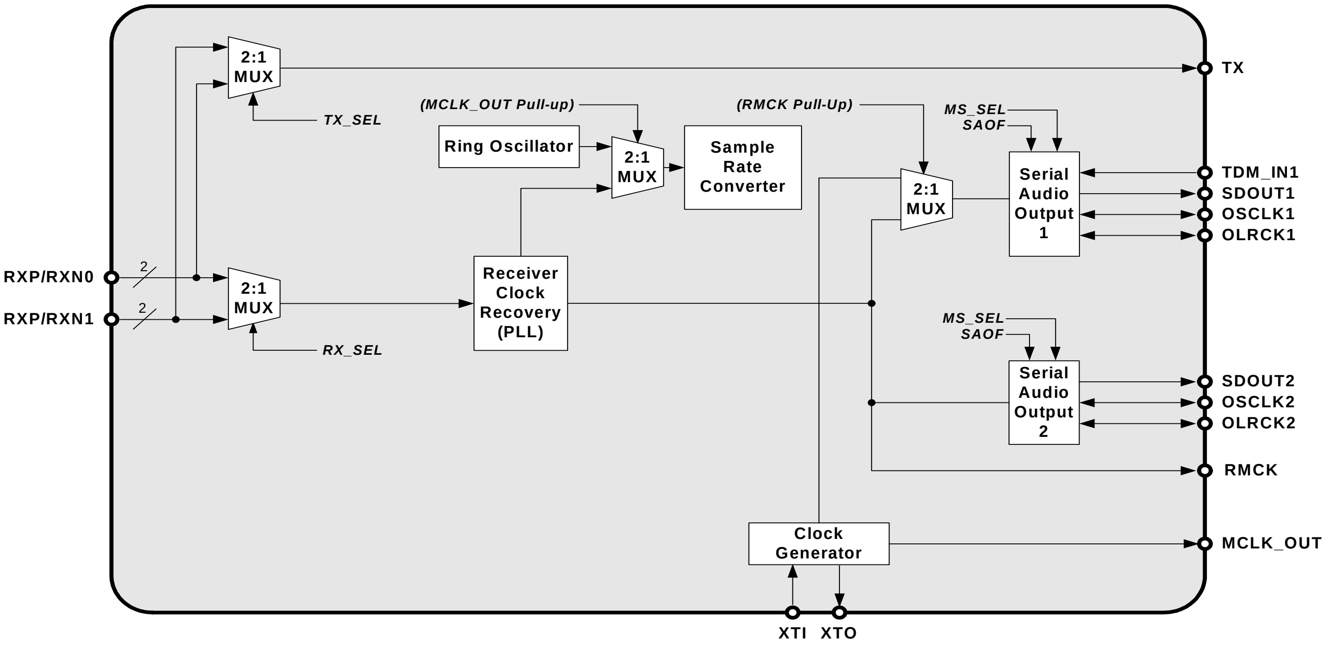
In Software Mode, the SRC master clock source is selected by the SRC_MCLK[1:0] bits in the “SRC Output Serial Port Clock Control (08h)” register. If the XTI clock is selected as the SRC MCLK and XTI is tied to VL or DGND and XTO is left unconnected, then the internal ring oscillator will take the place of the XTI-XTO clock source.

If the selected SRC MCLK source is XTI-XTO, and is greater that 33 MHz, the user can enable the internal clock divide-by-two by setting the SRC_DIV bit in control port register 08h. See “SRC Output Serial Port Clock Control (08h)” on page 51 for more details.

8. HARDWARE MODE CONTROL

The CS8422 provides a stand-alone hardware control mode in which the part does not require an I²C or SPI control port. In Hardware Mode, the user is provided with a subset of the features available in Software Mode as shown in Figure 21. The part will be in Hardware Mode if there is a 20 kΩ pull-up resistor connected between the C pin and VL upon reset.

Controlling the CS8422 in Hardware Mode is done through dedicated control inputs, 20 kΩ pull-up or pull-down resistors attached to dual-purpose pins, and by attaching a specific resistor values from one of two dedicated control pins (SAOF and MS_SEL) to either VL or ground. In the case of SAOF and MS_SEL, the resistor should be connected as close to the pin as possible and should have a tolerance no greater than ±1%. Dedicated controls (TX_SEL and RX_SEL) can be changed during operation whereas pull-up resistor controls are sensed on startup. Figure 21 shows clock routing options available in Hardware Mode. Control signal names are in italics and are described in the table below.



2:1 MUX
TX
TX_SEL
(MCLK_OUT Pull-up)
(RMCK Pull-Up)
MS_SEL
SAOF
Ring Oscillator
2:1 MUX
Sample Rate Converter
2:1 MUX
Serial Audio Output 1
TDM_IN1
SDOUT1
OSCLK1
OLRCK1
RXP/RXN0
RXP/RXN1
2
2
2:1 MUX
Receiver Clock Recovery (PLL)
RX_SEL
MS_SEL
SAOF
Serial Audio Output 2
SDOUT2
OSCLK2
OLRCK2
RMCK
Clock Generator
MCLK_OUT
XTI
XTO

Figure 21. Hardware Mode Clock Routing

Pin Name	Description	Pin Configuration	Selection
RX_SEL	Selects Active AES3 RX Input	Connected to GND	RXP0/RXN0 is active
		Connected to VL	RXP1/RXN1 is active
TX_SEL	Selects RX Input to be output on TX pin	Connected to GND	RXP0/RXN0 to TX
		Connected to VL	RXP1/RXN1 to TX
SDOUT1	Enables or Disables De-emphasis Auto-detect	No pull-up on SDOUT1	De-emphasis Auto-detect Enabled
		20 kΩ pull-up on SDOUT1	De-emphasis Auto-detect Disabled
SAOF	Selects data format for SDOUT1 & SDOUT2	See Table 4 on page 41	
MS_SEL	Selects master/slave and clock configuration for SDOUT1& SDOUT 2	See Table 5 on page 41	
RMCK	Selects master clock source for SDOUT1 serial port	No pull-up on RMCK	XTI-XTO
		20 kΩ pull-up on RMCK	RMCK
MCLK_OUT	Selects master clock source for the SRC	No pull-up on MCLK_OUT	Ring Oscillator
		20 kΩ pull-up on MCLK_OUT	PLL Clock
TX/U	Selects TX pass-through output or incoming U data output	No pull-up on U	TX Pass-through
		20 kΩ pull-up on U	U Data Output
C	Selects Software or Hardware Mode	No pull-up on C	Software Mode
		20 kΩ pull-up on C	Hardware Mode
NV/RERR	Selects error signal output on NV/RERR	No pull-up on RERR/NVERR	NVERR
		20 kΩ pull-up on RERR/NVERR	RERR
V/$\overline{\text{AUDIO}}$	Selects either incoming Validity data output or $\overline{\text{AUDIO}}$ indicator output	20 kΩ pull-down on V/$\overline{\text{AUDIO}}$	Validity data output
		20 kΩ pull-up on V/$\overline{\text{AUDIO}}$	$\overline{\text{AUDIO}}$ indicator output

Table 3. Hardware Mode Control Settings

8.1 Hardware Mode Serial Audio Port Control

The CS8422 uses the resistors attached to the MS_SEL and SAOF pins to determine the modes of operation for its serial output ports. After a RST is asserted, the resistor value and condition (VL or GND) are sensed. This operation will take approximately 4 ms to complete. The SRC_UNLOCK pin will remain high and both SDOUT pins will be muted until the mode detection sequence has completed. After this, if all clocks are stable, SRC_UNLOCK will be brought low when audio output is valid and normal operation will begin.

The resistor attached to each mode selection pin should be placed physically close to the CS8422. The end of the resistor not connected to the mode selection pins should be connected as close as possible to VL and GND to minimize noise. Table 4 and Table 5 show the pin functions and their corresponding settings.

Table 4 shows the Hardware Mode options for output serial port format and the required SAOF pin configurations. In the case of SDOUT2, the output resolution depends on the resolution of the incoming AES3-compatible data. In Right-Justified Modes, the serial format word-length will be equal to the AES3 input data resolution. The exception is the case where Right-Justified Mode is selected and the AES3 input word-length is an odd number of bits. In this case, the SDOUT2 word-length will be zero-stuffed to be 1 bit longer then the AES3 input word-length (example: a 19-bit AES3 input word will result in an 20-bit right-justified serial format). For a more detailed description of serial formats, refer to Section 5. on page 24.

Table 5 shows the Hardware Mode master/slave and clock options for both serial ports, and the required MS_SEL pin configurations. For SDOUT1, when the serial port is set to master mode, the master clock ratio determines what the output sample rate will be based on the MCLK selected for SDOUT1, as shown in the hardware control pin descriptions shown above. For SDOUT2, the output sample rate is dictated by the incoming AES3 data, and the master mode clock ratio determines the frequency of RMCK relative to the incoming AES3 sample rate. Note: if TDM Mode is selected for SDOUT1, then SDOUT1 cannot be set to “Master, Fso = MCLK/128”.

SAOF pin	SDOUT1 Data Format	SDOUT2 Data Format
32.4 kΩ ± 1% to GND	I^{2}S 24-bit data	I^{2}S
16.2 kΩ ± 1% to GND	I^{2}S 20-bit data	I^{2}S
8.06 kΩ ± 1% to GND	I^{2}S 16-bit data	I^{2}S
4.02 kΩ ± 1% to GND	Left-Justified 24-bit data	Left-Justified
1.96 kΩ ± 1% to GND	Left-Justified 20-bit data	Left-Justified
≤1.0 kΩ + 1% to GND	Left-Justified 16-bit data	Left-Justified
32.4 kΩ ± 1% to VL	Right-Justified 24-bit data (Master mode only)	Right-Justified (Master mode only)
16.2 kΩ ± 1% to VL	Right-Justified 20-bit data (Master mode only)	Right-Justified (Master mode only)
8.06 kΩ ± 1% to VL	Right-Justified 16-bit data (Master mode only)	Right-Justified (Master mode only)
4.02 kΩ ± 1% to VL	TDM Mode 24-bit data	I^{2}S
1.96 kΩ ± 1% to VL	TDM Mode 20-bit data	I^{2}S
≤1.0 kΩ + 1% to VL	TDM Mode 16-bit data	I^{2}S

Table 4. Hardware Mode Serial Audio Format Control

MS_SEL pin	SDOUT1	SDOUT2
127.0 kΩ ± 1% to GND	Slave	Slave RMCK = 256 x Fsi
63.4 kΩ ± 1% to GND	Master, Fso = MCLK/128	
32.4 kΩ ± 1% to GND	Master, Fso = MCLK/256	
16.2 kΩ ± 1% to GND	Master, Fso = MCLK/512	
8.06 kΩ ± 1% to GND	Slave	Master Mode, RMCK = 128 x Fsi
4.02 kΩ ± 1% to GND	Master, Fso = MCLK/128	
1.96 kΩ ± 1% to GND	Master, Fso = MCLK/256	
≤1.0 kΩ + 1% to GND	Master, Fso = MCLK/512	
127.0 kΩ ± 1% to VL	Slave	Master Mode, RMCK = 256 x Fsi
63.4 kΩ ± 1% to VL	Master, Fso = MCLK/128	
32.4 kΩ ± 1% to VL	Master, Fso = MCLK/256	
16.2 kΩ ± 1% to VL	Master, Fso = MCLK/512	
8.06 kΩ ± 1% to VL	Slave	Master Mode, RMCK = 512 x Fsi
4.02 kΩ ± 1% to VL	Master, Fso = MCLK/128	
1.96 kΩ ± 1% to VL	Master, Fso = MCLK/256	
≤1.0 kΩ + 1% to VL	Master, Fso = MCLK/512	

Table 5. Hardware Mode Serial Audio Port Clock Control

9. SOFTWARE MODE CONTROL

9.1 Control Port Description

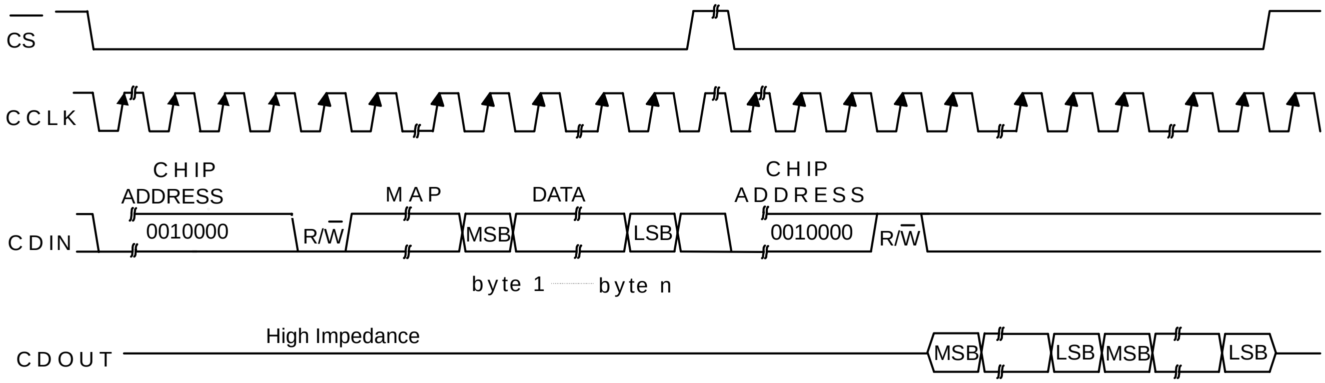
The control port is used to access the registers, allowing the CS8422 to be configured for the desired operational modes and formats. The operation of the control port may be completely asynchronous with respect to the audio sample rates. However, to avoid potential interference problems, the control port pins should remain static if no operation is required.

The control port has two modes: SPI and I²C, with the CS8422 acting as a slave device. SPI Mode is selected if there is a high to low transition on the AD0/CS pin, after the RST pin has been brought high. I²C Mode is selected by connecting the AD0/CS pin through a resistor to VL or DGND, thereby permanently selecting the desired AD0 bit address state.

9.1.1 SPI Mode

In SPI Mode, CS is the CS8422 chip select signal, CCLK is the control port bit clock (input into the CS8422 from the microcontroller), CDIN is the input data line from the microcontroller, CDOUT is the output data line to the microcontroller. Data is clocked in on the rising edge of CCLK and out on the falling edge.

Figure 22 shows the operation of the control port in SPI Mode. To write to a register, bring CS low. The first seven bits on CDIN form the chip address and must be 0010000. The eighth bit is a read/write indicator (R/W), which should be low to write. The next eight bits include the 7-bit Memory Address Pointer (MAP), which is set to the address of the register that is to be updated. The next eight bits are the data which will be placed into the register designated by the MAP. During writes, the CDOUT output stays in the Hi-Z state. It may be externally pulled high or low with a 20 kΩ resistor, if desired.



MAP = Memory Address Pointer, 8 bits, MSB first

Figure 22. Control Port Timing in SPI Mode

To read a register, the MAP has to be set to the correct address by executing a partial write cycle which finishes (CS high) immediately after the MAP byte. To begin a read, bring CS low, send out the chip address and set the read/write bit (R/W) high. The next falling edge of CCLK will clock out the MSB of the addressed register (CDOUT will leave the high impedance state). The MAP automatically increments, so data for successive registers will appear consecutively.

9.1.2 I^{2}C Mode

In I^{2}C Mode, SDA is a bidirectional data line. Data is clocked into and out of the part by the clock, SCL. There is no $\overline{\text{CS}}$ pin. Pins AD0 and AD1 form the two least significant bits of the chip address and should be connected to VL or DGND as desired. The GPO2 pin is used to set the AD2 bit by connecting a 20 kΩ resistor from the GPO2 pin to VL (a 20 kΩ pull-up sets AD2 = 1, and the absence of a pull-up sets AD2 = 0). The states of the pins are sensed while the CS8422 is being reset.

The signal timings for a read and write cycle are shown in Figure 23 and Figure 24. A Start condition is defined as a falling transition of SDA while the clock is high. A Stop condition is a rising transition while the clock is high. All other transitions of SDA occur while the clock is low. The first byte sent to the CS8422 after a Start condition consists of a 7-bit chip address field and a R/$\overline{\text{W}}$ bit (high for a read, low for a write). The upper 4 bits of the 7-bit address field are fixed at 0010.

To communicate with a CS8422, the chip address field, which is the first byte sent to the CS8422, should match 0010 followed by the settings of the AD2, AD1, and AD0 pins. The eighth bit of the address is the R/$\overline{\text{W}}$ bit. If the operation is a write, the next byte includes the Memory Address Pointer (MAP) which selects the register to be read or written. If the operation is a read, the contents of the register pointed to by the MAP will be output. Each byte is separated by an acknowledge bit (ACK). The ACK bit is output from the CS8422 after each input byte is read, and is input to the CS8422 from the microcontroller after each transmitted byte.

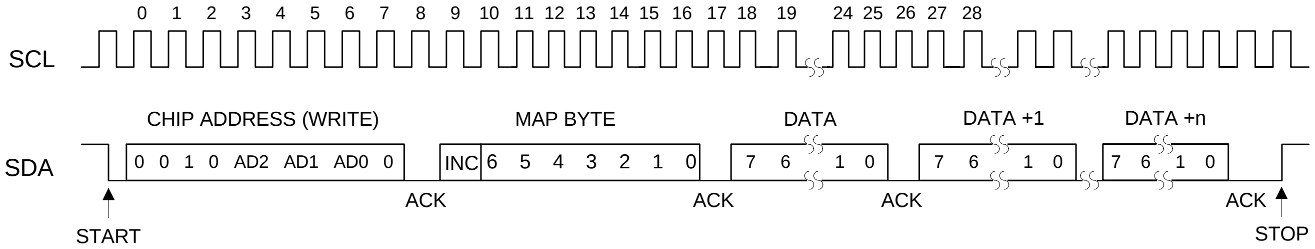

0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 24 25 26 27 28
SCL
CHIP ADDRESS (WRITE)
MAP BYTE
DATA
DATA +1
DATA +n
SDA
0 0 1 0 AD2 AD1 AD0 0
INC 6 5 4 3 2 1 0
7 6 1 0
7 6 1 0
7 6 1 0
ACK
ACK
ACK
ACK
START
STOP

Figure 23. Control Port Timing, I^{2}C Slave Mode Write

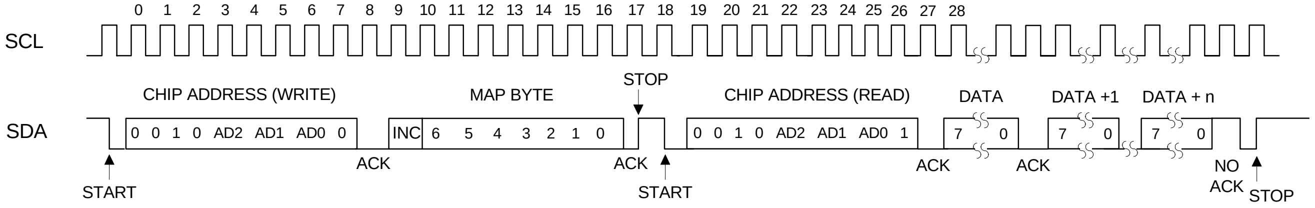

0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 23 24 25 26 27 28
SCL
CHIP ADDRESS (WRITE)
MAP BYTE
STOP
CHIP ADDRESS (READ)
DATA
DATA +1
DATA + n
SDA
0 0 1 0 AD2 AD1 AD0 0
INC 6 5 4 3 2 1 0
0 0 1 0 AD2 AD1 AD0 1
7 0
7 0
7 0
START
ACK
ACK
START
ACK
ACK
NO ACK
STOP

Figure 24. Control Port Timing, I^{2}C Slave Mode Read

Note that the read operation can not set the MAP so an aborted write operation is used as a preamble. As shown in Figure 24, the write operation is aborted after the acknowledge for the MAP byte by sending a stop condition.

9.1.3 Memory Address Pointer (MAP)

The MAP is an 8-bit word containing the control port address to be read or written in both SPI and I^{2}C Modes and a bit to control an auto-increment feature. MAP[6:0] constitute the address to be read or written, while bit 7 of the MAP (INC) determines whether or not MAP[6:0] will automatically increment after each control port read or write. If INC = 0, MAP[6:0] will not automatically increment after each control port read or write. If INC = 1, MAP[6:0] will automatically increment after each control port read or write. The MAP byte is shown in Figures 23 and 24.

10.REGISTER QUICK REFERENCE

This table shows the register names and default values for read-write registers.

Addr	Function	7	6	5	4	3	2	1	0
01h	Chip ID & Version	ID4	ID3	ID2	ID1	ID0	REV2	REV1	REV0
		0	0	0	1	0	0	0	0
02h	Clock Control	PDN	FSWCLK	SWCLK	RMCK_CTL1	RMCK_CTL0	INT1	INT0	Reserved
		1	0	0	0	0	0	0	0
03h	Receiver Input Control	RX_MODE	RXSEL1	RXSEL0	TXSEL1	TXSEL0	INPUT_TYPE	Reserved	Reserved
		0	0	0	0	1	0	0	0
04h	Receiver Data Control	TRUNC	HOLD1	HOLD0	CHS	DETCI	EMPH_CNTL2	EMPH_CNTL1	EMPH_CNTL0
		0	0	0	0	0	1	0	0
05h	GPO Control 1	GPO0SEL3	GPO0SEL2	GPO0SEL1	GPO0SEL0	GPO1SEL3	GPO1SEL2	GPO1SEL1	GPO1SEL0
		0	0	0	0	0	0	0	0
06h	GPO Control 2	GPO2SEL3	GPO2SEL2	GPO2SEL1	GPO2SEL3	GPO3SEL2	GPO3SEL1	GPO3SEL0	GPO3SEL3
		0	0	0	0	0	0	0	0
07h	SAI Clock Control	SAI_CLK3	SAI_CLK2	SAI_CLK1	SAI_CLK0	SAI_MCLK	Reserved	Reserved	Reserved
		0	1	0	0	0	0	0	0
08h	SRC SAO Clock Control	SAO_CLK3	SAO_CLK2	SAO_CLK1	SAO_CLK0	SAO_MCLK	SRC_MCLK1	SRC_MCLK2	SRC_DIV
		0	1	1	0	0	0	0	0
09h	RMCK Cntl.& Misc.	RMCK3	RMCK2	RMCK1	RMCK0	SRC_MUTE	Reserved	Reserved	Reserved
		0	0	0	0	1	0	0	0
0Ah	Data Routing Control	SDOUT1_1	SDOUT1_0	SDOUT2_1	SDOUT2_0	MUTE_SAO1	MUTE_SAO2	SRCD	Reserved
		0	0	0	1	0	0	0	0
0Bh	SAI Data Format	SIMS	SISF	SIFSEL2	SIFSEL1	SIFSEL0	Reserved	Reserved	Reserved
		0	0	0	0	0	0	0	0
0Ch	SAO1 Data Format & TDM	SOMS1	SOSF1	SORES1_1	SORES1_0	SOFSEL1_1	SOFSEL1_0	TDM1	TDM0
		0	0	0	0	0	0	0	0
0Dh	SAO2 Data Format	SOMS2	SOSF2	SORES2_1	SORES2_0	SOFSEL2_1	SOFSEL2_0	Reserved	Reserved
		0	0	0	0	0	0	0	0
0Eh	RERR Unmasking	ACTIVEM	QCRCM	CCRCM	UNLOCKM	VM	CONFM	BIPM	PARM
		0	0	0	0	0	0	0	0
0Fh	Interrupt Unmasking	PCCHM	OSLIPM	DETCM	CCHM	RERRM	QCHM	FCHM	SRC_UNLOCKM
		0	0	0	0	0	0	0	0
10h	Interrupt Mode	Reserved	Reserved	Reserved	Reserved	RERR1	RERR0	SRC_UNLOCK1	SRC_UNLOCK0
		0	0	0	0	0	0	0	0

Table 6. Summary of Software Register Bits

Addr	Function	7	6	5	4	3	2	1	0
11h	Receiver Channel Status	AUX3	AUX2	AUX1	AUX0	PRO	COPY	ORIG	EMPH
12h	Format Detect Status	PCM	IEC61937	DTS_LD	DTS_CD	HD_CD	DGTL_SIL	Reserved	Reserved
13h	Receiver Error	ACTIVE	QCRC	CCRC	UNLOCK	V	CONF	BIP	PAR
14h	Interrupt Status	PCCH	OSLIP	DETC	CCH	RERR	QCH	FCH	SRC_UNLOCK
15h	PLL Status	RX_ACTIVE	ISCLK_ACTIVE	PLL_LOCK	96KHZ	192KHZ	Reserved	Reserved	Reserved
16h	Receiver Status	CS_UPDATE 0	RCVR_RATE1	RCVR_RATE0	RX_LOCK	BLK_VERR	BLK_CERR	BLK_BERR	BLK_PERR
17h	Fs/XTI Ratio 1	FS_XT15	FS_XT14	FS_XT13	FS_XT12	FS_XT11	FS_XT10	FS_XT9	FS_XT8
18h	Fs/XTI Ratio 2	FS_XT7	FS_XT6	FS_XT5	FS_XT4	FS_XT3	FS_XT2	FS_XT1	FS_XT0
19h	Q Subcode 1	CONTROL	CONTROL	CONTROL	CONTROL	ADDRESS	ADDRESS	ADDRESS	ADDRESS
1Ah	Q Subcode 2	TRACK	TRACK	TRACK	TRACK	TRACK	TRACK	TRACK	TRACK
1Bh	Q Subcode 3	INDEX	INDEX	INDEX	INDEX	INDEX	INDEX	INDEX	INDEX
1Ch	Q Subcode 4	MINUTE	MINUTE	MINUTE	MINUTE	MINUTE	MINUTE	MINUTE	MINUTE
1Dh	Q Subcode 5	SECOND	SECOND	SECOND	SECOND	SECOND	SECOND	SECOND	SECOND
1Eh	Q Subcode 6	FRAME	FRAME	FRAME	FRAME	FRAME	FRAME	FRAME	FRAME
1Fh	Q Subcode 7	ZERO	ZERO	ZERO	ZERO	ZERO	ZERO	ZERO	ZERO
20h	Q Subcode 8	ABS MINUTE	ABS MINUTE	ABS MINUTE	ABS MINUTE	ABS MINUTE	ABS MINUTE	ABS MINUTE	ABS MINUTE
21h	Q Subcode 9	ABS SECOND	ABS SECOND	ABS SECOND	ABS SECOND	ABS SECOND	ABS SECOND	ABS SECOND	ABS SECOND
22h	Q Subcode 10	ABS FRAME	ABS FRAME	ABS FRAME	ABS FRAME	ABS FRAME	ABS FRAME	ABS FRAME	ABS FRAME
23h	Channel A Status Byte 0	AC0[7]	AC0[6]	AC0[5]	AC0[4]	AC0[3]	AC0[2]	AC0[1]	AC0[0]
24h	Channel A Status Byte 1	AC1[7]	AC1[6]	AC1[5]	AC1[4]	AC1[3]	AC1[2]	AC1[1]	AC1[0]
25h	Channel A Status Byte 2	AC2[7]	AC2[6]	AC2[5]	AC2[4]	AC2[3]	AC2[2]	AC2[1]	AC2[0]
26h	Channel A Status Byte 3	AC3[7]	AC3[6]	AC3[5]	AC3[4]	AC3[3]	AC3[2]	AC3[1]	AC3[0]
27h	Channel A Status Byte 4	AC4[7]	AC4[6]	AC4[5]	AC4[4]	AC4[3]	AC4[2]	AC4[1]	AC4[0]
28h	Channel B Status Byte 0	BC0[7]	BC0[6]	BC0[5]	BC0[4]	BC0[3]	BC0[2]	BC0[1]	BC0[0]
29h	Channel B Status Byte 1	BC1[7]	BC1[6]	BC1[5]	BC1[4]	BC1[3]	BC1[2]	BC1[1]	BC1[0]
2Ah	Channel B Status Byte 2	BC2[7]	BC2[6]	BC2[5]	BC2[4]	BC2[3]	BC2[2]	BC2[1]	BC2[0]
2Bh	Channel B Status Byte 3	BC3[7]	BC3[6]	BC3[5]	BC3[4]	BC3[3]	BC3[2]	BC3[1]	BC3[0]

Table 6. Summary of Software Register Bits (Continued)

Addr	Function	7	6	5	4	3	2	1	0
2Ch	Channel B Status Byte 4	BC4[7]	BC4[6]	BC4[5]	BC4[4]	BC4[3]	BC4[2]	BC4[1]	BC4[0]
2Dh	Burst Preamble PC Byte 0	PC0[7]	PC0[6]	PC0[5]	PC0[4]	PC0[3]	PC0[2]	PC0[1]	PC0[0]
2Eh	Burst Preamble PC Byte 1	PC1[7]	PC1[6]	PC1[5]	PC1[4]	PC1[3]	PC1[2]	PC1[1]	PC1[0]
2Fh	Burst Preamble Pd Byte 0	PD0[7]	PD0[6]	PD0[5]	PD0[4]	PD0[3]	PD0[2]	PD0[1]	PD0[0]
30h	Burst Preamble PD Byte 1	PD1[7]	PD1[6]	PD1[5]	PD1[4]	PD1[3]	PD1[2]	PD1[1]	PD1[0]

Table 6. Summary of Software Register Bits (Continued)

11.SOFTWARE REGISTER BIT DEFINITIONS

The table row beneath the row that contains the register-bit name shows the register bit default value. Bits labeled 'Reserved' must remain at their default value.

11.1 CS8422 I.D. and Version Register (01h)

7	6	5	4	3	2	1	0
ID4	ID3	ID2	ID1	ID0	REV2	REV1	REV0
0	0	0	1	0	0	0	0

ID[4:0] - ID code for the CS8422. Permanently set to 00010

REV[2:0] = 000 (revision A)
REV[2:0] = 010 (revision B1)

11.2 Clock Control (02h)

7	6	5	4	3	2	1	0
PDN	FSWCLK	SWCLK	RMCK_CTL1	RMCK_CTL0	INT1	INT0	Reserved
1	0	0	0	0	0	0	0

PDN - Controls the internal clocks, allowing the CS8422 to be placed in a "powered down", low current consumption state. This bit must be written to the 0 state to allow the CS8422 to begin operation. All input clocks should be stable in frequency and phase when PDN is set to 0.

0- Normal part operation.

1- Internal clocks are stopped. Internal state machines are reset. The fully static control port is operational, allowing registers to be read or changed. Power consumption is low.

FSWCLK – Forces the clock signal on XTI to be output on RMCK regardless of the SWCLK bit functionality or PLL lock.

0 – Clock signal on XTI is output on RMCK according to the SWCLK bit functionality.

1 – Forces the clock signal on XTI to be output on RMCK regardless of the SWCLK bit functionality.

SWCLK - Outputs XTI clock signal on RMCK pin when PLL loses lock. Any OSCLK or OLRCK derived from RMCK under normal conditions will be derived from XTI in this case.

0 - Disable automatic clock switching.

1 - Enable automatic clock switching on PLL unlock. Clock signal selected on XTI is automatically output on RMCK on PLL Unlock.

RMCK_CTL[1:0] - RMCK Control

00 - RMCK is an output and is derived from the frame rate of incoming AES3 data.

01 - RMCK is an output and is derived from the ISCLK input frequency divided by 64. Only valid if serial audio input port is in slave mode (SIMS = 0 in "Serial Audio Input Data Format (0Bh)" on page 53).

10 - RMCK is high-impedance.

11 - Reserved

INT[1:0] - Interrupt output pin (INT) control

00 - Active high; high output indicates interrupt condition has occurred.

01 - Active low, low output indicates an interrupt condition has occurred.

10 - Open drain, active low. Requires an external pull-up resistor on the INT pin.

11 - Reserved.

11.3 Receiver Input Control (03h)

7	6	5	4	3	2	1	0
RX_MODE	RXSEL1	RXSEL0	TXSEL1	TXSEL0	INPUT_TYPE	Reserved	Reserved
0	0	0	1	0	0	0	0

RX_MODE - Selects the input mode (single-ended or differential) of the RX pins

0 - Receiver inputs are differential-pair inputs RXP1/RXN1 and RXP0/RXN0.

1 - Receiver inputs are single-ended inputs RX[3:0].

RX_SEL[**1:0]** – Input multiplexer to the receiver

00 - RX0 or RXP0/RXN0

01 - RX1 (Only valid if RX_MODE = 1)

10 - RX2 or RXP1/RXN1

11 - RX3 (Only valid if RX_MODE = 1)

TX_SEL[1:0] – Selects receiver input for GPO TX source

00 - RX0 or RXP0/RXN0

01 - RX1 (Only valid if RX_MODE = 1)

10 - RX2 or RXP1/RXN1

11 - RX3 (Only valid if RX_MODE = 1)

INPUT_TYPE – Selects receiver input type

0 - Mode 1, receiver multiplexer inputs are comparator inputs biased at VA/2.

1 - Mode 2, receiver multiplexer inputs are digital inputs, referenced to VA. Valid only if RX_MODE = 1.

11.4 Receiver Data Control (04h)

7	6	5	4	3	2	1	0
TRUNC	HOLD1	HOLD0	CHS	DETCI	EMPH_CNTL2	EMPH_CNTL1	EMPH_CNTL0
0	0	0	0	0	1	0	0

TRUNC – Determines if the audio word length is set according to the incoming channel status data as decoded by the AUX[3:0] bits. The resulting word length in bits is 24 minus AUX[3:0].

0 – Incoming data is not truncated.

1 – Incoming data is truncated according to the length specified in the channel status data.

Truncation occurs before the de-emphasis filter. TRUNC has no effect on output data is detected as being non-audio.

HOLD[1:0] – Determine how received AES3 audio sample is affected when a receive error occurs

00 - hold last audio sample.

01 - replace the current audio sample with all zeros (mute).

10 - do not change the received audio sample.

11 - reserved

CHS – Sets which channel's C data is decoded in the Receiver Channel Status register (11h) (Default = ‘0’)

0 - A channel

1 - B channel

If CHS = 0 and TRUNC = 1, both channels' audio data will be truncated by the AUX[3:0] bits indicated in the channel A Channel Status data. If CHS = 1 and TRUNC = 1, both channels' audio data will be truncated by the AUX[3:0] bits indicated in the channel B Channel Status data. This will occur even if the AUX[3:0] bits indicated in the channel A Channel Status data are not equal to the AUX[3:0] bits indicated in the channel B Channel Status data.

DETCI - D to E status transfer inhibit

0 -Allow update

1 -Inhibit update

DEM_CNTL[2:0] – De-emphasis filter control. See Figure 25 for De-emphasis filter response.

000 - De-emphasis filter off.

001 - 32 kHz setting

010 - 44.1 kHz setting

011 - 48 kHz setting

100 - Auto-detect Sample Rate. If the PLL estimates that the incoming sample rate is below 49 kHz, de-emphasis will be applied according to the Channel Status data of the incoming AES3 or S/PDIF data. If the PLL estimates that the incoming sample rate is not below 49 kHz, de-emphasis will not be enabled. If the incoming Channel Status data indicates that no de-emphasis should be applied, de-emphasis will not be enabled. If data is detected as being non-audio, the de-emphasis filter will not be enabled.

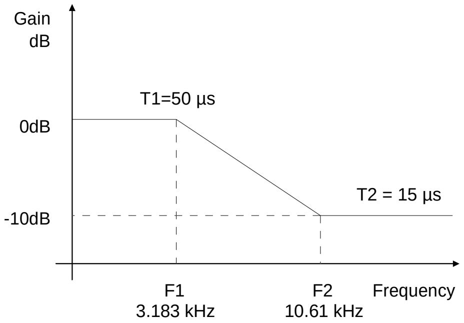


Figure 25. De-Emphasis Filter Response

11.5 GPO Control 1 (05h)

7	6	5	4	3	2	1	0
GPO0SEL3	GPO0SEL2	GPO0SEL1	GPO0SEL0	GPO1SEL3	GPO1SEL2	GPO1SEL1	GPO1SEL0
0	0	0	0	0	0	0	0

GPOxSEL[3:0] – GPO Source select for GPO0 and GPO1 pins. See Table 7 for available outputs for GPO[3:0].

11.6 GPO Control 2 (06h)

7	6	5	4	3	2	1	0
GPO2SEL3	GPO2SEL2	GPO2SEL1	GPO2SEL0	GPO3SEL3	GPO3SEL2	GPO3SEL1	GPO3SEL0
0	0	0	0	0	0	0	0

GPOxSEL[3:0] – GPO Source select for GPO2 and GPO3 pins. See Table 7 for available outputs for GPO[3:0].

Function	Code	Definition
GND	0000	Fixed low level
VL	0001	Fixed VL level.
$\overline{\text{EMPH}}$	0010	State of $\overline{\text{EMPH}}$ bit in the incoming data stream
INT	0011	CS8422 interrupt output
C	0100	Channel status bit
U	0101	User data bit
RERR	0110	Receiver Error
NVERR	0111	Non-Validity Receiver Error
RCBL	1000	Receiver Channel Status Block
96KHZ	1001	Defined in "PLL Status (15h)" on page 60.
192KHZ	1010	Defined in "PLL Status (15h)" on page 60.
$\overline{\text{AUDIO}}$	1011	Non-audio indicator for decoded input stream
VLRCK	1100	Virtual LRCK, can be used to frame the C and U output data.
TX	1101	Pass through of AES/SPDIF input selected by TXSEL[2:0] in Section 11.3 "Receiver Input Control (03h)" on page 48.
SRC_UNLOCK	1110	SRC unlock indicator
XTI_OUT	1111	Buffered XTI-XTO output

Table 7. GPO Pin Configurations

11.7 Serial Audio Input Clock Control (07h)

7	6	5	4	3	2	1	0
SAI_CLK3	SAI_CLK2	SAI_CLK1	SAI_CLK0	SAI_MCLK	Reserved	Reserved	Reserved
0	1	0	0	0			

SAI_CLK[3:0] – Selects the serial audio input master clock-to-ILRCK ratio when the serial audio input port is set to master mode (SIMS = 1 as shown in "Serial Audio Input Data Format (0Bh)" on page 53). Note: if a serial audio output is sourced directly by the serial audio input port, SAI_CLK[3:0] determine the MCLK/LRCK ratio for both serial ports if they are set to master mode.

0000 - ILRCK = MCLK/64

0001 - ILRCK = MCLK/96

0010 - ILRCK = MCLK/128

0011 - ILRCK = MCLK/192

0100 - ILRCK = MCLK/256

0101 - ILRCK = MCLK/384

0110 - ILRCK = MCLK/512

0111 - ILRCK = MCLK/768

1000 - ILRCK = MCLK/1024

SAI_MCLK – Selects the master clock (MCLK) source for the serial audio input when set to master mode (SIMS = 1, as shown in "Serial Audio Input Data Format (0Bh)" on page 53). When set to master, ILRCK and ISCLK are derived from the MCLK selected in this register. Note: if either serial audio output port is sourced directly by the serial audio input port, this bit determines the master clock source for the selected serial output port when it is in master mode.

0 - XTI-XTO

1 - RMCK

11.8 SRC Output Serial Port Clock Control (08h)

7	6	5	4	3	2	1	0
SAO_CLK3	SAO_CLK2	SAO_CLK1	SAO_CLK0	SAO_MCLK	SRC_MCLK1	SRC_MCLK0	SRC_DIV
0	1	0	0	0	0	0	0

SAO_CLK[3:0] – Valid only for the serial port sourced by the SRC. Selects the serial audio input master clock-to-OLRCK ratio when the serial audio output port is set to master mode (SOMS = 1 as shown in "Serial Audio Output Data Format - SDOUT1 (0Ch)" on page 54 and "Serial Audio Output Data Format - SDOUT2 (0Dh)" on page 55).

0000 - OLRCK = MCLK/64

0001 - OLRCK = MCLK/96

0010 - OLRCK = MCLK/128

0011 - OLRCK = MCLK/192

0100 - OLRCK = MCLK/256

0101 - OLRCK = MCLK/384

0110 - OLRCK = MCLK/512

0111 - OLRCK = MCLK/768

1000 - OLRCK = MCLK/1024

SAO_MCLK – Selects the master clock (MCLK) source for the serial audio output, sourced by the SRC, when set to master mode (SOMS1 or SOMS 2 = 1, as shown in "Serial Audio Output Data Format - SDOUT1 (0Ch)" on page 54 and "Serial Audio Output Data Format - SDOUT2 (0Dh)" on page 55). When set to master, OLRCK and OSCLK are derived from the MCLK selected in this register.

0 - XTI-XTO

1 - RMCK

SRC_MCLK[1:0] - Controls the master clock (MCLK) source for the sample rate converter. See "SRC Master Clock" on page 38 for details.

00 - XTI-XTO. If XTI is connected to GND or VL and XTO is left floating, the SRC MCLK will be the internal ring oscillator.

01 - PLL clock

10 - Internal Ring Oscillator

11 - Reserved

SRC_DIV – Divide-by-two for the SRC MCLK source. Valid only if SRC_MCLK = 00.

0 - SRC MCLK is not divided. Maximum allowable SRC MCLK frequency is 33 MHz.

1 - SRC MCLK is divided. Maximum allowable SRC MCLK frequency is 49.152 MHz.

11.9 Recovered Master Clock Ratio Control & Misc. (09h)

7	6	5	4	3	2	1	0
RMCK3	RMCK2	RMCK1	RMCK0	SRC_MUTE	Reserved	Reserved	Reserved
0	0	0	0	1			

RMCK[3:0] – Selects the RMCK/Fsi ratio, where Fsi is the sample rate of the incoming AES3-compatible data or ISCLK/64. Note: If a serial audio output port is in master mode and sourced directly by the AES3 receiver, then RMCK is the master clock source for the selected serial output port and RMCK[3:0] determine the MCLK/OLRCK ratio for the selected serial output port.

0000 - RMCK = 64 x Fsi

0001 - RMCK = 96 x Fsi

0010 - RMCK = 128 x Fsi

0011 - RMCK = 192 x Fsi

0100 - RMCK = 256 x Fsi

0101 - RMCK = 384 x Fsi

0110 - RMCK = 512 x Fsi

0111 - RMCK = 768 x Fsi

1000 - RMCK = 1024 x Fsi

SRC_MUTE – When SRC_MUTE is set to '1', the SRC will soft-mute when it loses lock and soft unmute when it regains lock.

0 - Soft mute disabled

1 - Soft mute enabled

11.10 Data Routing Control(0Ah)

7	6	5	4	3	2	1	0
SDOUT1(1)	SDOUT1(0)	SDOUT2(1)	SDOUT2(0)	MUTESAO1	MUTESAO2	SRCD	Reserved
0	0	0	1	0	0	0	

SDOUT1[1:0] - Controls the data source for SDOUT1

00 - Sample Rate Converter

01 - AES3 Receiver Output

10 - SDIN (SDIN and SDOUT should be synchronous)

11 - Reserved

SDOUT2[1:0] - Controls the data source for SDOUT2

00 - Sample Rate Converter

01 - AES3 Receiver Output

10 - SDIN (SDIN and SDOUT should be synchronous)

11 - Reserved

MUTESAO1 - Mute control for the serial audio output port 1

0 - SDOUT1 not muted

1 - SDOUT1 muted (set to all zeros)

MUTESAO2 - Mute control for the serial audio output port 2

0 - SDOUT2 not muted.

1 - SDOUT2 muted (set to all zeros).

SRCD - Controls the data source of the sample rate converter

0 - Serial Audio Input Port (SDIN)

1 - AES3 Receiver Output

11.11 Serial Audio Input Data Format (0Bh)

7	6	5	4	3	2	1	0
SIMS	SISF	SIFSEL2	SIFSEL1	SIFSEL0	Reserved	Reserved	Reserved
0	0	0	0	0			

SIMS - Master/Slave Mode Selector

0 - Serial audio input port is in slave mode. ISCLK and ILRCK are inputs.

1 - Serial audio input port is in master mode. ISCLK and ILRCK are outputs.

SISF - ISCLK Frequency. Valid only in master mode (SIMS = 1). Should be changed when PDN = 1. See Table 8 for details.

SAI_CLK[3:0]	MCLK/ILRCK Ratio	ISCLK/ILRCK Ratio	
		SISF = 0	SISF = 1
0000	64	64	INVALID
0001	96	48	96
0010	128	64	128
0011	192	48	96
0100	256	64	128

Table 8. ISCLK/ILRCK Ratios and SISF Settings

0101	384	48	96
0110	512	64	128
0111	768	48	96
1000	1024	64	128

Table 8. ISCLK/ILRCK Ratios and SISF Settings

SIFSEL[2:0] - Serial audio input data format

000 - Left-Justified, up to 24-bit data

001 - I^{2}S, up to 24-bit data

010 - Right-Justified, 24-bit data

011 - Right-Justified, 20-bit data

100 - Right-Justified, 18-bit data

101 - Right-Justified, 16-bit data

110, 111 - Reserved

11.12 Serial Audio Output Data Format - SDOUT1 (0Ch)

7	6	5	4	3	2	1	0
SOMS1	SOSF1	SORES1_1	SORES1_0	SOFSEL1_1	SOFSEL1_0	TDM1	TDM0
0	0	0	0	0	0	0	0

SOMS1 - Master/Slave Mode Selector

0 - Serial audio output port is in slave mode. OSCLK and OLRCK are inputs.

1 - Serial audio output port is in master mode. OSCLK and OLRCK are outputs.

SOSF1 - OSCLK1 Frequency. Valid only in master mode (SOMS1 = 1). If the SRC is selected as the source for SDOUT1 (SDOUT1[1:0] = 00 in register 0Ah), then the master clock (MCLK) is the SAO MCLK (as selected by the SAO_MCLK bit in register 08h). If the AES3 receiver is selected as the source for SDOUT1 (SDOUT1[1:0] = 01 in register 0Ah), then the MCLK is RMCK. Should be changed when PDN = 1. See Table 9 for details. **Note:** If serial output 1 is in master mode and sourced directly by the serial input port, SAI_CLK[3:0] determines the MCLK/OLRCK1 ratio.

SAO_CLK[3:0], SAI_CLK[3:0], or RMCK[3:0]	MCLK/OLRCK1 Ratio	OSCLK1/OLRCK1 Ratio	
		SOSF1 = 0	SOSF1 = 1
0000	64	64	INVALID
0001	96	48	96
0010	128	64	128
0011	192	48	96
0100	256	64	128
0101	384	48	96
0110	512	64	128
0111	768	48	96
1000	1024	64	128

Table 9. OSCLK1/OLRCK1 Ratios and SOSF1 Settings

SORES1[1:0] - Resolution of the output data on SDOUT

00 - 24-bit resolution.

01 - 20-bit resolution.

10 - 18-bit resolution.

11 - 16-bit resolution

SOFSEL1[1:0] - Format of the output data on SDOUT

00 - Left-Justified

01 - I²S

10 - Right-Justified (Master mode only)

11 - AES3 Direct. Direct copy of the received NRZ data from the AES3 receiver including C, U, and V bits. The time slot occupied by the Z bit is used to indicate the location of the block start. Only valid if serial port sourced directly by the AES3-compatible receiver.

TDM[1:0] - Enable the time-division multiplexing (TDM) through TDM_IN and either SDOUT1 or SDOUT2. See "Time Division Multiplexing (TDM) Mode" on page 27 for more details.

00 - TDM Mode not enabled. Serial audio format selected by SOFSEL1[1:0]

01 - TDM Mode enabled through TDM_IN and SDOUT1. SOFSEL1[1:0] has no effect in this mode.

10 - TDM Mode enabled through TDM_IN and SDOUT2. SOFSEL2[1:0] has no effect in this mode.

11 - Reserved

11.13 Serial Audio Output Data Format - SDOUT2 (0Dh)

7	6	5	4	3	2	1	0
SOMS2	SOSF2	SORES2_1	SORES2_0	SOFSEL2_1	SOFSEL2_0	Reserved	Reserved
0	0	0	0	0	0		

SOMS2 - Master/Slave Mode Selector

0 - Serial audio output port is in slave mode. OSCLK and OLRCK are inputs.

1 - Serial audio output port is in master mode. OSCLK and OLRCK are outputs.

SOSF2 - OSCLK2 Frequency. Valid only in master mode (SOMS2 = 1). If the SRC is selected as the source for SDOUT2 (SDOUT2[1:0] = 00 in register 0Ah), then the master clock (MCLK) is the SAO MCLK (as selected by the SAO_MCLK bit in register 08h). If the AES3 receiver is selected as the source for SDOUT2 (SDOUT2[1:0] = 01 in register 0Ah), then the MCLK is RMCK. Should be changed when PDN = 1. See Table 10 for details. **Note:** If serial output 2 is in master mode and sourced directly by the serial input port, then SAI_CLK[3:0] determine the MCLK/OLRCK1 ratio.

SAO_CLK[3:0], SAI_CLK[3:0], or RMCK[3:0]	MCLK/OLRCK2 Ratio	OSCLK2/OLRCK2 Ratio	
		SOSF2 = 0	SOSF2 = 1
0000	64	64	INVALID
0001	96	48	96

Table 10. OSCLK2/OLRCK2 Ratios and SOSF1 Settings

0010	128	64	128
0011	192	48	96
0100	256	64	128
0101	384	48	96
0110	512	64	128
0111	768	48	96
1000	1024	64	128

Table 10. OSCLK2/OLRCK2 Ratios and SOSF1 Settings

SORES2[1:0] - Resolution of the output data on SDOUT

00 - 24-bit resolution.

01 - 20-bit resolution.

10 - 18-bit resolution.

11 - 16-bit resolution

SOFSEL2[1:0] - Format of the output data on SDOUT

00 - Left-Justified

01 - I^{2}S

10 - Right-Justified (Master mode only)

11 - AES3 Direct. Direct copy of the received NRZ data from the AES3 receiver including C, U, and V bits. The time slot occupied by the Z bit is used to indicate the location of the block start. Only valid if serial port source is the AES3-compatible receiver.

11.14 Receiver Error Unmasking (0Eh)

7	6	5	4	3	2	1	0
ACTIVEM	QCRCM	CCRCM	UNLOCKM	VM	CONFM	BIPM	PARM
	0	0	0	0	0	0	0

RECEIVER ERROR MASK[7:0]

The bits[7:0] in this register serve as masks for the corresponding bits of the Receiver Error Register. If a mask bit is set to 1, the error is unmasked, meaning that its occurrence will appear in the receiver error register, will affect RERR[6:0], will affect the RERR interrupt, and will affect the current audio sample according to the status of the HOLD bit. If a mask bit is set to 0, the error is masked, meaning that its occurrence will not appear in the receiver error register, will not affect the RERR pin, will not affect the RERR interrupt, and will not affect the current audio sample. The ACTIVE, CCRC, and QCRC bits behave differently from the other bits: they do not affect the current audio sample even when unmasked. If QCRC, CCRC, CONF, BIP, or PARM are unmasked, and RERRM in register 0Fh is unmasked, then RERR[1:0] should be set to “Rising Edge Active” in the Interrupt Mode register (register 10h). This register defaults to 00h.

11.15 Interrupt Unmasking (0Fh)

7	6	5	4	3	2	1	0
PCCHM	OSLIPM	DETCM	CCHM	RERRM	QCHM	FCHM	SRC_UNLOCKM
0	0	0	0	0	0	0	0

The bits of this register serve as a mask for the Interrupt Status register. If a mask bit is set to 1, the error is unmasked, meaning that its occurrence will affect the INT pin and the status register. If a mask bit is set to 0, the error is masked, meaning that its occurrence will not affect the internal INT signal or the status register. The bit positions align with the corresponding bits in Interrupt Status register. This register defaults to 00h.

The INT signal may be selected to output on the GPO pins. See Section 11.5 on page 50 for more details.

11.16 Interrupt Mode (10h)

7	6	5	4	3	2	1	0
Reserved	Reserved	Reserved	Reserved	RERR1	RERR0	SRC_UNLOCK1	SRC_UNLOCK0
				0	0	0	0

The interrupt mode control in the behavior of the INT pin to RERR and SRC_UNLOCK interrupts. There are three ways to set the INT pin active in accordance with the interrupt condition. In the Rising edge active mode, the INT pin becomes active on the arrival of the interrupt condition. In the Falling edge active mode, the INT pin becomes active on the removal of the interrupt condition. In Level active mode, the INT interrupt pin becomes active during the interrupt condition. Be aware that the active level (Active High or Low) only depends on the INT[1:0] bits. These registers default to 00h. The interrupts in the Interrupt Status register not represented here are all rising edge active.

00 - Rising edge active

01 - Falling edge active

10 - Level active

11 - Reserved

11.17 Receiver Channel Status (11h)

7	6	5	4	3	2	1	0
AUX3	AUX2	AUX1	AUX0	PRO	COPY	ORIG	EMPH

The bits in this register can be associated with either channel A or B of the received data. The desired channel is selected with the CHS bit of “Receiver Data Control (04h)” on page 48.

AUX3:0 - Incoming auxiliary data field width, as indicated by the incoming channel status bits, decoded according to IEC60958 and AES3.

0000 - Auxiliary data is not present.

0001 - Auxiliary data is 1 bit long.

0010 - Auxiliary data is 2 bits long.

0011 - Auxiliary data is 3 bits long.

0100 - Auxiliary data is 4 bits long.

0101 - Auxiliary data is 5 bits long.

0110 - Auxiliary data is 6 bits long.

0111 - Auxiliary data is 7 bits long.

1000 - Auxiliary data is 8 bits long.

1001 - 1111 Reserved

PRO - Channel status block format indicator

0 - Received channel status block is in the consumer format.

1 - Received channel status block is in the professional format.

COPY - SCMS copyright indicator

0 - Copyright asserted.

1 - Copyright not asserted. If the category code is set to General in the incoming AES3 stream, copyright will always be indicated by COPY, even when the stream indicates no copyright.

ORIG - SCMS generation indicator, decoded from the category code and the L bit.

0 - Received data is 1st generation or higher.

1 - Received data is original.

Note: COPY and ORIG will both be set to 1 if incoming data is flagged as professional or if the receiver is not in use.

$\overline{\text{EMPH}}$ – Indicates if the input channel status data indicates that the incoming audio data has been pre-emphasized.

0 – 50 µs/15 µs pre-emphasis indicated.

1 – 50 µs/15 µs pre-emphasis not indicated.

11.18 Format Detect Status (12h)

7	6	5	4	3	2	1	0
PCM	IEC61937	DTS_LD	DTS_CD	HD_CD	DGTL_SIL	Reserved	Reserved

Note: PCM, DTS_LD, DTS_CD and IEC61937 are mutually exclusive. A ‘1’ indicated the condition was detected.

PCM – Un-compressed PCM data was detected.

IEC61937 – IEC61937 data was detected.

DTS_LD – DTS_LD data was detected.

DTS_CD – DTS_CD data was detected.

HD_CD – HD_CD data was detected.

DGTL_SIL – Digital Silence was detected: at least 2047 consecutive constant samples of the same 24-bit audio data on both channels.

11.19 Receiver Error (13h)

7	6	5	4	3	2	1	0
Reserved	QCRC	CCRC	UNLOCK	V	CONF	BIP	PAR

This register contains the AES3 receiver status bits. Unmasked bits will go high on occurrence of the error, and will stay high until the register is read. Reading the register resets all bits to 0, unless the error source is still true. Bits that are masked off in the receiver error mask register will always be 0 in this register.

QCRC - Q-subcode data CRC error indicator. Updated on Q-subcode block boundaries

0 - No error.

1 - Error.

CCRC - Channel Status Block Cyclic Redundancy Check bit. Updated on CS block boundaries, valid only in Pro mode.

0 - No error.

1 - Error.

UNLOCK - Receiver lock status when sourced by incoming AES3-compatible data. Updated on CS block boundaries.

0 - Receiver locked.

1 - Receiver out of lock.

V - Received AES3 Validity bit status. Updated on sub-frame boundaries.

0 - Data is valid and is normally linear coded PCM audio.

1 - Data is invalid, or may be valid compressed audio.

CONF - Confidence bit. Updated on sub-frame boundaries.

0 - No error.

1 - Confidence error. The input data stream may be near error condition due to jitter degradation.

BIP - Bi-phase error bit. Updated on sub-frame boundaries.

0 - No error.

1 - Bi-phase error. This indicates an error in the received bi-phase coding.

PAR - Parity bit. Updated on sub-frame boundaries.

0 - No error.

1 - Parity error.

11.20 Interrupt Status (14h)

7	6	5	4	3	2	1	0
PCCH	OSLIP	DETC	CCH	RERR	QCH	FCH	SRC_UNLOCK

For all bits in this register, a “1” means the associated interrupt condition has occurred at least once since the register was last read. A “0” means the associated interrupt condition has NOT occurred since the last reading of the register. Reading the register resets all bits to 0, unless the interrupt mode is set to level and the interrupt source is still true. Status bits that are masked off in the associated mask register will always be “0” in this register.

PCCH – PC burst preamble change.

Indicates that the PC byte has changed from its previous value. If the IEC61937 bit in the Format Detect Status register goes high, it will cause a PCCH interrupt even if the PC byte hasn’t changed since the last time the IEC61937 bit went high.

OSLIP - Serial audio output port data slip interrupt

When the serial audio output port is in slave mode, and OLRCK is asynchronous to the port data source, this bit will go high every time a data sample is dropped or repeated. See “Serial Port Clock Operation” on page 25 for more information.

DETC - D to E C-buffer transfer interrupt.

Indicates the completion of a D to E C-buffer transfer. See “Channel Status Buffer Management” on page 53.

CCH - C-Data change.

Indicates that the current 10 bytes of channel status is different from the previous 10 bytes. (5 bytes per channel)

RERR - A receiver error has occurred.

The Receiver Error register may be read to determine the nature of the error which caused the interrupt.

QCH – A new block of Q-subcode is available for reading.

The data must be read within 588 AES3 frames after the interrupt occurs to avoid corruption of the data by the next block.

FCH – Format Change

Goes high when the PCM, IEC61937, DTS_LD, DTS_CD, or DGTL_SIL bits in the Format Detect Status register transition from 0 to 1. When these bits in the Format Detect Status register transition from 1 to 0, an interrupt will not be generated.

SRC_UNLOCK - SRC Unlock condition.

Indicates that the SRC has lost the ability to output valid data

11.21 PLL Status (15h)

7	6	5	4	3	2	1	0
RX_ACTIVE	ISCLK ACTIVE	PLL_LOCK	96KHZ	192KHZ	Reserved	Reserved	Reserved

RX_ACTIVE - Receiver Active

This bit is a level-signal version of the ACTIVE bit in register 13h.

ISCLK_ACTIVE- ISCLK Active

0 - There is no toggling on the ISCLK pin, or the frequency of toggling is less than 36 kHz on the ISCLK pin.

1 - There is toggling at a frequency of at least 1.536 MHz on the ISCLK pin.

PLL_LOCK -

0 - The PLL has not achieved lock.

1 - The PLL, driven by either an AES3 or ISCLK input, has achieved lock.

96KHZ – Indicates the frequency range of the sample rate of incoming AES3 data (Fsi). If Fsi ≤ 49 kHz or Fsi ≥ 120 kHz, this bit will output a “0”. If 60 kHz ≤ Fsi ≤ 98 kHz, this bit will output a “1”. Otherwise the output is indeterminate.

192KHZ – Indicates the frequency range of the sample rate of incoming AES3 data (Fsi). If Fsi ≤ 98 kHz, this bit will output a “0”. If Fsi ≥120 kHz, this bit will output a “1”. Otherwise the output is indeterminate.

11.22 Receiver Status (16h)

7	6	5	4	3	2	1	0
CS_UPDATE	RCVR_RATE1	RCVR_RATE0	RX_LOCK	BLK_VERR	BLK_CERR	BLK_BERR	BLK_PERR
0	-	-	-	-	-	-	-

CS_UPDATE - Determines whether channel status registers and RCVR_RATE are updated in the presence of a receiver error (register 14h).

0 - The receiver channel status registers and RCVR_RATE are updated on each AES3 block boundary.

1 - The receiver channel status registers and RCVR_RATE are updated on each AES3 block boundary if no biphase, confidence, parity, or CRCC error has occurred during the reception of the channel status block.

RCVR_RATE - Input sample rate represented in the channel status data of incoming AES3 data.

00 - Reserved

01 - 32 kHz

10 - 44.1 kHz

11 - 48 kHz

RX_LOCK - AES3 Receiver PLL Lock

0 - The PLL has not achieved lock for more than 2 Z preambles or AES3 input is not driving PLL.

1 - Goes high 2 Z preambles after the PLL has achieved lock when an AES3 input has been selected to drive the PLL.

BLK_VERR - Block Validity Error. Updated on DETC boundaries

0 - The Validity bit of the incoming AES3 data has remained low during the input of the last AES3 data block.

1 - The Validity bit of incoming AES3 data has gone high at some point during the input of the last AES3 data block.

BLK_CERR - Block Confidence Error. Updated on DETC boundaries

0 - The Confidence bit associated with incoming AES3 data has remained high during the input of the last AES3 data block.

1 - The Confidence bit associated with incoming AES3 data has gone low at least once during the input of the last AES3 data block.

BLK_BERR - Block Biphase Error. Updated on DETC boundaries

0 - There has been no biphase error associated with incoming AES3 data during the input of the last AES3 data block.

1 - There has been at least one biphase error associated with incoming AES3 data during the input of the last AES3 data block.

BLK_PERR - Block Parity Error. Updated on DETC boundaries

0 - There has been no parity error associated with incoming AES3 data during the input of the last AES3 data block.

1 - There has been at least one parity error associated with incoming AES3 data during the input of the last AES3 data block.

11.23 Fs/XTI Ratio (17h - 18h)

7	6	5	4	3	2	1	0
FS_XT15	FS_XT14	FS_XT13	FS_XT12	FS_XT11	FS_XT10	FS_XT9	FS_XT8
FS_XT7	FS_XT6	FS_XT5	FS_XT4	FS_XT3	FS_XT2	FS_XT1	FS_XT0

FS_XTI[15:0] - 256*Fs/XTI, where Fs is the sample rate of incoming AES3-compatible data.

The integer part of FS_XT[15:0] is represented in bits [15:10] in register 17h, and the fractional part is represented in bits [9:0] of registers 17h and 18h; with a precision of 300 Hz in Fs and is updated approximately every 2048/(XTI frequency). Reading register 17h will cause the value of 18h to freeze until register 18h is read.

11.24 Q-Channel Subcode (19h - 22h)

7	6	5	4	3	2	1	0
CONTROL	CONTROL	CONTROL	CONTROL	ADDRESS	ADDRESS	ADDRESS	ADDRESS
TRACK	TRACK	TRACK	TRACK	TRACK	TRACK	TRACK	TRACK
INDEX	INDEX	INDEX	INDEX	INDEX	INDEX	INDEX	INDEX
MINUTE	MINUTE	MINUTE	MINUTE	MINUTE	MINUTE	MINUTE	MINUTE
SECOND	SECOND	SECOND	SECOND	SECOND	SECOND	SECOND	SECOND
FRAME	FRAME	FRAME	FRAME	FRAME	FRAME	FRAME	FRAME
ZERO	ZERO	ZERO	ZERO	ZERO	ZERO	ZERO	ZERO
ABS MINUTE	ABS MINUTE	ABS MINUTE	ABS MINUTE	ABS MINUTE	ABS MINUTE	ABS MINUTE	ABS MINUTE
ABS SECOND	ABS SECOND	ABS SECOND	ABS SECOND	ABS SECOND	ABS SECOND	ABS SECOND	ABS SECOND
ABS FRAME	ABS FRAME	ABS FRAME	ABS FRAME	ABS FRAME	ABS FRAME	ABS FRAME	ABS FRAME

Each byte is LSB first with respect to the 80 Q-subcode bits Q[79:0]. Thus bit 7 of address 19h is Q[0] while bit 0 of address 19h is Q[7]. Similarly bit 0 of address 22h corresponds to Q[79].

11.25 Channel Status Registers (23h - 2Ch)

Address	Channel Status Byte	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
23h	Channel A Status Byte 0	AC0[7]	AC0[6]	AC0[5]	AC0[4]	AC0[3]	AC0[2]	AC0[1]	AC0[0]
24h	Channel A Status Byte 1	AC1[7]	AC1[6]	AC1[5]	AC1[4]	AC1[3]	AC1[2]	AC1[1]	AC1[0]
25h	Channel A Status Byte 2	AC2[7]	AC2[6]	AC2[5]	AC2[4]	AC2[3]	AC2[2]	AC2[1]	AC2[0]
26h	Channel A Status Byte 3	AC3[7]	AC3[6]	AC3[5]	AC3[4]	AC3[3]	AC3[2]	AC3[1]	AC3[0]
27h	Channel A Status Byte 4	AC4[7]	AC4[6]	AC4[5]	AC4[4]	AC4[3]	AC4[2]	AC4[1]	AC4[0]
28h	Channel B Status Byte 0	BC0[7]	BC0[6]	BC0[5]	BC0[4]	BC0[3]	BC0[2]	BC0[1]	BC0[0]
29h	Channel B Status Byte 1	BC1[7]	BC1[6]	BC1[5]	BC1[4]	BC1[3]	BC1[2]	BC1[1]	BC1[0]
2Ah	Channel B Status Byte 2	BC2[7]	BC2[6]	BC2[5]	BC2[4]	BC2[3]	BC2[2]	BC2[1]	BC2[0]
2Bh	Channel B Status Byte 3	BC3[7]	BC3[6]	BC3[5]	BC3[4]	BC3[3]	BC3[2]	BC3[1]	BC3[0]
2Ch	Channel B Status Byte 4	BC4[7]	BC4[6]	BC4[5]	BC4[4]	BC4[3]	BC4[2]	BC4[1]	BC4[0]

Each byte is MSB first with respect to the 80 Channel Status bits. Thus bit 0 of address 23h, AC0[0], is the location of the Pro bit. For N = 0-79, Channel Status bit N (per AES specification) is mapped to bit N mod 8 (remainder of N divided by 8) at address 23h+floor(N/8) (23h + integer result of N divided by 8 rounded down). For example, Channel Status bit 35 is mapped to bit 3 (35/8 = 4 remainder 3) of address 27h (23h + 4h).

11.26 IEC61937 PC/PD Burst preamble (2Dh - 30h)

Address	Burst Preamble Byte	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
2Dh	Burst Preamble PC Byte 0	PC0[7]	PC0[6]	PC0[5]	PC0[4]	PC0[3]	PC0[2]	PC0[1]	PC0[0]
2Eh	Burst Preamble PC Byte 1	PC1[7]	PC1[6]	PC1[5]	PC0[4]	PC1[3]	PC1[2]	PC1[1]	PC1[0]
2Fh	Burst Preamble PD Byte 0	PD0[7]	PD0[6]	PD0[5]	PC0[4]	PD0[3]	PD0[2]	PD0[1]	PD0[0]
30h	Burst Preamble PD Byte 1	PD1[7]	PD1[6]	PD1[5]	PD1[4]	PD1[3]	PD1[2]	PD1[1]	PD1[0]

12. APPLICATIONS

12.1 Reset, Power Down, and Start-Up

When $\overline{\text{RST}}$ is low the CS8422 enters a low power mode, all internal states are reset, and the outputs are disabled. After $\overline{\text{RST}}$ transitions from low to high the part senses the resistor value on the configuration pins (MS_SEL and SAOF) and sets the appropriate mode of operation. After the mode has been set (approximately 4 µs) the part is set to normal operation and all outputs are functional.

12.2 Power Supply, Grounding, and PCB layout

The CS8422 operates from a VA = +3.3 V and VL = +1.8 V to +5.0 V supply. These supplies may be set independently. Follow normal supply decoupling practices, see Figure 7 and 8 for details.

Extensive use of power and ground planes, ground plane fill in unused areas, and surface mount decoupling capacitors are recommended. Decoupling capacitors should be mounted on the same side of the board as the CS8422 to minimize inductance effects and all decoupling capacitors should be as close to the CS8422 as possible. The pin of the configuration resistors not connected to MS_SEL and SAOF should be connected as close as possible to VL or DGND.

12.3 External Receiver Components

The CS8422 AES3 receiver is designed to accept both the professional and consumer interfaces. The digital audio specifications for professional use call for a balanced receiver, using XLR connectors, with 110 Ω ± 20% impedance. The XLR connector on the receiver should have female pins with a male shell. Since the receiver has a very high input impedance, a 110 Ω resistor should be placed across the receiver terminals to match the line impedance, as shown in Figure 26 and Figure 27. Although transformers are not required by the AES specification, they are strongly recommended.

If some isolation is desired without the use of transformers, a 0.01 µF capacitor should be placed in series with each input pin (RXP[3:0] and RXN[3:0]) as shown in Figure 27. However, if a transformer is not used, high frequency energy could be coupled into the receiver, causing degradation in analog performance.

Figure 26 and Figure 27 show an optional (recommended) DC blocking capacitor (0.1 µF to 0.47 µF) in series with the cable input. This improves the robustness of the receiver, preventing the saturation of the transformer, or any DC current flow, if a DC voltage is present on the cable.

The circuit in Figure 28 shows the input circuit for switching between up to four single-ended signals in receiver input Mode 1 (analog sensitivity mode). If the application requires switching between a single-ended consumer interface and a differential interface, the CS8422 must be in differential mode and the input circuit in Figure 28 should be used for the single ended source. Standards for the consumer interface call for an unbalanced circuit having a receiver impedance of 75 Ω ±5%. The connector for the consumer interface is an RCA phono socket.

The circuit in Figure 29 shows the input circuit for switching between up to four single-ended TTL or CMOS signals, and should be used when the S/PDIF receiver is in Receiver Input Mode 2. If the application requires switching between a CMOS or TTL source and a differential source, the CS8422 must be in differential mode and the input circuit in Figure 30 should be used for the single-ended digital source. If the application requires switching between a single ended source in Mode 1, and a TTL or CMOS source, the circuit in Figure 30 should be used for the CMOS/TTL source (no RXN connection is present in this case).

When designing systems, it is important to avoid ground loops and DC current flowing down the shield of the cable that could result when boxes with different ground potentials are connected. Generally, it is good practice to ground the shield to the chassis of the transmitting unit, and connect the shield through a capacitor to chassis ground at the receiver. However, in some cases it is advantageous to have the ground of two boxes held to the same potential, and the cable shield might be depended upon to make that electrical connection. Generally, it is a good idea to provide the option of grounding or capacitively coupling the shield to the chassis.

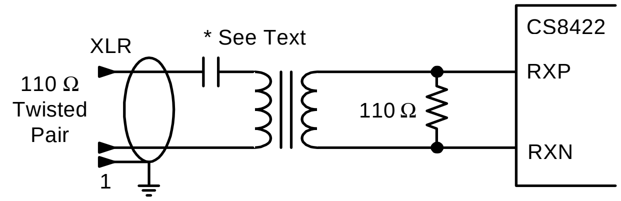

XLR
* See Text
110 Ω Twisted Pair
1
110 Ω
CS8422
RXP
RXN

Figure 26. Professional Input Circuit – Differential Mode

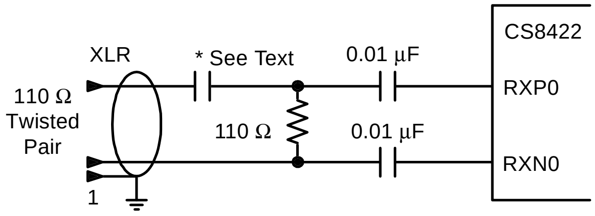

XLR
* See Text
0.01 µF
110 Ω Twisted Pair
1
110 Ω
0.01 µF
CS8422
RXP0
RXN0

Figure 27. Transformerless Professional Input Circuit – Differential Mode

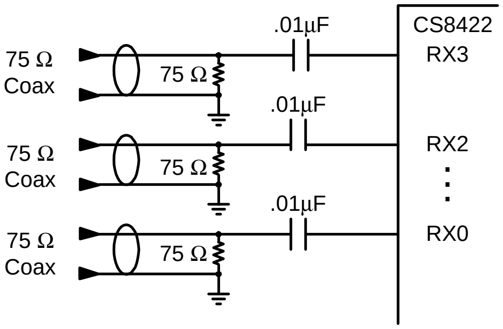
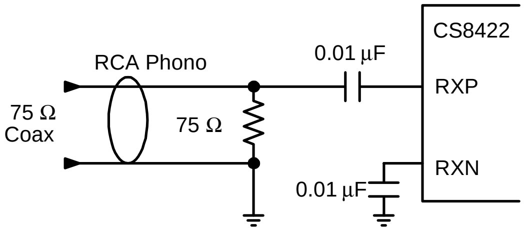

75 Ω Coax
75 Ω
.01µF
75 Ω Coax
75 Ω
.01µF
75 Ω Coax
75 Ω
.01µF
CS8422
RX3
RX2
RX0

Figure 28. S/PDIF MUX Input Circuit – Single-Ended


RCA Phono
75 Ω Coax
75 Ω
0.01 µF
0.01 µF
CS8422
RXP
RXN

Receiver Mode 1 Single-Ended Input Circuit – Differential Mode

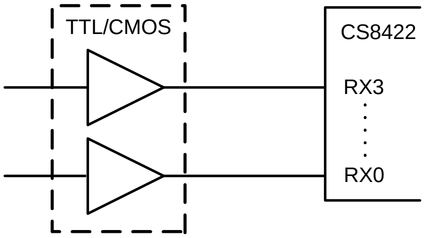

TTL/CMOS
CS8422
RX3
RX0

Figure 29. S/PDIF MUX Input Circuit – Digital Mode

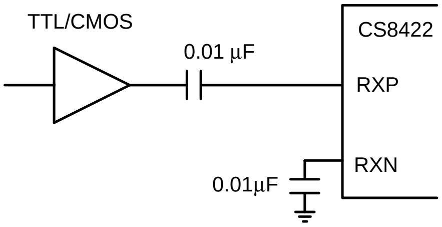
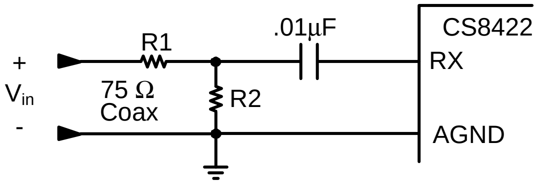

TTL/CMOS
0.01 µF
0.01µF
CS8422
RXP
RXN

Figure 30. TTL/CMOS Input Circuit – Differential Mode

12.3.1 Attenuating Input signals

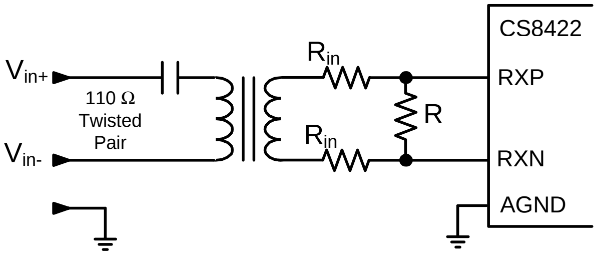
The input signals to the RX, RXP, and RXN pins in all modes of operation are limited to amplitudes equal to, or less than +3.3 V. In some cases it may be necessary to attenuate the input signal so the input to the device is within the valid operating range. Figures 31 and 32 illustrate how this should be done for both single-ended and differential inputs. In both cases, equations (1) and (2) must be satisfied simultaneously.



$$(1)\quad R2 = \frac{247.5}{V_{in}}$$

$$(2)\quad R1 = 75 - R2$$

Figure 31. Receiver Input Attenuation – Single-ended Input



$$(1)\quad R = \frac{726}{V_{in+} - V_{in-}}$$

$$(2)\quad R_{in} = 55 - \frac{R}{2}$$

Figure 32. Receiver Input Attenuation – Differential Input

12.3.2 *Isolating Transformer Requirements*

Please refer to the application note AN134: *AES and SPDIF Recommended Transformers* for resources on transformer selection

12.4 Channel Status Buffer Management

12.4.1 *AES3 Channel Status (C) Bit Management*

The CS8422 contains sufficient RAM to store the first 5 bytes of C data for both A and B channels (5 x 2 x 8 = 80 bits). The user may read from this buffer's RAM through the control port.

The buffering scheme involves two buffers, named D and E, as shown in Figure 33. The MSB of each byte represents the first bit in the serial C data stream. For example, the MSB of byte 0 (which is at control port address 23h) is the consumer/professional bit for channel status block A.

The first buffer (D) accepts incoming C data from the AES receiver. The 2nd buffer (E) accepts entire blocks of data from the D buffer. The E buffer is also accessible from the control port, allowing reading of the first five bytes of C data.

The complete C data may be obtained through the C pin in Hardware Mode and through one of the GPO pins in Software Mode. The C data is serially shifted out of the CS8422 clocked by the rising and falling edges of OLRCK or VLRCK.

There are a number of conditions that will inhibit the buffer update. If the CS_UPDATE bit in "Receiver Status (16h)" is set to '0', the only condition that will inhibit the update is PLL phase unlock. If the CS_UPDATE bit in "Receiver Status (16h)" is set to '1', a biphase, confidence, parity, or CRC error will also inhibit the update.

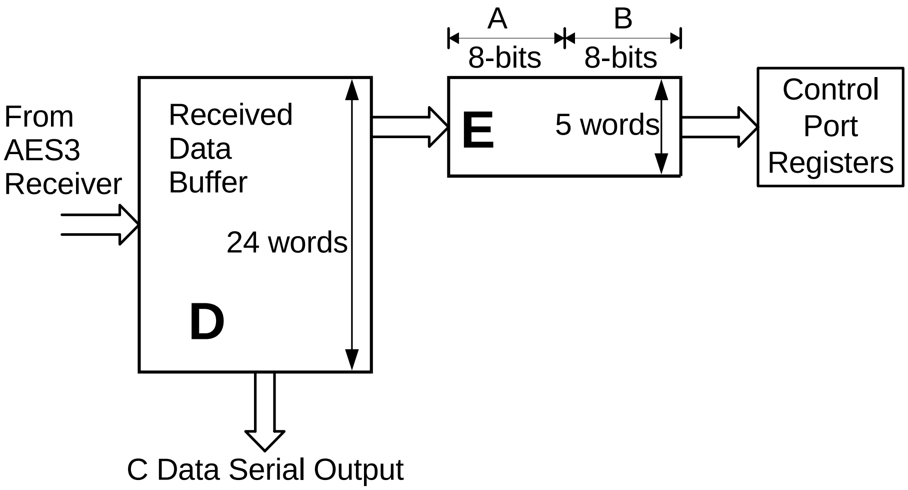

A
B
8-bits
8-bits
From
AES3
Receiver
Received
Data
Buffer
24 words
D
E
5 words
Control
Port
Registers
C Data Serial Output

Figure 33. Channel Status Data Buffer Structure

12.4.2 *Accessing the E buffer*

The user can monitor the incoming data by reading the E buffer, which is mapped into the register space of the CS8422, through the control port.

The user can configure the interrupt enable register to cause interrupts to occur whenever D to E buffer transfers occur. This allows determination of the allowable time periods to interact with the E buffer.

Also provided is a D to E inhibit bit in the "Receiver Data Control (04h)" register. This may be used whenever "long" control port interactions are occurring or for debugging purposes.

A flowchart for reading the E buffer is shown in Figure 34. Since a D to E interrupt occurs just after reading, there is a substantial time interval until the next D to E transfer (approximately 192 frames worth of time). This is usually enough time to access the E data without having to inhibit the next transfer.

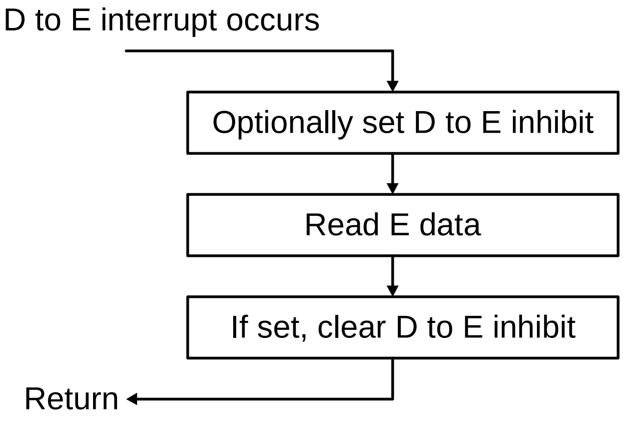

D to E interrupt occurs
Optionally set D to E inhibit
Read E data
If set, clear D to E inhibit
Return

Figure 34. Flowchart for Reading the E Buffer

12.4.3 Serial Copy Management System (SCMS)

In Software Mode, the CS8422 allows read access to all the channel status bits. For consumer mode SCMS compliance, the host microcontroller needs to read and interpret the Category Code, Copy bit and L bit appropriately.

In Hardware Mode, the SCMS protocol can be followed by using the C bit serial output pin. See "Channel Status and User Data Handling" on page 34 for more details.

12.5 Jitter Attenuation

Figure 35 shows the jitter attenuation characteristics of the CS8422 PLL. The AES3 and IEC60958-4 specifications state a maximum of 2 dB jitter gain.

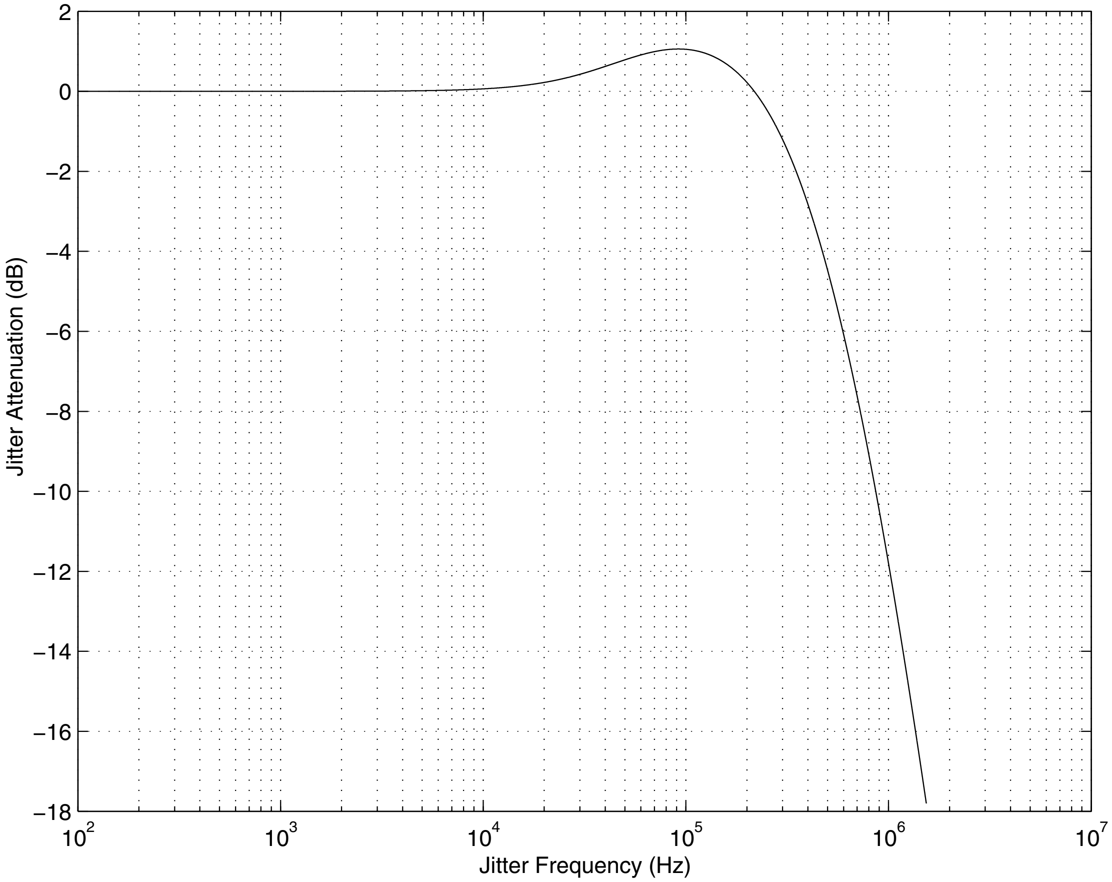


Figure 35. CS8422 PLL Jitter Attenuation Characteristics

12.6 Jitter Tolerance

Figure 36 shows the Receiver Jitter Tolerance template as illustrated in the AES3 and IEC60958-4 specification. CS8422 devices have been tested to pass this template.

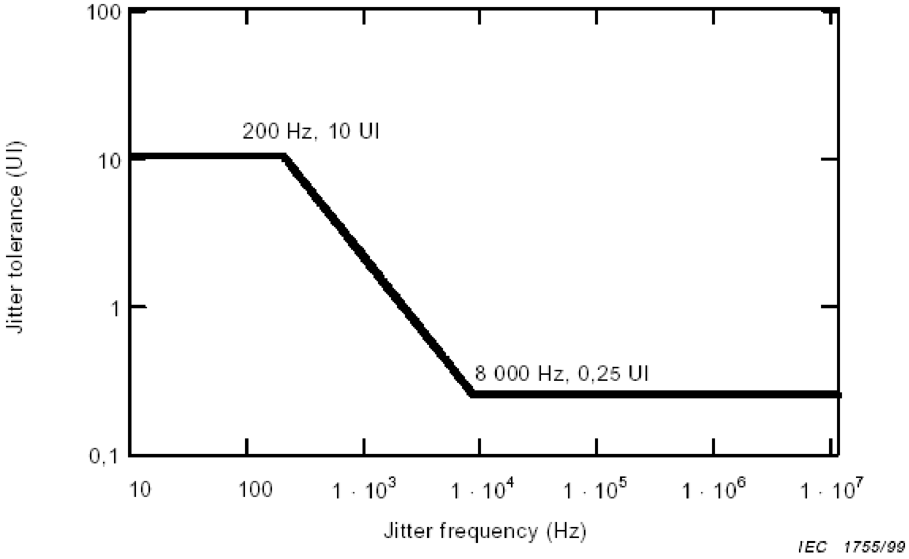


Figure 36. Jitter Tolerance Template

12.7 Group Delay

The group delay introduced by the CS8422 depends on the type of interface selected, and input and output sample rates of the sample rate converter. The expression for the group delay through the CS8422 with the use of the sample rate converter is shown below, where the interface delay is 3 OLRCK periods in all modes except AES3 direct mode, in which it is 2 OLRCK periods. If the sample rate converter is not being used, then the approximate group delay will be equal to the interface delay.

$$TotalGroupDelay = \left(\frac{8.7}{Fsi} + \frac{5}{Fso} + InterfaceDelay\right)$$

13.PERFORMANCE PLOTS

Test conditions (unless otherwise specified): Measurement bandwidth is 20 Hz to Fso/2 Hz (unweighted); VA = VL = V_REG = 3.3 V; XTI - XTO = 24.576 MHz; Input signal is a 0 dBFS 1 kHz sine wave; data resolution is 24 bits; Serial Audio Input and Output ports set to slave; Input and output clocks and data are asynchronous.

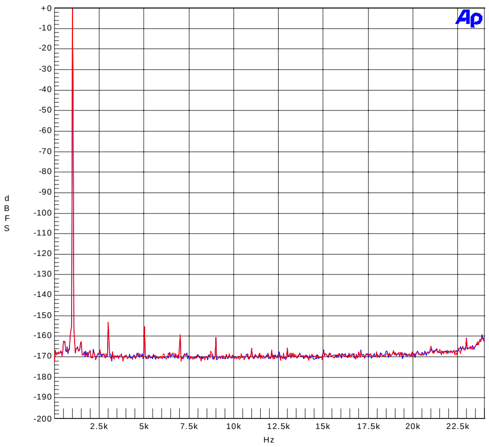


Figure 37. Wideband FFT – 0 dBFS 1 kHz Tone, 48 kHz:48 kHz

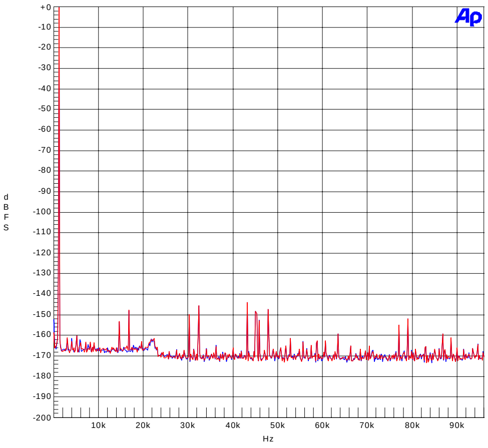


Figure 38. Wideband FFT – 0 dBFS 1 kHz Tone, 44.1 kHz:192 kHz

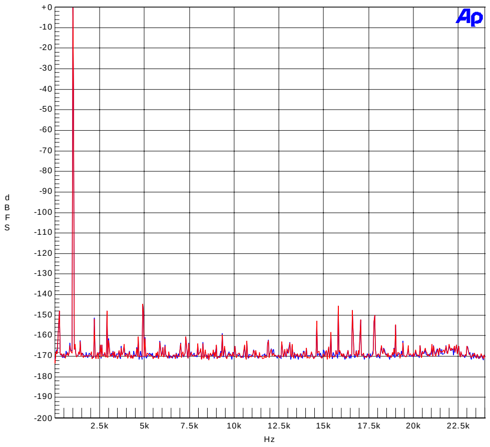


Figure 39. Wideband FFT – 0 dBFS 1 kHz Tone, 44.1 kHz:48 kHz

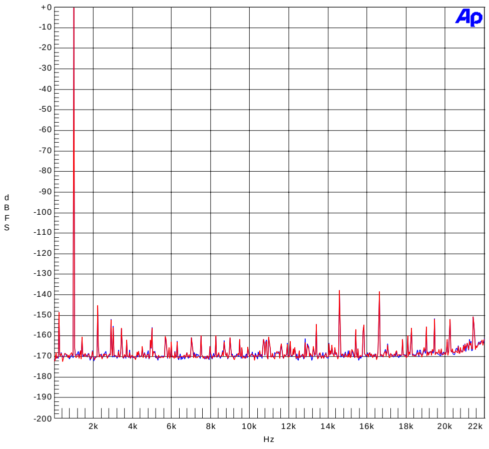


Figure 40. Wideband FFT – 0 dBFS 1 kHz Tone, 48 kHz:44.1 kHz

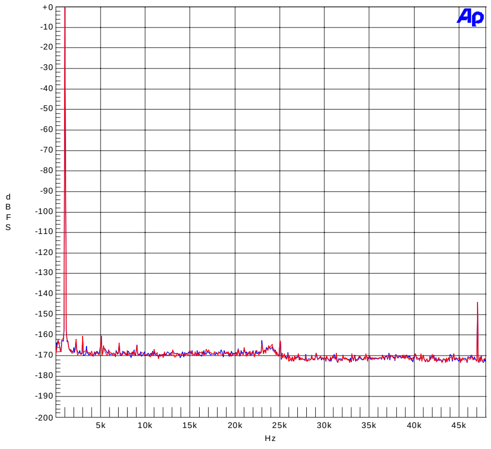


Figure 41. Wideband FFT – 0 dBFS 1 kHz Tone, 48 kHz:96 kHz

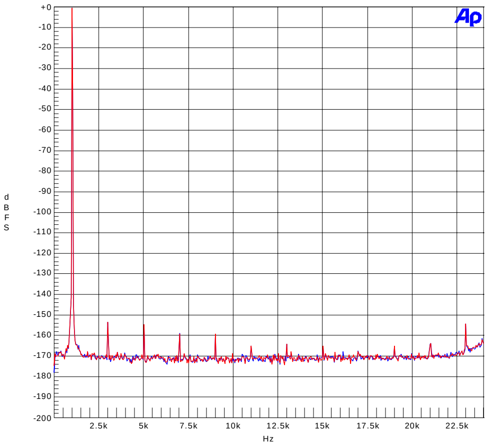


Figure 42. Wideband FFT – 0 dBFS 1 kHz Tone, 96 kHz:48 kHz

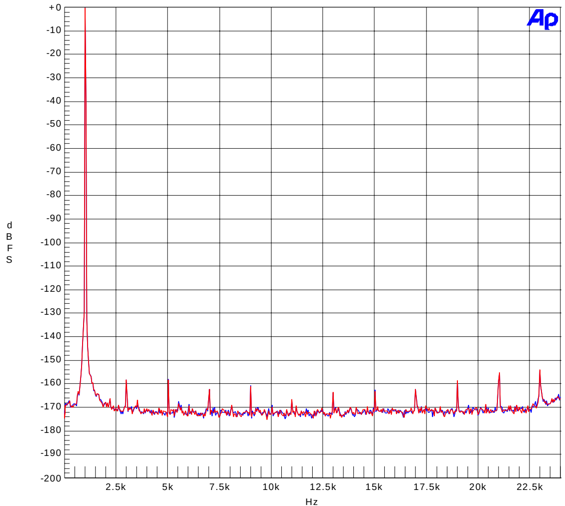


Figure 43. Wideband FFT –
0 dBFS 1 kHz Tone, 192 kHz:48 kHz

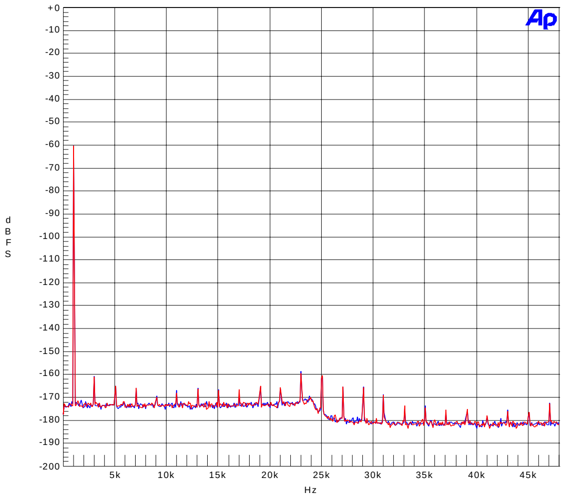


Figure 44. Wideband FFT –
-60 dBFS 1 kHz Tone, 48 kHz:96 kHz

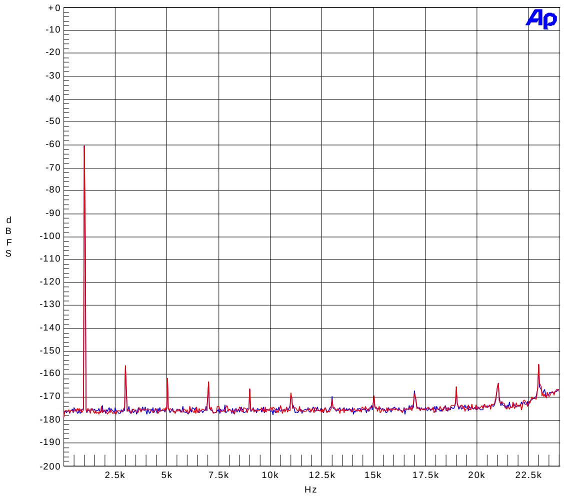


Figure 45. Wideband FFT –
-60 dBFS 1 kHz Tone, 48 kHz:48 kHz

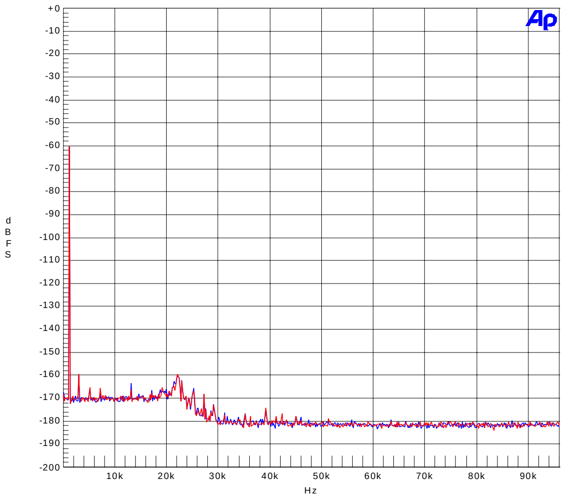


Figure 46. Wideband FFT –
-60 dBFS 1 kHz Tone, 44.1 kHz:192 kHz

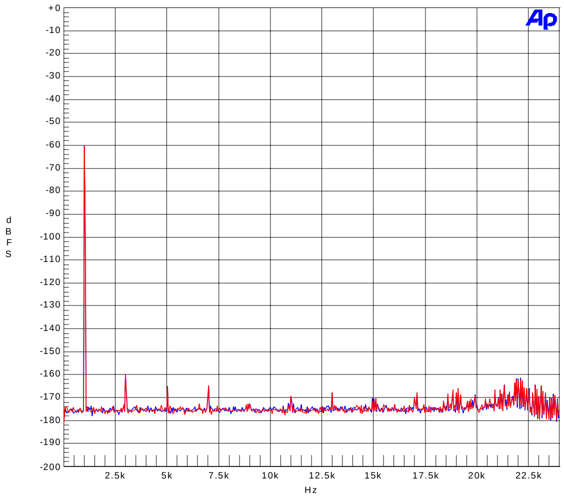


Figure 47. Wideband FFT –
-60 dBFS 1 kHz Tone, 44.1 kHz:48 kHz

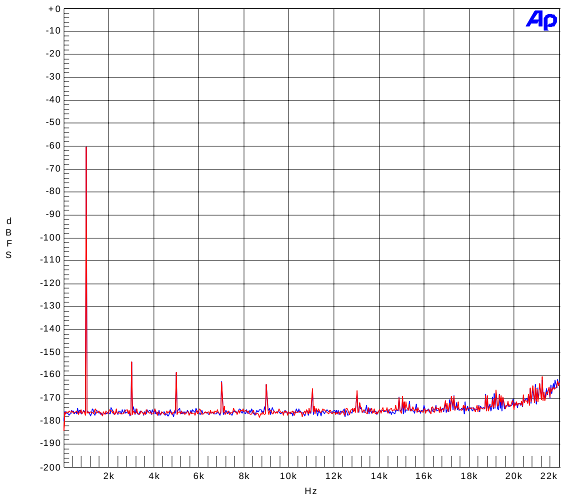


Figure 48. Wideband FFT –
-60 dBFS 1 kHz Tone, 48 kHz:44.1 kHz

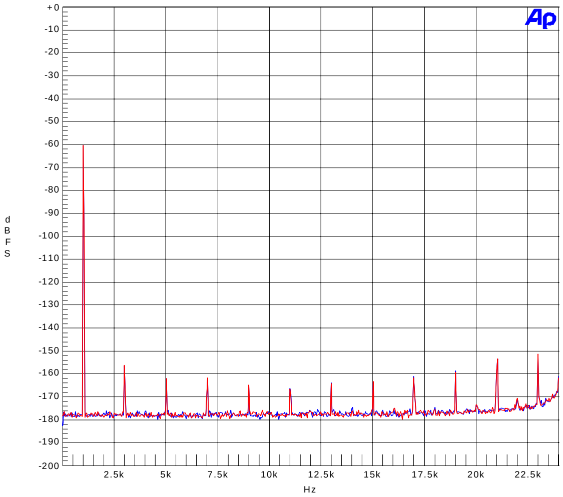


Figure 49. Wideband FFT –
-60 dBFS 1 kHz Tone, 96 kHz:48 kHz

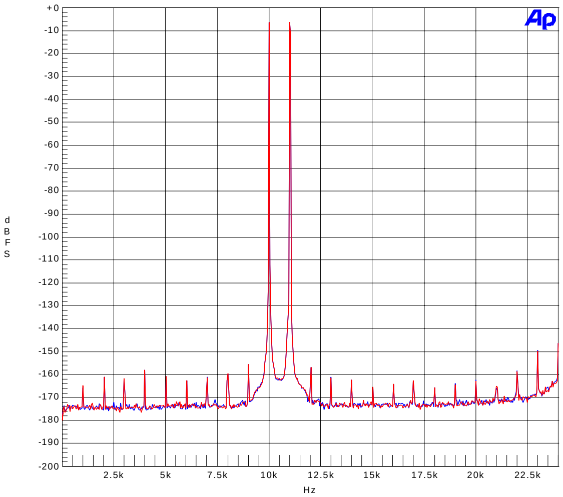


Figure 50. IMD –
10 kHz and 11 kHz -7 dBFS, 96 kHz:48 kHz

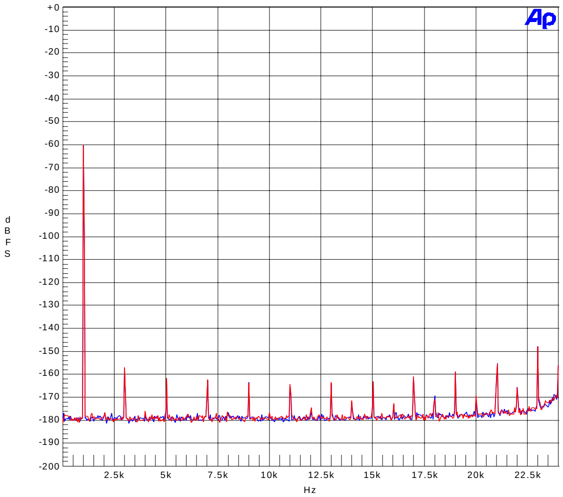


Figure 51. Wideband FFT –
-60 dBFS 1 kHz Tone, 192 kHz:48 kHz

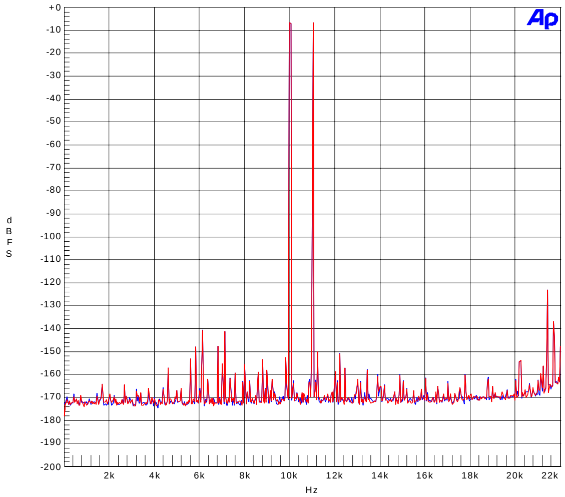


Figure 52. IMD –
10 kHz and 11 kHz -7 dBFS, 48 kHz:44.1 kHz

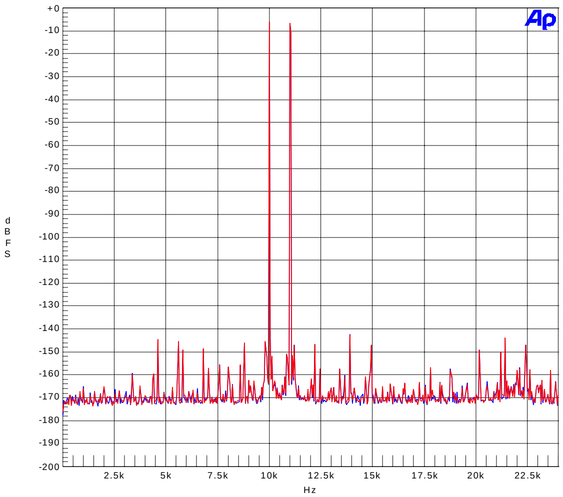


Figure 53. IMD –
10 kHz and 11 kHz -7 dBFS, 44.1 kHz:48 kHz

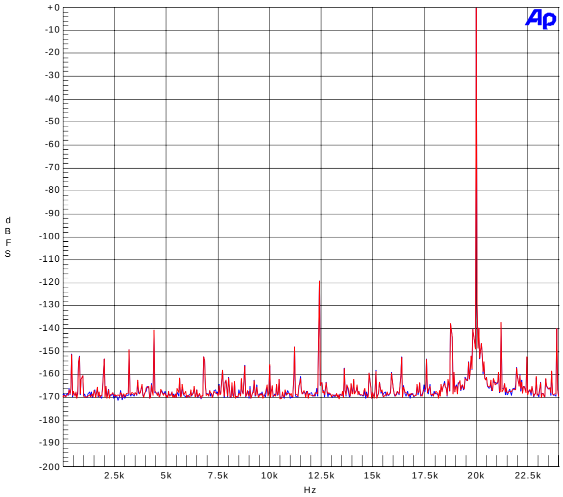


Figure 54. Wideband FFT –
0 dBFS 20 kHz Tone, 44.1 kHz:48 kHz

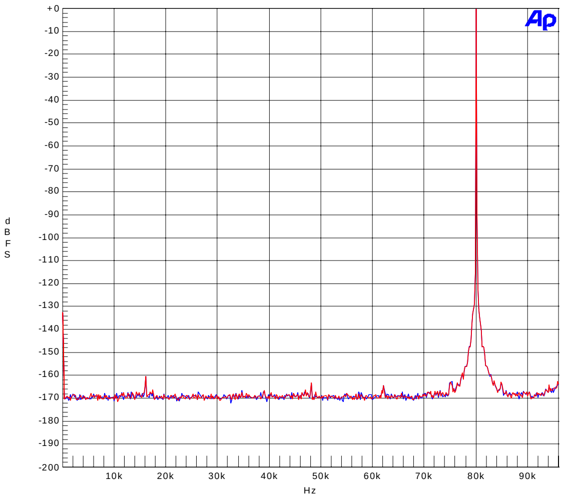


Figure 55. Wideband FFT –
0 dBFS 80 kHz Tone, 192 kHz:192 kHz

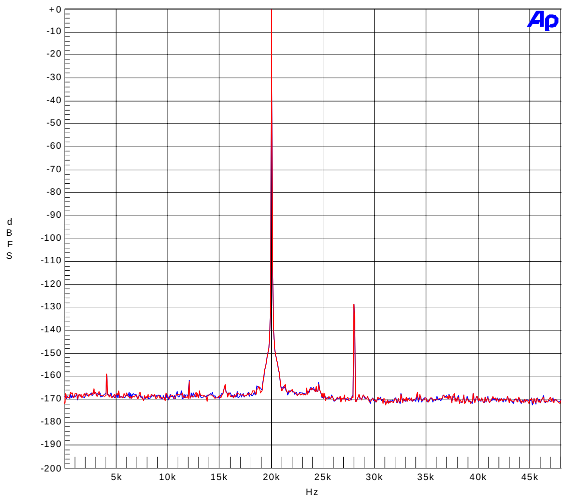


Figure 56. Wideband FFT –
0 dBFS 20 kHz Tone, 48 kHz:96 kHz

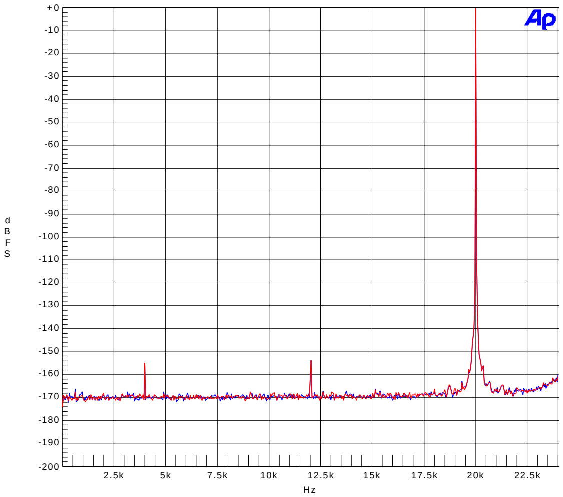


Figure 57. Wideband FFT –
0 dBFS 20 kHz Tone, 48 kHz:48 kHz

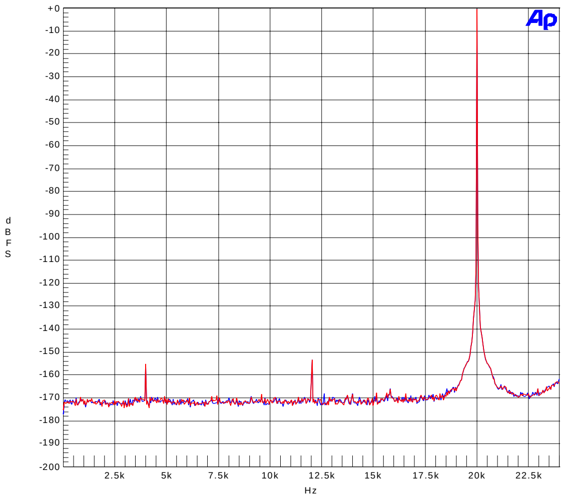


Figure 58. Wideband FFT –
0 dBFS 20 kHz Tone, 96 kHz:48 kHz

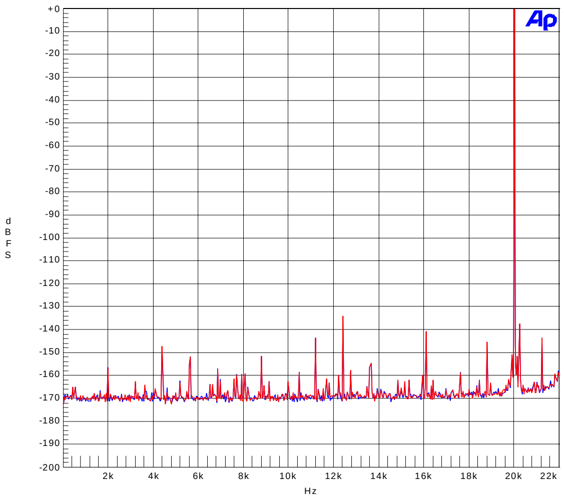


Figure 59. Wideband FFT –
0 dBFS 20 kHz Tone, 48 kHz:44.1 kHz

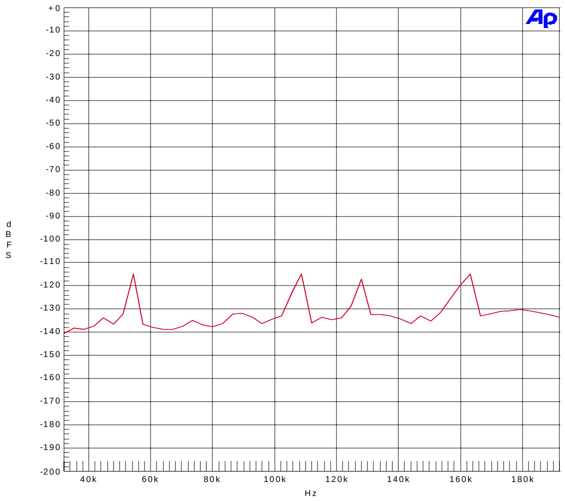


Figure 60. THD+N vs. Output Sample Rate –
0 dBFS 1 kHz Tone, Fsi = 192 kHz

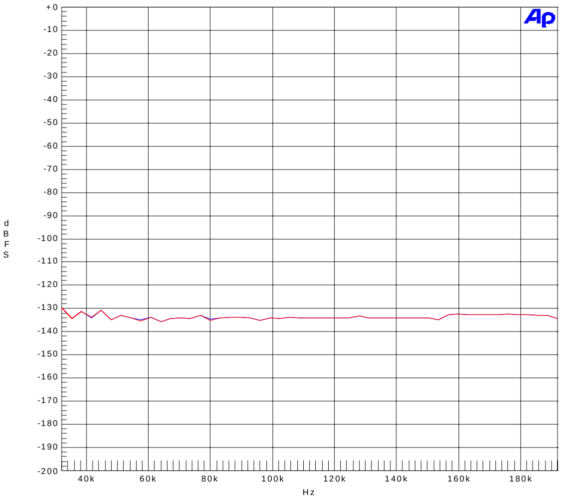


Figure 61. THD+N vs. Output Sample Rate – 0 dBFS 1 kHz Tone, Fsi = 48 kHz

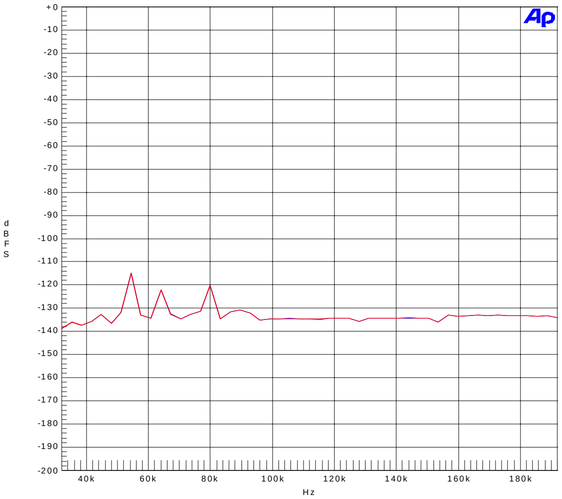


Figure 62. THD+N vs. Output Sample Rate – 0 dBFS 1 kHz Tone, Fsi = 96 kHz

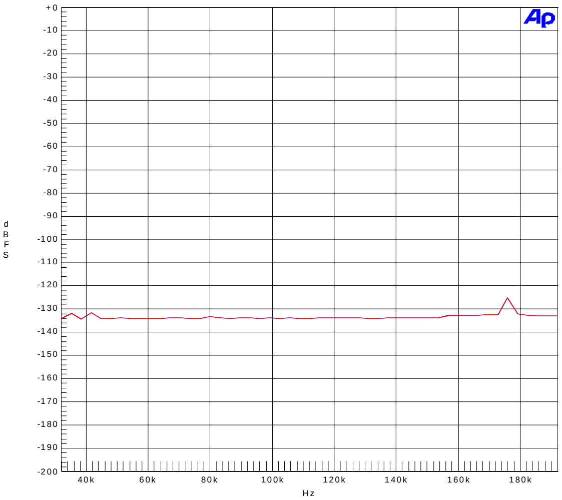


Figure 63. THD+N vs. Output Sample Rate – 0 dBFS 1 kHz Tone, Fsi = 44.1 kHz

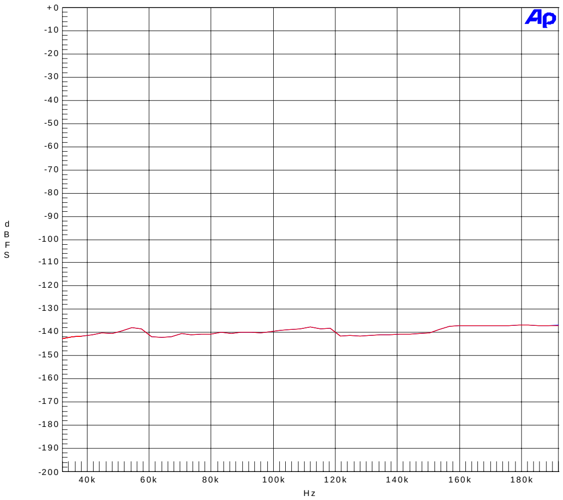


Figure 64. Dynamic Range vs. Output Sample Rate – -60 dBFS 1 kHz Tone, Fsi = 192 kHz

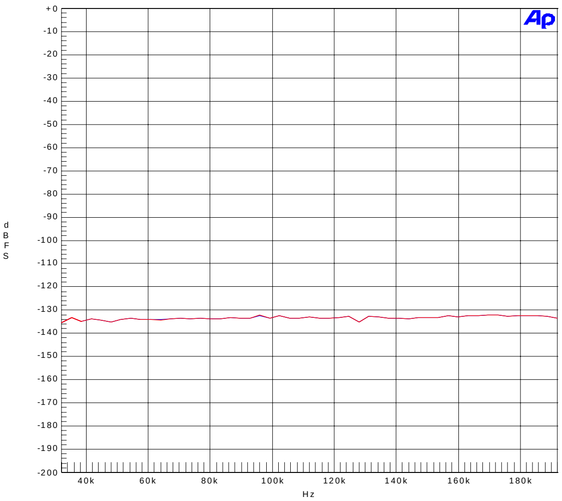


Figure 65. THD+N vs. Output Sample Rate – 0 dBFS 1 kHz Tone, Fsi = 32 kHz

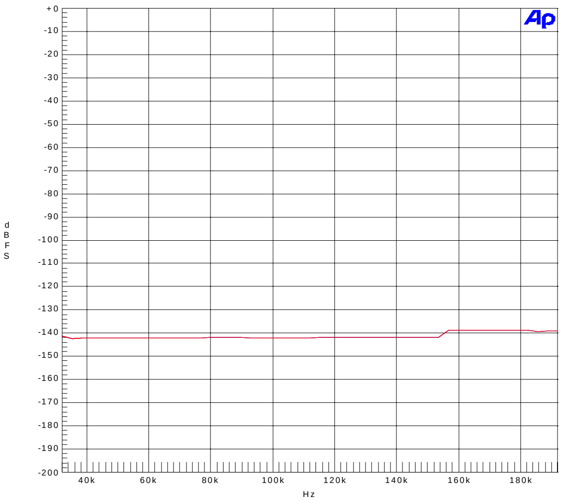


Figure 66. Dynamic Range vs. Output Sample Rate – -60 dBFS 1 kHz Tone, Fsi = 32 kHz

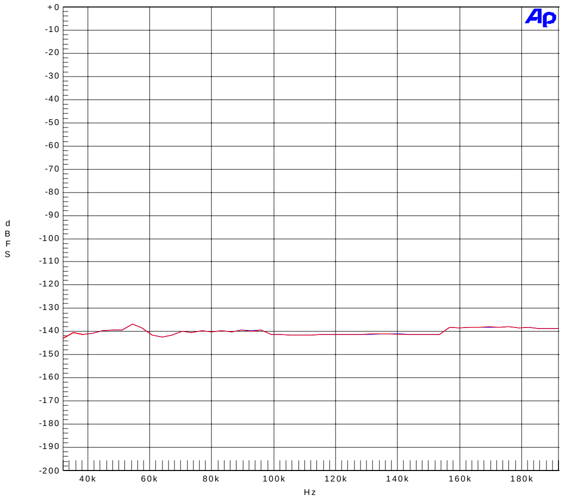


Figure 67. Dynamic Range vs. Output Sample Rate – -60 dBFS 1 kHz Tone, Fsi = 96 kHz

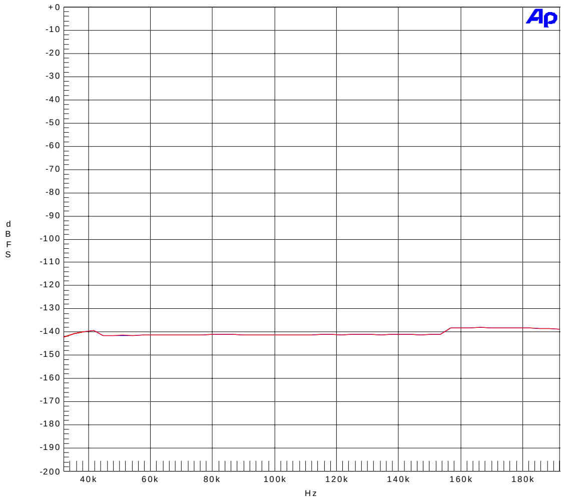


Figure 68. Dynamic Range vs. Output Sample Rate – -60 dBFS 1 kHz Tone, Fsi = 44.1 kHz

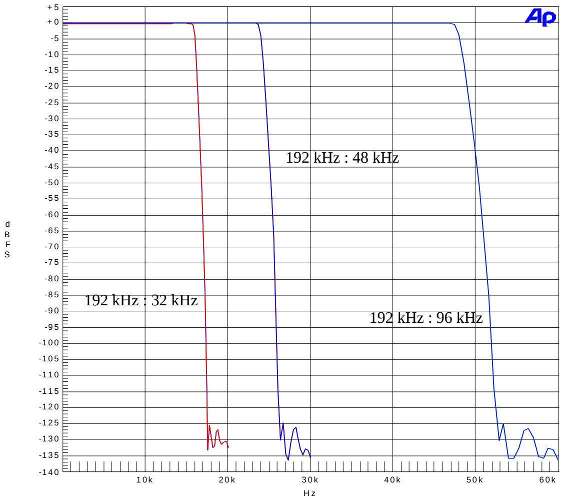


Figure 69. Frequency Response – 0 dBFS Input

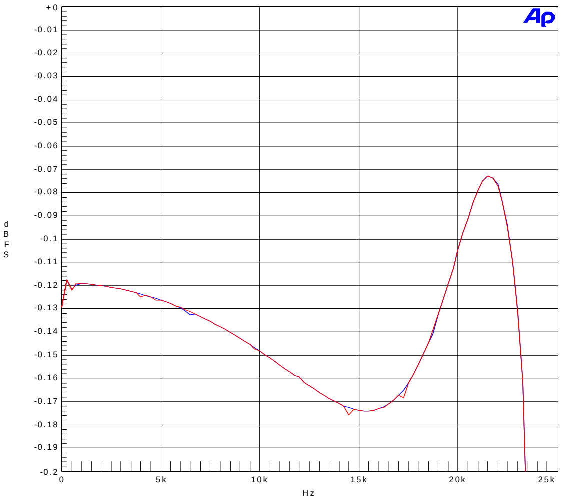


Figure 70. Passband Ripple – 192 kHz:48 kHz

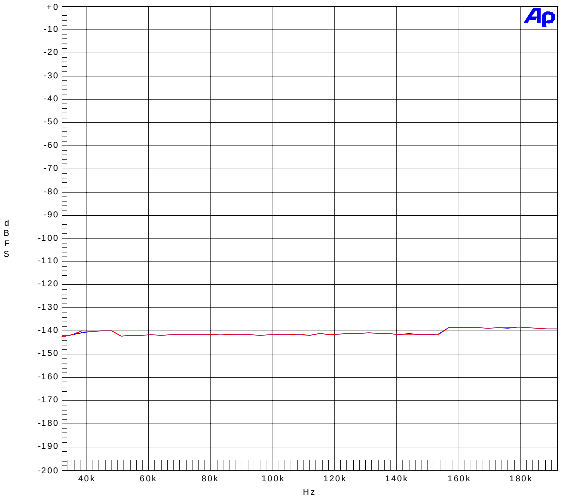


Figure 71. Dynamic Range vs. Output Sample Rate – -60 dBFS 1 kHz Tone, Fsi = 48 kHz

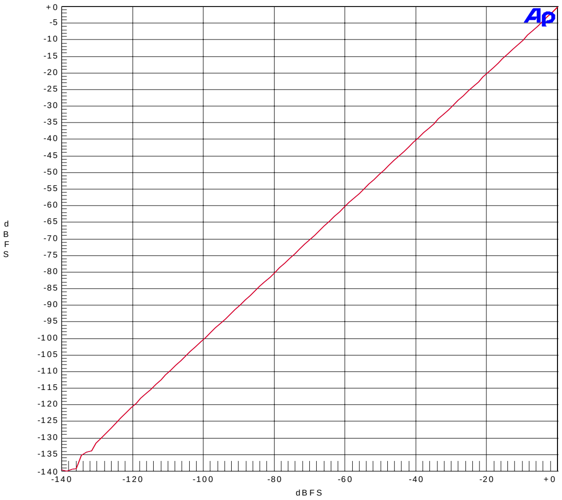


Figure 72. Linearity Error – 0 to -140 dBFS Input, 200 Hz Tone, 48 kHz:48 kHz

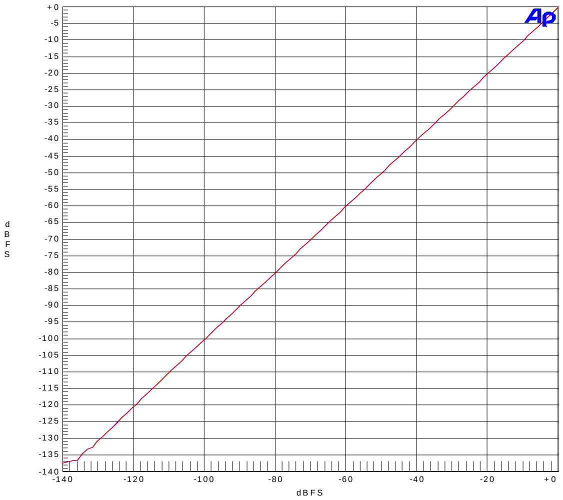


Figure 73. Linearity Error –
0 to -140 dBFS Input, 200 Hz Tone, 48 kHz:44.1 kHz

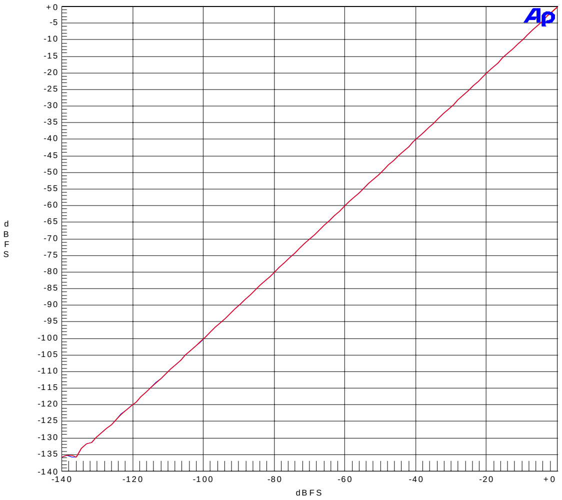


Figure 74. Linearity Error –
0 to -140 dBFS Input, 200 Hz Tone, 48 kHz:96 kHz

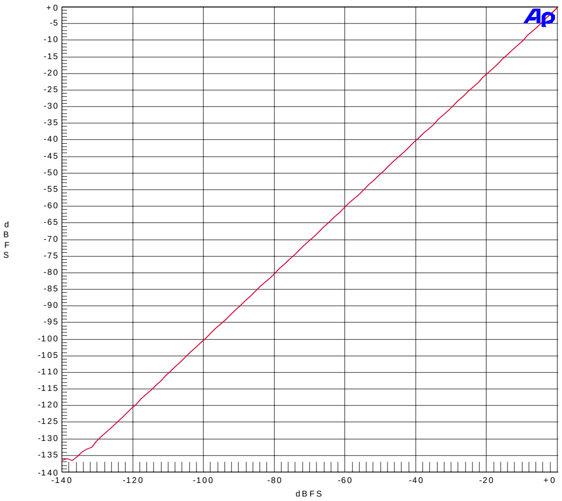


Figure 75. Linearity Error –
0 to -140 dBFS Input, 200 Hz Tone, 96 kHz:48 kHz

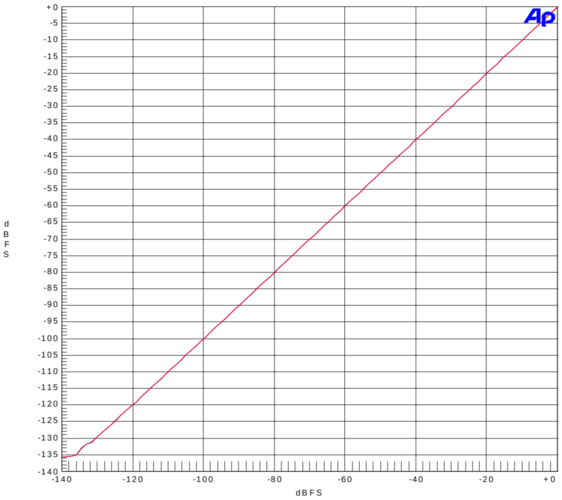


Figure 76. Linearity Error –
0 to -140 dBFS Input, 200 Hz Tone, 44.1 kHz:192 kHz

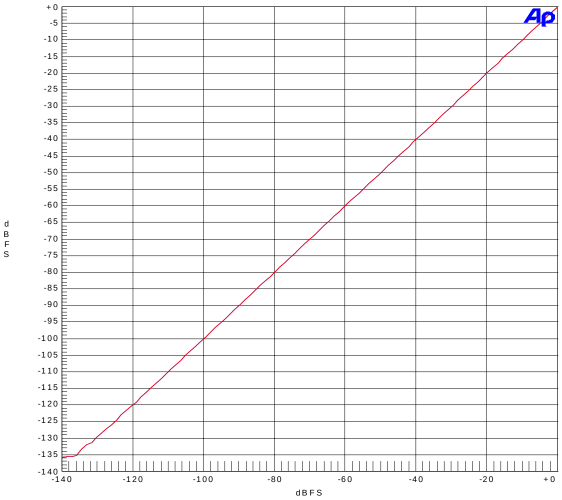


Figure 77. Linearity Error –
0 to -140 dBFS Input, 200 Hz Tone, 44.1 kHz:48 kHz

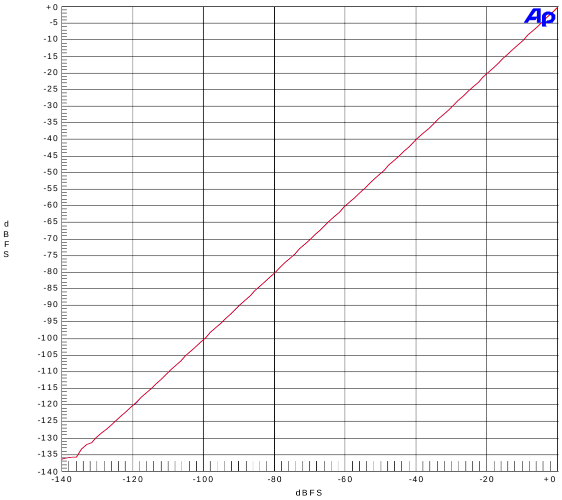


Figure 78. Linearity Error –
0 to -140 dBFS Input, 200 Hz Tone, 192 kHz:44.1 kHz

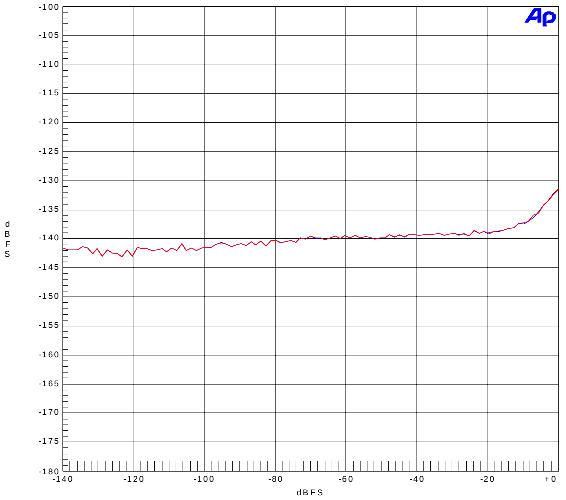


Figure 79. THD+N vs. Input Amplitude – 1 kHz Tone, 48 kHz:44.1 kHz

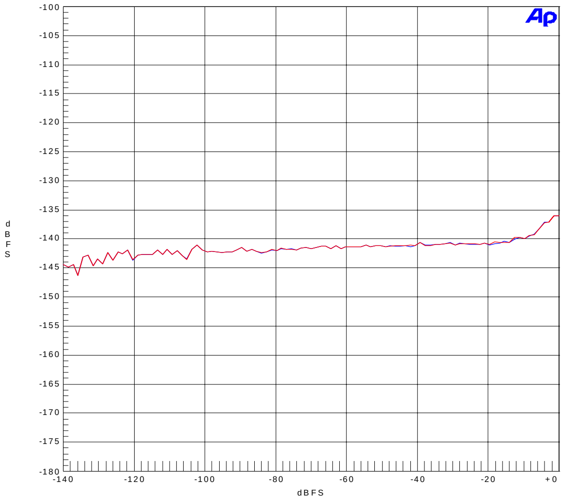


Figure 80. THD+N vs. Input Amplitude – 1 kHz Tone, 48 kHz:96 kHz

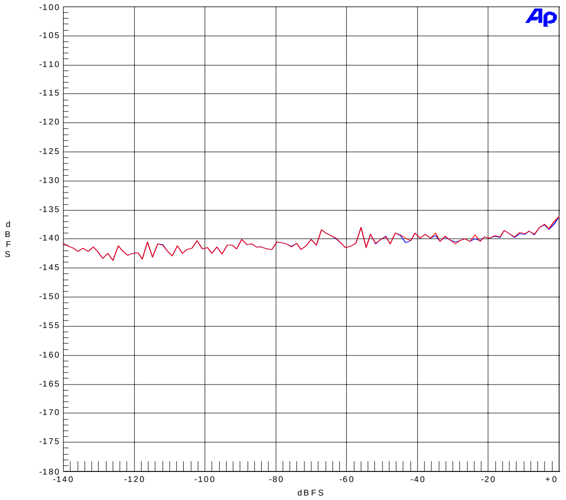


Figure 81. THD+N vs. Input Amplitude – 1 kHz Tone, 96 kHz:48 kHz

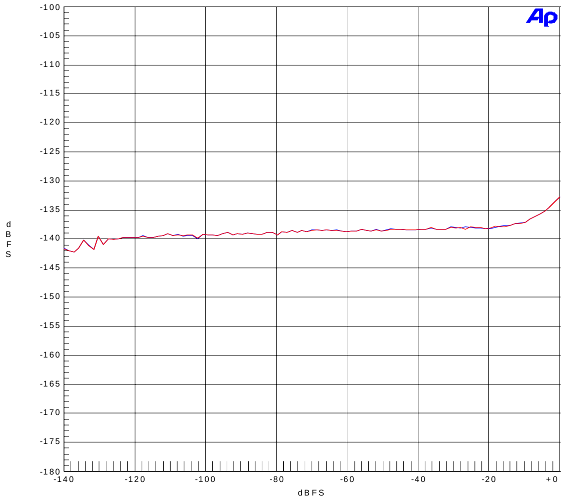


Figure 82. THD+N vs. Input Amplitude – 1 kHz Tone, 44.1 kHz:192 kHz

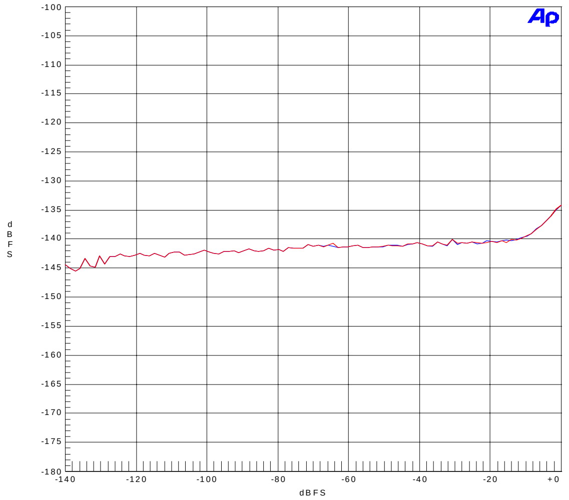


Figure 83. THD+N vs. Input Amplitude – 1 kHz Tone, 44.1 kHz:48 kHz

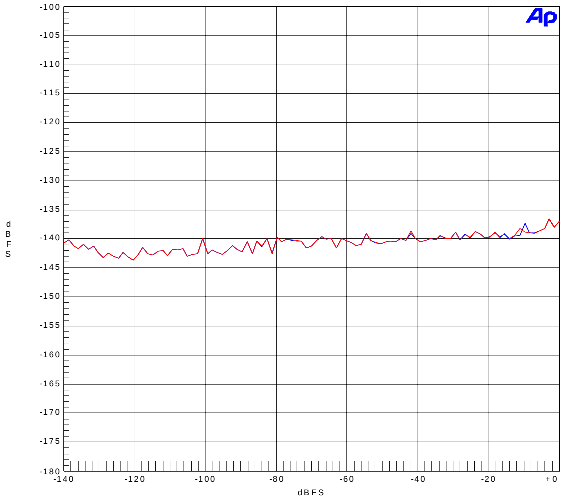


Figure 84. THD+N vs. Input Amplitude – 1 kHz Tone, 192 kHz:48 kHz

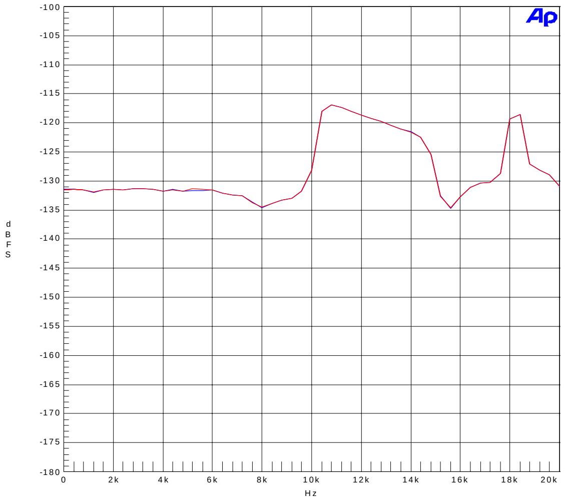


Figure 85. THD+N vs. Input Frequency – 0 dBFS, 48 kHz:44.1 kHz

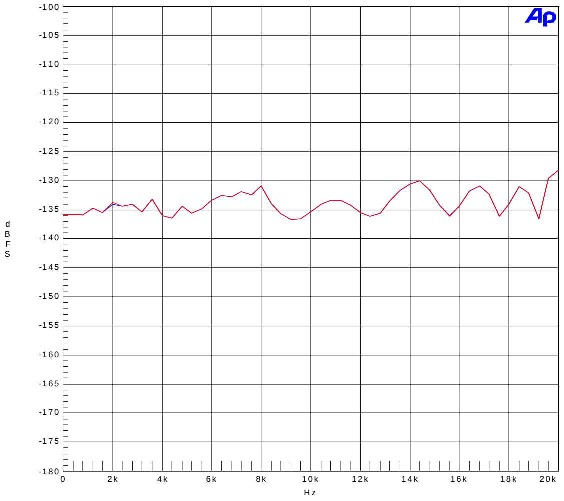


Figure 86. THD+N vs. Input Frequency – 0 dBFS, 48 kHz:96 kHz

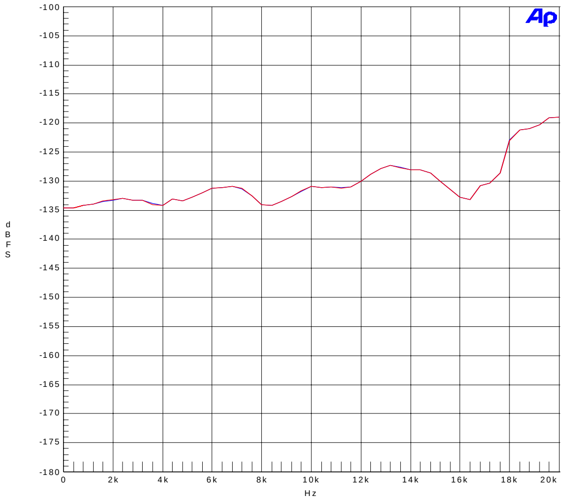


Figure 87. THD+N vs. Input Frequency – 0 dBFS, 44.1 kHz:48 kHz

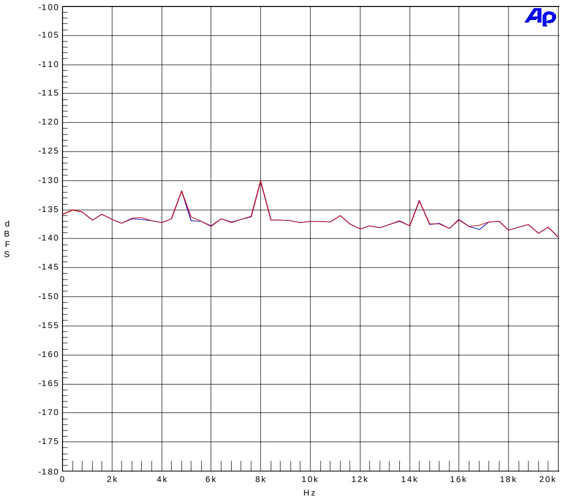


Figure 88. THD+N vs. Input Frequency – 0 dBFS, 96 kHz:48 kHz

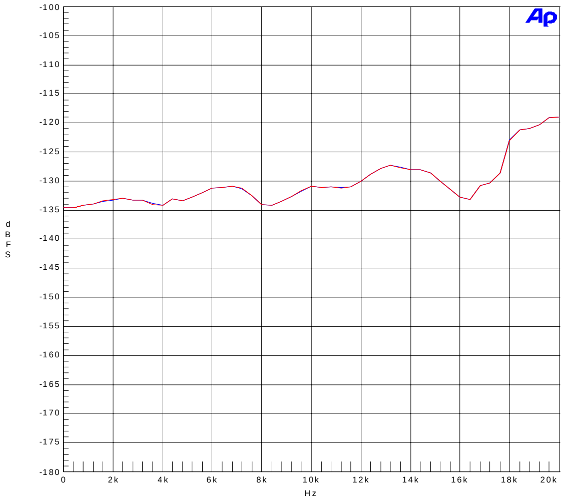
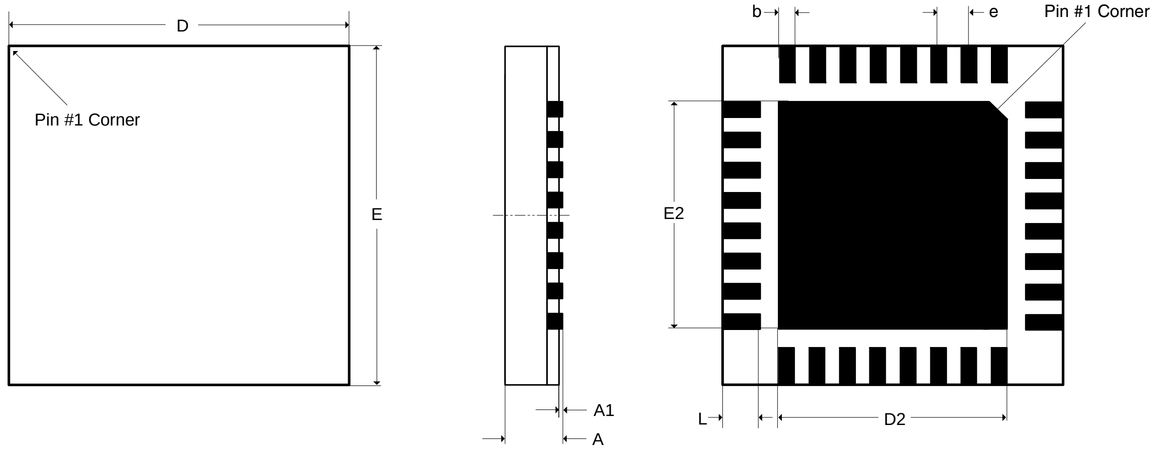


Figure 89. Total Power Supply Current vs. Differential Mode Receiver Input Sample Frequency

14.PACKAGE DIMENSIONS

32L QFN (5 X 5 mm BODY) PACKAGE DRAWING



Top View

Side View

Bottom View

	INCHES			MILLIMETERS			NOTE
DIM	**MIN**	**NOM**	**MAX**	**MIN**	**NOM**	**MAX**	
A	--	--	0.0394	--	--	1.00	1
A1	0.0000	--	0.0020	0.00	--	0.05	1
b	0.0071	0.0091	0.0110	0.18	0.23	0.28	1,2
D		0.1969 BSC			5.00 BSC		1
D2	0.1280	0.1299	0.1319	3.25	3.30	3.35	1
E		0.1969 BSC			5.00 BSC		1
E2	0.1280	0.1299	0.1319	3.25	3.30	3.35	1
e		0.0197 BSC			0.50 BSC		1
L	0.0118	0.0157	0.0197	0.30	0.40	0.50	1

JEDEC #: MO-220
Controlling Dimension is Millimeters.

Notes:

1. Dimensioning and tolerance per ASME Y 14.5M-1995.
2. Dimensioning lead width applies to the plated terminal and is measured between 0.20 mm and 0.25 mm from the terminal tip

15.THERMAL CHARACTERISTICS AND SPECIFICATIONS

Parameters	Symbol	Min	Typ	Max	Units
Package Thermal Resistance (Note 1)	θ_{JA}	-	38	-	°C/Watt
Allowable Junction Temperature		-	-	125	°C

Notes:

1. θ_{JA} is specified according to JEDEC specifications for multi-layer PCBs.

16.ORDERING INFORMATION

Product	Description	Package	Pb-Free	Grade	Temp Range	Container	Order#
CS8422	24-bit, Asynchronous Sample Rate Converter with Integrated Digital Interface Receiver	QFN	YES	Commercial	-40° to +85°C	Rail	CS8422-CNZ
						Tape and Reel	CS8422-CNZR
				Automotive	-40° to +105°C	Rail	CS8422-DNZ
						Tape and Reel	CS8422-DNZR
CDB8422	Evaluation Board for CS8422	-	YES	-	-	-	CDB8422

17.REFERENCES

1. Audio Engineering Society AES3-2003: *“AES standard for digital audio - Digital input-output interfacing - Serial transmission format for two-channel linearly represented digital audio data,”* September 2003.
2. Audio Engineering Society AES-12id-2006: *“AES Information Document for digital audio measurements - Jitter performance specifications,”* May 2007.
3. Philips Semiconductor, “*The I^{2}C-Bus Specification: Version 2*,” Dec. 1998.
   http://www.semiconductors.philips.com

18.REVISION HISTORY

Release	Changes
PP1	Added interchannel phase deviation to Performance Specifications - Sample Rate Converter table Added gain error to Performance Specifications - Sample Rate Converter table Added 32 kHz:48 kHz dynamic range to Performance Specifications - Sample Rate Converter table Updated (Note 2) in Performance Specifications - Sample Rate Converter table Updated values in DC Electrical Characteristics table Changed (Note 3) and (Note 4) in DC Electrical Characteristics table Updated RMCK jitter specification in Switching Specifications table Changed (Note 9) in Switching Specifications table Moved SDIN/TDM_IN setup and hold times in Switching Specifications table Changed master mode non-TDM I/OSCLK minimum frequency in Switching Specifications table Changed t_{srs} value in Switching Characteristics - Control Port - SPI mode Changed t_{irs} value in Switching Characteristics - Control Port - I²C mode Fixed calculation error in Section 5.1.5.2 TDM Slave Mode Added note to Section 11.9 Recovered Master Clock Ratio Control & Misc. (09h) Added Section 12.6 Jitter Tolerance Added Section 13. Performance Plots Added Section 17. References Updated VIH minimum specification in Digital Interface Specifications table Updated VIL maximum specification in Digital Interface Specifications table Updated Input Hysteresis specification in Digital Interface Specifications table Added (Note 6) to Digital Interface Specifications table Removed VIH maximum specification in Digital Interface Specifications table Removed VIL minimum specification in Digital Interface Specifications table

Contacting Cirrus Logic Support

For all product questions and inquiries, contact a Cirrus Logic Sales Representative.
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