Practical Hints for Enhancing EMC Performance with Atmel ATA6612/ATA6613

Atmel ATA6612
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Application Note

1. Description

Highly integrated solutions such as the Atmel® ATA6612/ATA6613 automotive-grade system-in-package (SiP) development board help designers easily develop complete LIN-bus slave-node applications. In addition to an integrated LIN transceiver, a 5V regulator and a window watchdog, it also includes an automotive microcontroller from the Atmel AVR® 8-bit microcontroller series featuring advanced RISC architecture. While the powerful, integrated microcontroller gives the design engineer full freedom for any LIN-node development, its flexibility also requires that EMC be given individual consideration for each application. This application note provides some guidance and practical hints on how the electromagnetic compatibility of your Atmel ATA6612/ATA6613 application can be optimized in order to meet stringent requirements.

Those involved in the field of electronics, especially in the automotive sector, will certainly have been confronted by EMC-related issues more than once already. The phenomenon of radio interference is nearly as old as the invention of radio itself, and at an early stage led to the definition of guidelines for noise suppression. The other aspect of EMC, immunity against distortions, only began to attract attention around fifty years ago. As operating frequencies for electronic (especially mobile) equipment are constantly attaining higher values, smaller structures can behave like an antenna and cross-coupling needs to be considered even for relatively small coupling capacitances. It is therefore only natural that in recent decades there has been a growing need to define certain rules of the game.

Nowadays all car manufacturers are highly aware of the fact that EMC testing is an important part of car electronics development, and understand that EMC issues become more costly the later they are discovered. That is the reason why they do not simply rely on a final test inside the car, but insist on tests of the electronic control unit (ECU), and even on test results for integrated circuits used in the design before deployment in vehicles. Especially ECUs incorporating wire-less functionality or bus line transceivers are regarded as critical due to the fact that antennas or long wiring harnesses are connected to them. A wide variety of testing methods have been developed all over the world for both unwanted electromagnetic emissions as well as the susceptibility to electromagnetic distortion. In the meantime, all integration levels are covered, and over the past 10 years the various standardization committees have devoted their time to the IC level. Unfortunately, not only have quite a large number of different standards been established (perhaps the bane of testing specialists), but at the same time many OEMs apply these standards in slightly different ways.

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Two different types of measurements can be distinguished in the case of emission as well as susceptibility tests:

- The radiated measurements, involving an antenna, a coupling clamp, a magnetic or electric probe, a stripline, or a TEM cell
- Measurements carried out using galvanic coupling to certain ports to measure or inject RF signals

The “classic” EMC tests at the IC level measure the emissions in varying frequency bands at defined frequency steps, dwell times, measurement bandwidths, and detector types, as well as measuring immunity by applying an unmodulated or AM-modulated RF signal of defined amplitude, again while varying the frequency at defined steps. These tests are specified in the international standards IEC 61967 for emission and IEC 62132 for immunity. Currently these standards are supplemented by new test standards for pulse measurements.

Most ports at the IC level are designed to be connected internally on the PCB only while only a few ports, such as supply pins, bus lines, or antenna pins, are connected externally. While EMC requirements are less stringent for local (internal) ports, global (external) ports are far more critical, because the cable lengths involved increase the cross-coupling between different lines or they may behave as an undesired antenna for RF signals. Certainly a few ports like the Atmel® ATA6612/ATA6613 LIN-bus line are external ports by definition, but for most ports it is the application that determines whether these need to be treated as local or global ones.

The good news is that designing circuits and board layouts which are robust will not only ensure an assembly works better and is more dependable, but in most cases will also help to achieve the required performance regarding both electromagnetic emissions and immunity. Furthermore, Atmel has already eliminated some of the burden on the circuit designer by performing EMC compliance tests on the most critical external LIN and supply pins. Nevertheless, as mentioned at the beginning, the flexibility of the integrated AVR® controller necessitates an individual strategy for EMC performance optimization. Having said this, how can circuit design be achieved which is that robust? Of course, there are a few general rules which help to improve the EMC behavior of the circuit:

- Careful consideration should be given to what clock frequency is really needed for the development application. The lowest possible clock frequency should be chosen, because this is the first measure which will reduce electromagnetic emissions.
- Normally, for LIN slave node applications precise clock generation using an external crystal is not required, as the slave node will synchronize with the LIN master’s accurate clock. Using the Atmel ATA6612/ATA6613 internal clock generation will avoid routing the clock signal with its fast slopes via the PCB, and will thus help reduce emissions.
- Atmel ATA6612/ATA6613 has two GND pins (GND1, GND2) that are related to certain VCC pins (MCUVDD1 and MCUVDD2 respectively) - designers should take this knowledge into account and place decoupling caps as close as possible between the related pin pairs. Good decoupling is essential because the supply lines are global pins. An example of a good PCB layout is depicted in Figure 1-1 on page 4. The two capacitors C2 and C8 are placed directly between MCUVDDx and the respective GND pin with the shortest connections. If a pair of capacitors is used as shown in Figure 1-2 on page 5, the smaller value (C8 and C2) need to be placed closer to the IC than the larger values (C14 and C15).
- High-impedant microcontroller ports are susceptible to RF distortions; therefore, impedance should be kept as low as acceptable or a low-impedance path to GND for the RF disturbance should be provided.

- Ports that are connected on the outside of the ECU require special attention. Where possible, the prototype should allow for decoupling capacitors to GND and series resistors - 10 to 100Ω are often acceptable. Values higher than this will result in a more efficient filter but also cause a higher voltage drop for DC signals. If emission of a particular port is the problem, one end of the resistor is connected to the port while the capacitor is on the other side. The layout example in Figure 1-4 on page 6 shows such RC filters, assuming that pins 10, 11, and 12 carry switched signals. The components are arranged inversely to protect a port against RF distortions the components. For frequencies > 10MHz ferrite beads may be more efficient than only using small resistors and, as a further benefit, their DC resistance is negligible, meaning that the circuit will not suffer from a drop in voltage.
- It should be remembered that for higher frequencies a capacitor functions not only as a capacitor but also has some inherent, built-in parasitic components such as series inductance and resistance - known as equivalent series resistance (ESR) - to name only the most important components with adverse effects. Because the correct choice and placement of decoupling capacitors is of vital importance, this will be discussed in more detail below.
- In addition, resistors need to be regarded as a more complex component (highly dependent on the type of construction and also on the resistance value). Fortunately, for a typical low-ohmic thin film resistor such as those used for building EMC filters, the contribution of its parasitic components is largely negligible up to 1GHz.
- When developing the PCB layout, the different circuit blocks should be arranged in such way that sufficient space around sensitive inputs is provided towards switched signals of high amplitude and/or frequency because of the possible interferences these signals may cause. Having parallel tracks on a board provides good coupling between the signals on these tracks - if this kind of coupling is not desired, insert some GND area between the tracks; should these tracks cross each other at different layers, have the tracks cross at right angles to minimize the coupling area. An example for improving the decoupling between adjacent tracks is shown in the four-layer PCB designs in Figure 1-5 on page 6 and Figure 1-6 on page 7, assuming that the ports at pins 10,11, and 12 are carrying switched signals and need to be decoupled from each other as well as from pin 9. While there are tiny “fingers” of the GND plane between the tracks in Figure 1-5 on page 6, the decoupling can be improved by inserting some vias which connect to the GND plane in the first inner layer and the bottom layer as illustrated in Figure 1-6 on page 7.
- Keep tracks as short as possible, especially those carrying switched signals with fast slopes or RF. Critical parts of the circuit such as tuners may require shielding. The highest frequency the circuit produces or is exposed to should be considered, and the track length of critical connections kept below 1/10 of the wavelength. Two considerations must be kept in mind here:
  First, the wavelength λ on the PCB is shortened due to ε_r of the board material; for FR4 this is typically around 4.5. However the effective ε_r will be somewhat lower, because part of the electric field of a micro strip line is in free space. For a frequency of 3GHz the formula

$$\lambda = \frac{c}{f \times \sqrt{\varepsilon_r}}$$

  reveals that a track length of about 50mm already equals λ/10. Secondly, the highest frequency in the circuit is determined by the fastest slopes - so if some parts of the design operate at 1MHz but with slopes of 1ns, there will be frequencies of at least 500MHz on the PCB.

- The ground plane should be designed as solidly as possible, preferably using a multilayer PCB with dedicated layers for GND and power planes. Typically the signal layers will be on the top and bottom side of the PCB and the GND/power planes on the inner layers. A solid ground area underneath the Atmel® ATA6612/ATA6613 heat slug is very important, with preferably 9 vias to the inner ground plane in case of multilayer or to the bottom layer ground plane in case of a two-layer board. Figure 1-3 on page 5 shows an example of a recommended footprint, even with 16 vias in the center pad (note: the other layout example figures don't show these vias; as they are part of the IC footprint library element they are not displayed in standard printouts). It is beneficial to keep the distance between signal layer and adjacent GND/power plane to a minimum. Doing so helps achieve relatively low track impedance even for fairly thin connections. Slots in the GND plane should be avoided to prevent creating unwanted slot antennas. In addition, small "islands" should be avoided, different GND areas need to be connected using a sufficient number of vias (one via every 3mm to 5mm is sufficient for most designs).
- Differential signals must be routed close to each other with the same track length for both lines. Avoid generating large loops and keep the path for the return current in mind. The larger the area of a loop the higher the susceptibility and the lower the frequencies which may affect the circuit. Analogously, this is valid for emission, too - any tracks forming a loop with an RF current flow can behave like a loop antenna.
- Hopping between the layers should be kept to a minimum during board development (except for signal tracks which carry only static signals or very low frequencies). Every via, especially "long" ones from top to bottom layer, involve some inductance; as a rule of thumb this is in the range of 0.5nH to 1nH. Particular care needs to be taken about GND connections of decoupling capacitors. Atmel highly recommends placing several vias in parallel close to the respective capacitor. This can be seen in layout example Figure 1-2 on page 5 where most capacitors have at least one dedicated via to GND (C3, C5, C6, C7,…) and the most critical capacitors C2 and C8 both use two vias.

Figure 1-1. PCB Layout Example for VCC Decoupling

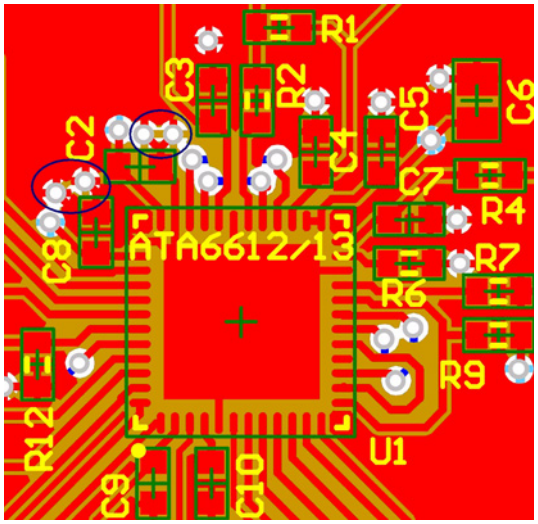


Figure 1-2. PCB Layout Example for Improved VCC Decoupling

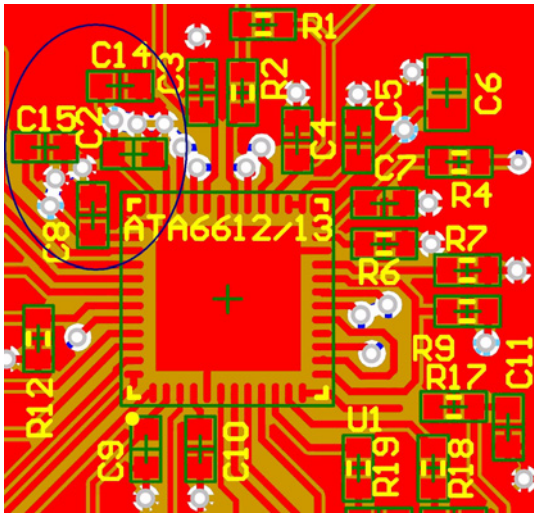


Figure 1-3. PCB Layout Example for Atmel® ATA6612/ATA6613 Central Pad

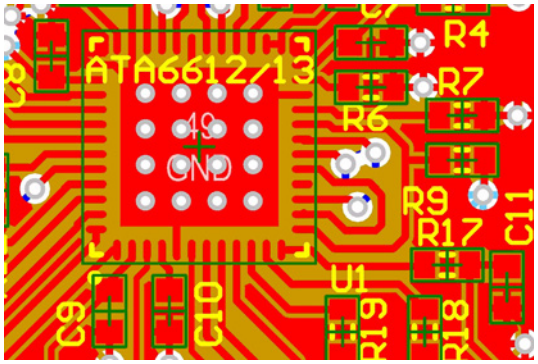


Figure 1-4. PCB Layout Example for RC Filters in Switched Signal Lines

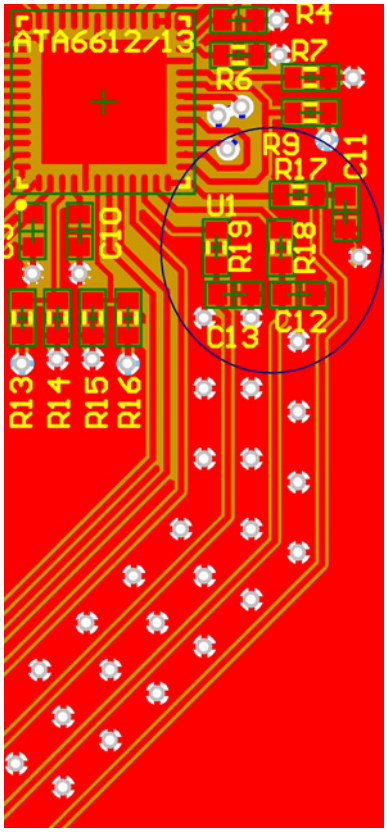


Figure 1-5. PCB Layout Example for Signal Track Decoupling

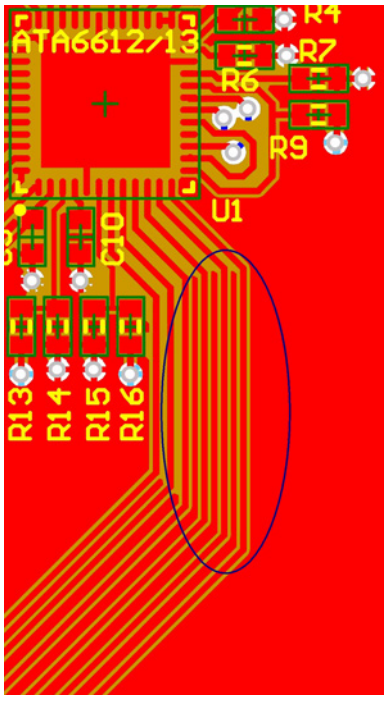
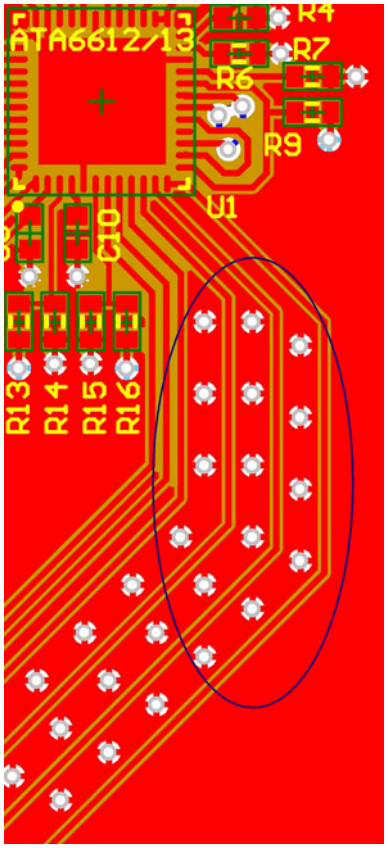


Figure 1-6. PCB Layout Example for Improved Signal Track Decoupling



2. Equivalent Circuit Model of the Capacitor

In the capacitor's equivalent circuit model, the simplest model comprises only a serial connection of the nominal capacitor, an equivalent series resistance and a parasitic series inductance. The ESR determines the lowest impedance reached at the capacitor's series resonance. Above this series resonance the capacitor's impedance will increase with frequency, thus behaving like an inductor. A more sophisticated model would also include the components C_p and R_p, connected in gray in Figure 2-1. Modified equivalent circuits are also found in literature which show C_p and R_p in parallel to the whole serial connection of (desired) capacitor, ESR and parasitic inductance; it is merely a question of transforming the values of the respective inherent components. The parasitic inductance together with C_p leads to a parallel resonance that is frequently neglected, because such parallel resonance of typical SMD ceramic capacitors will only appear at several GHz.

Figure 2-1. Equivalent Circuit of a Capacitor

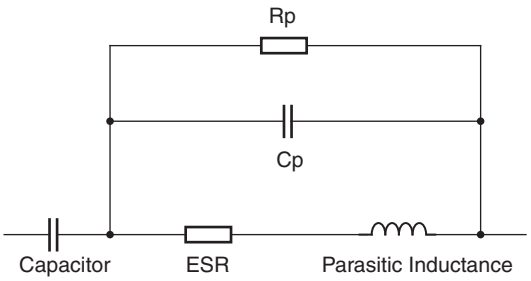
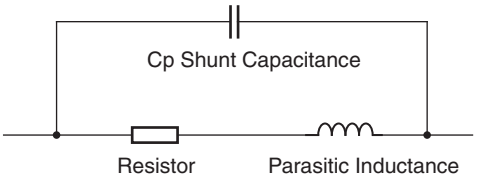
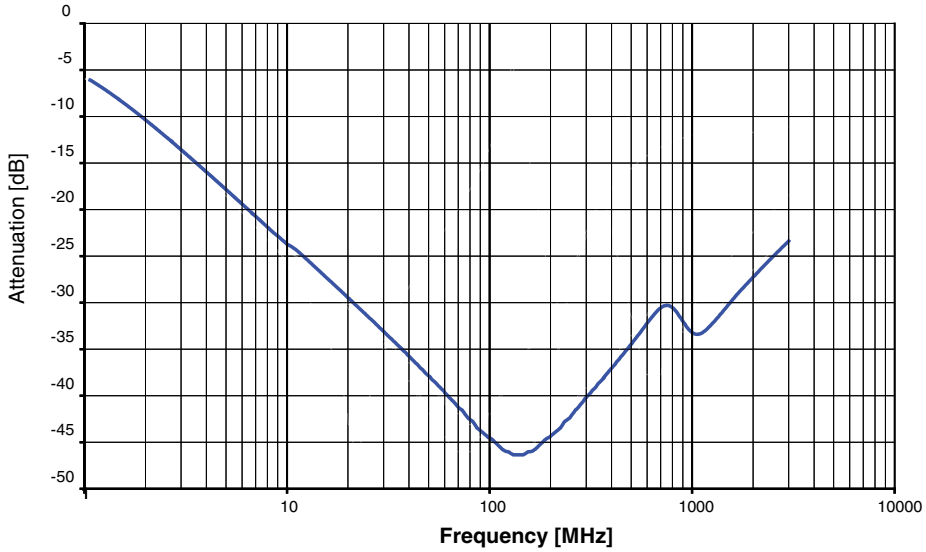


Figure 2-2. Equivalent Circuit of a Resistor



The series resonance of the capacitor is determined by its type (electrolytic, foil, ceramic), mechanical dimensions (axial, radial, SMD, size), and of course its value. The higher the capacitance of a given capacitor type, the lower its series resonance frequency. Therefore it is advisable not just to place a single capacitor for decoupling purpose, but combine two or several caps to achieve broadband decoupling. For example, pairing a 10nF capacitor for lower frequencies with a 100pF cap for higher frequencies is often recommended. The following will explore whether this is advisable. A very basic linear RF simulation tool is sufficient for demonstrating this; there are even freeware tools available for this purpose. Many manufacturers of ceramic capacitors supply S-Parameter files for their products and it is advisable to use them. Figure 2-3 on page 9 shows the attenuation of the above two capacitors when placed in parallel from a 50Ω track to GND.

Figure 2-3. Attenuation of 2 Ceramic Capacitors of 10nF and 100pF in Parallel in a 50Ω System

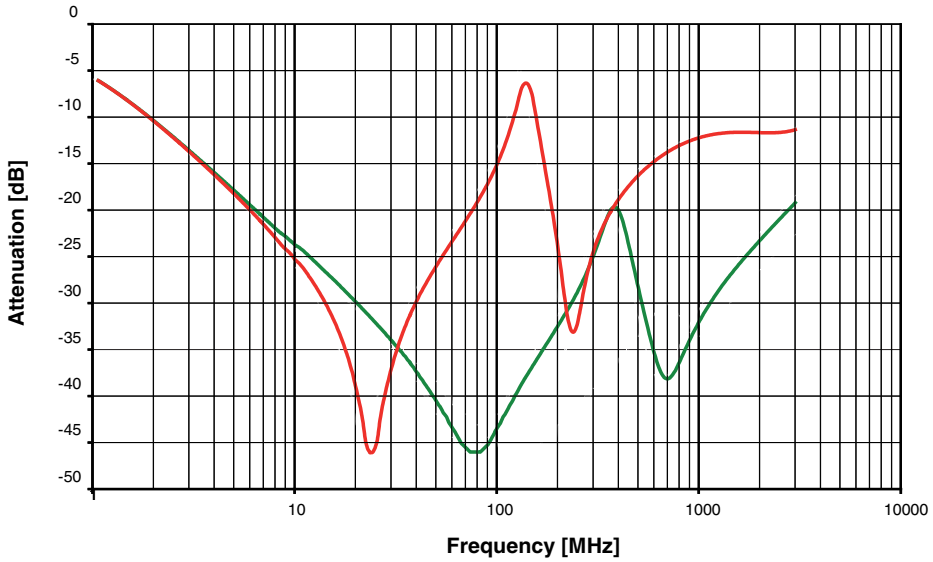


This looks quite acceptable. Attenuation of at least 30dB was achieved for frequencies between 20MHz and well above 1GHz. If a higher reference impedance than 50Ω had been used, it would look even better. In an ideal world, it would be possible to stop here. But has something been overlooked? In reality, it is not possible to connect the capacitors perfectly to GND or to the track or pad which needs to be decoupled. Every track on the PCB above behaves like a transmission line and its impedance is determined primarily by track width, the thickness of the PCB or, where a multilayer PCB is used, the distance between signal and GND layer, the distance to adjacent GND areas and the dielectric constant ε_r of the PCB material. Again, there are specialized books and free calculation tools available for guidance on this issue. With track widths of 0.2mm, GND area >0.5mm away from the track and $\varepsilon_r = 4.7$, impedance of well above 100Ω for 2-layer boards (1.6mm standard thickness) will result, and close to 50Ω will result for a multilayer board with 150µm distance between the signal layer and GND plane.

Figure 2-4 on page 10 shows how decoupling performance changes if the board layout is not done with care. When considering the red curve in Figure 2-4 on page 10 standard 2-layer PCB, distance between caps and to their GND vias: 10mm with just one GND via per cap. Now, quite unexpectedly, there is a highly undesirable resonance around 130MHz, with attenuation of only 6dB. The green graph in Figure 2-4 on page 10 shows the performance for an improved board layout: Now a multilayer board is used, the two caps are closer to each other and each one has two GND vias only 1mm away from the respective cap. The resulting decoupling performance is significantly improved, but there still seems to be room for improvement.

The lesson learned from this example is, first, the decoupling caps need to be as close as possible to each other and to the component which needs to be decoupled. Secondly, using a multilayer PCB with a GND plane just below the signal layer is beneficial too. And, finally, it appears to be a good idea to do some simulation with “real” capacitors rather than just selecting them based on instinct. Innovative layout designs even place only a single centralized group of capacitors to decouple a larger area - but that is something which should not be attempted without careful simulation.

Figure 2-4. Attenuation of 2 Ceramic Capacitors of 10nF and 100pF in Parallel in a 50Ω System with Realistic Parasitic Components in Connecting Tracks



Red: distance between caps and to their GND vias: 10mm, one GND via per cap, track width: 0.2mm, board thickness top to GND: 1.6mm.

Green: optimized, distance between caps: 5mm, between caps and their GND vias: 1mm, two GND vias per cap, track width: 0.2mm, board thickness top to inner GND plane: 0.15mm.

As mentioned previously in this application note, car manufacturers are aware that EMC issues generally become more costly the later they are discovered. Engineers can benefit from this insight within their own development work. Giving some thought to EMC behavior already when designing a circuit definitely helps avoid unpleasant surprises during EMC approval testing. Having said that much - what needs to be done if a design fails EMC testing, despite the care exercised prior to testing? Or, just in case it was not possible to provide sufficient time, budget, or experience appropriate for EMC assessment in a project, what can be done to improve matters?

The truth is that no standard procedure exists. If emission is the problem, a probe across the circuit can be attempted with a field probe to detect any potential “hot spots”. Or, if fast enough, it is possible to re-perform the particular failed emission measurement while connecting a short isolated wire to some “suspicious” spots on the PCB. If a critical one shows up, the number of spurs will increase; this becomes immediately noticeable on the connected receiving instrument. If the design performs weakly in terms of susceptibility, consideration must be given to what parts of the circuit are affected (this can often be deduced from the malfunction occurring during the immunity measurement), and the coupling path must be located. Once the critical parts of the circuit have been pinpointed, the techniques described above can be used to improve EMC performance. A key consideration in this regard is that effective decoupling requires a solid GND area. Lacking this, it may be easier to redesign the board first; alternatively, copper foil could be added to facilitate further optimization measures in the lab.

Hopefully it has become apparent that there is nothing magical at all about EMC and that it is simply applied physics. Naturally, our knowledge about coupling mechanisms and particularly their parameters tends to be inaccurate and some-times incomplete, even if highly sophisticated electromagnetic simulation tools have been used and care has been taken during PCB development. Thus, the final assessment and optimization will always be performed on the hardware, and it is therefore highly advantageous to allow enough time when planning.

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