ACPL-M483/P483/W483

Inverted Logic High CMR Intelligent Power Module and Gate Drive Interface Optocoupler

Data Sheet

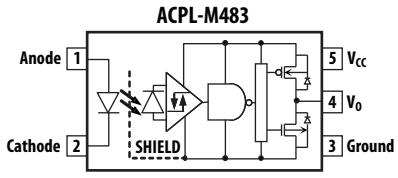
Description

The ACPL-M483/P483/W483 fast speed optocoupler contains a AlGaAs LED and photo detector with built-in Schmitt trigger to provide logic-compatible waveforms, eliminating the need for additional wave shaping. The totem pole output eliminates the need for a pull up resistor and allows for direct drive of Intelligent Power Module or as a gate driver. Minimized propagation delay difference between devices makes these optocouplers excellent solutions for improving inverter efficiency through reduced switching dead time.

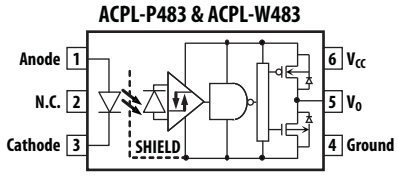
Applications

- IPM Interface Isolation
- Isolated IGBT/MOSFET Gate Drive
- AC and Brushless DC Motor Drives
- Industrial Inverters
- General Digital Isolation

Functional Diagram



Note: A 0.1 µF bypass capacitor must be connected between pins Vcc and Ground.



Truth Table (Negative Logic)

LED	V_O
ON	LOW
OFF	HIGH

Truth Table Guaranteed: Vcc from 4.5 V to 30 V

Features

- Inverted output type (totem pole output)
- Truth Table Guaranteed: Vcc from 4.5 V to 30 V
- Performance Specified for Common IPM Applications Over Industrial Temperature Range.
- Short Maximum Propagation Delays
- Minimized Pulse Width Distortion (PWD)
- Very High Common Mode Rejection (CMR)
- Hysteresis
- Available in SO-5 (ACPL-M483) and Stretched SO-6 package (ACPCL-P483/W483).
- Package Clearance/Creepage at 8 mm (ACPL-W483)
- Safety Approval: (pending)
  - UL Recognized with 5000 V_{rms} (ACPL-W483) for 1 minute per UL1577.
  - CSA Approved.
  - IEC/EN/DIN EN 60747-5-5 Approved with V_{IORM} = 567 V_{peak} for ACPL-M483 and V_{IORM} = 891 V_{peak} for ACPL-P483 and V_{IORM} = 1140 V_{peak} for ACPL-W483, under option 060.

Specifications

- Wide operating temperature range: -40° C to 105° C.
- Maximum propagation delay t_{PHL}/t_{PLH} = 120/120 ns
- Maximum Pulse Width Distortion (PWD) = 50 ns.
- Propagation Delay Difference Min/Max = -100/100 ns
- Wide Operating V_{CC} Range: 4.5 to 30 Volts
- 30 kV/µs minimum common mode rejection (CMR) at V_{CM} = 1000 V.

CAUTION: *It is advised that normal static precautions be taken in handling and assembly of this component to prevent damage and/or degradation which may be induced by ESD.*

Ordering Information

ACPL-M483/P483/W483 is UL recognized with 3750/3750/5000 V_{rms}/1 minute rating per UL 1577 respectively.

Part number	Option RoHS Compliant	Package	Surface Mount	Tape & Reel	IEC/EN/DIN EN 60747-5-5	Quantity
ACPL-M483	-000E	SO-5	X			100 per tube
	-500E		X	X		1500 per reel
	-060E		X		X	100 per tube
	-560E		X	X	X	1500 per reel
ACPL-P483 ACPL-W483	-000E	Stretched SO-6	X			100 per tube
	-500E		X	X		1000 per reel
	-060E		X		X	100 per tube
	-560E		X	X	X	1000 per reel

To order, choose a part number from the part number column and combine with the desired option from the option column to form an order entry.

Example 1:

ACPL-P483-560E to order product of Stretched SO-6 Surface Mount package in Tape and Reel packaging with IEC/EN/DIN EN 60747-5-5 Safety Approval in RoHS compliant.

Example 2:

ACPL-P483-000E to order product of Stretched SO-6 Surface Mount package in Tube packaging and RoHS compliant.

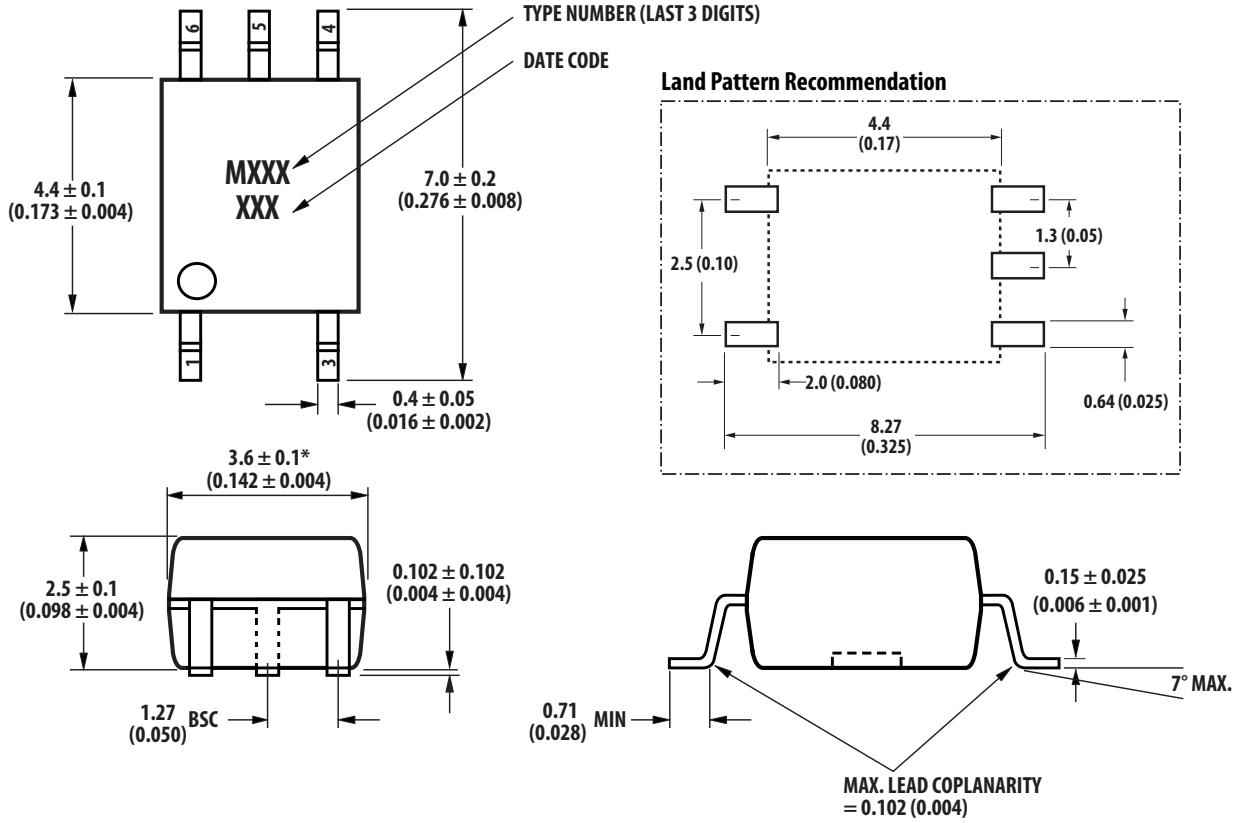
Example 3:

ACPL-M483-000E to order product of SO-5 Surface Mount package in Tube packaging and RoHS compliant.

Option datasheets are available. Contact your Avago sales representative or authorized distributor for information.

Package Outline Drawings

ACPL-M483 SO-5 Package, 5 mm Creepage & Clearance

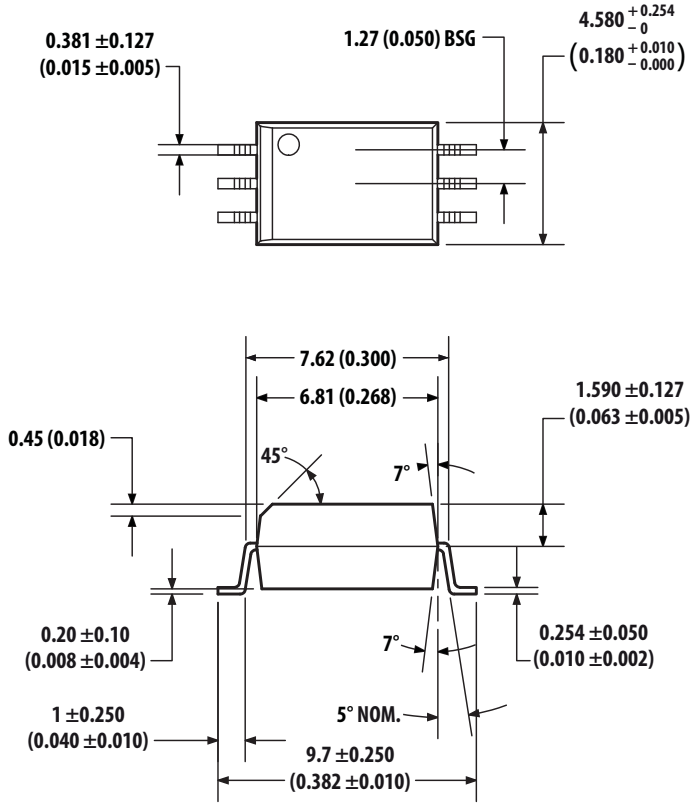


Dimensions in millimeters (inches).

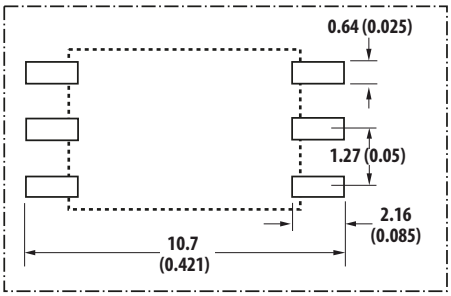
* Maximum Mold flash on each side is 0.15 mm (0.006).

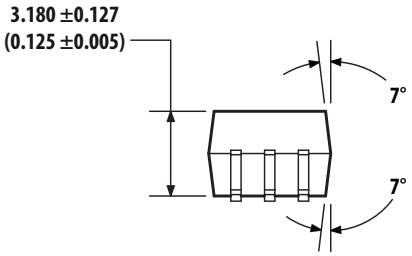
Note: Foating Lead Protrusion is 0.15 mm (6 mils) max.

ACPL-P483 Stretched SO-6 Package, 7 mm clearance



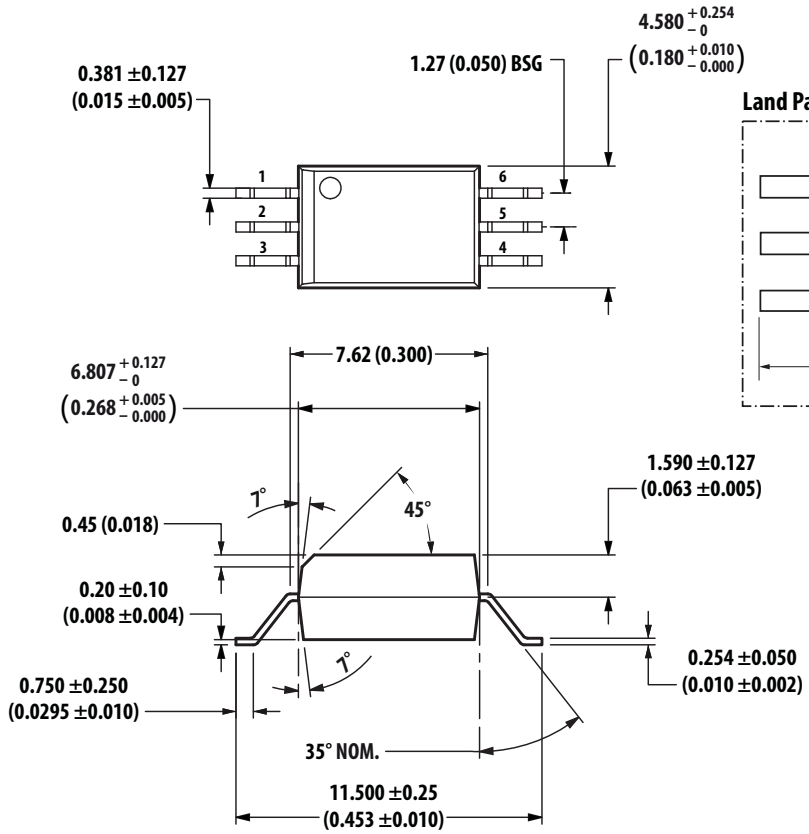
Land Pattern Recommendation



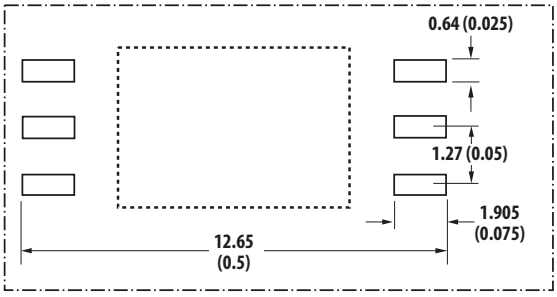


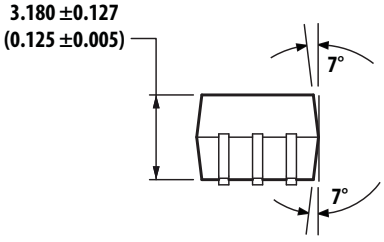
Floating Lead Protusions max. 0.25 (0.01)
Dimensions in Millimeters (Inches)
Lead Coplanarity = 0.1 mm (0.004 Inches)

ACPL-W483 Stretched SO-6 Package, 8 mm clearance



Land Pattern Recommendation





Floating Lead Protusions max. 0.25 (0.01)
Dimensions in Millimeters (Inches)
Lead Coplanarity = 0.1 mm (0.004 Inches)

Recommended Pb-Free IR Profile

Recommended reflow condition as per JEDEC Standard, J-STD-020 (latest revision). Non-Halide Flux should be used.

Regulatory Information

The ACPL-M483/P483/W483 is pending approval by the following organizations:

IEC/EN/DIN EN 60747-5-5 (Option 060 only)

Approved with Maximum Working Insulation Voltage V_{IORM} = 567 V_{peak} for ACPL-M483, V_{IORM} = 891 V_{peak} for ACPL-P483 and V_{IORM} = 1140 V_{peak} for ACPL-W483

UL

Approval under UL 1577, component recognition program up to V_{ISO} = 3750 V_{RMS} File E55361 for ACPL-M483 & ACPL-P483;

Approval under UL 1577, component recognition program up to V_{ISO} = 5000 V_{RMS} File E55361 for ACPL-W483;

CSA

Approval under CSA Component Acceptance Notice #5, File CA 88324.

Table 1. IEC/EN/DIN EN 60747-5-5 Insulation Characteristics* (ACPL-M483/P483/W483 Option 060)

Description	Symbol	ACPL-M483	ACPL-P483	ACPL-W483	Unit
Installation classification per DIN VDE 0110/1.89, Table 1					
for rated mains voltage ≤ 150 V_{rms}		I – IV	I – IV	I – IV	
for rated mains voltage ≤ 300 V_{rms}		I – III	I – III	I – III	
for rated mains voltage ≤ 600 V_{rms}		I – II	I – II	I – II	
Climatic Classification		55/105/21	55/105/21	55/105/21	
Pollution Degree (DIN VDE 0110/1.89)		2	2	2	
Maximum Working Insulation Voltage	V_{IORM}	567	891	1140	V_{peak}
Input to Output Test Voltage, Method b* V_{IORM} x 1.875 = V_{PR}, 100% Production Test with t_m = 1 sec, Partial discharge < 5 pC	V_{PR}	1063	1670	2137	V_{peak}
Input to Output Test Voltage, Method a* V_{IORM} x 1.6 = V_{PR}, Type and Sample Test, t_m = 10 sec, Partial discharge < 5 pC	V_{PR}	907	1426	1824	V_{peak}
Highest Allowable Overvoltage (Transient Overvoltage t_{ini} = 60 sec)	V_{IOTM}	6000	6000	8000	V_{peak}
Safety-limiting values – maximum values allowed in the event of a failure.	T_S	175	175	175	°C
Case Temperature	$I_{S, INPUT}$	230	230	230	mA
Input Current	$P_{S, OUTPUT}$	600	600	600	mW
Output Power					
Insulation Resistance at T_S, V_{IO} = 500 V	R_S	$>10^9$	$>10^9$	$>10^9$	Ω

* Refer to the optocoupler section of the Isolation and Control Components Designer's Catalog, under Product Safety Regulations section, (IEC/EN/DIN EN 60747-5-2) for a detailed description of Method a and Method b partial discharge test profiles.

Table 2. Insulation and Safety Related Specifications

Parameter	Symbol	ACPL-M483	ACPL-P483	ACPL-W483	Units	Conditions
Minimum External Air Gap (External Clearance)	L(101)	5.0	7.0	8.0	mm	Measured from input terminals to output terminals, shortest distance through air.
Minimum External Tracking (External Creepage)	L(102)	5.0	8.0	8.0	mm	Measured from input terminals to output terminals, shortest distance path along body.
Minimum Internal Plastic Gap (Internal Clearance)		0.08	0.08	0.08	mm	Through insulation distance conductor to conductor, usually the straight line distance thickness between the emitter and detector.
Tracking Resistance (Comparative Tracking Index)	CTI	>175	>175	>175	V	DIN IEC 112/VDE 0303 Part 1
Isolation Group		IIIa	IIIa	IIIa		Material Group (DIN VDE 0110, 1/89, Table 1)

Table 3. Absolute Maximum Ratings

Parameter	Symbol	Min.	Max.	Units	Note
Storage Temperature	T_S	-55	125	°C	
Operating Temperature	T_A	-40	105	°C	
Average Input Current	$I_{F(avg)}$		10	mA	
Peak Transient Input Current	$I_{F(tran)}$				
(<1 μs pulse width, 300 pps)			1.0	A	
(<200 μs pulse width, < 1% duty cycle)			40	mA	
Reverse Input Voltage	V_R		5	V	
Average Output Current	I_O		50	mA	
Supply Voltage	V_{CC}	0	35		
Output Voltage	V_O	-0.5	35		
Total Package Power Dissipation (ACPL-M483)	P_T		145	mW	1
Total Package Power Dissipation (Others)	P_T		210	mW	1
Solder Reflow Temperature Profile		See Reflow Thermal Profile.			

Table 4. Recommended Operating Conditions

Parameter	Symbol	Min.	Max.	Units	Note
Power Supply Voltage [1]	V_{CC}	4.5	30	V	2
Forward Input Current (ON)	$I_{F(ON)}$	4	7	mA	
Forward Input Voltage (OFF)	$V_{F(OFF)}$	–	0.8	V	
Operating Temperature	T_A	-40	105	°C	

Note:
1. Truth Table guaranteed: 4.5 V to 30 V

Table 5. Electrical Specifications

Over recommended operating conditions T_A = -40° C to 105° C, V_{CC} = +4.5 V to 30 V, $I_{F(ON)}$ = 4 mA to 7 mA, $V_{F(OFF)}$ = 0 V to 0.8 V, unless otherwise specified. All typical values at T_A = 25° C.

Parameter	Symbol	Min.	Typ.	Max.	Units	Test Conditions	Fig.	Note
Logic Low Output Voltage	V_{OL}			0.3	V	I_{OL} = 3.5 mA	1, 3	
				0.5		I_{OL} = 6.5 mA		
Logic High Output Voltage	V_{OH}	V_{CC} -0.3	V_{CC} -0.04		V	I_{OH} = -3.5 mA	2, 3, 7	
		V_{CC} -0.5	V_{CC} -0.07			I_{OH} = -6.5 mA		
Logic Low Supply Current	I_{CCL}		1.5	3.0	mA	V_{CC} = 5.5 V, I_F = 7 mA, I_o = 0 mA		
			1.7	3.0	mA	V_{CC} = 20 V, I_F = 7 mA, I_o = 0 mA		
Logic High Supply Current	I_{CCH}		1.5	3.0	mA	V_{CC} = 5.5 V, V_F = 0 V, I_o = 0 mA		
			1.7	3.0	mA	V_{CC} = 30 V, V_F = 0 V, I_o = 0 mA		
Threshold Input Current, Output High to Low	I_{FHL}		0.8	2.2	mA			
Threshold Input Voltage Output Low to High	V_{FLH}	0.8			V			
Logic Low Short Circuit Output Current	I_{OSL}	125	200		mA	V_O = V_{CC} = 5.5 V, I_F = 7 mA, V_O = GND		3
		125	200		mA	V_O = V_{CC} = 20 V, I_F = 7 mA, V_O = GND		
Logic High Short Circuit Output Current	I_{OSH}		-200	-125	mA	V_{CC} = 5.5 V, V_F = 0 V		3
			-200	-125	mA	V_{CC} = 20 V, V_F = 0 V		
Input Forward Voltage	V_F	1.3	1.5	1.7	V	T_A = 25° C, I_F = 4 mA	4	
				1.85	V	I_F = 4 mA		
Input Reverse Breakdown Voltage	BV_R	5			V	I_R = 10 µA		
Input Diode Temperature Coefficient	$\Delta V_F/\Delta T_A$		1.7		mV/°C	I_F = 4 mA		
Input Capacitance	C_{IN}		60		pF	f = 1 MHz, V_F = 0 V		4

Table 6. Switching Specifications

Over recommended operating conditions T_A = -40° C to 105° C, V_{CC} = +4.5 V to 30 V, $I_{F(ON)}$ = 4 mA to 7 mA, $V_{F(OFF)}$ = 0 V to 0.8 V, unless otherwise specified. All typicals at T_A = 25° C.

Parameter	Symbol	Min.	Typ.	Max.	Units	Test Conditions	Fig.	Note
Propagation Delay Time to Logic Low Output Level	t_{PHL}		75	120	ns	C_L = 100pF, V_F = 0 V → $I_{F(OFF)}$ = 4 mA	5, 6, 8	6
				120		Loaded as per Fig. 5		
Propagation Delay Time to Logic High Output Level	t_{PLH}		75	120	ns	C_L = 100 pF, $I_{F(OFF)}$ = 4 mA → V_F = 0 V	5, 6, 8	6
				120		Loaded as per Fig. 5		
Pulse Width Distortion	$\|t_{PHL} - t_{PLH}\|$ = PWD			50	ns	C_L = 100 pF	5, 6, 8	9
				50		Loaded as per Fig. 5		
Propagation Delay Difference Between Any 2 Parts	PDD	-100		100	ns	C_L = 100 pF	5, 6, 8	10
		-100		100		Loaded as per Fig. 5		
Output Rise Time (10-90%)	t_r		6		ns		5	
Output Fall Time (90-10%)	t_f		6		ns		5	
Logic High Common Mode Transient Immunity	$\|CM_H\|$	30			kV/µs	$\|V_{CM}\|$ = 1000 V, V_F = 0 V, V_{CC} = 5 V, T_A = 25° C	9	7
Logic Low Common Mode Transient Immunity	$\|CM_L\|$	30			kV/µs	$\|V_{CM}\|$ = 1000 V, I_F = 4.0 mA, V_{CC} = 5 V, T_A = 25° C	9	7

Table 7. Package Characteristics

Parameter	Symbol	Min.	Typ.	Max.	Units	Test Conditions	Fig.	Note
Input-Output Momentary Withstand Voltage*	V_{ISO}	3750 (ACPL-M483 & P483) 5000 (ACPL-W483)			V_{rms}	RH < 50%, t = 1 min. T_A = 25° C		5, 8
Input-Output Resistance	R_{I-O}		10^{12}		Ohm	V_{I-O} = 500 V_{dc}		5
Input-Output Capacitance	C_{I-O}		0.6		pF	f = 1 MHz, V_{I-O} = 0 V_{dc}		5

* The Input-Output Momentary Withstand Voltage is a dielectric voltage rating that should not be interpreted as an input-output continuous voltage rating. For the continuous voltage rating, refer to the IEC/EN/DIN EN 60747-5-5 Insulation Characteristics Table (if applicable).

Inverted UVLO

Figure 10a & b show typical output waveforms during Power-up and Power-down processes.

Notes:

1. Derate total package power dissipation, PT, linearly above 70° C free-air temperature at a rate of 4.5mW/°C (ACPL-P483/W483) and linearly above 85° C free-air temperature at a rate of 0.75 mW/°C (ACPL-M483).
2. Detector requires a Vcc of 4.5 V or higher for stable operation as output might be unstable if Vcc is lower than 4.5 V. Be sure to check the power ON/OFF operation other than the supply current.
3. Duration of output short circuit time should not exceed 500 µs.
4. Input capacitance is measured between pin 1 and pin 3.
5. Device considered a two-terminal device: pins 1, 2 and 3 shorted together and pins 4, 5 and 6 shorted together.
6. The t_{PLH} propagation delay is measured from the 50% point on the trailing edge of the input pulse to the 1.3 V point on the leading edge of the output pulse. The t_{PHL} propagation delay is measured from the 50% point on the leading edge of the input pulse to the 1.3 V point on the trailing edge of the output pulse. Peaking capacitor, C1 = 120 pF must be connected as shown in Figure 5.
7. CM_H is the maximum slew rate of the common mode voltage that can be sustained with the output voltage in the logic high state, V_O > 2.0 V. CM_L is the maximum slew rate of the common mode voltage that can be sustained with the output voltage in the logic low state, V_O < 0.8 V. Note: Equal value split resistors (Rin/2) must be used at both ends of the LED.
8. In accordance with UL 1577, each optocoupler is proof tested by applying an insulation test voltage ≥ 4500 V_{RMS} for one second (leakage detection current limit, I_{I-O} < = 5 µA). This test is performed before the 100% production test for partial discharge (Method b) shown in the IEC/EN/DIN EN 60747-5-5 Insulation Characteristics Table, if applicable.
9. Pulse Width Distortion (PWD) is defined as $|t_{PHL} - t_{PLH}|$ for any given device.
10. The difference of tPLH and tPHL between any two devices under the same test condition.
11. Use of a 0.1 µF bypass capacitor connected between pins Vcc and Ground is recommended.

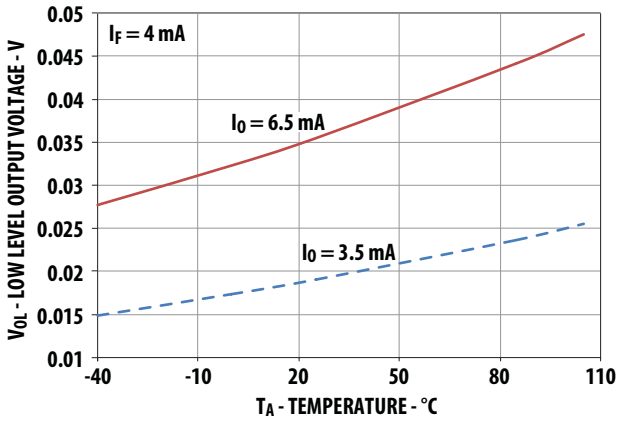


Figure 1. Typical Logic Low Output Voltage vs. Temperature

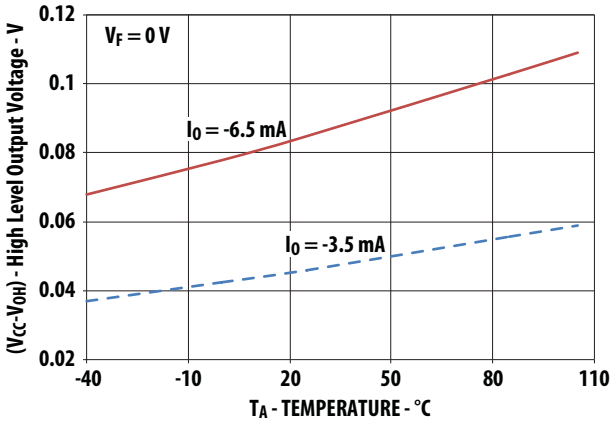


Figure 2. Typical Logic High Output Voltage vs. Temperature

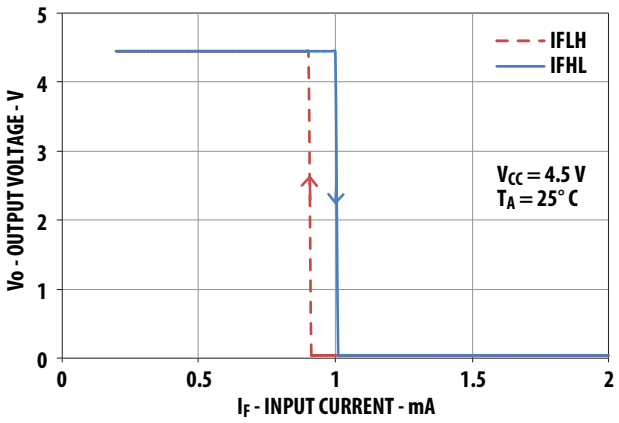


Figure 3. Typical Output Voltage vs. Forward Input Current

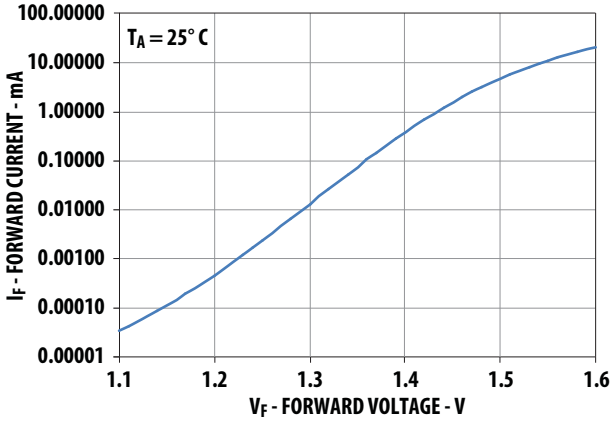
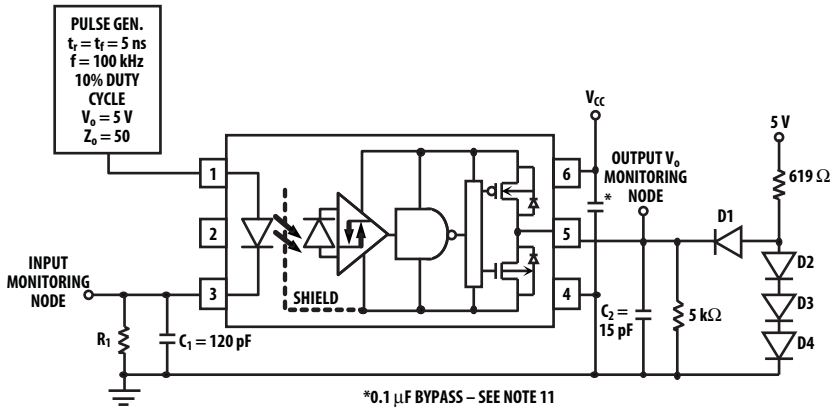


Figure 4. Typical Input Diode Forward Characteristic



THE PROBE AND JIG CAPACITANCES ARE INCLUDED IN C1 AND C2.

R_1	820 Ω	560 Ω
$I_{F(ON)}$	4 mA	7 mA

ALL DIODES ARE EITHER 1N916 OR 1N3064

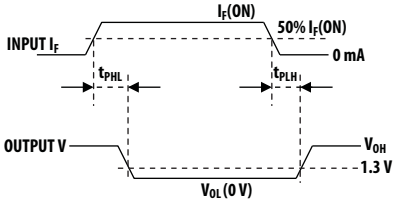


Figure 5. Circuit for t_{PLH}, t_{PHL}, t_r, t_f

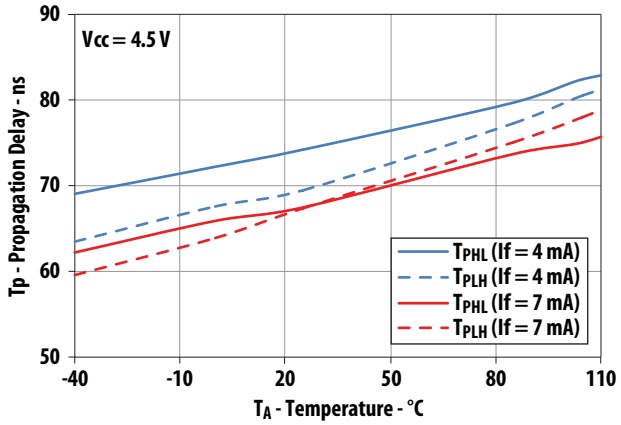


Figure 6. Typical Propagation Delays vs. Temperature.

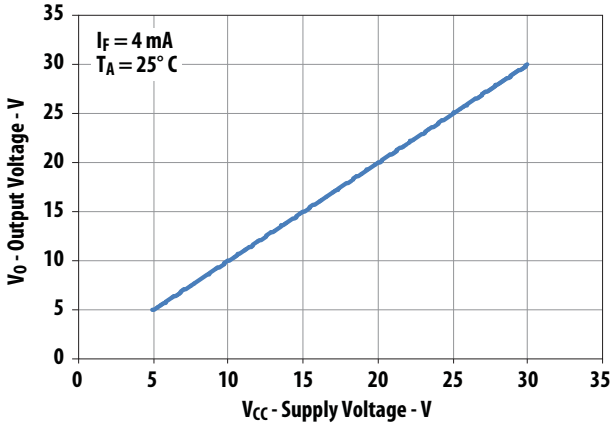


Figure 7. Typical Logic High Output Voltage vs. Supply Voltage

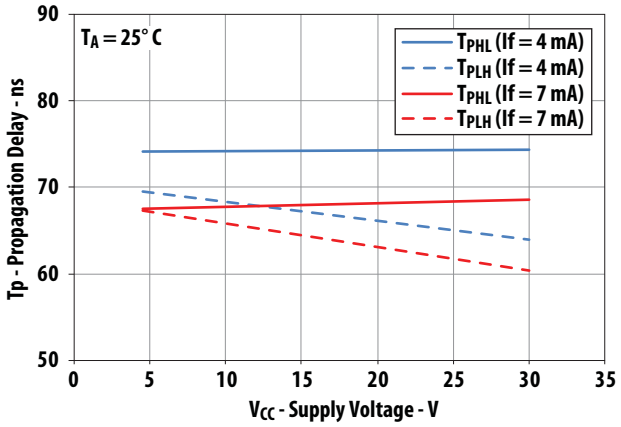
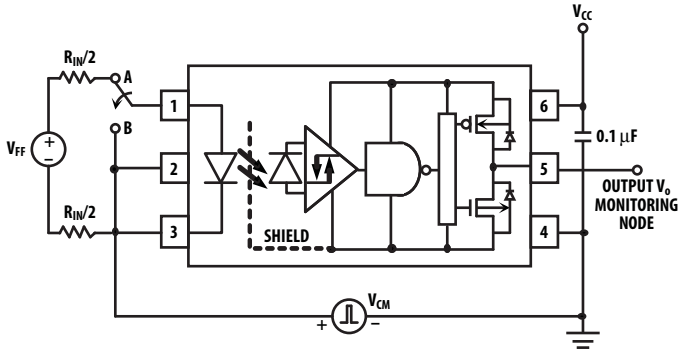


Figure 8. Typical Propagation Delay vs. Supply Voltage



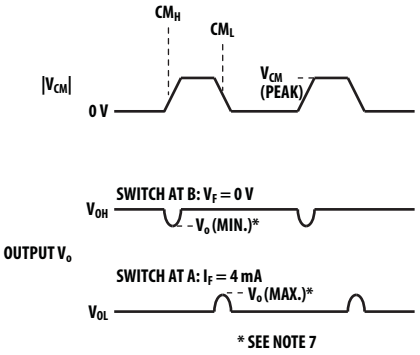


Figure 9. Test Circuit for Common Mode Transient Immunity and Typical Waveforms

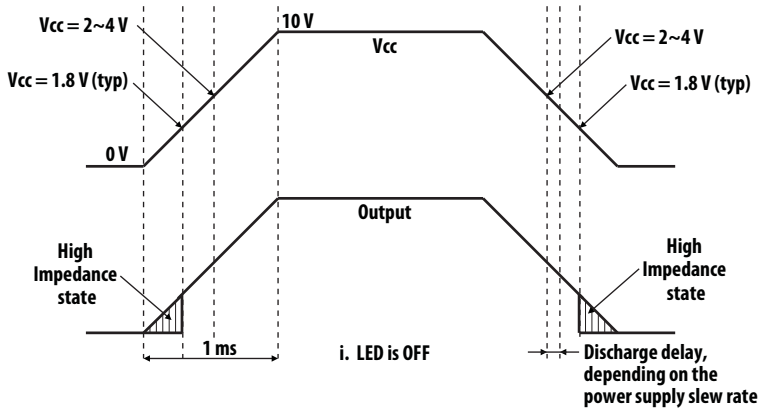


Figure 10a. Vcc Ramp when LED is OFF.

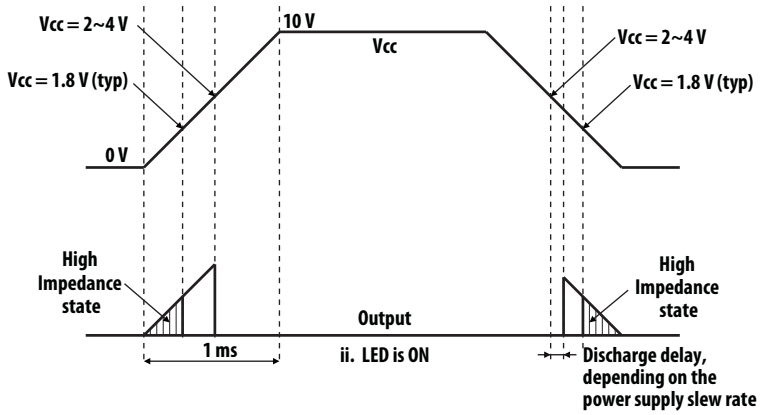


Figure 10b. Vcc Ramp when LED is ON.

Thermal Model for ACPL-M483 SO5 Package Optocoupler

Definitions

R_{11}: Junction to Ambient Thermal Resistance of LED due to heating of LED

R_{12}: Junction to Ambient Thermal Resistance of LED due to heating of Detector (Output IC)

R_{21}: Junction to Ambient Thermal Resistance of Detector (Output IC) due to heating of LED.

R_{22}: Junction to Ambient Thermal Resistance of Detector (Output IC) due to heating of Detector (Output IC).

P_1: Power dissipation of LED (W).

P_2: Power dissipation of Detector / Output IC (W).

T_1: Junction temperature of LED (˚C).

T_2: Junction temperature of Detector (˚C).

T_a: Ambient temperature.

ΔT_1: Temperature difference between LED junction and ambient (˚C).

ΔT_2: Temperature deference between Detector junction and ambient.

Ambient Temperature: Junction to Ambient Thermal Resistances were measured approximately 1.25cm above optocoupler at ~23˚C in still air

Description

This thermal model assumes that an 5-pin single-channel plastic package optocoupler is soldered into a 7.62 cm x 7.62 cm printed circuit board (PCB). The temperature at the LED and Detector junctions of the optocoupler can be calculated using the equations below.

$T_1 = (R_{11} * P_1 + R_{12} * P_2) + T_a$ -- (1)

$T_2 = (R_{21} * P_1 + R_{22} * P_2) + T_a$ -- (2)

Jedec Specifications	R_{11}	R_{12}, R_{21}	R_{22}
low K board	191	77, 91	99
high K board	126	26, 35	51

Notes:
1. Maximum junction temperature for above parts: 125 °C.

Thermal Model for ACPL-P483/W483 SO6 Package Optocoupler

Definitions

R_{11}: Junction to Ambient Thermal Resistance of LED due to heating of LED

R_{12}: Junction to Ambient Thermal Resistance of LED due to heating of Detector (Output IC)

R_{21}: Junction to Ambient Thermal Resistance of Detector (Output IC) due to heating of LED.

R_{22}: Junction to Ambient Thermal Resistance of Detector (Output IC) due to heating of Detector (Output IC).

P_1: Power dissipation of LED (W).

P_2: Power dissipation of Detector / Output IC (W).

T_1: Junction temperature of LED (˚C).

T_2: Junction temperature of Detector (˚C).

T_a: Ambient temperature.

ΔT_1: Temperature difference between LED junction and ambient (˚C).

ΔT_2: Temperature deference between Detector junction and ambient.

Ambient Temperature: Junction to Ambient Thermal Resistances were measured approximately 1.25cm above optocoupler at ~23˚C in still air

Description

This thermal model assumes that an 6-pin single-channel plastic package optocoupler is soldered into a 7.62 cm x 7.62 cm printed circuit board (PCB). The temperature at the LED and Detector junctions of the optocoupler can be calculated using the equations below.

$T_1 = (R_{11} * P_1 + R_{12} * P_2) + T_a$ -- (1)

$T_2 = (R_{21} * P_1 + R_{22} * P_2) + T_a$ -- (2)

Jedec Specifications	R_{11}	R_{12}, R_{21}	R_{22}
low K board	167	64, 81	89
high K board	117	31, 39	54

Notes:
1. Maximum junction temperature for above parts: 125 °C.

For product information and a complete list of distributors, please go to our web site: **www.avagotech.com**

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