



PRODUCT BULLETIN

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ISSUE DATE: 08-Mar-2013
NOTIFICATION: 15557
TITLE: ERRATUM: SIMULTANEOUS INSTRUCTION L1 MMU MISS (DUE TO EVICTION) AND INTERRUPT SERVICING CAN CAUSE AN E500 CORE HANG
EFFECTIVE DATE: 09-Mar-2013

DEVICE(S)

MPN
DS783PBGAPQ38PXD
DS783PBGAPQ38VTD
MPC8533EVTALF
MPC8533EVTALFA
MPC8533EVTANG
MPC8533EVTANGA
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MPC8533EVTAQGA
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MPC8533EVTARJA
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MPC8536EAVTANGA
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SPC8548ECVTAUJB
SPC8548EPXAUJB
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SPC8548PXAUJB
SPC8548VTAUJB
TV2-BLOCK-28NM

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AFFECTED CHANGE CATEGORIES

- DEVICE SPECIFICATION / ERRATA

DESCRIPTION OF CHANGE

Alert customers of erratum A-006184 affecting the e500 core. A simultaneous instruction L1 MMU miss and

an exception servicing can cause an e500 core hang.

The erratum affects the following product families:

e500 version 1:

MPC8540, MPC8541, MPC8555, MPC8560

e500 version 2:

MPC8533, MPC8535, MPC8536, MPC8543, MPC8544, MPC8545, MPC8547, MPC8548, MPC8567, MPC8568, MPC8569, MPC8572, P1010, P1011, P1012, P1013, P1014, P1015, P1016, P1017, P1020, P1021, P1022, P1023, P1024, P1025, P2010, P2020, PSC9131.

e500 multicore (e500MC)

P2040, P2041, P3041, P4040, P4080

e5500 devices:

P5010, P5020.

There are two software-based workarounds for the erratum described in erratum A-006184 and a fix is planned for BSC9131 (revision 1.1).

This is a "for your information only" communication. No device sampling is needed as a result of this product communication.

REASON FOR CHANGE

A system hang is possible when an exception occurs at the same time as several other internal core conditions occur. For a hang to happen, the L2 Message Management Unit (MMU) Translation Lookaside Buffer 1 (TLB1) entry which maps the translation for the first instruction in the exception handler must not be in the I-L1VSP.

As a result of the core hang, no further progress will be made until a higher priority exception is received for which interrupts are enabled.

ANTICIPATED IMPACT OF PRODUCT CHANGE(FORM, FIT, FUNCTION, OR RELIABILITY)

There are two options for workarounds:

Option 1 (All of the following steps must be performed):

* All line items with an asterisk (*), are for devices with an e500mc or e5500 core.

a- Do not use more than 4 (8* for e500MC or e5500) TLB1 entries, and ensure all interrupt handlers are mapped to one of the 4 (8* for e500MC or e5500) TLB1 entries with TID=0 and IPROT=1.

b- Prevent explicit invalidation of the TLB1 entry that contains the interrupt handler page by not overwriting or invalidating it (never clear the valid bit).

c- Prevent non-explicit invalidations of the TLB1 entry that contains the interrupt handler page by never:

- Setting MMUCSR0[L2TLB_FI]

- Executing a tlbivax with RA[60:61] set to 0b11 (invalidate all). This should not be executed from any core in the integrated device as tlbivax is broadcast to all cores.

- *Executing tlbilx with T=0 or T=1 ; (only in e500MC or e5500)

- *Executing mtspr LPIDR ; (only in e500MC or e5500)

Software may do non-explicit invalidations if

1- the instructions for invalidation are mapped by the same TLB1 entry which maps the interrupt handlers. (This will normally be the case if the operating system maps all its static executable code with a single TLB1 entry); AND

2- all interrupts should be blocked while performing the actions) set MSR[EE], MSR[CE], MSR[ME] & MSR[DE] =0))

Option 2 (All the following steps must be performed):

a- In order to restart a core that has hung due to this erratum, set the watchdog timer to take an interrupt at some period greater than the decremter interrupt interval, but smaller than an unacceptable hang time.

b- Have software reset the watchdog timer trigger during the decremter interrupt, ensuring the core only takes the watchdog interrupt if it is hung.

Notes:

- This will still allow for hangs, but will put a limit on the degradation in performance.

- If the software already performs critical interrupts, the core may still hang. If the customer wants to set the "watchdog timer reset" field (TCR[WRC]), (actual value will be SOC dependent), then a core reboot will exit the hang condition.

NOTE:
THE CHANGE(S) SPECIFIED IN THIS NOTIFICATION WILL BE IMPLEMENTED ON THE EFFECTIVE DATE LISTED ABOVE. To request further data or inquire about the notification, please enter a [Service Request](#)

For sample inquiries - please go to www.freescale.com

QUAL DATA AVAILABILITY DATE: 13-Mar-2013

QUALIFICATION STATUS: N/A

QUALIFICATION PLAN:

N/A

RELIABILITY DATA SUMMARY:

N/A

ELECTRICAL CHARACTERISTIC SUMMARY:

N/A

CHANGED PART IDENTIFICATION:

N/A

SAMPLE AVAILABILITY DATE: 26-Feb-2013

ATTACHMENT(S):

External attachment(s) FOR this notification can be viewed AT:

[15557_A-006184_Presentation_for_Customer_r3_-_no_animation.pdf](https://www.freescale.com/files/shared/doc/pcn/PCN15557.htm)
