

BTA2008W-800D

3Q Hi-Com Triac
8 November 2012

Product data sheet

1. Product profile

1.1 General description

Planar passivated high commutation three quadrant triac in a SOT223 surface mountable plastic package. This "series D" triac balances the requirements of commutation performance and gate sensitivity and is intended for interfacing with low power drivers and logic ICs including microcontrollers.

1.2 Features and benefits

- 3Q technology for improved noise immunity
- Direct gate triggering from low power drivers and logic ICs
- High commutation capability with very sensitive gate
- High voltage capability
- Planar passivated for voltage ruggedness and reliability
- Surface mountable package
- Triggering in three quadrants only
- Very sensitive gate for easy logic level triggering

1.3 Applications

- Low power motor controls
- Small inductive loads e.g. solenoids, door locks, water valves
- Small loads in large white goods

1.4 Quick reference data

Table 1. Quick reference data

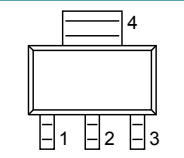
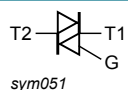
| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|-------------------------------|--------------------------------------|--|------|-----|-----|--------------------|
| V_{DRM} | repetitive peak off-state voltage | | - | - | 800 | V |
| I_{TSM} | non-repetitive peak on-state current | full sine wave; $T_{\text{j(Init)}} = 25\text{ }^{\circ}\text{C}$; $t_{\text{p}} = 20\text{ ms}$; Fig. 4 ; Fig. 5 | - | - | 9 | A |
| T_{j} | junction temperature | | - | - | 125 | $^{\circ}\text{C}$ |
| $I_{\text{T(RMS)}}$ | RMS on-state current | full sine wave; $T_{\text{sp}} \leq 111\text{ }^{\circ}\text{C}$; Fig. 1 ; Fig. 2 ; Fig. 3 | - | - | 0.8 | A |
| Static characteristics | | | | | | |
| I_{GT} | gate trigger current | $V_{\text{D}} = 12\text{ V}$; $I_{\text{T}} = 0.1\text{ A}$; T2+ G-; $T_{\text{j}} = 25\text{ }^{\circ}\text{C}$; Fig. 7 | 0.25 | - | 5 | mA |



| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|--------------------------------|---------------------------------------|--|------|-----|-----|------------------|
| | | $V_D = 12\text{ V}$; $I_T = 0.1\text{ A}$; T2+ G+; $T_j = 25\text{ }^\circ\text{C}$; Fig. 7 | 0.25 | - | 5 | mA |
| | | $V_D = 12\text{ V}$; $I_T = 0.1\text{ A}$; T2- G-; $T_j = 25\text{ }^\circ\text{C}$; Fig. 7 | 0.25 | - | 5 | mA |
| Dynamic characteristics | | | | | | |
| dV_D/dt | rate of rise of off-state voltage | $V_{DM} = 536\text{ V}$; $T_j = 125\text{ }^\circ\text{C}$; ($V_{DM} = 67\%$ of V_{DRM}); exponential waveform; gate open circuit | 200 | - | - | V/ μs |
| dI_{com}/dt | rate of change of commutating current | $V_D = 400\text{ V}$; $T_j = 125\text{ }^\circ\text{C}$; $I_{T(RMS)} = 0.8\text{ A}$; $dV_{com}/dt = 10\text{ V}/\mu\text{s}$; gate open circuit | 0.5 | - | - | A/ms |

2. Pinning information

Table 2. Pinning information

| Pin | Symbol | Description | Simplified outline | Graphic symbol |
|-----|--------|-----------------|---|---|
| 1 | T1 | main terminal 1 |  <p>SC-73 (SOT223)</p> |  <p>sym051</p> |
| 2 | T2 | main terminal 2 | | |
| 3 | G | gate | | |
| 4 | T2 | main terminal 2 | | |

3. Ordering information

Table 3. Ordering information

| Type number | Package | | |
|---------------|---------|--|---------|
| | Name | Description | Version |
| BTA2008W-800D | SC-73 | plastic surface-mounted package with increased heatsink; 4 leads | SOT223 |

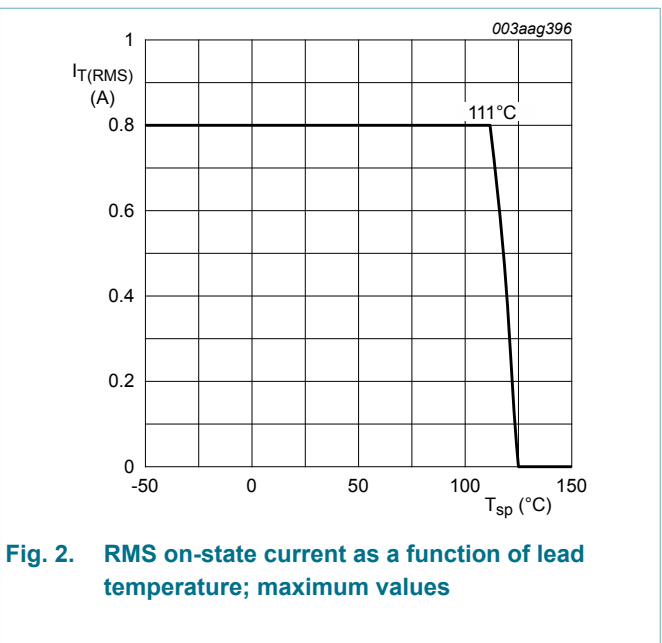
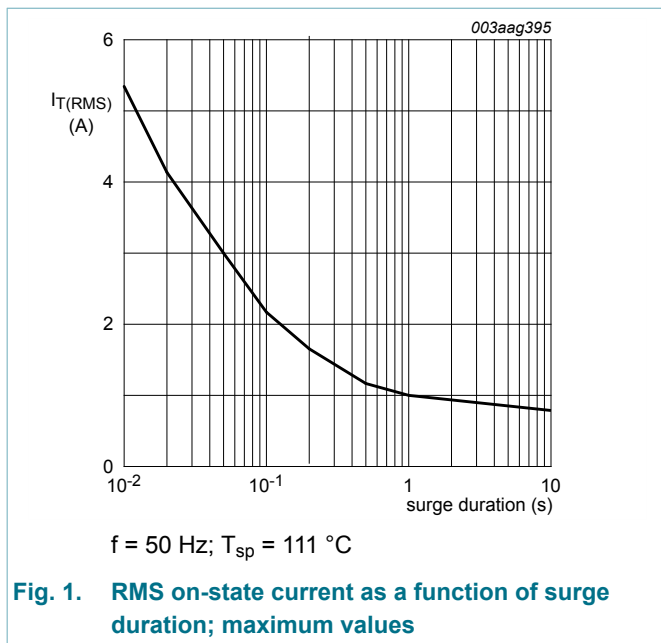
4. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

| Symbol | Parameter | Conditions | Min | Max | Unit |
|--------------|--------------------------------------|---|-----|-----|------|
| V_{DRM} | repetitive peak off-state voltage | | - | 800 | V |
| $I_{T(RMS)}$ | RMS on-state current | full sine wave; $T_{sp} \leq 111\text{ }^\circ\text{C}$; Fig. 1 ; Fig. 2 ; Fig. 3 | - | 0.8 | A |
| I_{TSM} | non-repetitive peak on-state current | full sine wave; $T_{j(\text{init})} = 25\text{ }^\circ\text{C}$; $t_p = 20\text{ ms}$; Fig. 4 ; Fig. 5 | - | 9 | A |

| Symbol | Parameter | Conditions | Min | Max | Unit |
|-------------|----------------------------------|--|-----|------|--------------------|
| | | full sine wave; $T_{j(\text{init})} = 25\text{ °C}$; $t_p = 16.7\text{ ms}$ | - | 9.9 | A |
| I^2t | I^2t for fusing | $t_p = 10\text{ ms}$; SIN | - | 0.41 | A^2s |
| dl_T/dt | rate of rise of on-state current | $I_T = 1.5\text{ A}$; $I_G = 20\text{ mA}$; $dl_G/dt = 0.2\text{ A}/\mu\text{s}$ | - | 100 | $A/\mu\text{s}$ |
| I_{GM} | peak gate current | | - | 2 | A |
| P_{GM} | peak gate power | | - | 5 | W |
| $P_{G(AV)}$ | average gate power | over any 20ms period | - | 0.1 | W |
| T_{stg} | storage temperature | | -40 | 150 | $^{\circ}\text{C}$ |
| T_j | junction temperature | | - | 125 | $^{\circ}\text{C}$ |



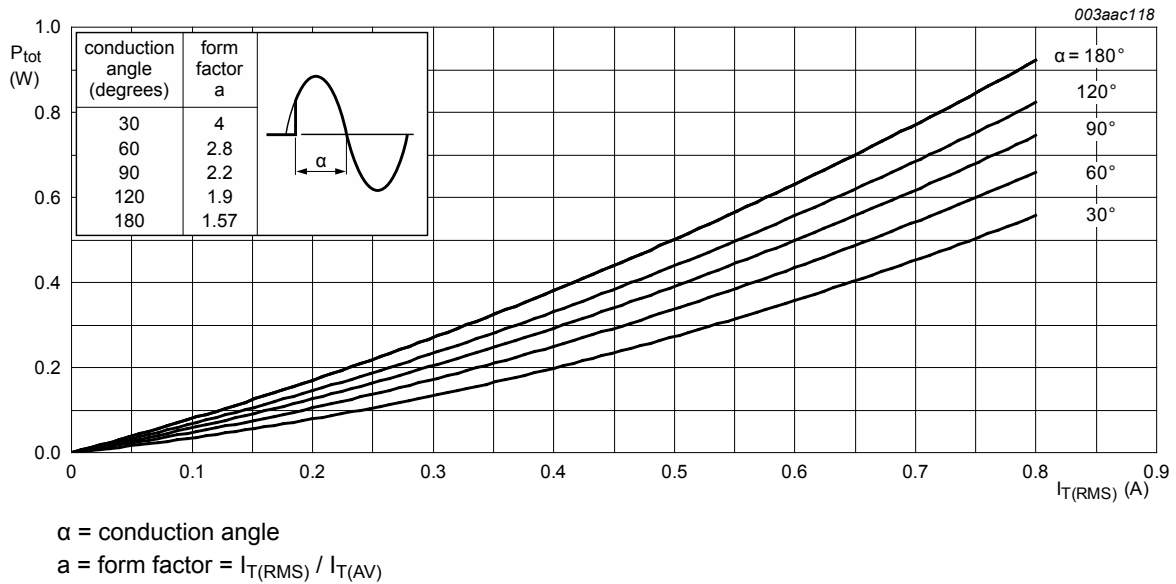


Fig. 3. Total power dissipation as a function of RMS on-state current; maximum values

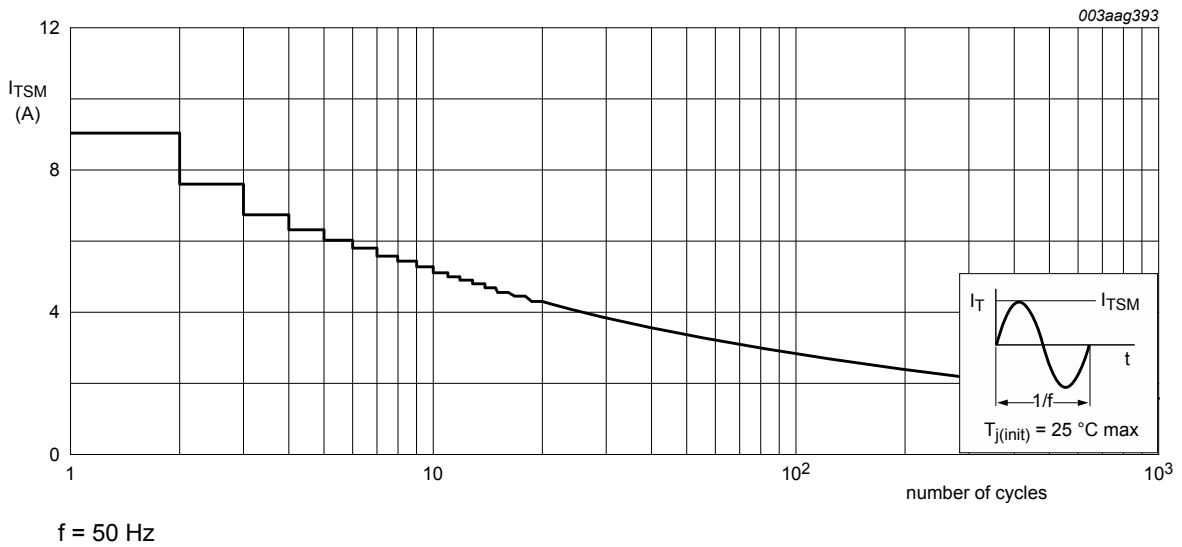
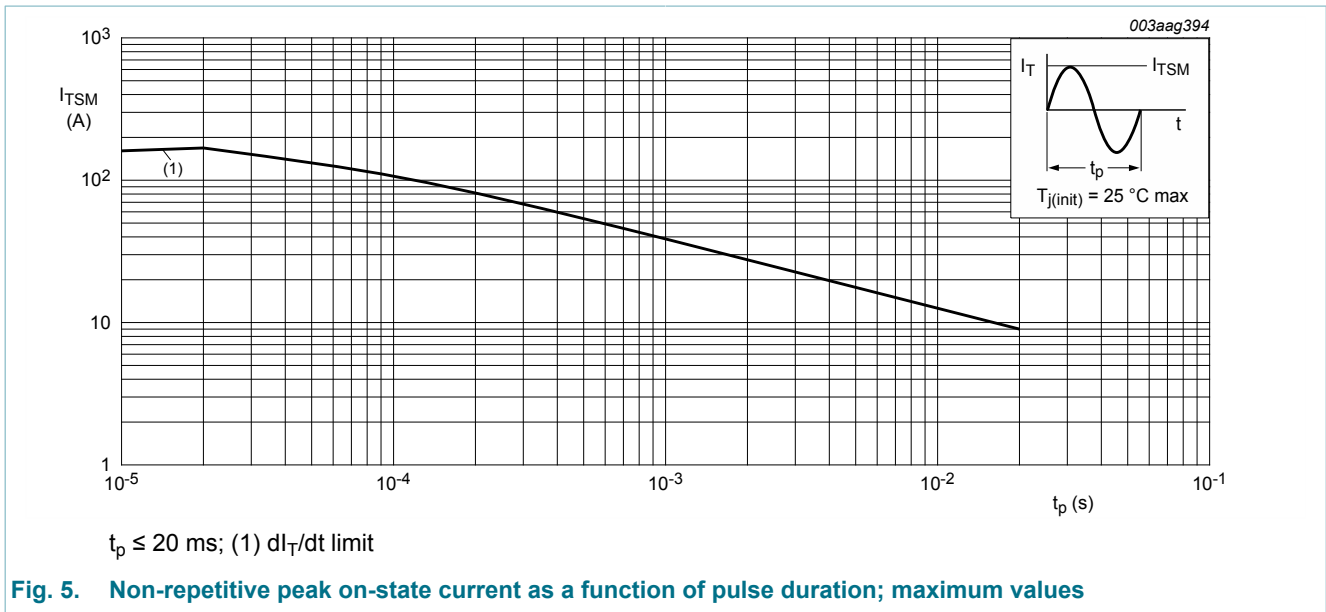


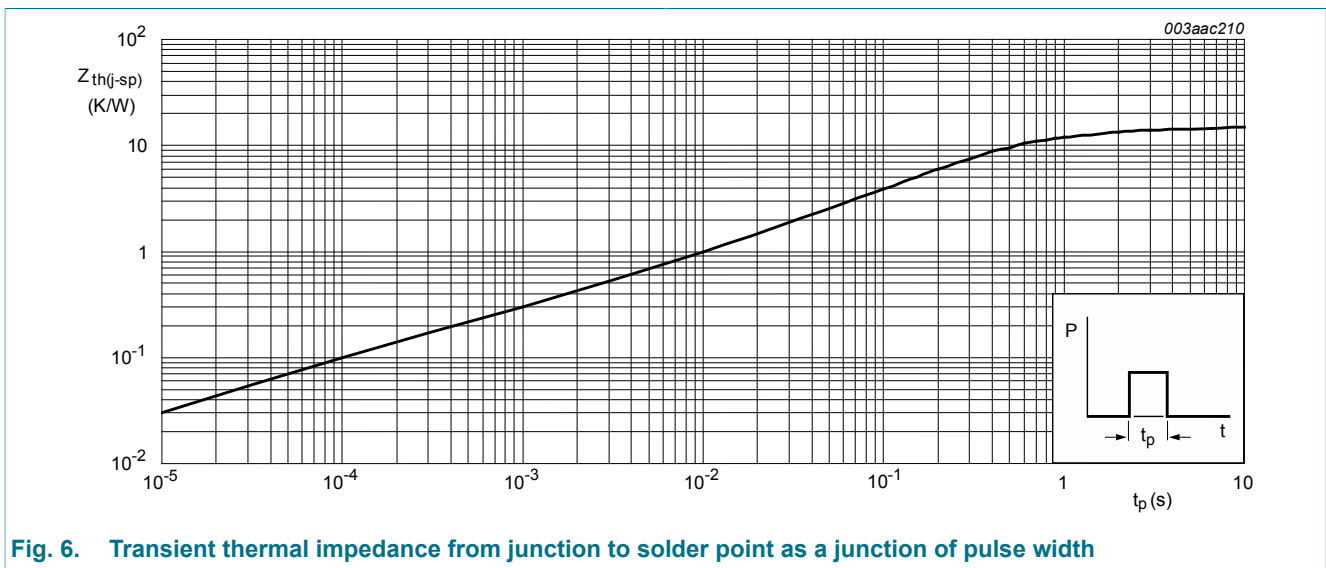
Fig. 4. Non-repetitive peak on-state current as a function of the number of sinusoidal current cycles; maximum values



5. Thermal characteristics

Table 5. Thermal characteristics

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|----------------|--|---|-----|-----|-----|------|
| $R_{th(j-sp)}$ | thermal resistance from junction to solder point | full cycle; Fig. 6 | - | - | 15 | K/W |
| $R_{th(j-a)}$ | thermal resistance from junction to ambient | in free air; printed-circuit board mounted: minimum footprint; full cycle | - | 156 | - | K/W |
| | | in free air; printed-circuit board mounted: pad area; full cycle | - | 70 | - | K/W |



6. Characteristics

Table 6. Characteristics

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|--------------------------------|---------------------------------------|--|------|------|-----|------------------|
| Static characteristics | | | | | | |
| I_{GT} | gate trigger current | $V_D = 12\text{ V}$; $I_T = 0.1\text{ A}$; T2+ G-; $T_j = 25\text{ }^\circ\text{C}$; Fig. 7 | 0.25 | - | 5 | mA |
| | | $V_D = 12\text{ V}$; $I_T = 0.1\text{ A}$; T2+ G+; $T_j = 25\text{ }^\circ\text{C}$; Fig. 7 | 0.25 | - | 5 | mA |
| | | $V_D = 12\text{ V}$; $I_T = 0.1\text{ A}$; T2- G-; $T_j = 25\text{ }^\circ\text{C}$; Fig. 7 | 0.25 | - | 5 | mA |
| I_L | latching current | $V_D = 12\text{ V}$; $I_G = 0.1\text{ A}$; T2+ G+; $T_j = 25\text{ }^\circ\text{C}$; Fig. 8 | - | - | 10 | mA |
| | | $V_D = 12\text{ V}$; $I_G = 0.1\text{ A}$; T2+ G-; $T_j = 25\text{ }^\circ\text{C}$; Fig. 8 | - | - | 20 | mA |
| | | $V_D = 12\text{ V}$; $I_G = 0.1\text{ A}$; T2- G-; $T_j = 25\text{ }^\circ\text{C}$; Fig. 8 | - | - | 10 | mA |
| I_H | holding current | $V_D = 12\text{ V}$; $T_j = 25\text{ }^\circ\text{C}$; Fig. 9 | - | - | 10 | mA |
| V_T | on-state voltage | $I_T = 0.85\text{ A}$; $T_j = 25\text{ }^\circ\text{C}$; Fig. 10 | - | 1.35 | 1.6 | V |
| V_{GT} | gate trigger voltage | $V_D = 12\text{ V}$; $I_T = 0.1\text{ A}$; $T_j = 25\text{ }^\circ\text{C}$; Fig. 11 | - | 0.9 | 2 | V |
| | | $V_D = 400\text{ V}$; $I_T = 0.1\text{ A}$; $T_j = 125\text{ }^\circ\text{C}$; Fig. 11 | 0.2 | 0.3 | - | V |
| I_D | off-state current | $V_D = 800\text{ V}$; $T_j = 125\text{ }^\circ\text{C}$ | - | 0.1 | 0.5 | mA |
| Dynamic characteristics | | | | | | |
| dV_D/dt | rate of rise of off-state voltage | $V_{DM} = 536\text{ V}$; $T_j = 125\text{ }^\circ\text{C}$; ($V_{DM} = 67\%$ of V_{DRM}); exponential waveform; gate open circuit | 200 | - | - | V/ μs |
| dI_{com}/dt | rate of change of commutating current | $V_D = 400\text{ V}$; $T_j = 125\text{ }^\circ\text{C}$; $I_{T(RMS)} = 0.8\text{ A}$; $dV_{com}/dt = 10\text{ V}/\mu\text{s}$; gate open circuit | 0.5 | - | - | A/ms |

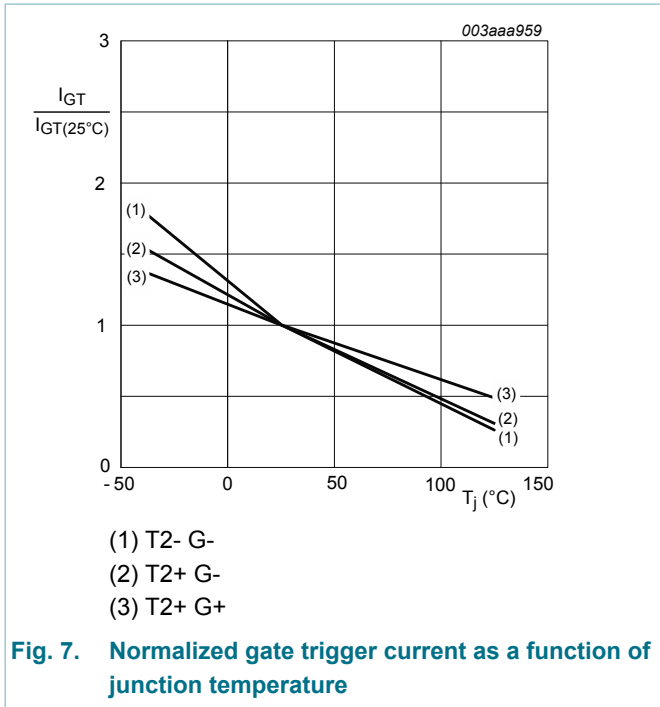


Fig. 7. Normalized gate trigger current as a function of junction temperature

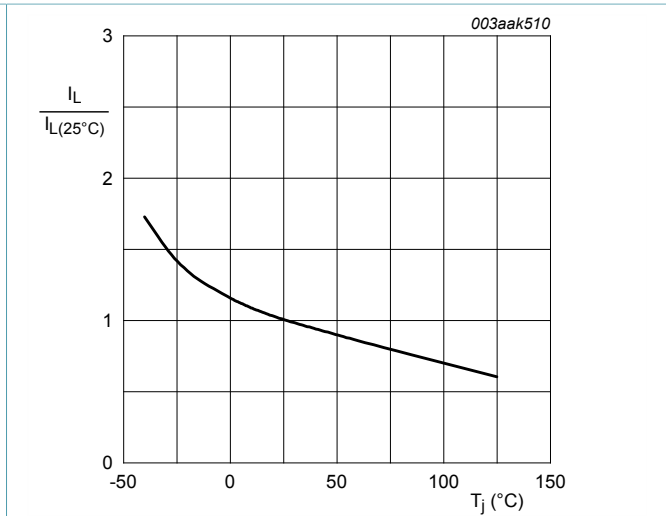


Fig. 8. Normalized latching current as a function of junction temperature

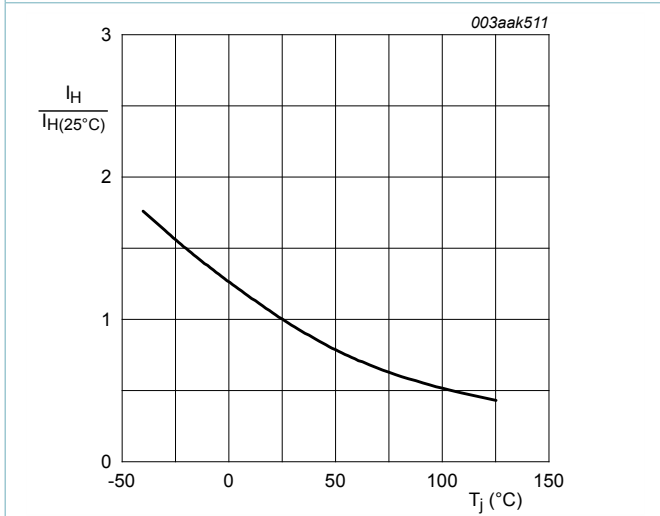


Fig. 9. Normalized holding current as a function of junction temperature

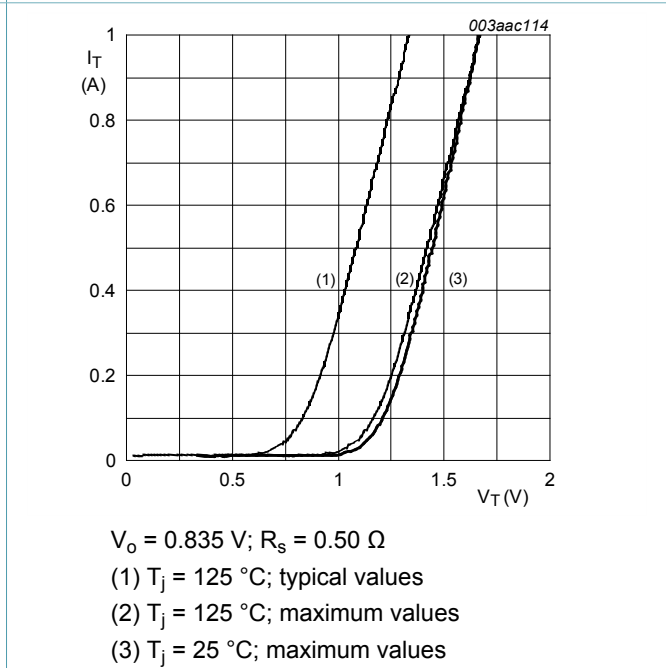


Fig. 10. On-state current as a function of on-state voltage

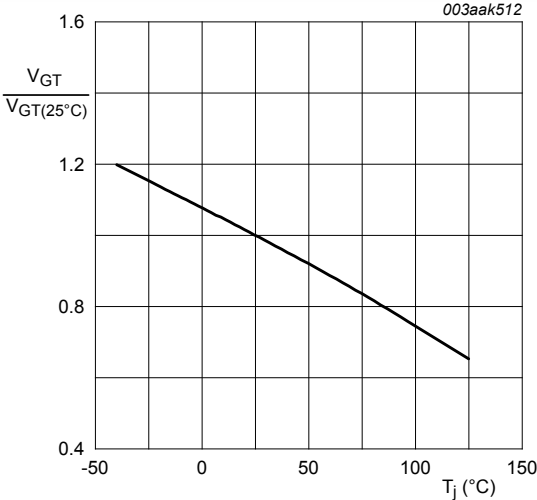


Fig. 11. Normalized gate trigger voltage as a function of junction temperature

7. Package outline

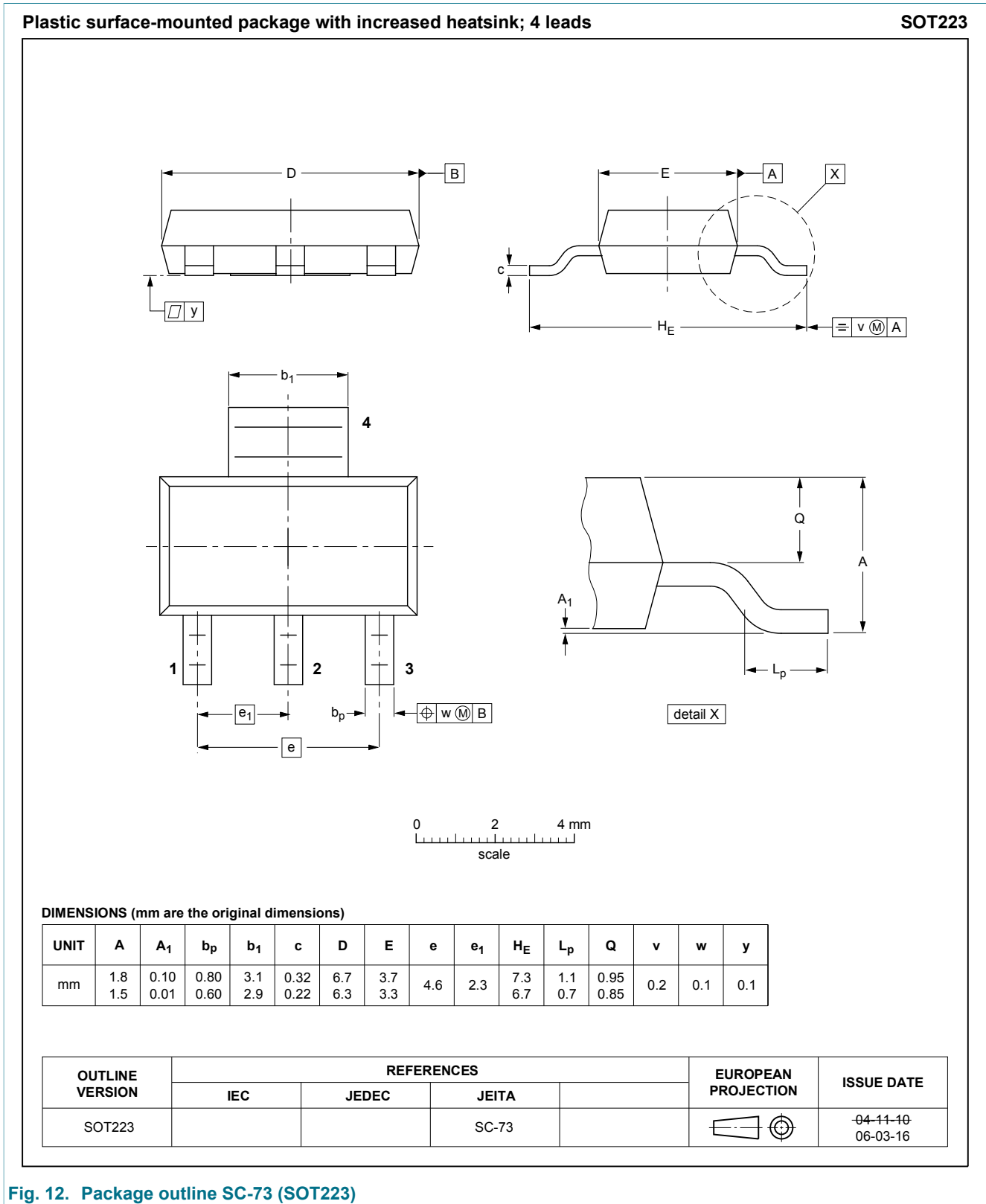


Fig. 12. Package outline SC-73 (SOT223)

8. Soldering

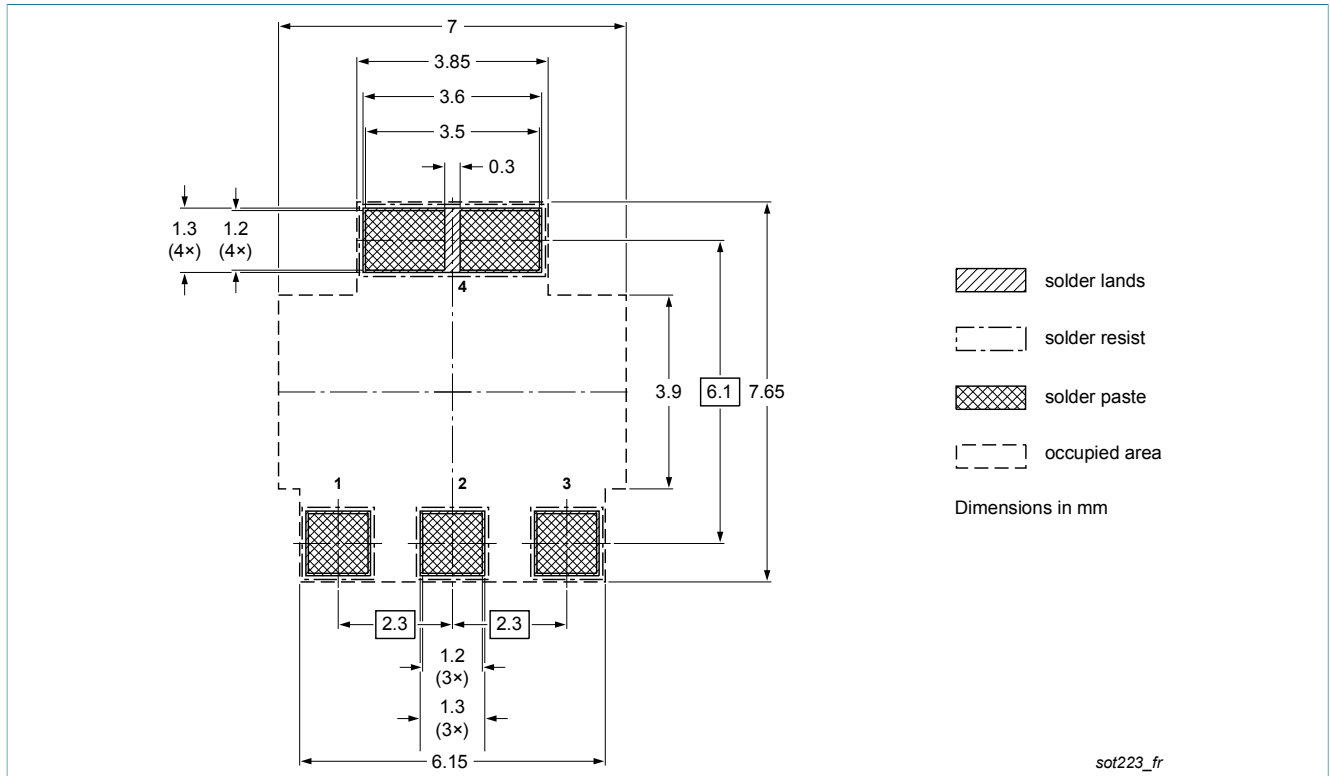


Fig. 13. Reflow soldering footprint for SC-73 (SOT223)

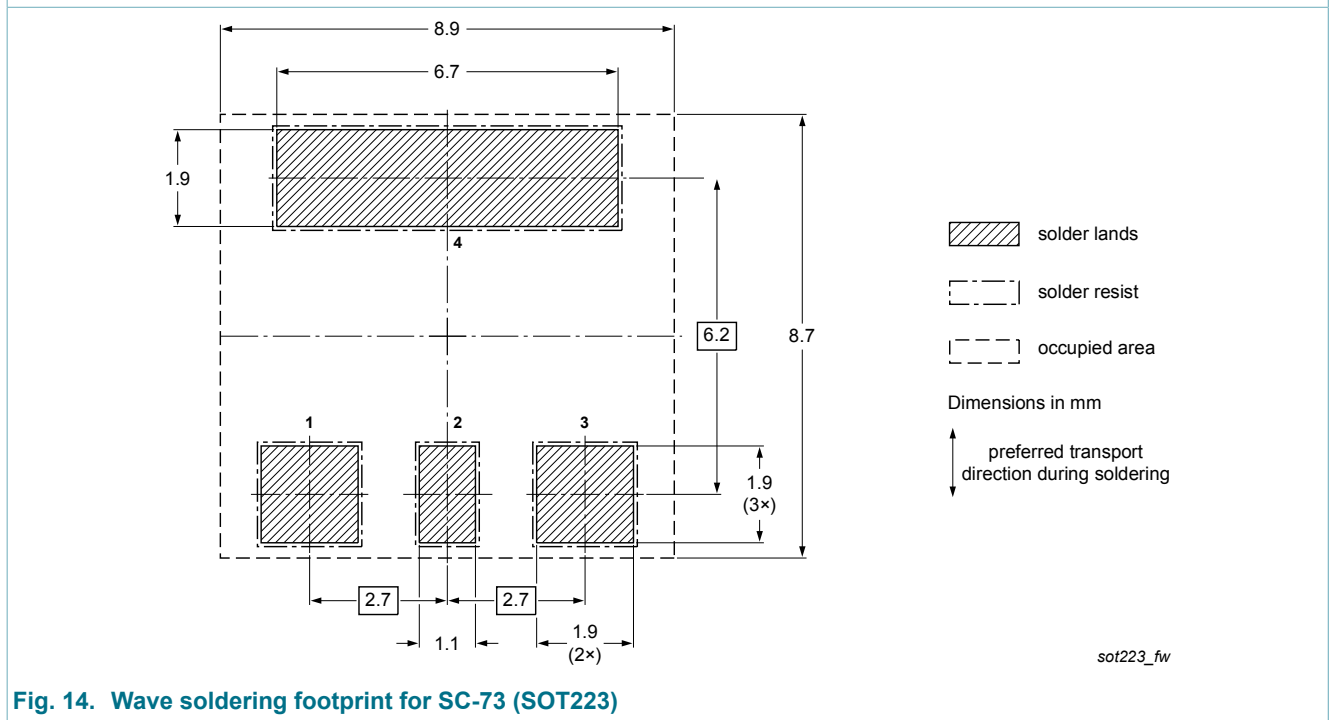


Fig. 14. Wave soldering footprint for SC-73 (SOT223)

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