CY7C1380D
CY7C1380F
CY7C1382D

18-Mbit (512 K × 36/1 M × 18) Pipelined SRAM

Features

- Supports bus operation up to 250 MHz
- Available speed grades are 250, 200, and 167 MHz
- Registered inputs and outputs for pipelined operation
- 3.3 V core power supply
- 2.5 V or 3.3 V I/O power supply
- Fast clock-to-output times
  - 2.6 ns (for 250 MHz device)
- Provides high performance 3-1-1-1 access rate
- User selectable burst counter supporting Intel® Pentium® interleaved or linear burst sequences
- Separate processor and controller address strobes
- Synchronous self-timed write
- Asynchronous output enable
- Single cycle chip deselect
- CY7C1380D/CY7C1382D is available in JEDEC-standard Pb-free 100-pin TQFP package; CY7C1380F is available in non Pb-free 165-ball FBGA package
- IEEE 1149.1 JTAG-Compatible Boundary Scan
- ZZ sleep mode option

Functional Description

The CY7C1380D/CY7C1380F/CY7C1382D SRAM integrates 524,288 × 36 and 1,048,576 × 18 SRAM cells with advanced synchronous peripheral circuitry and a two-bit counter for internal burst operation. All synchronous inputs are gated by registers controlled by a positive edge triggered clock input (CLK). The synchronous inputs include all addresses, all data inputs, address-pipelining chip enable ($\overline{CE}_1$), depth-expansion chip enables (CE_2 and $\overline{CE}_3$), burst control inputs ($\overline{ADSC}$, $\overline{ADSP}$, and $\overline{ADV}$), write enables ($\overline{BW}_X$, and $\overline{BWE}$), and global write ($\overline{GW}$). Asynchronous inputs include the output enable ($\overline{OE}$) and the ZZ pin.

Addresses and chip enables are registered at rising edge of clock when address strobe processor ($\overline{ADSP}$) or address strobe controller ($\overline{ADSC}$) are active. Subsequent burst addresses can be internally generated as they are controlled by the advance pin ($\overline{ADV}$).

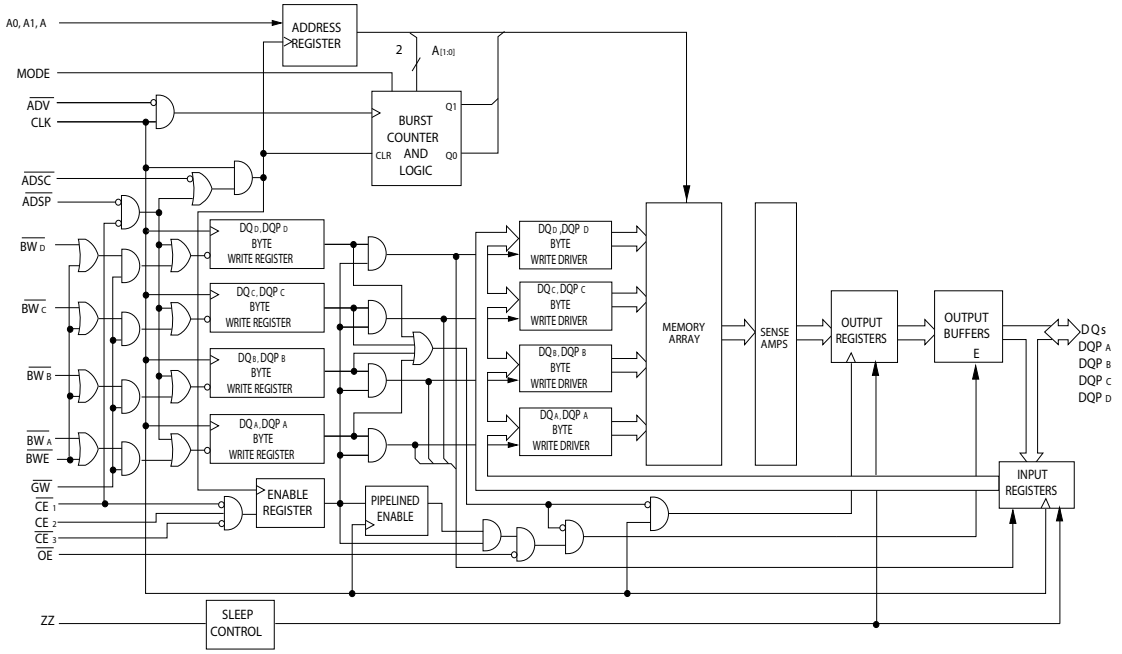
Address, data inputs, and write controls are registered on-chip to initiate a self-timed write cycle. This part supports byte write operations (see Pin Definitions on page 6 and Truth Table on page 9 for further details). Write cycles can be one to two or four bytes wide as controlled by the byte write control inputs. $\overline{GW}$ when active LOW causes all bytes to be written.

The CY7C1380D/CY7C1380F/CY7C1382D operates from a +3.3 V core power supply while all outputs operate with a +2.5 or +3.3 V power supply. All inputs and outputs are JEDEC-standard and JESD8-5-compatible.

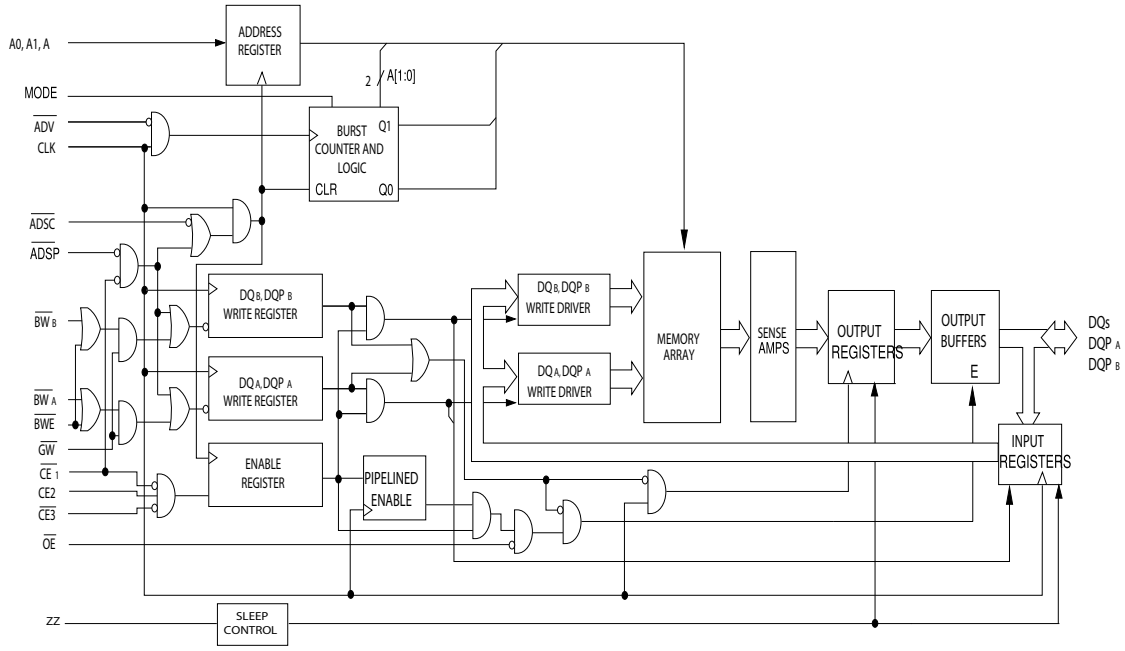
Selection Guide

Description	250 MHz	200 MHz	167 MHz	Unit
Maximum Access Time	2.6	3.0	3.4	ns
Maximum Operating Current	350	300	275	mA
Maximum CMOS Standby Current	70	70	70	mA

Logic Block Diagram – CY7C1380D/CY7C1380F



Logic Block Diagram – CY7C1382D



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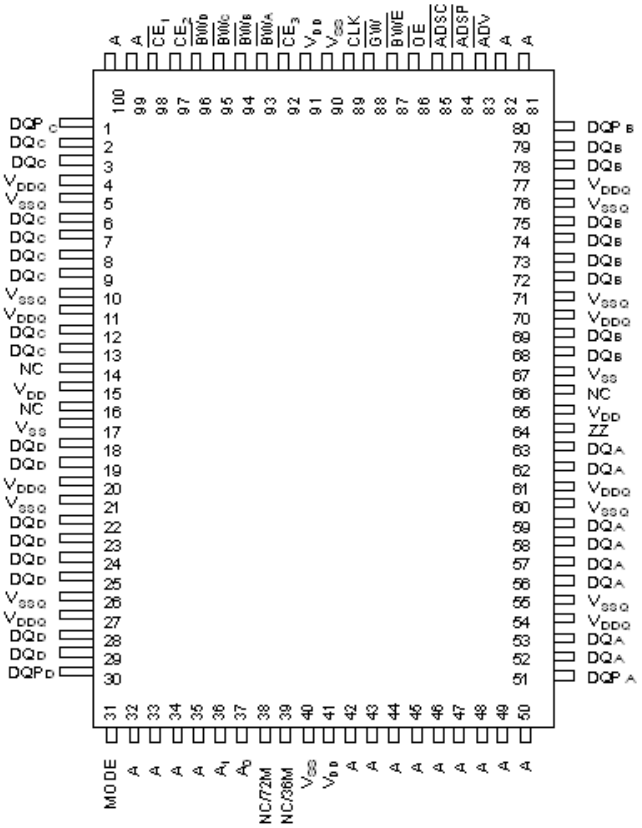
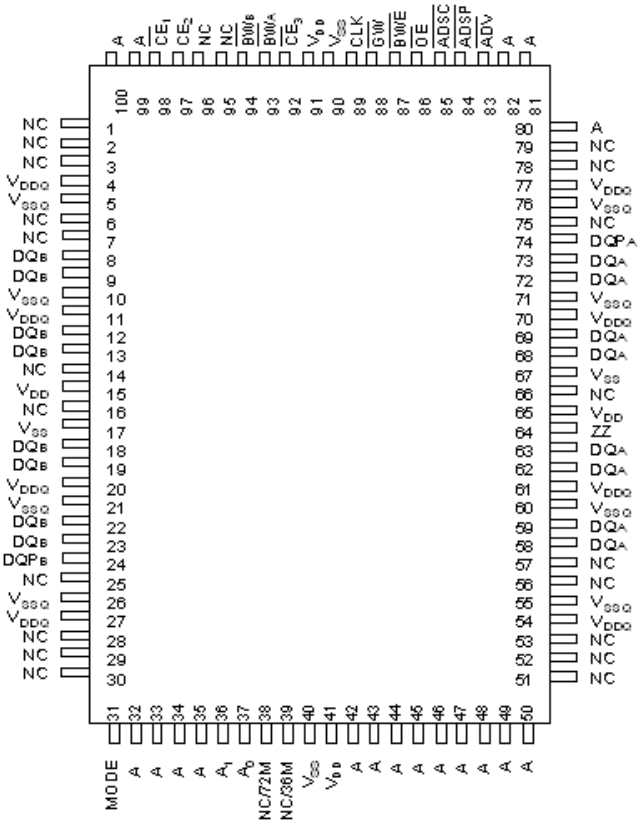
Pin Configurations

Figure 1. 100-pin TQFP (14 × 20 × 1.4 mm) pinout (3-Chip Enable)

CY7C1380D (512 K × 36)



CY7C1382D (1 M × 18)



Pin Configurations *(continued)*

Figure 2. 165-ball FBGA (13 × 15 × 1.4 mm) pinout (3-Chip Enable)

CY7C1380F (512 K × 36)

	1	2	3	4	5	6	7	8	9	10	11
A	NC/288M	A	$\overline{CE}_1$	$\overline{BW}_C$	$\overline{BW}_B$	$\overline{CE}_3$	$\overline{BWE}$	$\overline{ADSC}$	$\overline{ADV}$	A	NC
B	NC/144M	A	CE2	$\overline{BW}_D$	$\overline{BW}_A$	CLK	$\overline{GW}$	$\overline{OE}$	$\overline{ADSP}$	A	NC/576M
C	DQP_C	NC	V_{DDQ}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{DDQ}	NC/1G	DQP_B
D	DQ_C	DQ_C	V_{DDQ}	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	V_{DDQ}	DQ_B	DQ_B
E	DQ_C	DQ_C	V_{DDQ}	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	V_{DDQ}	DQ_B	DQ_B
F	DQ_C	DQ_C	V_{DDQ}	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	V_{DDQ}	DQ_B	DQ_B
G	DQ_C	DQ_C	V_{DDQ}	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	V_{DDQ}	DQ_B	DQ_B
H	NC	NC	NC	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	NC	NC	ZZ
J	DQ_D	DQ_D	V_{DDQ}	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	V_{DDQ}	DQ_A	DQ_A
K	DQ_D	DQ_D	V_{DDQ}	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	V_{DDQ}	DQ_A	DQ_A
L	DQ_D	DQ_D	V_{DDQ}	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	V_{DDQ}	DQ_A	DQ_A
M	DQ_D	DQ_D	V_{DDQ}	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	V_{DDQ}	DQ_A	DQ_A
N	DQP_D	NC	V_{DDQ}	V_{SS}	NC	A	NC	V_{SS}	V_{DDQ}	NC	DQP_A
P	NC	NC/72M	A	A	TDI	A1	TDO	A	A	A	A
R	MODE	NC/36M	A	A	TMS	A0	TCK	A	A	A	A

Pin Definitions

Name	I/O	Description
A_0, A_1, A	Input-Synchronous	**Address inputs used to select one of the address locations**. Sampled at the rising edge of the CLK if $\overline{ADSP}$ or $\overline{ADSC}$ is active LOW, and $\overline{CE}_1$, CE_2, and $\overline{CE}_3$ are sampled active. A1:A0 are fed to the two-bit counter.
$\overline{BW}_A$, $\overline{BW}_B$, $\overline{BW}_C$, $\overline{BW}_D$	Input-Synchronous	**Byte write select inputs, active LOW.** Qualified with $\overline{BWE}$ to conduct byte writes to the SRAM. Sampled on the rising edge of CLK.
$\overline{GW}$	Input-Synchronous	**Global write enable input, active LOW**. When asserted LOW on the rising edge of CLK, a global write is conducted (all bytes are written, regardless of the values on $\overline{BW}_X$ and $\overline{BWE}$).
$\overline{BWE}$	Input-Synchronous	**Byte write enable input, active LOW**. Sampled on the rising edge of CLK. This signal must be asserted LOW to conduct a byte write.
CLK	Input-Clock	**Clock input**. Used to capture all synchronous inputs to the device. Also used to increment the burst counter when $\overline{ADV}$ is asserted LOW, during a burst operation.
$\overline{CE}_1$	Input-Synchronous	**Chip enable 1 input, active LOW**. Sampled on the rising edge of CLK. Used in conjunction with CE_2 and $\overline{CE}_3$ to select or deselect the device. $\overline{ADSP}$ is ignored if $\overline{CE}_1$ is HIGH. $\overline{CE}_1$ is sampled only when a new external address is loaded.
CE_2	Input-Synchronous	**Chip enable 2 input, active HIGH**. Sampled on the rising edge of CLK. Used in conjunction with $\overline{CE}_1$ and $\overline{CE}_3$ to select or deselect the device. CE_2 is sampled only when a new external address is loaded.
$\overline{CE}_3$	Input-Synchronous	**Chip enable 3 input, active LOW**. Sampled on the rising edge of CLK. Used in conjunction with $\overline{CE}_1$ and CE_2 to select or deselect the device. $\overline{CE}_3$ is sampled only when a new external address is loaded.
$\overline{OE}$	Input-Asynchronous	**Output enable, asynchronous input, active LOW**. Controls the direction of the I/O pins. When LOW, the I/O pins behave as outputs. When deasserted HIGH, I/O pins are tri-stated, and act as input data pins. $\overline{OE}$ is masked during the first clock of a read cycle when emerging from a deselected state.
$\overline{ADV}$	Input-Synchronous	**Advance input signal, sampled on the rising edge of CLK, active LOW**. When asserted, it automatically increments the address in a burst cycle.
$\overline{ADSP}$	Input-Synchronous	**Address strobe from processor, sampled on the rising edge of CLK, active LOW**. When asserted LOW, addresses presented to the device are captured in the address registers. A1:A0 are also loaded into the burst counter. When $\overline{ADSP}$ and $\overline{ADSC}$ are both asserted, only $\overline{ADSP}$ is recognized. ASDP is ignored when $\overline{CE}_1$ is deasserted HIGH.
$\overline{ADSC}$	Input-Synchronous	**Address strobe from controller, sampled on the rising edge of CLK, active LOW**. When asserted LOW, addresses presented to the device are captured in the address registers. A1:A0 are also loaded into the burst counter. When $\overline{ADSP}$ and $\overline{ADSC}$ are both asserted, only $\overline{ADSP}$ is recognized.
ZZ	Input-Asynchronous	**ZZ sleep input**. This active HIGH input places the device in a non-time critical sleep condition with data integrity preserved. For normal operation, this pin has to be LOW or left floating. ZZ pin has an internal pull down.
DQs, DQP_X	I/O-Synchronous	**Bidirectional data I/O lines**. As inputs, they feed into an on-chip data register that is triggered by the rising edge of CLK. As outputs, they deliver the data contained in the memory location specified by the addresses presented during the previous clock rise of the read cycle. The direction of the pins is controlled by $\overline{OE}$. When $\overline{OE}$ is asserted LOW, the pins behave as outputs. When HIGH, DQs and DQP_X are placed in a tri-state condition.
V_{DD}	Power Supply	**Power supply inputs to the core of the device**
V_{SS}	Ground	**Ground for the core of the device**.
V_{SSQ}	I/O Ground	**Ground for the I/O circuitry**.
V_{DDQ}	I/O Power Supply	**Power supply for the I/O circuitry**.
MODE	Input-Static	**Selects burst order**. When tied to GND selects linear burst sequence. When tied to V_{DD} or left floating selects interleaved burst sequence. This is a strap pin and must remain static during device operation. Mode pin has an internal pull up.

Pin Definitions *(continued)*

Name	I/O	Description
TDO	JTAG serial output Synchronous	**Serial data-out to the JTAG circuit**. Delivers data on the negative edge of TCK. If the JTAG feature is not being utilized, this pin must be disconnected. This pin is not available on TQFP packages.
TDI	JTAG serial input Synchronous	**Serial data-in to the JTAG circuit**. Sampled on the rising edge of TCK. If the JTAG feature is not being utilized, this pin can be disconnected or connected to V_{DD}. This pin is not available on TQFP packages.
TMS	JTAG serial input Synchronous	**Serial data-in to the JTAG circuit**. Sampled on the rising edge of TCK. If the JTAG feature is not being utilized, this pin can be disconnected or connected to V_{DD}. This pin is not available on TQFP packages.
TCK	JTAG-Clock	**Clock input to the JTAG circuitry**. If the JTAG feature is not being utilized, this pin must be connected to V_{SS}. This pin is not available on TQFP packages.
NC	–	**No Connects**. 36M, 72M, 144M, 288M, 576M, and 1G are address expansion pins and are not internally connected to the die.

Functional Overview

All synchronous inputs pass through input registers controlled by the rising edge of the clock. All data outputs pass through output registers controlled by the rising edge of the clock. Maximum access delay from the clock rise (t_{CO}) is 2.6 ns (250 MHz device).

CY7C1380D/CY7C1380F/CY7C1382D supports secondary cache in systems using a linear or interleaved burst sequence. The interleaved burst order supports Pentium and i486™ processors. The linear burst sequence suits processors that use a linear burst sequence. The burst order is user selectable, and is determined by sampling the MODE input. Accesses can be initiated with either the processor address strobe ($\overline{ADSP}$) or the controller address strobe ($\overline{ADSC}$). Address advancement through the burst sequence is controlled by the $\overline{ADV}$ input. A two-bit on-chip wraparound burst counter captures the first address in a burst sequence and automatically increments the address for the rest of the burst access.

Byte write operations are qualified with the byte write enable ($\overline{BWE}$) and byte write select ($\overline{BW_X}$) inputs. A global write enable ($\overline{GW}$) overrides all byte write inputs and writes data to all four bytes. All writes are simplified with on-chip synchronous self-timed write circuitry.

Three synchronous chip selects ($\overline{CE_1}$, CE_2, $\overline{CE_3}$) and an asynchronous output enable ($\overline{OE}$) provide for easy bank selection and output tri-state control. $\overline{ADSP}$ is ignored if $\overline{CE_1}$ is HIGH.

Single Read Accesses

This access is initiated when the following conditions are satisfied at clock rise: (1) $\overline{ADSP}$ or $\overline{ADSC}$ is asserted LOW, (2) $\overline{CE_1}$, CE_2, $\overline{CE_3}$ are all asserted active, and (3) the write signals ($\overline{GW}$, $\overline{BWE}$) are all deserted HIGH. $\overline{ADSP}$ is ignored if $\overline{CE_1}$ is HIGH. The address presented to the address inputs (A) is stored into the address advancement logic and the address register while being presented to the memory array. The corresponding data is enabled to propagate to the input of the output registers. At the rising edge of the next clock, the data is enabled to propagate through the output register and onto the data bus within 2.6 ns (250 MHz device) if $\overline{OE}$ is active LOW. The only exception occurs when the SRAM is emerging from a deselected state to a selected state; its outputs are always tri-stated during the first cycle of the access. After the first cycle of the access, the outputs are controlled by the $\overline{OE}$ signal. Consecutive single read cycles are supported. Once the SRAM is deselected at clock rise by the chip select and either $\overline{ADSP}$ or $\overline{ADSC}$ signals, its output tri-states immediately.

Single Write Accesses Initiated by $\overline{ADSP}$

This access is initiated when both the following conditions are satisfied at clock rise: (1) $\overline{ADSP}$ is asserted LOW and (2) $\overline{CE_1}$, CE_2, and $\overline{CE_3}$ are all asserted active. The address presented to A is loaded into the address register and the address advancement logic while being delivered to the memory array. The write signals ($\overline{GW}$, $\overline{BWE}$, and $\overline{BW_X}$) and $\overline{ADV}$ inputs are ignored during this first cycle.

$\overline{ADSP}$ triggered write accesses require two clock cycles to complete. If $\overline{GW}$ is asserted LOW on the second clock rise, the data presented to the DQs inputs is written into the corresponding address location in the memory array. If $\overline{GW}$ is HIGH, then the write operation is controlled by $\overline{BWE}$ and $\overline{BW_X}$ signals.

CY7C1380D/CY7C1380F/CY7C1382D provides byte write capability that is described in the write cycle descriptions table. Asserting the byte write enable input ($\overline{BWE}$) with the selected byte write ($\overline{BW_X}$) input, selectively writes to only the desired bytes. Bytes not selected during a byte write operation remain unaltered. A synchronous self-timed write mechanism has been provided to simplify the write operations.

CY7C1380D/CY7C1380F/CY7C1382D is a common I/O device, the output enable ($\overline{OE}$) must be deserted HIGH before presenting data to the DQs inputs. Doing so tri-states the output drivers. As a safety precaution, DQs are automatically tri-stated whenever a write cycle is detected, regardless of the state of $\overline{OE}$.

Single Write Accesses Initiated by $\overline{ADSC}$

$\overline{ADSC}$ write accesses are initiated when the following conditions are satisfied: (1) $\overline{ADSC}$ is asserted LOW, (2) $\overline{ADSP}$ is deserted HIGH, (3) $\overline{CE}_1$, CE_2, and $\overline{CE}_3$ are all asserted active, and (4) the appropriate combination of the write inputs ($\overline{GW}$, $\overline{BWE}$, and $\overline{BW}_X$) are asserted active to conduct a write to the desired byte(s). $\overline{ADSC}$-triggered Write accesses require a single clock cycle to complete. The address presented to A is loaded into the address register and the address advancement logic while being delivered to the memory array. The $\overline{ADV}$ input is ignored during this cycle. If a global write is conducted, the data presented to the DQs is written into the corresponding address location in the memory core. If a byte write is conducted, only the selected bytes are written. Bytes not selected during a byte write operation remain unaltered. A synchronous self-timed write mechanism has been provided to simplify the write operations.

CY7C1380D/CY7C1380F/CY7C1382D is a common I/O device, the output enable ($\overline{OE}$) must be deserted HIGH before presenting data to the DQs inputs. Doing so tri-states the output drivers. As a safety precaution, DQs are automatically tri-stated whenever a write cycle is detected, regardless of the state of $\overline{OE}$.

Burst Sequences

CY7C1380D/CY7C1380F/CY7C1382D provides a two-bit wraparound counter, fed by A1:A0, that implements an interleaved or a linear burst sequence. The interleaved burst sequence is designed specifically to support Intel Pentium applications. The linear burst sequence is designed to support processors that follow a linear burst sequence. The burst sequence is user selectable through the MODE input.

Asserting $\overline{ADV}$ LOW at clock rise automatically increments the burst counter to the next address in the burst sequence. Both read and write burst operations are supported.

Sleep Mode

The ZZ input pin is an asynchronous input. Asserting ZZ places the SRAM in a power conservation sleep mode. Two clock cycles are required to enter into or exit from this sleep mode. While in this mode, data integrity is guaranteed. Accesses pending when entering the sleep mode are not considered valid nor is the completion of the operation guaranteed. The device must be deselected prior to entering the sleep mode. $\overline{CE}_1$, CE_2, $\overline{CE}_3$, $\overline{ADSP}$, and $\overline{ADSC}$ must remain inactive for the duration of t_{ZZREC} after the ZZ input returns LOW.

Interleaved Burst Address Table

(MODE = Floating or V_{DD})

First Address A1:A0	Second Address A1:A0	Third Address A1:A0	Fourth Address A1:A0
00	01	10	11
01	00	11	10
10	11	00	01
11	10	01	00

Linear Burst Address Table

(MODE = GND)

First Address A1:A0	Second Address A1:A0	Third Address A1:A0	Fourth Address A1:A0
00	01	10	11
01	10	11	00
10	11	00	01
11	00	01	10

ZZ Mode Electrical Characteristics

Parameter	Description	Test Conditions	Min	Max	Unit
I_{DDZZ}	Sleep mode standby current	$ZZ \geq V_{DD} - 0.2$ V	–	80	mA
t_{ZZS}	Device operation to ZZ	$ZZ \geq V_{DD} - 0.2$ V	–	$2t_{CYC}$	ns
t_{ZZREC}	ZZ recovery time	$ZZ \leq 0.2$ V	$2t_{CYC}$	–	ns
t_{ZZI}	ZZ Active to sleep current	This parameter is sampled	–	$2t_{CYC}$	ns
t_{RZZI}	ZZ Inactive to exit sleep current	This parameter is sampled	0	–	ns

Truth Table

The Truth Table for CY7C1380D/CY7C1380F/CY7C1382D follows. [1, 2, 3, 4, 5]

Operation	Add. Used	$\overline{CE_1}$	CE_2	$\overline{CE_3}$	ZZ	$\overline{ADSP}$	$\overline{ADSC}$	$\overline{ADV}$	$\overline{WRITE}$	$\overline{OE}$	CLK	DQ
Deselect Cycle, Power Down	None	H	X	X	L	X	L	X	X	X	L–H	Tri-state
Deselect Cycle, Power Down	None	L	L	X	L	L	X	X	X	X	L–H	Tri-state
Deselect Cycle, Power Down	None	L	X	H	L	L	X	X	X	X	L–H	Tri-state
Deselect Cycle, Power Down	None	L	L	X	L	H	L	X	X	X	L–H	Tri-state
Deselect Cycle, Power Down	None	L	X	H	L	H	L	X	X	X	L–H	Tri-state
Sleep Mode, Power Down	None	X	X	X	H	X	X	X	X	X	X	Tri-state
READ Cycle, Begin Burst	External	L	H	L	L	L	X	X	X	L	L–H	Q
READ Cycle, Begin Burst	External	L	H	L	L	L	X	X	X	H	L–H	Tri-state
WRITE Cycle, Begin Burst	External	L	H	L	L	H	L	X	L	X	L–H	D
READ Cycle, Begin Burst	External	L	H	L	L	H	L	X	H	L	L–H	Q
READ Cycle, Begin Burst	External	L	H	L	L	H	L	X	H	H	L–H	Tri-state
READ Cycle, Continue Burst	Next	X	X	X	L	H	H	L	H	L	L–H	Q
READ Cycle, Continue Burst	Next	X	X	X	L	H	H	L	H	H	L–H	Tri-state
READ Cycle, Continue Burst	Next	H	X	X	L	X	H	L	H	L	L–H	Q
READ Cycle, Continue Burst	Next	H	X	X	L	X	H	L	H	H	L–H	Tri-state
WRITE Cycle, Continue Burst	Next	X	X	X	L	H	H	L	L	X	L–H	D
WRITE Cycle, Continue Burst	Next	H	X	X	L	X	H	L	L	X	L–H	D
READ Cycle, Suspend Burst	Current	X	X	X	L	H	H	H	H	L	L–H	Q
READ Cycle, Suspend Burst	Current	X	X	X	L	H	H	H	H	H	L–H	Tri-state
READ Cycle, Suspend Burst	Current	H	X	X	L	X	H	H	H	L	L–H	Q
READ Cycle, Suspend Burst	Current	H	X	X	L	X	H	H	H	H	L–H	Tri-state
WRITE Cycle, Suspend Burst	Current	X	X	X	L	H	H	H	L	X	L–H	D
WRITE Cycle, Suspend Burst	Current	H	X	X	L	X	H	H	L	X	L–H	D

Notes
1. X = Don't Care, H = Logic HIGH, L = Logic LOW.
2. $\overline{WRITE}$ = L when any one or more byte write enable signals, and $\overline{BWE}$ = L or $\overline{GW}$ = L. $\overline{WRITE}$ = H when all byte write enable signals, $\overline{BWE}$, $\overline{GW}$ = H.
3. The DQ pins are controlled by the current cycle and the $\overline{OE}$ signal. $\overline{OE}$ is asynchronous and is not sampled with the clock.
4. The SRAM always initiates a read cycle when ADSP is asserted, regardless of the state of $\overline{GW}$, $\overline{BWE}$, or $\overline{BW_X}$. Writes may occur only on subsequent clocks after the $\overline{ADSP}$ or with the assertion of $\overline{ADSC}$. As a result, $\overline{OE}$ must be driven HIGH prior to the start of the write cycle to allow the outputs to tri-state. $\overline{OE}$ is a don't care for the remainder of the write cycle.
5. $\overline{OE}$ is asynchronous and is not sampled with the clock rise. It is masked internally during write cycles. During a read cycle all data bits are tri-state when $\overline{OE}$ is inactive or when the device is deselected, and all data bits behave as output when $\overline{OE}$ is active (LOW).

Truth Table for Read/Write

The Truth Table for Read/Write for CY7C1380D/CY7C1380F follows. [6, 7]

Function (CY7C1380D/CY7C1380F)	$\overline{GW}$	$\overline{BWE}$	$\overline{BW_D}$	$\overline{BW_C}$	$\overline{BW_B}$	$\overline{BW_A}$
Read	H	H	X	X	X	X
Read	H	L	H	H	H	H
Write Byte A – (DQ_A and DQP_A)	H	L	H	H	H	L
Write Byte B – (DQ_B and DQP_B)	H	L	H	H	L	H
Write Bytes B, A	H	L	H	H	L	L
Write Byte C – (DQ_C and DQP_C)	H	L	H	L	H	H
Write Bytes C, A	H	L	H	L	H	L
Write Bytes C, B	H	L	H	L	L	H
Write Bytes C, B, A	H	L	H	L	L	L
Write Byte D – (DQ_D and DQP_D)	H	L	L	H	H	H
Write Bytes D, A	H	L	L	H	H	L
Write Bytes D, B	H	L	L	H	L	H
Write Bytes D, B, A	H	L	L	H	L	L
Write Bytes D, C	H	L	L	L	H	H
Write Bytes D, C, A	H	L	L	L	H	L
Write Bytes D, C, B	H	L	L	L	L	H
Write All Bytes	H	L	L	L	L	L
Write All Bytes	L	X	X	X	X	X

Truth Table for Read/Write

The Truth Table for Read/Write for CY7C1382D follows. [6, 7]

Function (CY7C1382D)	$\overline{GW}$	$\overline{BWE}$	$\overline{BW_B}$	$\overline{BW_A}$
Read	H	H	X	X
Read	H	L	H	H
Write Byte A – (DQ_A and DQP_A)	H	L	H	L
Write Byte B – (DQ_B and DQP_B)	H	L	L	H
Write Bytes B, A	H	L	L	L
Write All Bytes	H	L	L	L
Write All Bytes	L	X	X	X

Notes
6. X = Don't Care, H = Logic HIGH, L = Logic LOW.
7. Table only lists a partial listing of the byte write combinations. Any combination of $\overline{BW_X}$ is valid. Appropriate write is done based on which byte write is active.

IEEE 1149.1 Serial Boundary Scan (JTAG)

The CY7C1380F incorporates a serial boundary scan test access port (TAP).This part is fully compliant with 1149.1. The TAP operates using JEDEC-standard 3.3 V or 2.5 V I/O logic levels.

CY7C1380F contains a TAP controller, instruction register, boundary scan register, bypass register, and ID register.

Disabling the JTAG Feature

It is possible to operate the SRAM without using the JTAG feature. To disable the TAP controller, TCK must be tied LOW (V_{SS}) to prevent clocking of the device. TDI and TMS are internally pulled up and may be unconnected. They may alternately be connected to V_{DD} through a pull up resistor. TDO must be left unconnected. Upon power up, the device comes up in a reset state which does not interfere with the operation of the device.

Test Access Port (TAP)

Test Clock (TCK)

The test clock is used only with the TAP controller. All inputs are captured on the rising edge of TCK. All outputs are driven from the falling edge of TCK.

Test MODE SELECT (TMS)

The TMS input is used to give commands to the TAP controller and is sampled on the rising edge of TCK. This pin may be left unconnected if the TAP is not used. The ball is pulled up internally, resulting in a logic HIGH level.

Test Data-In (TDI)

The TDI ball is used to serially input information into the registers and can be connected to the input of any of the registers. The register between TDI and TDO is chosen by the instruction that is loaded into the TAP instruction register. For information on loading the instruction register, see TAP Controller State Diagram on page 13. TDI is internally pulled up and can be unconnected if the TAP is unused in an application. TDI is connected to the most significant bit (MSB) of any register.

Test Data-Out (TDO)

The TDO output ball is used to serially clock data-out from the registers. The output is active depending upon the current state of the TAP state machine (see Identification Codes on page 17). The output changes on the falling edge of TCK. TDO is connected to the least significant bit (LSB) of any register.

Performing a TAP Reset

A Reset is performed by forcing TMS HIGH (V_{DD}) for five rising edges of TCK. This Reset does not affect the operation of the SRAM and may be performed while the SRAM is operating.

At power up, the TAP is reset internally to ensure that TDO comes up in a high Z state.

TAP Registers

Registers are connected between the TDI and TDO balls and enable data to be scanned in and out of the SRAM test circuitry. Only one register can be selected at a time through the instruction register. Data is serially loaded into the TDI ball on the rising edge of TCK. Data is output on the TDO ball on the falling edge of TCK.

Instruction Register

Three-bit instructions can be serially loaded into the instruction register. This register is loaded when it is placed between the TDI and TDO balls as shown in the TAP Controller Block Diagram on page 14. Upon power up, the instruction register is loaded with the IDCODE instruction. It is also loaded with the IDCODE instruction if the controller is placed in a reset state as described in the previous section.

When the TAP controller is in the Capture-IR state, the two least significant bits are loaded with a binary ‘01’ pattern to enable fault isolation of the board-level serial test data path.

Bypass Register

To save time when serially shifting data through registers, it is sometimes advantageous to skip certain chips. The bypass register is a single-bit register that can be placed between the TDI and TDO balls. This enables data to be shifted through the SRAM with minimal delay. The bypass register is set LOW (V_{SS}) when the BYPASS instruction is executed.

Boundary Scan Register

The boundary scan register is connected to all the input and bidirectional balls on the SRAM.

The boundary scan register is loaded with the contents of the RAM input and output ring when the TAP controller is in the Capture-DR state and is then placed between the TDI and TDO balls when the controller is moved to the Shift-DR state. The EXTEST, SAMPLE/PRELOAD, and SAMPLE Z instructions can be used to capture the contents of the input and output ring.

The Boundary Scan Order on page 18 show the order in which the bits are connected. Each bit corresponds to one of the bumps on the SRAM package. The MSB of the register is connected to TDI, and the LSB is connected to TDO.

Identification (ID) Register

The ID register is loaded with a vendor-specific 32-bit code during the Capture-DR state when the IDCODE command is loaded in the instruction register. The IDCODE is hardwired into the SRAM and can be shifted out when the TAP controller is in the Shift-DR state. The ID register has a vendor code and other information described in the Identification Register Definitions on page 17.

TAP Instruction Set

Overview

Eight different instructions are possible with the three bit instruction register. All combinations are listed in Identification Codes on page 17. Three of these instructions are listed as RESERVED and must not be used. The other five instructions are described in detail in this section.

Instructions are loaded into the TAP controller during the Shift-IR state when the instruction register is placed between TDI and TDO. During this state, instructions are shifted through the instruction register through the TDI and TDO balls. To execute

the instruction once it is shifted in, the TAP controller must be moved into the Update-IR state.

EXTEST

The EXTEST instruction enables the preloaded data to be driven out through the system output pins. This instruction also selects the boundary scan register to be connected for serial access between the TDI and TDO in the Shift-DR controller state.

IDCODE

The IDCODE instruction causes a vendor-specific 32-bit code to be loaded into the instruction register. It also places the instruction register between the TDI and TDO balls and enables the IDCODE to be shifted out of the device when the TAP controller enters the Shift-DR state.

The IDCODE instruction is loaded into the instruction register upon power up or whenever the TAP controller is given a test logic reset state.

SAMPLE Z

The SAMPLE Z instruction causes the boundary scan register to be connected between the TDI and TDO balls when the TAP controller is in a Shift-DR state. The SAMPLE Z command places all SRAM outputs into a high Z state.

SAMPLE/PRELOAD

SAMPLE/PRELOAD is a 1149.1 mandatory instruction. When the SAMPLE/PRELOAD instructions are loaded into the instruction register and the TAP controller is in the Capture-DR state, a snapshot of data on the input and output pins is captured in the boundary scan register.

The TAP controller clock can only operate at a frequency up to 20 MHz, while the SRAM clock operates more than an order of magnitude faster. As there is a large difference in the clock frequencies, it is possible that during the Capture-DR state, an input or output undergoes a transition. The TAP may then try to capture a signal while in transition (metastable state). This does not harm the device, but there is no guarantee as to the value that is captured. Repeatable results may not be possible.

To guarantee that the boundary scan register captures the correct value of a signal, the SRAM signal must be stabilized long enough to meet the TAP controller's capture setup plus hold times (t_{CS} and t_{CH}). The SRAM clock input might not be captured correctly if there is no way in a design to stop (or slow) the clock during a SAMPLE/PRELOAD instruction. If this is an issue, it is still possible to capture all other signals and simply ignore the value of the CK and CK# captured in the boundary scan register.

Once the data is captured, it is possible to shift out the data by putting the TAP into the Shift-DR state. This places the boundary scan register between the TDI and TDO pins.

PRELOAD enables an initial data pattern to be placed at the latched parallel outputs of the boundary scan register cells prior to the selection of another boundary scan test operation.

The shifting of data for the SAMPLE and PRELOAD phases can occur concurrently when required; that is, while data captured is shifted out, the preloaded data is shifted in.

BYPASS

When the BYPASS instruction is loaded in the instruction register and the TAP is placed in a Shift-DR state, the bypass register is placed between the TDI and TDO balls. The advantage of the BYPASS instruction is that it shortens the boundary scan path when multiple devices are connected together on a board.

EXTEST Output Bus Tri-State

IEEE Standard 1149.1 mandates that the TAP controller be able to put the output bus into a tri-state mode.

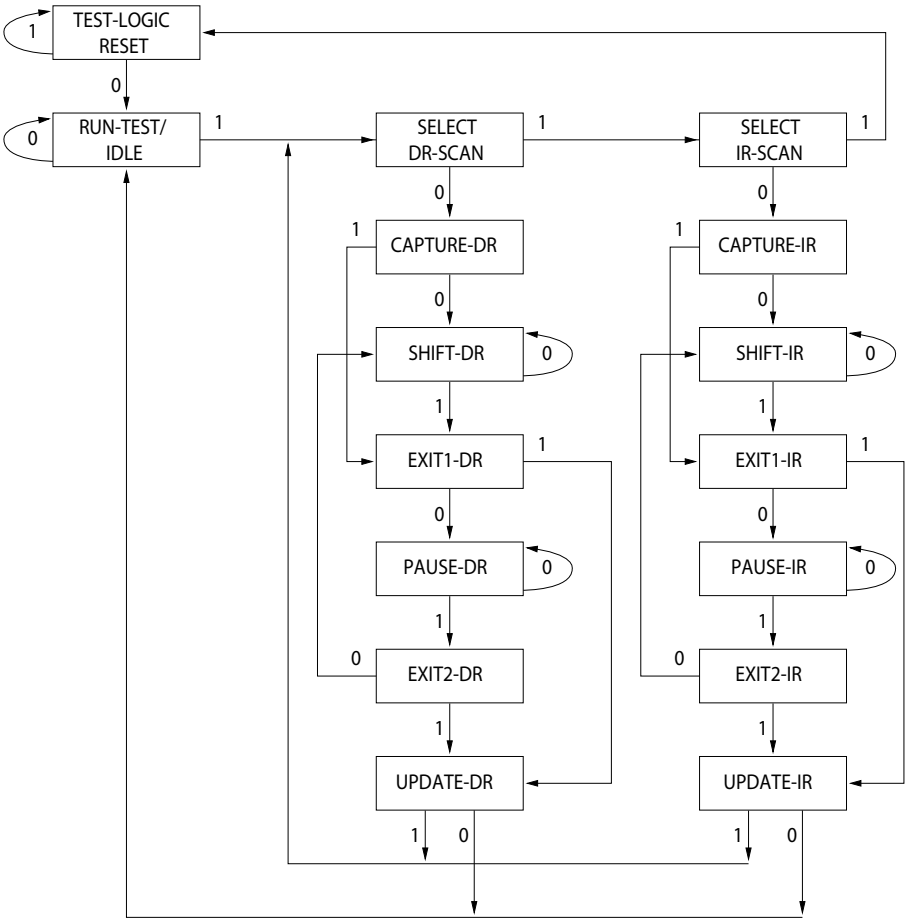
The boundary scan register has a special bit located at Bit #89 (for 165-ball FBGA package). When this scan cell, called the "extest output bus tri-state," is latched into the preload register during the Update-DR state in the TAP controller, it directly controls the state of the output (Q-bus) pins, when the EXTEST is entered as the current instruction. When HIGH, it enables the output buffers to drive the output bus. When LOW, this bit places the output bus into a high Z condition.

This bit can be set by entering the SAMPLE/PRELOAD or EXTEST command, and then shifting the desired bit into that cell, during the Shift-DR state. During Update-DR, the value loaded into that shift-register cell latches into the preload register. When the EXTEST instruction is entered, this bit directly controls the output Q-bus pins. Note that this bit is preset HIGH to enable the output when the device is powered up, and also when the TAP controller is in the Test-Logic-Reset state.

Reserved

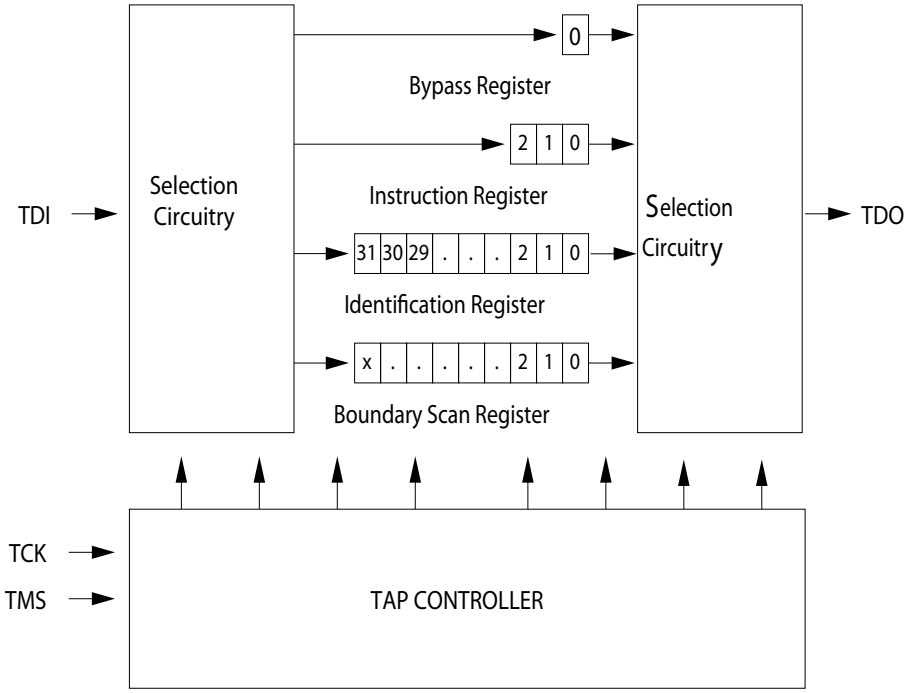
These instructions are not implemented but are reserved for future use. Do not use these instructions.

TAP Controller State Diagram



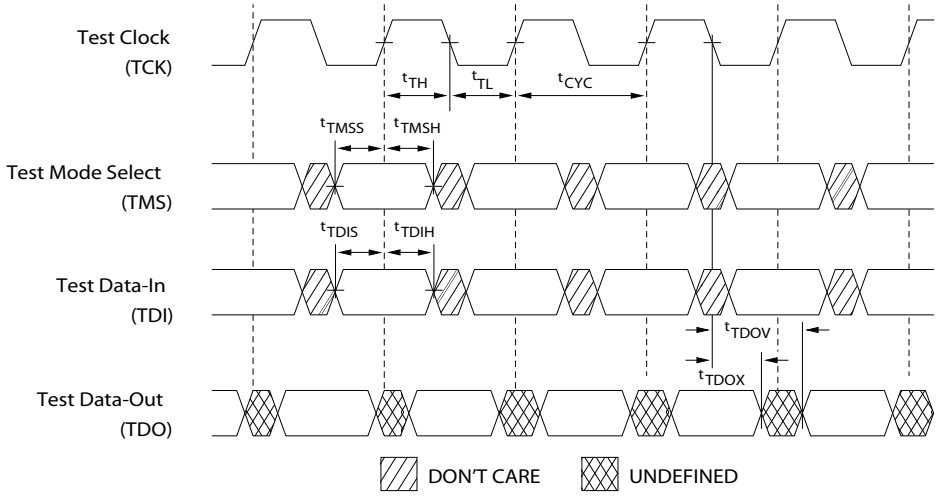
The 0 or 1 next to each state represents the value of TMS at the rising edge of TCK.

TAP Controller Block Diagram



TAP Timing

Figure 3. TAP Timing



TAP AC Switching Characteristics

Over the Operating Range

Parameter [8, 9]	Description	Min	Max	Unit
Clock				
t_{TCYC}	TCK Clock Cycle Time	50	–	ns
t_{TF}	TCK Clock Frequency	–	20	MHz
t_{TH}	TCK Clock HIGH time	20	–	ns
t_{TL}	TCK Clock LOW time	20	–	ns
Output Times				
t_{TDOV}	TCK Clock LOW to TDO Valid	–	10	ns
t_{TDOX}	TCK Clock LOW to TDO Invalid	0	–	ns
Setup Times				
t_{TMSS}	TMS Setup to TCK Clock Rise	5	–	ns
t_{TDIS}	TDI Setup to TCK Clock Rise	5	–	ns
t_{CS}	Capture Setup to TCK Rise	5	–	ns
Hold Times				
t_{TMSH}	TMS Hold after TCK Clock Rise	5	–	ns
t_{TDIH}	TDI Hold after Clock Rise	5	–	ns
t_{CH}	Capture Hold after Clock Rise	5	–	ns

Notes
8. t_{CS} and t_{CH} refer to the setup and hold time requirements of latching data from the boundary scan register.
9. Test conditions are specified using the load in TAP AC test conditions. t_R/t_F = 1 ns.

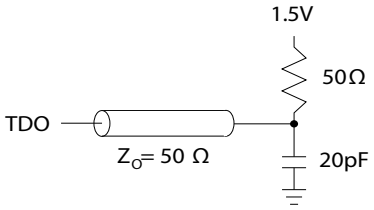
3.3 V TAP AC Test Conditions

Input pulse levels ..... V_{SS} to 3.3 V
Input rise and fall times ..... 1 ns
Input timing reference levels ..... 1.5 V
Output reference levels ..... 1.5 V
Test load termination supply voltage ..... 1.5 V

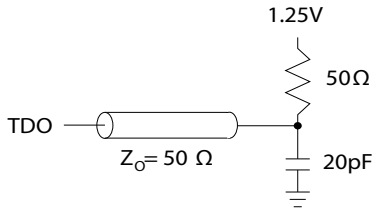
2.5 V TAP AC Test Conditions

Input pulse levels ..... V_{SS} to 2.5 V
Input rise and fall time ..... 1 ns
Input timing reference levels ..... 1.25 V
Output reference levels ..... 1.25 V
Test load termination supply voltage ..... 1.25 V

3.3 V TAP AC Output Load Equivalent



2.5 V TAP AC Output Load Equivalent



TAP DC Electrical Characteristics and Operating Conditions

(0 °C < T_A < +70 °C; V_{DD} = 3.3 V ± 0.165 V unless otherwise noted)

Parameter [10]	Description	Test Conditions		Min	Max	Unit
V_{OH1}	Output HIGH Voltage	I_{OH} = –4.0 mA, V_{DDQ} = 3.3 V		2.4	–	V
		I_{OH} = –1.0 mA, V_{DDQ} = 2.5 V		2.0	–	V
V_{OH2}	Output HIGH Voltage	I_{OH} = –100 µA	V_{DDQ} = 3.3 V	2.9	–	V
			V_{DDQ} = 2.5 V	2.1	–	V
V_{OL1}	Output LOW Voltage	I_{OL} = 8.0 mA	V_{DDQ} = 3.3 V	–	0.4	V
			V_{DDQ} = 2.5 V	–	0.4	V
V_{OL2}	Output LOW Voltage	I_{OL} = 100 µA	V_{DDQ} = 3.3 V	–	0.2	V
			V_{DDQ} = 2.5 V	–	0.2	V
V_{IH}	Input HIGH Voltage		V_{DDQ} = 3.3 V	2.0	V_{DD} + 0.3	V
			V_{DDQ} = 2.5 V	1.7	V_{DD} + 0.3	V
V_{IL}	Input LOW Voltage		V_{DDQ} = 3.3 V	–0.3	0.8	V
			V_{DDQ} = 2.5 V	–0.3	0.7	V
I_X	Input Load Current	GND ≤ V_{IN} ≤ V_{DDQ}		–5	5	µA

Note
10. All voltages referenced to V_{SS} (GND).

Identification Register Definitions

Instruction Field	CY7C1380F (512 K × 36)	Description
Revision Number (31:29)	000	Describes the version number.
Device Depth (28:24) [11]	01011	Reserved for internal use.
Device Width (23:18) 165-ball FBGA	000000	Defines the memory type and architecture.
Cypress Device ID (17:12)	100101	Defines the width and density.
Cypress JEDEC ID Code (11:1)	00000110100	Allows unique identification of SRAM vendor.
ID Register Presence Indicator (0)	1	Indicates the presence of an ID register.

Scan Register Sizes

Register Name	Bit Size (× 36)
Instruction	3
Bypass	1
ID	32
Boundary Scan Order (165-ball FBGA package)	89

Identification Codes

Instruction	Code	Description
EXTEST	000	Captures I/O ring contents. Places the boundary scan register between TDI and TDO. Forces all SRAM outputs to high Z state.
IDCODE	001	Loads the ID register with the vendor ID code and places the register between TDI and TDO. This operation does not affect SRAM operations.
SAMPLE Z	010	Captures I/O ring contents. Places the boundary scan register between TDI and TDO. Forces all SRAM output drivers to a high Z state.
RESERVED	011	Do Not Use. This instruction is reserved for future use.
SAMPLE/PRELOAD	100	Captures I/O ring contents. Places the boundary scan register between TDI and TDO. Does not affect SRAM operation.
RESERVED	101	Do Not Use. This instruction is reserved for future use.
RESERVED	110	Do Not Use. This instruction is reserved for future use.
BYPASS	111	Places the bypass register between TDI and TDO. This operation does not affect SRAM operations.

Note
11. Bit #24 is 1 in the register definitions for both 2.5 V and 3.3 V versions of this device.

Boundary Scan Order

165-ball BGA [12, 13]

Bit #	Ball ID
1	N6
2	N7
3	N10
4	P11
5	P8
6	R8
7	R9
8	P9
9	P10
10	R10
11	R11
12	H11
13	N11
14	M11
15	L11
16	K11
17	J11
18	M10
19	L10
20	K10
21	J10
22	H9
23	H10
24	G11
25	F11
26	E11
27	D11
28	G10
29	F10
30	E10

Bit #	Ball ID
31	D10
32	C11
33	A11
34	B11
35	A10
36	B10
37	A9
38	B9
39	C10
40	A8
41	B8
42	A7
43	B7
44	B6
45	A6
46	B5
47	A5
48	A4
49	B4
50	B3
51	A3
52	A2
53	B2
54	C2
55	B1
56	A1
57	C1
58	D1
59	E1
60	F1

Bit #	Ball ID
61	G1
62	D2
63	E2
64	F2
65	G2
66	H1
67	H3
68	J1
69	K1
70	L1
71	M1
72	J2
73	K2
74	L2
75	M2
76	N1
77	N2
78	P1
79	R1
80	R2
81	P3
82	R3
83	P2
84	R4
85	P4
86	N5
87	P6
88	R6
89	Internal

Note
12. Balls which are NC (No Connect) are pre-set LOW.
13. Bit# 89 is pre-set HIGH.

Maximum Ratings

Exceeding the maximum ratings may impair the useful life of the device. For user guidelines, not tested.

Storage Temperature ..... –65 °C to +150 °C

Ambient Temperature with Power Applied ..... –55 °C to +125 °C

Supply Voltage on V_{DD} Relative to GND .....–0.3 V to +4.6 V

Supply Voltage on V_{DDQ} Relative to GND .... –0.3 V to +V_{DD}

DC Voltage Applied to Outputs in tri-state .....–0.5 V to V_{DDQ} + 0.5 V

DC Input Voltage ..... –0.5 V to V_{DD} + 0.5 V

Current into Outputs (LOW) ..... 20 mA

Static Discharge Voltage (per MIL-STD-883, Method 3015) ..... > 2001 V

Latch-up Current ..... > 200 mA

Operating Range

Range	Ambient Temperature	V_{DD}	V_{DDQ}
Commercial	0 °C to +70 °C	3.3 V – 5% / + 10%	2.5 V – 5% to V_{DD}
Industrial	–40 °C to +85 °C		

Electrical Characteristics

Over the Operating Range

Parameter [14, 15]	Description	Test Conditions		Min	Max	Unit
V_{DD}	Power Supply Voltage			3.135	3.6	V
V_{DDQ}	I/O Supply Voltage	for 3.3 V I/O		3.135	V_{DD}	V
		for 2.5 V I/O		2.375	2.625	V
V_{OH}	Output HIGH Voltage	for 3.3 V I/O, I_{OH} = –4.0 mA		2.4	–	V
		for 2.5 V I/O, I_{OH} = –1.0 mA		2.0	–	V
V_{OL}	Output LOW Voltage	for 3.3 V I/O, I_{OL} = 8.0 mA		–	0.4	V
		for 2.5 V I/O, I_{OL} = 1.0 mA		–	0.4	V
V_{IH}	Input HIGH Voltage [14]	for 3.3 V I/O		2.0	V_{DD} + 0.3 V	V
		for 2.5 V I/O		1.7	V_{DD} + 0.3 V	V
V_{IL}	Input LOW Voltage [14]	for 3.3 V I/O		–0.3	0.8	V
		for 2.5 V I/O		–0.3	0.7	V
I_X	Input Leakage Current except ZZ and MODE	GND ≤ V_I ≤ V_{DDQ}		–5	5	µA
	Input Current of MODE	Input = V_{SS}		–30	–	µA
		Input = V_{DD}			5	µA
	Input Current of ZZ	Input = V_{SS}		–5	–	µA
		Input = V_{DD}			30	µA
I_{OZ}	Output Leakage Current	GND ≤ V_I ≤ V_{DDQ}, Output Disabled		–5	5	µA
I_{DD}	V_{DD} Operating Supply Current	V_{DD} = Max., I_{OUT} = 0 mA, f = f_{MAX} = 1/t_{CYC}	4.0-ns cycle, 250 MHz	–	350	mA
			5.0-ns cycle, 200 MHz	–	300	mA
			6.0-ns cycle, 167 MHz	–	275	mA
I_{SB1}	Automatic CE Power Down Current – TTL Inputs	V_{DD} = Max, Device Deselected, V_{IN} ≥ V_{IH} or V_{IN} ≤ V_{IL}, f = f_{MAX} = 1/t_{CYC}	4.0-ns cycle, 250 MHz	–	160	mA
			5.0-ns cycle, 200 MHz	–	150	mA
			6.0-ns cycle, 167 MHz	–	140	mA

Notes
14. Overshoot: $V_{IH(AC)}$ < V_{DD} + 1.5 V (pulse width less than t_{CYC}/2), undershoot: $V_{IL(AC)}$ > –2 V (pulse width less than t_{CYC}/2).
15. TPower up: Assumes a linear ramp from 0 V to $V_{DD(min.)}$ within 200 ms. During this time V_{IH} < V_{DD} and V_{DDQ} ≤ V_{DD}.

Electrical Characteristics *(continued)*

Over the Operating Range

Parameter [14, 15]	Description	Test Conditions		Min	Max	Unit
I_{SB2}	Automatic CE Power Down Current – CMOS Inputs	V_{DD} = Max, Device Deselected, $V_{IN} \le 0.3$ V or $V_{IN} \ge V_{DDQ} - 0.3$ V, f = 0	All speeds	–	70	mA
I_{SB3}	Automatic CE Power Down Current – CMOS Inputs	V_{DD} = Max, Device Deselected, $V_{IN} \le 0.3$ V or $V_{IN} \ge V_{DDQ} - 0.3$ V, f = f_{MAX} = $1/t_{CYC}$	4.0-ns cycle, 250 MHz	–	135	mA
			5.0-ns cycle, 200 MHz	–	130	mA
			6.0-ns cycle, 167 MHz	–	125	mA
I_{SB4}	Automatic CE Power Down Current – TTL Inputs	V_{DD} = Max, Device Deselected, $V_{IN} \ge V_{IH}$ or $V_{IN} \le V_{IL}$, f = 0	All speeds	–	80	mA

Capacitance

Parameter [16]	Description	Test Conditions	100-pin TQFP Package	165-ball FBGA Package	Unit
C_{IN}	Input capacitance	T_A = 25 °C, f = 1 MHz, V_{DD} = 3.3 V, V_{DDQ} = 2.5 V	5	9	pF
C_{CLK}	Clock input capacitance		5	9	pF
C_{IO}	Input/Output capacitance		5	9	pF

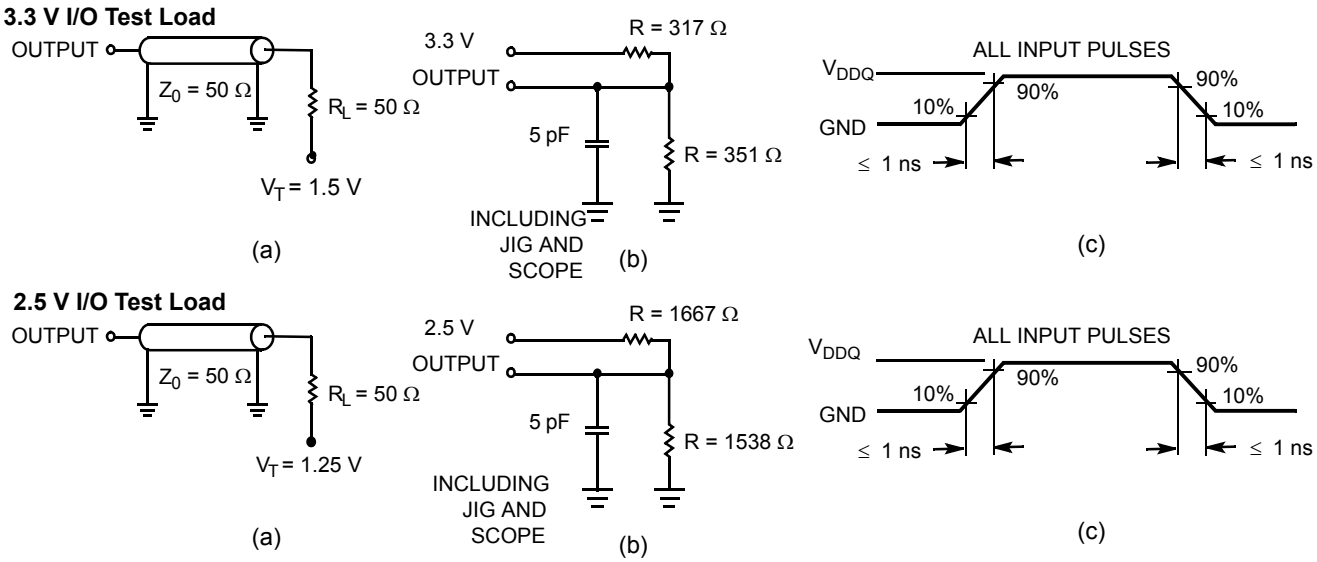
Thermal Resistance

Parameter [16]	Description	Test Conditions	100-pin TQFP Package	165-ball FBGA Package	Unit
Θ_{JA}	Thermal resistance (junction to ambient)	Test conditions follow standard test methods and procedures for measuring thermal impedance, in accordance with EIA/JESD51.	28.66	20.7	°C/W
Θ_{JC}	Thermal resistance (junction to case)		4.08	4.0	°C/W

Note
16. Tested initially and after any design or process change that may affect these parameters.

AC Test Loads and Waveforms

Figure 4. AC Test Loads and Waveforms



Switching Characteristics

Over the Operating Range

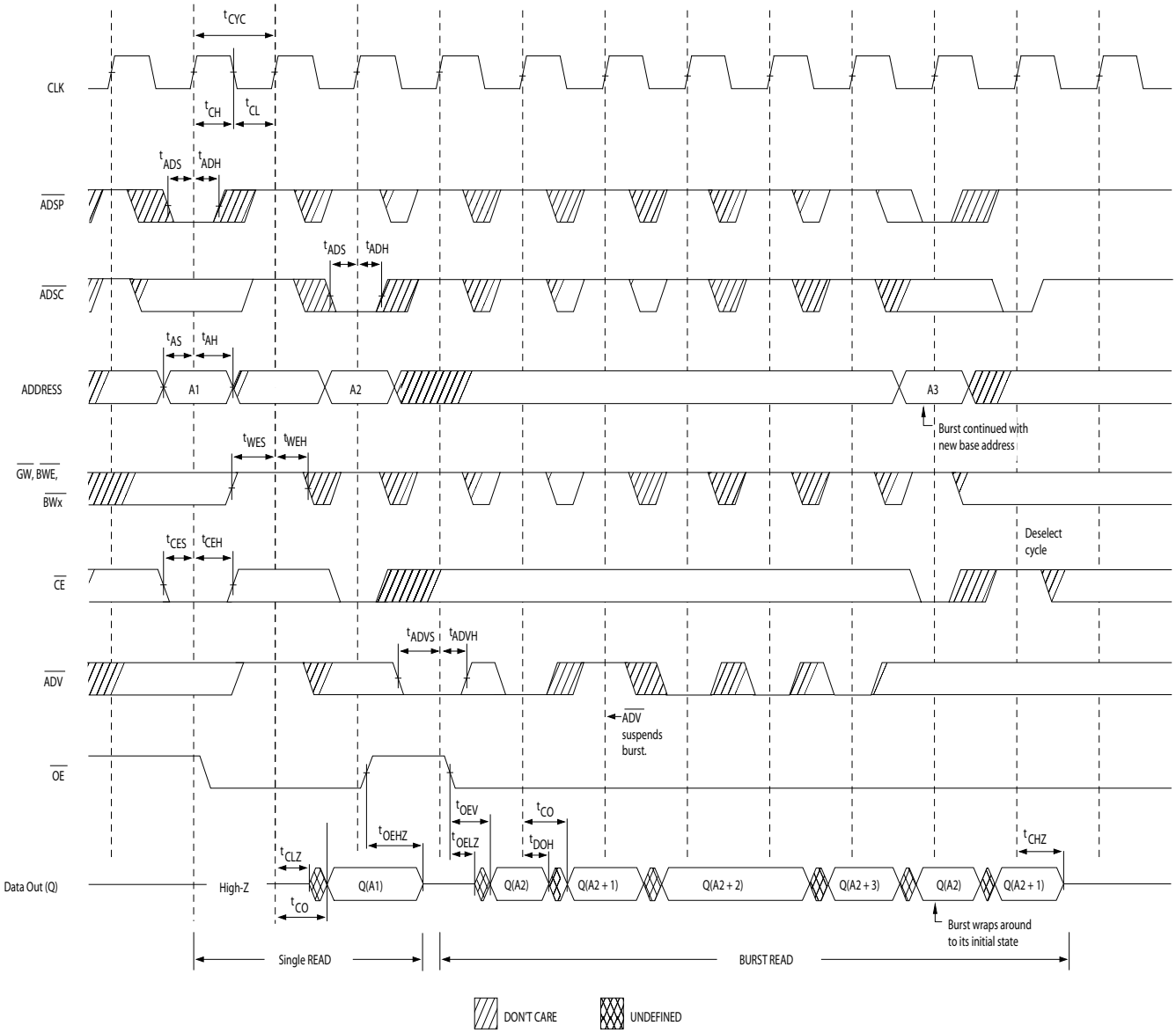
Parameter [17, 18]	Description	250 MHz		200 MHz		167 MHz		Unit
		Min	Max	Min	Max	Min	Max	
t_{POWER}	V_{DD}(typical) to the first Access [19]	1	–	1	–	1	–	ms
Clock								
t_{CYC}	Clock Cycle Time	4.0	–	5	–	6	–	ns
t_{CH}	Clock HIGH	1.7	–	2.0	–	2.2	–	ns
t_{CL}	Clock LOW	1.7	–	2.0	–	2.2	–	ns
Output Times								
t_{CO}	Data Output Valid After CLK Rise	–	2.6	–	3.0	–	3.4	ns
t_{DOH}	Data Output Hold After CLK Rise	1.0	–	1.3	–	1.3	–	ns
t_{CLZ}	Clock to Low-Z [20, 21, 22]	1.0	–	1.3	–	1.3	–	ns
t_{CHZ}	Clock to High-Z [20, 21, 22]	–	2.6	–	3.0	–	3.4	ns
t_{OEV}	$\overline{OE}$ LOW to Output Valid	–	2.6	–	3.0	–	3.4	ns
t_{OELZ}	$\overline{OE}$ LOW to Output Low-Z [20, 21, 22]	0	–	0	–	0	–	ns
t_{OEHZ}	$\overline{OE}$ HIGH to Output High-Z [20, 21, 22]	–	2.6	–	3.0	–	3.4	ns
Setup Times								
t_{AS}	Address Setup Before CLK Rise	1.2	–	1.4	–	1.5	–	ns
t_{ADS}	$\overline{ADSC}$, $\overline{ADSP}$ Setup Before CLK Rise	1.2	–	1.4	–	1.5	–	ns
t_{ADVS}	$\overline{ADV}$ Setup Before CLK Rise	1.2	–	1.4	–	1.5	–	ns
t_{WES}	$\overline{GW}$, $\overline{BWE}$, $\overline{BW_X}$ Setup Before CLK Rise	1.2	–	1.4	–	1.5	–	ns
t_{DS}	Data Input Setup Before CLK Rise	1.2	–	1.4	–	1.5	–	ns
t_{CES}	Chip Enable SetUp Before CLK Rise	1.2	–	1.4	–	1.5	–	ns
Hold Times								
t_{AH}	Address Hold After CLK Rise	0.3	–	0.4	–	0.5	–	ns
t_{ADH}	$\overline{ADSP}$, $\overline{ADSC}$ Hold After CLK Rise	0.3	–	0.4	–	0.5	–	ns
t_{ADVH}	$\overline{ADV}$ Hold After CLK Rise	0.3	–	0.4	–	0.5	–	ns
t_{WEH}	$\overline{GW}$, $\overline{BWE}$, $\overline{BW_X}$ Hold After CLK Rise	0.3	–	0.4	–	0.5	–	ns
t_{DH}	Data Input Hold After CLK Rise	0.3	–	0.4	–	0.5	–	ns
t_{CEH}	Chip Enable Hold After CLK Rise	0.3	–	0.4	–	0.5	–	ns

Notes

17. Timing reference level is 1.5 V when V_{DDQ} = 3.3 V and is 1.25 V when V_{DDQ} = 2.5 V.
18. Test conditions shown in (a) of Figure 4 on page 21 unless otherwise noted.
19. This part has a voltage regulator internally; t_{POWER} is the time that the power needs to be supplied above $V_{DD(minimum)}$ initially before a read or write operation can be initiated.
20. t_{CHZ}, t_{CLZ}, t_{OELZ}, and t_{OEHZ} are specified with AC test conditions shown in part (b) of Figure 4 on page 21. Transition is measured ±200 mV from steady-state voltage.
21. At any given voltage and temperature, t_{OEHZ} is less than t_{OELZ} and t_{CHZ} is less than t_{CLZ} to eliminate bus contention between SRAMs when sharing the same data bus. These specifications do not imply a bus contention condition, but reflect parameters guaranteed over worst case user conditions. Device is designed to achieve high Z prior to low Z under the same system conditions.
22. This parameter is sampled and not 100% tested.

Switching Waveforms

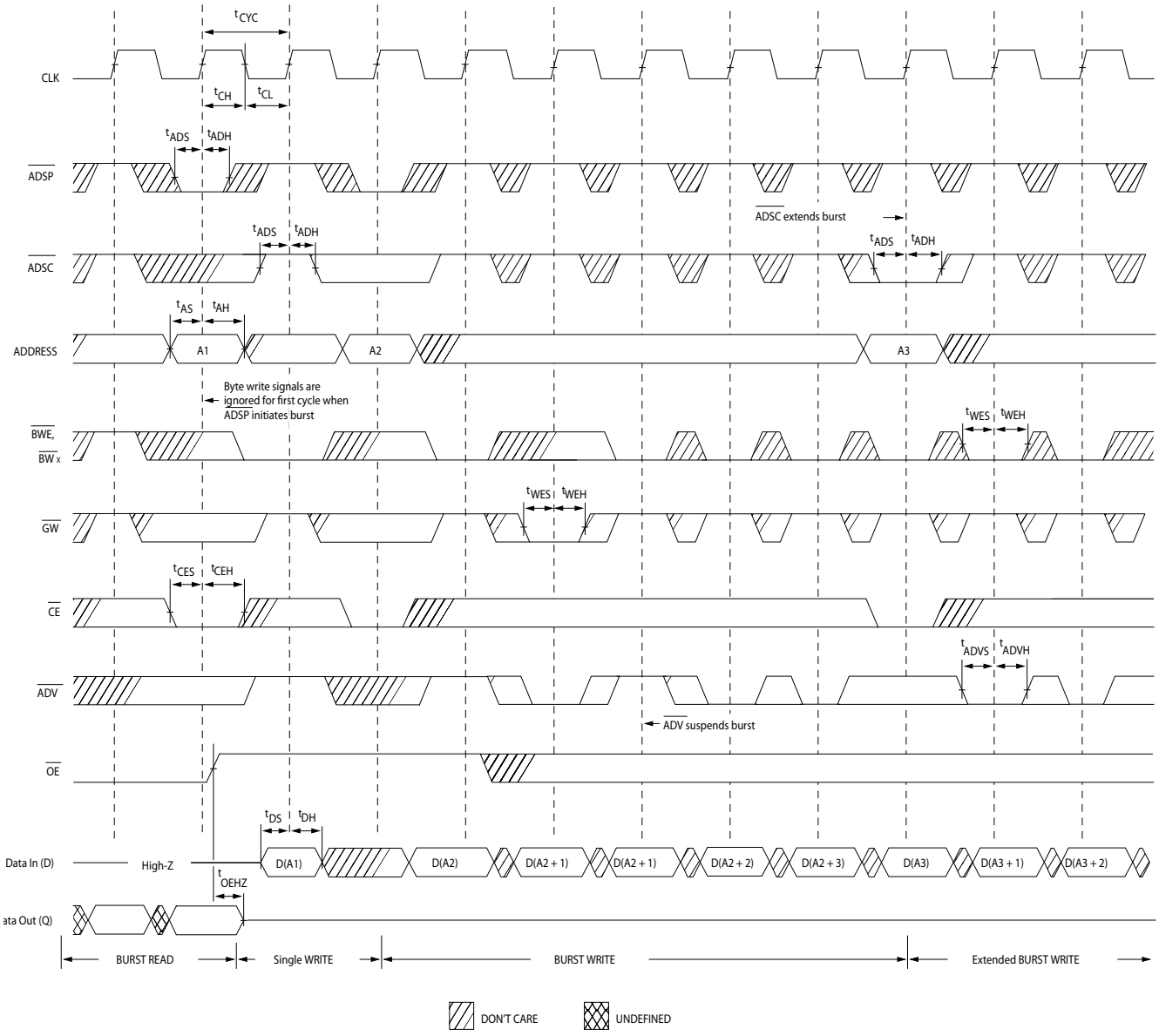
Figure 5. Read Cycle Timing [23]



Note
23. On this diagram, when $\overline{CE}$ is LOW: $\overline{CE}_1$ is LOW, CE_2 is HIGH and $\overline{CE}_3$ is LOW. When $\overline{CE}$ is HIGH: $\overline{CE}_1$ is HIGH or CE_2 is LOW or $\overline{CE}_3$ is HIGH.

Switching Waveforms *(continued)*

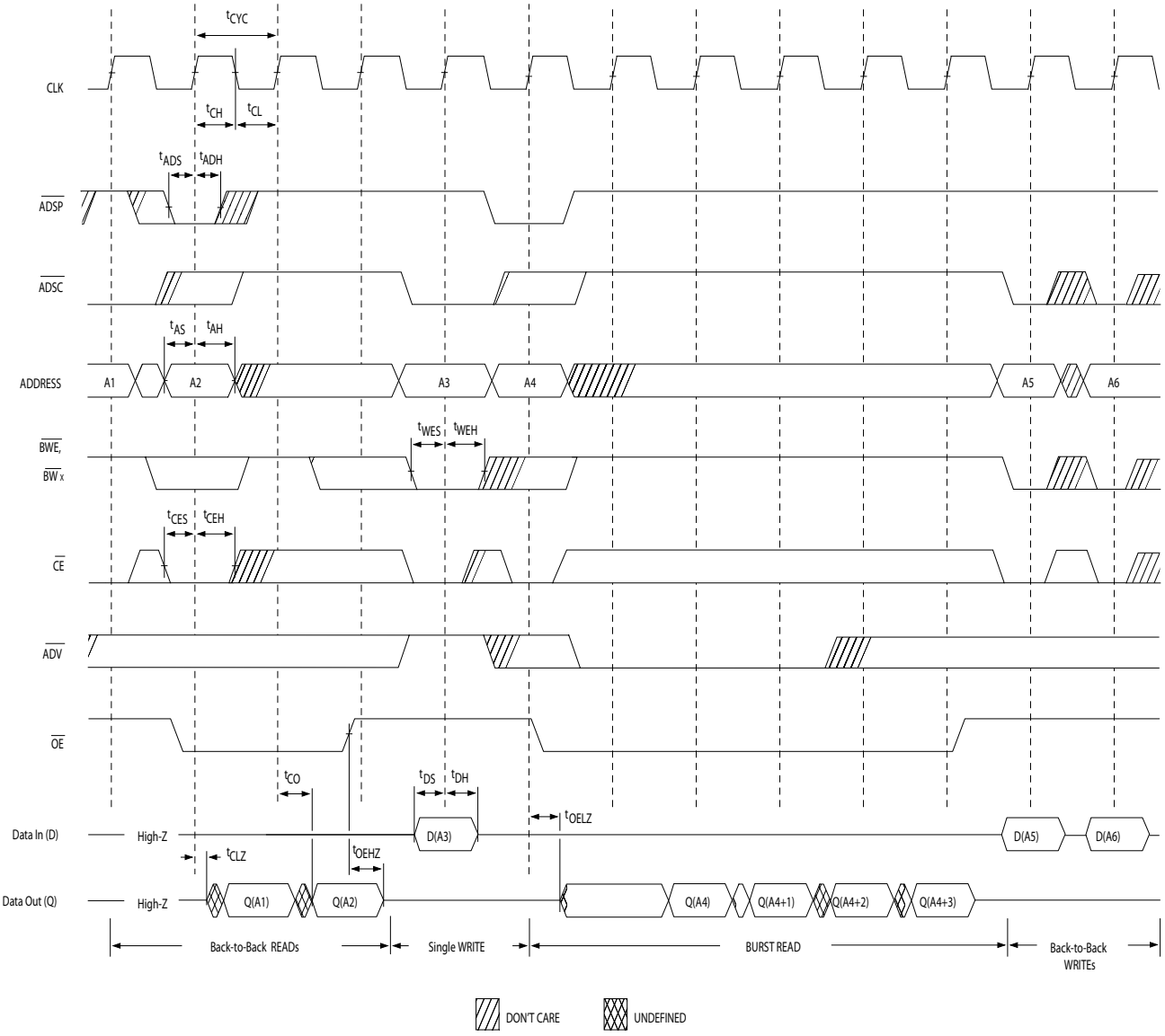
Figure 6. Write Cycle Timing [24, 25]



Notes
24. On this diagram, when $\overline{CE}$ is LOW: $\overline{CE}_1$ is LOW, CE_2 is HIGH and $\overline{CE}_3$ is LOW. When $\overline{CE}$ is HIGH: $\overline{CE}_1$ is HIGH or CE_2 is LOW or $\overline{CE}_3$ is HIGH.
25. Full width write can be initiated by either $\overline{GW}$ LOW; or by $\overline{GW}$ HIGH, $\overline{BWE}$ LOW and $\overline{BW}_X$ LOW.

Switching Waveforms *(continued)*

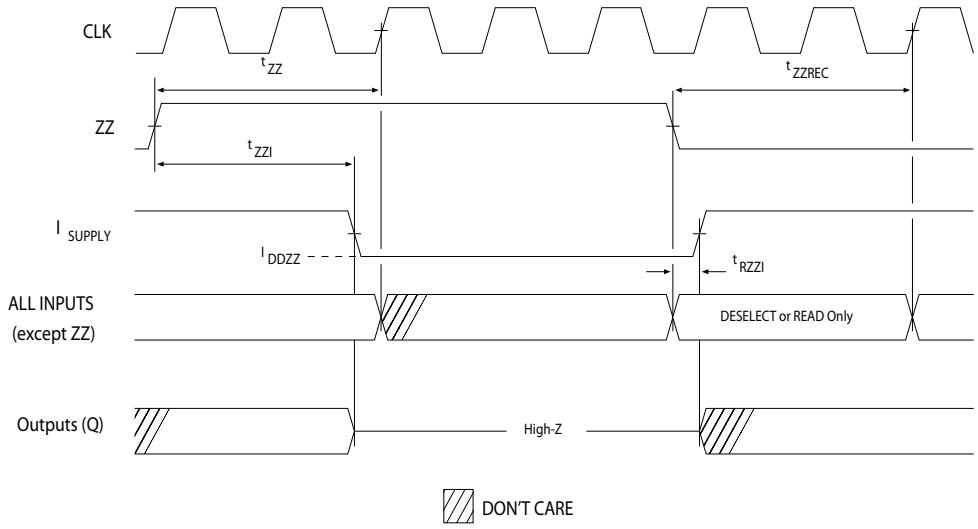
Figure 7. Read/Write Cycle Timing [26, 27, 28]



Notes
26. On this diagram, when $\overline{CE}$ is LOW: $\overline{CE}_1$ is LOW, CE_2 is HIGH and $\overline{CE}_3$ is LOW. When $\overline{CE}$ is HIGH: $\overline{CE}_1$ is HIGH or CE_2 is LOW or $\overline{CE}_3$ is HIGH.
27. The data bus (Q) remains in high Z following a WRITE cycle, unless a new read access is initiated by $\overline{ADSP}$ or $\overline{ADSC}$.
28. $\overline{GW}$ is HIGH.

Switching Waveforms *(continued)*

Figure 8. ZZ Mode Timing [29, 30]



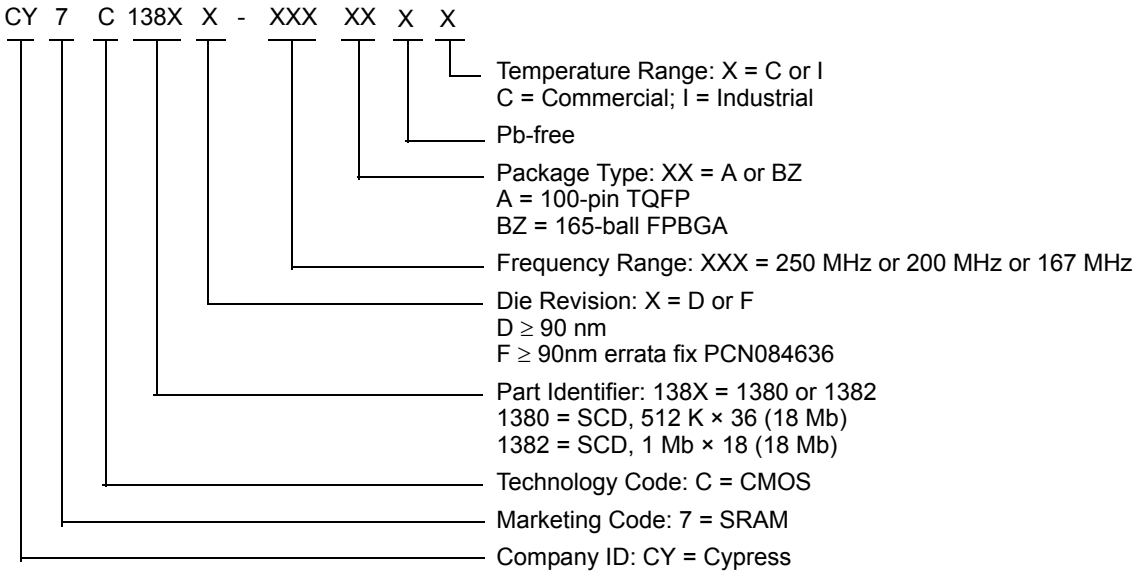
Notes
29. Device must be deselected when entering ZZ mode. See Truth Table on page 9 for all possible signal conditions to deselect the device.
30. DQs are in high Z when exiting ZZ sleep mode.

Ordering Information

The below table lists the key package features and ordering codes. The table contains only the parts that are currently available. If you do not see what you are looking for, contact your local sales representative. For more information, visit the Cypress website at www.cypress.com and refer to the product summary page at http://www.cypress.com/products.

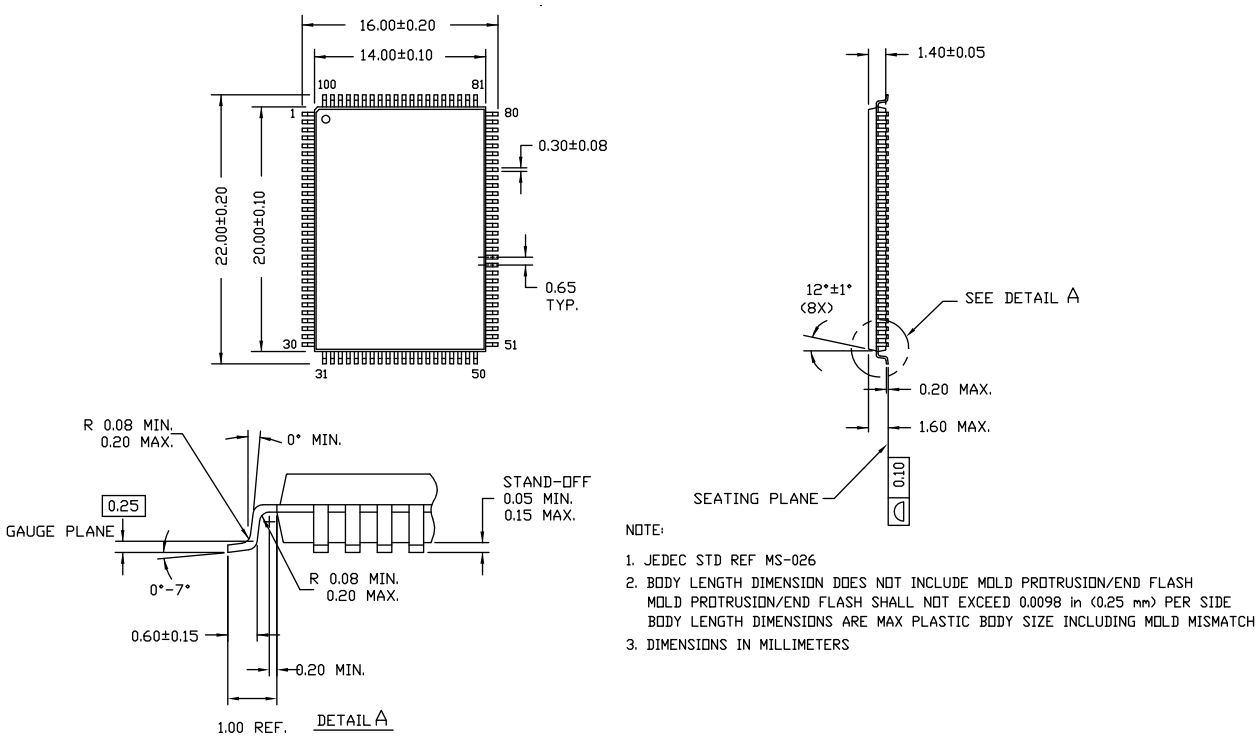
Speed (MHz)	Ordering Code	Package Diagram	Part and Package Type	Operating Range
250	CY7C1380D-250AXC	51-85050	100-pin TQFP (14 × 20 × 1.4 mm) Pb-free	Commercial
200	CY7C1380D-200AXC	51-85050	100-pin TQFP (14 × 20 × 1.4 mm) Pb-free	Commercial
	CY7C1382D-200AXC			
167	CY7C1380D-167AXC	51-85050	100-pin TQFP (14 × 20 × 1.4 mm) Pb-free	Commercial
	CY7C1382D-167AXC			
	CY7C1380D-167AXI	51-85050	100-pin TQFP (14 × 20 × 1.4 mm) Pb-free	Industrial
	CY7C1380F-167BZI	51-85180	165-ball FBGA (13 × 15 × 1.4 mm)	

Ordering Code Definitions



Package Diagrams

Figure 9. 100-pin TQFP (14 × 20 × 1.4 mm) A100RA Package Outline, 51-85050

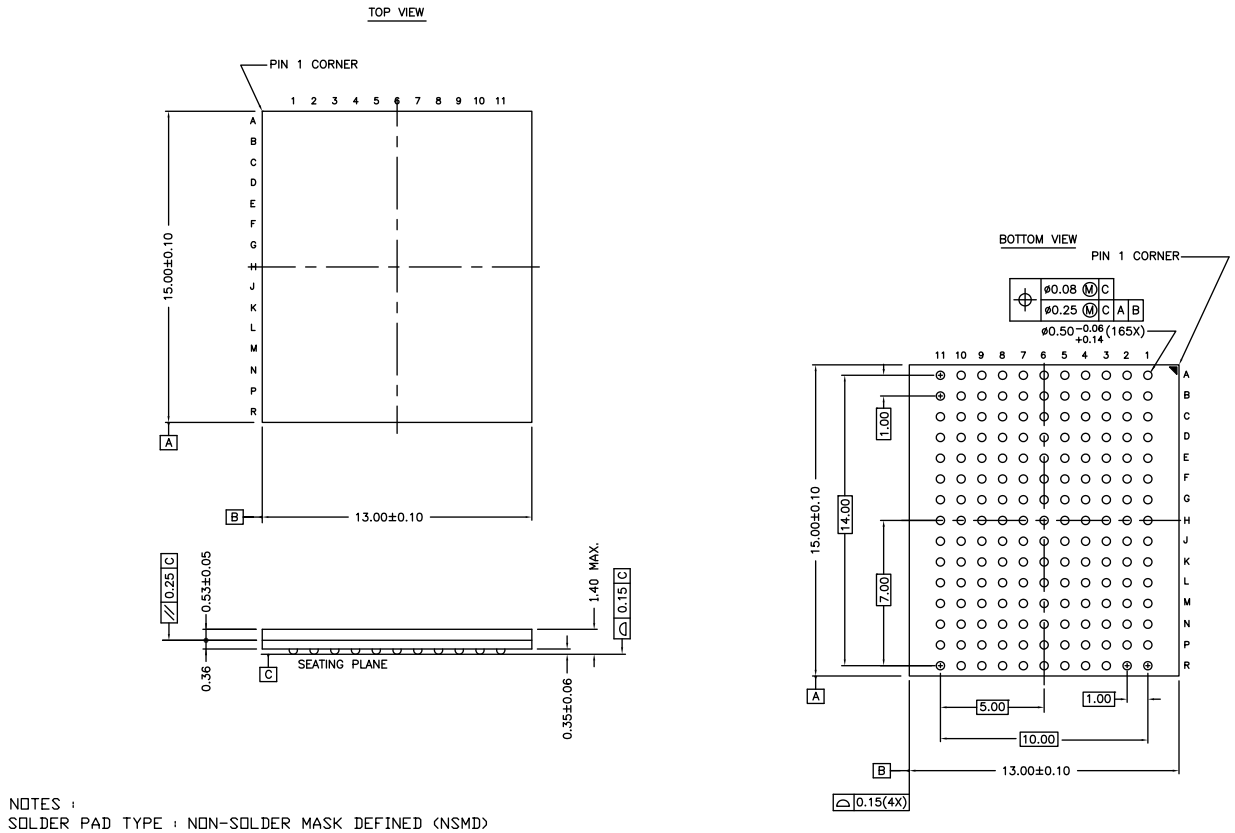


NOTE:
1. JEDEC STD REF MS-026
2. BODY LENGTH DIMENSION DOES NOT INCLUDE MOLD PROTRUSION/END FLASH
   MOLD PROTRUSION/END FLASH SHALL NOT EXCEED 0.0098 in (0.25 mm) PER SIDE
   BODY LENGTH DIMENSIONS ARE MAX PLASTIC BODY SIZE INCLUDING MOLD MISMATCH
3. DIMENSIONS IN MILLIMETERS

51-85050 *D

Package Diagrams *(continued)*

Figure 10. 165-ball FBGA (13 × 15 × 1.4 mm) BB165D/BW165D (0.5 Ball Diameter) Package Outline, 51-85180



NOTES :
SOLDER PAD TYPE : NON-SOLDER MASK DEFINED (NSMD)
JEDEC REFERENCE : MO-216 / ISSUE E
PACKAGE CODE : BB0AC/BW0AC
PACKAGE WEIGHT : SEE CYPRESS PACKAGE MATERIAL DECLARATION
DATASHEET (PMDD) POSTED ON THE CYPRESS WEB.

51-85180 *F

Acronyms

Acronym	Description
CMOS	Complementary Metal Oxide Semiconductor
FBGA	Fine-Pitch Ball Grid Array
I/O	Input/Output
JTAG	Joint Test Action Group
LSB	Least Significant Bit
MSB	Most Significant Bit
$\overline{OE}$	Output Enable
SRAM	Static Random Access Memory
TCK	Test Clock
TMS	Test Mode Select
TDI	Test Data-In
TDO	Test Data-Out
TQFP	Thin Quad Flat Pack
TTL	Transistor-Transistor Logic

Document Conventions

Units of Measure

Symbol	Unit of Measure
°C	degree Celsius
MHz	megahertz
µA	microampere
mA	milliampere
mm	millimeter
ms	millisecond
ns	nanosecond
Ω	ohm
%	percent
pF	picofarad
V	volt
W	watt

Appendix: Silicon Errata Document for RAM9 (90-nm), 18-Mb (CY7C138*D) Synchronous & NoBL™ SRAMs

This section describes the Ram9 Sync/NOBL ZZ pin, JTAG and Chip Enable issues. Details include trigger conditions, the devices affected, proposed workaround and silicon revision applicability. Please contact your local Cypress sales representative if you have further questions.

Part Numbers Affected

Density & Revision	Package Type	Operating Range
18Mb-Ram9 Synchronous SRAMs: CY7C138*D	All packages	Commercial/ Industrial

Product Status

All of the devices in the Ram9 4Mb/18Mb/72Mb Sync/NoBL family are qualified and available in production quantities.

Ram9 Sync/NoBL ZZ Pin, JTAG & Chip Enable Issues Errata Summary

The following table defines the errata applicable to available Ram9 18Mb Sync/NoBL family devices.

Item	Issues	Description	Device	Fix Status
1.	ZZ Pin	When asserted HIGH, the ZZ pin places device in a “sleep” condition with data integrity preserved.The ZZ pin currently does not have an internal pull-down resistor and hence cannot be left floating externally by the user during normal mode of operation.	18M-Ram9 (90nm)	For the 18M Ram9 (90 nm) devices, there is no plan to fix this issue.
2.	JTAG Functionality	During JTAG test mode, the Boundary scan circuitry does not perform as described in the datasheet.However, it is possible to perform the JTAG test with these devices in “BYPASS mode”.	18M-Ram9 (90nm)	This issue will be fixed in the new revision, which use the 65 nm technology. Please contact your local sales rep for availability.
3.	Chip Enable	The internal Chip Enable CE3# pad is floating instead of being tied to Ground. This floating input may cause unstable behavior of the device during normal mode of operation.	18M-Ram9 Synchronous SRAMs 119-ball BGA package option only (90nm)	This issue was fixed in the new revision of the device by a substrate change. Please contact your local sales rep for availability.

1. ZZ Pin Issue

- PROBLEM DEFINITION
  The problem occurs only when the device is operated in the normal mode with ZZ pin left floating. The ZZ pin on the SRAM device does not have an internal pull-down resistor. Switching noise in the system may cause the SRAM to recognize a HIGH on the ZZ input, which may cause the SRAM to enter sleep mode. This could result in incorrect or undesirable operation of the SRAM.

- TRIGGER CONDITIONS
  Device operated with ZZ pin left floating.

- SCOPE OF IMPACT
  When the ZZ pin is left floating, the device delivers incorrect data.

- WORKAROUND
  Tie the ZZ pin externally to ground.

- FIX STATUS
  Fix was done for the 72Mb RAM9 Synchronous SRAMs and 72M RAM9 NoBL SRAMs devices. Fixed devices have a new revision. The following table lists the devices affected and the new revision after the fix.

2. JTAG Functionality

- PROBLEM DEFINITION
  The problem occurs only when the device is operated in the JTAG test mode.During this mode, the JTAG circuitry can perform incorrectly by delivering the incorrect data or the incorrect scan chain length.

- TRIGGER CONDITIONS
  Several conditions can trigger this failure mode.
  1. The device can deliver an incorrect length scan chain when operating in JTAG mode.
  2. Some Byte Write inputs only recognize a logic HIGH level when in JTAG mode.
  3. Incorrect JTAG data can be read from the device when the ZZ input is tied HIGH during JTAG operation.

- SCOPE OF IMPACT
  The device fails for JTAG test. This does not impact the normal functionality of the device.

- WORKAROUND
  1.Perform JTAG testing with these devices in “BYPASS mode”.
  2.Do not use JTAG test.

3. Chip Enable Issue

- PROBLEM DEFINITION
  The die used for CY7C138*D has three Chip Enables, CE1#, CE2 and CE3#. The devices having part numbers CY7C138*D (with 119-ball BGA package option only) utilize a single Chip Enable (CE1#) signal. CE2 and CE3# signals which are unused should be internally connected to Vcc and Ground respectively to keep them in “enabled” state, thus allowing CE1# to have full control of the chip. The internal Chip Enable CE3# pad is floating instead of being tied to Ground. This state of CE3# signal can result in incorrect or undesirable operation of the SRAM.

- TRIGGER CONDITIONS
  There are no specific trigger conditions. The issue can occur at any time during the normal operation of the device.

- SCOPE OF IMPACT
  This issue affects the normal functionality, and can cause unstable operation of the device.

- WORKAROUND
  Use the fixed revision of the device.

- FIX STATUS
  Fix was done for all the devices having this issue and was involved re-design of the substrate in order to have CE2 and CE3# pads bonded to Vcc and Ground lines respectively in the substrate. Fixed devices have a new revision. The following table lists the devices affected and the new revision after the fix.

Table 1. List of Affected Devices and the new revision

Revision after the Fix	New Revision after the Fix
CY7C138*D (119-ball BGA package)	CY7C138*F (119-ball BGA package)

Document History Page

Document Title: CY7C1380D/CY7C1380F/CY7C1382D, 18-Mbit (512 K × 36/1 M × 18) Pipelined SRAM Document Number: 38-05543				
Rev.	**ECN No.**	**Submission Date**	**Orig. of Change**	**Description of Change**
**	254515	See ECN	RKF	New data sheet.
*A	288531	See ECN	SYT	Updated Selection Guide (Removed 225 MHz and 133 MHz frequencies related information). Updated IEEE 1149.1 Serial Boundary Scan (JTAG) (Edited description for non-compliance with 1149.1). Updated Electrical Characteristics (Removed 225 MHz and 133 MHz frequencies related information). Updated Switching Characteristics (Removed 225 MHz and 133 MHz frequencies related information). Updated Ordering Information (Added Pb-free information for 100-pin TQFP, 119-ball BGA and 165-ball FBGA packages) and added comment for 'Pb-free BG packages availability' below the Ordering Information.
*B	326078	See ECN	PCI	Updated Pin Configurations (Address expansion pins/balls in the pinouts for all packages are modified as per JEDEC standard). Updated IEEE 1149.1 Serial Boundary Scan (JTAG) (Updated TAP Instruction Set (Updated OVERVIEW (description), updated EXTEST (description), added EXTEST Output Bus Tri-State)). Updated Identification Register Definitions (Splitted Device Width (23:18) into two rows (one for 119-ball BGA and another for 165-ball FBGA), retained the same values of 165-ball FBGA and changed the values from 000000 to 101000 for 119-ball BGA) Updated Electrical Characteristics (Modified Test Conditions for V_{OL}, V_{OH} parameters). Updated Thermal Resistance (Changed Θ_{JA} and Θ_{JC} for 100-pin TQFP Package from 31 and 6 °C/W to 28.66 and 4.08 °C/W respectively, changed Θ_{JA} and Θ_{JC} for 119-ball BGA Package from 45 and 7 °C/W to 23.8 and 6.2 °C/W respectively, changed Θ_{JA} and Θ_{JC} for 165-ball FBGA Package from 46 and 3 °C/W to 20.7 and 4.0 °C/W respectively). Updated Ordering Information (Updated part numbers) and removed comment of 'Pb-free BG packages availability' below the Ordering Information.
*C	416321	See ECN	NXR	Changed status from Preliminary to Final. Changed address of Cypress Semiconductor Corporation from "3901 North First Street" to "198 Champion Court". Updated Electrical Characteristics (Changed the description of I_X parameter from Input Load Current to Input Leakage Current, changed the minimum and maximum values of I_X parameter (corresponding to Input Current of MODE) from –5 μA and 30 μA to –30 μA and 5 μA, changed the minimum and maximum values of I_X parameter (corresponding to Input current of ZZ) from –30 μA and 5 μA to –5 μA and 30 μA, updated Note 15). Updated Ordering Information (Updated part numbers) and replaced Package Name column with Package Diagram in the Ordering Information table.
*D	475009	See ECN	VKN	Updated TAP AC Switching Characteristics (Changed minimum values of t_{TH}, and t_{TL} parameters from 25 ns to 20 ns, and maximum value of t_{TDOV} parameter from 5 ns to 10 ns). Updated Maximum Ratings (Added the Maximum Rating for Supply Voltage on V_{DDQ} Relative to GND). Updated Ordering Information (Updated part numbers).

Document History Page *(continued)*

Document Title: CY7C1380D/CY7C1380F/CY7C1382D, 18-Mbit (512 K × 36/1 M × 18) Pipelined SRAM Document Number: 38-05543				
Rev.	**ECN No.**	**Submission Date**	**Orig. of Change**	**Description of Change**
*E	776456	See ECN	VKN	Updated Features (Included CY7C1380F/CY7C1382F related information). Updated Functional Description (Included CY7C1380F/CY7C1382F related information). Updated Logic Block Diagram – CY7C1380D/CY7C1380F (Included CY7C1380F related information, added the Note “CY7C1380F and CY7C1382F in 119-ball BGA package have only 1 chip enable ($\overline{CE}_1$).” and referred the same note in the title). Updated Logic Block Diagram – CY7C1382D/CY7C1382F (Included CY7C1382F related information, added the Note “CY7C1380F and CY7C1382F in 119-ball BGA package have only 1 chip enable ($\overline{CE}_1$).” and referred the same note in the title). Updated Pin Configurations (Included CY7C1380F/CY7C1382F related information). Updated Functional Overview (Included CY7C1380F/CY7C1382F related information). Updated Truth Table (Included CY7C1380F/CY7C1382F related information). Updated Truth Table for Read/Write (Included CY7C1380F related information). Updated Truth Table for Read/Write (Included CY7C1382F related information). Updated IEEE 1149.1 Serial Boundary Scan (JTAG) (Included CY7C1380F/CY7C1382F related information). Updated Identification Register Definitions (Included CY7C1380F/CY7C1382F related information). Updated Ordering Information (Updated part numbers).
*F	2648065	01/27/09	VKN / PYRS	Updated Ordering Information (To include CY7C1380F/CY7C1382F in 100-pin TSOP package and 165-ball FBGA package) and modified text on top of the Ordering information table.
*G	2897120	03/22/2010	NJY	Updated Ordering Information (Removed inactive parts). Updated Package Diagrams.
*H	3067398	10/20/10	NJY	Updated Ordering Information (The part CY7C1380F-167BGC is found to be in “EOL-Prune” state in Oracle PLM and therefore, it has been removed) and added Ordering Code Definitions.
*I	3159479	02/01/2011	NJY	Added Acronyms and Units of Measure. Minor edits and updated in new template. Updated Package Diagrams.
*J	3192403	03/10/2011	NJY	Updated in new template.
*K	3210400	03/30/11	NJY	Updated Ordering Information (Removed pruned part CY7C1380D-167BZC from the ordering information table).

Document History Page *(continued)*

Document Title: CY7C1380D/CY7C1380F/CY7C1382D, 18-Mbit (512 K × 36/1 M × 18) Pipelined SRAM Document Number: 38-05543				
Rev.	**ECN No.**	**Submission Date**	**Orig. of Change**	**Description of Change**
*L	3575733	04/09/2012	NJY / PRIT	Updated Features (Removed CY7C1382F related information, removed 165-ball FBGA package related information for CY7C1382D, removed 100-pin TQFP package related information for CY7C1380F, removed 119-ball BGA package related information). Updated Functional Description (Removed the Note “For best practices or recommendations, please refer to the Cypress application note AN1064, *SRAM System Design Guidelines* on www.cypress.com.” and its reference, removed the Note “$\overline{CE}_3$, CE_2 are for 100-pin TQFP and 165-ball FBGA packages only. 119-ball BGA is offered only in 1 chip enable.” and its reference). Updated Logic Block Diagram – CY7C1380D/CY7C1380F (Removed the Note “CY7C1380F and CY7C1382F in 119-ball BGA package have only 1 chip enable ($\overline{CE}_1$).” and its reference). Updated Logic Block Diagram – CY7C1382D (Removed CY7C1382F related information, removed the Note “CY7C1380F and CY7C1382F in 119-ball BGA package have only 1 chip enable ($\overline{CE}_1$).” and its reference). Updated Pin Configurations (Removed CY7C1382F related information, removed 119-ball BGA package related information, removed 100-pin TQFP package related information for CY7C1380F, removed 165-ball FBGA package related information for CY7C1382D, removed the Note “$\overline{CE}_3$, CE_2 are for 100-pin TQFP and 165-ball FBGA packages only. 119-ball BGA is offered only in 1 chip enable.” and its reference). Updated Functional Overview (Removed CY7C1382F related information). Updated Truth Table (Removed CY7C1382F related information). Updated Truth Table for Read/Write (Removed CY7C1382F related information). Updated IEEE 1149.1 Serial Boundary Scan (JTAG) (Removed CY7C1380D, CY7C1382D, and CY7C1382F related information). Updated Identification Register Definitions (Removed CY7C1380D, CY7C1382D, and CY7C1382F related information, removed 119-ball BGA package related information). Updated Scan Register Sizes (Removed 119-ball BGA package related information). Removed Boundary Scan Order (Corresponding to 119-ball BGA). Updated Capacitance (Removed 119-ball BGA package related information). Updated Thermal Resistance (Removed 119-ball BGA package related information). Updated Package Diagrams (Removed 119-ball BGA package related information).
*M	3945784	03/27/2013	PRIT	Updated Package Diagrams: spec 51-85180 – Changed revision from *E to *F.
*N	3977530	04/23/2013	PRIT	Added Appendix: Silicon Errata Document for RAM9 (90-nm), 18-Mb (CY7C138*D) Synchronous & NoBL™ SRAMs.

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