Using the UCD3138PFCEVM-026

User's Guide



Literature Number: SLUU885B March 2012-Revised July 2012



WARNING

Always follow TI's set-up and application instructions, including use of all interface components within their recommended electrical rated voltage and power limits. Always use electrical safety precautions to help ensure your personal safety and the safety of those working around you. Contact TI's Product Information Center http://support/ti./com for further information.

Save all warnings and instructions for future reference.

Failure to follow warnings and instructions may result in personal injury, property damage, or death due to electrical shock and/or burn hazards.

The term TI HV EVM refers to an electronic device typically provided as an open framed, unenclosed printed circuit board assembly. It is intended strictly for use in development laboratory environments, solely for qualified professional users having training, expertise, and knowledge of electrical safety risks in development and application of high-voltage electrical circuits. Any other use and/or application are strictly prohibited by Texas Instruments. If you are not suitably qualified, you should immediately stop from further use of the HV EVM.

1. Work Area Safety:

- (a) Keep work area clean and orderly.
- (b) Qualified observer(s) must be present anytime circuits are energized.
- (c) Effective barriers and signage must be present in the area where the TI HV EVM and its interface electronics are energized, indicating operation of accessible high voltages may be present, for the purpose of protecting inadvertent access.
- (d) All interface circuits, power supplies, evaluation modules, instruments, meters, scopes and other related apparatus used in a development environment exceeding 50 V_{RMS}/75 VDC must be electrically located within a protected Emergency Power Off (EPO) protected power strip.
- (e) Use a stable and non-conductive work surface.
- (f) Use adequately insulated clamps and wires to attach measurement probes and instruments. No freehand testing whenever possible.

2. Electrical Safety:

- (a) De-energize the TI HV EVM and all its inputs, outputs, and electrical loads before performing any electrical or other diagnostic measurements. Revalidate that TI HV EVM power has been safely deenergized.
- (b) With the EVM confirmed de-energized, proceed with required electrical circuit configurations, wiring, measurement equipment hook-ups and other application needs, while still assuming the EVM circuit and measuring instruments are electrically live.
- (c) Once EVM readiness is complete, energize the EVM as intended.

WARNING: while the EVM is energized, never touch the EVM or its electrical circuits as they could be at high voltages capable of causing electrical shock hazard.

3. Personal Safety:

(a) Wear personal protective equipment e.g. latex gloves and/or safety glasses with side shields or protect EVM in an adequate lucent plastic box with interlocks from accidental touch.

4. Limitation for Safe Use:

(a) EVMs are not to be used as all or part of a production unit.



Digitally Controlled Single-Phase PFC Pre-Regulator

1 Introduction

This EVM is to help evaluate the UCD3138 64-pin digital control device in off-line power converter application and then to aid its design. The EVM is a standalone Power Factor Correction (PFC) pre-regulator of single-phase AC input. The EVM UCD3138PFCEVM-026 is used together with its control card, UCD3138CC64EVM-030, also an EVM on which is placed UCD3138RGC.

The EVM of UCD3138PFCEVM-026 together with UCD3138CC64EVM-030 can be used as they are delivered without additional work, from either hardware or firmware, to evaluate PFC. The UCD3138PFCEVM-026 together with the UCD3138CC64EVM-030 can also be re-tuned on its design parameters through the operation of GUI, called <u>Texas Instruments Fusion Digital Power Designer</u>, or reloaded up with custom firmware with user's definition and development.

The EVM system is in topology of single-phase boost converter at its delivery on both hardware and firmware, but can be re-configured into two other PFC topologies: dual-phase interleaved, and bridgeless, then corresponding operation can be made by reloading with that associated firmware. All necessity of hardware and firmware for the two additional topologies are already developed and delivered with the shipment. Please contact Texas Instruments to obtain the instructions how to make re-configuration.

In the package delivered, three EVMs are included UCD3138PFCEVM-026, UCD3138CC64EVM-030, and USB-TO-GPIO. In the same package, also included is a hard copy of *Evaluation Module Electrical Safety Guideline*.

This user's guide provides basic evaluation instruction from a viewpoint of system operation in standalone PFC in its boost configuration.



Description

2 Description

UCD3138PFCEVM-026 together with UCD3138CC64EVM-030 is an EVM of PFC pre-regulator with digital control using UCD3138 device in boost converter topology and in the application of single-phase AC input. UCD3138 device is located on the board of UCD3138CC64EVM-030. UCD3138CC64EVM-030 is a daughter card and serves all PFC required control functions with preloaded single-phase boost PFC firmware. UCD3138PFCEVM-026 accepts universal AC line input from 90 V_{AC} to 264 V_{AC}, and outputs nominal 390 V_{DC} with full load output power 360 W, or full output current 0.92 A.

2.1 Typical Applications

- Single-Phase Universal AC Line Power Factor Correction Pre-Regulator
- Servers
- Telecommunication Systems

2.2 Features

- Digitally Controlled PFC Pre-Regulator
- Universal AC Line Input from 90 V_{AC} to 264 V_{AC} with AC Line Frequency 47 Hz to 63 Hz
- Regulated Output 390 V_{DC} with Output from No-Load to Full-Load
- Full-Load Power 360 W, or full-Load Current 0.92 A
- High Power Factor Close to 0.999 and Low THD Below 5% in Most Operation Conditions
- High Efficiency
- Protection:
 - Over Voltage
 - Over Current
 - Brownout
 - Power-On Inrush Current
- Test Points to Facilitate Device and Topology Evaluation
- Re-Configurable to Dual-Phase Interleaved PFC or Bridgeless PFC (please contact TI for detail)



Electrical Performance Specifications

www.ti.com

3 Electrical Performance Specifications

PARAMETER	TEST CONDITIONS	MIN	ТҮР	MAX	UNITS
Input Characteristics					
Voltage range		90		264	VAC
Line frequency		47		63	Hz
Input current, peak	Input = 90 VAC, 60 Hz, full load = 0.92 A		6.5	7.0	А
Input current, RMS	Input = 90 VAC, 60 Hz, full load = 0.92 A		4.5	5.5	
Input UVLO On	PFC function start (no load)	86		90	VAC
Input UVLO Off	PFC function stop (no load)	80		83	
Power factor	Half load		0.99		-
THD, input current	10% to 30% full load		10%		
	30% to 100% full load		5%		
Output Characteristics					
Output voltage, V _{OUT}	No load to full load		390		VDC
Output load current, I _{OUT}	90 VAC to 264 VAC			0.92	А
Output voltage ripple	Full load and 115 VAC, 60 Hz		13		Vpp
	Full load and 230 VAC, 50 Hz		15		
Output over current		0.95			А
Systems Characteristics					
Switching frequency	Normal operation		100		kHz
Peak efficiency	230 VAC, full load		96%		
Full load efficiency	115 VAC, full load		94%		
Operating temperature	Natural convection		25 °C		°C

Table 1. UCD3138PFCEVM-026 Electrical Performance Specifications

4 **Schematics**

AC_L_PFC

AC NEU

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R20 200k R15 R15 R15 R15 C00k

C38

C37 7 0.47uF

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C6

2mH SmH

C2 17nF C3 47nF

L4 7.80uH

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F2

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5



A Parts not used

to 63Hz

Vac (47

£§

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Copper fill for

LN1371GTR

D19

+12V_EXT

4.7k

R19 4.7

(J3-13)

4.7k

²²

(J3-25) LED 2) (J3-26)

R75 -Þ

[∃] ↓ ↑ ↑

Figure 1. UCD3138PFCEVM-026 Schematic

DB-1

BUS+



Schematics





5 Test Setup

5.1 Test Equipment

AC Voltage Source:capable of single-phase output AC voltage 85 V_{AC} to 265 V_{AC} , 47 Hz to 63 Hz, adjustable, with minimum power rating 400 W, the AC voltage source to be used should meet IEC60950 reinforced insulation requirement.

DC Multimeter: capable of 0-V to 500-V input range, four digits display preferred.

Output Load: DC load capable of 400 V_{DC} or greater, 1 A or greater, and 400 W or greater, with display such as load current and load power.

Oscilloscope: capable of 500-MHz full bandwidth, digital or analog, if digital 5 Gs/s or better.

Current probe: capable of 0 A to 10 A, 100-MHz or greater full bandwidth, AC coupling.

Fan: 200 LFM to 400 LFM forced air cooling is recommended, but not a must.

Recommended Wire Gauge: capable of 4-A RMS, or better than #16 AWG, with the total length of wire less than 8 feet (4 feet input and 4 feet return).

5.2 Recommended Test Setup



Figure 3. UCD3138PFCEVM-026 Recommended Test Setup





Figure 4. EVM Orientation of UCD3138PFCEVM-030 on the UCD3138PFCEVM-026

6 List of Test Points

TEST POINTS	NAME	DESCRIPTION
TP1	T1OUT	UART0 (J9-2) T1OUT
TP2	R1IN	UART0 (J9-3) R1IN
TP3	DGND	Digital GND of J3 connection
TP4	+3_3V	3.3-V LDO output on board from 12 V
TP5	RC-PWM-0A	DPWM0A RC filter
TP6	CT_2	Second phase current sensing signal
TP7	AC_N	Input voltage sensing signal of Neutral wire
TP8	DGND	Digital GND and same as TP3
TP9	VAUX_S	Secondary side 12 V on board. Not used, but can be used for external circuit.
TP10	VAUX_P	12-V output on board from DB-1, UCC28600EVM400V-12V
TP11	+12V_EXT	12 V on board from VAUX_P
TP12	K1	Relay K1 coil
TP14	AC_L	Input sensing signal of Line wire
TP15	VBUS_SENSE	PFC output voltage sensing signal
TP16	GND	Analog GND
TP17	BUS-	PFC output return
TP18	REC-1	Rectifier positive output
TP19	CT-1	Current sensing signal from current transformer T1
TP20	ISENSE	Current sensing signal after conditioning
TP21	REC-2	Rectifier return
TP22	BUS+	PFC output positive, nominal 390VDC
TP23	SW2	Q2 Drain pin
TP24	SW1	Q3 Drain pin
TP25	Q2-Gate	Gate pin of Q2 MOSFET
TP26	Q3-Gate	Gate pin of Q3 MOSFET

Table 2. List of Test Points

7 List of Terminals

Table 3. List of Terminals

TERMINAL	NAME	DESCRIPTION			
J1	Line	Board AC input line, single-pin connection – screw type, J1 and J2 are AC input terminals, rated up to 264 V_{AC} and maximum 7.5 A, 47 Hz to 63 Hz.			
J2	Neutral	Board AC input neutral, single-pin connection – screw type			
J3	DJ	Digital signal connection, 40 pins			
J4	AJ	Analog signal connection, 40 pins			
J5	BUS+	PFC output positive connection, single-pin connection – screw type, BUS+ and BUS- are D output terminals, rated maximum 400 V_{DC} , and maximum current 1 A.			
J6	BUS-	PFC output return, single-pin connection – screw type			
J7	12V_Sec	12-V auxiliary to supply to external circuit on the secondary side, 2 pins			
J8	UART1	Isolated and communication to DC converter, not production tested, 6 pins			
J9	UART0	Non-isolated connection, standard RS232, 9 pins,			
J10	Sync	External 12-V bias and sync signal, 3 pins			
J11	Chassis	Chassis ground, or earth connection, single-pin connection – screw type			



8 Test Procedure

8.1 Efficiency Measurement Procedure

- 1. Refer to Figure 3 for basic setup to measure power conversion efficiency. The required equipment to do this measurement is listed in Section 5.1.
- 2. Before making electrical connections, visually check the boards to make sure there are no suspected spots of damages.
- In this EVM package, three EVMs are included, UCD3138PFCEVM-026, UCD3138CC64EVM-030, and USB-TO-GPIO. In this measurement, the board of UCD3138PFCEVM-026 and UCD3138CC64EVM-030 is needed.
- 4. First install the board of UCD3138CC64EVM-030 onto the board of UCD3138PFCEVM-026. Care must be given to the alignment and the orientation of two boards, or damage may occur. Refer to Figure 4 for UCD3138CC64EVM-030 board orientation.
- Connect the AC voltage source to J1 (Line) and J2 (Neutral). The AC voltage source should be an isolated one and meet IEC60950 requirement. Set up the AC output voltage in the range specified in Table 1, between 90 V_{AC} and 264 V_{AC}, between 47 Hz and 63 Hz; set up the AC source current limit to 7.5-A peak and RMS, respectively.
- 6. Connect an electronic load with either constant current mode or constant resistance mode. The load range is from 0 A to 0.92 A. Initial power on is recommended with 0-A load current. The load is required to receive 0 V_{DC} to 500 V_{DC} .
- 7. If the load does not have a current or a power display, a current meter is needed to insert into between the load and the board.
- 8. Connect a volt-meter across the load and set up the volt-meter scale 0 V to 500 V on its voltage, DC.
- 9. Turn on the AC voltage output and varying the load. Then the measurement can be made.



Do not leave EVM powered when unattended!

8.2 Equipment Shutdown

- 1. Shut down AC voltage source.
- 2. Shut down electronic load.

9 Performance Data and Typical Characteristic Curves

Figure 5 through Figure 18 present typical performance curves for UCD3138PFCEVM-026.

9.1 Efficiency



Figure 5. UCD3138PFCEVM-026 Efficiency

9.2 Power Factor



Figure 6. UCD3138PFCEVM-026 Power Factor



9.3 Input Current at 115 V_{AC} and 60 Hz



Figure 7. Input Current and Voltage 115 $V_{\mbox{\scriptsize AC}}$ and Half Load



Figure 8. Input Current and Voltage 115 V_{AC} and Full Load



Performance Data and Typical Characteristic Curves

9.4 Input Current at 230 V_{AC} and 50 Hz



Figure 9. Input Current and Voltage 230 $V_{\mbox{\scriptsize AC}}$ and Half Load



Figure 10. Input Current and Voltage 230 $\rm V_{AC}$ and Full Load



9.5 Output Voltage Ripple



Figure 11. Output Voltage Ripple 115 V_{AC} and Full Load



Figure 12. Output Voltage Ripple 230 V_{AC} and Full Load



Performance Data and Typical Characteristic Curves

9.6 Output Turn On



Figure 13. Output Turn On 115 $\rm V_{AC}$ and No Load



Figure 14. Output Turn On 115 $V_{\mbox{\scriptsize AC}}$ and Full Load



9.7 Total Harmonic Distortion (THD)



Figure 15. UCD3138PFCEVM-026 Input Current THD

9.8 Other Waveforms



Figure 16. UCD3138PFCEVM-026 Sensing Signal AC_L (TP14) or AC_N (TP7)



Performance Data and Typical Characteristic Curves



Figure 17. UCD3138PFCEVM-026 Sensing Signal I_{SENSE} (TP20)



Figure 18. UCD3138PFCEVM-026 MOSFET V_{GS} (top) and V_{DS}



10 EVM Assembly Drawing and PCB Layout

The following figures (Figure 19 through Figure 24) show the design of the UCD3138PFCEVM-026 printed circuit board. PCB dimensions: L x W = 9.0 inch x 6.0 inch, PCB material: FR4 or compatible, four layers and 2-oz copper on each layer.



Figure 19. UCD3138PFCEVM-026 Top Layer Assembly Drawing (top view)



Figure 20. UCD3138PFCEVM-026 Bottom Assembly Drawing (bottom view)



EVM Assembly Drawing and PCB Layout



Figure 21. UCD3138PFCEVM-026 Top Copper (top view)



Figure 22. UCD3138PFCEVM-026 Internal Layer 1 (top view)





Figure 23. UCD3138PFCEVM-026 Internal Layer 2 (top view)



Figure 24. UCD3138PFCEVM-026 Bottom Copper (top view)

List of Materials

11 List of Materials

The List of Materials is Based on Figure 1 and Figure 2.

QTY	REF DES	DESCRIPTION	PART NUMBER	MFR
1	C1	Capacitor, tantalum, 25 V, 20%, 10 µF, 3528	TPSB106M025R180 0	AVX
0	C10, C11	Capacitor, ceramic, 50 V, X7R, 10%, open, 1206	Std	Std
2	C12, C20	Capacitor, ceramic, 50 V, X7R, 10%, 1 nF, 0805	Std	Std
1	C16	Capacitor, ceramic, 50 V, X7R, 10%, 0.01 µF, 0805	Std	Std
0	C17, C25, C29	Capacitor, ceramic, 50 V, X7R, 10%, open, 0805	Std	Std
2	C2, C3	Capacitor, metalized polyester, 250 VAC, ±20%, 47 nF, 0.472 inch x 0.925 inch	ECQ-U2A473MV	Panasonic
1	C21	Capacitor, tantalum, 10 V, 20%, 10 µF, 3216	TAJA106M010RNJ	AVX
1	C22	Capacitor, film, 300 VAC, ±20%, 47 nF, 0.236 inch x 0.591 inch	ECQ-U3A473MG	Panasonic
1	C26	Capacitor, ceramic, 50 V, X7R, 10%, 1 µF, 0805	Std	Std
1	C30	Capacitor, ceramic, 50 V, X7R, 10%, 330 pF, 0805	Std	Std
1	C31	Capacitor, tantalum chip, 16 V, 47 µF, 0.281 inch x 0.126 inch	595D476X9016C2T	Vishay
1	C32	Capacitor, ceramic, 50 V, NP0, 5%, 150 pF, 0805	Std	Std
4	C33, C39, C40, C41	Capacitor, polyester, 630 V, 10%, 47 nF, 0.256 inch x 0.650 inch	ECQ-E6473KF	Panasonic
1	C34	Capacitor, aluminum electrolytic, 450 VDC, -40°C to 85°C, ±20%, 220 μF, 0.984 inch diameter	ECOS2WP221CX	Panasonic
2	C35, C36	Capacitor, ceramic, 50 V, X7R, 10%, 100 pF, 0603	Std	Std
2	C37, C38	Capacitor, film, 275 VAC, ±20%, 0.47 µF, 0.236 inch x 0.591 inch	ECQU2A474ML	Panasonic
7	C4, C18, C19, C23, C24, C27, C28	Capacitor, ceramic, 50 V, X7R, 10%, 0.1 µF, 0805	Std	Std
3	C5, C6, C7	Capacitor, metalized polyester, 250 VAC, ±20%, 4.7 nF, 0.295 inch x 0.730 inch	BFC233820472	Vishay
5	C8, C9, C13, C14, C15	Capacitor, ceramic, 50 V, X7R, 10%, 0.1 µF, 0603	Std	TDK
9	D1, D2, D3, D4, D6, D15, D22, D23, D25	Diode, dual Schottky, 200 mA, 30 V, SOT23	BAT54S	Zetex
2	D11, D12, D24	Diode, Schottky, 500 mA, 30 V, SOD123	MBR0530T1G	On Semi
2	D13, D14	Diode, Schottky rectifier, 10 A, 600 V, TO-263-2	C3D10060G	CREE
1	D16	Diode, 600 V, 6 A, 400 A peak surge, P600	6A6-T	Diodes
1	D17	Diode, bridge rectifier, 8 A, 600 V, 0.880 inch x 0.140 inch	GBU8J	Fairchild
1	D18	Diode, LED, green, 2.1 V, 20 mA, 6 mcd, 0603	LTST-C190GKT	Lite On
1	D19	Diode, LED, green, 2.1 V, 20 mA, 0.9 mcd, 0.068 inch x 0.049 inch	LN1371GTR	Panasonic
1	D20	Diode, LED, red, 2.1 V, 20 mA, 6 mcd, 0603	LTST-C190CKT	Lite On
1	D21	Diode, LED, yellow, 2.1 V, 20 mA, 6 mcd, 0603	LTST-C190YKT	Lite On
1	D5	Diode, signal, 300 mA, 75 V, 350 mW, SOD-123	1N4148W-TP	MICROSEMI
1	D7	Diode, ultrafast rectifier, 1 A, 200 V, SMB	MURS160T3G	On Semi
1	D8	Diode, dual Schottky, 200 mA, 30 V, SOT-23	BAT54C	Fairchild
2	D9, D10	Diode, Schottky, 500 mA, 60 V, SOT-23	ZHCS506	Zetex
1	DB-1	Module, 5 W, auxiliary bias PS, PCB assembly, 1.200 inch x 2.200 inch	PWR050	ТІ
1	DB-2	Control card, UCD3138 control card, PCB assembly, 3.400 inch x 1.800 inch	UCD3138CCEVM- 030	ТІ

Table 4. UCD3138PFCEVM-026 List of Materials

QTY	REF DES	DESCRIPTION	PART NUMBER	MFR
1	F1	Fuse, 250 VAC, SLO-BLO, 3 AG, 7-A cart, 0.250 inch x 1.250 inch	0313007.HXP	Littlefuse
1	F2	Ffuse holder, 1/4 inch, board mount, 1.54 inch x 0.30 inch	BK/1A3398-07	Bussmann
1	HS1	Heatsink, TO-220, vertical mount, 15 x C/W, 0.5 inch x 0.95 inch	593002B00000G	Aavid
2	HS2, HS3	Heatsink, TO-220, vertical mount, 5 x C/W, 0.5 inch x 1.38 inch	513201	Aavid
5	J1, J2, J5, J6, J11	Terminal block, 2 pin, 15 A, 5.1 mm, 0.40 inch x 0.35 inch	ED120/2DS	OST
1	J10	Header, male 3 pin, 100-mil spacing, 0.100 inch x 3 inch	PEC03SAAN	Sullins
2	J3, J4	Header, 40 pin, 2 mm pitch, 4.00 mm x 40.00 mm	87758-4016	Molex
1	J7	Terminal block, 2 pin, 6 A, 3.5 mm, 0.27 inch x 0.25 inch	ED555/2DS	OST
1	J8	Header, male 2 x 3 pin, 100-mil spacing, 0.20 inch x 0.30 inch	PEC03DAAN	Sullins
1	J9	Connector, 9-pin D, right angle, female, 1.213 inch x 0.510 inch	182-009-213R171	Norcomp
1	JMP1	Jumper, 0.400 inch length, bare, solid, bus-bar wire, AWG 16, 0.051 inch	295 SV005	ALPHA WIRE
1	K1	Relay, SPDT, 10-A miniature, 12-V coil, 0.630 inch x 0.870 inch	T7NS5D1-12	Тусо
2	L1, L2	Inductor, toroid, 327 $\mu H,$ vertical THT, 327 $\mu H,$ 0.866 inch x 1.380 inch	7804-09-0014	Nova Magnetics
2	L3, L4	Inductor, toroid, 7.8 μH at 0 A and 3.22 μH at 20.5 A, 7.80 $\mu H,$ 0.874 inch x 0.374 inch	PA0431L	Pulse
1	L5	IND, common mode emi suppression, 7.5 A, 2 mH at 1 kHz, 2 mH, 0.800 inch x 1.440 inch	PE-62917	Pulse
3	Q1, Q4, Q5	MOSFET, N-channel, 60 V, 115 mA, 1.2 Ω, SOT23	2N7002	Fairchild
2	Q2, Q3	MOSFET, N-channel, 650 V, 9 A, 199 mΩ, TO-220V	IPP60R199CP	Infineon
3	Q6, Q7, Q8	Bipolar, NPN, 40 V, 200 mA, 200 mW, SC-75	MMBT3904TT1G	On Semi
0	R1, R24, R40, R43, R68	Resistor, chip, 1/10 W, 1%, open, 0805	Std	Std
6	R13, R15, R27, R28, R29, R30	Resistor, chip, 1/4 W, 1%, 200 kΩ, 1210	Std	Std
2	R14, R16	Resistor, chip, 1/4 W, 1%, 3.83 kΩ, 1210	Std	Std
4	R19, R20, R21, R22	Resistor, chip, 1/10 W, 1%, 4.7 kΩ, 0805	Std	Std
1	R2	Resistor, chip, 1/10 W, 1%, 3.3 MΩ, 0805	Std	Std
1	R23	Resistor, chip, 1/10 W, 1%, 3.3 kΩ, 0805	Std	Std
1	R3	Resistor, wire-wound, 5 W, 5%, 50 Ω , 1.000 inch x 0.276 inch	25J50RE	Ohmite
2	R31, R72	Resistor, chip, 1/4 W, 1%, 1.5 kΩ, 1210	Std	Std
9	R32, R41, R44, R49, R52, R54, R75, R76, R77	Resistor, chip, 1/10 W, 1%, 0 Ω, 0805	Std	Std
2	R33, R35	Resistor, chip, 1/4 W, 1%, 0 Ω, 1210	Std	Std
0	R34, R36	Resistor, chip, 1/4 W, 1%, open, 1210	Std	Std

Table 4. UCD3138PFCEVM-026 List of Materials (continued)



List of Materials

QTY	REF DES	DESCRIPTION	PART NUMBER	MFR
7	R37, R38, R56, R57, R70, R73, R74	Resistor, chip, 1/10 W, 1%, 10 kΩ, 0805	Std	Std
2	R39, R58	Resistor, chip, 1/10 W, 1%, 2 kΩ, 0805	Std	Std
1	R4	Resistor, chip, 1/10 W, 1%, 5.01 kΩ, 0805	Std	Std
2	R45, R79	Resistor, chip, 1/10 W, 1%, 100 Ω, 0805	Std	Std
3	R47, R48, R50	Resistor, chip, 1/10 W, 1%, 1.8 kΩ, 0805	Std	Std
7	R5, R8, R42, R61, R80, R81, R82	Resistor, chip, 1/10 W, 1%, 1 kΩ, 0805	Std	Std
2	R53, R55	Resistor, chip, 1/10 W, 1%, 5.23 Ω, 0805	Std	std
2	R59, R60	Resistor, chip, 1/10 W, 1%, 49.9 kΩ, 0805	Std	Std
2	R6, R7	Resistor, metal strip, 2 W, 1%, 0.02 Ω , 0.49 inch x 0.10 inch	WSR2R0200FEA	Vishay Dale
2	R63, R66	Resistor, chip, 1/10 W, 1%, 15 Ω, 0805	Std	Std
2	R64, R65	Resistor, chip, 1/10 W, 1%, 10 kΩ, 1206	Std	std
1	R69	Resistor, chip, 1/10 W, 1%, 1.6 kΩ, 0805	Std	Std
1	R71	Resistor, chip, 1/10 W, 1%, 910 Ω, 0805	Std	Std
1	R78	Resistor, chip, 1/10 W, 1%, 1.1 kΩ, 0805	Std	Std
12	R9, R10, R11, R12, R17, R18, R25, R26, R46, R51, R62, R67	Resistor, metal film, 1/4 W, ±5%, 100 kΩ, 1206	RC1206FR- 07100KL	Yageo
2	U1, U3	High Voltage, High Current Op-Amp, MSOP-8	OPA350EA/250	ТΙ
1	U2	RS-232 Transceivers with Auto Shutdown, SSOP-16	SN75C3221DBR	ТІ
1	U4	High-Speed Low-Side Power MOSFET driver, SO8	UCC27324D	ТΙ
0	U5, U6	4-A Single Channel High-Speed Low-Side Gate Drivers, open, SOT23-6	UCC27517DBV	ТІ
1	U7	3.3-V, 800-mA LDO Voltage Regulators, SOT-223	TLV1117-33IDCY	ТІ
1	U8	Digital Isolators, xx Mbps, SO-8	ISO7221CD	ТІ
1	U9	Opto-coupler, SMD-4P	SFH6156-2	Vishay

Table 4. UCD3138PFCEVM-026 List of Mate	erials (continued)
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12 Digital PFC Description

12.1 1PFC Block Diagram

12.1.1 Single-Phase PFC Block Diagram

Single-phase PFC function block diagram is shown in Figure 25. The digital controlled single-phase PFC has the same power stage as those seen in other analog controlled devices. The main difference is the line voltage is sensed then rectified inside the UCD3138 digital controller. All signals interact with UCD3138 and explained in section Section 12.2.



Figure 25. Digitally Controlled Single-Phase PFC System Block Diagram



12.1.2 2-Phase PFC Block Diagram

A functional block diagram of a 2-phase interleaved PFC is shown in Figure 26. The digital controlled 2-phase interleaved PFC has the same power stage seen in other analog controlled devices. All signals interact with UCD3138 and are explained in section 12.2.



Figure 26. Digitally Controlled 2-Phase PFC System Block Diagram

12.1.3 Bridgeless PFC Block Diagram

A function block diagram of a bridgeless PFC is shown in Figure 27. The digital controlled bridgeless PFC has a same power stage as those seen in analog controlled. All signals interacted with UCD3138 are explained in the section Section 12.2.



Figure 27. Digitally Controlled Bridgeless PFC System Block Diagram



12.2 UCD3138 Pin Definition

In this EVM, the PFC DC bus voltage feedback loop control is implemented using firmware execution by the ARM7 microcontroller, while the high-speed current loop control is implemented in the digital power peripherals in the UCD3138. The DC bus voltage, AC line and AC neutral voltages are sensed using the general purpose ADC in the ARM block. This is executed while the current signal is sensed and processed using the Front-End (EADC) block in the digital power peripherals. All protection functions such as cycle-by-cycle current limiting and overvoltage protection are implemented using the high-speed analog comparators available in the UCD3138.

12.2.1 UCD3138 Pin Definition in Single-Phase PFC

UCD3138 is a 64-pin device. When using the UCD3138 as a single-phase PFC controller, the pins used are defined in Figure 28.



Figure 28. Definition of UCD3138 in Single-Phase PFC Control

12.2.2 UCD3138 Pin Definition in 2-Phase PFC

UCD3138 pin definition in 2-phase interleaved PFC control, shown in Figure 29.



Figure 29. Definition of UCD3138 in 2-Phase PFC Control

12.2.3 UCD3138 Pin Definition in Bridgeless PFC

UCD3138 pin definition shown in bridgeless PFC control, see Figure 30.







12.3 EVM Hardware – Introduction

12.3.1 PFC Pre-Regulator Input

The power entry section, PFC pre-regulator input, as shown in Figure 31, consists of EMI input filter, AC voltage sense circuit and inrush relay control circuit. The series resistor R3 limits the inrush current. The inrush control relay K1, controlled by the UCD3138 controller, is used to bypass this resistor. The controller measures input and output voltages and decides the appropriate time for closure of this relay. Input AC voltage is scaled and conditioned, and the sensed signal is applied to the UCD3138 ADC input AD_07 and AD_08. Figure 31 also shows a DC voltage regulator D3, which converts the 12 V into 3.3 V to provide the bias for on-board 3.3 V.



Figure 31. AC Power Filtering, Inrush Current Limit and AC Voltage Sense



Digital PFC Description

12.3.2 PFC Power Stage

The PFC power stage shown in Figure 32 employs a 2-phase boost PFC topology, even though the default configuration of the EVM is single phase PFC. The power MOSFETs, Q3 and Q4, are driven by the controller's DPWM signals, DPWM1B and DPWM2B, through UCC27324 MOSFET gate drive device. The schematic also shows that four additional signals are sensed and eventually connected to UCD3138 controller's 12-bit ADC input pins. These four signals are the rectified AC line and neutral voltage, the DC bus voltage for voltage loop control, redundant OVP protection and input current. The sensed signals are scaled and conditioned to a range of 0 V to 2.5 V which corresponds to the full scale range of the ADC.

For single-phase PFC and 2-phase interleaved PFC, the PFC stage total input current is differentially sensed across the sense resistors, R6 and R7, and then conditioned by the current sense amplifier U1. This is shown in Figure 32. This sensed input current signal is scaled and conditioned to a range of 0 V to 1.6 V corresponding to the range of the on-chip DAC associated with the error ADC0 (EADC0).

In DCM mode, the inductor current oscillates between the inductor and switch node equivalent capacitor. As a result, the inductor current goes to negative, but the negative current will not show up at the output of the current amplifier. Therefore, the amplifier output does not represent the total inductor current. In order to sense this negative current, an offset is added to the amplifier's positive input terminal, this is shown as R113 in Figure 32.

For bridgeless PFC, the PFC stage input current is sensed by current transformer T2 and T3. The output signal of T2 and T3 is rectified, scaled and conditioned to a range of 0 V to 1.6 V corresponding to the range of the on-chip DAC associated with the error ADC1 (EADC1) and error ADC2 (EADC2).





Figure 32. PFC Power Stage

12.3.3 Non-Isolated UART Interface

The non-isolated UART interface shown in Figure 33 is used to control the PFC module from the host PC over the serial port. It is also used to monitor some of the parameters, debug and test firmware functions.



Figure 33. Non-Isolated PFC Module to Host PC Interface



12.3.4 Isolated UART Interface

The isolated UART interface shown in Figure 34 is used to communicate with another digital controller, for example one used in a secondary referenced isolated DC-to-DC converter application.



Figure 34. Isolated UART and AC_DROP Signal Interface

12.3.5 Interface Connector of Control Card

The interface connector between the PFC board and the UCD3138 controller board is shown in Figure 35.



Figure 35. UCD3138 Controller Board and PFC Board Signal Interface Connector Diagram



12.3.6 UCD3138 Resource Allocation for PFC Control

HEADER PIN NUMBER	UCD3138 CONTROL CARD PIN NAME	DESCRIPTION			
J3-1	DPWM_0A	RC filter for debug monitoring			
J3-2	DPWM_0B	Not used			
J3-3	DPWM_1A	Not used(available as an option for PFC PWM1)			
J3-4	DPWM_1B	PFC PWM1			
J3-5	DPWM_2A	Not used(available as an option for PFC PWM2)			
J3-6	DPWM_2B	PFC PWM2			
J3-7	DPWM_3A	PFC ZVS control			
J3-8	DPWM_3B	AC drop indicator signal			
J3-9	DGND	Digital ground GND1			
J3-10	DGND	Digital ground GND1			
J3-11	FAULT-0	Inrush relay control			
J3-12	Not used	Not used			
J3-13	FAULT-1	LED 1			
J3-14	Not used	Not used			
J3-15	SYNC	Sync input signal for PFC stage			
J3-16	Not used	Not used			
J3-17	FAULT-2	Not used			
J3-18	Not used	Not used			
J3-19	Not used	Not used			
J3-20	Not used	Not used			
J3-21	Not used	Not used			
J3-22	FAULT-3	Not used			
J3-23	SCI_TX1	SCI_TX1			
J3-24	SCI_RX1	SCI_RX1			
J3-25	PWM0	LED 2			
J3-26	PWM1	LED 3			
J3-27	Not used	Not used			
J3-28	Not used	Not used			
J3-29	TCAP	Not used			
J3-30	Not used	Not used			
J3-31	SCI TX0	SCI TX0			
J3-32	SCI TX0	SCI RX0			
J3-33	INT-EXT	Not used			
J3-34	EXT-TRIG	Not used			
J3-35	DGND	Not used			
J3-36	RESET*	Not used			
J3-37	DGND	Digital ground GND1			
J3-38	DGND	Digital ground GND1			
J3-39	+12V_EXT	External +12V DC supply			
J3-40	3.3VD	Not used			
J4-01	AGND	Analog ground GND2			
J4-02	Not used	Not used			
J4-03	AGND	Analog ground GND2			
J4-04	AD_00	PMBus address			
J4-05	AGND	Analog ground GND2			

Table 5. J3 and J4 Pin Assignment

HEADER PIN NUMBER	UCD3138 CONTROL CARD PIN NAME	DESCRIPTION			
J4-06	AD_01	IPM			
J4-07	AGND	Analog ground GND2			
J4-08	AD_02	PFC input current sense			
J4-09	AGND	Analog ground GND2			
J4-10	AD_03	PFC BUS voltage sense			
J4-11	AGND	Analog ground GND2			
J4-12	AD_04	PFC MOSFET Q3 current sense			
J4-13	AGND	Analog ground GND2			
J4-14	AD_05	Not used			
J4-15	AGND	Analog ground GND2			
J4-16	AD_06	PFC BUS voltage sense(for OVP)			
J4-17	AGND	Analog ground GND2			
J4-18	AD_07	PFC Vin line voltage sense			
J4-19	AGND	Analog ground GND2			
J4-20	AD_08	PFC Vin neutral voltage sense			
J4-21	AGND	Analog ground GND2			
J4-22	AD_09	Not used			
J4-23	AGND	Analog ground GND2			
J4-24	AD_10	Not used			
J4-25	AGND	Analog ground GND2			
J4-26	AD_11	Not used			
J4-27	AGND	Analog ground GND2			
J4-28	AD_12	Not used			
J4-29	AGND	Analog ground GND2			
J4-30	AD_13	PFC MOSFET Q4 current sense			
J4-31	AGND	Analog ground GND2			
J4-32	Not used	Not used			
J4-33	Not used	Not used			
J4-34	Not used	Not used			
J4-35	EAN2	Analog ground GND2			
J4-36	EAP2	PFC MOSFET Q4 current sense			
J4-37	EAN1	Analog ground GND2			
J4-38	EAP1	PFC MOSFET Q3 current sense			
J4-39	EAN0	Analog ground GND2			
J4-40	EAP0	PFC Input current sense			

Table 5. J3 and J4 Pin Assignment (continued)



12.4 EVM Firmware – Introduction

The referenced firmware provided with the EVM is intended to demonstrate basic PFC functionality, as well as some basic PMBus communication and primary and secondary communication. A brief introduction to the firmware is provided in this section.

There are three timing levels in the current version of the firmware, as shown in Figure 36:

- 1. Fast Interrupt (FIQ)
- 2. Standard Interrupt (IRQ)
- 3. Background



Figure 36. Firmware Structure Overview

Almost all firmware tasks occur during the standard interrupt. The only exceptions are the serial interface and PMBus tasks, which occur in the background, and the Over Voltage Protection (OVP), which is handled by the FIQ.

For more details, please refer to the source code and training material.



Digital PFC Description

12.4.1 Background Loop

The firmware starts from function main(). In this function, after the system initialization, it goes to an infinite loop. All the non-time critical tasks are put in this loop, it includes:

- Calculate voltage feed forward.
- Clear current offset at zero load.
- System monitoring.
- PMBus communication.
- Primary and secondary UART communication.

NOTE: User can always add any non-time critical functions in this loop.

12.4.2 Voltage Loop Configuration

The voltage control loop is a pure firmware loop. V_{OUT} is sensed by a 12-bit ADC, and compared with voltage reference. The error goes into a firmware Proportional-Integral (PI) controller, and its output is used to do current loop reference calculations.

12.4.3 Current Loop Configuration

Current loop consists of several modules:

- Front End (FE) Module, to configure the AFE block gain.
 - For single phase PFC, AFE0 is used.
- Filter Module, to configure the current loop compensation.
 - FILTER1 is used.
- DPWM Module, to generate the PWM signal driving PFC.
 - For single phase PFC, DPWM1B is used.

NOTE: Loop Mux Module, to configure interconnection among front end, filter and DPWM modules.

12.4.4 Interrupts

There are two interrupts, the Standard Interrupt (IRQ), and the Fast Interrupt (FIQ).

- IRQ contains the state machine and most of the PFC control firmware.
- FIQ is used in relation to implementing OVP protections.



12.5 State Machine

The PFC hiccups once an over-voltage condition is detected. Only very serious over voltage causes PFC shut down and latch.

Digital PFC Description

Figure 37 is the PFC state machine diagram shown below.



Figure 37. PFC State Machine

12.6 PFC Control Firmware

The PFC Control Firmware is almost all implemented in the IRQ function, which includes:

- ADC measurement
- State machine
- V_{RMS} calculation
- Voltage loop calculation
- Current reference calculation
- AC drop detection
- UART receive data
- Frequency dithering
- ZVS control



12.7 System Protection

12.7.1 Cycle-by-Cycle Current Protection (CBC)

The cycle-by-cycle current protection is achieved through AD04 (Comparator D) and AD13 (Comparator E). Once the current signal has exceeded the threshold, the PWM is chopped to limit the current.

12.7.2 Over-Voltage Protection (OVP)

There are two levels of OVP that exist. Under fault condition if the output voltage reaches 420 V, a nonlatched OV protection is activated. Under this condition the output oscillates between 420 V and 380 V.

In the event of a more severe overvoltage condition, if the output reaches to 435 V, the latched overvoltage protection is activated and the unit is completely shut off.

The FIQ is currently used only for latched over-voltage protection. It is triggered by the comparator on AD06 (Comparator F). Comparator F's threshold is set above the limit for the DC bus voltage, and the logic on DPWM1 and DPWM2 is set up to turn off DPWM1B and DPWM2B when the threshold is exceeded. In the current configuration, the only way to restart the PFC after a latched OVP fault is to reset the processor.

12.8 PFC System Control

The system control block diagram is shown in Figure 38. In steady state, the average current-mode control is used with switching frequency fixed at 100 kHz. At low line below 160 V_{AC} and light load, ZVS and valley control is used to reduce the switching losses and reduce total harmonic distortion.



Figure 38. Single-Phase PFC System Control Diagram



(1)

12.8.1 Average Current Mode Control

The current loop is shown in the dashed line of Figure 38. The current reference signal I_{REF} is calculated as:

$$I_{REF} = K_{m} \times A \times C \times B = K_{m} \times (U_{v}) \times (K_{f} \times V_{IN}) \times \left(\frac{1}{V_{RMS}^{2}}\right)$$

where

- Km multiplier gain
- A voltage loop output
- B 1/(V_{IN(rms)})2
- C V_{IN}

For sine wave input, the multiplier gain K_m is expressed as,

$$K_{\rm m} = 0.5 \times K_{\rm f} \times V_{\rm MIN(pk)} \tag{2}$$

In Figure 27, Ks and Kf are scaling factors. For further detail, please refer to reference , and .

12.8.2 ZVS and Valley Control

Please refer to the reference and .

12.9 Current Feedback Control Compensation Using PID Control

A functional block diagram of single-phase PFC control loop is shown in Figure 39.

PID control is usually used in the feedback loop compensation in digitally controlled power converters. Described below are several aspects using PID control in the single-phase PFC feedback control loop.



Figure 39. Single-phase PFC Feedback Loop Using PID Control



(9)

Digital PFC Description

12.9.1 Loop Compensation from Poles and Zeros in s-Domain

PID control in the UCD3138 CLA for current control loop in single-phase PFC is formed in the following equation in z-domain:

$$G_{c}(z) = K_{P} + K_{I} \frac{1 + z^{-1}}{1 - z^{-1}} + K_{D} \frac{1 - z^{-1}}{1 - \alpha \times z^{-1}}$$
(3)

If Equation 3 is converted to the s-domain equivalent using the bilinear transform, the result has two forms. One is with two real zeros:

$$G_{cz}(s) = K_0 \frac{\left(\frac{s}{\omega_{z1}} + 1\right)\left(\frac{s}{\omega_{z2}} + 1\right)}{s\left(\frac{s}{\omega_{p1}} + 1\right)}$$
(4)

The two zeros can also be presented with complex conjugates and in such case,

$$G_{cz}(s) = K_0 \frac{\left(\frac{s^2}{\omega_r^2} + \frac{s}{Q \times \omega_r} + 1\right)}{s\left(\frac{s}{\omega_{p1}} + 1\right)}$$
(5)

Two complex conjugate zeros are expressed as:

$$\omega_{z1, z2} = \frac{\omega_{r}}{2 \times Q} \left(1 \pm \sqrt{1 - 4 \times Q^{2}} \right)$$
(6)

$$\omega_{\rm r} = \sqrt{\omega_{\rm z1} \times \omega_{\rm z2}} \tag{7}$$

$$Q = \frac{\sqrt{\omega_{z1} \times \omega_{z2}}}{\omega_{z1} + \omega_{z2}}$$
(8)

The complex conjugate zeros become real zeros when:

 $Q \leq 0.5\,$



The sensing circuit in the current loop forms a low-pass filter and adds a pole to the loop:

$$\omega_{pcs} = \frac{1}{R_4 \times C_{p2}}$$

$$H_{cs}(s) = R_s \times \frac{R_4}{R_3} \frac{1}{\frac{s}{\omega_{pcs}} + 1}$$
(10)
(11)

The current closed-loop transfer function is then shown below:

$$G_{cs}(s) = \frac{G_M(s) \times G_{PID}(s)}{1 + G_M(s) \times G_{PID}(s) \times H_{cs}(s)}$$

where

• GM(s) is the transfer function of current loop before adding in PID. (12)

The parameters can be calculated with the assumption of current sensor sampling cycle T_s much smaller than the time constant of the PFC choke L_B and R_B , where L_B is the choke inductance and R_B is the choke DC resistance. Choose the sampling frequency to meet:

$$T_{s} = \frac{1}{f_{s}} \le 0.05 \times \frac{L_{B}}{R_{B}}$$
(13)

When the above assumption is true, the delay effect from the sampling can be ignored and the parameters can be determined after we know where the poles and zeros should be positioned.

$$K_{P} = \frac{K_{0} \times \left(\omega_{p1} \times \omega_{z1} + \omega_{p1} \times \omega_{z2} - \omega_{z1} \times \omega_{z2}\right)}{\omega_{p1} \times \omega_{z1} \times \omega_{z2}}$$
(14)

$$K_{I} = \frac{K_{0} \times T_{s}}{2}$$
(15)

$$K_{\rm D} = \frac{2 \times K_0 \times \left(\omega_{\rm p1} - \omega_{\rm z1}\right) \times \left(\omega_{\rm p1} - \omega_{\rm z2}\right)}{\omega_{\rm p1} \times \omega_{\rm z1} \times \omega_{\rm z2} \left(T_{\rm s} \times \omega_{\rm p1} + 2\right)}$$
(16)

$$\alpha = \frac{2 - T_s \times \omega_{p1}}{2 + T_s \times \omega_{p1}}$$
(17)



12.9.2 Feedback Loop Compenstaion Tuning with PID Coefficients

When fine tuning the feedback control loop, one would like to know each parameter in PID how to affect the control loop characteristics without going through complicated description of the above equations. Table 6 below helps this and is visually shown in Figure 40.

Control Parameters	Impact on bode plot	
KP	Increasing KP	
•	Pushes up the minimum gain between the two zeros.	
•	Moves the two zeros apart.	
KI	Increasing KI	
•	Pushes up integration curve at low frequencies.	
•	Gives a higher low frequency gain.	
•	Moves the first zero to the right.	
KD	Increasing KD	
•	Shifts the second zero left.	
•	Does not impact the second pole.	
α	Increasing a	
•	Shifts the second pole to the right.	
•	Shifts the second zero to the right.	
$T_s = 1 / f_s$	Increasing the sampling frequency f_s :	
•	Causes the whole Bode plot to shift to right.	

Table 6. Tuning with PID Coefficients



Figure 40. Tuning PID Parameters

12.9.3 Feedback Loop Compensation with Multiple-Set of Parameters

The digital control provides more flexibility to establish PID coefficients in multiple sets to adapt various operation conditions. For example, the single-phase PFC EVM has two sets of PID coefficients, set A is for low-line operation when the line voltage is between 90 V_{AC} and 160 V_{AC} ; while set B is for high-line operation when the line voltage is above 160 V_{AC} until 264 V_{AC} .

12.10 Voltage Feedback Loop

The voltage feedback loop is a slow response loop with cross-over frequency is usually designed below 20 Hz to reduce the effect from AC line frequency. PI control is usually sufficient in this feedback loop control. During high-transient operation which causes large bulk-voltage deviation greater than certain values, for example, over 5%, digital control can adapt this high-transient requirement to use a different set of PI coefficients.



13 Evaluating the Single-Phase PFC with GUI

Further evaluation of UCD3138PFCEVM-026 can be made with the designer GUI while no need to directly access the firmware codes. The designer GUI, called Fusion Digital Power Designer is described in Section 13.1. The description is given on how to use the GUI to make further evaluation of UCD3138PFCEVM-026.

13.1 Graphical User Interface (GUI)

Collectively, the GUI is called Texas Instruments Fusion Digital Power Designer. The GUI serves the interface for several families of TI digital control devices including the family of UCD31xx, that is the UCD3138 as its one member. The GUI can be divided into two main categories, Designer GUI and Device GUI. In the family of UCD31xx, each EVM is related to a particular Designer GUI to allow users to re-tune/re-configure a particular EVM in that regarding with existing hardware and firmware. Device GUI is related to a particular device to access its internal registers and memories.

UCD3138PFCEVM-026 is used with its control card UCD3138CC64EVM-030 where UCD3138 device is placed. The firmware for single-phase PFC control is loaded into UCD3138CC64EVM-030 board through device GUI. How to install the GUI is described in the user's guide *Using the UCD3138CC64EVM-030 (TI Liturature Number, SLUU886)*. The designer GUI is installed at the same time when installing the device GUI.

13.2 Open the Designer GUI

To open the Designer GUI, click the start with the path as shown in Figure 41.







13.3 Overview of the Designer GUI

When the designer GUI is open, it identifies the connected board by the ID in the firmware. Figure 42 shows the opened GUI. The Designer GUI provides various assistance to access the firmware codes indirectly. For the full set of the functions that the Designer GUI can provide, please refer to the user's manual. In this application note, we focus on how to make monitoring, board re-configuring and re-tuning to show basic aspects on how to use the GUI in a typical power supply design evaluation on a bench test.



Figure 42. Designer GUI Overview

13.3.1 Monitor

On the lower left corner of that shown in Figure 42, there are four tabs, called *Configure*, *Design*, *Monitor* and *Status*. Clicking each tab brings a unique page to the front of that page. The clicked tab is highlighted in blue. Figure 42 shows *Monitor* tab was clicked. The page shows all variables in monitoring with UCD3138 single-phase PFC. These variables are communicated through PMBus. Adding more variables in *Monitoring* is possible but has to be executed through the firmware code change and re-compile process.



13.3.2 Status

When click tab *Status*, its corresponding page is shown in Figure 43. What can be seen is all entries are grayed out. This means nothing was designed to show from this tab. The page of *Status* provides all possible PMBus supported variables in communication. To activate these variables in communication, corresponding firmware codes need to be in place. As what can be seen is all in gray which means none of the variables is established in communication in this page.



Figure 43. Page of Status

13.3.3 Design and Configure

If click *Design* or *Configure* two more different pages will be brought up to the front. These pages provide more functions and described in the following section.

14 Monitoring, Re-configuring and Re-tuning with Designer GUI

In this section, we describe how to use the Designer GUI to evaluate the single-phase PFC board, UCD3138PFCEVM-026

14.1 Power On and Test Procedure

Power stage connection is the same as described earlier. Additionally to that setup, PMBus connection is required through USB-to-GPIO as shown in Figure 44.

After all connections are made, apply an AC source voltage with a specified value to the board AC input and refer to the other steps in the UCD3138PFCEVM-026 user's guide. Open and start the "Fusion Digital Power Designer" GUI following the steps described in Section 13.2 and Section 13.3. Once PFC preregulator is up and running and the GUI is opened, then it is ready to use the Designer GUI to make evaluation.



Figure 44. Hardware Setup for Evaluation with Designer GUI



Monitoring, Re-configuring and Re-tuning with Designer GUI

14.2 Monitoring with GUI

The page shows three variables in monitoring:

- V_{OUT} PFC output bulk voltage.
- OV Fault PFC output bulk voltage over voltage fault threshold.
- Freq switching frequency in normal operation.

Among three monitoring variables, we can see V_{OUT} and OV Fault can be accessed by write to change them to a different value into the firmware. However, when attempting to do so, make sure to understand the design of all aspects to avoid any possible damage. As a warning to help avoid damage, if one wants to modify "Vout" or "OV Fault" to a different value, the recommendation is 375 V to 395 V for V_{OUT}, and not exceeding 430 V for *OV* Fault. Also, logically, V_{OUT} has to be smaller than *OV* Fault.

One may modify them to other values but before doing that, fully understanding the design is needed to find out any other parameters needed to change accordingly such that not over stress the components in use or inducing any stability concerns.



Monitoring, Re-configuring and Re-tuning with Designer GUI

14.3 Configuration and Re-configuring with GUI

After click the tab of "Configure", the corresponding page called "Configuration" is shown as in Figure 45.

The variables shown in the page are the existing configuration. Most of them are fixed and can only be modified through firmware codes. One can designate which and how many variables can be re-configured in this page through firmware codes change. With the single-phase PFC board, there are three variables can be re-configured through this page without going through the firmware codes. As mentioned before, modify these variables to a different value requires fully understanding the design to avoid possible damage.

- V_{OUT} PFC output bulk voltage
- OV Fault PFC output bulk voltage over voltage fault threshold
- Freq switching frequency in normal operation.

As mentioned earlier, the firmware version in use is shown in the page of "Configuration". The firmware version is called DEVICE_ID. When place the mouse curser on, the version indication is shown,

UCD3100ISO1 | 0.0.8.0129 | 111209

The firmware version or Device_ID is divided by two vertical lines. UCD3100ISO1 is the IC device family code. Between the two vertical lines, the show is the firmware recompilation indicator. The last six digits are date of the last time the recompilation was made.

File Device Tools H	lelp			PEC	SinglePhase @ Address 88d	
onfigure	Configuration					
Write to Hardware	Command	Code	Value/Edit	Hex/Edit		P
Auto write on rail or	▼ Configuration					
Discard Changes	FREQUENCY_SWITCH	0x33	100.0 😴 kHz	0x0064		
	YOUT_COMMAND	0x21	390.000 🕀 V	0x0186		
Store RAM To Flash	YOUT_MODE	0x20	EXP 0	0x00		
estore Flash to RAM	▼ Limits					
lear Restore Notices	YOUT_OY_FAULT_LIMIT	0×40	434.000 😌 V	0×01B2		
t Daramatars Bu	🔻 Manufacturer Info					
Command Name Command Code	CMDS_DCDC_NONPAGED [MFR 21]	0×E5	Click 🔽	0x00 🔽		
	CMDS_DCDC_PAGED [MFR 20]	0xE4	Click	0x00		
	CMD5_PFC [MFR 22]	0xE6	Click 🕑	0×00 🔽		
Group by category	DEVICE_ID [MFR 45]	0xFD	UCD3100ISO1	0x55 🔽		
	MFR_ID	0×99	П	0x5449 🔽		
	MFR_MODEL	0x9A	PFC UCD3100ISO1	0.0.8.0129 1112	14	
	MFR_REVISION	0×9B	0.0.0	0x30 🔽		
	PMBUS_REVISION	0×98	1.1,1.1 - Part	0x11		
	SETUP_ID [MFR 23]	0xE7	VERSIO	0x56 🔽		
	▼ Status	11.58.538				
	Tips & Hints	PMBus Log				
Configure	MFR_ID [0x99]	10:12:09.743: USB-	SAA #1: CONTROL1 n	ow Low		
Design	Manufacturer's ID as ASCII text (name, abbreviation or symbol that	10:12:10.243: PFC	binglernase (± 660; U.	DER_RAM_UU [MFI	R 10,0XDAJ: WROLE I [0X01] LO RAM	
Monitor	identifies the unit's manufacturer).					
Status	Ch Ch	PMBus Log				P

Figure 45. Page of Configuration



14.4 Feedback Control Loop Tuning and Re-Tuning with GUI

After click the tab of *Designer*, the page is shown as in Figure 46. In the UCD3138PFCEVM-026, this page is dedicated to the feedback loop design. This page including two sub-pages. One is for the current loop PID coefficients and the other is for the voltage feedback loop which uses PI control.

Calculate	Current Loop (CLA #1) Voltage	Lease / Coffeenant			
Calculate	And a second sec	Loop (Software,			
	R1: 400.00 🔽 KΩ 💟	CD2:	100.00 🚽 pF 🖂		(Franusser Barnance
OTHER C SLOUGERS	R2: 1.24 🖶 kΩ 💌	Cap. ESR:	0.00 🕀 mΩ 🔽		
Auto calculate	R3: 2.00 🚭 kΩ 💌	Induct, DCR	0.00 🖶 mΩ 🔽		Metrics: Loop Stage Coop:
View Coeff "C" Code	R4: 50.00 🗧 kΩ 💌	Vbus:	390.00 🕀 V 🔽	_	Phase Margin: 22.18°
Inload Compensation	R5: 400.00 🚭 kΩ 💌	DC Vin:	195.00 🕀 V 🖂		Gain Margin: Not Defined
	R6: 1.83 😴 kΩ 💌	DC Vin min:	80.00 🕀 V 🔽		Gain - Magnitude
rite Loop Coefficients	Cb: 220.00 😴 µF 🗹	Vin sense os:	0.00 🕀 V 🔽	1	
	L3: 0.000 🗐 🖬 🖂	11	300.00 😌 µH 🔽		1 75
Store RAM to Hash	C2: 0.000 🗐 🔎 🔽	DCR2;	0.000 🗐 😡 🔽		
Frors	C3: 0.000 🕀 🕼 🔽	Esr2:	0.000 🗐 🖟 🖂		25
	Rd: 0.000 🕀 μΩ 🔽	Esr3:	0.000 🗐 😡 🔽		Σ -25
	Vf: 0.000 🕀 µV 🔽	Rds_Q1:	0.000 🕄 μΩ 🔽		10 100 1,000 10,000
	Rs1: 10.00 🕀 mΩ 🔽	Cds_Q1:	0.000 🕀 µF 🔽		Frequency (Hz)
		Condet of Deal			Gain - Phase
	PFC current loop:	I/DCM based on (parameters.		
	CCM power stage model				
	O DCM power stage model				
Configure	Resistive 🔽 RL: 45	50.00 😴 Ω	~		
Design	Tdelay:	0,00 🐳 s	~		-1881 10 100 1,000 10,000 Frequency (Hz)
Monitor	Scher	matic View			
Status	4 New PMBus Log Messages	Show PMBus Lo	a (Unique	e open/close settings for Configure, Design, and Monit

Figure 46. Page of Designer



14.4.1 Current Loop Evaluation

Figure 46shows the current control loop. To evaluate the design or to re-tune the current loop PID coefficients, the first thing to do is to check all the parameters up to date in use. This can be done by click *Schematic View* to bring out a new window with the schematics shown in Figure 47. If any values are different from those in the physical circuitry, one needs to update them before doing any control loop re-tuning.



Figure 47. Schematics of Single-Phase PFC.

Monitoring, Re-configuring and Re-tuning with Designer GUI

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14.4.2 Current Loop Re-Tuning

The current loop PID coefficients can be re-tuned following the approaches described in section 1.4. Scroll down the window that is shown in Figure 46, then Figure 48 is obtained.

Figure 37 shows the current loop compensation details. There are two sets of PID coefficients used in the current control loop, Set A and Set B. In Figure 48 Set A is shown. The corresponding bode plots are shown on the left in Figure 48.

Coefficients of Set A are used when input line voltage is between 90 V_{AC} and 160 V_{AC} . Coefficients of Set B are used when input line voltage is above 160 V_{AC} till the maximum input of 264 V_{AC} .

The actual PID control makes re-scale of the values shown in Figure 48 when used inside the UCD3138.

$$G_{\text{PID}}(z) = \left(K_{\text{P}} + K_{\text{I}}\frac{1 + z^{-1}}{1 - z^{-1}} + K_{\text{D}}\frac{1 - z^{-1}}{1 - 2^{-8} \times \alpha \times z^{-1}}\right) \times 2^{\text{SC}} \times \text{KCOMP} \times 2^{-19} \times \frac{1000}{2^{4} \times (\text{PRD} + 1)}$$
(18)

PRD is a threshold value used to generate DPWM cycle ending point. The DPWM is centered on a period counter which counts up from 0 to PRD, and then is reset and starts over again. In the single-phase PFC design, KCOMP is set up equal to PRD.

In the current control page of the *Design*, PID coefficients can be re-tuned. The GUI also provides conversion results from PID coefficients to the zeros and the pole by clicking *Mode* to select a corresponding conversion. One can also change the zeros and the poles and then use the GUI to convert to PID coefficients by clicking *Mode* to select back to K_P , K_I , and K_D . Be aware that from the two zeros can be complex conjugates. When a set of PID coefficients does make complex conjugate zeros, the GUI pumps up a message to notify that Q and ω r have to be generated instead of real zeros. In this case, the users may need to calculate the complex conjugate zeros based on Equation 6.



Figure 48. Current Loop Re-Tuning

SLUU885B-March 2012-Revised July 2012

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14.4.3 Voltage Loop Evaluation and Re-tuning

Voltage loop can be evaluated and re-tuned in a similar way. Figure 49 shows voltage loop PI control coefficients and corresponding bode plots.

The voltage loop PI control is implemented with software and has the below form,

$$G_{PI}(z) = K_P + K_I \frac{1}{1 - z^{-1}}$$

There are two sets of the PI coefficients for voltage loop control. In normal operation, the control is with *Linear Coefficients*. In transient when the PFC output bulk voltage exceeds the defined *Error Threshold*, for example, 16.0 V, as shown, the PI control coefficients are changed to *Non-Linear Coefficients* to achieve better transient response and to eliminate the output large deviation faster. The output error threshold is usually within 5% of the output set point, or within 20 V on 390-V_{DC} output.

👆 Fusion Digital Power Designer - PFC SinglePhase @ Address 88 - Page 0x0 - Texas Instruments File Device Tools Help PFC SinglePhase @ Address 88 Design Current Loop (CLA #1) Voltage Loop (Software) L3: 0.000 L1 300.00 🕀 µH 🔽 ~ Plots **Frequency Response** C2: DCR2: 0.000 Auto Calculate Loop: Metrics:
 Loop
 Stage Frequency Data C3: 0.000 Esr2: 0.000 Stage: Crossover: 2.67 Hz View Coeff "C" Code Comp: 🚃 Rd: 0.000 🗧 μΩ 🔽 Esr3: 0.000 Phase Margin: 74.76° Gain Margin: Not Defined VF: 0.000 🕀 µV **Upload** Compensation N Rds_Q1: 0.000 😫 μΩ 🔽 10.00 🗧 mΩ 🔽 Cds_Q1: 0.000 🕀 µF 🔽 Rs1: Gain - Magnitude Write Coefficients Resistive RL: 450.00 🚔 Ω × Store RAM to Flash Schematic View ... Magnitude Errors **Compensation - Voltage Loop** -60 Plot in Bode:

Linear
Non-Linear 1000 10 100 0.1 1 Frequency (Hz) Linear Coefficients: Kp: 1.000E+0 0×00008000 Gain - Phase Ki: 3.693E-3 0x00000079 -10 Non-Linear Coefficients: (Degr -30 0x00058147 Kp: 1.101E+1 -50 -70 Angle 0x000001CA Ki: 1.398E-2 Configure -90 -110 16.0 🕀 V Error Threshold: 1000 0.1 1 10 100 Design Frequency (Hz) If Vbus-Vref is greater than threshold, non-linear coefficients are used. Monitor 🔄 Unique open/close settings for Configure, Design, and Monitor 📮 6 New PMBus Log Messages Show PMBus Log Status Fusion Digital Power Designer v1.8.186 [2012-02-29] PFC SinglePhase Firmware v0.0.8.129 @ Address 88 USB Adapter v1.0. TEXAS INSTRUMENTS | fusion digital power

Figure 49. Voltage Loop PI Control Re-Tuning





15 Digital PFC Firmware Development

Please contact TI for additional information regarding UCD3138 digital PFC firmware development.

16 References

- 1. UCD3138 Datasheet, SLUSAP2, 2012
- 2. UCD3138CC64EVM-030 Evaluation Module and User's Guide, SLUU886, 2012
- 3. SEM600, 1988, High Power Factor Pre-regulator for Off-line Power Supplies
- 4. SEM700, 1990, Optimizing the Design of a High Power Factor Switching Pre-regulator
- 5. <u>TI Application Note SLUA644</u>, "PFC THD Reduction and Efficiency Improvement by ZVS or Valley Switching", April 2012.
- Zhong Ye and Bosheng Sun, "PFC Efficiency Improvement and THD Reduction at Light Loads with ZVS and Valley Switching", APEC 2012, pp 802-806
- 7. UCD3138 Digital Power Peripherals Programmer's Manual (please contact TI)
- 8. UCD3138 Monitoring and Communications Programmer's Manual (please contact TI)
- 9. UCD3138 ARM and Digital System Programmer's Manual (please contact TI)
- 10. UCD3138 Isolated Power Fusion GUI User Guide (please contact TI)

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- Reorient or relocate the receiving antenna.
- Increase the separation between the equipment and receiver.
- · Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.
- Consult the dealer or an experienced radio/TV technician for help.

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This radio transmitter has been approved by Industry Canada to operate with the antenna types listed in the user guide with the maximum permissible gain and required antenna impedance for each antenna type indicated. Antenna types not included in this list, having a gain greater than the maximum gain indicated for that type, are strictly prohibited for use with this device.

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- Reorient or relocate the receiving antenna.
- Increase the separation between the equipment and receiver.
- · Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.
- Consult the dealer or an experienced radio/TV technician for help.

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- 3. Use of this product only after you obtained the Technical Regulations Conformity Certification as provided in Radio Law of Japan with respect to this product. Also, please do not transfer this product, unless you give the same notice above to the transferee. Please note that if you could not follow the instructions above, you will be subject to penalties of Radio Law of Japan.

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EVALUATION BOARD/KIT/MODULE (EVM) WARNINGS, RESTRICTIONS AND DISCLAIMERS

For Feasibility Evaluation Only, in Laboratory/Development Environments. Unless otherwise indicated, this EVM is not a finished electrical equipment and not intended for consumer use. It is intended solely for use for preliminary feasibility evaluation in laboratory/development environments by technically qualified electronics experts who are familiar with the dangers and application risks associated with handling electrical mechanical components, systems and subsystems. It should not be used as all or part of a finished end product.

Your Sole Responsibility and Risk. You acknowledge, represent and agree that:

- 1. You have unique knowledge concerning Federal, State and local regulatory requirements (including but not limited to Food and Drug Administration regulations, if applicable) which relate to your products and which relate to your use (and/or that of your employees, affiliates, contractors or designees) of the EVM for evaluation, testing and other purposes.
- 2. You have full and exclusive responsibility to assure the safety and compliance of your products with all such laws and other applicable regulatory requirements, and also to assure the safety of any activities to be conducted by you and/or your employees, affiliates, contractors or designees, using the EVM. Further, you are responsible to assure that any interfaces (electronic and/or mechanical) between the EVM and any human body are designed with suitable isolation and means to safely limit accessible leakage currents to minimize the risk of electrical shock hazard.
- 3. You will employ reasonable safeguards to ensure that your use of the EVM will not result in any property damage, injury or death, even if the EVM should fail to perform as described or expected.
- 4. You will take care of proper disposal and recycling of the EVM's electronic components and packing materials.

Certain Instructions. It is important to operate this EVM within TI's recommended specifications and environmental considerations per the user guidelines. Exceeding the specified EVM ratings (including but not limited to input and output voltage, current, power, and environmental ranges) may cause property damage, personal injury or death. If there are questions concerning these ratings please contact a TI field representative prior to connecting interface electronics including input power and intended loads. Any loads applied outside of the specified output range may result in unintended and/or inaccurate operation and/or possible permanent damage to the EVM and/or interface electronics. Please consult the EVM User's Guide prior to connecting any load to the EVM output. If there is uncertainty as to the load specification, please contact a TI field representative. During normal operation, some circuit components may have case temperatures greater than 60°C as long as the input and output are maintained at a normal ambient operating temperature. These components include but are not limited to linear regulators, switching transistors, pass transistors, and current sense resistors which can be identified using the EVM schematic located in the EVM User's Guide. When placing measurement probes near these devices during normal operation, please be aware that these devices may be very warm to the touch. As with all electronic evaluation tools, only qualified personnel knowledgeable in electronic measurement and diagnostics normally found in development environments should use these EVMs.

Agreement to Defend, Indemnify and Hold Harmless. You agree to defend, indemnify and hold TI, its licensors and their representatives harmless from and against any and all claims, damages, losses, expenses, costs and liabilities (collectively, "Claims") arising out of or in connection with any use of the EVM that is not in accordance with the terms of the agreement. This obligation shall apply whether Claims arise under law of tort or contract or any other legal theory, and even if the EVM fails to perform as described or expected.

Safety-Critical or Life-Critical Applications. If you intend to evaluate the components for possible use in safety critical applications (such as life support) where a failure of the TI product would reasonably be expected to cause severe personal injury or death, such as devices which are classified as FDA Class III or similar classification, then you must specifically notify TI of such intent and enter into a separate Assurance and Indemnity Agreement.

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