**Freescale Semiconductor**
**Technical Data**

MPC7447AECS02AD
Rev. 1, 10/2004

# MPC7447A Hardware Specification Addendum for the MC7447AT*xxnnnn*N*x* Series

This document describes part-number-specific changes to recommended operating conditions and revised electrical specifications, as applicable, from those described in the general *MPC7447A RISC Microprocessor Hardware Specifications*. The MPC7447A is a PowerPC™ microprocessor.

Specifications provided in this document supersede those in the *MPC7447A RISC Microprocessor Hardware Specifications* (Freescale document order number MPC7447AEC), Rev 1 or later, for the part numbers listed in Table A only. Specifications not addressed herein are unchanged.

Note that headings and table numbers in this document are not consecutively numbered. They are intended to correspond to the heading or table affected in the general hardware specification.

*Freescale Part Numbers Affected:*

*MC7447ATHX867NB*
*MC7447ATHX1000NB*
*MC7447ATHX1167NB*



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Part numbers addressed in this document are listed in Table A.

**Table A. Part Numbers Addressed by this Data Sheet**

| Motorola Part Number | Operating Conditions | | | Significant Differences from Hardware Specification |
|---|---|---|---|---|
| | CPU Frequency (MHz) | $V_{DD}$ | $T_j$ (°C) | |
| MC7447ATHX867NB | 867 | 1.1 V ± 50 mV | –40 to 105 | Modified core frequency and voltage to reduce power consumption; extended temperature range. |
| MC7447ATHX1000NB | 1000 | | | |
| MC7447ATHX1167NB | 1167 | | | |

# 4 General Parameters

Core power supply 1.1 V ± 50 mV DC (nominal), or
1.0 V ± 50 mV DC (derated)

## 5.1 DC Electrical Characteristics

Table 4 provides the recommended operating conditions for the MPC7447A part numbers described herein.

**NOTE**

Table 4 describes the nominal operating conditions of the device. For information regarding the operation of the device at supported derated core voltage conditions, see Section 5.3, "Voltage and Frequency Derating."

**Table 4. Recommended Operating Conditions [1]**

| Characteristic | Symbol | Recommended Value | Unit | Notes |
|---|---|---|---|---|
| Core supply voltage | $V_{DD}$ | 1.1 V ± 50 mV | V | 3 |
| PLL supply voltage | $AV_{DD}$ | 1.1 V ± 50 mV | V | 2, 3 |

**Note:**
1. These are the recommended and tested operating conditions. In addition, these devices also support voltage derating; see Section 5.3, "Voltage and Frequency Derating." Proper device operation outside of these conditions and those specified in Section 5.3 is not guaranteed.
2. This voltage is the input to the filter discussed in *MPC7447A RISC Microprocessor Hardware Specifications*, Section 9.2, "PLL Power Supply Filtering," and not necessarily the voltage at the $AV_{DD}$ pin, which may be reduced from $V_{DD}$ by the filter.
3. $V_{DD}$ and $AV_{DD}$ may be reduced in order to reduce power consumption if further maximum core frequency constraints are observed. See Section 5.3, "Voltage and Frequency Derating," for specific information.

Table 7 provides the power consumption for the MPC7447A part numbers described herein. For information regarding power consumption when dynamic frequency switching (DFS) is enabled, see the *MPC7447A RISC Microprocessor Hardware Specifications*.

**NOTE**

The power consumption information in this table applies when the device is operated at the nominal core voltage indicated in Table 4. For power consumption at derated core voltage conditions, see Section 5.3, "Voltage and Frequency Derating."

**Table 7. Power Consumption for MPC7447A**

| | Processor (CPU) Frequency | | | Unit | Notes |
|---|---|---|---|---|---|
| | 867 MHz | 1000 MHz | 1167 MHz | | |
| **Full-Power Mode** | | | | | |
| Typical | 7.8 | 8.0 | 9.2 | W | 1, 2 |
| Maximum | 10.3 | 11.5 | 13.0 | W | 1, 3 |
| **Nap Mode** | | | | | |
| Typical | 1.3 | 1.3 | 1.3 | W | 1, 2 |
| **Sleep Mode** | | | | | |
| Typical | 1.3 | 1.3 | 1.3 | W | 1, 2 |
| **Deep Sleep Mode (PLL Disabled)** | | | | | |
| Typical | 1.2 | 1.2 | 1.2 | W | 1, 2 |

**Notes:**

1. These values apply for all valid processor buses. The values do not include I/O supply power ($OV_{DD}$) or PLL supply power ($AV_{DD}$). $OV_{DD}$ power is system dependent but is typically < 5% of $V_{DD}$ power. Worst case power consumption for $AV_{DD}$ < 3 mW.
2. Typical power is an average value measured at the nominal recommended $V_{DD}$ (see Table 4) and 65°C while running the Dhrystone 2.1 benchmark and achieving 2.3 Dhrystone MIPs/MHz.
3. Maximum power is the average measured at nominal $V_{DD}$ and maximum operating junction temperature (see Table 4) while running an entirely cache-resident, contrived sequence of instructions which keep all the execution units maximally busy.
4. Doze mode is not a user-definable state; it is an intermediate state between full-power and either nap or sleep mode. As a result, power consumption for this mode is not tested.

## 5.2 AC Electrical Characteristics

Table 8 provides the clock AC timing specifications for the MPC7447A part numbers described herein.

**NOTE**

The core frequency information in this table applies when the device is operated at the nominal core voltage indicated in Table 4. For core frequency specifications at derated core voltage conditions, see Section 5.3, "Voltage and Frequency Derating."

**Table 8. Clock AC Timing Specifications**

At recommended operating conditions. See Table 4.

| Characteristic | Symbol | Maximum Processor Core Frequency | | | | | | Unit | Notes |
|---|---|---|---|---|---|---|---|---|---|
| | | 867 MHz | | 1000 MHz | | 1167 MHz | | | |
| | | Min | Max | Min | Max | Min | Max | | |
| Processor frequency | $f_{core}$ | 500 | 867 | 500 | 1000 | 500 | 1167 | MHz | 1, 2, 3 |
| VCO frequency | $f_{VCO}$ | 1000 | 1733 | 1000 | 2000 | 1000 | 2333 | MHz | 1, 3 |

**Notes**:

1. **Caution**: The SYSCLK frequency and PLL_CFG[0:4] settings must be chosen such that the resulting SYSCLK (bus) frequency, CPU (core) frequency, and PLL (VCO) frequency do not exceed their respective maximum or minimum operating frequencies. Refer to the PLL_CFG[0:4] signal description in *MPC7447A RISC Microprocessor Hardware Specifications,* Section 9.1, "PLL Configuration," for valid PLL_CFG[0:4] settings.
2. **Caution**: If dynamic frequency switching (DFS) is enabled, the SYSCLK frequency and PLL_CFG[0:4] settings must be chosen such that the resulting processor frequency is greater than or equal to the minimum core frequency.
3. **Caution**: These values specify the maximum processor core and VCO frequencies when the device is operated at the nominal core voltage. If operating the device at the derated core voltage, the processor core and VCO frequencies must be reduced. See Section 5.3, "Voltage and Frequency Derating," for more information.

## 5.3 Voltage and Frequency Derating

To reduce the power consumption of the device, these devices support voltage and frequency derating whereby the core voltage ($V_{DD}$) may be reduced if the reduced maximum processor core frequency requirements are observed. The supported derated core voltage, resulting maximum processor core frequency ($f_{core}$), and power consumption are provided in Table 11. Only those parameters in Table 11 are affected; all other parameter specifications are unaffected.

**Table 11. Supported Voltage, Core Frequency, and Power Consumption Derating**

| Maximum Rated Core Frequency (Device Marking) | Supported Derated Core Voltage ($V_{DD}$) | Maximum Derated Core Frequency ($f_{core}$) | Full-Power Mode Power Consumption | |
|---|---|---|---|---|
| | | | Maximum | Typical |
| 867 | 1.0 V ± 50mV | 667 | 6.9 W | 4.9 W |
| 1000 | | 800 | 8.0 W | 5.6 W |
| 1167 | | 1000 | 9.4 W | 6.6 W |

# 11 Ordering Information

## 11.1 Part Numbers Addressed by This Specification

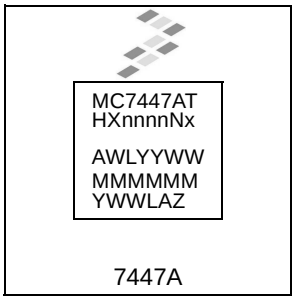
Table 17 provides the ordering information for the MPC7447A parts described in this document.

**Table 17. Part Marking Nomenclature**

| MC | 7447A | T | *xx* | *nnnn* | N | *x* |
|---|---|---|---|---|---|---|
| **Product Code** | **Part Identifier** | **Specification Modifier** | **Package** | **Processor Frequency** | **Application Modifier** | **Revision Level** |
| MC | 7447A | T = Extended Temperature Device | HX = HCTE | 867<br>1000<br>1167 | N: 1.1 V ± 50 mV<br>–40 to 105°C | B:1.1: PVR = 8003 0101 |

## 11.3 Part Marking

Parts are marked as the example shown in Figure 23.




BGA

**Notes:**
AWYYYWW is the test code.
MMMMMM is the M00 (mask) number.
YWWWLAZ is the assembly traceability code.

**Figure 23. Part Marking for BGA Device**

# Document Revision History

Table B provides a revision history for this hardware specification addendum.

**Table B. Document Revision History**

| Rev. No. | Date | Substantive Change(s) |
|---|---|---|
| 1 | 10/05/2004 | Added information on voltage derating, including Table 7 and Table 8; added 1167-MHz speed bin |
| 0 | 09/27/2004 | Initial release |

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