8/16-bit Atmel AVR XMEGA D3 Microcontroller

ATxmega32D3* / ATxmega64D3 / ATxmega128D3 / ATxmega192D3 / ATxmega256D3 / ATxmega384D3*

*Preliminary

Features

- High-performance, low-power Atmel® AVR® XMEGA® 8/16-bit Microcontroller
- Nonvolatile program and data memories
  - 32K - 384KBytes of in-system self-programmable flash
  - 4K - 8KBytes boot section
  - 2K - 4KBytes EEPROM
  - 4K - 16KBytes internal SRAM
- Peripheral features
  - Four-channel event system
  - Five 16-bit timer/counters
    - Four timer/counters with four output compare or input capture channels
    - One timer/counter with two output compare or input capture channels
    - High resolution extension on two timer/counters
    - Advanced waveform extension (AWeX) on one timer/counter
  - Three USARTs with IrDA support for one USART
  - Two two-wire interfaces with dual address match (I^2C and SMBus compatible)
  - Two serial peripheral interfaces (SPIs)
  - CRC-16 (CRC-CCITT) and CRC-32 (IEEE®802.3) generator
  - 16-bit real time counter (RTC) with separate oscillator
  - One sixteen-channel, 12-bit, 300ksps Analog to Digital Converter
  - Two Analog Comparators with window compare function, and current sources
  - External interrupts on all general purpose I/O pins
  - Programmable watchdog timer with separate on-chip ultra low power oscillator
  - Atmel QTouch® library support
    - Capacitive touch buttons, sliders and wheels
- Special microcontroller features
  - Power-on reset and programmable brown-out detection
  - Internal and external clock options with PLL and prescaler
  - Programmable multilevel interrupt controller
  - Five sleep modes
  - Programming and debug interface
    - PDI (program and debug interface)
- I/O and packages
  - 50 programmable I/O pins
  - 64-lead TQFP
  - 64-pad QFN
- Operating voltage
  - 1.6 – 3.6V
- Operating frequency
  - 0 – 12MHz from 1.6V
  - 0 – 32MHz from 2.7V

1. Ordering information

Ordering code	Flash [bytes]	EEPROM [bytes]	SRAM [bytes]	Speed [MHz]	Power supply	Package (1)(2)(3)	Temp.
ATxmega32D3-AU	32K + 4K	2K	4K	32	1.6 - 3.6V	64A	-40°C - 85°C
ATxmega32D3-AUR (4)	32K + 4K	2K	4K				
ATxmega64D3-AU	64K + 4K	2K	4K				
ATxmega64D3-AUR (4)	64K + 4K	2K	4K				
ATxmega128D3-AU	128K + 8K	2K	8K				
ATxmega128D3-AUR (4)	128K + 8K	2K	8K				
ATxmega192D3-AU	192K + 8K	2K	16K				
ATxmega192D3-AUR (4)	192K + 8K	2K	16K				
ATxmega256D3-AU	256K + 8K	4K	16K				
ATxmega256D3-AUR (4)	256K + 8K	4K	16K				
ATxmega384D3-AU	384K + 8K	4K	32K				
ATxmega384D3-AUR (4)	384K + 8K	4K	32K				
ATxmega32D3-MH	32K + 4K	2K	4K			64M	
ATxmega32D3-MHR (4)	32K + 4K	2K	4K				
ATxmega64D3-MH	64K + 4K	2K	4K				
ATxmega64D3-MHR (4)	64K + 4K	2K	4K				
ATxmega128D3-MH	128K + 8K	2K	8K				
ATxmega128D3-MHR (4)	128K + 8K	2K	8K				
ATxmega192D3-MH	192K + 8K	2K	16K				
ATxmega192D3-MHR (4)	192K + 8K	2K	16K				
ATxmega256D3-MH	256K + 8K	4K	16K				
ATxmega256D3-MHR (4)	256K + 8K	4K	16K				
ATxmega384D3-MH	384K + 8K	4K	32K				
ATxmega384D3-MHR (4)	384K + 8K	4K	32K				

Notes:
1. This device can also be supplied in wafer form. Please contact your local Atmel sales office for detailed ordering information.
2. Pb-free packaging, complies to the European Directive for Restriction of Hazardous Substances (RoHS directive). Also Halide free and fully Green.
3. For packaging information, see "Packaging information" on page 61.
4. Tape and Reel.

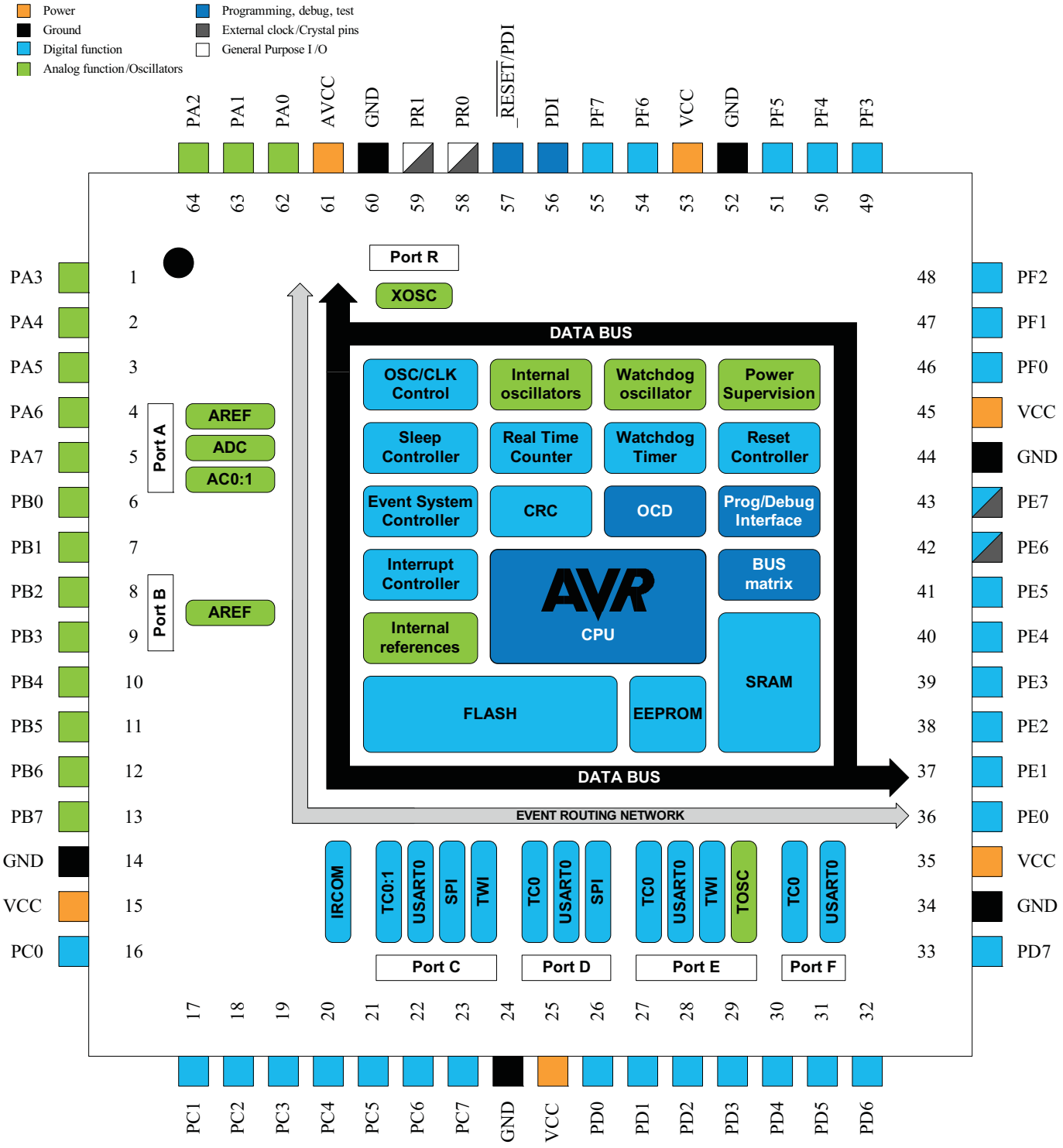
Package type	
64A	64-lead, 14 * 14mm body size, 1.0mm body thickness, 0.8mm lead pitch, thin profile plastic quad flat package (TQFP)
64M	64-pad, 9 * 9 * 1.0mm body, lead pitch 0.50mm, 7.65mm exposed pad, quad flat no-lead package (QFN)

Typical applications

Industrial control	Climate control	Low power battery applications
Factory automation	RF and ZigBee®	Power tools
Building control	Motor control	HVAC
Board control	Sensor control	Utility metering
White goods	Optical	Medical applications

2. Pinout/block diagram

Figure 2-1. Block diagram and pinout.



Notes: 1. For full details on pinout and alternate pin functions refer to "Pinout and pin functions" on page 49.

2. The large center pad underneath the QFN/MLF package should be soldered to ground on the board to ensure good mechanical stability.

3. Overview

The Atmel AVR XMEGA is a family of low power, high performance, and peripheral rich 8/16-bit microcontrollers based on the AVR enhanced RISC architecture. By executing instructions in a single clock cycle, the AVR XMEGA devices achieve CPU throughput approaching one million instructions per second (MIPS) per megahertz, allowing the system designer to optimize power consumption versus processing speed.

The AVR CPU combines a rich instruction set with 32 general purpose working registers. All 32 registers are directly connected to the arithmetic logic unit (ALU), allowing two independent registers to be accessed in a single instruction, executed in one clock cycle. The resulting architecture is more code efficient while achieving throughputs many times faster than conventional single-accumulator or CISC based microcontrollers.

The XMEGA D3 devices provide the following features: in-system programmable flash with read-while-write capabilities; internal EEPROM and SRAM; four-channel event system and programmable multilevel interrupt controller, 50 general purpose I/O lines, 16-bit real-time counter (RTC); five, 16-bit timer/counters with compare and PWM channels; three USARTs; two two-wire serial interfaces (TWIs); two serial peripheral interfaces (SPIs); one sixteen-channel, 12-bit ADC with programmable gain; two analog comparators (ACs) with window mode; programmable watchdog timer with separate internal oscillator; accurate internal oscillators with PLL and prescaler; and programmable brown-out detection.

The program and debug interface (PDI), a fast, two-pin interface for programming and debugging, is available.

The AVR XMEGA devices have five software selectable power saving modes. The idle mode stops the CPU while allowing the SRAM, event system, interrupt controller, and all peripherals to continue functioning. The power-down mode saves the SRAM and register contents, but stops the oscillators, disabling all other functions until the next TWI, or pin-change interrupt, or reset. In power-save mode, the asynchronous real-time counter continues to run, allowing the application to maintain a timer base while the rest of the device is sleeping. In standby mode, the external crystal oscillator keeps running while the rest of the device is sleeping. This allows very fast startup from the external crystal, combined with low power consumption. In extended standby mode, both the main oscillator and the asynchronous timer continue to run. To further reduce power consumption, the peripheral clock to each individual peripheral can optionally be stopped in active mode and idle sleep mode.

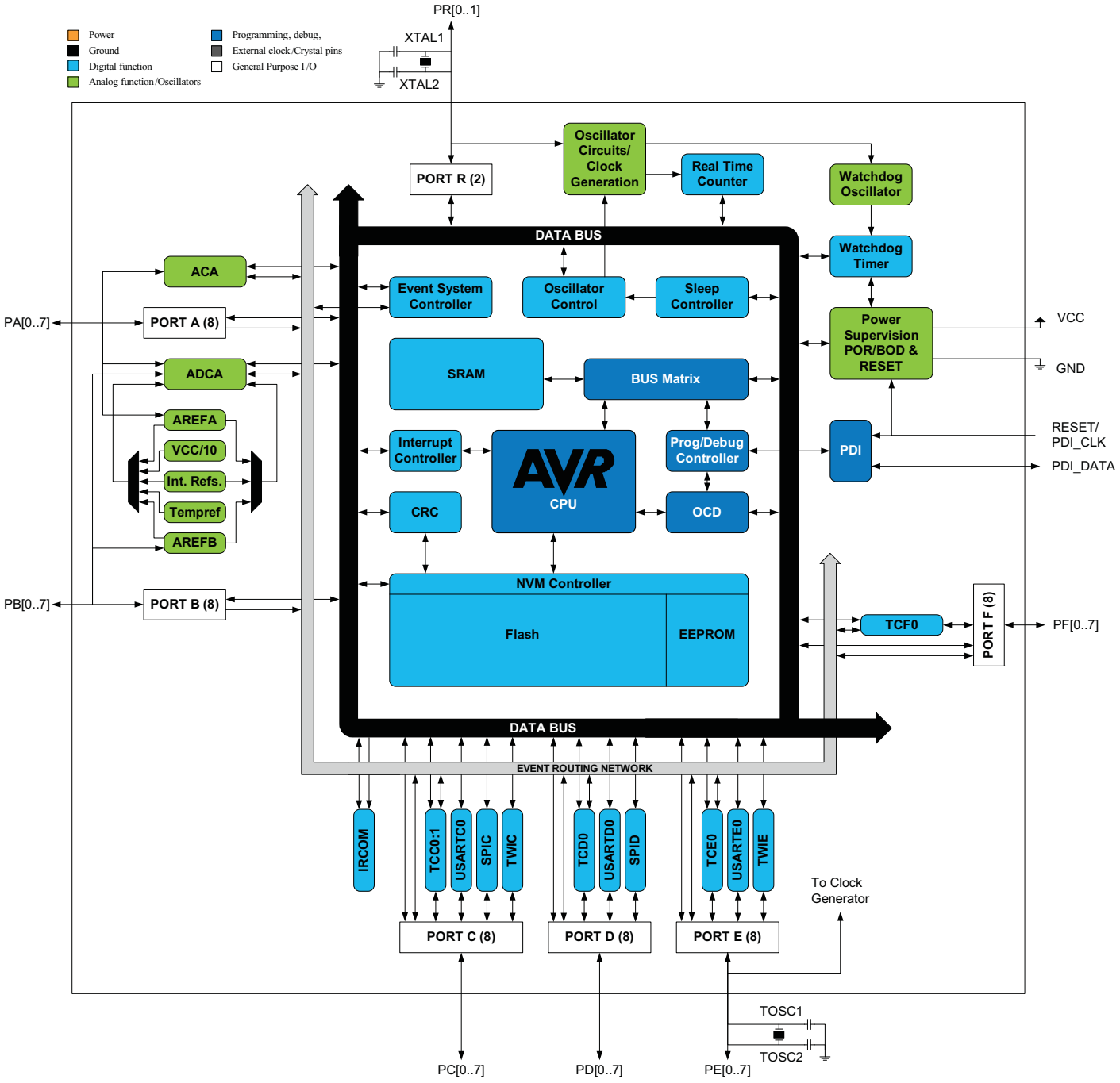
Atmel offers a free QTouch library for embedding capacitive touch buttons, sliders and wheels functionality into AVR microcontrollers.

The devices are manufactured using Atmel high-density, nonvolatile memory technology. The program flash memory can be reprogrammed in-system through the PDI. A boot loader running in the device can use any interface to download the application program to the flash memory. The boot loader software in the boot flash section will continue to run while the application flash section is updated, providing true read-while-write operation. By combining an 8/16-bit RISC CPU with in-system, self-programmable flash, the AVR XMEGA is a powerful microcontroller family that provides a highly flexible and cost effective solution for many embedded applications.

All AVR XMEGA devices are supported with a full suite of program and system development tools, including: C compilers, macro assemblers, program debugger/simulators, programmers, and evaluation kits.

3.1 Block diagram

Figure 3-1. XMEGA D3 block diagram.



4. Resources

A comprehensive set of development tools, application notes and datasheets are available for download on www.atmel.com/avr.

4.1 Recommended reading

- Atmel AVR XMEGA D manual
- XMEGA application notes

This device data sheet only contains part specific information with a short description of each peripheral and module. The XMEGA D manual describes the modules and peripherals in depth. The XMEGA application notes contain example code and show applied use of the modules and peripherals.

All documentation are available from www.atmel.com/avr.

5. Capacitive touch sensing

The Atmel QTouch library provides a simple to use solution to realize touch sensitive interfaces on most Atmel AVR microcontrollers. The patented charge-transfer signal acquisition offers robust sensing and includes fully debounced reporting of touch keys and includes Adjacent Key Suppression® (AKS®) technology for unambiguous detection of key events. The QTouch library includes support for the QTouch and Atmel QMatrix acquisition methods.

Touch sensing can be added to any application by linking the appropriate Atmel QTouch library for the AVR microcontroller. This is done by using a simple set of APIs to define the touch channels and sensors, and then calling the touch sensing API's to retrieve the channel information and determine the touch sensor states.

The QTouch library is FREE and downloadable from the Atmel website at the following location: http://www.atmel.com/tools/qtouchlibrary.aspx. For implementation details and other information, refer to the QTouch library user guide - also available for download from the Atmel website.

6. AVR CPU

6.1 Features

- 8/16-bit, high-performance Atmel AVR RISC CPU
  - 137 instructions
  - Hardware multiplier
- 32x8-bit registers directly connected to the ALU
- Stack in RAM
- Stack pointer accessible in I/O memory space
- Direct addressing of up to 16MB of program memory and 16MB of data memory
- True 16/24-bit access to 16/24-bit I/O registers
- Efficient support for 8-, 16- and 32-bit arithmetic
- Configuration change protection of system-critical features

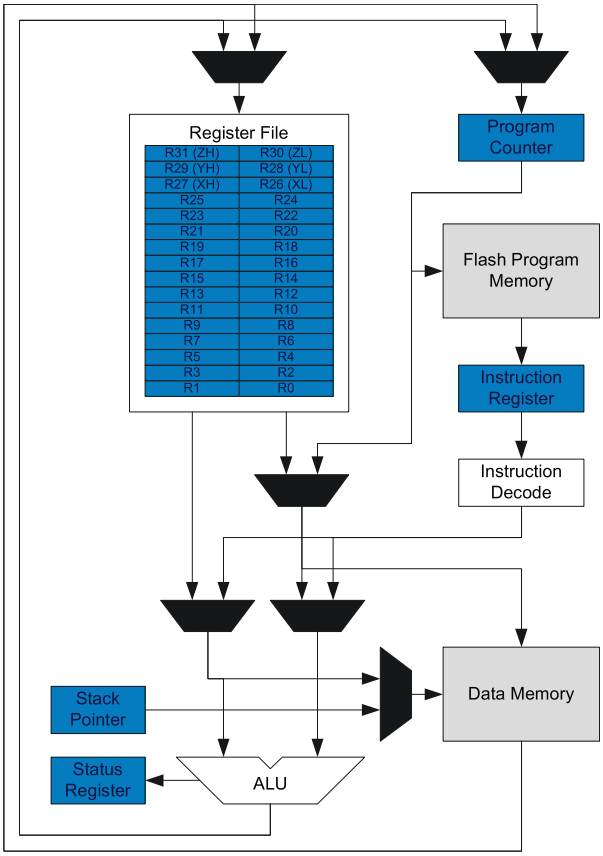
6.2 Overview

All Atmel AVR XMEGA devices use the 8/16-bit AVR CPU. The main function of the CPU is to execute the code and perform all calculations. The CPU is able to access memories, perform calculations, control peripherals, and execute the program in the flash memory. Interrupt handling is described in a separate section, refer to “Interrupts and programmable multilevel interrupt controller” on page 27.

6.3 Architectural overview

In order to maximize performance and parallelism, the AVR CPU uses a Harvard architecture with separate memories and buses for program and data. Instructions in the program memory are executed with single-level pipelining. While one instruction is being executed, the next instruction is pre-fetched from the program memory. This enables instructions to be executed on every clock cycle. For details of all AVR instructions, refer to www.atmel.com/avr.

Figure 6-1. Block diagram of the AVR CPU architecture.



The arithmetic logic unit (ALU) supports arithmetic and logic operations between registers or between a constant and a register. Single-register operations can also be executed in the ALU. After an arithmetic operation, the status register is updated to reflect information about the result of the operation.

The ALU is directly connected to the fast-access register file. The 32 * 8-bit general purpose working registers all have single clock cycle access time allowing single-cycle arithmetic logic unit (ALU) operation between registers or between a register and an immediate. Six of the 32 registers can be used as three 16-bit address pointers for program and data space addressing, enabling efficient address calculations.

The memory spaces are linear. The data memory space and the program memory space are two different memory spaces.

The data memory space is divided into I/O registers, SRAM, and external RAM. In addition, the EEPROM can be memory mapped in the data memory.

All I/O status and control registers reside in the lowest 4KB addresses of the data memory. This is referred to as the I/O memory space. The lowest 64 addresses can be accessed directly, or as the data space locations from 0x00 to 0x3F. The rest is the extended I/O memory space, ranging from 0x0040 to 0x0FFF. I/O registers here must be accessed as data space locations using load (LD/LDS/LDD) and store (ST/STS/STD) instructions.

The SRAM holds data. Code execution from SRAM is not supported. It can easily be accessed through the five different addressing modes supported in the AVR architecture. The first SRAM address is 0x2000.

Data addresses 0x1000 to 0x1FFF are reserved for memory mapping of EEPROM.

The program memory is divided in two sections, the application program section and the boot program section. Both sections have dedicated lock bits for write and read/write protection. The SPM instruction that is used for self-programming of the application flash memory must reside in the boot program section. The application section contains an application table section with separate lock bits for write and read/write protection. The application table section can be used for safe storing of nonvolatile data in the program memory.

6.4 ALU - Arithmetic Logic Unit

The arithmetic logic unit (ALU) supports arithmetic and logic operations between registers or between a constant and a register. Single-register operations can also be executed. The ALU operates in direct connection with all 32 general purpose registers. In a single clock cycle, arithmetic operations between general purpose registers or between a register and an immediate are executed and the result is stored in the register file. After an arithmetic or logic operation, the status register is updated to reflect information about the result of the operation.

ALU operations are divided into three main categories – arithmetic, logical, and bit functions. Both 8- and 16-bit arithmetic is supported, and the instruction set allows for efficient implementation of 32-bit aritmetic. The hardware multiplier supports signed and unsigned multiplication and fractional format.

6.4.1 Hardware multiplier

The multiplier is capable of multiplying two 8-bit numbers into a 16-bit result. The hardware multiplier supports different variations of signed and unsigned integer and fractional numbers:

- Multiplication of unsigned integers
- Multiplication of signed integers
- Multiplication of a signed integer with an unsigned integer
- Multiplication of unsigned fractional numbers
- Multiplication of signed fractional numbers
- Multiplication of a signed fractional number with an unsigned one

A multiplication takes two CPU clock cycles.

6.5 Program flow

After reset, the CPU starts to execute instructions from the lowest address in the flash programmemory ‘0.’ The program counter (PC) addresses the next instruction to be fetched.

Program flow is provided by conditional and unconditional jump and call instructions capable of addressing the whole address space directly. Most AVR instructions use a 16-bit word format, while a limited number use a 32-bit format.

During interrupts and subroutine calls, the return address PC is stored on the stack. The stack is allocated in the general data SRAM, and consequently the stack size is only limited by the total SRAM size and the usage of the SRAM. After reset, the stack pointer (SP) points to the highest address in the internal SRAM. The SP is read/write accessible in the I/O memory space, enabling easy implementation of multiple stacks or stack areas. The data SRAM can easily be accessed through the five different addressing modes supported in the AVR CPU.

6.6 Status register

The status register (SREG) contains information about the result of the most recently executed arithmetic or logic instruction. This information can be used for altering program flow in order to perform conditional operations. Note that the status register is updated after all ALU operations, as specified in the instruction set reference. This will in many cases remove the need for using the dedicated compare instructions, resulting in faster and more compact code.

The status register is not automatically stored when entering an interrupt routine nor restored when returning from an interrupt. This must be handled by software.

The status register is accessible in the I/O memory space.

6.7 Stack and Stack Pointer

The stack is used for storing return addresses after interrupts and subroutine calls. It can also be used for storing temporary data. The Stack Pointer (SP) register always points to the top of the stack. It is implemented as two 8-bit registers that are accessible in the I/O memory space. Data are pushed and popped from the stack using the PUSH and POP instructions. The stack grows from a higher memory location to a lower memory location. This implies that pushing data onto the stack decreases the SP, and popping data off the stack increases the SP. The SP is automatically loaded

after reset, and the initial value is the highest address of the internal SRAM. If the SP is changed, it must be set to point above address 0x2000, and it must be defined before any subroutine calls are executed or before interrupts are enabled.

During interrupts or subroutine calls, the return address is automatically pushed on the stack. The return address can be two or three bytes, depending on program memory size of the device. For devices with 128KB or less of program memory, the return address is two bytes, and hence the stack pointer is decremented/incremented by two. For devices with more than 128KB of program memory, the return address is three bytes, and hence the SP is decremented/incremented by three. The return address is popped off the stack when returning from interrupts using the RETI instruction, and from subroutine calls using the RET instruction.

The SP is decremented by one when data are pushed on the stack with the PUSH instruction, and incremented by one when data is popped off the stack using the POP instruction.

To prevent corruption when updating the stack pointer from software, a write to SPL will automatically disable interrupts for up to four instructions or until the next I/O memory write.

After reset the stack pointer is initialized to the highest address of the SRAM. See Figure 7-2 on page 15.

6.8 Register file

The register file consists of 32 * 8-bit general purpose working registers with single clock cycle access time. The register file supports the following input/output schemes:

- One 8-bit output operand and one 8-bit result input
- Two 8-bit output operands and one 8-bit result input
- Two 8-bit output operands and one 16-bit result input
- One 16-bit output operand and one 16-bit result input

Six of the 32 registers can be used as three 16-bit address register pointers for data space addressing, enabling efficient address calculations. One of these address pointers can also be used as an address pointer for lookup tables in flash program memory.

7. Memories

7.1 Features

- Flash program memory
  - One linear address space
  - In-system programmable
  - Self-programming and boot loader support
  - Application section for application code
  - Application table section for application code or data storage
  - Boot section for application code or boot loader code
  - Separate read/write protection lock bits for all sections
  - Built in fast CRC check of a selectable flash program memory section
- Data memory
  - One linear address space
  - Single-cycle access from CPU
  - SRAM
  - EEPROM
    - Byte and page accessible
    - Optional memory mapping for direct load and store
  - I/O memory
    - Configuration and status registers for all peripherals and modules
    - Four bit-accessible general purpose registers for global variables or flags
- Production signature row memory for factory programmed data
  - ID for each microcontroller device type
  - Serial number for each device
  - Calibration bytes for factory calibrated peripherals
- User signature row
  - One flash page in size
  - Can be read and written from software
  - Content is kept after chip erase

7.2 Overview

The Atmel AVR architecture has two main memory spaces, the program memory and the data memory. Executable code can reside only in the program memory, while data can be stored in the program memory and the data memory. The data memory includes the internal SRAM, and EEPROM for nonvolatile data storage. All memory spaces are linear and require no memory bank switching. Nonvolatile memory (NVM) spaces can be locked for further write and read/write operations. This prevents unrestricted access to the application software.

A separate memory section contains the fuse bytes. These are used for configuring important system functions, and can only be written by an external programmer.

The available memory size configurations are shown in “Ordering information” on page 2. In addition, each device has a Flash memory signature row for calibration data, device identification, serial number etc.

7.3 Flash program memory

The Atmel AVR XMEGA devices contain on-chip, in-system reprogrammable flash memory for program storage. The flash memory can be accessed for read and write from an external programmer through the PDI or from application software running in the device.

All AVR CPU instructions are 16 or 32 bits wide, and each flash location is 16 bits wide. The flash memory is organized in two main sections, the application section and the boot loader section. The sizes of the different sections are fixed, but

device-dependent. These two sections have separate lock bits, and can have different levels of protection. The store program memory (SPM) instruction, which is used to write to the flash from the application software, will only operate when executed from the boot loader section.

The application section contains an application table section with separate lock settings. This enables safe storage of nonvolatile data in the program memory.

Figure 7-1. Flash program memory (Hexadecimal address).

	Word address					
ATxmega	**32D3**	**64D3**	**128D3**	**192D3**	**256D3**	**384D3**
Application section (32K/64K/128K/192K/256K/384K)	0	0	0	0	0	0
...						
	37FF	77FF	EFFF	16FFF	1EFFF	2EFFF
Application table section (4K/4K/8K/8K/8K/8K)	3800	7800	F000	17000	1F000	2F000
	3FFF	7FFF	FFFF	17FFF	1FFFF	2FFFF
Boot section (4K/4K/8K/8K/8K/8K)	4000	8000	10000	18000	20000	30000
	47FF	87FF	10FFF	18FFF	20FFF	30FFF

7.3.1 Application section

The Application section is the section of the flash that is used for storing the executable application code. The protection level for the application section can be selected by the boot lock bits for this section. The application section can not store any boot loader code since the SPM instruction cannot be executed from the application section.

7.3.2 Application table section

The application table section is a part of the application section of the flash memory that can be used for storing data. The size is identical to the boot loader section. The protection level for the application table section can be selected by the boot lock bits for this section. The possibilities for different protection levels on the application section and the application table section enable safe parameter storage in the program memory. If this section is not used for data, application code can reside here.

7.3.3 Boot loader section

While the application section is used for storing the application code, the boot loader software must be located in the boot loader section because the SPM instruction can only initiate programming when executing from this section. The SPM instruction can access the entire flash, including the boot loader section itself. The protection level for the boot loader section can be selected by the boot loader lock bits. If this section is not used for boot loader software, application code can be stored here.

7.3.4 Production signature row

The production signature row is a separate memory section for factory programmed data. It contains calibration data for functions such as oscillators and analog modules. Some of the calibration values will be automatically loaded to the corresponding module or peripheral unit during reset. Other values must be loaded from the signature row and written to the corresponding peripheral registers from software. For details on calibration conditions, refer to “Electrical characteristics” on page 63.

The production signature row also contains an ID that identifies each microcontroller device type and a serial number for each manufactured device. The serial number consists of the production lot number, wafer number, and wafer coordinates for the device. The device ID for the available devices is shown in Table 7-1.

The production signature row cannot be written or erased, but it can be read from application software and external programmers.

Table 7-1. Device ID bytes.

Device	Device ID bytes		
	Byte 2	Byte 1	Byte 0
ATxmega32D3	4A	95	1E
ATxmega64D3	4A	96	1E
ATxmega128D3	48	97	1E
ATxmega192D3	49	97	1E
ATxmega256D3	44	98	1E
ATxmega384D3	47	98	1E

7.3.5 User signature row

The user signature row is a separate memory section that is fully accessible (read and write) from application software and external programmers. It is one flash page in size, and is meant for static user parameter storage, such as calibration data, custom serial number, identification numbers, random number seeds, etc. This section is not erased by chip erase commands that erase the flash, and requires a dedicated erase command. This ensures parameter storage during multiple program/erase operations and on-chip debug sessions.

7.4 Fuses and lock bits

The fuses are used to configure important system functions, and can only be written from an external programmer. The application software can read the fuses. The fuses are used to configure reset sources such as brownout detector and watchdog, and startup configuration.

The lock bits are used to set protection levels for the different flash sections (that is, if read and/or write access should be blocked). Lock bits can be written by external programmers and application software, but only to stricter protection levels. Chip erase is the only way to erase the lock bits. To ensure that flash contents are protected even during chip erase, the lock bits are erased after the rest of the flash memory has been erased.

An unprogrammed fuse or lock bit will have the value one, while a programmed fuse or lock bit will have the value zero.

Both fuses and lock bits are reprogrammable like the flash program memory.

7.5 Data memory

The data memory contains the I/O memory, internal SRAM, optionally memory mapped EEPROM, and external memory if available. The data memory is organized as one continuous memory section, see Figure 7-2 on page 15. To simplify development, I/O Memory, EEPROM and SRAM will always have the same start addresses for all Atmel AVR XMEGA devices.

Figure 7-2. Data memory map (hexadecimal address).

Byte address	ATxmega32D3
0	I/O registers (4K)
FFF	
1000	EEPROM (2K)
17FF	
	RESERVED
2000	Internal SRAM (4K)
2FFF	

Byte address	ATxmega64D3
0	I/O registers (4K)
FFF	
1000	EEPROM (2K)
17FF	
	RESERVED
2000	Internal SRAM (4K)
2FFF	

Byte address	ATxmega128D3
0	I/O registers (4K)
FFF	
1000	EEPROM (2K)
17FF	
	RESERVED
2000	Internal SRAM (8K)
3FFF	

Byte address	ATxmega192D3
0	I/O registers (4K)
FFF	
1000	EEPROM (2K)
17FF	
	RESERVED
2000	Internal SRAM (16K)
5FFF	

Byte address	ATxmega256D3
0	I/O registers (4K)
FFF	
1000	EEPROM (4K)
1FFF	
2000	Internal SRAM (16K)
5FFF	

Byte address	ATxmega384D3
0	I/O registers (4K)
FFF	
1000	EEPROM (4K)
1FFF	
2000	Internal SRAM (32K)
9FFF	

7.6 EEPROM

All devices have EEPROM for nonvolatile data storage. It is either addressable in a separate data space (default) or memory mapped and accessed in normal data space. The EEPROM supports both byte and page access. Memory mapped EEPROM allows highly efficient EEPROM reading and EEPROM buffer loading. When doing this, EEPROM is accessible using load and store instructions. Memory mapped EEPROM will always start at hexadecimal address 0x1000.

7.7 I/O memory

The status and configuration registers for peripherals and modules, including the CPU, are addressable through I/O memory locations. All I/O locations can be accessed by the load (LD/LDS/LDD) and store (ST/STS/STD) instructions, which are used to transfer data between the 32 registers in the register file and the I/O memory. The IN and OUT instructions can address I/O memory locations in the range of 0x00 to 0x3F directly. In the address range 0x00 - 0x1F, single-cycle instructions for manipulation and checking of individual bits are available.

The I/O memory address for all peripherals and modules is shown in the "Peripheral module address map" on page 54.

7.7.1 General purpose I/O registers

The lowest 16 I/O memory addresses are reserved as general purpose I/O registers. These registers can be used for storing global variables and flags, as they are directly bit-accessible using the SBI, CBI, SBIS, and SBIC instructions.

7.8 Memory timing

Read and write access to the I/O memory takes one CPU clock cycle. A write to SRAM takes one cycle, and a read from SRAM takes two cycles. EEPROM page load (write) takes one cycle, and three cycles are required for read. For burst read, new data are available every second cycle. Refer to the instruction summary for more details on instructions and instruction timing.

7.9 Device ID and revision

Each device has a three-byte device ID. This ID identifies Atmel as the manufacturer of the device and the device type. A separate register contains the revision number of the device.

7.10 I/O memory protection

Some features in the device are regarded as critical for safety in some applications. Due to this, it is possible to lock the I/O register related to the clock system, the event system, and the advanced waveform extensions. As long as the lock is enabled, all related I/O registers are locked and they can not be written from the application software. The lock registers themselves are protected by the configuration change protection mechanism.

7.11 Flash and EEPROM page size

The flash program memory and EEPROM data memory are organized in pages. The pages are word accessible for the flash and byte accessible for the EEPROM.

Table 7-2 on page 17 shows the Flash Program Memory organization and Program Counter (PC) size. Flash write and erase operations are performed on one page at a time, while reading the Flash is done one byte at a time. For Flash access the Z-pointer (Z[m:n]) is used for addressing. The most significant bits in the address (FPAGE) give the page number and the least significant address bits (FWORD) give the word in the page.

Table 7-2. Number of words and pages in the flash TBD.

Devices	PC size	Flash size	Page size	FWORD	FPAGE	Application		Boot	
	[bits]	[bytes]	[words]			Size	No. of pages	Size	No. of pages
ATxmega32D3	15	32K + 4K	128	Z[7:1]	Z[15:7]	32K	128	4K	16
ATxmega64D3	16	64K + 4K	128	Z[7:1]	Z[16:9]	64K	256	4K	16
ATxmega128D3	17	128K + 8K	256	Z[8:1]	Z[17:9]	128K	256	8K	16
ATxmega192D3	17	192K + 8K	256	Z[8:1]	Z[17:9]	192K	384	8K	16
ATxmega256D3	18	256K + 8K	256	Z[8:1]	Z[18:9]	256K	512	8K	16
ATxmega384D3	18	384K + 8K	256	Z[8:1]	Z[19:9]	384K	768	8K	16

Table 7-3 shows EEPROM memory organization. EEEPROM write and erase operations can be performed one page or one byte at a time, while reading the EEPROM is done one byte at a time. For EEPROM access the NVM address register (ADDR[m:n]) is used for addressing. The most significant bits in the address (E2PAGE) give the page number and the least significant address bits (E2BYTE) give the byte in the page.

Table 7-3. Number of bytes and pages in the EEPROM.

Devices	EEPROM	Page size	E2BYTE	E2PAGE	No. of pages
	size	**[bytes]**			
ATxmega32D3	2K	32	ADDR[4:0]	ADDR[10:5]	64
ATxmega64D3	2K	32	ADDR[4:0]	ADDR[10:5]	64
ATxmega128D3	2K	32	ADDR[4:0]	ADDR[10:5]	64
ATxmega192D3	2K	32	ADDR[4:0]	ADDR[10:5]	64
ATxmega256D3	4K	32	ADDR[4:0]	ADDR[11:5]	128
ATxmega384D3	4K	32	ADDR[4:0]	ADDR[11:5]	128

8. Event system

8.1 Features

- System for direct peripheral-to-peripheral communication and signaling
- Peripherals can directly send, receive, and react to peripheral events
  - CPU independent operation
  - 100% predictable signal timing
  - Short and guaranteed response time
- Four event channels for up to four different and parallel signal routing configurations
- Events can be sent and/or used by most peripherals, clock system, and software
- Additional functions include
  - Quadrature decoders
  - Digital filtering of I/O pin state
- Works in active mode and idle sleep mode

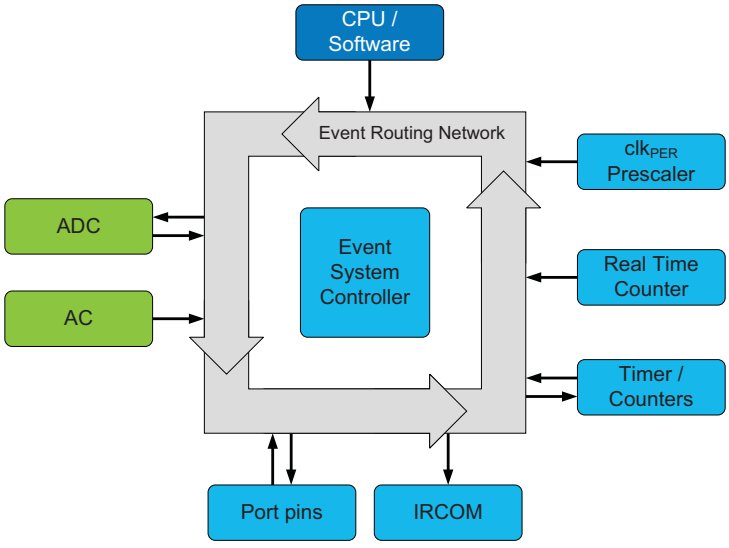
8.2 Overview

The event system enables direct peripheral-to-peripheral communication and signaling. It allows a change in one peripheral's state to automatically trigger actions in other peripherals. It is designed to provide a predictable system for short and predictable response times between peripherals. It allows for autonomous peripheral control and interaction without the use of interrupts or CPU resources, and is thus a powerful tool for reducing the complexity, size and execution time of application code. It also allows for synchronized timing of actions in several peripheral modules.

A change in a peripheral's state is referred to as an event, and usually corresponds to the peripheral's interrupt conditions. Events can be directly passed to other peripherals using a dedicated routing network called the event routing network. How events are routed and used by the peripherals is configured in software.

Figure 8-1 shows a basic diagram of all connected peripherals. The event system can directly connect together analog to digital converter, analog comparators, I/O port pins, the real-time counter, timer/counters, and IR communication module (IRCOM). Events can also be generated from software and the peripheral clock.

Figure 8-1. Event system overview and connected peripherals.



The event routing network consists of four software-configurable multiplexers that control how events are routed and used. These are called event channels, and allow for up to four parallel event routing configurations. The maximum routing latency is two peripheral clock cycles. The event system works in both active mode and idle sleep mode.

9. System clock and clock options

9.1 Features

- Fast start-up time
- Safe run-time clock switching
- Internal oscillators:
  - 32MHz run-time calibrated and tuneable oscillator
  - 2MHz run-time calibrated oscillator
  - 32.768kHz calibrated oscillator
  - 32kHz ultra low power (ULP) oscillator with 1kHz output
- External clock options
  - 0.4MHz - 16MHz crystal oscillator
  - 32.768kHz crystal oscillator
  - External clock
- PLL with 20MHz - 128MHz output frequency
  - Internal and external clock options and 1× to 31× multiplication
  - Lock detector
- Clock prescalers with 1× to 2048× division
- Fast peripheral clocks running at two and four times the CPU clock
- Automatic run-time calibration of internal oscillators
- External oscillator and PLL lock failure detection with optional non-maskable interrupt

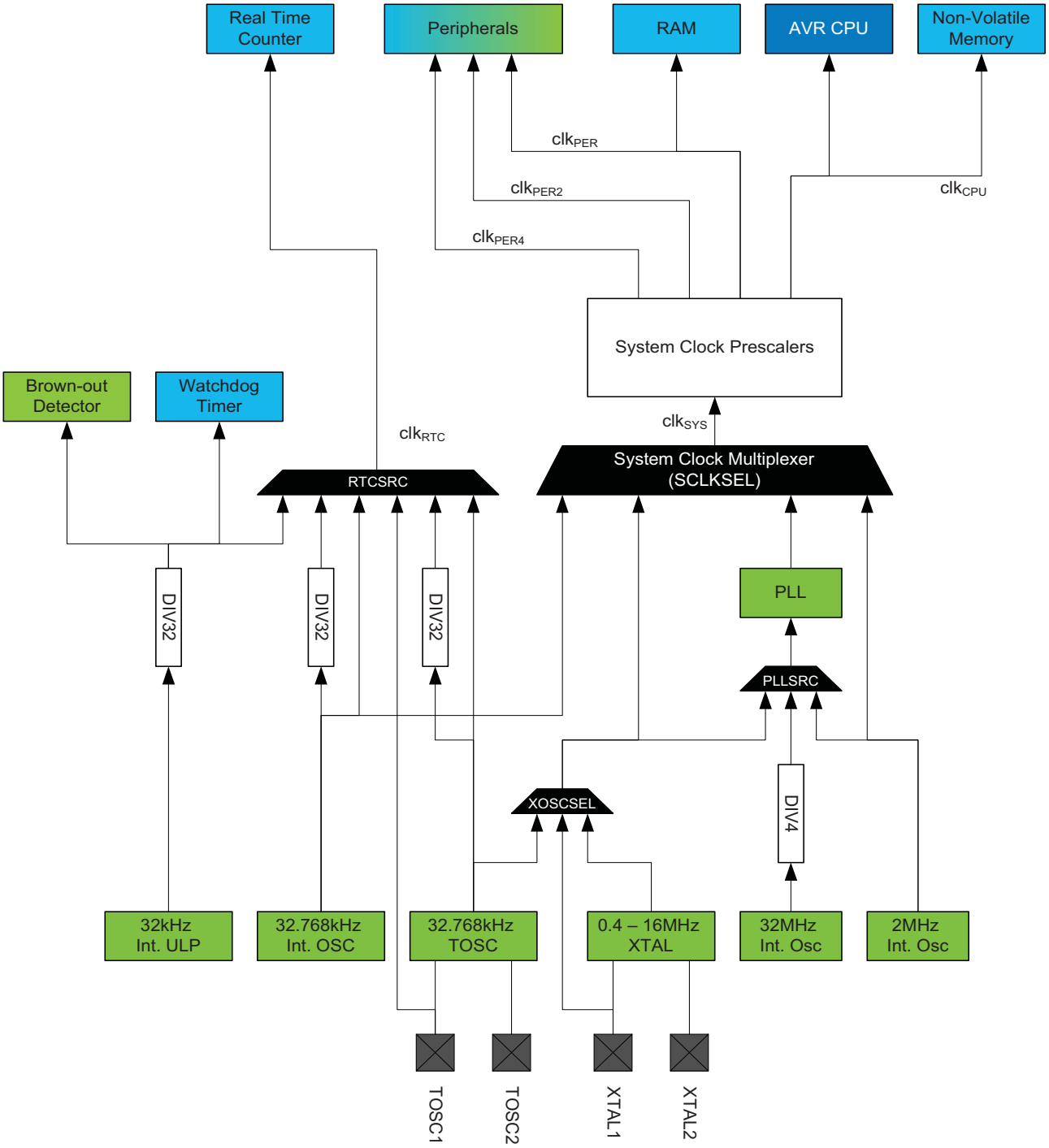
9.2 Overview

Atmel AVR XMEGA D3 devices have a flexible clock system supporting a large number of clock sources. It incorporates both accurate internal oscillators and external crystal oscillator and resonator support. A high-frequency phase locked loop (PLL) and clock prescalers can be used to generate a wide range of clock frequencies. A calibration feature (DFLL) is available, and can be used for automatic run-time calibration of the internal oscillators to remove frequency drift over voltage and temperature. An oscillator failure monitor can be enabled to issue a non-maskable interrupt and switch to the internal oscillator if the external oscillator or PLL fails.

When a reset occurs, all clock sources except the 32kHz ultra low power oscillator are disabled. After reset, the device will always start up running from the 2MHz internal oscillator. During normal operation, the system clock source and prescalers can be changed from software at any time.

Figure 9-1 on page 20 presents the principal clock system. Not all of the clocks need to be active at a given time. The clocks for the CPU and peripherals can be stopped using sleep modes and power reduction registers, as described in “Power management and sleep modes” on page 22.

Figure 9-1. The clock system, clock sources and clock distribution.



9.3 Clock sources

The clock sources are divided in two main groups: internal oscillators and external clock sources. Most of the clock sources can be directly enabled and disabled from software, while others are automatically enabled or disabled, depending on peripheral settings. After reset, the device starts up running from the 2MHz internal oscillator. The other clock sources, DFLLs and PLL, are turned off by default.

The internal oscillators do not require any external components to run. For details on characteristics and accuracy of the internal oscillators, refer to the device datasheet.

9.3.1 32kHz ultra low power internal oscillator

This oscillator provides an approximate 32kHz clock. The 32kHz ultra low power (ULP) internal oscillator is a very low power clock source, and it is not designed for high accuracy. The oscillator employs a built-in prescaler that provides a 1kHz output. The oscillator is automatically enabled/disabled when it is used as clock source for any part of the device. This oscillator can be selected as the clock source for the RTC.

9.3.2 32.768kHz calibrated internal oscillator

This oscillator provides an approximate 32.768kHz clock. It is calibrated during production to provide a default frequency close to its nominal frequency. The calibration register can also be written from software for run-time calibration of the oscillator frequency. The oscillator employs a built-in prescaler, which provides both a 32.768kHz output and a 1.024kHz output.

9.3.3 32.768kHz crystal oscillator

A 32.768kHz crystal oscillator can be connected between the TOSC1 and TOSC2 pins and enables a dedicated low frequency oscillator input circuit. A low power mode with reduced voltage swing on TOSC2 is available. This oscillator can be used as a clock source for the system clock and RTC, and as the DFLL reference clock.

9.3.4 0.4 - 16MHz crystal oscillator

This oscillator can operate in four different modes optimized for different frequency ranges, all within 0.4 - 16MHz.

9.3.5 2MHz run-time calibrated internal oscillator

The 2MHz run-time calibrated internal oscillator is the default system clock source after reset. It is calibrated during production to provide a default frequency close to its nominal frequency. A DFLL can be enabled for automatic run-time calibration of the oscillator to compensate for temperature and voltage drift and optimize the oscillator accuracy.

9.3.6 32MHz run-time calibrated internal oscillator

The 32MHz run-time calibrated internal oscillator is a high-frequency oscillator. It is calibrated during production to provide a default frequency close to its nominal frequency. A digital frequency looked loop (DFLL) can be enabled for automatic run-time calibration of the oscillator to compensate for temperature and voltage drift and optimize the oscillator accuracy. This oscillator can also be adjusted and calibrated to any frequency between 30MHz and 55MHz.

9.3.7 External clock sources

The XTAL1 and XTAL2 pins can be used to drive an external oscillator, either a quartz crystal or a ceramic resonator. XTAL1 can be used as input for an external clock signal. The TOSC1 and TOSC2 pins is dedicated to driving a 32.768kHz crystal oscillator.

9.3.8 PLL with 1x-31x multiplication factor

The built-in phase locked loop (PLL) can be used to generate a high-frequency system clock. The PLL has a user-selectable multiplication factor of from 1 to 31. In combination with the prescalers, this gives a wide range of output frequencies from all clock sources.

10. Power management and sleep modes

10.1 Features

- Power management for adjusting power consumption and functions
- Five sleep modes
  - Idle
  - Power down
  - Power save
  - Standby
  - Extended standby
- Power reduction register to disable clock and turn off unused peripherals in active and idle modes

10.2 Overview

Various sleep modes and clock gating are provided in order to tailor power consumption to application requirements. This enables the Atmel AVR XMEGA microcontroller to stop unused modules to save power.

All sleep modes are available and can be entered from active mode. In active mode, the CPU is executing application code. When the device enters sleep mode, program execution is stopped and interrupts or a reset is used to wake the device again. The application code decides which sleep mode to enter and when. Interrupts from enabled peripherals and all enabled reset sources can restore the microcontroller from sleep to active mode.

In addition, power reduction registers provide a method to stop the clock to individual peripherals from software. When this is done, the current state of the peripheral is frozen, and there is no power consumption from that peripheral. This reduces the power consumption in active mode and idle sleep modes and enables much more fine-tuned power management than sleep modes alone.

10.3 Sleep modes

Sleep modes are used to shut down modules and clock domains in the microcontroller in order to save power. XMEGA microcontrollers have five different sleep modes tuned to match the typical functional stages during application execution. A dedicated sleep instruction (SLEEP) is available to enter sleep mode. Interrupts are used to wake the device from sleep, and the available interrupt wake-up sources are dependent on the configured sleep mode. When an enabled interrupt occurs, the device will wake up and execute the interrupt service routine before continuing normal program execution from the first instruction after the SLEEP instruction. If other, higher priority interrupts are pending when the wake-up occurs, their interrupt service routines will be executed according to their priority before the interrupt service routine for the wake-up interrupt is executed. After wake-up, the CPU is halted for four cycles before execution starts.

The content of the register file, SRAM and registers are kept during sleep. If a reset occurs during sleep, the device will reset, start up, and execute from the reset vector.

10.3.1 Idle mode

In idle mode the CPU and nonvolatile memory are stopped (note that any ongoing programming will be completed), but all peripherals, including the interrupt controller and event system are kept running. Any enabled interrupt will wake the device.

10.3.2 Power-down mode

In power-down mode, all clocks, including the real-time counter clock source, are stopped. This allows operation only of asynchronous modules that do not require a running clock. The only interrupts that can wake up the MCU are the two-wire interface address match interrupt and asynchronous port interrupts.

10.3.3 Power-save mode

Power-save mode is identical to power down, with one exception. If the real-time counter (RTC) is enabled, it will keep running during sleep, and the device can also wake up from either an RTC overflow or compare match interrupt.

10.3.4 Standby mode

Standby mode is identical to power down, with the exception that the enabled system clock sources are kept running while the CPU, peripheral, and RTC clocks are stopped. This reduces the wake-up time.

10.3.5 Extended standby mode

Extended standby mode is identical to power-save mode, with the exception that the enabled system clock sources are kept running while the CPU and peripheral clocks are stopped. This reduces the wake-up time.

11. System control and reset

11.1 Features

- Reset the microcontroller and set it to initial state when a reset source goes active
- Multiple reset sources that cover different situations
  - Power-on reset
  - External reset
  - Watchdog reset
  - Brownout reset
  - PDI reset
  - Software reset
- Asynchronous operation
  - No running system clock in the device is required for reset
- Reset status register for reading the reset source from the application code

11.2 Overview

The reset system issues a microcontroller reset and sets the device to its initial state. This is for situations where operation should not start or continue, such as when the microcontroller operates below its power supply rating. If a reset source goes active, the device enters and is kept in reset until all reset sources have released their reset. The I/O pins are immediately tri-stated. The program counter is set to the reset vector location, and all I/O registers are set to their initial values. The SRAM content is kept. However, if the device accesses the SRAM when a reset occurs, the content of the accessed location can not be guaranteed.

After reset is released from all reset sources, the default oscillator is started and calibrated before the device starts running from the reset vector address. By default, this is the lowest program memory address, 0, but it is possible to move the reset vector to the lowest address in the boot section.

The reset functionality is asynchronous, and so no running system clock is required to reset the device. The software reset feature makes it possible to issue a controlled system reset from the user software.

The reset status register has individual status flags for each reset source. It is cleared at power-on reset, and shows which sources have issued a reset since the last power-on.

11.3 Reset sequence

A reset request from any reset source will immediately reset the device and keep it in reset as long as the request is active. When all reset requests are released, the device will go through three stages before the device starts running again:

- Reset counter delay
- Oscillator startup
- Oscillator calibration

If another reset requests occurs during this process, the reset sequence will start over again.

11.4 Reset sources

11.4.1 Power-on reset

A power-on reset (POR) is generated by an on-chip detection circuit. The POR is activated when the V_{CC} rises and reaches the POR threshold voltage (V_{POT}), and this will start the reset sequence.

The POR is also activated to power down the device properly when the V_{CC} falls and drops below the V_{POT} level.

The V_{POT} level is higher for falling V_{CC} than for rising V_{CC}. Consult the datasheet for POR characteristics data.

11.4.2 Brownout detection

The on-chip brownout detection (BOD) circuit monitors the V_{CC} level during operation by comparing it to a fixed, programmable level that is selected by the BODLEVEL fuses. If disabled, BOD is forced on at the lowest level during chip erase and when the PDI is enabled.

11.4.3 External reset

The external reset circuit is connected to the external $\overline{\text{RESET}}$ pin. The external reset will trigger when the $\overline{\text{RESET}}$ pin is driven below the $\overline{\text{RESET}}$ pin threshold voltage, V_{RST}, for longer than the minimum pulse period, t_{EXT}. The reset will be held as long as the pin is kept low. The $\overline{\text{RESET}}$ pin includes an internal pull-up resistor.

11.4.4 Watchdog reset

The watchdog timer (WDT) is a system function for monitoring correct program operation. If the WDT is not reset from the software within a programmable timeout period, a watchdog reset will be given. The watchdog reset is active for one to two clock cycles of the 2MHz internal oscillator. For more details see “WDT – Watchdog Timer” on page 26.

11.4.5 Software reset

The software reset makes it possible to issue a system reset from software by writing to the software reset bit in the reset control register.The reset will be issued within two CPU clock cycles after writing the bit. It is not possible to execute any instruction from when a software reset is requested until it is issued.

11.4.6 Program and debug interface reset

The program and debug interface reset contains a separate reset source that is used to reset the device during external programming and debugging. This reset source is accessible only from external debuggers and programmers.

12. WDT – Watchdog Timer

12.1 Features

- Issues a device reset if the timer is not reset before its timeout period
- Asynchronous operation from dedicated oscillator
- 1kHz output of the 32kHz ultra low power oscillator
- 11 selectable timeout periods, from 8ms to 8s
- Two operation modes:
  - Normal mode
  - Window mode
- Configuration lock to prevent unwanted changes

12.2 Overview

The watchdog timer (WDT) is a system function for monitoring correct program operation. It makes it possible to recover from error situations such as runaway or deadlocked code. The WDT is a timer, configured to a predefined timeout period, and is constantly running when enabled. If the WDT is not reset within the timeout period, it will issue a microcontroller reset. The WDT is reset by executing the WDR (watchdog timer reset) instruction from the application code.

The window mode makes it possible to define a time slot or window inside the total timeout period during which WDT must be reset. If the WDT is reset outside this window, either too early or too late, a system reset will be issued. Compared to the normal mode, this can also catch situations where a code error causes constant WDR execution.

The WDT will run in active mode and all sleep modes, if enabled. It is asynchronous, runs from a CPU-independent clock source, and will continue to operate to issue a system reset even if the main clocks fail.

The configuration change protection mechanism ensures that the WDT settings cannot be changed by accident. For increased safety, a fuse for locking the WDT settings is also available.

13. Interrupts and programmable multilevel interrupt controller

13.1 Features

- Short and predictable interrupt response time
- Separate interrupt configuration and vector address for each interrupt
- Programmable multilevel interrupt controller
  - Interrupt prioritizing according to level and vector address
  - Three selectable interrupt levels for all interrupts: low, medium, and high
  - Selectable, round-robin priority scheme within low-level interrupts
  - Non-maskable interrupts for critical functions
- Interrupt vectors optionally placed in the application section or the boot loader section

13.2 Overview

Interrupts signal a change of state in peripherals, and this can be used to alter program execution. Peripherals can have one or more interrupts, and all are individually enabled and configured. When an interrupt is enabled and configured, it will generate an interrupt request when the interrupt condition is present. The programmable multilevel interrupt controller (PMIC) controls the handling and prioritizing of interrupt requests. When an interrupt request is acknowledged by the PMIC, the program counter is set to point to the interrupt vector, and the interrupt handler can be executed.

All peripherals can select between three different priority levels for their interrupts: low, medium, and high. Interrupts are prioritized according to their level and their interrupt vector address. Medium-level interrupts will interrupt low-level interrupt handlers. High-level interrupts will interrupt both medium- and low-level interrupt handlers. Within each level, the interrupt priority is decided from the interrupt vector address, where the lowest interrupt vector address has the highest interrupt priority. Low-level interrupts have an optional round-robin scheduling scheme to ensure that all interrupts are serviced within a certain amount of time.

Non-maskable interrupts (NMI) are also supported, and can be used for system critical functions.

13.3 Interrupt vectors

The interrupt vector is the sum of the peripheral's base interrupt address and the offset address for specific interrupts in each peripheral. The base addresses for the Atmel AVR XMEGA D3 devices are shown in Table 13-1 on page 28. Offset addresses for each interrupt available in the peripheral are described for each peripheral in the XMEGA D manual. For peripherals or modules that have only one interrupt, the interrupt vector is shown in Table 13-1 on page 28. The program address is the word address.

Table 13-1. Reset and interrupt vectors.

Program address (base address)	Source	Interrupt description
0x000	RESET	
0x002	OSCF_INT_vect	Crystal oscillator failure interrupt vector (NMI)
0x004	PORTC_INT_base	Port C interrupt base
0x008	PORTR_INT_base	Port R interrupt base
0x014	RTC_INT_base	Real Time Counter Interrupt base
0x018	TWIC_INT_base	Two-Wire Interface on Port C Interrupt base
0x01C	TCC0_INT_base	Timer/Counter 0 on port C Interrupt base
0x028	TCC1_INT_base	Timer/Counter 1 on port C Interrupt base
0x030	SPIC_INT_vect	SPI on port C Interrupt vector
0x032	USARTC0_INT_base	USART 0 on port C Interrupt base
0x040	NVM_INT_base	Non-Volatile Memory Interrupt base
0x044	PORTB_INT_base	Port B Interrupt base
0x056	PORTE_INT_base	Port E INT base
0x05A	TWIE_INT_base	Two-Wire Interface on Port E Interrupt base
0x05E	TCE0_INT_base	Timer/Counter 0 on port E Interrupt base
0x074	USARTE0_INT_base	USART 0 on port E Interrupt base
0x080	PORTD_INT_base	Port D Interrupt base
0x084	PORTA_INT_base	Port A Interrupt base
0x088	ACA_INT_base	Analog Comparator on Port A Interrupt base
0x08E	ADCA_INT_base	Analog to Digital Converter on Port A Interrupt base
0x09A	TCD0_INT_base	Timer/Counter 0 on port D Interrupt base
0x0AE	SPID_INT_vector	SPI D Interrupt vector
0x0B0	USARTD0_INT_base	USART 0 on port D Interrupt base
0x0B6	USARTD1_INT_base	USART 1 on port D Interrupt base
0x0D0	PORTF_INT_base	Port F Interrupt base
0x0D8	TCF0_INT_base	Timer/Counter 0 on port F Interrupt base

14. I/O ports

14.1 Features

- 50 general purpose input and output pins with individual configuration
- Output driver with configurable driver and pull settings:
  - Totem-pole
  - Wired-AND
  - Wired-OR
  - Bus-keeper
  - Inverted I/O
- Input with synchronous and/or asynchronous sensing with interrupts and events
  - Sense both edges
  - Sense rising edges
  - Sense falling edges
  - Sense low level
- Optional pull-up and pull-down resistor on input and Wired-OR/AND configuration
- Asynchronous pin change sensing that can wake the device from all sleep modes
- Two port interrupts with pin masking per I/O port
- Efficient and safe access to port pins
  - Hardware read-modify-write through dedicated toggle/clear/set registers
  - Configuration of multiple pins in a single operation
  - Mapping of port registers into bit-accessible I/O memory space
- Peripheral clocks output on port pin
- Real-time counter clock output to port pin
- Event channels can be output on port pin
- Remapping of digital peripheral pin functions
  - Selectable USART, SPI, and timer/counter input/output pin locations

14.2 Overview

One port consists of up to eight port pins: pin 0 to 7. Each port pin can be configured as input or output with configurable driver and pull settings. They also implement synchronous and asynchronous input sensing with interrupts and events for selectable pin change conditions. Asynchronous pin-change sensing means that a pin change can wake the device from all sleep modes, included the modes where no clocks are running.

All functions are individual and configurable per pin, but several pins can be configured in a single operation. The pins have hardware read-modify-write (RMW) functionality for safe and correct change of drive value and/or pull resistor configuration. The direction of one port pin can be changed without unintentionally changing the direction of any other pin.

The port pin configuration also controls input and output selection of other device functions. It is possible to have both the peripheral clock and the real-time clock output to a port pin, and available for external use. The same applies to events from the event system that can be used to synchronize and control external functions. Other digital peripherals, such as USART, SPI, and timer/counters, can be remapped to selectable pin locations in order to optimize pin-out versus application needs.

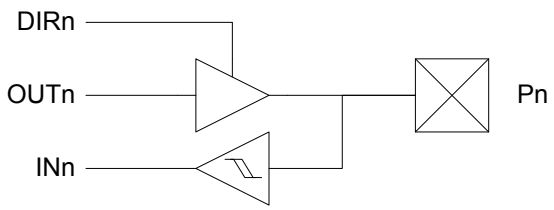
The notation of the ports are PORTA, PORTB, PORTC, PORTD, PORTE, PORTF and PORTR.

14.3 Output driver

All port pins (Pn) have programmable output configuration.

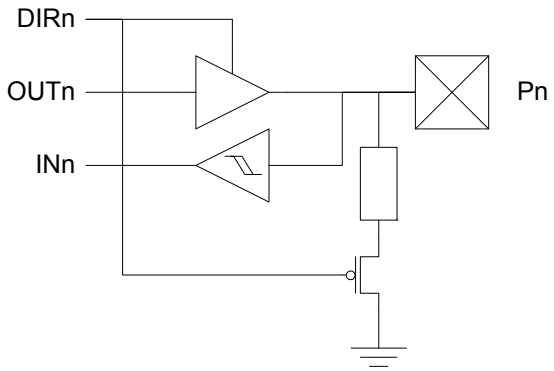
14.3.1 Push-pull

Figure 14-1. I/O configuration - Totem-pole.



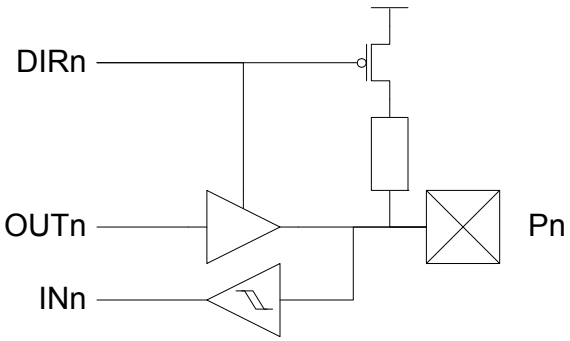
14.3.2 Pull-down

Figure 14-2. I/O configuration - Totem-pole with pull-down (on input).



14.3.3 Pull-up

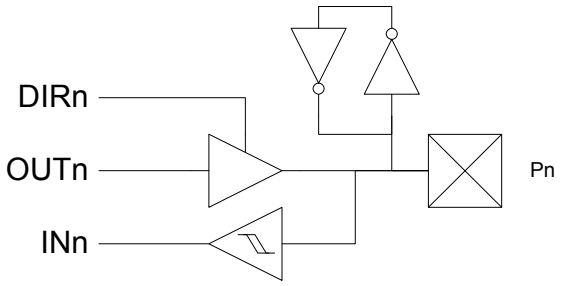
Figure 14-3. I/O configuration - Totem-pole with pull-up (on input).



14.3.4 Bus-keeper

The bus-keeper's weak output produces the same logical level as the last output level. It acts as a pull-up if the last level was '1', and pull-down if the last level was '0'.

Figure 14-4. I/O configuration - Totem-pole with bus-keeper.



14.3.5 Others

Figure 14-5. Output configuration - Wired-OR with optional pull-down.

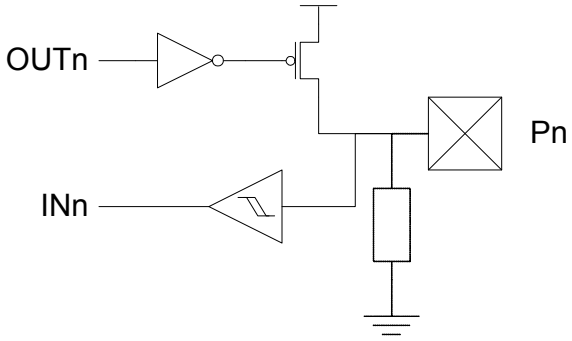
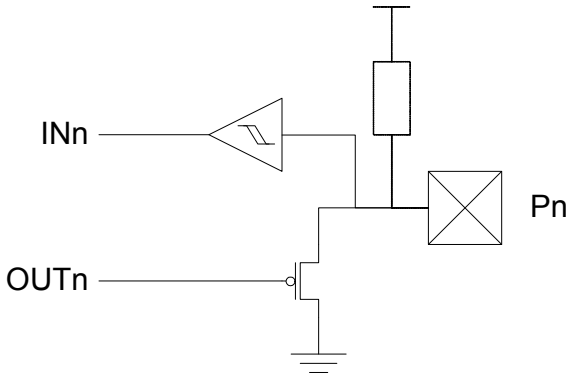


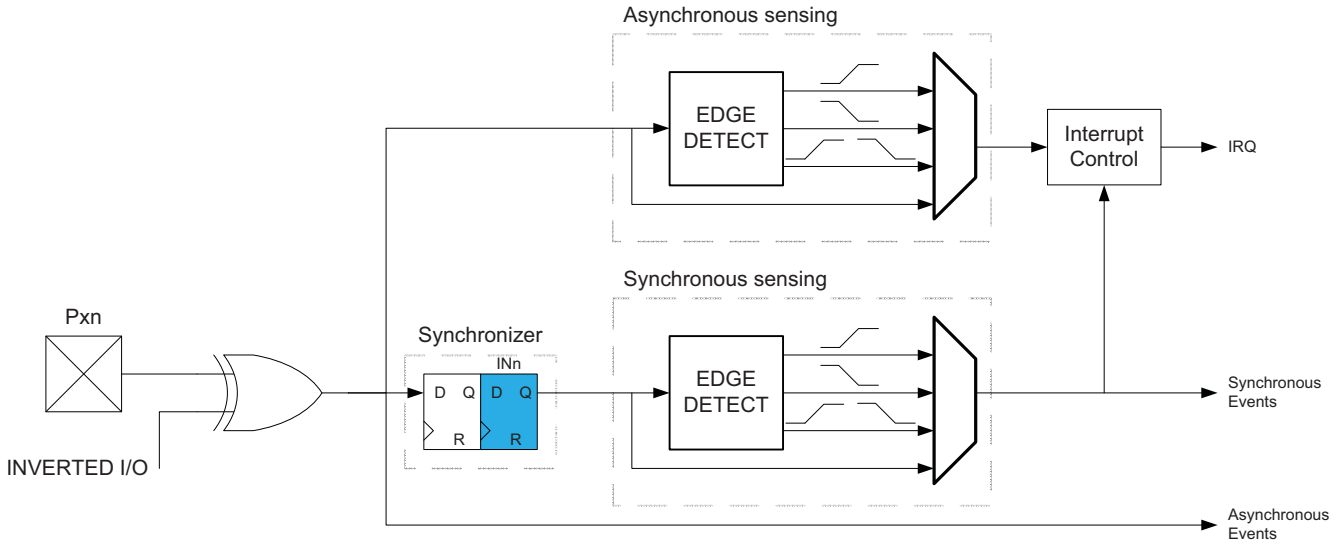
Figure 14-6. I/O configuration - Wired-AND with optional pull-up.



14.4 Input sensing

Input sensing is synchronous or asynchronous depending on the enabled clock for the ports, and the configuration is shown in Figure 14-7.

Figure 14-7. Input sensing system overview.



When a pin is configured with inverted I/O, the pin value is inverted before the input sensing.

14.5 Alternate port functions

Most port pins have alternate pin functions in addition to being a general purpose I/O pin. When an alternate function is enabled, it might override the normal port pin function or pin value. This happens when other peripherals that require pins are enabled or configured to use pins. If and how a peripheral will override and use pins is described in the section for that peripheral. “Pinout and pin functions” on page 49 shows which modules on peripherals that enable alternate functions on a pin, and which alternate functions that are available on a pin.

15. TC0/1 – 16-bit Timer/Counter Type 0 and 1

15.1 Features

- Five 16-bit timer/counters
  - Four timer/counters of type 0
  - One timer/counter of type 1
  - Split-mode enabling two 8-bit timer/counter from each timer/counter type 0
- 32-bit timer/counter support by cascading two timer/counters
- Up to four compare or capture (CC) channels
  - Four CC channels for timer/counters of type 0
  - Two CC channels for timer/counters of type 1
- Double buffered timer period setting
- Double buffered capture or compare channels
- Waveform generation:
  - Frequency generation
  - Single-slope pulse width modulation
  - Dual-slope pulse width modulation
- Input capture:
  - Input capture with noise cancelling
  - Frequency capture
  - Pulse width capture
  - 32-bit input capture
- Timer overflow and error interrupts/events
- One compare match or input capture interrupt/event per CC channel
- Can be used with event system for:
  - Quadrature decoding
  - Count and direction control
  - Capture
- High-resolution extension
  - Increases frequency and waveform resolution by 4× (2-bit) or 8× (3-bit)
- Advanced waveform extension:
  - Low- and high-side output with programmable dead-time insertion (DTI)
- Event controlled fault protection for safe disabling of drivers

15.2 Overview

Atmel AVR XMEGA D3 devices have a set of five flexible 16-bit timer/counters (TC). Their capabilities include accurate program execution timing, frequency and waveform generation, and input capture with time and frequency measurement of digital signals. Two timer/counters can be cascaded to create a 32-bit timer/counter with optional 32-bit capture.

A timer/counter consists of a base counter and a set of compare or capture (CC) channels. The base counter can be used to count clock cycles or events. It has direction control and period setting that can be used for timing. The CC channels can be used together with the base counter to do compare match control, frequency generation, and pulse width waveform modulation, as well as various input capture operations. A timer/counter can be configured for either capture or compare functions, but cannot perform both at the same time.

A timer/counter can be clocked and timed from the peripheral clock with optional prescaling or from the event system. The event system can also be used for direction control and capture trigger or to synchronize operations.

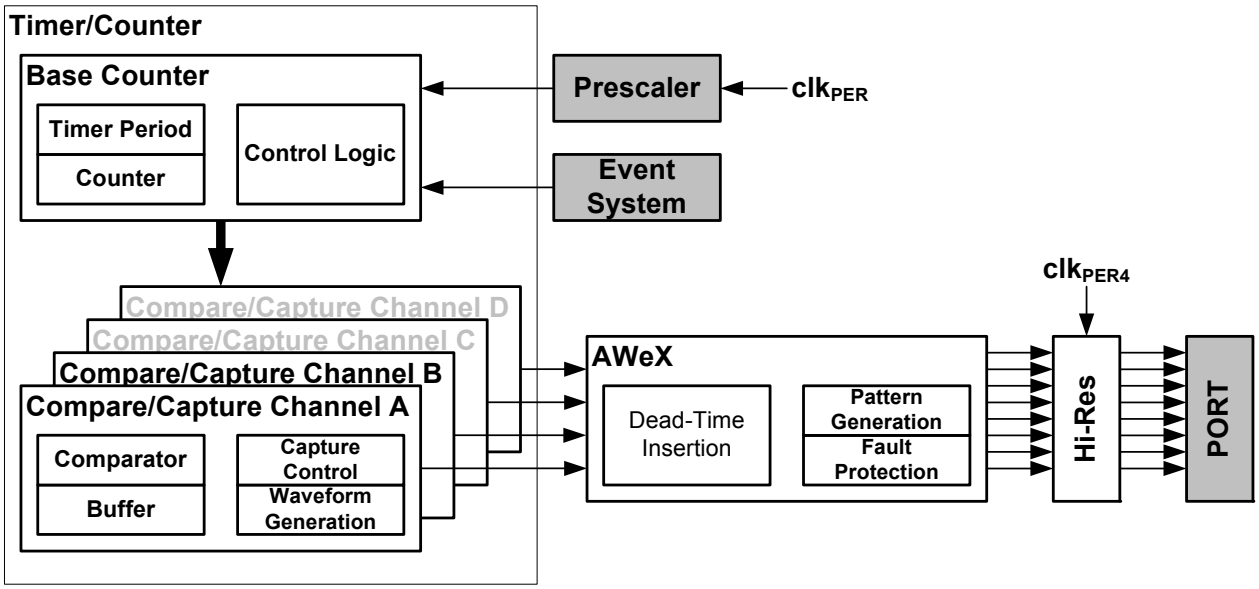
There are two differences between timer/counter type 0 and type 1. Timer/counter 0 has four CC channels, and timer/counter 1 has two CC channels. All information related to CC channels 3 and 4 is valid only for timer/counter 0. Only Timer/Counter 0 has the split mode feature that split it into two 8-bit Timer/Counters with four compare channels each.

Some timer/counters have extensions to enable more specialized waveform and frequency generation. The advanced waveform extension (AWeX) is intended for motor control and other power control applications. It enables low- and high-side output with dead-time insertion, as well as fault protection for disabling and shutting down external drivers. It can also generate a synchronized bit pattern across the port pins.

The advanced waveform extension can be enabled to provide extra and more advanced features for the Timer/Counter. This are only available for Timer/Counter 0. See “AWeX – Advanced Waveform Extension” on page 36 for more details.

The high-resolution (hi-res) extension can be used to increase the waveform output resolution by four or eight times by using an internal clock source running up to four times faster than the peripheral clock. See “Hi-Res – High Resolution Extension” on page 37 for more details.

Figure 15-1. Overview of a Timer/Counter and closely related peripherals.



PORTC has one Timer/Counter 0 and one Timer/Counter1. PORTD, PORTE and PORTF each has one Timer/Counter 0. Notation of these are TCC0 (Time/Counter C0), TCC1, TCD0, TCE0, and TCF0, respectively.

16. TC2 – Timer/Counter Type 2

16.1 Features

- Eight 8-bit timer/counters
  - Four Low-byte timer/counter
  - Four High-byte timer/counter
- Up to eight compare channels in each Timer/Counter 2
  - Four compare channels for the low-byte timer/counter
  - Four compare channels for the high-byte timer/counter
- Waveform generation
  - Single slope pulse width modulation
- Timer underflow interrupts/events
- One compare match interrupt/event per compare channel for the low-byte timer/counter
- Can be used with the event system for count control

16.2 Overview

There are four Timer/Counter 2. These are realized when a Timer/Counter 0 is set in split mode. It is then a system of two eight-bit timer/counters, each with four compare channels. This results in eight configurable pulse width modulation (PWM) channels with individually controlled duty cycles, and is intended for applications that require a high number of PWM channels.

The two eight-bit timer/counters in this system are referred to as the low-byte timer/counter and high-byte timer/counter, respectively. The difference between them is that only the low-byte timer/counter can be used to generate compare match interrupts and events. The two eight-bit timer/counters have a shared clock source and separate period and compare settings. They can be clocked and timed from the peripheral clock, with optional prescaling, or from the event system. The counters are always counting down.

PORTC, PORTD, PORTE and PORTF each has one Timer/Counter 2. Notation of these are TCC2 (Timer/Counter C2), TCD2, TCE2 and TCF2, respectively.

17. AWeX – Advanced Waveform Extension

17.1 Features

- Waveform output with complementary output from each compare channel
- Four dead-time insertion (DTI) units
  - 8-bit resolution
  - Separate high and low side dead-time setting
  - Double buffered dead time
  - Optionally halts timer during dead-time insertion
- Pattern generation unit creating synchronised bit pattern across the port pins
  - Double buffered pattern generation
  - Optional distribution of one compare channel output across the port pins
- Event controlled fault protection for instant and predictable fault triggering

17.2 Overview

The advanced waveform extension (AWeX) provides extra functions to the timer/counter in waveform generation (WG) modes. It is primarily intended for use with different types of motor control and other power control applications. It enables low- and high side output with dead-time insertion and fault protection for disabling and shutting down external drivers. It can also generate a synchronized bit pattern across the port pins.

Each of the waveform generator outputs from the timer/counter 0 are split into a complimentary pair of outputs when any AWeX features are enabled. These output pairs go through a dead-time insertion (DTI) unit that generates the non-inverted low side (LS) and inverted high side (HS) of the WG output with dead-time insertion between LS and HS switching. The DTI output will override the normal port value according to the port override setting.

The pattern generation unit can be used to generate a synchronized bit pattern on the port it is connected to. In addition, the WG output from compare channel A can be distributed to and override all the port pins. When the pattern generator unit is enabled, the DTI unit is bypassed.

The fault protection unit is connected to the event system, enabling any event to trigger a fault condition that will disable the AWeX output. The event system ensures predictable and instant fault reaction, and gives flexibility in the selection of fault triggers.

The AWeX is available for TCC0. The notation of this is AWEXC.

18. Hi-Res – High Resolution Extension

18.1 Features

- Increases waveform generator resolution up to 8× (three bits)
- Supports frequency, single-slope PWM, and dual-slope PWM generation
- Supports the AWeX when this is used for the same timer/counter

18.2 Overview

The high-resolution (hi-res) extension can be used to increase the resolution of the waveform generation output from a timer/counter by four or eight. It can be used for a timer/counter doing frequency, single-slope PWM, or dual-slope PWM generation. It can also be used with the AWeX if this is used for the same timer/counter.

The hi-res extension uses the peripheral 4× clock (Clk_{PER4}). The system clock prescalers must be configured so the peripheral 4× clock frequency is four times higher than the peripheral and CPU clock frequency when the hi-res extension is enabled.

There is one hi-res extensions that can be enabled for timer/counters pair on PORTC. The notation of this is HIRESC.

19. RTC – 16-bit Real-Time Counter

19.1 Features

- 16-bit resolution
- Selectable clock source
  - 32.768kHz external crystal
  - External clock
  - 32.768kHz internal oscillator
  - 32kHz internal ULP oscillator
- Programmable 10-bit clock prescaling
- One compare register
- One period register
- Clear counter on period overflow
- Optional interrupt/event on overflow and compare match

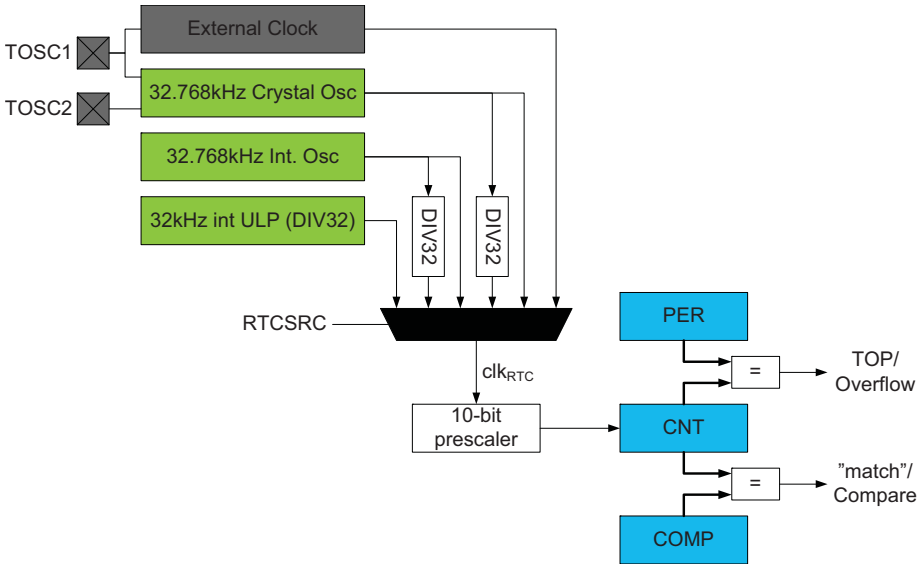
19.2 Overview

The 16-bit real-time counter (RTC) is a counter that typically runs continuously, including in low-power sleep modes, to keep track of time. It can wake up the device from sleep modes and/or interrupt the device at regular intervals.

The reference clock is typically the 1.024kHz output from a high-accuracy crystal of 32.768kHz, and this is the configuration most optimized for low power consumption. The faster 32.768kHz output can be selected if the RTC needs a resolution higher than 1ms. The RTC can also be clocked from an external clock signal, the 32.768kHz internal oscillator or the 32kHz internal ULP oscillator.

The RTC includes a 10-bit programmable prescaler that can scale down the reference clock before it reaches the counter. A wide range of resolutions and time-out periods can be configured. With a 32.768kHz clock source, the maximum resolution is 30.5µs, and time-out periods can range up to 2000 seconds. With a resolution of 1s, the maximum timeout period is more than18 hours (65536 seconds). The RTC can give a compare interrupt and/or event when the counter equals the compare register value, and an overflow interrupt and/or event when it equals the period register value.

Figure 19-1. Real-time counter overview.



20. TWI – Two-Wire Interface

20.1 Features

- Two Identical two-wire interface peripherals
- Bidirectional, two-wire communication interface
  - Phillips I^2C compatible
  - System Management Bus (SMBus) compatible
- Bus master and slave operation supported
  - Slave operation
  - Single bus master operation
  - Bus master in multi-master bus environment
  - Multi-master arbitration
- Flexible slave address match functions
  - 7-bit and general call address recognition in hardware
  - 10-bit addressing supported
  - Address mask register for dual address match or address range masking
  - Optional software address recognition for unlimited number of addresses
- Slave can operate in all sleep modes, including power-down
- Slave address match can wake device from all sleep modes
- 100kHz and 400kHz bus frequency support
- Slew-rate limited output drivers
- Input filter for bus noise and spike suppression
- Support arbitration between start/repeated start and data bit (SMBus)
- Slave arbitration allows support for address resolve protocol (ARP) (SMBus)

20.2 Overview

The two-wire interface (TWI) is a bidirectional, two-wire communication interface. It is I^2C and System Management Bus (SMBus) compatible. The only external hardware needed to implement the bus is one pull-up resistor on each bus line.

A device connected to the bus must act as a master or a slave. The master initiates a data transaction by addressing a slave on the bus and telling whether it wants to transmit or receive data. One bus can have many slaves and one or several masters that can take control of the bus. An arbitration process handles priority if more than one master tries to transmit data at the same time. Mechanisms for resolving bus contention are inherent in the protocol.

The TWI module supports master and slave functionality. The master and slave functionality are separated from each other, and can be enabled and configured separately. The master module supports multi-master bus operation and arbitration. It contains the baud rate generator. Both 100kHz and 400kHz bus frequency is supported. Quick command and smart mode can be enabled to auto-trigger operations and reduce software complexity.

The slave module implements 7-bit address match and general address call recognition in hardware. 10-bit addressing is also supported. A dedicated address mask register can act as a second address match register or as a register for address range masking. The slave continues to operate in all sleep modes, including power-down mode. This enables the slave to wake up the device from all sleep modes on TWI address match. It is possible to disable the address matching to let this be handled in software instead.

The TWI module will detect START and STOP conditions, bus collisions, and bus errors. Arbitration lost, errors, collision, and clock hold on the bus are also detected and indicated in separate status flags available in both master and slave modes.

It is possible to disable the TWI drivers in the device, and enable a four-wire digital interface for connecting to an external TWI bus driver. This can be used for applications where the device operates from a different V_{CC} voltage than used by the TWI bus.

PORTC and PORTE each has one TWI. Notation of these peripherals are TWIC and TWIE.

21. SPI – Serial Peripheral Interface

21.1 Features

- Two identical SPI peripherals
- Full-duplex, three-wire synchronous data transfer
- Master or slave operation
- Lsb first or msb first data transfer
- Eight programmable bit rates
- Interrupt flag at the end of transmission
- Write collision flag to indicate data collision
- Wake up from idle sleep mode
- Double speed master mode

21.2 Overview

The Serial Peripheral Interface (SPI) is a high-speed synchronous data transfer interface using three or four pins. It allows fast communication between an Atmel AVR XMEGA device and peripheral devices or between several microcontrollers. The SPI supports full-duplex communication.

A device connected to the bus must act as a master or slave. The master initiates and controls all data transactions.

PORTC and PORTD each has one SPI. Notation of these peripherals are SPIC and SPID, respectively.

22. USART

22.1 Features

- Three identical USART peripherals
- Full-duplex operation
- Asynchronous or synchronous operation
  - Synchronous clock rates up to 1/2 of the device clock frequency
  - Asynchronous clock rates up to 1/8 of the device clock frequency
- Supports serial frames with 5, 6, 7, 8 or 9 data bits and 1 or 2 stop bits
- Fractional baud rate generator
  - Can generate desired baud rate from any system clock frequency
  - No need for external oscillator with certain frequencies
- Built-in error detection and correction schemes
  - Odd or even parity generation and parity check
  - Data overrun and framing error detection
  - Noise filtering includes false start bit detection and digital low-pass filter
- Separate interrupts for
  - Transmit complete
  - Transmit data register empty
  - Receive complete
- Multiprocessor communication mode
  - Addressing scheme to address a specific devices on a multidevice bus
  - Enable unaddressed devices to automatically ignore all frames
- Master SPI mode
  - Double buffered operation
  - Operation up to 1/2 of the peripheral clock frequency
- IRCOM module for IrDA compliant pulse modulation/demodulation

22.2 Overview

The universal synchronous and asynchronous serial receiver and transmitter (USART) is a fast and flexible serial communication module. The USART supports full-duplex communication and asynchronous and synchronous operation. The USART can be configured to operate in SPI master mode and used for SPI communication.

Communication is frame based, and the frame format can be customized to support a wide range of standards. The USART is buffered in both directions, enabling continued data transmission without any delay between frames. Separate interrupts for receive and transmit complete enable fully interrupt driven communication. Frame error and buffer overflow are detected in hardware and indicated with separate status flags. Even or odd parity generation and parity check can also be enabled.

The clock generator includes a fractional baud rate generator that is able to generate a wide range of USART baud rates from any system clock frequencies. This removes the need to use an external crystal oscillator with a specific frequency to achieve a required baud rate. It also supports external clock input in synchronous slave operation.

When the USART is set in master SPI mode, all USART-specific logic is disabled, leaving the transmit and receive buffers, shift registers, and baud rate generator enabled. Pin control and interrupt generation are identical in both modes. The registers are used in both modes, but their functionality differs for some control settings.

An IRCOM module can be enabled for one USART to support IrDA 1.4 physical compliant pulse modulation and demodulation for baud rates up to 115.2kbps.

PORTC, PORTD, and PORTE each has one USART. Notation of these peripherals are USARTC0, USARTD0 and USARTE0, respectively.

23. IRCOM – IR Communication Module

23.1 Features

- Pulse modulation/demodulation for infrared communication
- IrDA compatible for baud rates up to 115.2kbps
- Selectable pulse modulation scheme
  - 3/16 of the baud rate period
  - Fixed pulse period, 8-bit programmable
  - Pulse modulation disabled
- Built-in filtering
- Can be connected to and used by any USART

23.2 Overview

Atmel AVR XMEGA devices contain an infrared communication module (IRCOM) that is IrDA compatible for baud rates up to 115.2kbps. It can be connected to any USART to enable infrared pulse encoding/decoding for that USART.

24. CRC – Cyclic Redundancy Check generator

24.1 Features

- Cyclic redundancy check (CRC) generation and checking for
  - Communication data
  - Program or data in flash memory
  - Data in SRAM and I/O memory space
- Integrated with flash memory and CPU
  - Automatic CRC of the complete or a selectable range of the flash memory
  - CPU can load data to the CRC generator through the I/O interface
- CRC polynomial software selectable to
  - CRC-16 (CRC-CCITT)
  - CRC-32 (IEEE 802.3)
- Zero remainder detection

24.2 Overview

A cyclic redundancy check (CRC) is an error detection technique test algorithm used to find accidental errors in data, and it is commonly used to determine the correctness of a data transmission, and data present in the data and program memories. A CRC takes a data stream or a block of data as input and generates a 16- or 32-bit output that can be appended to the data and used as a checksum. When the same data are later received or read, the device or application repeats the calculation. If the new CRC result does not match the one calculated earlier, the block contains a data error. The application will then detect this and may take a corrective action, such as requesting the data to be sent again or simply not using the incorrect data.

Typically, an n-bit CRC applied to a data block of arbitrary length will detect any single error burst not longer than n bits (any single alteration that spans no more than n bits of the data), and will detect the fraction $1-2^{-n}$ of all longer error bursts. The CRC module in Atmel AVR XMEGA devices supports two commonly used CRC polynomials; CRC-16 (CRC-CCITT) and CRC-32 (IEEE 802.3).

CRC-16:

Polynominal: $x^{16}+x^{12}+x^5+1$

Hex value: 0x1021

CRC-32:

Polynominal: $x^{32}+x^{26}+x^{23}+x^{22}+x^{16}+x^{12}+x^{11}+x^{10}+x^8+x^7+x^5+x^4+x^2+x+1$

Hex value: 0x04C11DB7

25. ADC – 12-bit Analog to Digital Converter

25.1 Features

- One Analog to Digital Converter (ADC)
- 12-bit resolution
- Up to 300 thousand samples per second
  - Down to 2.3µs conversion time with 8-bit resolution
  - Down to 3.35µs conversion time with 12-bit resolution
- Differential and single-ended input
  - 16 single-ended inputs
  - 16 * 4 differential inputs without gain
  - 8 * 4 differential input with gain
- Built-in differential gain stage
  - 1/2×, 1×, 2×, 4×, 8×, 16×, 32× and 64× gain options
- Single, continuous and scan conversion options
- Three internal inputs
  - Internal temperature sensor
  - V_{CC} voltage divided by 10
  - 1.1V bandgap voltage
- Internal and external reference options
- Compare function for accurate monitoring of user defined thresholds
- Optional event triggered conversion for accurate timing
- Optional interrupt/event on compare result

25.2 Overview

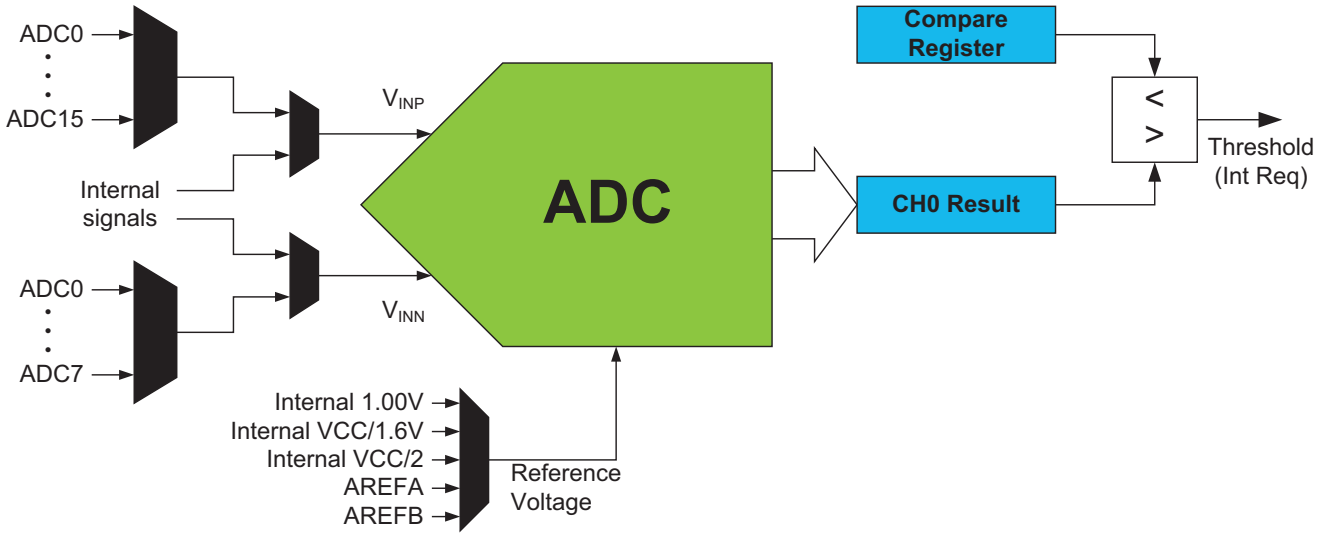
The ADC converts analog signals to digital values. The ADC has 12-bit resolution and is capable of converting up to 300 thousand samples per second (ksps). The input selection is flexible, and both single-ended and differential measurements can be done. For differential measurements, an optional gain stage is available to increase the dynamic range. In addition, several internal signal inputs are available. The ADC can provide both signed and unsigned results.

The ADC measurements can either be started by application software or an incoming event from another peripheral in the device. The ADC measurements can be started with predictable timing, and without software intervention.

Both internal and external reference voltages can be used. An integrated temperature sensor is available for use with the ADC. The V_{CC}/10 and the bandgap voltage can also be measured by the ADC.

The ADC has a compare function for accurate monitoring of user defined thresholds with minimum software intervention required.

Figure 25-1. ADC overview.



The ADC may be configured for 8- or 12-bit result, reducing the minimum conversion time (propagation delay) from 3.35µs for 12-bit to 2.3µs for 8-bit result.

ADC conversion results are provided left- or right adjusted with optional ‘1’ or ‘0’ padding. This eases calculation when the result is represented as a signed integer (signed 16-bit number).

PORTA has one ADC. Notation of this peripheral is ADCA.

26. AC – Analog Comparator

26.1 Features

- Two analog comparators (AC)
- Selectable hysteresis
  - No
  - Small
  - Large
- Analog comparator output available on pin
- Flexible input selection
  - All pins on the port
  - Bandgap reference voltage
  - A 64-level programmable voltage scaler of the internal V_{CC} voltage
- Interrupt and event generation on:
  - Rising edge
  - Falling edge
  - Toggle
- Window function interrupt and event generation on:
  - Signal above window
  - Signal inside window
  - Signal below window
- Constant current source with configurable output pin selection

26.2 Overview

The analog comparator (AC) compares the voltage levels on two inputs and gives a digital output based on this comparison. The analog comparator may be configured to generate interrupt requests and/or events upon several different combinations of input change.

The analog comparator hysteresis can be adjusted in order to achieve the optimal operation for each application.

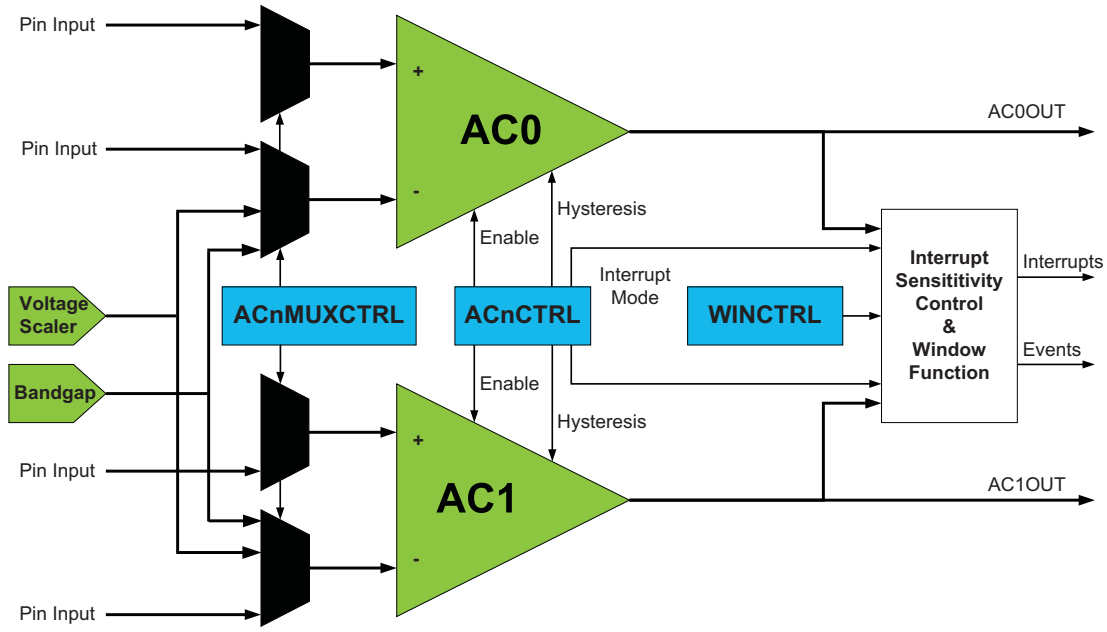
The input selection includes analog port pins, several internal signals, and a 64-level programmable voltage scaler. The analog comparator output state can also be output on a pin for use by external devices.

A constant current source can be enabled and output on a selectable pin. This can be used to replace, for example, external resistors used to charge capacitors in capacitive touch sensing applications.

The analog comparators are always grouped in pairs on each port. These are called analog comparator 0 (AC0) and analog comparator 1 (AC1). They have identical behavior, but separate control registers. Used as pair, they can be set in window mode to compare a signal to a voltage range instead of a voltage level.

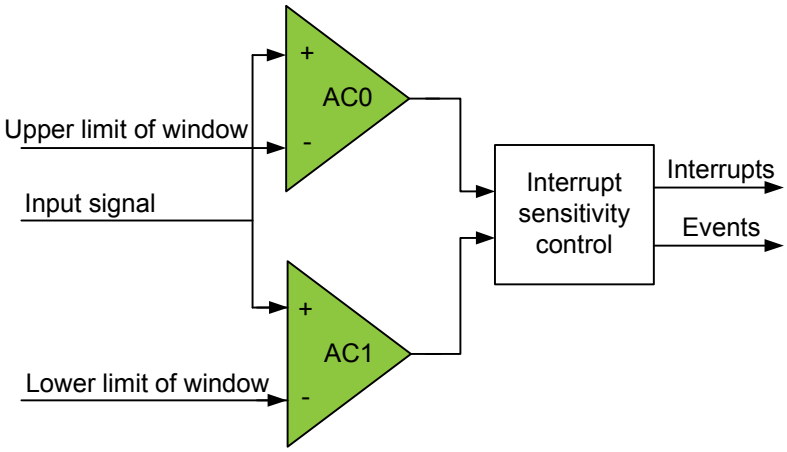
PORTA has one AC pair. Notation is ACA.

Figure 26-1. Analog comparator overview.



The window function is realized by connecting the external inputs of the two analog comparators in a pair as shown in Figure 26-2.

Figure 26-2. Analog comparator window function.



27. Programming and debugging

27.1 Features

- Programming
  - External programming through PDI interface
    - Minimal protocol overhead for fast operation
    - Built-in error detection and handling for reliable operation
  - Boot loader support for programming through any communication interface
- Debugging
  - Nonintrusive, real-time, on-chip debug system
  - No software or hardware resources required from device except pin connection
  - Program flow control
    - Go, Stop, Reset, Step Into, Step Over, Step Out, Run-to-Cursor
  - Unlimited number of user program breakpoints
  - Unlimited number of user data breakpoints, break on:
    - Data location read, write, or both read and write
    - Data location content equal or not equal to a value
    - Data location content is greater or smaller than a value
    - Data location content is within or outside a range
  - No limitation on device clock frequency
- Program and Debug Interface (PDI)
  - Two-pin interface for external programming and debugging
  - Uses the Reset pin and a dedicated pin
  - No I/O pins required during programming or debugging

27.2 Overview

The Program and Debug Interface (PDI) is an Atmel proprietary interface for external programming and on-chip debugging of a device.

The PDI supports fast programming of nonvolatile memory (NVM) spaces; flash, EEPOM, fuses, lock bits, and the user signature row.

Debug is supported through an on-chip debug system that offers nonintrusive, real-time debug. It does not require any software or hardware resources except for the device pin connection. Using the Atmel tool chain, it offers complete program flow control and support for an unlimited number of program and complex data breakpoints. Application debug can be done from a C or other high-level language source code level, as well as from an assembler and disassembler level.

Programming and debugging can be done through the PDI physical layer. This is a two-pin interface that uses the Reset pin for the clock input (PDI_CLK) and one other dedicated pin for data input and output (PDI_DATA). Any external programmer or on-chip debugger/emulator can be directly connected to this interface.

28. Pinout and pin functions

The device pinout is shown in “Pinout/block diagram” on page 4. In addition to general purpose I/O functionality, each pin can have several alternate functions. This will depend on which peripheral is enabled and connected to the actual pin. Only one of the pin functions can be used at time.

28.1 Alternate pin function description

The tables below show the notation for all pin functions available and describe its function.

28.1.1 Operation/power supply

V_{CC}	Digital supply voltage
AV_{CC}	Analog supply voltage
GND	Ground

28.1.2 Port Interrupt functions

SYNC	Port pin with full synchronous and limited asynchronous interrupt function
ASYNC	Port pin with full synchronous and full asynchronous interrupt function

28.1.3 Analog functions

ACn	Analog comparator input pin n
ACnOUT	Analog comparator n output
ADCn	Analog to digital converter input pin n
A_{REF}	Analog reference input pin

28.1.4 Timer/counter and AWEX functions

OCnxLS	Output compare channel x low side for Timer/Counter n
OCnxHS	Output compare channel x high side for Timer/Counter n

28.1.5 Communication functions

SCL	Serial Clock for TWI
SDA	Serial Data for TWI
SCLIN	Serial Clock In for TWI when external driver interface is enabled
SCLOUT	Serial Clock Out for TWI when external driver interface is enabled
SDAIN	Serial Data In for TWI when external driver interface is enabled
SDAOUT	Serial Data Out for TWI when external driver interface is enabled
XCKn	Transfer Clock for USART n
RXDn	Receiver Data for USART n
TXDn	Transmitter Data for USART n
$\overline{SS}$	Slave Select for SPI
MOSI	Master Out Slave In for SPI
MISO	Master In Slave Out for SPI
SCK	Serial Clock for SPI

28.1.6 Oscillators, Clock and Event

TOSCn	Timer Oscillator pin n
XTALn	Input/Output for Oscillator pin n
CLKOUT	Peripheral Clock Output
EVOUT	Event Channel Output
RTCOUT	RTC Clock Source Output

28.1.7 Debug/System functions

$\overline{RESET}$	Reset pin
PDI_CLK	Program and Debug Interface Clock pin
PDI_DATA	Program and Debug Interface Data pin

28.2 Alternate pin functions

The tables below show the primary/default function for each pin on a port in the first column, the pin number in the second column, and then all alternate pin functions in the remaining columns. The head row shows what peripheral that enable and use the alternate pin functions.

For better flexibility, some alternate functions also have selectable pin locations for their functions, this is noted under the first table where this apply.

Table 28-1. Port A - Alternate functions.

PORT A	PIN #	INTERRUPT	ADCA POS/ GAINPOS	ADCA NEG	ADCA GAINNEG	ACA POS	ACA NEG	ACA OUT	REFA
GND	60								
AVCC	61								
PA0	62	SYNC	ADC0	ADC0		AC0	AC0		AREFA
PA1	63	SYNC	ADC1	ADC1		AC1	AC1		
PA2	64	SYNC/ASYNC	ADC2	ADC2		AC2			
PA3	1	SYNC	ADC3	ADC3		AC3	AC3		
PA4	2	SYNC	ADC4		ADC4	AC4			
PA5	3	SYNC	ADC5		ADC5	AC5	AC5		
PA6	4	SYNC	ADC6		ADC6	AC6		AC1OUT	
PA7	5	SYNC	ADC7		ADC7		AC7	AC0OUT	

Table 28-2. Port B - Alternate functions.

PORT B	PIN #	INTERRUPT	ADCA POS	REFB
PB0	6	SYNC	ADC8	AREFB
PB1	6	SYNC	ADC9	
PB2	8	SYNC/ASYNC	ADC10	
PB3	9	SYNC	ADC11	
PB4	10	SYNC	ADC12	
PB5	11	SYNC	ADC13	
PB6	12	SYNC	ADC14	
PB7	13	SYNC	ADC15	
GND	14			
VCC	15			

Table 28-3. Port C - Alternate functions.

PORT C	PIN #	INTERRUPT	TCC0 (1)(2)	AWEXC	TCC1	USARTC0 (3)	SPIC (4)	TWIC	CLOCKOUT (5)	EVENTOUT (6)
PC0	16	SYNC	OC0A	$\overline{\text{OC0ALS}}$				SDA		
PC1	17	SYNC	OC0B	OC0AHS		XCK0		SCL		
PC2	18	SYNC/ASYNC	OC0C	$\overline{\text{OC0BLS}}$		RXD0				
PC3	19	SYNC	OC0D	OC0BHS		TXD0				
PC4	20	SYNC		$\overline{\text{OC0CLS}}$	OC1A		$\overline{\text{SS}}$			
PC5	21	SYNC		OC0CHS	OC1B		MOSI			

PORT C	PIN #	INTERRUPT	TCC0 (1)(2)	AWEXC	TCC1	USARTC0 (3)	SPIC (4)	TWIC	CLOCKOUT (5)	EVENTOUT (6)
PC6	22	SYNC		$\overline{\text{OC0DLS}}$			MISO		RTCOUT	
PC7	23	SYNC		OC0DHS			SCK		clk_{PER}	EVOUT
GND	24									
VCC	25									

Notes:
1. Pin mapping of all TC0 can optionally be moved to high nibble of port.
2. If TC0 is configured as TC2 all eight pins can be used for PWM output.
3. Pin mapping of all USART0 can optionally be moved to high nibble of port.
4. Pins MOSI and SCK for all SPI can optionally be swapped.
5. CLKOUT can optionally be moved between port C, D, and E and between pin 4 and 7.
6. EVOUT can optionally be moved between port C, D, and E and between pin 4 and 7.

Table 28-4. Port D - Alternate functions.

PORT D	PIN #	INTERRUPT	TCD0	USARTD0	SPID	CLOCKOUT	EVENTOUT
PD0	26	SYNC	OC0A				
PD1	27	SYNC	OC0B	XCK0			
PD2	28	SYNC/ASYNC	OC0C	RXD0			
PD3	29	SYNC	OC0D	TXD0			
PD4	30	SYNC			$\overline{\text{SS}}$		
PD5	31	SYNC			MOSI		
PD6	32	SYNC			MISO		
PD7	33	SYNC			SCK	Clk_{PER}	EVOUT
GND	34						
VCC	35						

Table 28-5. Port E - Alternate functions.

PORT E	PIN #	INTERRUPT	TCE0	USARTE0	TOSC	TWIE	CLOCKOUT	EVENTOUT
PE0	36	SYNC	OC0A			SDA		
PE1	37	SYNC	OC0B	XCK0		SCL		
PE2	38	SYNC/ASYNC	OC0C	RXD0				
PE3	39	SYNC	OC0D	TXD0				
PE4	40	SYNC						
PE5	41	SYNC						
PE6	42	SYNC			TOSC2			
PE7	43	SYNC			TOSC1		Clk_{PER}	EVOUT
GND	44							
VCC	45							

Table 28-6. Port F - Alternate functions.

PORT F	PIN #	INTERRUPT	TCF0
PF0	46	SYNC	OC0A
PF1	47	SYNC	OC0B
PF2	48	SYNC/ASYNC	OC0C
PF3	49	SYNC	OC0D
PF4	50	SYNC	
PF5	51	SYNC	
PF6	54	SYNC	
PF7	55	SYNC	
GND	52		
VCC	53		

Table 28-7. Port R - Alternate functions.

PORT R	PIN #	INTERRUPT	PDI	XTAL
PDI	56		PDI_DATA	
$\overline{\text{RESET}}$	57		PDI_CLOCK	
PRO	58	SYNC		XTAL2
PR1	59	SYNC		XTAL1

29. Peripheral module address map

The address maps show the base address for each peripheral and module in Atmel AVR XMEGA D3. For complete register description and summary for each peripheral module, refer to the XMEGA D manual.

Table 29-1. Peripheral module address map.

Base address	Name	Description
0x0000	GPIO	General Purpose IO Registers
0x0010	VPORT0	Virtual Port 0
0x0014	VPORT1	Virtual Port 1
0x0018	VPORT2	Virtual Port 2
0x001C	VPORT3	Virtual Port 2
0x0030	CPU	CPU
0x0040	CLK	Clock Control
0x0048	SLEEP	Sleep Controller
0x0050	OSC	Oscillator Control
0x0060	DFLLRC32M	DFLL for the 32MHz Internal Oscillator
0x0068	DFLLRC2M	DFLL for the 2MHz Internal Oscillator
0x0070	PR	Power Reduction
0x0078	RST	Reset Controller
0x0080	WDT	Watchdog Timer
0x0090	MCU	MCU Control
0x00A0	PMIC	Programmable Multilevel Interrupt Controller
0x00B0	PORTCFG	Port Configuration
0x0180	EVSYS	Event System
0x00D0	CRC	CRC Module
0x01C0	NVM	Non Volatile Memory (NVM) Controller
0x0200	ADCA	Analog to Digital Converter on port A
0x0380	ACA	Analog Comparator pair on port A
0x0400	RTC	Real-Time Counter
0x0480	TWIC	Two-Wire Interface on port C
0x04A0	TWIE	Two-Wire Interface on port E
0x0600	PORTA	Port A
0x0620	PORTB	Port B
0x0640	PORTC	Port C

Base address	Name	Description
0x0660	PORTD	Port D
0x0680	PORTE	Port E
0x06A0	PORTF	Port F
0x07E0	PORTR	Port R
0x0800	TCC0	Timer/Counter 0 on port C
0x0840	TCC1	Timer/Counter 1 on port C
0x0880	AWEXC	Advanced Waveform Extension on port C
0x0890	HIRESC	High Resolution Extension on port C
0x08A0	USARTC0	USART 0 on port C
0x08C0	SPIC	Serial Peripheral Interface on port C
0x08F8	IRCOM	Infrared Communication Module
0x0900	TCD0	Timer/Counter 0 on port D
0x09A0	USARTD0	USART 0 on port D
0x09C0	SPID	Serial Peripheral Interface on port D
0x0A00	TCE0	Timer/Counter 0 on port E
0x0A80	AWEXE	Advanced Waveform Extension on port E
0x0AA0	USARTE0	USART 0 on port E
0x0AC0	SPIE	Serial Peripheral Interface on port E
0x0B00	TCF0	Timer/Counter 0 on port F

30. Instruction set summary

Mnemonics	Operands	Description	Operation	Flags	#Clocks
Arithmetic and logic instructions					
ADD	Rd, Rr	Add without Carry	Rd ← Rd + Rr	Z,C,N,V,S,H	1
ADC	Rd, Rr	Add with Carry	Rd ← Rd + Rr + C	Z,C,N,V,S,H	1
ADIW	Rd, K	Add Immediate to Word	Rd ← Rd + 1:Rd + K	Z,C,N,V,S	2
SUB	Rd, Rr	Subtract without Carry	Rd ← Rd - Rr	Z,C,N,V,S,H	1
SUBI	Rd, K	Subtract Immediate	Rd ← Rd - K	Z,C,N,V,S,H	1
SBC	Rd, Rr	Subtract with Carry	Rd ← Rd - Rr - C	Z,C,N,V,S,H	1
SBCI	Rd, K	Subtract Immediate with Carry	Rd ← Rd - K - C	Z,C,N,V,S,H	1
SBIW	Rd, K	Subtract Immediate from Word	Rd + 1:Rd ← Rd + 1:Rd - K	Z,C,N,V,S	2
AND	Rd, Rr	Logical AND	Rd ← Rd • Rr	Z,N,V,S	1
ANDI	Rd, K	Logical AND with Immediate	Rd ← Rd • K	Z,N,V,S	1
OR	Rd, Rr	Logical OR	Rd ← Rd v Rr	Z,N,V,S	1
ORI	Rd, K	Logical OR with Immediate	Rd ← Rd v K	Z,N,V,S	1
EOR	Rd, Rr	Exclusive OR	Rd ← Rd ⊕ Rr	Z,N,V,S	1
COM	Rd	One's Complement	Rd ← $FF - Rd	Z,C,N,V,S	1
NEG	Rd	Two's Complement	Rd ← $00 - Rd	Z,C,N,V,S,H	1
SBR	Rd, K	Set Bit(s) in Register	Rd ← Rd v K	Z,N,V,S	1
CBR	Rd, K	Clear Bit(s) in Register	Rd ← Rd • ($FFh - K)	Z,N,V,S	1
INC	Rd	Increment	Rd ← Rd + 1	Z,N,V,S	1
DEC	Rd	Decrement	Rd ← Rd - 1	Z,N,V,S	1
TST	Rd	Test for Zero or Minus	Rd ← Rd • Rd	Z,N,V,S	1
CLR	Rd	Clear Register	Rd ← Rd ⊕ Rd	Z,N,V,S	1
SER	Rd	Set Register	Rd ← $FF	None	1
MUL	Rd, Rr	Multiply Unsigned	R1:R0 ← Rd x Rr (UU)	Z,C	2
MULS	Rd, Rr	Multiply Signed	R1:R0 ← Rd x Rr (SS)	Z,C	2
MULSU	Rd, Rr	Multiply Signed with Unsigned	R1:R0 ← Rd x Rr (SU)	Z,C	2
FMUL	Rd, Rr	Fractional Multiply Unsigned	R1:R0 ← Rd x Rr<<1 (UU)	Z,C	2
FMULS	Rd, Rr	Fractional Multiply Signed	R1:R0 ← Rd x Rr<<1 (SS)	Z,C	2
FMULSU	Rd, Rr	Fractional Multiply Signed with Unsigned	R1:R0 ← Rd x Rr<<1 (SU)	Z,C	2
Branch instructions					
RJMP	k	Relative Jump	PC ← PC + k + 1	None	2
IJMP		Indirect Jump to (Z)	PC(15:0) ← Z, PC(21:16) ← 0	None	2
EIJMP		Extended Indirect Jump to (Z)	PC(15:0) ← Z, PC(21:16) ← EIND	None	2
JMP	k	Jump	PC ← k	None	3
RCALL	k	Relative Call Subroutine	PC ← PC + k + 1	None	2 / 3 (1)
ICALL		Indirect Call to (Z)	PC(15:0) ← Z, PC(21:16) ← 0	None	2 / 3 (1)

Mnemonics	Operands	Description	Operation	Flags	#Clocks
EICALL		Extended Indirect Call to (Z)	PC(15:0) ← Z, PC(21:16) ← EIND	None	3 [1]
CALL	k	call Subroutine	PC ← k	None	3 / 4 [1]
RET		Subroutine Return	PC ← STACK	None	4 / 5 [1]
RETI		Interrupt Return	PC ← STACK	I	4 / 5 [1]
CPSE	Rd, Rr	Compare, Skip if Equal	if (Rd = Rr) PC ← PC + 2 or 3	None	1 / 2 / 3
CP	Rd, Rr	Compare	Rd - Rr	Z,C,N,V,S,H	1
CPC	Rd, Rr	Compare with Carry	Rd - Rr - C	Z,C,N,V,S,H	1
CPI	Rd, K	Compare with Immediate	Rd - K	Z,C,N,V,S,H	1
SBRC	Rr, b	Skip if Bit in Register Cleared	if (Rr(b) = 0) PC ← PC + 2 or 3	None	1 / 2 / 3
SBRS	Rr, b	Skip if Bit in Register Set	if (Rr(b) = 1) PC ← PC + 2 or 3	None	1 / 2 / 3
SBIC	A, b	Skip if Bit in I/O Register Cleared	if (I/O(A,b) = 0) PC ← PC + 2 or 3	None	2 / 3 / 4
SBIS	A, b	Skip if Bit in I/O Register Set	If (I/O(A,b) =1) PC ← PC + 2 or 3	None	2 / 3 / 4
BRBS	s, k	Branch if Status Flag Set	if (SREG(s) = 1) then PC ← PC + k + 1	None	1 / 2
BRBC	s, k	Branch if Status Flag Cleared	if (SREG(s) = 0) then PC ← PC + k + 1	None	1 / 2
BREQ	k	Branch if Equal	if (Z = 1) then PC ← PC + k + 1	None	1 / 2
BRNE	k	Branch if Not Equal	if (Z = 0) then PC ← PC + k + 1	None	1 / 2
BRCS	k	Branch if Carry Set	if (C = 1) then PC ← PC + k + 1	None	1 / 2
BRCC	k	Branch if Carry Cleared	if (C = 0) then PC ← PC + k + 1	None	1 / 2
BRSH	k	Branch if Same or Higher	if (C = 0) then PC ← PC + k + 1	None	1 / 2
BRLO	k	Branch if Lower	if (C = 1) then PC ← PC + k + 1	None	1 / 2
BRMI	k	Branch if Minus	if (N = 1) then PC ← PC + k + 1	None	1 / 2
BRPL	k	Branch if Plus	if (N = 0) then PC ← PC + k + 1	None	1 / 2
BRGE	k	Branch if Greater or Equal, Signed	if (N ⊕ V= 0) then PC ← PC + k + 1	None	1 / 2
BRLT	k	Branch if Less Than, Signed	if (N ⊕ V= 1) then PC ← PC + k + 1	None	1 / 2
BRHS	k	Branch if Half Carry Flag Set	if (H = 1) then PC ← PC + k + 1	None	1 / 2
BRHC	k	Branch if Half Carry Flag Cleared	if (H = 0) then PC ← PC + k + 1	None	1 / 2
BRTS	k	Branch if T Flag Set	if (T = 1) then PC ← PC + k + 1	None	1 / 2
BRTC	k	Branch if T Flag Cleared	if (T = 0) then PC ← PC + k + 1	None	1 / 2
BRVS	k	Branch if Overflow Flag is Set	if (V = 1) then PC ← PC + k + 1	None	1 / 2
BRVC	k	Branch if Overflow Flag is Cleared	if (V = 0) then PC ← PC + k + 1	None	1 / 2
BRIE	k	Branch if Interrupt Enabled	if (I = 1) then PC ← PC + k + 1	None	1 / 2
BRID	k	Branch if Interrupt Disabled	if (I = 0) then PC ← PC + k + 1	None	1 / 2
Data transfer instructions					
MOV	Rd, Rr	Copy Register	Rd ← Rr	None	1
MOVW	Rd, Rr	Copy Register Pair	Rd+1:Rd ← Rr+1:Rr	None	1
LDI	Rd, K	Load Immediate	Rd ← K	None	1
LDS	Rd, k	Load Direct from data space	Rd ← (k)	None	2 [1][2]
LD	Rd, X	Load Indirect	Rd ← (X)	None	1 [1][2]

Mnemonics	Operands	Description	Operation	Flags	#Clocks
LD	Rd, X+	Load Indirect and Post-Increment	Rd ← (X) X ← X + 1	None	1 (1)(2)
LD	Rd, -X	Load Indirect and Pre-Decrement	X ← X - 1, ← X - 1 Rd ← (X) ← (X)	None	2 (1)(2)
LD	Rd, Y	Load Indirect	Rd ← (Y) ← (Y)	None	1 (1)(2)
LD	Rd, Y+	Load Indirect and Post-Increment	Rd ← (Y) Y ← Y + 1	None	1 (1)(2)
LD	Rd, -Y	Load Indirect and Pre-Decrement	Y ← Y - 1 Rd ← (Y)	None	2 (1)(2)
LDD	Rd, Y+q	Load Indirect with Displacement	Rd ← (Y + q)	None	2 (1)(2)
LD	Rd, Z	Load Indirect	Rd ← (Z)	None	1 (1)(2)
LD	Rd, Z+	Load Indirect and Post-Increment	Rd ← (Z), Z ← Z+1	None	1 (1)(2)
LD	Rd, -Z	Load Indirect and Pre-Decrement	Z ← Z - 1, Rd ← (Z)	None	2 (1)(2)
LDD	Rd, Z+q	Load Indirect with Displacement	Rd ← (Z + q)	None	2 (1)(2)
STS	k, Rr	Store Direct to Data Space	(k) ← Rd	None	2 (1)
ST	X, Rr	Store Indirect	(X) ← Rr	None	1 (1)
ST	X+, Rr	Store Indirect and Post-Increment	(X) ← Rr, X ← X + 1	None	1 (1)
ST	-X, Rr	Store Indirect and Pre-Decrement	X ← X - 1, (X) ← Rr	None	2 (1)
ST	Y, Rr	Store Indirect	(Y) ← Rr	None	1 (1)
ST	Y+, Rr	Store Indirect and Post-Increment	(Y) ← Rr, Y ← Y + 1	None	1 (1)
ST	-Y, Rr	Store Indirect and Pre-Decrement	Y ← Y - 1, (Y) ← Rr	None	2 (1)
STD	Y+q, Rr	Store Indirect with Displacement	(Y + q) ← Rr	None	2 (1)
ST	Z, Rr	Store Indirect	(Z) ← Rr	None	1 (1)
ST	Z+, Rr	Store Indirect and Post-Increment	(Z) ← Rr Z ← Z + 1	None	1 (1)
ST	-Z, Rr	Store Indirect and Pre-Decrement	Z ← Z - 1	None	2 (1)
STD	Z+q, Rr	Store Indirect with Displacement	(Z + q) ← Rr	None	2 (1)
LPM		Load Program Memory	R0 ← (Z)	None	3
LPM	Rd, Z	Load Program Memory	Rd ← (Z)	None	3
LPM	Rd, Z+	Load Program Memory and Post-Increment	Rd ← (Z), Z ← Z + 1	None	3
ELPM		Extended Load Program Memory	R0 ← (RAMPZ:Z)	None	3
ELPM	Rd, Z	Extended Load Program Memory	Rd ← (RAMPZ:Z)	None	3
ELPM	Rd, Z+	Extended Load Program Memory and Post-Increment	Rd ← (RAMPZ:Z), Z ← Z + 1	None	3
SPM		Store Program Memory	(RAMPZ:Z) ← R1:R0	None	-
SPM	Z+	Store Program Memory and Post-Increment by 2	(RAMPZ:Z) ← R1:R0, Z ← Z + 2	None	-
IN	Rd, A	In From I/O Location	Rd ← I/O(A)	None	1
OUT	A, Rr	Out To I/O Location	I/O(A) ← Rr	None	1

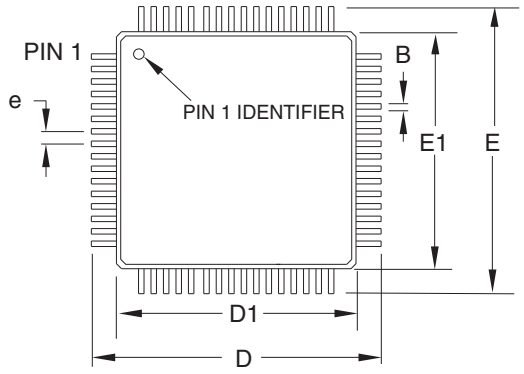
Mnemonics	Operands	Description	Operation	Flags	#Clocks
PUSH	Rr	Push Register on Stack	STACK ← Rr	None	1 [1]
POP	Rd	Pop Register from Stack	Rd ← STACK	None	2 [1]
Bit and bit-test instructions					
LSL	Rd	Logical Shift Left	Rd(n+1) ← Rd(n), Rd(0) ← 0, C ← Rd(7)	Z,C,N,V,H	1
LSR	Rd	Logical Shift Right	Rd(n) ← Rd(n+1), Rd(7) ← 0, C ← Rd(0)	Z,C,N,V	1
ROL	Rd	Rotate Left Through Carry	Rd(0) ← C, Rd(n+1) ← Rd(n), C ← Rd(7)	Z,C,N,V,H	1
ROR	Rd	Rotate Right Through Carry	Rd(7) ← C, Rd(n) ← Rd(n+1), C ← Rd(0)	Z,C,N,V	1
ASR	Rd	Arithmetic Shift Right	Rd(n) ← Rd(n+1), n=0..6	Z,C,N,V	1
SWAP	Rd	Swap Nibbles	Rd(3..0) ↔ Rd(7..4)	None	1
BSET	s	Flag Set	SREG(s) ← 1	SREG(s)	1
BCLR	s	Flag Clear	SREG(s) ← 0	SREG(s)	1
SBI	A, b	Set Bit in I/O Register	I/O(A, b) ← 1	None	1
CBI	A, b	Clear Bit in I/O Register	I/O(A, b) ← 0	None	1
BST	Rr, b	Bit Store from Register to T	T ← Rr(b)	T	1
BLD	Rd, b	Bit load from T to Register	Rd(b) ← T	None	1
SEC		Set Carry	C ← 1	C	1
CLC		Clear Carry	C ← 0	C	1
SEN		Set Negative Flag	N ← 1	N	1
CLN		Clear Negative Flag	N ← 0	N	1
SEZ		Set Zero Flag	Z ← 1	Z	1
CLZ		Clear Zero Flag	Z ← 0	Z	1
SEI		Global Interrupt Enable	I ← 1	I	1
CLI		Global Interrupt Disable	I ← 0	I	1
SES		Set Signed Test Flag	S ← 1	S	1
CLS		Clear Signed Test Flag	S ← 0	S	1
SEV		Set Two's Complement Overflow	V ← 1	V	1
CLV		Clear Two's Complement Overflow	V ← 0	V	1
SET		Set T in SREG	T ← 1	T	1
CLT		Clear T in SREG	T ← 0	T	1
SEH		Set Half Carry Flag in SREG	H ← 1	H	1
CLH		Clear Half Carry Flag in SREG	H ← 0	H	1
MCU control instructions					
BREAK		Break	(See specific descr. for BREAK)	None	1

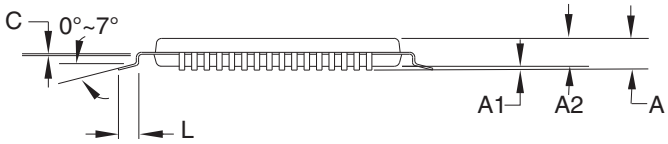
Mnemonics	Operands	Description	Operation	Flags	#Clocks
NOP		No Operation		None	1
SLEEP		Sleep	(See specific descr. for Sleep)	None	1
WDR		Watchdog Reset	(See specific descr. for WDR)	None	1

Notes: 1. Cycle times for data memory accesses assume internal memory accesses, and are not valid for accesses via the external RAM interface.
2. One extra cycle must be added when accessing internal SRAM.

31. Packaging information

31.1 64A





COMMON DIMENSIONS
(Unit of measure = mm)

SYMBOL	MIN	NOM	MAX	NOTE
A	–	–	1.20	
A1	0.05	–	0.15	
A2	0.95	1.00	1.05	
D	15.75	16.00	16.25	
D1	13.90	14.00	14.10	Note 2
E	15.75	16.00	16.25	
E1	13.90	14.00	14.10	Note 2
B	0.30	–	0.45	
C	0.09	–	0.20	
L	0.45	–	0.75	
e	0.80 TYP			

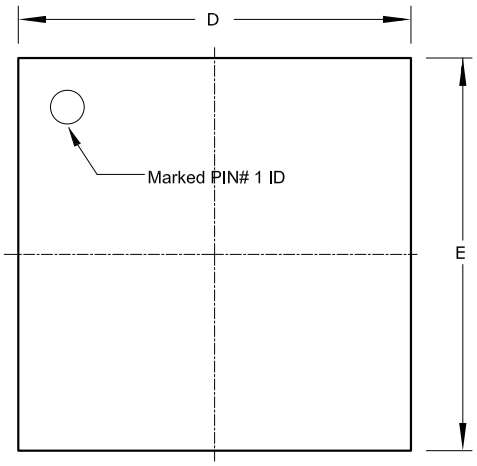
Notes:
1. This package conforms to JEDEC reference MS-026, Variation AEB.
2. Dimensions D1 and E1 do not include mold protrusion. Allowable protrusion is 0.25mm per side. Dimensions D1 and E1 are maximum plastic body size dimensions including mold mismatch.
3. Lead coplanarity is 0.10mm maximum.

2010-10-20

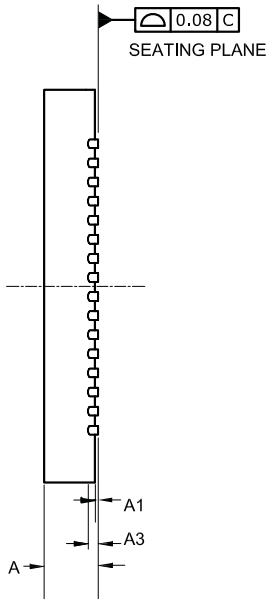
	TITLE	DRAWING NO.	REV.
Atmel 2325 Orchard Parkway San Jose, CA 95131	**64A,** 64-lead, 14 x 14mm Body Size, 1.0mm Body Thickness, 0.8mm Lead Pitch, Thin Profile Plastic Quad Flat Package (TQFP)	64A	C

31.2 64M

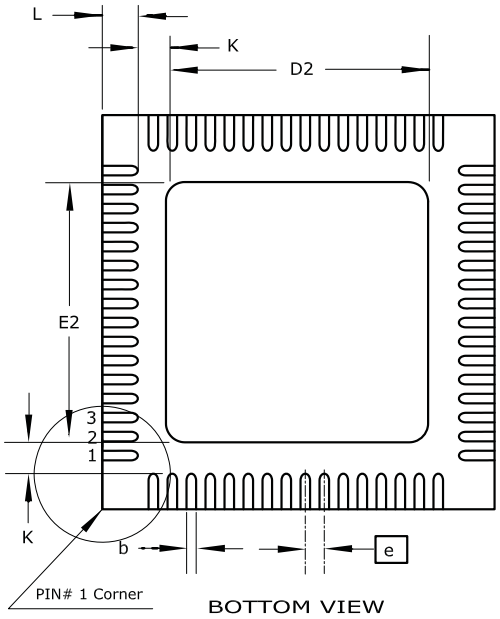
DRAWINGS NOT SCALED



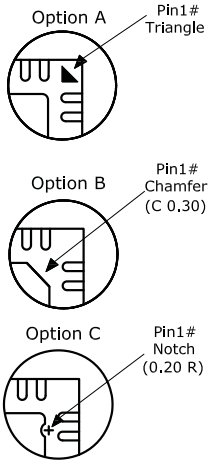
TOP VIEW



SIDE VIEW



BOTTOM VIEW



COMMON DIMENSIONS

(Unit of Measure = mm)

SYMBOL	MIN	NOM	MAX	NOTE
A	----	----	1.00	
A1	----	0.02	0.05	
A3		0.20 REF		
D/E	8.90	9.00	9.10	
D2/E2	7.50	7.65	7.80	
L	0.35	0.40	0.45	
K	0.20	0.27	0.40	
b	0.18	----	0.30	2
e		0.50 BSC		
n		64		

Notes : 1. This drawing is for general information only. Refer to JEDEC Drawing MO-220, Variation VMMD for proper dimensions, tolerances, datums, etc.
2. Dimension b applies to metallized terminal and is measured between 0.15mm and 0.30mm from the terminal tip.
If the terminal has the optical radius on the other end of the terminal, the dimension should not be measured in that radius area.

12/18/2012

	TITLE	GPC	DRAWING NO.	REV.
Atmel **Package Drawing Contact: packagedrawings@atmel.com**	PP, 64 Lds - 0.50mm Pitch, 9x9x1mm Body size Very Thin Quad Flat Package (VQFN) Sawn	ZFF	PP	A

32. Electrical characteristics

All typical values are measured at T = 25°C unless other temperature condition is given. All minimum and maximum values are valid across operating temperature and voltage unless other conditions are given.

32.1 Atmel ATxmega32D3

32.1.1 Absolute maximum ratings

Stresses beyond those listed in Table 32-30 on page 82 under may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Table 32-1. Absolute maximum ratings.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
V_{CC}	Power supply voltage		-0.3		4	V
I_{VCC}	Current into a V_{CC} pin				200	mA
I_{GND}	Current out of a Gnd pin				200	
V_{PIN}	Pin voltage with respect to Gnd and V_{CC}		-0.5		V_{CC} + 0.5	V
I_{PIN}	I/O pin sink/source current		-25		25	mA
T_A	Storage temperature		-65		150	°C
T_j	Junction temperature				150	

32.1.2 General operating ratings

The device must operate within the ratings listed in Table 32-31 on page 82 in order for all other electrical characteristics and typical characteristics of the device to be valid.

Table 32-2. General operating conditions.

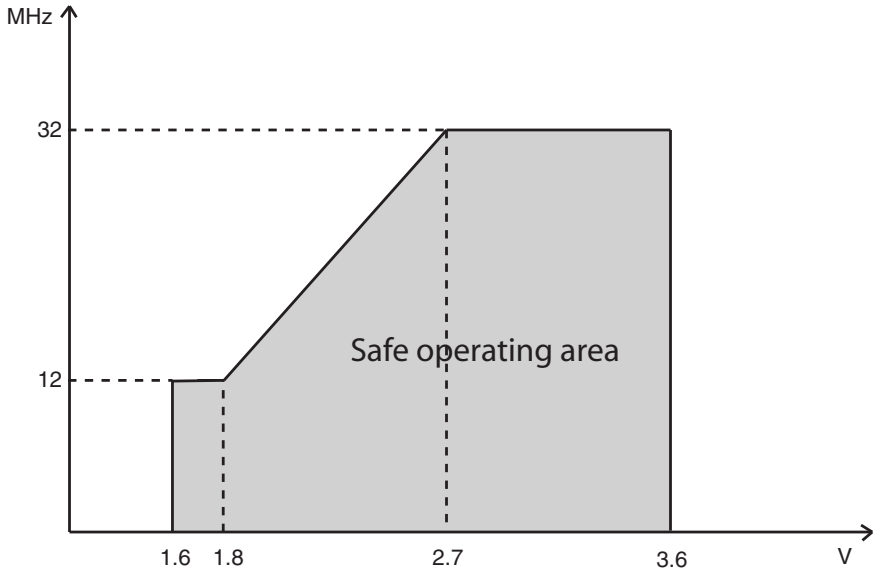
Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
V_{CC}	Power supply voltage		1.60		3.6	V
AV_{CC}	Analog supply voltage		1.60		3.6	
T_A	Temperature range		-40		85	°C
T_j	Junction temperature		-40		105	

Table 32-3. Operating voltage and frequency.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
Clk_{CPU}	CPU clock frequency	V_{CC} = 1.6V	0		12	MHz
		V_{CC} = 1.8V	0		12	
		V_{CC} = 2.7V	0		32	
		V_{CC} = 3.6V	0		32	

The maximum CPU clock frequency depends on V_{CC}. As shown in Figure 32-8 on page 83 the frequency vs. V_{CC} curve is linear between 1.8V < V_{CC} < 2.7V.

Figure 32-1. Maximum frequency vs. V_{CC}.



32.1.3 Current consumption

Table 32-4. Current consumption for Active mode and sleep modes.

Symbol	Parameter	Condition		Min.	Typ.	Max.	Units
I_{CC}	Active power consumption (1)	32kHz, Ext. Clk	V_{CC} = 1.8V		50		µA
			V_{CC} = 3.0V		130		
		1MHz, Ext. Clk	V_{CC} = 1.8V		215		
			V_{CC} = 3.0V		475		
		2MHz, Ext. Clk	V_{CC} = 1.8V		445	600	
			V_{CC} = 3.0V		0.95	1.5	mA
		32MHz, Ext. Clk			7.8	12.0	
	Idle power consumption (1)	32kHz, Ext. Clk	V_{CC} = 1.8V		2.8		µA
			V_{CC} = 3.0V		3		
		1MHz, Ext. Clk	V_{CC} = 1.8V		46		
			V_{CC} = 3.0V		92		
		2MHz, Ext. Clk	V_{CC} = 1.8V		93	225	
			V_{CC} = 3.0V		184	350	
		32MHz, Ext. Clk			2.9	5.0	mA
	Power-down power consumption	T = 25°C	V_{CC} = 3.0V		0.07	1.0	µA
		T = 85°C			1.3	5.0	
		WDT and sampled BOD enabled, T = 25°C	V_{CC} = 3.0V		1.3	2.0	
		WDT and sampled BOD enabled, T = 85°C			2.6	6.0	
	Power-save power consumption (2)	RTC from ULP clock, WDT and sampled BOD enabled, T = 25°C	V_{CC} = 1.8V		1.7		
			V_{CC} = 3.0V		1.8		
		RTC from 1.024kHz low power 32.768kHz TOSC, T = 25°C	V_{CC} = 1.8V		0.5	2.0	
			V_{CC} = 3.0V		0.7	2.0	
		RTC from low power 32.768kHz TOSC, T = 25°C	V_{CC} = 1.8V		0.9	3.0	
			V_{CC} = 3.0V		1.2	3.0	
	Reset power consumption	Current through $\overline{\text{RESET}}$ pin substracted	V_{CC} = 3.0V		120		

Notes:
1. All Power Reduction Registers set.
2. Maximum limits are based on characterization, and not tested in production.

Table 32-5. Current consumption for modules and peripherals.

Symbol	Parameter	Condition [1]			Min.	Typ.	Max.	Units
I_{CC}	ULP oscillator					0.9		µA
	32.768kHz int. oscillator					29		
	2MHz int. oscillator					82		
		DFLL enabled with 32.768kHz int. osc. as reference				114		
	32MHz int. oscillator					250		
		DFLL enabled with 32.768kHz int. osc. as reference				400		
	PLL	20× multiplication factor, 32MHz int. osc. DIV4 as reference				300		
	Watchdog timer					1.0		
	BOD	Continuous mode				140		
		Sampled mode, includes ULP oscillator				1.4		
	Internal 1.0V reference					180		
	Temperature sensor					175		
	ADC	200ksps V_{REF} = Ext. ref.				1.23		mA
			CURRLIMIT = LOW			1.1		
			CURRLIMIT = MEDIUM			0.98		
			CURRLIMIT = HIGH			0.87		
		75ksps V_{REF} = Ext. ref.	CURRLIMIT = LOW			1.7		
		300ksps V_{REF} = Ext. ref.				3.1		
	USART	Rx and Tx enabled, 9600 BAUD				9.7		µA
	Flash memory and EEPROM programming					5		mA

Note: 1. All parameters measured as the difference in current consumption between module enabled and disabled. All data at V_{CC} = 3.0V, Clk_{SYS} = 1MHz external clock without prescaling, T = 25°C unless other conditions are given.

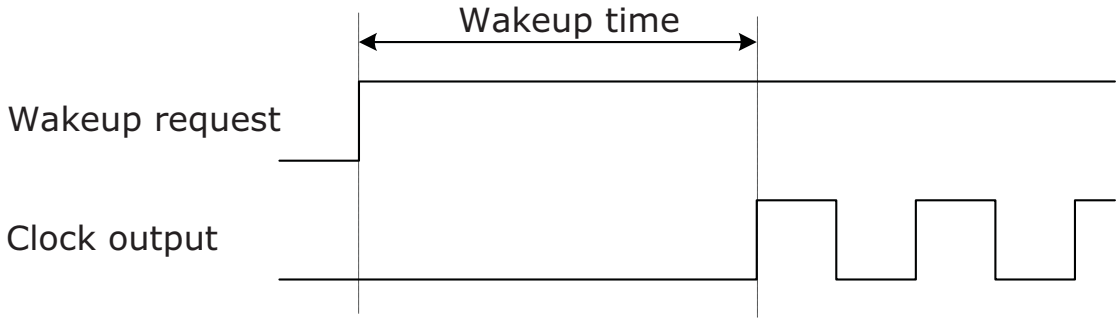
32.1.4 Wake-up time from sleep modes

Table 32-6. Device wake-up time from sleep modes with various system clock sources.

Symbol	Parameter	Condition	Min.	Typ. (1)	Max.	Units
t_{wakeup}	Wake-up time from idle, standby, and extended standby mode	External 2MHz clock		2.0		µs
		32.768kHz internal oscillator		125		
		2MHz internal oscillator		2.0		
		32MHz internal oscillator		0.2		
	Wake-up time from power-save and power-down mode	External 2MHz clock		4.6		
		32.768kHz internal oscillator		330		
		2MHz internal oscillator		9.5		
		32MHz internal oscillator		5.6		

Note: 1. The wake-up time is the time from the wake-up request is given until the peripheral clock is available on pin, see Figure 32-9 on page 86. All peripherals and modules start execution from the first clock cycle, expect the CPU that is halted for four clock cycles before program execution starts.

Figure 32-2. Wake-up time definition.



32.1.5 I/O pin characteristics

The I/O pins complies with the JEDEC LVTTL and LVCMOS specification and the high- and low level input and output voltage limits reflect or exceed this specification.

Table 32-7. I/O pin characteristics.

Symbol	Parameter	Condition		Min.	Typ.	Max.	Units
I_{OH} (1)/ I_{OL} (2)	I/O pin source/sink current			-15		15	mA
V_{IH}	High level input voltage	V_{CC} = 2.4 - 3.6V		0.7 * V_{CC}		V_{CC} + 0.5	V
		V_{CC} = 1.6 - 2.4V		0.8 * V_{CC}		V_{CC} + 0.5	
V_{IL}	Low level input voltage	V_{CC} = 2.4 - 3.6V		-0.5		0.3 * V_{CC}	
		V_{CC} = 1.6 - 2.4V		-0.5		0.2 * V_{CC}	
V_{OH}	High level output voltage	V_{CC} = 3.3V	I_{OH} = -4mA	2.6	2.9		
		V_{CC} = 3.0V	I_{OH} = -3mA	2.1	2.6		
		V_{CC} = 1.8V	I_{OH} = -1mA	1.4	1.6		
V_{OL}	Low level output voltage	V_{CC} = 3.3V	I_{OL} = 8mA		0.4	0.76	
		V_{CC} = 3.0V	I_{OL} = 5mA		0.3	0.64	
		V_{CC} = 1.8V	I_{OL} = 3mA		0.2	0.46	
I_{IN}	Input leakage current I/O pin	T = 25°C			<0.01	1	µA
R_P	Pull/buss keeper resistor				25		kΩ

Notes:
1. The sum of all I_{OH} for PORTA and PORTB must not exceed 100mA.
   The sum of all I_{OH} for PORTC, PORTD, PORTE must for each port not exceed 200mA.
   The sum of all I_{OH} for pins PF[0-5] on PORTF must not exceed 200mA.
   The sum of all I_{OL} for pins PF[6-7] on PORTF, PORTR and PDI must not exceed 100mA.
2. The sum of all I_{OL} for PORTA and PORTB must not exceed 100mA.
   The sum of all I_{OL} for PORTC, PORTD, PORTE must for each port not exceed 200mA.
   The sum of all I_{OL} for pins PF[0-5] on PORTF must not exceed 200mA.
   The sum of all I_{OL} for pins PF[6-7] on PORTF, PORTR and PDI must not exceed 100mA.

32.1.6 ADC characteristics

Table 32-8. Power supply, reference and input range.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
AV_{CC}	Analog supply voltage		V_{CC} - 0.3		V_{CC} + 0.3	V
V_{REF}	Reference voltage		1		AV_{CC} - 0.6	
R_{in}	Input resistance	Switched			4.5	kΩ
C_{in}	Input capacitance	Switched			5	pF
R_{AREF}	Reference input resistance	(leakage only)		>10		MΩ
C_{AREF}	Reference input capacitance	Static load		7		pF
V_{in}	Input range		0		V_{REF}	V
	Conversion range	Differential mode, Vinp - Vinn	$-V_{REF}$		V_{REF}	
	Conversion range	Single ended unsigned mode, Vinp	-ΔV		V_{REF} - ΔV	
ΔV	Fixed offset voltage			200		lsb

Table 32-9. Clock and timing.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
Clk_{ADC}	ADC clock frequency	Maximum is 1/4 of peripheral clock frequency	100		1800	kHz
		Measuring internal signals	100		125	
f_{ClkADC}	Sample rate		16		300	ksps
f_{ADC}	Sample rate	Current limitation (CURRLIMIT) off	16		300	
		CURRLIMIT = LOW	16		250	
		CURRLIMIT = MEDIUM	16		150	
		CURRLIMIT = HIGH	16		50	
	Sampling time	Configurable in steps of 1/2 Clk_{ADC} cycle up to 32 Clk_{ADC} cycles	0.28		320	µs
	Conversion time (latency)	(RES+2)/2 + 1 + GAIN RES (Resolution) = 8 or 12, GAIN = 0 to 3	5.5		10	Clk_{ADC} cycles
	Start-up time	ADC clock cycles		12	24	
	ADC settling time	After changing reference or input mode		7	7	

Table 32-10. Accuracy characteristics.

Symbol	Parameter	Condition [2]		Min.	Typ.	Max.	Units
RES	Resolution	12-bit resolution	Differential	8	12	12	Bits
			Single ended signed	7	11	11	
			Single ended unsigned	8	12	12	
INL [1]	Integral non-linearity	Differential mode	16ksps, V_{REF} = 3V		0.5	1	lsb
			16ksps, all V_{REF}		0.8	2	
			300ksps, V_{REF} = 3V		0.6	1	
			300ksps, all V_{REF}		1	2	
		Single ended unsigned mode	16ksps, V_{REF} = 3.0V		0.5	1	
			16ksps, all V_{REF}		1.3	2	
DNL [1]	Differential non-linearity	Differential mode	16ksps, V_{REF} = 3V		0.3	1	
			16ksps, all V_{REF}		0.5	1	
			300ksps, V_{REF} = 3V		0.3	1	
			300ksps, all V_{REF}		0.5	1	
		Single ended unsigned mode	16ksps, V_{REF} = 3V		0.6	1	
			16ksps, all V_{REF}		0.6	1	
	Offset error	Differential mode	300ksps, V_{REF} = 3V		-7		mV
			Temperature drift, V_{REF} = 3V		0.01		mV/K
			Operating voltage drift		0.16		mV/V
	Gain error	Differential mode	External reference		-5		mV
			AV_{CC}/1.6		-5		
			AV_{CC}/2.0		-6		
			Bandgap		±10		
			Temperature drift		0.02		mV/K
			Operating voltage drift		2		mV/V
	Gain error	Single ended unsigned mode	External reference		-8		mV
			AV_{CC}/1.6		-8		
			AV_{CC}/2.0		-8		
			Bandgap		±10		
			Temperature drift		0.03		mV/K
			Operating voltage drift		2		mV/V

Notes:
1. Maximum numbers are based on characterisation and not tested in production, and valid for 5% to 95% input voltage range.
2. Unless otherwise noted all linearity, offset and gain error numbers are valid under the condition that external VREF is used.

Table 32-11. Gain stage characteristics.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
R_{in}	Input resistance	Switched in normal mode		4.0		kΩ
C_{sample}	Input capacitance	Switched in normal mode		4.4		pF
	Signal range	Gain stage output	0		AV_{CC} - 0.6	V
	Propagation delay	ADC conversion rate	1/2	1	3	Clk_{ADC} cycles
	Clock frequency	Same as ADC	100		1800	kHz
	Gain error	0.5× gain, normal mode		-1		%
		1× gain, normal mode		-1		
		8× gain, normal mode		-1		
		64× gain, normal mode		5		
	Offset error, input referred	0.5× gain, normal mode		10		mV
		1× gain, normal mode		5		
		8× gain, normal mode		-20		
		64× gain, normal mode		-126		

32.1.7 Analog comparator characteristics

Table 32-12. Analog comparator characteristics.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
V_{off}	Input offset voltage			10		mV
I_{lk}	Input leakage current			<10	50	nA
	Input voltage range		-0.1		AV_{CC}	V
	AC startup time			50		µs
V_{hys1}	Hysteresis, none	V_{CC} = 1.6V - 3.6V		0		mV
V_{hys2}	Hysteresis, small	V_{CC} = 1.6V - 3.6V		15		
V_{hys3}	Hysteresis, large	V_{CC} = 1.6V - 3.6V		30		
t_{delay}	Propagation delay	V_{CC} = 3.0V, T = 85°C		20	40	ns
		V_{CC} = 3.0V		17		
	64-level voltage scaler	Integral non-linearity (INL)		0.3	0.5	lsb
	Current source accuracy after calibration			5		%
	Current source calibration range	Single mode	4		6	µA

32.1.8 Bandgap and internal 1.0V reference characteristics

Table 32-13. Bandgap and internal 1.0V reference characteristics.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
	Startup time	As reference for ADC		1 Clk_{PER} + 2.5µs		µs
		As input voltage to ADC and AC		1.5		
	Bandgap voltage			1.1		V
INT1V	Internal 1.00V reference	T = 85°C, after calibration	0.99	1	1.01	
	Variation over voltage and temperature	Calibrated at T = 85°C		1		%

32.1.9 Brownout detection characteristics

Table 32-14. Brownout detection characteristics [(1)].

Symbol	Parameter (BOD level 0 at 85°C)	Condition	Min.	Typ.	Max.	Units
V_{BOT}	BOD level 0 falling V_{CC}		1.40	1.60	1.70	V
	BOD level 1 falling V_{CC}			1.8		
	BOD level 2 falling V_{CC}			2.0		
	BOD level 3 falling V_{CC}			2.2		
	BOD level 4 falling V_{CC}			2.4		
	BOD level 5 falling V_{CC}			2.6		
	BOD level 6 falling V_{CC}			2.8		
	BOD level 7 falling V_{CC}			3.0		
t_{BOD}	Detection time	Continuous mode		0.4		µs
		Sampled mode		1000		
V_{HYST}	Hysteresis			1.0		%

Note: 1. BOD is calibrated at 85°C within BOD level 0 values, and BOD level 0 is the default level.

32.1.10 External reset characteristics

Table 32-15. External reset characteristics.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
t_{EXT}	Minimum reset pulse width		1000	90		ns
V_{RST}	Reset threshold voltage	V_{CC} = 2.7 - 3.6V		0.45 * V_{CC}		V
		V_{CC} = 1.6 - 2.7V		0.42 * V_{CC}		
R_{RST}	Reset pin pull-up resistor			25		kΩ

32.1.11 Power-on reset characteristics

Table 32-16. Power-on reset characteristics.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
V_{POT-} (1)	POR threshold voltage falling V_{CC}	V_{CC} falls faster than 1V/ms	0.4	1.0		V
		V_{CC} falls at 1V/ms or slower	0.8	1.3		
V_{POT+}	POR threshold voltage rising V_{CC}			1.3	1.59	

Note: 1. V_{POT-} values are only valid when BOD is disabled. When BOD is enabled $V_{POT-} = V_{POT+}$.

32.1.12 Flash and EEPROM memory characteristics

Table 32-17. Endurance and data retention.

Symbol	Parameter	Condition		Min.	Typ.	Max.	Units
	Flash	Write/erase cycles	25°C	10K			Cycle
			85°C	10K			
		Data retention	25°C	100			Year
			55°C	25			
	EEPROM	Write/erase cycles	25°C	100K			Cycle
			85°C	100K			
		Data retention	25°C	100			Year
			55°C	25			

Table 32-18. Programming time.

Symbol	Parameter	Condition	Min.	Typ. (1)	Max.	Units
	Chip erase (2)	32KB Flash, EEPROM		50		ms
	Application erase	Section erase		6		
	Flash	Page erase		4		
		Page write		4		
		Atomic page erase and write		8		
	EEPROM	Page erase		4		
		Page write		4		
		Atomic page erase and write		8		

Notes: 1. Programming is timed from the 2MHz internal oscillator.
2. EEPROM is not erased if the EESAVE fuse is programmed.

32.1.13 Clock and oscillator characteristics

32.1.13.1 Calibrated 32.768kHz internal oscillator characteristics

Table 32-19. 32.768kHz internal oscillator characteristics.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
	Frequency			32.768		kHz
	Factory calibration accuracy	T = 85°C, V_{CC} = 3.0V	-0.5		0.5	%
	User calibration accuracy		-0.5		0.5	

32.1.13.2 Calibrated 2MHz RC internal oscillator characteristics

Table 32-20. 2MHz internal oscillator characteristics.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
	Frequency range	DFLL can tune to this frequency over voltage and temperature	1.8	2.0	2.2	MHz
	Factory calibrated frequency			2.0		
	Factory calibration accuracy	T = 85°C, V_{CC} = 3.0V	-1.5		1.5	%
	User calibration accuracy		-0.2		0.2	
	DFLL calibration stepsize			0.18		

32.1.13.3 Calibrated 32MHz internal oscillator characteristics

Table 32-21. 32MHz internal oscillator characteristics.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
	Frequency range	DFLL can tune to this frequency over voltage and temperature	30	32	55	MHz
	Factory calibrated frequency			32		
	Factory calibration accuracy	T = 85°C, V_{CC} = 3.0V	-1.5		1.5	%
	User calibration accuracy		-0.2		0.2	
	DFLL calibration step size			0.19		

32.1.13.4 32kHz internal ULP oscillator characteristics

Table 32-22. 32kHz internal ULP oscillator characteristics.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
	Factory calibrated frequency			32		kHz
	Factory calibration accuracy	T = 85°C, V_{CC} = 3.0V	-12		12	%
	Accuracy		-30		30	

32.1.13.5 Internal Phase Locked Loop (PLL) characteristics

Table 32-23. Internal PLL characteristics.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
f_{IN}	Input frequency	Output frequency must be within f_{OUT}	0.4		64	MHz
f_{OUT}	Output frequency (1)	V_{CC} = 1.6 - 1.8V	20		48	
		V_{CC} = 2.7 - 3.6V	20		128	
	Start-up time			25		µs
	Re-lock time			25		

Note: 1. The maximum output frequency vs. supply voltage is linear between 1.8V and 2.7V, and can never be higher than four times the maximum CPU frequency.

32.1.13.6 External clock characteristics

Figure 32-3. External clock drive waveform.

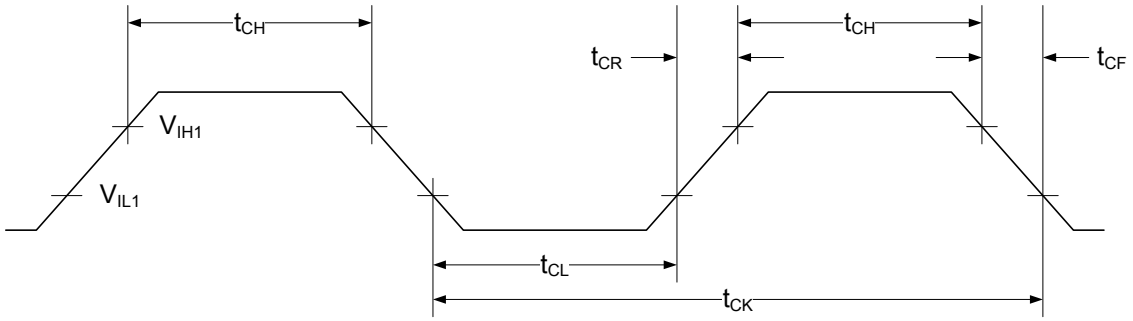


Table 32-24. External clock used as system clock without prescaling.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
$1/t_{CK}$	Clock Frequency (1)	V_{CC} = 1.6 - 1.8V	0		12	MHz
		V_{CC} = 2.7 - 3.6V	0		32	
t_{CK}	Clock Period	V_{CC} = 1.6 - 1.8V	83.3			ns
		V_{CC} = 2.7 - 3.6V	31.5			
t_{CH}	Clock High Time	V_{CC} = 1.6 - 1.8V	30.0			ns
		V_{CC} = 2.7 - 3.6V	12.5			
t_{CL}	Clock Low Time	V_{CC} = 1.6 - 1.8V	30.0			ns
		V_{CC} = 2.7 - 3.6V	12.5			
t_{CR}	Rise Time (for maximum frequency)	V_{CC} = 1.6 - 1.8V			10	ns
		V_{CC} = 2.7 - 3.6V			3	
t_{CF}	Fall Time (for maximum frequency)	V_{CC} = 1.6 - 1.8V			10	ns
		V_{CC} = 2.7 - 3.6V			3	
Δt_{CK}	Change in period from one clock cycle to the next				10	%

Note: 1. The maximum frequency vs. supply voltage is linear between 1.6V and 2.7V, and the same applies for all other parameters with supply voltage conditions.

Table 32-25. External clock with prescaler [1] for system clock.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
$1/t_{CK}$	Clock Frequency [2]	V_{CC} = 1.6 - 1.8V	0		90	MHz
		V_{CC} = 2.7 - 3.6V	0		142	
t_{CK}	Clock Period	V_{CC} = 1.6 - 1.8V	11			ns
		V_{CC} = 2.7 - 3.6V	7			
t_{CH}	Clock High Time	V_{CC} = 1.6 - 1.8V	4.5			ns
		V_{CC} = 2.7 - 3.6V	2.4			
t_{CL}	Clock Low Time	V_{CC} = 1.6 - 1.8V	4.5			ns
		V_{CC} = 2.7 - 3.6V	2.4			
t_{CR}	Rise Time (for maximum frequency)	V_{CC} = 1.6 - 1.8V			1.5	ns
		V_{CC} = 2.7 - 3.6V			1.0	
t_{CF}	Fall Time (for maximum frequency)	V_{CC} = 1.6 - 1.8V			1.5	ns
		V_{CC} = 2.7 - 3.6V			1.0	
Δt_{CK}	Change in period from one clock cycle to the next				10	%

Notes: 1. System Clock Prescalers must be set so that maximum CPU clock frequency for device is not exceeded.
2. The maximum frequency vs. supply voltage is linear between 1.6V and 2.7V, and the same applies for all other parameters with supply voltage conditions.

32.1.13.7 External 16MHz crystal oscillator and XOSC characteristics

Table 32-26. External 16MHz crystal oscillator and XOSC characteristics.

Symbol	Parameter	Condition		Min.	Typ.	Max.	Units
	Cycle to cycle jitter	XOSCPWR=0	FRQRANGE=0		0		ns
			FRQRANGE=1, 2, or 3		0		
		XOSCPWR=1			0		
	Long term jitter	XOSCPWR=0	FRQRANGE=0		0		
			FRQRANGE=1, 2, or 3		0		
		XOSCPWR=1			0		
	Frequency error	XOSCPWR=0	FRQRANGE=0		0.03		%
			FRQRANGE=1		0.03		
			FRQRANGE=2 or 3		0.03		
		XOSCPWR=1			0.003		
	Duty cycle	XOSCPWR=0	FRQRANGE=0		50		
			FRQRANGE=1		50		
			FRQRANGE=2 or 3		50		
		XOSCPWR=1			50		

Symbol	Parameter	Condition		Min.	Typ.	Max.	Units
R_Q	Negative impedance [1]	XOSCPWR=0, FRQRANGE=0	0.4MHz resonator, CL=100pF		44k		Ω
			1MHz crystal, CL=20pF		67k		
			2MHz crystal, CL=20pF		67k		
		XOSCPWR=0, FRQRANGE=1, CL=20pF	2MHz crystal		82k		
			8MHz crystal		1500		
			9MHz crystal		1500		
		XOSCPWR=0, FRQRANGE=2, CL=20pF	8MHz crystal		2700		
			9MHz crystal		2700		
			12MHz crystal		1000		
		XOSCPWR=0, FRQRANGE=3, CL=20pF	9MHz crystal		3600		
			12MHz crystal		1300		
			16MHz crystal		590		
		XOSCPWR=1, FRQRANGE=0, CL=20pF	9MHz crystal		390		
			12MHz crystal		50		
			16MHz crystal		10		
R_Q	Negative impedance [1]	XOSCPWR=1, FRQRANGE=1, CL=20pF	9MHz crystal		1500		
			12MHz crystal		650		
			16MHz crystal		270		
		XOSCPWR=1, FRQRANGE=2, CL=20pF	12MHz crystal		1000		
			16MHz crystal		440		
		XOSCPWR=1, FRQRANGE=3, CL=20pF	12MHz crystal		1300		
			16MHz crystal		590		
	ESR	SF = safety factor				min(R_Q)/SF	kΩ
	Start-up time	XOSCPWR=0, FRQRANGE=0	0.4MHz resonator, CL=100pF		1.0		ms
		XOSCPWR=0, FRQRANGE=1	2MHz crystal, CL=20pF		2.6		
		XOSCPWR=0, FRQRANGE=2	8MHz crystal, CL=20pF		0.8		
		XOSCPWR=0, FRQRANGE=3	12MHz crystal, CL=20pF		1.0		
		XOSCPWR=1, FRQRANGE=3	16MHz crystal, CL=20pF		1.4		

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
C_{XTAL1}	Parasitic capacitance XTAL1 pin			5.9		pF
C_{XTAL2}	Parasitic capacitance XTAL2 pin			8.3		
C_{LOAD}	Parasitic capacitance load			3.5		

Note: 1. Numbers for negative impedance are not tested in production but guaranteed from design and characterization.

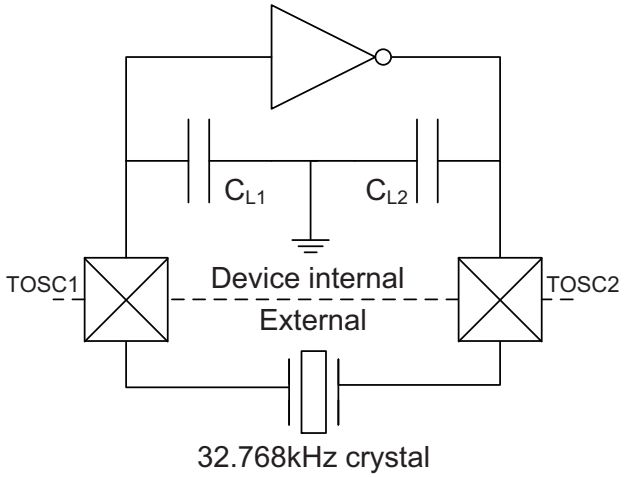
32.1.13.8 External 32.768kHz crystal oscillator and TOSC characteristics

Table 32-27. External 32.768kHz crystal oscillator and TOSC characteristics.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
ESR/R1	Recommended crystal equivalent series resistance (ESR)	Crystal load capacitance 6.5pF			60	kΩ
		Crystal load capacitance 9.0pF			35	
		Crystal load capacitance 12pF			28	
C_{TOSC1}	Parasitic capacitance TOSC1 pin			3.5		pF
C_{TOSC2}	Parasitic capacitance TOSC2 pin			3.5		
	Recommended safety factor	Capacitance load matched to crystal specification	3			

Note: See Figure 32-11 on page 96 for definition.

Figure 32-4. TOSC input capacitance.



The parasitic capacitance between the TOSC pins is C_{L1} + C_{L2} in series as seen from the crystal when oscillating without external capacitors.

32.1.14 SPI characteristics

Figure 32-5. SPI timing requirements in master mode.

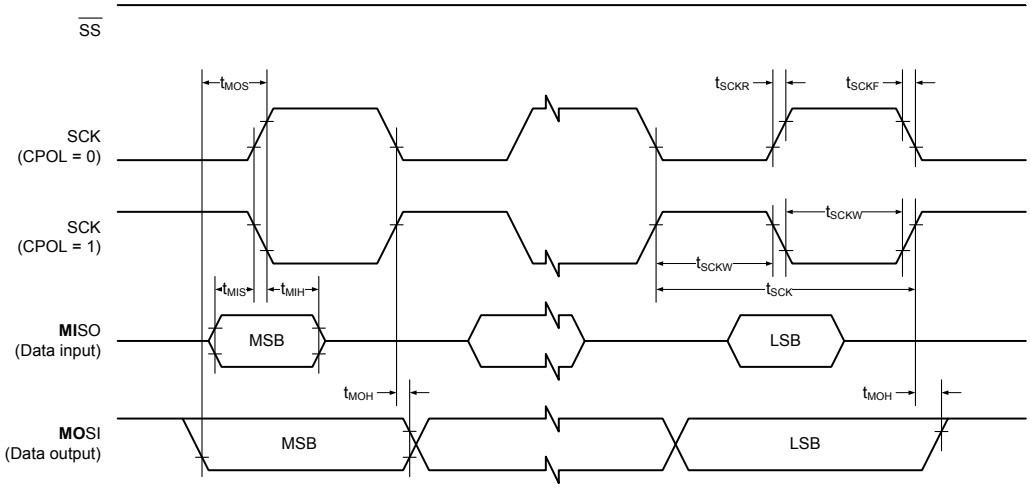


Figure 32-6. SPI timing requirements in slave mode.

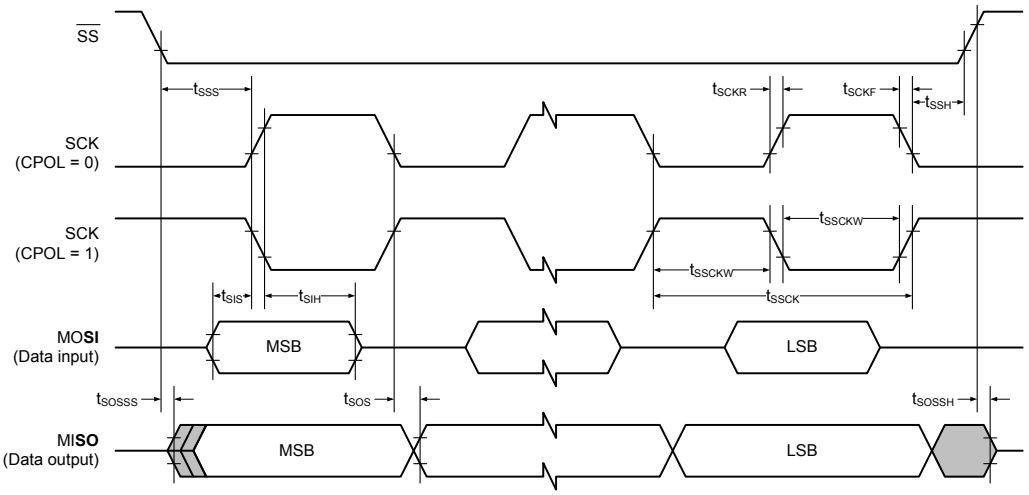


Table 32-28. SPI timing characteristics and requirements.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
t_{SCK}	SCK period	Master		(See Table 20-3 in XMEGA D manual)		ns
t_{SCKW}	SCK high/low width	Master		0.5 * SCK		
t_{SCKR}	SCK rise time	Master		2.7		
t_{SCKF}	SCK fall time	Master		2.7		
t_{MIS}	MISO setup to SCK	Master		10		
t_{MIH}	MISO hold after SCK	Master		10		
t_{MOS}	MOSI setup SCK	Master		0.5 * SCK		
t_{MOH}	MOSI hold after SCK	Master		1		
t_{SSCK}	Slave SCK Period	Slave	4 * t Clk_{PER}			
t_{SSCKW}	SCK high/low width	Slave	2 * t Clk_{PER}			
t_{SSCKR}	SCK rise time	Slave			1600	
t_{SSCKF}	SCK fall time	Slave			1600	
t_{SIS}	MOSI setup to SCK	Slave	3			
t_{SIH}	MOSI hold after SCK	Slave	t Clk_{PER}			
t_{SSS}	$\overline{SS}$ setup to SCK	Slave	21			
t_{SSH}	$\overline{SS}$ hold after SCK	Slave	20			
t_{SOS}	MISO setup SCK	Slave		8		
t_{SOH}	MISO hold after SCK	Slave		13		
t_{SOSS}	MISO setup after $\overline{SS}$ low	Slave		11		
t_{SOSH}	MISO hold after $\overline{SS}$ high	Slave		8		

32.1.15 Two-wire interface characteristics

Table 32-29 on page 81 describes the requirements for devices connected to the two-wire interface bus. The Atmel AVR XMEGA two-wire interface meets or exceeds these requirements under the noted conditions. Timing symbols refer to Figure 32-7.

Figure 32-7. Two-wire interface bus timing.

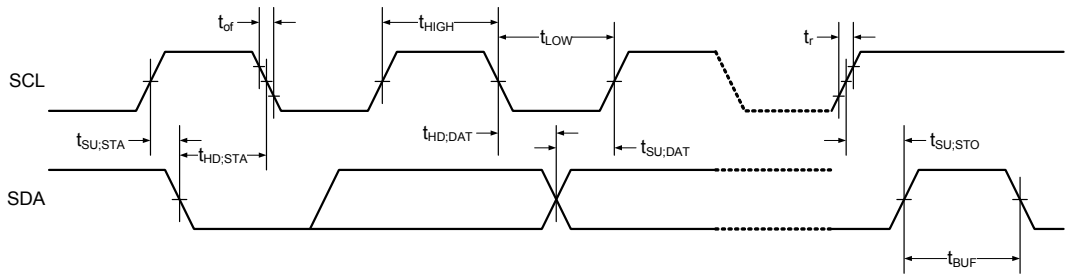


Table 32-29. Two-wire interface characteristics.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
V_{IH}	Input high voltage		$0.7V_{CC}$		V_{CC} + 0.5	V
V_{IL}	Input low voltage		-0.5		$0.3V_{CC}$	
V_{hys}	Hysteresis of Schmitt trigger inputs		$0.05V_{CC}$ (1)			
V_{OL}	Output low voltage	3mA, sink current	0		0.4	
t_r	Rise time for both SDA and SCL		$20 + 0.1C_b$ (1)(2)		300	ns
t_{of}	Output fall time from V_{IHmin} to V_{ILmax}	$10pF < C_b < 400pF$ (2)	$20 + 0.1C_b$ (1)(2)		250	
t_{SP}	Spikes suppressed by input filter		0		50	
I_I	Input current for each I/O pin	$0.1V_{CC} < V_I < 0.9V_{CC}$	-10		10	µA
C_I	Capacitance for each I/O pin				10	pF
f_{SCL}	SCL clock frequency	f_{PER} (3) > max(10f_{SCL}, 250kHz)	0		400	kHz
R_P	Value of pull-up resistor	$f_{SCL} \leq 100kHz$	$\frac{V_{CC}-0.4V}{3mA}$		$\frac{100ns}{C_b}$	Ω
		$f_{SCL} > 100kHz$			$\frac{300ns}{C_b}$	
$t_{HD;STA}$	Hold time (repeated) START condition	$f_{SCL} \leq 100kHz$	4.0			µs
		$f_{SCL} > 100kHz$	0.6			
t_{LOW}	Low period of SCL clock	$f_{SCL} \leq 100kHz$	4.7			
		$f_{SCL} > 100kHz$	1.3			
t_{HIGH}	High period of SCL clock	$f_{SCL} \leq 100kHz$	4.0			
		$f_{SCL} > 100kHz$	0.6			
$t_{SU;STA}$	Set-up time for a repeated START condition	$f_{SCL} \leq 100kHz$	4.7			
		$f_{SCL} > 100kHz$	0.6			
$t_{HD;DAT}$	Data hold time	$f_{SCL} \leq 100kHz$	0		3.45	
		$f_{SCL} > 100kHz$	0		0.9	
$t_{SU;DAT}$	Data setup time	$f_{SCL} \leq 100kHz$	250			
		$f_{SCL} > 100kHz$	100			
$t_{SU;STO}$	Setup time for STOP condition	$f_{SCL} \leq 100kHz$	4.0			
		$f_{SCL} > 100kHz$	0.6			
t_{BUF}	Bus free time between a STOP and START condition	$f_{SCL} \leq 100kHz$	4.7			
		$f_{SCL} > 100kHz$	1.3			

Notes:
1. Required only for $f_{SCL} > 100kHz$.
2. C_b = Capacitance of one bus line in pF.
3. f_{PER} = Peripheral clock frequency.

32.2 Atmel ATxmega64D3

32.2.1 Absolute maximum ratings

Stresses beyond those listed in Table 32-30 under may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Table 32-30. Absolute maximum ratings.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
V_{CC}	Power supply voltage		-0.3		4	V
I_{VCC}	Current into a V_{CC} pin				200	mA
I_{GND}	Current out of a Gnd pin				200	
V_{PIN}	Pin voltage with respect to Gnd and V_{CC}		-0.5		V_{CC} + 0.5	V
I_{PIN}	I/O pin sink/source current		-25		25	mA
T_A	Storage temperature		-65		150	°C
T_j	Junction temperature				150	

32.2.2 General operating ratings

The device must operate within the ratings listed in Table 32-31 in order for all other electrical characteristics and typical characteristics of the device to be valid.

Table 32-31. General operating conditions.

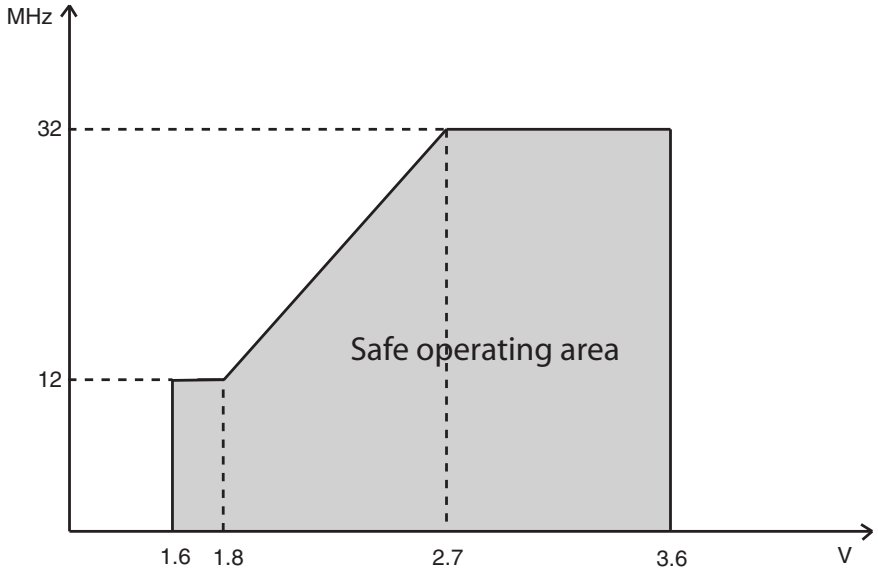
Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
V_{CC}	Power supply voltage		1.60		3.6	V
AV_{CC}	Analog supply voltage		1.60		3.6	
T_A	Temperature range		-40		85	°C
T_j	Junction temperature		-40		105	

Table 32-32. Operating voltage and frequency.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
Clk_{CPU}	CPU clock frequency	V_{CC} = 1.6V	0		12	MHz
		V_{CC} = 1.8V	0		12	
		V_{CC} = 2.7V	0		32	
		V_{CC} = 3.6V	0		32	

The maximum CPU clock frequency depends on V_{CC}. As shown in Figure 32-8 on page 83 the frequency vs. V_{CC} curve is linear between 1.8V < V_{CC} < 2.7V.

Figure 32-8. Maximum frequency vs. V_{CC}.



32.2.3 Current consumption

Table 32-33. Current consumption for Active mode and sleep modes.

Symbol	Parameter	Condition		Min.	Typ.	Max.	Units
I_{CC}	Active power consumption (1)	32kHz, Ext. Clk	V_{CC} = 1.8V		50		µA
			V_{CC} = 3.0V		130		
		1MHz, Ext. Clk	V_{CC} = 1.8V		215		
			V_{CC} = 3.0V		475		
		2MHz, Ext. Clk	V_{CC} = 1.8V		445	600	
			V_{CC} = 3.0V		0.95	1.5	mA
		32MHz, Ext. Clk			7.8	12.0	
	Idle power consumption (1)	32kHz, Ext. Clk	V_{CC} = 1.8V		2.8		µA
			V_{CC} = 3.0V		3		
		1MHz, Ext. Clk	V_{CC} = 1.8V		46		
			V_{CC} = 3.0V		92		
		2MHz, Ext. Clk	V_{CC} = 1.8V		93	225	
			V_{CC} = 3.0V		184	350	
		32MHz, Ext. Clk			2.9	5.0	mA
	Power-down power consumption	T = 25°C	V_{CC} = 3.0V		0.07	1.0	µA
		T = 85°C			1.3	5.0	
		WDT and sampled BOD enabled, T = 25°C	V_{CC} = 3.0V		1.3	2.0	
		WDT and sampled BOD enabled, T = 85°C			2.6	6.0	
	Power-save power consumption (2)	RTC from ULP clock, WDT and sampled BOD enabled, T = 25°C	V_{CC} = 1.8V		1.7		
			V_{CC} = 3.0V		1.8		
		RTC from 1.024kHz low power 32.768kHz TOSC, T = 25°C	V_{CC} = 1.8V		0.5	2.0	
			V_{CC} = 3.0V		0.7	2.0	
		RTC from low power 32.768kHz TOSC, T = 25°C	V_{CC} = 1.8V		0.9	3.0	
			V_{CC} = 3.0V		1.2	3.0	
	Reset power consumption	Current through $\overline{\text{RESET}}$ pin substracted	V_{CC} = 3.0V		120		

Notes:
1. All Power Reduction Registers set.
2. Maximum limits are based on characterization, and not tested in production.

Table 32-34. Current consumption for modules and peripherals.

Symbol	Parameter	Condition [1]			Min.	Typ.	Max.	Units
I_{CC}	ULP oscillator					0.9		µA
	32.768kHz int. oscillator					29		
	2MHz int. oscillator					82		
		DFLL enabled with 32.768kHz int. osc. as reference				114		
	32MHz int. oscillator					250		
		DFLL enabled with 32.768kHz int. osc. as reference				400		
	PLL	20× multiplication factor, 32MHz int. osc. DIV4 as reference				300		
	Watchdog timer					1.0		
	BOD	Continuous mode				140		
		Sampled mode, includes ULP oscillator				1.4		
	Internal 1.0V reference					180		
	Temperature sensor					175		
	ADC	200ksps V_{REF} = Ext. ref.				1.23		mA
			CURRLIMIT = LOW			1.1		
			CURRLIMIT = MEDIUM			0.98		
			CURRLIMIT = HIGH			0.87		
		75ksps V_{REF} = Ext. ref.	CURRLIMIT = LOW			1.7		
		300ksps V_{REF} = Ext. ref.				3.1		
	USART	Rx and Tx enabled, 9600 BAUD				9.7		µA
	Flash memory and EEPROM programming					5		mA

Note: 1. All parameters measured as the difference in current consumption between module enabled and disabled. All data at V_{CC} = 3.0V, Clk_{SYS} = 1MHz external clock without prescaling, T = 25°C unless other conditions are given.

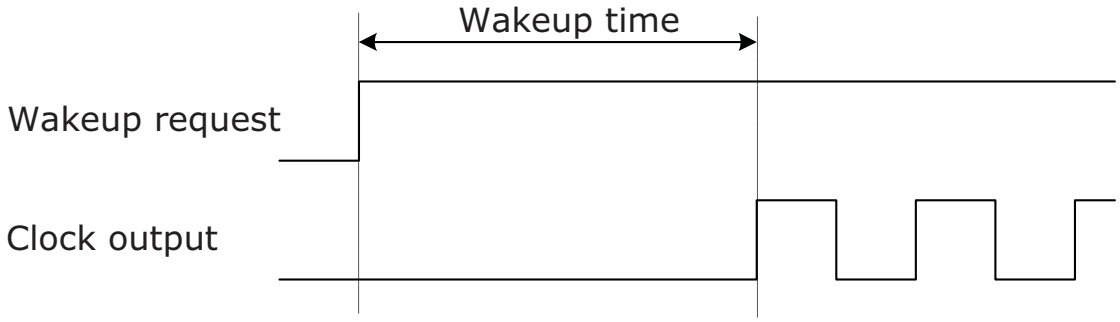
32.2.4 Wake-up time from sleep modes

Table 32-35. Device wake-up time from sleep modes with various system clock sources.

Symbol	Parameter	Condition	Min.	Typ. (1)	Max.	Units
t_{wakeup}	Wake-up time from idle, standby, and extended standby mode	External 2MHz clock		2.0		µs
		32.768kHz internal oscillator		125		
		2MHz internal oscillator		2.0		
		32MHz internal oscillator		0.2		
	Wake-up time from power-save and power-down mode	External 2MHz clock		4.6		
		32.768kHz internal oscillator		330		
		2MHz internal oscillator		9.5		
		32MHz internal oscillator		5.6		

Note: 1. The wake-up time is the time from the wake-up request is given until the peripheral clock is available on pin, see Figure 32-9. All peripherals and modules start execution from the first clock cycle, expect the CPU that is halted for four clock cycles before program execution starts.

Figure 32-9. Wake-up time definition.



32.2.5 I/O pin characteristics

The I/O pins complies with the JEDEC LVTTL and LVCMOS specification and the high- and low level input and output voltage limits reflect or exceed this specification.

Table 32-36. I/O pin characteristics.

Symbol	Parameter	Condition		Min.	Typ.	Max.	Units
I_{OH} (1)/ I_{OL} (2)	I/O pin source/sink current			-15		15	mA
V_{IH}	High level input voltage	V_{CC} = 2.4 - 3.6V		0.7 * V_{CC}		V_{CC} + 0.5	V
		V_{CC} = 1.6 - 2.4V		0.8 * V_{CC}		V_{CC} + 0.5	
V_{IL}	Low level input voltage	V_{CC} = 2.4 - 3.6V		-0.5		0.3 * V_{CC}	
		V_{CC} = 1.6 - 2.4V		-0.5		0.2 * V_{CC}	
V_{OH}	High level output voltage	V_{CC} = 3.3V	I_{OH} = -4mA	2.6	2.9		
		V_{CC} = 3.0V	I_{OH} = -3mA	2.1	2.6		
		V_{CC} = 1.8V	I_{OH} = -1mA	1.4	1.6		
V_{OL}	Low level output voltage	V_{CC} = 3.3V	I_{OL} = 8mA		0.4	0.76	
		V_{CC} = 3.0V	I_{OL} = 5mA		0.3	0.64	
		V_{CC} = 1.8V	I_{OL} = 3mA		0.2	0.46	
I_{IN}	Input leakage current I/O pin	T = 25°C			<0.01	1	µA
R_P	Pull/buss keeper resistor				25		kΩ

Notes:
1. The sum of all I_{OH} for PORTA and PORTB must not exceed 100mA.
   The sum of all I_{OH} for PORTC, PORTD, PORTE must for each port not exceed 200mA.
   The sum of all I_{OH} for pins PF[0-5] on PORTF must not exceed 200mA.
   The sum of all I_{OL} for pins PF[6-7] on PORTF, PORTR and PDI must not exceed 100mA.
2. The sum of all I_{OL} for PORTA and PORTB must not exceed 100mA.
   The sum of all I_{OL} for PORTC, PORTD, PORTE must for each port not exceed 200mA.
   The sum of all I_{OL} for pins PF[0-5] on PORTF must not exceed 200mA.
   The sum of all I_{OL} for pins PF[6-7] on PORTF, PORTR and PDI must not exceed 100mA.

32.2.6 ADC characteristics

Table 32-37. Power supply, reference and input range.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
AV_{CC}	Analog supply voltage		V_{CC} - 0.3		V_{CC} + 0.3	V
V_{REF}	Reference voltage		1		AV_{CC} - 0.6	
R_{in}	Input resistance	Switched			4.5	kΩ
C_{in}	Input capacitance	Switched			5	pF
R_{AREF}	Reference input resistance	(leakage only)		>10		MΩ
C_{AREF}	Reference input capacitance	Static load		7		pF
V_{in}	Input range		0		V_{REF}	V
	Conversion range	Differential mode, Vinp - Vinn	$-V_{REF}$		V_{REF}	
	Conversion range	Single ended unsigned mode, Vinp	-ΔV		V_{REF} - ΔV	
ΔV	Fixed offset voltage			200		lsb

Table 32-38. Clock and timing.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
Clk_{ADC}	ADC clock frequency	Maximum is 1/4 of peripheral clock frequency	100		1800	kHz
		Measuring internal signals	100		125	
f_{ClkADC}	Sample rate		16		300	ksps
f_{ADC}	Sample rate	Current limitation (CURRLIMIT) off	16		300	
		CURRLIMIT = LOW	16		250	
		CURRLIMIT = MEDIUM	16		150	
		CURRLIMIT = HIGH	16		50	
	Sampling time	Configurable in steps of 1/2 Clk_{ADC} cycle up to 32 Clk_{ADC} cycles	0.28		320	µs
	Conversion time (latency)	(RES+2)/2 + 1 + GAIN RES (Resolution) = 8 or 12, GAIN = 0 to 3	5.5		10	Clk_{ADC} cycles
	Start-up time	ADC clock cycles		12	24	
	ADC settling time	After changing reference or input mode		7	7	

Table 32-39. Accuracy characteristics.

Symbol	Parameter	Condition [2]		Min.	Typ.	Max.	Units
RES	Resolution	12-bit resolution	Differential	8	12	12	Bits
			Single ended signed	7	11	11	
			Single ended unsigned	8	12	12	
INL [1]	Integral non-linearity	Differential mode	16ksps, V_{REF} = 3V		0.5	1	lsb
			16ksps, all V_{REF}		0.8	2	
			300ksps, V_{REF} = 3V		0.6	1	
			300ksps, all V_{REF}		1	2	
		Single ended unsigned mode	16ksps, V_{REF} = 3.0V		0.5	1	
			16ksps, all V_{REF}		1.3	2	
DNL [1]	Differential non-linearity	Differential mode	16ksps, V_{REF} = 3V		0.3	1	
			16ksps, all V_{REF}		0.5	1	
			300ksps, V_{REF} = 3V		0.3	1	
			300ksps, all V_{REF}		0.5	1	
		Single ended unsigned mode	16ksps, V_{REF} = 3V		0.6	1	
			16ksps, all V_{REF}		0.6	1	
	Offset error	Differential mode	300ksps, V_{REF} = 3V		-7		mV
			Temperature drift, V_{REF} = 3V		0.01		mV/K
			Operating voltage drift		0.16		mV/V
	Gain error	Differential mode	External reference		-5		mV
			AV_{CC}/1.6		-5		
			AV_{CC}/2.0		-6		
			Bandgap		±10		
			Temperature drift		0.02		mV/K
			Operating voltage drift		2		mV/V
	Gain error	Single ended unsigned mode	External reference		-8		mV
			AV_{CC}/1.6		-8		
			AV_{CC}/2.0		-8		
			Bandgap		±10		
			Temperature drift		0.03		mV/K
			Operating voltage drift		2		mV/V

Notes:
1. Maximum numbers are based on characterisation and not tested in production, and valid for 5% to 95% input voltage range.
2. Unless otherwise noted all linearity, offset and gain error numbers are valid under the condition that external VREF is used.

Table 32-40. Gain stage characteristics.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
R_{in}	Input resistance	Switched in normal mode		4.0		kΩ
C_{sample}	Input capacitance	Switched in normal mode		4.4		pF
	Signal range	Gain stage output	0		AV_{CC} - 0.6	V
	Propagation delay	ADC conversion rate	1/2	1	3	Clk_{ADC} cycles
	Clock frequency	Same as ADC	100		1800	kHz
	Gain error	0.5× gain, normal mode		-1		%
		1× gain, normal mode		-1		
		8× gain, normal mode		-1		
		64× gain, normal mode		5		
	Offset error, input referred	0.5× gain, normal mode		10		mV
		1× gain, normal mode		5		
		8× gain, normal mode		-20		
		64× gain, normal mode		-126		

32.2.7 Analog comparator characteristics

Table 32-41. Analog comparator characteristics.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
V_{off}	Input offset voltage			10		mV
I_{lk}	Input leakage current			<10	50	nA
	Input voltage range		-0.1		AV_{CC}	V
	AC startup time			50		µs
V_{hys1}	Hysteresis, none	V_{CC} = 1.6V - 3.6V		0		mV
V_{hys2}	Hysteresis, small	V_{CC} = 1.6V - 3.6V		15		
V_{hys3}	Hysteresis, large	V_{CC} = 1.6V - 3.6V		30		
t_{delay}	Propagation delay	V_{CC} = 3.0V, T = 85°C		20	40	ns
		V_{CC} = 3.0V		17		
	64-level voltage scaler	Integral non-linearity (INL)		0.3	0.5	lsb
	Current source accuracy after calibration			5		%
	Current source calibration range	Single mode	4		6	µA

32.2.8 Bandgap and internal 1.0V reference characteristics

Table 32-42. Bandgap and internal 1.0V reference characteristics.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
	Startup time	As reference for ADC		1 Clk_{PER} + 2.5µs		µs
		As input voltage to ADC and AC		1.5		
	Bandgap voltage			1.1		V
INT1V	Internal 1.00V reference	T = 85°C, after calibration	0.99	1	1.01	
	Variation over voltage and temperature	Calibrated at T = 85°C		1		%

32.2.9 Brownout detection characteristics

Table 32-43. Brownout detection characteristics [(1)].

Symbol	Parameter (BOD level 0 at 85°C)	Condition	Min.	Typ.	Max.	Units
V_{BOT}	BOD level 0 falling V_{CC}		1.40	1.60	1.70	V
	BOD level 1 falling V_{CC}			1.8		
	BOD level 2 falling V_{CC}			2.0		
	BOD level 3 falling V_{CC}			2.2		
	BOD level 4 falling V_{CC}			2.4		
	BOD level 5 falling V_{CC}			2.6		
	BOD level 6 falling V_{CC}			2.8		
	BOD level 7 falling V_{CC}			3.0		
t_{BOD}	Detection time	Continuous mode		0.4		µs
		Sampled mode		1000		
V_{HYST}	Hysteresis			1.0		%

Note: 1. BOD is calibrated at 85°C within BOD level 0 values, and BOD level 0 is the default level.

32.2.10 External reset characteristics

Table 32-44. External reset characteristics.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
t_{EXT}	Minimum reset pulse width		1000	90		ns
V_{RST}	Reset threshold voltage	V_{CC} = 2.7 - 3.6V		0.45 * V_{CC}		V
		V_{CC} = 1.6 - 2.7V		0.42 * V_{CC}		
R_{RST}	Reset pin pull-up resistor			25		kΩ

32.2.11 Power-on reset characteristics

Table 32-45. Power-on reset characteristics.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
V_{POT-} (1)	POR threshold voltage falling V_{CC}	V_{CC} falls faster than 1V/ms	0.4	1.0		V
		V_{CC} falls at 1V/ms or slower	0.8	1.3		
V_{POT+}	POR threshold voltage rising V_{CC}			1.3	1.59	

Note: 1. V_{POT-} values are only valid when BOD is disabled. When BOD is enabled $V_{POT-} = V_{POT+}$.

32.2.12 Flash and EEPROM memory characteristics

Table 32-46. Endurance and data retention.

Symbol	Parameter	Condition		Min.	Typ.	Max.	Units
	Flash	Write/erase cycles	25°C	10K			Cycle
			85°C	10K			
		Data retention	25°C	100			Year
			55°C	25			
	EEPROM	Write/erase cycles	25°C	100K			Cycle
			85°C	100K			
		Data retention	25°C	100			Year
			55°C	25			

Table 32-47. Programming time.

Symbol	Parameter	Condition	Min.	Typ. (1)	Max.	Units
	Chip erase (2)	64KB Flash, EEPROM		55		ms
	Application erase	Section erase		6		
	Flash	Page erase		4		
		Page write		4		
		Atomic page erase and write		8		
	EEPROM	Page erase		4		
		Page write		4		
		Atomic page erase and write		8		

Notes: 1. Programming is timed from the 2MHz internal oscillator.
2. EEPROM is not erased if the EESAVE fuse is programmed.

32.2.13 Clock and oscillator characteristics

32.2.13.1 Calibrated 32.768kHz internal oscillator characteristics

Table 32-48. 32.768kHz internal oscillator characteristics.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
	Frequency			32.768		kHz
	Factory calibration accuracy	T = 85°C, V_{CC} = 3.0V	-0.5		0.5	%
	User calibration accuracy		-0.5		0.5	

32.2.13.2 Calibrated 2MHz RC internal oscillator characteristics

Table 32-49. 2MHz internal oscillator characteristics.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
	Frequency range	DFLL can tune to this frequency over voltage and temperature	1.8	2.0	2.2	MHz
	Factory calibrated frequency			2.0		
	Factory calibration accuracy	T = 85°C, V_{CC} = 3.0V	-1.5		1.5	%
	User calibration accuracy		-0.2		0.2	
	DFLL calibration stepsize			0.18		

32.2.13.3 Calibrated 32MHz internal oscillator characteristics

Table 32-50. 32MHz internal oscillator characteristics.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
	Frequency range	DFLL can tune to this frequency over voltage and temperature	30	32	55	MHz
	Factory calibrated frequency			32		
	Factory calibration accuracy	T = 85°C, V_{CC} = 3.0V	-1.5		1.5	%
	User calibration accuracy		-0.2		0.2	
	DFLL calibration step size			0.19		

32.2.13.4 32kHz internal ULP oscillator characteristics

Table 32-51. 32kHz internal ULP oscillator characteristics.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
	Factory calibrated frequency			32		kHz
	Factory calibration accuracy	T = 85°C, V_{CC} = 3.0V	-12		12	%
	Accuracy		-30		30	

32.2.13.5 Internal Phase Locked Loop (PLL) characteristics

Table 32-52. Internal PLL characteristics.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
f_{IN}	Input frequency	Output frequency must be within f_{OUT}	0.4		64	MHz
f_{OUT}	Output frequency (1)	V_{CC} = 1.6 - 1.8V	20		48	
		V_{CC} = 2.7 - 3.6V	20		128	
	Start-up time			25		µs
	Re-lock time			25		

Note: 1. The maximum output frequency vs. supply voltage is linear between 1.8V and 2.7V, and can never be higher than four times the maximum CPU frequency.

32.2.13.6 External clock characteristics

Figure 32-10.External clock drive waveform.

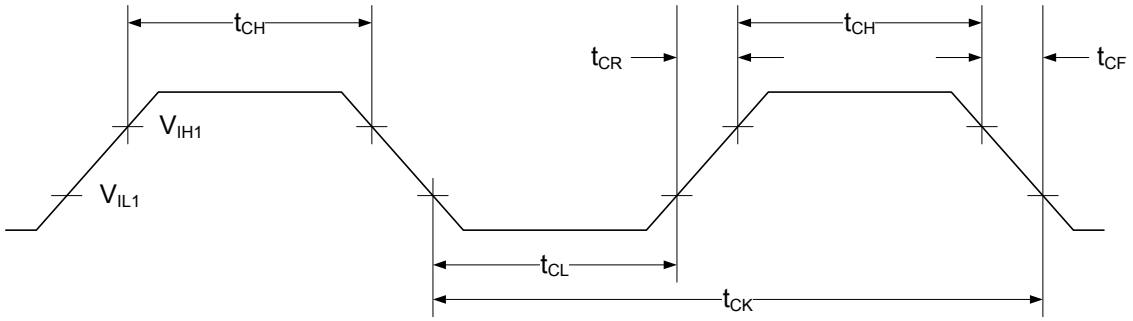


Table 32-53. External clock used as system clock without prescaling.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
$1/t_{CK}$	Clock Frequency (1)	V_{CC} = 1.6 - 1.8V	0		12	MHz
		V_{CC} = 2.7 - 3.6V	0		32	
t_{CK}	Clock Period	V_{CC} = 1.6 - 1.8V	83.3			ns
		V_{CC} = 2.7 - 3.6V	31.5			
t_{CH}	Clock High Time	V_{CC} = 1.6 - 1.8V	30.0			ns
		V_{CC} = 2.7 - 3.6V	12.5			
t_{CL}	Clock Low Time	V_{CC} = 1.6 - 1.8V	30.0			ns
		V_{CC} = 2.7 - 3.6V	12.5			
t_{CR}	Rise Time (for maximum frequency)	V_{CC} = 1.6 - 1.8V			10	ns
		V_{CC} = 2.7 - 3.6V			3	
t_{CF}	Fall Time (for maximum frequency)	V_{CC} = 1.6 - 1.8V			10	ns
		V_{CC} = 2.7 - 3.6V			3	
Δt_{CK}	Change in period from one clock cycle to the next				10	%

Note: 1. The maximum frequency vs. supply voltage is linear between 1.6V and 2.7V, and the same applies for all other parameters with supply voltage conditions.

Table 32-54. External clock with prescaler [1] for system clock.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
$1/t_{CK}$	Clock Frequency [2]	V_{CC} = 1.6 - 1.8V	0		90	MHz
		V_{CC} = 2.7 - 3.6V	0		142	
t_{CK}	Clock Period	V_{CC} = 1.6 - 1.8V	11			ns
		V_{CC} = 2.7 - 3.6V	7			
t_{CH}	Clock High Time	V_{CC} = 1.6 - 1.8V	4.5			ns
		V_{CC} = 2.7 - 3.6V	2.4			
t_{CL}	Clock Low Time	V_{CC} = 1.6 - 1.8V	4.5			ns
		V_{CC} = 2.7 - 3.6V	2.4			
t_{CR}	Rise Time (for maximum frequency)	V_{CC} = 1.6 - 1.8V			1.5	ns
		V_{CC} = 2.7 - 3.6V			1.0	
t_{CF}	Fall Time (for maximum frequency)	V_{CC} = 1.6 - 1.8V			1.5	ns
		V_{CC} = 2.7 - 3.6V			1.0	
Δt_{CK}	Change in period from one clock cycle to the next				10	%

Notes: 1. System Clock Prescalers must be set so that maximum CPU clock frequency for device is not exceeded.
2. The maximum frequency vs. supply voltage is linear between 1.6V and 2.7V, and the same applies for all other parameters with supply voltage conditions.

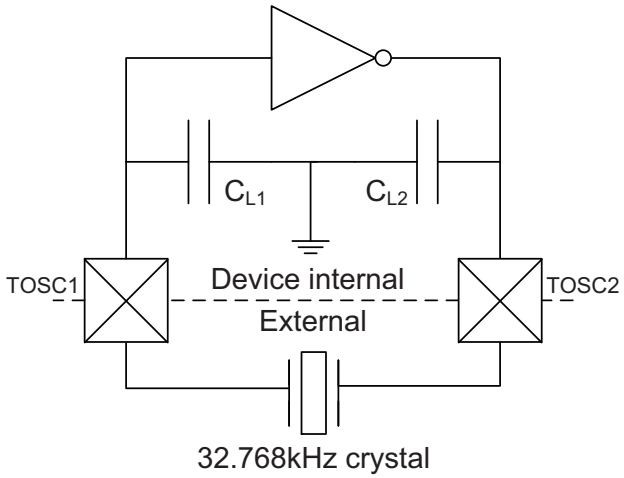
32.2.13.7 External 32.768kHz crystal oscillator and TOSC characteristics

Table 32-55. External 32.768kHz crystal oscillator and TOSC characteristics.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
ESR/R1	Recommended crystal equivalent series resistance (ESR)	Crystal load capacitance 6.5pF			60	kΩ
		Crystal load capacitance 9.0pF			35	
		Crystal load capacitance 12pF			28	
C_{TOSC1}	Parasitic capacitance TOSC1 pin			3.5		pF
C_{TOSC2}	Parasitic capacitance TOSC2 pin			3.5		
	Recommended safety factor	Capacitance load matched to crystal specification	3			

Note: See Figure 32-11 for definition.

Figure 32-11.TOSC input capacitance.



The parasitic capacitance between the TOSC pins is C_{L1} + C_{L2} in series as seen from the crystal when oscillating without external capacitors.

32.2.14 SPI characteristics

Figure 32-12.SPI timing requirements in master mode.

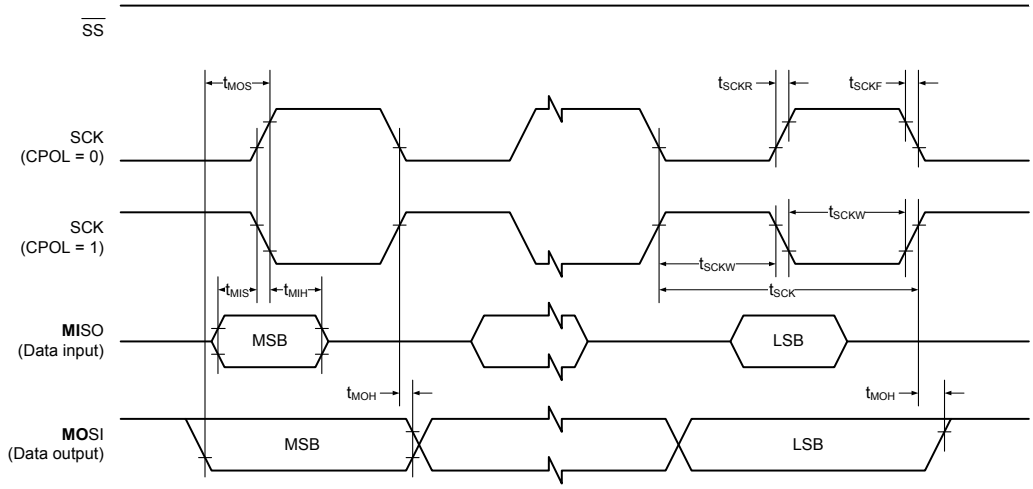


Figure 32-13.SPI timing requirements in slave mode.

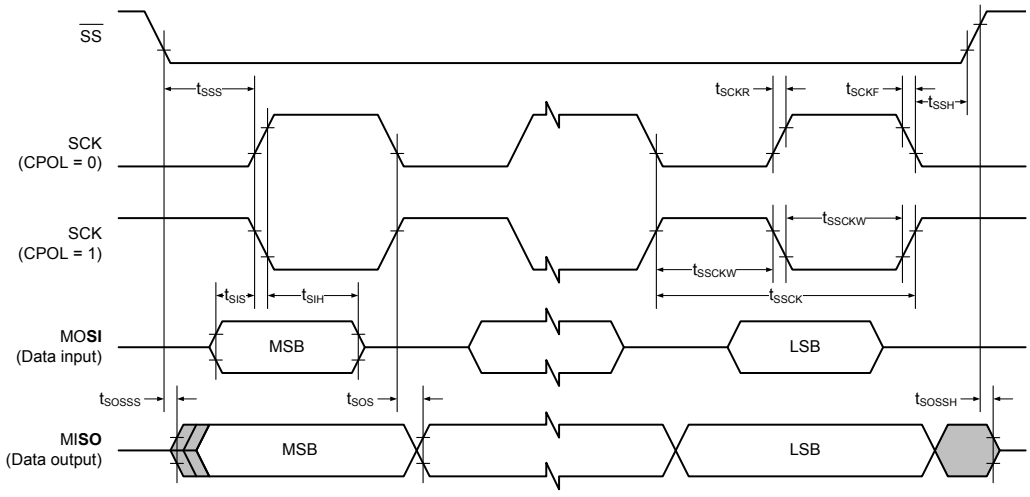


Table 32-56. SPI timing characteristics and requirements.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
t_{SCK}	SCK period	Master		(See Table 20-3 in XMEGA D manual)		ns
t_{SCKW}	SCK high/low width	Master		0.5 * SCK		
t_{SCKR}	SCK rise time	Master		2.7		
t_{SCKF}	SCK fall time	Master		2.7		
t_{MIS}	MISO setup to SCK	Master		10		
t_{MIH}	MISO hold after SCK	Master		10		
t_{MOS}	MOSI setup SCK	Master		0.5 * SCK		
t_{MOH}	MOSI hold after SCK	Master		1		
t_{SSCK}	Slave SCK Period	Slave	4 * t Clk_{PER}			
t_{SSCKW}	SCK high/low width	Slave	2 * t Clk_{PER}			
t_{SSCKR}	SCK rise time	Slave			1600	
t_{SSCKF}	SCK fall time	Slave			1600	
t_{SIS}	MOSI setup to SCK	Slave	3			
t_{SIH}	MOSI hold after SCK	Slave	t Clk_{PER}			
t_{SSS}	$\overline{SS}$ setup to SCK	Slave	21			
t_{SSH}	$\overline{SS}$ hold after SCK	Slave	20			
t_{SOS}	MISO setup SCK	Slave		8		
t_{SOH}	MISO hold after SCK	Slave		13		
t_{SOSS}	MISO setup after $\overline{SS}$ low	Slave		11		
t_{SOSH}	MISO hold after $\overline{SS}$ high	Slave		8		

32.2.15 Two-wire interface characteristics

Table 32-57 on page 98 describes the requirements for devices connected to the two-wire interface bus. The Atmel AVR XMEGA two-wire interface meets or exceeds these requirements under the noted conditions. Timing symbols refer to Figure 32-14 on page 97.

Figure 32-14.Two-wire interface bus timing.

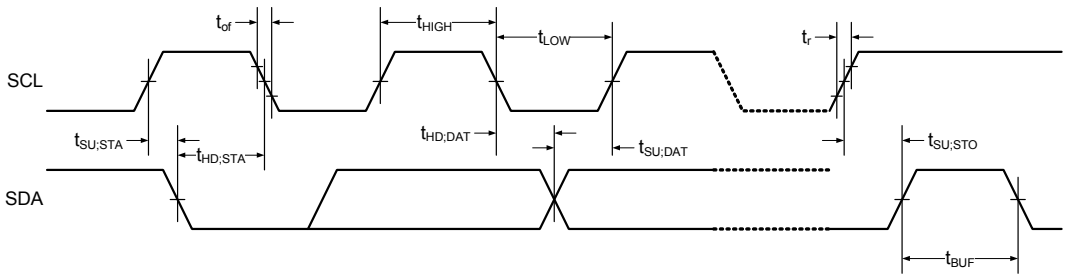


Table 32-57. Two-wire interface characteristics.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
V_{IH}	Input high voltage		$0.7V_{CC}$		V_{CC} + 0.5	V
V_{IL}	Input low voltage		-0.5		$0.3V_{CC}$	
V_{hys}	Hysteresis of Schmitt trigger inputs		$0.05V_{CC}$ (1)			
V_{OL}	Output low voltage	3mA, sink current	0		0.4	
t_r	Rise time for both SDA and SCL		$20 + 0.1C_b$ (1)(2)		300	ns
t_{of}	Output fall time from V_{IHmin} to V_{ILmax}	$10pF < C_b < 400pF$ (2)	$20 + 0.1C_b$ (1)(2)		250	
t_{SP}	Spikes suppressed by input filter		0		50	
I_I	Input current for each I/O pin	$0.1V_{CC} < V_I < 0.9V_{CC}$	-10		10	µA
C_I	Capacitance for each I/O pin				10	pF
f_{SCL}	SCL clock frequency	f_{PER} (3) > max($10f_{SCL}$, 250kHz)	0		400	kHz
R_P	Value of pull-up resistor	$f_{SCL} \leq 100kHz$	$\frac{V_{CC}-0.4V}{3mA}$		$\frac{100ns}{C_b}$	Ω
		$f_{SCL} > 100kHz$			$\frac{300ns}{C_b}$	
$t_{HD;STA}$	Hold time (repeated) START condition	$f_{SCL} \leq 100kHz$	4.0			µs
		$f_{SCL} > 100kHz$	0.6			
t_{LOW}	Low period of SCL clock	$f_{SCL} \leq 100kHz$	4.7			
		$f_{SCL} > 100kHz$	1.3			
t_{HIGH}	High period of SCL clock	$f_{SCL} \leq 100kHz$	4.0			
		$f_{SCL} > 100kHz$	0.6			
$t_{SU;STA}$	Set-up time for a repeated START condition	$f_{SCL} \leq 100kHz$	4.7			
		$f_{SCL} > 100kHz$	0.6			
$t_{HD;DAT}$	Data hold time	$f_{SCL} \leq 100kHz$	0		3.45	µs
		$f_{SCL} > 100kHz$	0		0.9	
$t_{SU;DAT}$	Data setup time	$f_{SCL} \leq 100kHz$	250			
		$f_{SCL} > 100kHz$	100			
$t_{SU;STO}$	Setup time for STOP condition	$f_{SCL} \leq 100kHz$	4.0			
		$f_{SCL} > 100kHz$	0.6			
t_{BUF}	Bus free time between a STOP and START condition	$f_{SCL} \leq 100kHz$	4.7			
		$f_{SCL} > 100kHz$	1.3			

Notes:
1. Required only for $f_{SCL} > 100kHz$.
2. C_b = Capacitance of one bus line in pF.
3. f_{PER} = Peripheral clock frequency.

32.3 Atmel ATxmega128D3

32.3.1 Absolute maximum ratings

Stresses beyond those listed in Table 32-58 under may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Table 32-58. Absolute maximum ratings.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
V_{CC}	Power supply voltage		-0.3		4	V
I_{VCC}	Current into a V_{CC} pin				200	mA
I_{GND}	Current out of a Gnd pin				200	
V_{PIN}	Pin voltage with respect to Gnd and V_{CC}		-0.5		V_{CC} + 0.5	V
I_{PIN}	I/O pin sink/source current		-25		25	mA
T_A	Storage temperature		-65		150	°C
T_j	Junction temperature				150	

32.3.2 General operating ratings

The device must operate within the ratings listed in Table 32-59 in order for all other electrical characteristics and typical characteristics of the device to be valid.

Table 32-59. General operating conditions.

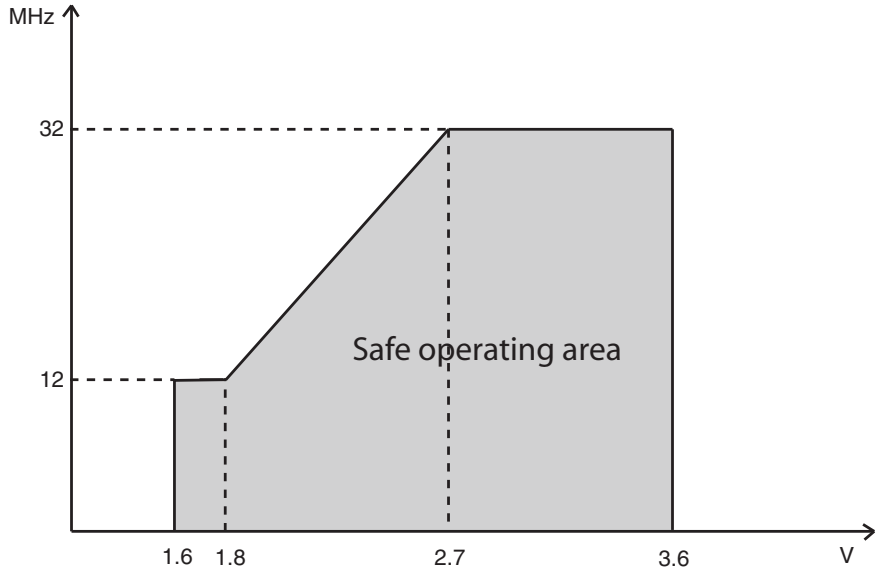
Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
V_{CC}	Power supply voltage		1.60		3.6	V
AV_{CC}	Analog supply voltage		1.60		3.6	
T_A	Temperature range		-40		85	°C
T_j	Junction temperature		-40		105	

Table 32-60. Operating voltage and frequency.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
Clk_{CPU}	CPU clock frequency	V_{CC} = 1.6V	0		12	MHz
		V_{CC} = 1.8V	0		12	
		V_{CC} = 2.7V	0		32	
		V_{CC} = 3.6V	0		32	

The maximum CPU clock frequency depends on V_{CC}. As shown in Figure 32-15 on page 100 the frequency vs. V_{CC} curve is linear between 1.8V < V_{CC} < 2.7V.

Figure 32-15.Maximum frequency vs. V_{CC}.



32.3.3 Current consumption

Table 32-61. Current consumption for Active mode and sleep modes.

Symbol	Parameter	Condition		Min.	Typ.	Max.	Units
I_{CC}	Active power consumption (1)	32kHz, Ext. Clk	V_{CC} = 1.8V		55		µA
			V_{CC} = 3.0V		135		
		1MHz, Ext. Clk	V_{CC} = 1.8V		237		
			V_{CC} = 3.0V		515		
		2MHz, Ext. Clk	V_{CC} = 1.8V		425	700	
			V_{CC} = 3.0V		0.9	1.5	mA
		32MHz, Ext. Clk			8.3	12	
	Idle power consumption (1)	32kHz, Ext. Clk	V_{CC} = 1.8V		2.8		µA
			V_{CC} = 3.0V		3.1		
		1MHz, Ext. Clk	V_{CC} = 1.8V		47		
			V_{CC} = 3.0V		95		
		2MHz, Ext. Clk	V_{CC} = 1.8V		94	200	
			V_{CC} = 3.0V		190	400	
		32MHz, Ext. Clk			3.0	7.0	mA
	Power-down power consumption	T = 25°C	V_{CC} = 3.0V		0.1	1.0	µA
		T = 85°C			1.9	4.0	
		WDT and sampled BOD enabled, T = 25°C	V_{CC} = 3.0V		1.5	2.0	
		WDT and sampled BOD enabled, T = 85°C			3.0	8.0	
	Power-save power consumption (2)	RTC from ULP clock, WDT and sampled BOD enabled, T = 25°C	V_{CC} = 1.8V		1.3		
			V_{CC} = 3.0V		1.4		
		RTC from 1.024kHz low power 32.768kHz TOSC, T = 25°C	V_{CC} = 1.8V		0.7	2.0	
			V_{CC} = 3.0V		0.8	2.0	
		RTC from low power 32.768kHz TOSC, T = 25°C	V_{CC} = 1.8V		0.9	3.0	
			V_{CC} = 3.0V		1.1	3.0	
	Reset power consumption	Current through $\overline{\text{RESET}}$ pin substracted	V_{CC} = 3.0V		145		

Notes:
1. All Power Reduction Registers set.
2. Maximum limits are based on characterization, and not tested in production.

Table 32-62. Current consumption for modules and peripherals.

Symbol	Parameter	Condition [1]		Min.	Typ.	Max.	Units
I_{CC}	ULP oscillator				0.9		µA
	32.768kHz int. oscillator				26		
	2MHz int. oscillator				79		
		DFLL enabled with 32.768kHz int. osc. as reference			110		
	32MHz int. oscillator				245		
		DFLL enabled with 32.768kHz int. osc. as reference			415		
	PLL	20× multiplication factor, 32MHz int. osc. DIV4 as reference			305		
	Watchdog timer				1.0		
	BOD	Continuous mode			138		
		Sampled mode, includes ULP oscillator			1.4		
	Internal 1.0V reference				185		
	Temperature sensor				173		
	ADC	16ksps V_{REF} = Ext. ref.			1.3		mA
			CURRLIMIT = LOW		1.15		
			CURRLIMIT = MEDIUM		1.0		
			CURRLIMIT = HIGH		0.9		
		75ksps V_{REF} = Ext. ref.	CURRLIMIT = LOW		1.7		
		300ksps V_{REF} = Ext. ref.			3.1		
	USART	Rx and Tx enabled, 9600 BAUD			7.5		µA
	Flash memory and EEPROM programming				4		mA

Note: 1. All parameters measured as the difference in current consumption between module enabled and disabled. All data at V_{CC} = 3.0V, Clk_{SYS} = 1MHz external clock without prescaling, T = 25°C unless other conditions are given.

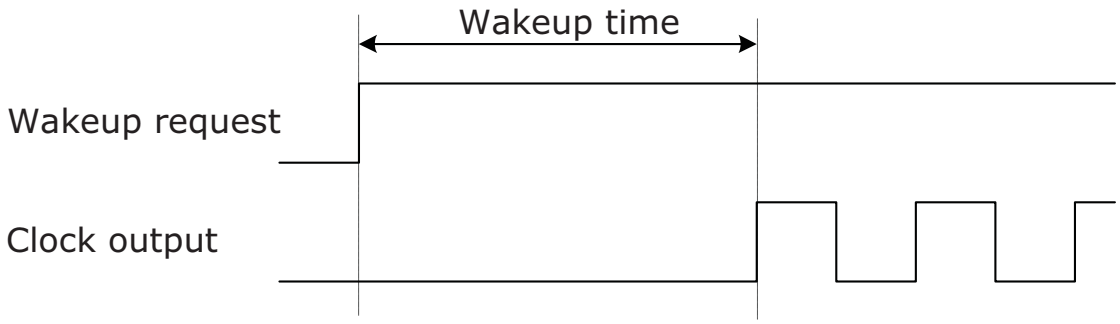
32.3.4 Wake-up time from sleep modes

Table 32-63. Device wake-up time from sleep modes with various system clock sources.

Symbol	Parameter	Condition	Min.	Typ. (1)	Max.	Units
t_{wakeup}	Wake-up time from idle, standby, and extended standby mode	External 2MHz clock		2.0		µs
		32.768kHz internal oscillator		130		
		2MHz internal oscillator		2.0		
		32MHz internal oscillator		0.2		
	Wake-up time from power-save and power-down mode	External 2MHz clock		4.5		
		32.768kHz internal oscillator		320		
		2MHz internal oscillator		9.0		
		32MHz internal oscillator		5.0		

Note: 1. The wake-up time is the time from the wake-up request is given until the peripheral clock is available on pin, see Figure 32-16. All peripherals and modules start execution from the first clock cycle, expect the CPU that is halted for four clock cycles before program execution starts.

Figure 32-16.Wake-up time definition.



32.3.5 I/O pin characteristics

The I/O pins compiles with the JEDEC LVTTL and LVCMOS specification and the high- and low level input and output voltage limits or exceeds this specification.

Table 32-64. I/O pin characteristics.

Symbol	Parameter	Condition		Min.	Typ.	Max.	Units
I_{OH} (1)/ I_{OL} (2)	I/O pin source/sink current			-15		15	mA
V_{IH}	High level input voltage	V_{CC} = 2.4 - 3.6V		0.7 * V_{CC}		V_{CC} + 0.5	V
		V_{CC} = 1.6 - 2.4V		0.8 * V_{CC}		V_{CC} + 0.5	
V_{IL}	Low level input voltage	V_{CC} = 2.4 - 3.6V		-0.5		0.3 * V_{CC}	
		V_{CC} = 1.6 - 2.4V		-0.5		0.2 * V_{CC}	
V_{OH}	High level output voltage	V_{CC} = 3.3V	I_{OH} = -4mA	2.6	2.9		
		V_{CC} = 3.0V	I_{OH} = -3mA	2.1	2.6		
		V_{CC} = 1.8V	I_{OH} = -1mA	1.4	1.6		
V_{OL}	Low level output voltage	V_{CC} = 3.3V	I_{OL} = 8mA		0.4	0.76	
		V_{CC} = 3.0V	I_{OL} = 5mA		0.3	0.64	
		V_{CC} = 1.8V	I_{OL} = 3mA		0.2	0.46	
I_{IN}	Input leakage current I/O pin	T = 25°C			<0.01	1.0	µA
R_P	Pull/buss keeper resistor				25		kΩ

Notes:
1. The sum of all I_{OH} for PORTA and PORTB must not exceed 100mA.
   The sum of all I_{OH} for PORTC, PORTD, PORTE must for each port not exceed 200mA.
   The sum of all I_{OH} for pins PF[0-5] on PORTF must not exceed 200mA.
   The sum of all I_{OL} for pins PF[6-7] on PORTF, PORTR and PDI must not exceed 100mA.
2. The sum of all I_{OL} for PORTA and PORTB must not exceed 100mA.
   The sum of all I_{OL} for PORTC, PORTD, PORTE must for each port not exceed 200mA.
   The sum of all I_{OL} for pins PF[0-5] on PORTF must not exceed 200mA.
   The sum of all I_{OL} for pins PF[6-7] on PORTF, PORTR and PDI must not exceed 100mA.

32.3.6 ADC characteristics

Table 32-65. Power supply, reference and input range.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
AV_{CC}	Analog supply voltage		V_{CC} - 0.3		V_{CC} + 0.3	V
V_{REF}	Reference voltage		1		AV_{CC} - 0.6	
R_{in}	Input resistance	Switched			4.5	kΩ
C_{in}	Input capacitance	Switched			5	pF
R_{AREF}	Reference input resistance	(leakage only)		>10		MΩ
C_{AREF}	Reference input capacitance	Static load		7		pF
V_{in}	Input range		0		V_{REF}	V
	Conversion range	Differential mode, Vinp - Vinn	$-V_{REF}$		V_{REF}	
	Conversion range	Single ended unsigned mode, Vinp	-ΔV		V_{REF} - ΔV	
ΔV	Fixed offset voltage			200		lsb

Table 32-66. Clock and timing.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
Clk_{ADC}	ADC clock frequency	Maximum is 1/4 of peripheral clock frequency	100		1800	kHz
		Measuring internal signals	100		125	
f_{ClkADC}	Sample rate		16		300	ksps
f_{ADC}	Sample rate	Current limitation (CURRLIMIT) off	16		300	ksps
		CURRLIMIT = LOW	16		250	
		CURRLIMIT = MEDIUM	16		150	
		CURRLIMIT = HIGH	16		50	
	Sampling time	1/2 Clk_{ADC} cycle	0.28		320	µs
	Conversion time (latency)	(RES+2)/2 + GAIN RES (Resolution) = 8 or 12, GAIN = 0 to 3	5.5		10	Clk_{ADC} cycles
	Start-up time	ADC clock cycles		12	24	
	ADC settling time	After changing reference or input mode		7	7	

Table 32-67. Accuracy characteristics.

Symbol	Parameter	Condition [2]		Min.	Typ.	Max.	Units
RES	Resolution	12-bit resolution	Differential	8	12	12	Bits
			Single ended signed	7	11	11	
			Single ended unsigned	8	12	12	
INL [1]	Integral non-linearity	Differential mode	16ksps, V_{REF} = 3V		0.5	1	lsb
			16ksps, all V_{REF}		0.8	2	
			300ksps, V_{REF} = 3V		0.6	1	
			300ksps, all V_{REF}		1.0	2	
		Single ended unsigned mode	16ksps, V_{REF} = 3.0V		0.5	1	
			16ksps, all V_{REF}		1.3	2	
DNL [1]	Differential non-linearity	Differential mode	16ksps, V_{REF} = 3V		0.3	1	lsb
			16ksps, all V_{REF}		0.5	1	
			300ksps, V_{REF} = 3V		0.3	1	
			300ksps, all V_{REF}		0.5	1	
		Single ended unsigned mode	16ksps, V_{REF} = 3.0V		0.6	1	
			16ksps, all V_{REF}		0.6	1	
	Offset error	Differential mode	300ksps, V_{REF} = 3V		-7		mV
			Temperature drift, V_{REF} = 3V		0.01		mV/K
			Operating voltage drift		0.16		mV/V
	Gain error	Differential mode	External reference		-5		mV
			AV_{CC}/1.6		-5		
			AV_{CC}/2.0		-6		
			Bandgap		±10		
			Temperature drift		0.02		mV/K
			Operating voltage drift		2		mV/V
	Gain error	Single ended unsigned mode	External reference		-8		mV
			AV_{CC}/1.6		-8		
			AV_{CC}/2.0		-8		
			Bandgap		±10		
			Temperature drift		0.03		mV/K
			Operating voltage drift		2		mV/V

Notes:
1. Maximum numbers are based on characterization and not tested in production and valid for 5% to 95% input voltage range.
2. Unless otherwise noted all linearity, offset and gain error numbers are valid under the condition that external VREF is used.

Table 32-68. Gain stage characteristics.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
R_{in}	Input resistance	Switched in normal mode		4.0		kΩ
C_{sample}	Input capacitance	Switched in normal mode		4.4		pF
	Signal range	Gain stage output	0		AV_{CC} - 0.6	V
	Propagation delay	ADC conversion rate	1/2	1	3	Clk_{ADC} cycles
	Clock frequency	Same as ADC	100		1800	kHz
	Gain error	0.5x gain, normal mode		-1		%
		1x gain, normal mode		-1		
		8x gain, normal mode		-1		
		64x gain, normal mode		5		
	Offset error, input referred	0.5x gain, normal mode		10		mV
		1x gain, normal mode		5		
		8x gain, normal mode		-20		
		64x gain, normal mode		-126		

32.3.7 Analog comparator characteristics

Table 32-69. Analog comparator characteristics.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
V_{off}	Input offset voltage			10		mV
I_{lk}	Input leakage current			<10	50	nA
	Input voltage range		-0.1		AV_{CC}	V
	AC startup time			50		µs
V_{hys1}	Hysteresis, none	V_{CC} = 1.6V - 3.6V		0		mV
V_{hys2}	Hysteresis, small	V_{CC} = 1.6V - 3.6V		15		
V_{hys3}	Hysteresis, large	V_{CC} = 1.6V - 3.6V		30		
t_{delay}	Propagation delay	V_{CC} = 3.0V, T = 85°C		20	90	ns
		V_{CC} = 3.0V		17		
	64-level voltage scaler	Integral non-linearity (INL)		0.3	0.5	lsb
	Current source accuracy after calibration			5		%
	Current source calibration range	Single mode	4		6	µA

32.3.8 Bandgap and internal 1.0V reference characteristics

Table 32-70. Bandgap and internal 1.0V reference characteristics.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
	Startup time	As reference for ADC		1 Clk_{PER} + 2.5µs		µs
		As input voltage to ADC and AC		1.5		
	Bandgap voltage			1.1		V
INT1V	Internal 1.00V reference	T = 85°C, after calibration	0.99	1.0	1.01	
	Variation over voltage and temperature	Calibrated at T = 85°C		1		%

32.3.9 Brownout detection characteristics

Table 32-71. Brownout detection characteristics (1).

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
V_{BOT}	BOD level 0 falling V_{CC}		1.40	1.60	1.70	V
	BOD level 1 falling V_{CC}			1.8		
	BOD level 2 falling V_{CC}			2.0		
	BOD level 3 falling V_{CC}			2.2		
	BOD level 4 falling V_{CC}			2.4		
	BOD level 5 falling V_{CC}			2.6		
	BOD level 6 falling V_{CC}			2.8		
	BOD level 7 falling V_{CC}			3.0		
t_{BOD}	Detection time	Continuous mode		0.4		µs
		Sampled mode		1000		
V_{HYST}	Hysteresis			1.0		%

Note: 1. BOD is calibrated at 85°C within BOD level 0 values, and BOD level 0 is the default level.

32.3.10 External reset characteristics

Table 32-72. External reset characteristics.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
t_{EXT}	Minimum reset pulse width		1000	100		ns
V_{RST}	Reset threshold voltage	V_{CC} = 2.7 - 3.6V		0.45 * V_{CC}		V
		V_{CC} = 1.6 - 2.7V		0.45 * V_{CC}		
R_{RST}	Reset pin pull-up resistor			27		kΩ

32.3.11 Power-on reset characteristics

Table 32-73. Power-on reset characteristics.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
V_{POT-} (1)	POR threshold voltage falling V_{CC}	V_{CC} falls faster than 1V/ms	0.4	1.0		V
		V_{CC} falls at 1V/ms or slower	0.8	1.3		
V_{POT+}	POR threshold voltage rising V_{CC}			1.3	1.59	

Note: 1. V_{POT-} values are only valid when BOD is disabled. When BOD is enabled $V_{POT-} = V_{POT+}$.

32.3.12 Flash and EEPROM memory characteristics

Table 32-74. Endurance and data retention.

Symbol	Parameter	Condition		Min.	Typ.	Max.	Units
	Flash	Write/erase cycles	25°C	10K			Cycle
			85°C	10K			
		Data retention	25°C	100			Year
			55°C	25			
	EEPROM	Write/erase cycles	25°C	100K			Cycle
			85°C	100K			
		Data retention	25°C	100			Year
			55°C	25			

Table 32-75. Programming time.

Symbol	Parameter	Condition	Min.	Typ. (1)	Max.	Units
	Chip erase (2)	128KB Flash, EEPROM		75		ms
	Application erase	Section erase		6		
	Flash	Page erase		4		
		Page write		4		
		Atomic page erase and write		8		
	EEPROM	Page erase		4		
		Page write		4		
		Atomic page erase and write		8		

Notes: 1. Programming is timed from the 2MHz internal oscillator.
2. EEPROM is not erased if the EESAVE fuse is programmed.

32.3.13 Clock and oscillator characteristics

32.3.13.1 Calibrated 32.768kHz internal oscillator characteristics

Table 32-76. 32.768kHz internal oscillator characteristics.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
	Frequency			32.768		kHz
	Factory calibration accuracy	T = 85°C, V_{CC} = 3.0V	-0.5		0.5	%
	User calibration accuracy		-0.5		0.5	

32.3.13.2 Calibrated 2MHz RC internal oscillator characteristics

Table 32-77. 2MHz internal oscillator characteristics.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
	Frequency range	DFLL can tune to this frequency over voltage and temperature	1.8	2.0	2.2	MHz
	Factory calibrated frequency			2.0		
	Factory calibration accuracy	T = 85°C, V_{CC} = 3.0V	-1.5		1.5	%
	User calibration accuracy		-0.2		0.2	
	DFLL calibration stepsize			0.18		

32.3.13.3 Calibrated 32MHz internal oscillator characteristics

Table 32-78. 32MHz internal oscillator characteristics.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
	Frequency range	DFLL can tune to this frequency over voltage and temperature	30	32	55	MHz
	Factory calibrated frequency			32		
	Factory calibration accuracy	T = 85°C, V_{CC} = 3.0V	-1.5		1.5	%
	User calibration accuracy		-0.2		0.2	
	DFLL calibration step size			0.2		

32.3.13.4 32kHz internal ULP oscillator characteristics

Table 32-79. 32kHz internal ULP oscillator characteristics.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
	Factory calibrated frequency			32		kHz
	Factory calibration accuracy	T = 85°C, V_{CC} = 3.0V	-12		12	%
	Accuracy		-30		30	

32.3.13.5 Internal Phase Locked Loop (PLL) characteristics

Table 32-80. Internal PLL characteristics.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
f_{IN}	Input frequency	Output frequency must be within f_{OUT}	0.4		64	MHz
f_{OUT}	Output frequency (1)	V_{CC} = 1.6 - 1.8V	20		48	
		V_{CC} = 2.7 - 3.6V	20		128	
	Start-up time			25		µs
	Re-lock time			25		

Note: 1. The maximum output frequency vs. supply voltage is linear between 1.8V and 2.7V, and can never be higher than four times the maximum CPU frequency.

32.3.13.6 External clock characteristics

Figure 32-17.External clock drive waveform.

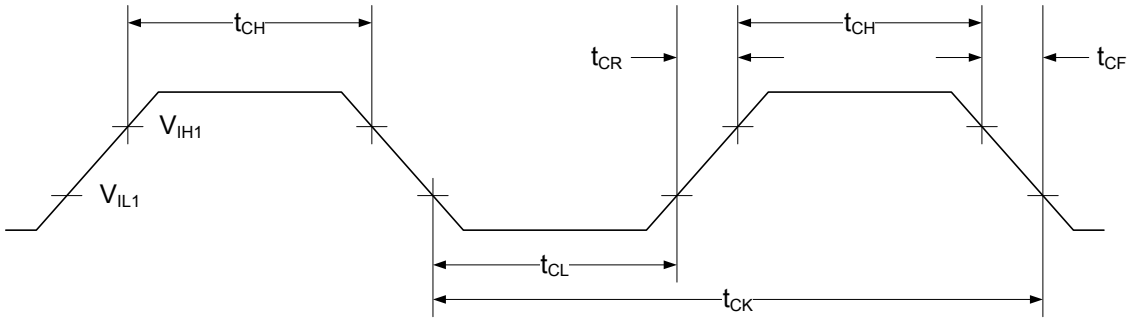


Table 32-81. External clock used as system clock without prescaling.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
$1/t_{CK}$	Clock Frequency (1)	V_{CC} = 1.6 - 1.8V	0		12	MHz
		V_{CC} = 2.7 - 3.6V	0		32	
t_{CK}	Clock Period	V_{CC} = 1.6 - 1.8V	83.3			ns
		V_{CC} = 2.7 - 3.6V	31.5			
t_{CH}	Clock High Time	V_{CC} = 1.6 - 1.8V	30.0			ns
		V_{CC} = 2.7 - 3.6V	12.5			
t_{CL}	Clock Low Time	V_{CC} = 1.6 - 1.8V	30.0			ns
		V_{CC} = 2.7 - 3.6V	12.5			
t_{CR}	Rise Time (for maximum frequency)	V_{CC} = 1.6 - 1.8V			10	ns
		V_{CC} = 2.7 - 3.6V			3	
t_{CF}	Fall Time (for maximum frequency)	V_{CC} = 1.6 - 1.8V			10	ns
		V_{CC} = 2.7 - 3.6V			3	
Δt_{CK}	Change in period from one clock cycle to the next				10	%

Note: 1. The maximum frequency vs. supply voltage is linear between 1.6V and 2.7V, and the same applies for all other parameters with supply voltage conditions.

Table 32-82. External clock with prescaler [1] for system clock.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
$1/t_{CK}$	Clock Frequency [2]	V_{CC} = 1.6 - 1.8V	0		90	MHz
		V_{CC} = 2.7 - 3.6V	0		142	
t_{CK}	Clock Period	V_{CC} = 1.6 - 1.8V	11			ns
		V_{CC} = 2.7 - 3.6V	7			
t_{CH}	Clock High Time	V_{CC} = 1.6 - 1.8V	4.5			ns
		V_{CC} = 2.7 - 3.6V	2.4			
t_{CL}	Clock Low Time	V_{CC} = 1.6 - 1.8V	4.5			ns
		V_{CC} = 2.7 - 3.6V	2.4			
t_{CR}	Rise Time (for maximum frequency)	V_{CC} = 1.6 - 1.8V			1.5	ns
		V_{CC} = 2.7 - 3.6V			1.0	
t_{CF}	Fall Time (for maximum frequency)	V_{CC} = 1.6 - 1.8V			1.5	ns
		V_{CC} = 2.7 - 3.6V			1.0	
Δt_{CK}	Change in period from one clock cycle to the next				10	%

Notes: 1. System Clock Prescalers must be set so that maximum CPU clock frequency for device is not exceeded.
2. The maximum frequency vs. supply voltage is linear between 1.6V and 2.7V, and the same applies for all other parameters with supply voltage conditions.

32.3.13.7 External 16MHz crystal oscillator and XOSC characteristics

Table 32-83. External 16MHz crystal oscillator and XOSC characteristics.

Symbol	Parameter	Condition		Min.	Typ.	Max.	Units
	Cycle to cycle jitter	XOSCPWR=0	FRQRANGE=0		0		ns
			FRQRANGE=0		0		
		XOSCPWR=1			0		
	Long term jitter	XOSCPWR=0	FRQRANGE=0		0		
			FRQRANGE=0		0		
		XOSCPWR=1			0		
	Frequency error	XOSCPWR=0	FRQRANGE=0		0.03		%
			FRQRANGE=0		0.03		
			FRQRANGE=0		0.03		
		XOSCPWR=1			0.003		
	Duty cycle	XOSCPWR=0	FRQRANGE=0		50		
			FRQRANGE=0		50		
			FRQRANGE=0		50		
		XOSCPWR=1			50		

Symbol	Parameter	Condition		Min.	Typ.	Max.	Units
	Negative impedance [1]	XOSCPWR=0, FRQRANGE=0	0.4MHz resonator, CL=100pF		44k		Ω
R_Q			1MHz resonator, CL=20pF		67k		
			2MHz resonator, CL=20pF		67k		
		XOSCPWR=0, FRQRANGE=1, CL=20pF	2MHz crystal		82k		
			8MHz crystal		1500		
			9MHz crystal		1500		
		XOSCPWR=0, FRQRANGE=2, CL=20pF	8MHz crystal		2700		
			9MHz crystal		2700		
			12MHz crystal		1000		
		XOSCPWR=0, FRQRANGE=3, CL=20pF	9MHz crystal		3600		
			12MHz crystal		1300		
			16MHz crystal		590		
		XOSCPWR=1, FRQRANGE=0, CL=20pF	9MHz crystal		390		
			12MHz crystal		50		
			16MHz crystal		10		
		XOSCPWR=1, FRQRANGE=1, CL=20pF	9MHz crystal		1500		
			12MHz crystal		650		
			16MHz crystal		270		
		XOSCPWR=1, FRQRANGE=2, CL=20pF	12MHz crystal		1000		
			16MHz crystal		440		
		XOSCPWR=1, FRQRANGE=3, CL=20pF	12MHz crystal		1300		
			16MHz crystal		590		
	ESR	SF = safety factor				$min(R_Q)/SF$	kΩ
	Start-up time	XOSCPWR=0, FRQRANGE=0	0.4MHz resonator, CL=100pF		1.0		ms
		XOSCPWR=0, FRQRANGE=1	2MHz crystal, CL=20pF		2.6		
		XOSCPWR=0, FRQRANGE=2	8MHz crystal, CL=20pF		0.8		
		XOSCPWR=0, FRQRANGE=3	12MHz crystal, CL=20pF		1.0		
		XOSCPWR=1, FRQRANGE=3	16MHz crystal, CL=20pF		1.4		

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
C_{XTAL1}	Parasitic capacitance XTAL1 pin			5.9		pF
C_{XTAL2}	Parasitic capacitance XTAL1 pin			8.3		
C_{LOAD}	Parasitic capacitance load			3.5		

Note: 1. Numbers for negative impedance are not tested in production but guaranteed from design and characterization.

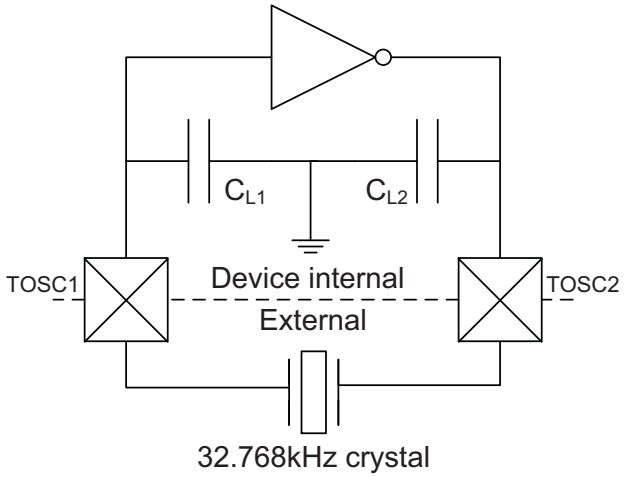
32.3.13.8 External 32.768kHz crystal oscillator and TOSC characteristics

Table 32-84. External 32.768kHz crystal oscillator and TOSC characteristics.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
ESR/R1	Recommended crystal equivalent series resistance (ESR)	Crystal load capacitance 6.5pF			60	kΩ
		Crystal load capacitance 9.0pF			35	
		Crystal load capacitance 12pF			28	
C_{TOSC1}	Parasitic capacitance TOSC1 pin			3.5		pF
C_{TOSC2}	Parasitic capacitance TOSC2 pin			3.5		
	Recommended safety factor	Capacitance load matched to crystal specification	3			

Note: See Figure 32-18 for definition.

Figure 32-18.TOSC input capacitance.



The parasitic capacitance between the TOSC pins is C_{L1} + C_{L2} in series as seen from the crystal when oscillating without external capacitors.

32.3.14 SPI characteristics

Figure 32-19.SPI timing requirements in master mode.

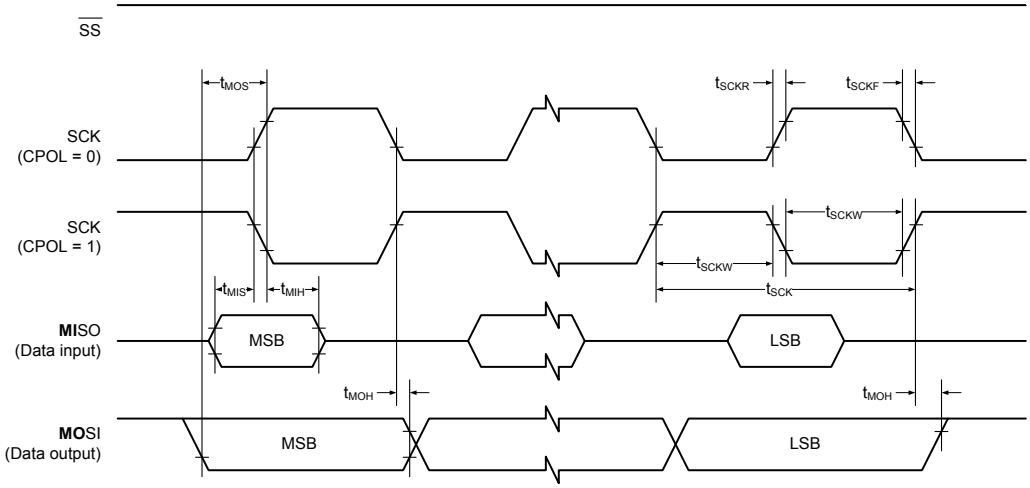


Figure 32-20.SPI timing requirements in slave mode.

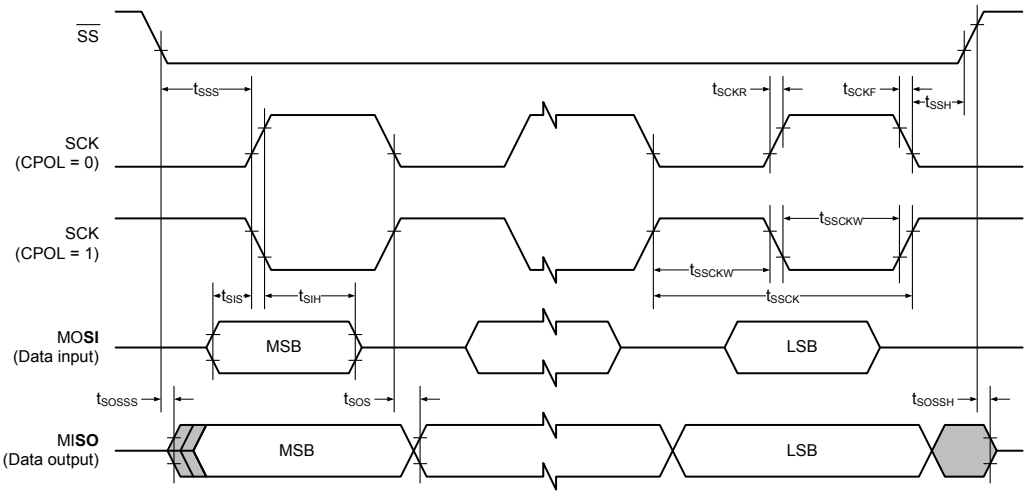


Table 32-85. SPI timing characteristics and requirements.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
t_{SCK}	SCK period	Master		(See Table 20-3 in XMEGA D manual)		ns
t_{SCKW}	SCK high/low width	Master		0.5 * SCK		
t_{SCKR}	SCK rise time	Master		2.7		
t_{SCKF}	SCK fall time	Master		2.7		
t_{MIS}	MISO setup to SCK	Master		10		
t_{MIH}	MISO hold after SCK	Master		10		
t_{MOS}	MOSI setup SCK	Master		0.5 * SCK		
t_{MOH}	MOSI hold after SCK	Master		1		
t_{SSCK}	Slave SCK Period	Slave	4 * t Clk_{PER}			
t_{SSCKW}	SCK high/low width	Slave	2 * t Clk_{PER}			
t_{SSCKR}	SCK rise time	Slave			1600	
t_{SSCKF}	SCK fall time	Slave			1600	
t_{SIS}	MOSI setup to SCK	Slave	3			
t_{SIH}	MOSI hold after SCK	Slave	t Clk_{PER}			
t_{SSS}	$\overline{SS}$ setup to SCK	Slave	21			
t_{SSH}	$\overline{SS}$ hold after SCK	Slave	20			
t_{SOS}	MISO setup SCK	Slave		8		
t_{SOH}	MISO hold after SCK	Slave		13		
t_{SOSS}	MISO setup after $\overline{SS}$ low	Slave		11		
t_{SOSH}	MISO hold after $\overline{SS}$ high	Slave		8		

32.3.15 Two-wire interface characteristics

Table 32-86 on page 117 describes the requirements for devices connected to the Two-Wire Interface Bus. The Atmel AVR XMEGA Two-Wire Interface meets or exceeds these requirements under the noted conditions. Timing symbols refer to Figure 32-21.

Figure 32-21.Two-wire interface bus timing.

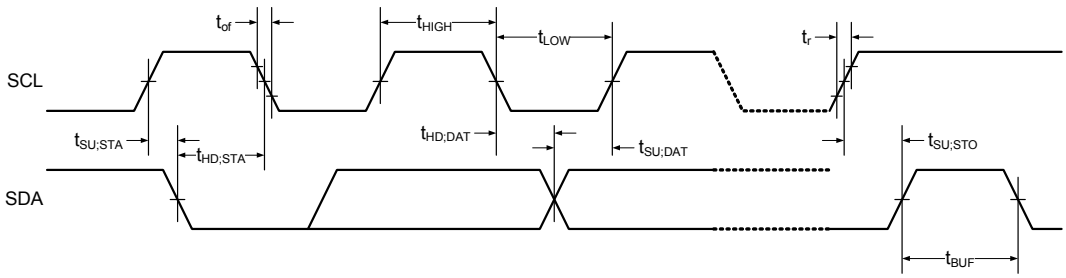


Table 32-86. Two-wire interface characteristics.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
V_{IH}	Input high voltage		$0.7V_{CC}$		V_{CC} + 0.5	V
V_{IL}	Input low voltage		-0.5		$0.3V_{CC}$	
V_{hys}	Hysteresis of Schmitt trigger inputs		$0.05V_{CC}$ (1)			
V_{OL}	Output low voltage	3mA, sink current	0		0.4	
t_r	Rise time for both SDA and SCL		$20 + 0.1C_b$ (1)(2)		300	ns
t_{of}	Output fall time from V_{IHmin} to V_{ILmax}	$10pF < C_b < 400pF$ (2)	$20 + 0.1C_b$ (1)(2)		250	
t_{SP}	Spikes suppressed by input filter		0		50	
I_I	Input current for each I/O pin	$0.1V_{CC} < V_I < 0.9V_{CC}$	-10		10	µA
C_I	Capacitance for each I/O pin				10	pF
f_{SCL}	SCL clock frequency	f_{PER} (3) > max($10f_{SCL}$, 250kHz)	0		400	kHz
R_P	Value of pull-up resistor	$f_{SCL} \leq 100kHz$	$\frac{V_{CC} - 0.4V}{3mA}$		$\frac{100ns}{C_b}$	Ω
		$f_{SCL} > 100kHz$			$\frac{300ns}{C_b}$	
$t_{HD;STA}$	Hold time (repeated) START condition	$f_{SCL} \leq 100kHz$	4.0			µs
		$f_{SCL} > 100kHz$	0.6			
t_{LOW}	Low period of SCL clock	$f_{SCL} \leq 100kHz$	4.7			
		$f_{SCL} > 100kHz$	1.3			
t_{HIGH}	High period of SCL clock	$f_{SCL} \leq 100kHz$	4.0			
		$f_{SCL} > 100kHz$	0.6			
$t_{SU;STA}$	Set-up time for a repeated START condition	$f_{SCL} \leq 100kHz$	4.7			
		$f_{SCL} > 100kHz$	0.6			
$t_{HD;DAT}$	Data hold time	$f_{SCL} \leq 100kHz$	0		3.45	µs
		$f_{SCL} > 100kHz$	0		0.9	
$t_{SU;DAT}$	Data setup time	$f_{SCL} \leq 100kHz$	250			
		$f_{SCL} > 100kHz$	100			
$t_{SU;STO}$	Setup time for STOP condition	$f_{SCL} \leq 100kHz$	4.0			
		$f_{SCL} > 100kHz$	0.6			
t_{BUF}	Bus free time between a STOP and START condition	$f_{SCL} \leq 100kHz$	4.7			
		$f_{SCL} > 100kHz$	1.3			

Notes:
1. Required only for $f_{SCL} > 100kHz$.
2. C_b = Capacitance of one bus line in pF.
3. f_{PER} = Peripheral clock frequency.

32.4 Atmel ATxmega192D3

32.4.1 Absolute maximum ratings

Stresses beyond those listed in Table 32-87 under may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Table 32-87. Absolute maximum ratings.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
V_{CC}	Power supply voltage		-0.3		4	V
I_{VCC}	Current into a V_{CC} pin				200	mA
I_{GND}	Current out of a Gnd pin				200	
V_{PIN}	Pin voltage with respect to Gnd and V_{CC}		-0.5		V_{CC} + 0.5	V
I_{PIN}	I/O pin sink/source current		-25		25	mA
T_A	Storage temperature		-65		150	°C
T_j	Junction temperature				150	

32.4.2 General operating ratings

The device must operate within the ratings listed in Table 32-88 in order for all other electrical characteristics and typical characteristics of the device to be valid.

Table 32-88. General operating conditions.

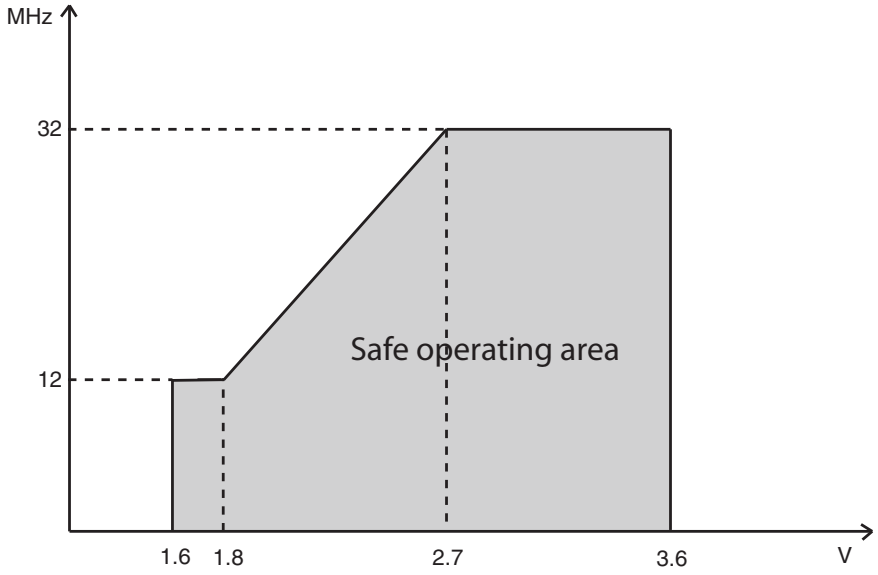
Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
V_{CC}	Power supply voltage		1.60		3.6	V
AV_{CC}	Analog supply voltage		1.60		3.6	
T_A	Temperature range		-40		85	°C
T_j	Junction temperature		-40		105	

Table 32-89. Operating voltage and frequency.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
Clk_{CPU}	CPU clock frequency	V_{CC} = 1.6V	0		12	MHz
		V_{CC} = 1.8V	0		12	
		V_{CC} = 2.7V	0		32	
		V_{CC} = 3.6V	0		32	

The maximum CPU clock frequency depends on V_{CC}. As shown in Figure 32-22 on page 119 the frequency vs. V_{CC} curve is linear between 1.8V < V_{CC} < 2.7V.

Figure 32-22.Maximum frequency vs. V_{CC}.



32.4.3 Current consumption

Table 32-90. Current consumption for Active mode and sleep modes.

Symbol	Parameter	Condition		Min.	Typ.	Max.	Units
I_{CC}	Active power consumption (1)	32kHz, Ext. Clk	V_{CC} = 1.8V		60		µA
			V_{CC} = 3.0V		140		
		1MHz, Ext. Clk	V_{CC} = 1.8V		245		
			V_{CC} = 3.0V		550		
		2MHz, Ext. Clk	V_{CC} = 1.8V		440	700	
			V_{CC} = 3.0V		0.9	1.5	mA
		32MHz, Ext. Clk			9.0	15	
	Idle power consumption (2)	32kHz, Ext. Clk	V_{CC} = 1.8V		3.0		µA
			V_{CC} = 3.0V		3.5		
		1MHz, Ext. Clk	V_{CC} = 1.8V		55		
			V_{CC} = 3.0V		110		
		2MHz, Ext. Clk	V_{CC} = 1.8V		105	350	
			V_{CC} = 3.0V		215	650	
		32MHz, Ext. Clk			3.4	8.0	mA
	Power-down power consumption	T = 25°C	V_{CC} = 3.0V		0.1	1.0	µA
		T = 85°C			3.5	6.0	
		WDT and sampled BOD enabled, T = 25°C	V_{CC} = 3.0V		1.5	2.0	
		WDT and sampled BOD enabled, T = 85°C			5.8	10	
	Power-save power consumption (3)	RTC from ULP clock, WDT and sampled BOD enabled, T = 25°C	V_{CC} = 1.8V		1.3		
			V_{CC} = 3.0V		1.4		
		RTC from 1.024kHz low power 32.768kHz TOSC, T = 25°C	V_{CC} = 1.8V		0.7	2.0	
			V_{CC} = 3.0V		0.8	2.0	
		RTC from low power 32.768kHz TOSC, T = 25°C	V_{CC} = 1.8V		0.9	3.0	
			V_{CC} = 3.0V		1.1	3.0	
	Reset power consumption	Current through $\overline{\text{RESET}}$ pin substracted	V_{CC} = 3.0V		170		

Notes:
1. All power reduction registers set including FPRM and EPRM.
2. All power reduction registers set without FPRM and EPRM.
3. Maximum limits are based on characterization, and not tested in production.

Table 32-91. Current consumption for modules and peripherals.

Symbol	Parameter	Condition [1]		Min.	Typ.	Max.	Units
I_{CC}	ULP oscillator				0.9		µA
	32.768kHz int. oscillator				25		
	2MHz int. oscillator				78		
		DFLL enabled with 32.768kHz int. osc. as reference			110		
	32MHz int. oscillator				250		
		DFLL enabled with 32.768kHz int. osc. as reference			440		
	PLL	20× multiplication factor, 32MHz int. osc. DIV4 as reference			310		
	Watchdog timer				1.0		
	BOD	Continuous mode			132		
		Sampled mode, includes ULP oscillator			1.4		
	Internal 1.0V reference				185		
	Temperature sensor				182		
	ADC	16ksps V_{REF} = Ext. ref.			1.12		mA
			CURRLIMIT = LOW		1.01		
			CURRLIMIT = MEDIUM		0.9		
			CURRLIMIT = HIGH		0.8		
		75ksps V_{REF} = Ext. ref.	CURRLIMIT = LOW		1.7		
		300ksps, V_{REF} = Ext. ref.			3.1		
	USART	Rx and Tx enabled, 9600 BAUD			9.5		µA
	Flash memory and EEPROM programming				10		mA

Note: 1. All parameters measured as the difference in current consumption between module enabled and disabled. All data at V_{CC} = 3.0V, Clk_{SYS} = 1MHz external clock without prescaling, T = 25°C unless other conditions are given.

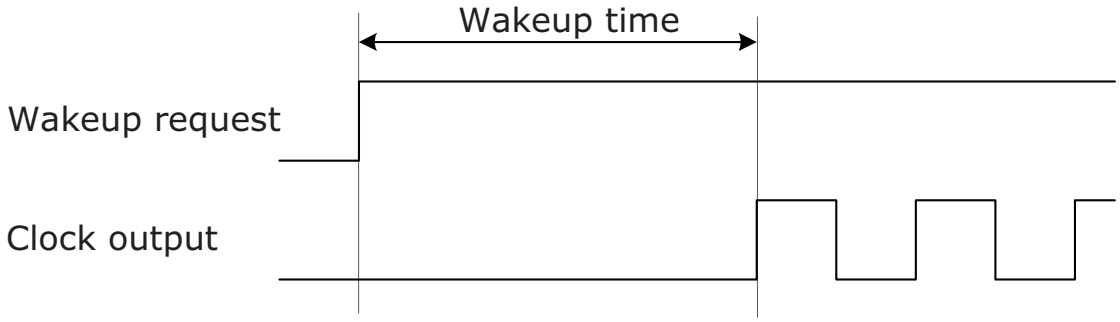
32.4.4 Wake-up time from sleep modes

Table 32-92. Device wake-up time from sleep modes with various system clock sources.

Symbol	Parameter	Condition	Min.	Typ. (1)	Max.	Units
t_{wakeup}	Wake-up time from idle, standby, and extended standby mode	External 2MHz clock		2.0		µs
		32.768kHz internal oscillator		125		
		2MHz internal oscillator		2.0		
		32MHz internal oscillator		0.2		
	Wake-up time from power-save and power-down mode	External 2MHz clock		4.6		
		32.768kHz internal oscillator		330		
		2MHz internal oscillator		9.5		
		32MHz internal oscillator		5.6		

Note: 1. The wake-up time is the time from the wake-up request is given until the peripheral clock is available on pin, see Figure 32-23. All peripherals and modules start execution from the first clock cycle, expect the CPU that is halted for four clock cycles before program execution starts.

Figure 32-23.Wake-up time definition.



32.4.5 I/O pin characteristics

The I/O pins complies with the JEDEC LVTTL and LVCMOS specification and the high- and low level input and output voltage limits reflect or exceed this specification.

Table 32-93. I/O pin characteristics.

Symbol	Parameter	Condition		Min.	Typ.	Max.	Units
I_{OH} (1)/ I_{OL} (2)	I/O pin source/sink current			-15		15	mA
V_{IH}	High level input voltage	V_{CC} = 2.4 - 3.6V		0.7 * V_{CC}		V_{CC} + 0.5	V
		V_{CC} = 1.6 - 2.4V		0.8 * V_{CC}		V_{CC} + 0.5	
V_{IL}	Low level input voltage	V_{CC} = 2.4 - 3.6V		-0.5		0.3 * V_{CC}	
		V_{CC} = 1.6 - 2.4V		-0.5		0.2 * V_{CC}	
V_{OH}	High level output voltage	V_{CC} = 3.3V	I_{OH} = -4mA	2.6	2.9		
		V_{CC} = 3.0V	I_{OH} = -3mA	2.1	2.6		
		V_{CC} = 1.8V	I_{OH} = -1mA	1.4	1.6		
V_{OL}	Low level output voltage	V_{CC} = 3.3V	I_{OL} = 8mA		0.4	0.76	
		V_{CC} = 3.0V	I_{OL} = 5mA		0.3	0.64	
		V_{CC} = 1.8V	I_{OL} = 3mA		0.2	0.46	
I_{IN}	Input leakage current I/O pin	T = 25°C			<0.01	1.0	µA
R_P	Pull/buss keeper resistor				25		kΩ

Notes:
1. The sum of all I_{OH} for PORTA and PORTB must not exceed 100mA.
   The sum of all I_{OH} for PORTC, PORTD, PORTE must for each port not exceed 200mA.
   The sum of all I_{OH} for pins PF[0-5] on PORTF must not exceed 200mA.
   The sum of all I_{OL} for pins PF[6-7] on PORTF, PORTR and PDI must not exceed 100mA.
2. The sum of all I_{OL} for PORTA and PORTB must not exceed 100mA.
   The sum of all I_{OL} for PORTC, PORTD, PORTE must for each port not exceed 200mA.
   The sum of all I_{OL} for pins PF[0-5] on PORTF must not exceed 200mA.
   The sum of all I_{OL} for pins PF[6-7] on PORTF, PORTR and PDI must not exceed 100mA.

32.4.6 ADC characteristics

Table 32-94. Power supply, reference and input range.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
AV_{CC}	Analog supply voltage		V_{CC} - 0.3		V_{CC} + 0.3	V
V_{REF}	Reference voltage		1		AV_{CC} - 0.6	
R_{in}	Input resistance	Switched			4.5	kΩ
C_{in}	Input capacitance	Switched			5	pF
R_{AREF}	Reference input resistance	(leakage only)		>10		MΩ
C_{AREF}	Reference input capacitance	Static load		7		pF
V_{in}	Input range		0		V_{REF}	V
	Conversion range	Differential mode, Vinp - Vinn	$-V_{REF}$		V_{REF}	
	Conversion range	Single ended unsigned mode, Vinp	-ΔV		V_{REF} - ΔV	
ΔV	Fixed offset voltage			200		lsb

Table 32-95. Clock and timing.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
Clk_{ADC}	ADC clock frequency	Maximum is 1/4 of peripheral clock frequency	100		1800	kHz
		Measuring internal signals	100		125	
f_{ClkADC}	Sample rate		16		300	ksps
f_{ADC}	Sample rate	Current limitation (CURRLIMIT) off	16		300	
		CURRLIMIT = LOW	16		250	
		CURRLIMIT = MEDIUM	16		150	
		CURRLIMIT = HIGH	16		50	
	Sampling time	Configurable in steps of 1/2 Clk_{ADC} cycles up to 32 Clk_{ADC} cycles	0.28		320	µs
	Conversion time (latency)	(RES+2)/2 + 1 + GAIN RES (Resolution) = 8 or 12, GAIN = 0 to 3	5.5		10	Clk_{ADC} cycles
	Start-up time	ADC clock cycles		12	24	
	ADC settling time	After changing reference or input mode		7	7	

Table 32-96. Accuracy characteristics.

Symbol	Parameter	Condition [2]		Min.	Typ.	Max.	Units
RES	Resolution	12-bit resolution	Differential	8	12	12	Bits
			Single ended signed	7	11	11	
			Single ended unsigned	8	12	12	
INL [1]	Integral non-linearity	Differential mode	16ksps, V_{REF} = 3V		0.5	1	lsb
			16ksps, all V_{REF}		0.8	2	
			300ksps, V_{REF} = 3V		0.6	1	
			300ksps, all V_{REF}		1	2	
		Single ended unsigned mode	16ksps, V_{REF} = 3.0V		0.5	1	
			16ksps, all V_{REF}		1.3	2	
DNL [1]	Differential non-linearity	Differential mode	16ksps, V_{REF} = 3V		0.3	1	
			16ksps, all V_{REF}		0.5	1	
			300ksps, V_{REF} = 3V		0.3	1	
			300ksps, all V_{REF}		0.5	1	
		Single ended unsigned mode	16ksps, V_{REF} = 3.0V		0.6	1	
			16ksps, All V_{REF}		0.6	1	
	Offset error	Differential mode	300ksps, V_{REF} = 3V		-7		mV
			Temperature drift, V_{REF} = 3V		0.01		mV/K
			Operating voltage drift		0.16		mV/V
	Gain error	Differential mode	External reference		-5		mV
			AV_{CC}/1.6		-5		
			AV_{CC}/2.0		-6		
			Bandgap		±10		
			Temperature drift		0.02		mV/K
			Operating voltage drift		2		mV/V
	Gain error	Single ended unsigned mode	External reference		-8		mV
			AV_{CC}/1.6		-8		
			AV_{CC}/2.0		-8		
			Bandgap		±10		
			Temperature drift		0.03		mV/K
			Operating voltage drift		2		mV/V

Notes:
1. Maximum numbers are based on characterisation and not tested in production, and valid for 5% to 95% input voltage range.
2. Unless otherwise noted all linearity, offset, and gain error numbers are valid under the condition that external VREF is used.

Table 32-97. Gain stage characteristics.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
R_{in}	Input resistance	Switched in normal mode		4.0		kΩ
C_{sample}	Input capacitance	Switched in normal mode		4.4		pF
	Signal range	Gain stage output	0		AV_{CC} - 0.6	V
	Propagation delay	ADC conversion rate	1/2	1	3	Clk_{ADC} cycles
	Clock frequency	Same as ADC	100		1800	kHz
	Gain error	0.5× gain, normal mode		-1		%
		1× gain, normal mode		-1		
		8× gain, normal mode		-1		
		64× gain, normal mode		5		
	Offset error, input referred	0.5× gain, normal mode		10		mV
		1× gain, normal mode		5		
		8× gain, normal mode		-20		
		64× gain, normal mode		-126		

32.4.7 Analog comparator characteristics

Table 32-98. Analog comparator characteristics.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
V_{off}	Input offset voltage			10		mV
I_{lk}	Input leakage current			<10	50	nA
	Input voltage range		-0.1		AV_{CC}	V
	AC startup time			50		µs
V_{hys1}	Hysteresis, none	V_{CC} = 1.6V - 3.6V		0		mV
V_{hys2}	Hysteresis, small	V_{CC} = 1.6V - 3.6V		15		
V_{hys3}	Hysteresis, large	V_{CC} = 1.6V - 3.6V		30		
t_{delay}	Propagation delay	V_{CC} = 3.0V, T = 85°C		20	40	ns
		V_{CC} = 3.0V		17		
	64-level voltage scaler	Integral non-linearity (INL)		0.3	0.5	lsb
	Current source accuracy after calibration			5		%
	Current source calibration range	Single mode	4		6	µA

32.4.8 Bandgap and internal 1.0V reference characteristics

Table 32-99. Bandgap and internal 1.0V reference characteristics.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
	Startup time	As reference for ADC		1 Clk_{PER} + 2.5µs		µs
		As input voltage to ADC and AC		1.5		
	Bandgap voltage			1.1		V
INT1V	Internal 1.00V reference	T = 85°C, after calibration	0.99	1.0	1.01	
	Variation over voltage and temperature	Calibrated at T = 85°C		1		%

32.4.9 Brownout detection characteristics

Table 32-100.Brownout detection characteristics (1).

Symbol	Parameter (BOD level 0 at 85°C)	Condition	Min.	Typ.	Max.	Units
V_{BOT}	BOD level 0 falling V_{CC}		1.40	1.60	1.70	V
	BOD level 1 falling V_{CC}			1.8		
	BOD level 2 falling V_{CC}			2.0		
	BOD level 3 falling V_{CC}			2.2		
	BOD level 4 falling V_{CC}			2.4		
	BOD level 5 falling V_{CC}			2.6		
	BOD level 6 falling V_{CC}			2.8		
	BOD level 7 falling V_{CC}			3.0		
t_{BOD}	Detection time	Continuous mode		0.4		µs
		Sampled mode		1000		
V_{HYST}	Hysteresis			1.0		%

Note: 1. BOD is calibrated at 85°C within BOD level 0 values, and BOD level 0 is the default level.

32.4.10 External reset characteristics

Table 32-101.External reset characteristics.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
t_{EXT}	Minimum reset pulse width		1000	90		ns
V_{RST}	Reset threshold voltage	V_{CC} = 2.7 - 3.6V		0.45 * V_{CC}		V
		V_{CC} = 1.6 - 2.7V		0.45 * V_{CC}		
R_{RST}	Reset pin pull-up resistor			25		kΩ

32.4.11 Power-on reset characteristics

Table 32-102.Power-on reset characteristics.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
V_{POT-} (1)	POR threshold voltage falling V_{CC}	V_{CC} falls faster than 1V/ms	0.4	1.0		V
		V_{CC} falls at 1V/ms or slower	0.8	1.3		
V_{POT+}	POR threshold voltage rising V_{CC}			1.3	1.59	

Note: 1. V_{POT-} values are only valid when BOD is disabled. When BOD is enabled $V_{POT-} = V_{POT+}$.

32.4.12 Flash and EEPROM memory characteristics

Table 32-103.Endurance and data retention.

Symbol	Parameter	Condition		Min.	Typ.	Max.	Units
	Flash	Write/erase cycles	25°C	10K			Cycle
			85°C	10K			
		Data retention	25°C	100			Year
			55°C	25			
	EEPROM	Write/erase cycles	25°C	100K			Cycle
			85°C	100K			
		Data retention	25°C	100			Year
			55°C	25			

Table 32-104. Programming time.

Symbol	Parameter	Condition	Min.	Typ. (1)	Max.	Units
	Chip erase (2)	192KB flash, EEPROM		90		ms
	Application erase	Section erase		6		
	Flash	Page erase		4		
		Page write		4		
		Atomic page erase and write		8		
	EEPROM	Page erase		4		
		Page write		4		
		Atomic page erase and write		8		

Notes: 1. Programming is timed from the 2MHz internal oscillator.
2. EEPROM is not erased if the EESAVE fuse is programmed.

32.4.13 Clock and oscillator characteristics

32.4.13.1 Calibrated 32.768kHz internal oscillator characteristics

Table 32-105. 32.768kHz internal oscillator characteristics.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
	Frequency			32.768		kHz
	Factory calibration accuracy	T = 85°C, V_{CC} = 3.0V	-0.5		0.5	%
	User calibration accuracy		-0.5		0.5	

32.4.13.2 Calibrated 2MHz RC internal oscillator characteristics

Table 32-106. 2MHz internal oscillator characteristics.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
	Frequency range	DFLL can tune to this frequency over voltage and temperature	1.8	2.0	2.2	MHz
	Factory calibrated frequency			2.0		
	Factory calibration accuracy	T = 85°C, V_{CC} = 3.0V	-1.5		1.5	%
	User calibration accuracy		-0.2		0.2	
	DFLL calibration stepsize			0.18		

32.4.13.3 Calibrated 32MHz internal oscillator characteristics

Table 32-107. 32MHz internal oscillator characteristics.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
	Frequency range	DFLL can tune to this frequency over voltage and temperature	30	32	55	MHz
	Factory calibrated frequency			32		
	Factory calibration accuracy	T = 85°C, V_{CC} = 3.0V	-1.5		1.5	%
	User calibration accuracy		-0.2		0.2	
	DFLL calibration step size			0.19		

32.4.13.4 32kHz internal ULP oscillator characteristics

Table 32-108. 32kHz internal ULP oscillator characteristics.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
	Factory calibrated frequency			32		kHz
	Factory calibration accuracy	T = 85°C, V_{CC} = 3.0V	-12		12	%
	Accuracy		-30		30	

32.4.13.5 Internal Phase Locked Loop (PLL) characteristics

Table 32-109. Internal PLL characteristics.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
f_{IN}	Input frequency	Output frequency must be within f_{OUT}	0.4		64	MHz
f_{OUT}	Output frequency (1)	V_{CC} = 1.6 - 1.8V	20		48	
		V_{CC} = 2.7 - 3.6V	20		128	
	Start-up time			25		µs
	Re-lock time			25		

Note: 1. The maximum output frequency vs. supply voltage is linear between 1.8V and 2.7V, and can never be higher than four times the maximum CPU frequency.

32.4.13.6 External clock characteristics

Figure 32-24. External clock drive waveform.

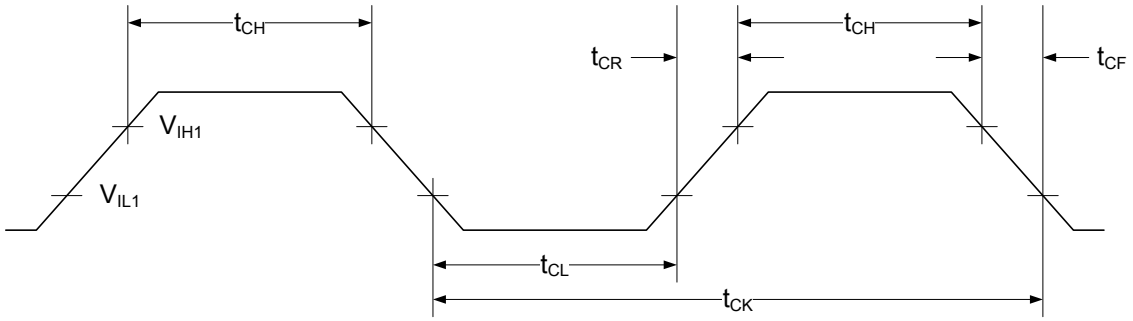


Table 32-110.External clock used as system clock without prescaling.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
$1/t_{CK}$	Clock Frequency (1)	V_{CC} = 1.6 - 1.8V	0		12	MHz
		V_{CC} = 2.7 - 3.6V	0		32	
t_{CK}	Clock Period	V_{CC} = 1.6 - 1.8V	83.3			ns
		V_{CC} = 2.7 - 3.6V	31.5			
t_{CH}	Clock High Time	V_{CC} = 1.6 - 1.8V	30.0			ns
		V_{CC} = 2.7 - 3.6V	12.5			
t_{CL}	Clock Low Time	V_{CC} = 1.6 - 1.8V	30.0			ns
		V_{CC} = 2.7 - 3.6V	12.5			
t_{CR}	Rise Time (for maximum frequency)	V_{CC} = 1.6 - 1.8V			10	ns
		V_{CC} = 2.7 - 3.6V			3	
t_{CF}	Fall Time (for maximum frequency)	V_{CC} = 1.6 - 1.8V			10	ns
		V_{CC} = 2.7 - 3.6V			3	
Δt_{CK}	Change in period from one clock cycle to the next				10	%

Note: 1. The maximum frequency vs. supply voltage is linear between 1.6V and 2.7V, and the same applies for all other parameters with supply voltage conditions.

Table 32-111.External clock with prescaler [1] for system clock.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
$1/t_{CK}$	Clock Frequency [2]	V_{CC} = 1.6 - 1.8V	0		90	MHz
		V_{CC} = 2.7 - 3.6V	0		142	
t_{CK}	Clock Period	V_{CC} = 1.6 - 1.8V	11			ns
		V_{CC} = 2.7 - 3.6V	7			
t_{CH}	Clock High Time	V_{CC} = 1.6 - 1.8V	4.5			ns
		V_{CC} = 2.7 - 3.6V	2.4			
t_{CL}	Clock Low Time	V_{CC} = 1.6 - 1.8V	4.5			ns
		V_{CC} = 2.7 - 3.6V	2.4			
t_{CR}	Rise Time (for maximum frequency)	V_{CC} = 1.6 - 1.8V			1.5	ns
		V_{CC} = 2.7 - 3.6V			1.0	
t_{CF}	Fall Time (for maximum frequency)	V_{CC} = 1.6 - 1.8V			1.5	ns
		V_{CC} = 2.7 - 3.6V			1.0	
Δt_{CK}	Change in period from one clock cycle to the next				10	%

Notes: 1. System Clock Prescalers must be set so that maximum CPU clock frequency for device is not exceeded.
2. The maximum frequency vs. supply voltage is linear between 1.6V and 2.7V, and the same applies for all other parameters with supply voltage conditions.

32.4.13.7 External 16MHz crystal oscillator and XOSC characteristics

Table 32-112. External 16MHz crystal oscillator and XOSC characteristics.

Symbol	Parameter	Condition		Min.	Typ.	Max.	Units
	Cycle to cycle jitter	XOSCPWR=0	FRQRANGE=0		0		ns
			FRQRANGE=1, 2, or 3		0		
		XOSCPWR=1			0		
	Long term jitter	XOSCPWR=0	FRQRANGE=0		0		
			FRQRANGE=1, 2, or 3		0		
		XOSCPWR=1			0		
	Frequency error	XOSCPWR=0	FRQRANGE=0		0.03		%
			FRQRANGE=1		0.03		
			FRQRANGE=2 or 3		0.03		
		XOSCPWR=1			0.003		
	Duty cycle	XOSCPWR=0	FRQRANGE=0		50		
			FRQRANGE=1		50		
			FRQRANGE=2 or 3		50		
		XOSCPWR=1			50		

Symbol	Parameter	Condition		Min.	Typ.	Max.	Units
R_Q	Negative impedance [1]	XOSCPWR=0, FRQRANGE=0	0.4MHz resonator, CL=100pF		44k		Ω
			1MHz crystal, CL=20pF		67k		
			2MHz crystal, CL=20pF		67k		
		XOSCPWR=0, FRQRANGE=1, CL=20pF	2MHz crystal		82k		
			8MHz crystal		1500		
			9MHz crystal		1500		
		XOSCPWR=0, FRQRANGE=2, CL=20pF	8MHz crystal		2700		
			9MHz crystal		2700		
			12MHz crystal		1000		
		XOSCPWR=0, FRQRANGE=3, CL=20pF	9MHz crystal		3600		
			12MHz crystal		1300		
			16MHz crystal		590		
		XOSCPWR=1, FRQRANGE=0, CL=20pF	9MHz crystal		390		
			12MHz crystal		50		
			16MHz crystal		10		
		XOSCPWR=1, FRQRANGE=1, CL=20pF	9MHz crystal		1500		
			12MHz crystal		650		
			16MHz crystal		270		
		XOSCPWR=1, FRQRANGE=2, CL=20pF	12MHz crystal		1000		
			16MHz crystal		440		
		XOSCPWR=1, FRQRANGE=3, CL=20pF	12MHz crystal		1300		
			16MHz crystal		590		ms
	Start-up time	XOSCPWR=0, FRQRANGE=0	0.4MHz resonator, CL=100pF		1.0		
		XOSCPWR=0, FRQRANGE=1	2MHz resonator, CL=20pF		2.6		
		XOSCPWR=0, FRQRANGE=2	8MHz resonator, CL=20pF		0.8		
		XOSCPWR=0, FRQRANGE=3	12MHz resonator, CL=20pF		1.0		
		XOSCPWR=1, FRQRANGE=3	16MHz resonator, CL=20pF		1.4		
C_{XTAL1}	Parasitic capacitance XTAL1 pin				5.9		pF
C_{XTAL2}	Parasitic capacitance XTAL2 pin				8.3		
C_{LOAD}	Paracitic capacitance load				3.5		

Notes: 1. Numbers for negative impedance are not tested in production but guaranteed from design and characterization.

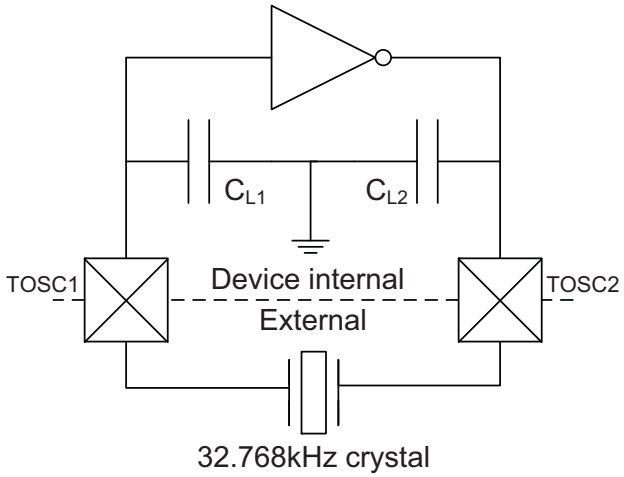
32.4.13.8 External 32.768kHz crystal oscillator and TOSC characteristics

Table 32-113. External 32.768kHz crystal oscillator and TOSC characteristics.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
ESR/R1	Recommended crystal equivalent series resistance (ESR)	Crystal load capacitance 6.5pF			60	kΩ
		Crystal load capacitance 9.0pF			35	
		Crystal load capacitance 12pF			28	
C_{TOSC1}	Parasitic capacitance TOSC1 pin			3.5		pF
C_{TOSC2}	Parasitic capacitance TOSC2 pin			3.5		
	Recommended safety factor	Capacitance load matched to crystal specification	3			

Note: See Figure 32-25 for definition.

Figure 32-25. TOSC input capacitance.



The parasitic capacitance between the TOSC pins is C_{L1} + C_{L2} in series as seen from the crystal when oscillating without external capacitors.

32.4.14 SPI characteristics

Figure 32-26. SPI timing requirements in master mode.

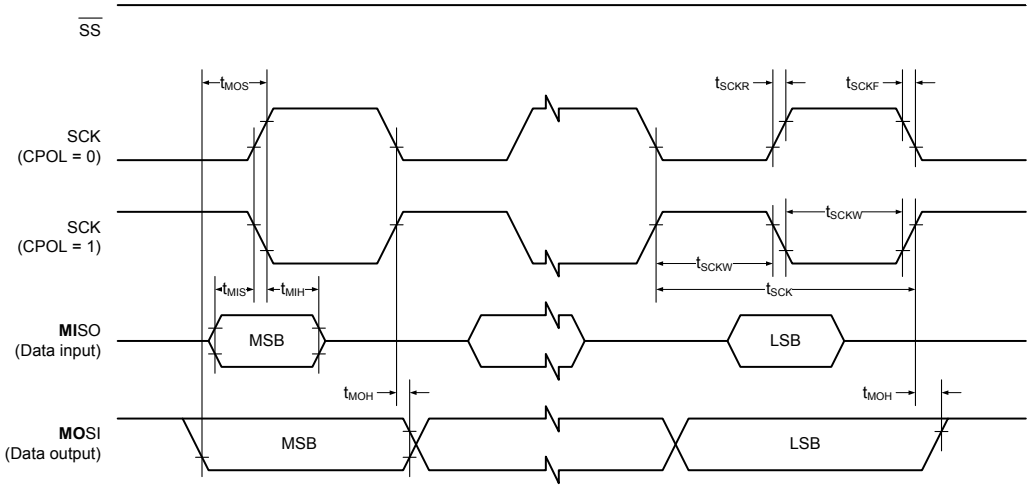


Figure 32-27. SPI timing requirements in slave mode.

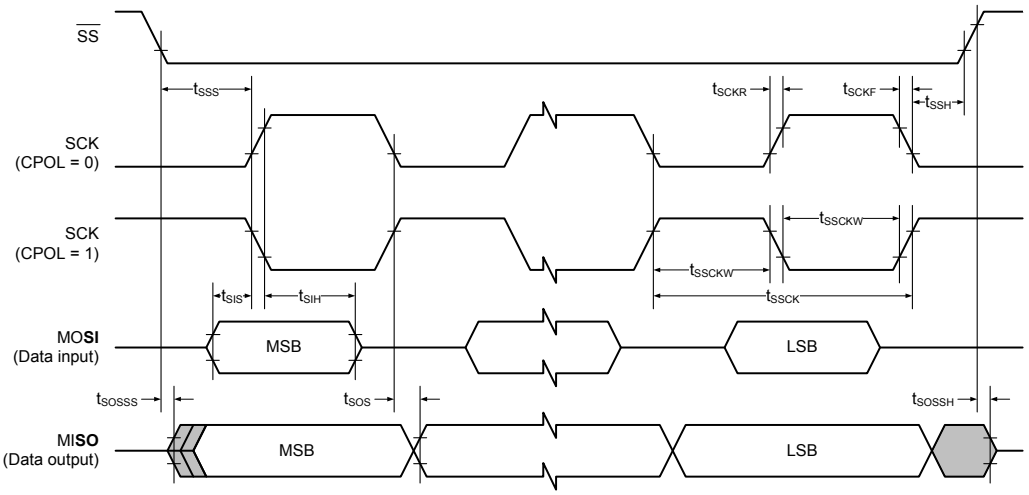


Table 32-114. SPI timing characteristics and requirements.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
t_{SCK}	SCK period	Master		(See Table 20-3 in XMEGA D manual)		ns
t_{SCKW}	SCK high/low width	Master		0.5 * SCK		
t_{SCKR}	SCK rise time	Master		2.7		
t_{SCKF}	SCK fall time	Master		2.7		
t_{MIS}	MISO setup to SCK	Master		10		
t_{MIH}	MISO hold after SCK	Master		10		
t_{MOS}	MOSI setup SCK	Master		0.5 * SCK		
t_{MOH}	MOSI hold after SCK	Master		1		
t_{SSCK}	Slave SCK Period	Slave	4 * t Clk_{PER}			
t_{SSCKW}	SCK high/low width	Slave	2 * t Clk_{PER}			
t_{SSCKR}	SCK rise time	Slave			1600	
t_{SSCKF}	SCK fall time	Slave			1600	
t_{SIS}	MOSI setup to SCK	Slave	3			
t_{SIH}	MOSI hold after SCK	Slave	t Clk_{PER}			
t_{SSS}	$\overline{SS}$ setup to SCK	Slave	21			
t_{SSH}	$\overline{SS}$ hold after SCK	Slave	20			
t_{SOS}	MISO setup SCK	Slave		8		
t_{SOH}	MISO hold after SCK	Slave		13		
t_{SOSS}	MISO setup after $\overline{SS}$ low	Slave		11		
t_{SOSH}	MISO hold after $\overline{SS}$ high	Slave		8		

32.4.15 Two-wire interface characteristics

Table 32-115 on page 136 describes the requirements for devices connected to the Two-Wire Interface Bus. The Atmel AVR XMEGA Two-Wire Interface meets or exceeds these requirements under the noted conditions. Timing symbols refer to Figure 32-28.

Figure 32-28. Two-wire interface bus timing.

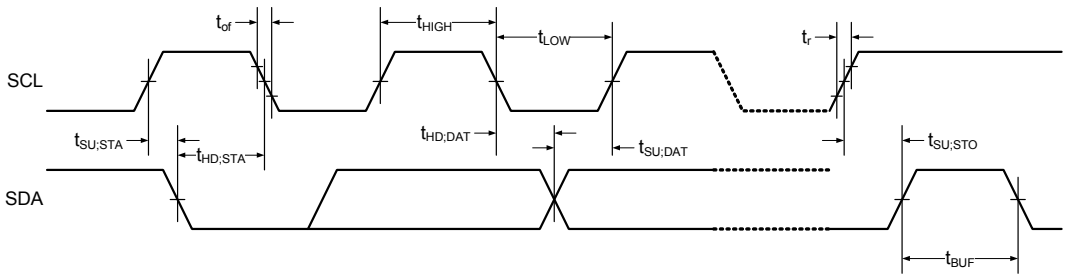


Table 32-115. Two-wire interface characteristics.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
V_{IH}	Input high voltage		$0.7V_{CC}$		V_{CC} + 0.5	V
V_{IL}	Input low voltage		-0.5		$0.3V_{CC}$	
V_{hys}	Hysteresis of Schmitt trigger inputs		$0.05V_{CC}$ (1)			
V_{OL}	Output low voltage	3mA, sink current	0		0.4	
t_r	Rise time for both SDA and SCL		$20 + 0.1C_b$ (1)(2)		300	ns
t_{of}	Output fall time from V_{IHmin} to V_{ILmax}	$10pF < C_b < 400pF$ (2)	$20 + 0.1C_b$ (1)(2)		250	
t_{SP}	Spikes suppressed by input filter		0		50	
I_I	Input current for each I/O pin	$0.1V_{CC} < V_I < 0.9V_{CC}$	-10		10	µA
C_I	Capacitance for each I/O pin				10	pF
f_{SCL}	SCL clock frequency	f_{PER} (3) > max($10f_{SCL}$, 250kHz)	0		400	kHz
R_P	Value of pull-up resistor	$f_{SCL} \leq 100kHz$	$\frac{V_{CC} - 0.4V}{3mA}$		$\frac{100ns}{C_b}$	Ω
		$f_{SCL} > 100kHz$			$\frac{300ns}{C_b}$	
$t_{HD;STA}$	Hold time (repeated) START condition	$f_{SCL} \leq 100kHz$	4.0			µs
		$f_{SCL} > 100kHz$	0.6			
t_{LOW}	Low period of SCL clock	$f_{SCL} \leq 100kHz$	4.7			
		$f_{SCL} > 100kHz$	1.3			
t_{HIGH}	High period of SCL clock	$f_{SCL} \leq 100kHz$	4.0			
		$f_{SCL} > 100kHz$	0.6			
$t_{SU;STA}$	Set-up time for a repeated START condition	$f_{SCL} \leq 100kHz$	4.7			
		$f_{SCL} > 100kHz$	0.6			
$t_{HD;DAT}$	Data hold time	$f_{SCL} \leq 100kHz$	0		3.45	µs
		$f_{SCL} > 100kHz$	0		0.9	
$t_{SU;DAT}$	Data setup time	$f_{SCL} \leq 100kHz$	250			
		$f_{SCL} > 100kHz$	100			
$t_{SU;STO}$	Setup time for STOP condition	$f_{SCL} \leq 100kHz$	4.0			
		$f_{SCL} > 100kHz$	0.6			
t_{BUF}	Bus free time between a STOP and START condition	$f_{SCL} \leq 100kHz$	4.7			
		$f_{SCL} > 100kHz$	1.3			

Notes:
1. Required only for $f_{SCL} > 100kHz$.
2. C_b = Capacitance of one bus line in pF.
3. f_{PER} = Peripheral clock frequency.

32.5 Atmel ATxmega256D3

32.5.1 Absolute maximum ratings

Stresses beyond those listed in Table 32-116 under may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Table 32-116. Absolute maximum ratings.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
V_{CC}	Power supply voltage		-0.3		4	V
I_{VCC}	Current into a V_{CC} pin				200	mA
I_{GND}	Current out of a Gnd pin				200	
V_{PIN}	Pin voltage with respect to Gnd and V_{CC}		-0.5		V_{CC} + 0.5	V
I_{PIN}	I/O pin sink/source current		-25		25	mA
T_A	Storage temperature		-65		150	°C
T_j	Junction temperature				150	

32.5.2 General operating ratings

The device must operate within the ratings listed in Table 32-117 in order for all other electrical characteristics and typical characteristics of the device to be valid.

Table 32-117. General operating conditions.

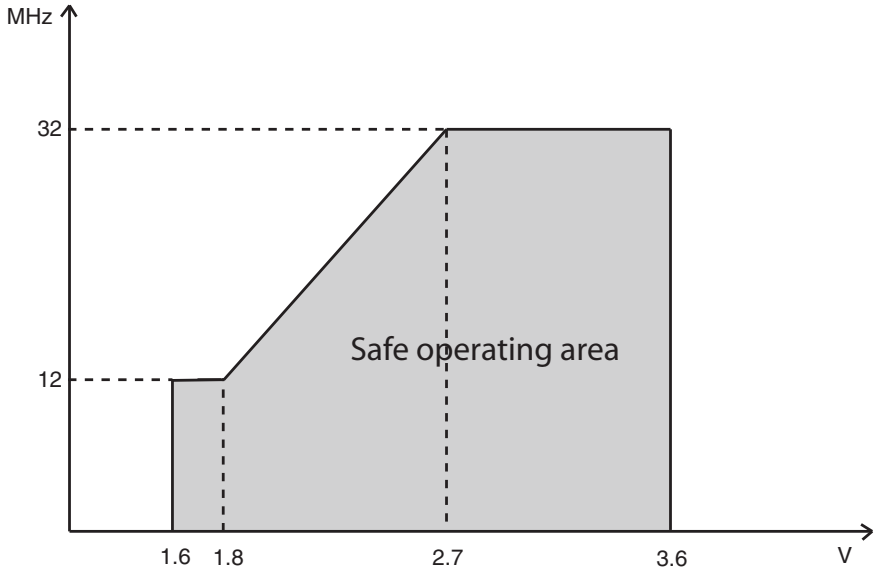
Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
V_{CC}	Power supply voltage		1.60		3.6	V
AV_{CC}	Analog supply voltage		1.60		3.6	
T_A	Temperature range		-40		85	°C
T_j	Junction temperature		-40		105	

Table 32-118. Operating voltage and frequency.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
Clk_{CPU}	CPU clock frequency	V_{CC} = 1.6V	0		12	MHz
		V_{CC} = 1.8V	0		12	
		V_{CC} = 2.7V	0		32	
		V_{CC} = 3.6V	0		32	

The maximum CPU clock frequency depends on V_{CC}. As shown in Figure 32-29 on page 138 the frequency vs. V_{CC} curve is linear between 1.8V < V_{CC} < 2.7V.

Figure 32-29. Maximum frequency vs. V_{CC}.



32.5.3 Current consumption

Table 32-119. Current consumption for Active mode and sleep modes.

Symbol	Parameter	Condition		Min.	Typ.	Max.	Units
I_{CC}	Active power consumption (1)	32kHz, Ext. Clk	V_{CC} = 1.8V		60		µA
			V_{CC} = 3.0V		140		
		1MHz, Ext. Clk	V_{CC} = 1.8V		245		
			V_{CC} = 3.0V		550		
		2MHz, Ext. Clk	V_{CC} = 1.8V		440	700	
			V_{CC} = 3.0V		0.9	1.5	mA
		32MHz, Ext. Clk			9.0	15	
	Idle power consumption (2)	32kHz, Ext. Clk	V_{CC} = 1.8V		3.0		µA
			V_{CC} = 3.0V		3.5		
		1MHz, Ext. Clk	V_{CC} = 1.8V		55		
			V_{CC} = 3.0V		110		
		2MHz, Ext. Clk	V_{CC} = 1.8V		105	350	
			V_{CC} = 3.0V		215	650	
		32MHz, Ext. Clk			3.4	8.0	mA
	Power-down power consumption	T = 25°C	V_{CC} = 3.0V		0.1	1.0	µA
		T = 85°C			3.5	6.0	
		WDT and sampled BOD enabled, T = 25°C	V_{CC} = 3.0V		1.5	2.0	
		WDT and sampled BOD enabled, T = 85°C			5.8	10	
	Power-save power consumption (3)	RTC from ULP clock, WDT and sampled BOD enabled, T = 25°C	V_{CC} = 1.8V		1.3		
			V_{CC} = 3.0V		1.4		
		RTC from 1.024kHz low power 32.768kHz TOSC, T = 25°C	V_{CC} = 1.8V		0.7	2.0	
			V_{CC} = 3.0V		0.8	2.0	
		RTC from low power 32.768kHz TOSC, T = 25°C	V_{CC} = 1.8V		0.9	3.0	
			V_{CC} = 3.0V		1.1	3.0	
	Reset power consumption	Current through $\overline{\text{RESET}}$ pin substracted	V_{CC} = 3.0V		170		

Notes:
1. All power reduction registers set including FPRM and EPRM.
2. All power reduction registers set without FPRM and EPRM.
3. Maximum limits are based on characterization, and not tested in production.

Table 32-120. Current consumption for modules and peripherals.

Symbol	Parameter	Condition [1]		Min.	Typ.	Max.	Units
I_{CC}	ULP oscillator				0.9		µA
	32.768kHz int. oscillator				25		
	2MHz int. oscillator				78		
		DFLL enabled with 32.768kHz int. osc. as reference			110		
	32MHz int. oscillator				250		
		DFLL enabled with 32.768kHz int. osc. as reference			440		
	PLL	20× multiplication factor, 32MHz int. osc. DIV4 as reference			310		
	Watchdog timer				1.0		
	BOD	Continuous mode			132		
		Sampled mode, includes ULP oscillator			1.4		
	Internal 1.0V reference				185		
	Temperature sensor				182		
	ADC	16ksps V_{REF} = Ext. ref.			1.12		mA
			CURRLIMIT = LOW		1.01		
			CURRLIMIT = MEDIUM		0.9		
			CURRLIMIT = HIGH		0.8		
		75ksps V_{REF} = Ext. ref.	CURRLIMIT = LOW		1.7		
		300ksps V_{REF} = Ext. ref.			3.1		
	USART	Rx and Tx enabled, 9600 BAUD			9.5		µA
	Flash memory and EEPROM programming				10		mA

Note: 1. All parameters measured as the difference in current consumption between module enabled and disabled. All data at V_{CC} = 3.0V, Clk_{SYS} = 1MHz external clock without prescaling, T = 25°C unless other conditions are given.

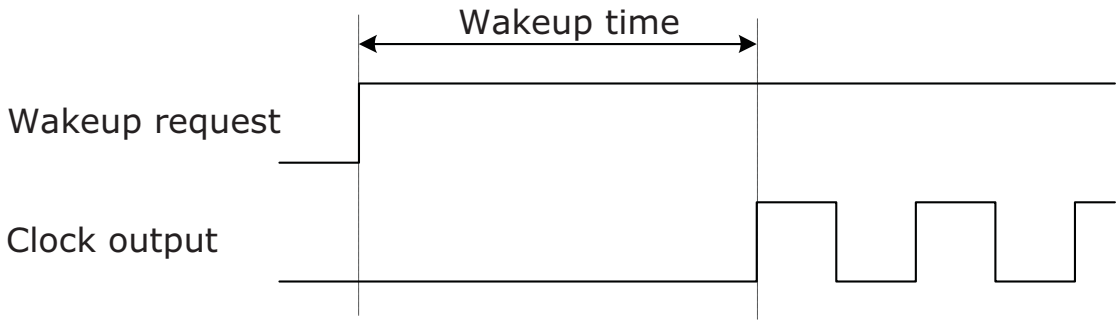
32.5.4 Wake-up time from sleep modes

Table 32-121. Device wake-up time from sleep modes with various system clock sources.

Symbol	Parameter	Condition	Min.	Typ. (1)	Max.	Units
t_{wakeup}	Wake-up time from idle, standby, and extended standby mode	External 2MHz clock		2.0		µs
		32.768kHz internal oscillator		125		
		2MHz internal oscillator		2.0		
		32MHz internal oscillator		0.2		
	Wake-up time from power-save and power-down mode	External 2MHz clock		4.6		
		32.768kHz internal oscillator		330		
		2MHz internal oscillator		9.5		
		32MHz internal oscillator		5.6		

Note: 1. The wake-up time is the time from the wake-up request is given until the peripheral clock is available on pin, see Figure 32-30. All peripherals and modules start execution from the first clock cycle, expect the CPU that is halted for four clock cycles before program execution starts.

Figure 32-30. Wake-up time definition.



32.5.5 I/O pin characteristics

The I/O pins complies with the JEDEC LVTTL and LVCMOS specification and the high- and low level input and output voltage limits reflect or exceed this specification.

Table 32-122. I/O pin characteristics.

Symbol	Parameter	Condition		Min.	Typ.	Max.	Units
I_{OH} (1)/ I_{OL} (2)	I/O pin source/sink current			-15		15	mA
V_{IH}	High level input voltage	V_{CC} = 2.4 - 3.6V		0.7 * V_{CC}		V_{CC} + 0.5	V
		V_{CC} = 1.6 - 2.4V		0.8 * V_{CC}		V_{CC} + 0.5	
V_{IL}	Low level input voltage	V_{CC} = 2.4 - 3.6V		-0.5		0.3 * V_{CC}	
		V_{CC} = 1.6 - 2.4V		-0.5		0.2 * V_{CC}	
V_{OH}	High level output voltage	V_{CC} = 3.3V	I_{OH} = -4mA	2.6	2.9		
		V_{CC} = 3.0V	I_{OH} = -3mA	2.1	2.6		
		V_{CC} = 1.8V	I_{OH} = -1mA	1.4	1.6		
V_{OL}	Low level output voltage	V_{CC} = 3.3V	I_{OL} = 8mA		0.4	0.76	
		V_{CC} = 3.0V	I_{OL} = 5mA		0.3	0.64	
		V_{CC} = 1.8V	I_{OL} = 3mA		0.2	0.46	
I_{IN}	Input leakage current I/O pin	T = 25°C			<0.01	1.0	µA
R_P	Pull/buss keeper resistor				25		kΩ

Notes:
1. The sum of all I_{OH} for PORTA and PORTB must not exceed 100mA.
   The sum of all I_{OH} for PORTC, PORTD, PORTE must for each port not exceed 200mA.
   The sum of all I_{OH} for pins PF[0-5] on PORTF must not exceed 200mA.
   The sum of all I_{OL} for pins PF[6-7] on PORTF, PORTR and PDI must not exceed 100mA.
2. The sum of all I_{OL} for PORTA and PORTB must not exceed 100mA.
   The sum of all I_{OL} for PORTC, PORTD, PORTE must for each port not exceed 200mA.
   The sum of all I_{OL} for pins PF[0-5] on PORTF must not exceed 200mA.
   The sum of all I_{OL} for pins PF[6-7] on PORTF, PORTR and PDI must not exceed 100mA.

32.5.6 ADC characteristics

Table 32-123. Power supply, reference and input range.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
AV_{CC}	Analog supply voltage		V_{CC} - 0.3		V_{CC} + 0.3	V
V_{REF}	Reference voltage		1		AV_{CC} - 0.6	
R_{in}	Input resistance	Switched			4.5	kΩ
C_{in}	Input capacitance	Switched			5	pF
R_{AREF}	Reference input resistance	(leakage only)		>10		MΩ
C_{AREF}	Reference input capacitance	Static load		7		pF
V_{in}	Input range		0		V_{REF}	V
	Conversion range	Differential mode, Vinp - Vinn	$-V_{REF}$		V_{REF}	
	Conversion range	Single ended unsigned mode, Vinp	-ΔV		V_{REF} - ΔV	
ΔV	Fixed offset voltage			200		lsb

Table 32-124. Clock and timing.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
Clk_{ADC}	ADC clock frequency	Maximum is 1/4 of peripheral clock frequency	100		1800	kHz
		Measuring internal signals	100		125	
f_{ClkADC}	Sample rate		16		300	ksps
f_{ADC}	Sample rate	Current limitation (CURRLIMIT) off	16		300	
		CURRLIMIT = LOW	16		250	
		CURRLIMIT = MEDIUM	16		150	
		CURRLIMIT = HIGH	16		50	
	Sampling time	Configurable in steps of 1/2 Clk_{ADC} cycles up to 32 Clk_{ADC} cycles	0.28		320	µs
	Conversion time (latency)	(RES+2)/2 + 1 + GAIN RES (Resolution) = 8 or 12, GAIN = 0 to 3	5.5		10	Clk_{ADC} cycles
	Start-up time	ADC clock cycles		12	24	
	ADC settling time	After changing reference or input mode		7	7	

Table 32-125. Accuracy characteristics.

Symbol	Parameter	Condition [2]		Min.	Typ.	Max.	Units
RES	Resolution	12-bit resolution	Differential	8	12	12	Bits
			Single ended signed	7	11	11	
			Single ended unsigned	8	12	12	
INL [1]	Integral non-linearity	Differential mode	16ksps, V_{REF} = 3V		0.5	1	lsb
			16ksps, all V_{REF}		0.8	2	
			300ksps, V_{REF} = 3V		0.6	1	
			300ksps, all V_{REF}		1	2	
		Single ended unsigned mode	16ksps, V_{REF} = 3.0V		0.5	1	
			16ksps, all V_{REF}		1.3	2	
DNL [1]	Differential non-linearity	Differential mode	16ksps, V_{REF} = 3V		0.3	1	
			16ksps, all V_{REF}		0.5	1	
			300ksps, V_{REF} = 3V		0.3	1	
			300ksps, all V_{REF}		0.5	1	
		Single ended unsigned mode	16ksps, V_{REF} = 3.0V		0.6	1	
			16ksps, All V_{REF}		0.6	1	
	Offset error	Differential mode	300ksps, V_{REF} = 3V		-7		mV
			Temperature drift, V_{REF} = 3V		0.01		mV/K
			Operating voltage drift		0.16		mV/V
	Gain error	Differential mode	External reference		-5		mV
			AV_{CC}/1.6		-5		
			AV_{CC}/2.0		-6		
			Bandgap		±10		
			Temperature drift		0.02		mV/K
			Operating voltage drift		2		mV/V
	Gain error	Single ended unsigned mode	External reference		-8		mV
			AV_{CC}/1.6		-8		
			AV_{CC}/2.0		-8		
			Bandgap		±10		
			Temperature drift		0.03		mV/K
			Operating voltage drift		2		mV/V

Notes:
1. Maximum numbers are based on characterisation and not tested in production, and valid for 5% to 95% input voltage range.
2. Unless otherwise noted all linearity, offset, and gain error numbers are valid under the condition that external VREF is used.

Table 32-126. Gain stage characteristics.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
R_{in}	Input resistance	Switched in normal mode		4.0		kΩ
C_{sample}	Input capacitance	Switched in normal mode		4.4		pF
	Signal range	Gain stage output	0		AV_{CC} - 0.6	V
	Propagation delay	ADC conversion rate	1/2	1	3	Clk_{ADC} cycles
	Clock frequency	Same as ADC	100		1800	kHz
	Gain error	0.5× gain, normal mode		-1		%
		1× gain, normal mode		-1		
		8× gain, normal mode		-1		
		64× gain, normal mode		5		
	Offset error, input referred	0.5× gain, normal mode		10		mV
		1× gain, normal mode		5		
		8× gain, normal mode		-20		
		64× gain, normal mode		-126		

32.5.7 Analog comparator characteristics

Table 32-127. Analog comparator characteristics.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
V_{off}	Input offset voltage			10		mV
I_{lk}	Input leakage current			<10	50	nA
	Input voltage range		-0.1		AV_{CC}	V
	AC startup time			50		µs
V_{hys1}	Hysteresis, none	V_{CC} = 1.6V - 3.6V		0		mV
V_{hys2}	Hysteresis, small	V_{CC} = 1.6V - 3.6V		15		
V_{hys3}	Hysteresis, large	V_{CC} = 1.6V - 3.6V		30		
t_{delay}	Propagation delay	V_{CC} = 3.0V, T = 85°C		20	40	ns
		V_{CC} = 3.0V		17		
	64-level voltage scaler	Integral non-linearity (INL)		0.3	0.5	lsb
	Current source accuracy after calibration			5		%
	Current source calibration range	Single mode	4		6	µA

32.5.8 Bandgap and internal 1.0V reference characteristics

Table 32-128. Bandgap and internal 1.0V reference characteristics.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
	Startup time	As reference for ADC		1 Clk_{PER} + 2.5µs		µs
		As input voltage to ADC and AC		1.5		
	Bandgap voltage			1.1		V
INT1V	Internal 1.00V reference	T = 85°C, after calibration	0.99	1.0	1.01	
	Variation over voltage and temperature	Calibrated at T = 85°C		1		%

32.5.9 Brownout detection characteristics

Table 32-129. Brownout detection characteristics (1).

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
V_{BOT}	BOD level 0 falling V_{CC}		1.40	1.60	1.70	V
	BOD level 1 falling V_{CC}			1.8		
	BOD level 2 falling V_{CC}			2.0		
	BOD level 3 falling V_{CC}			2.2		
	BOD level 4 falling V_{CC}			2.4		
	BOD level 5 falling V_{CC}			2.6		
	BOD level 6 falling V_{CC}			2.8		
	BOD level 7 falling V_{CC}			3.0		
t_{BOD}	Detection time	Continuous mode		0.4		µs
		Sampled mode		1000		
V_{HYST}	Hysteresis			1.0		%

Note: 1. BOD is calibrated at 85°C within BOD level 0 values, and BOD level 0 is the default level.

32.5.10 External reset characteristics

Table 32-130. External reset characteristics.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
t_{EXT}	Minimum reset pulse width		1000	90		ns
V_{RST}	Reset threshold voltage	V_{CC} = 2.7 - 3.6V		0.45 * V_{CC}		V
		V_{CC} = 1.6 - 2.7V		0.45 * V_{CC}		
R_{RST}	Reset pin pull-up resistor			25		kΩ

32.5.11 Power-on reset characteristics

Table 32-131. Power-on reset characteristics.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
V_{POT-} (1)	POR threshold voltage falling V_{CC}	V_{CC} falls faster than 1V/ms	0.4	1.0		V
		V_{CC} falls at 1V/ms or slower	0.8	1.3		
V_{POT+}	POR threshold voltage rising V_{CC}			1.3	1.59	

Note: 1. V_{POT-} values are only valid when BOD is disabled. When BOD is enabled $V_{POT-} = V_{POT+}$.

32.5.12 Flash and EEPROM memory characteristics

Table 32-132. Endurance and data retention.

Symbol	Parameter	Condition		Min.	Typ.	Max.	Units
	Flash	Write/erase cycles	25°C	10K			Cycle
			85°C	10K			
		Data retention	25°C	100			Year
			55°C	25			
	EEPROM	Write/erase cycles	25°C	100K			Cycle
			85°C	100K			
		Data retention	25°C	100			Year
			55°C	25			

Table 32-133. Programming time.

Symbol	Parameter	Condition	Min.	Typ. (1)	Max.	Units
	Chip erase (2)	256KB flash, EEPROM		105		ms
	Application erase	Section erase		6		
	Flash	Page erase		4		
		Page write		4		
		Atomic page erase and write		8		
	EEPROM	Page erase		4		
		Page write		4		
		Atomic page erase and write		8		

Notes: 1. Programming is timed from the 2MHz internal oscillator.
2. EEPROM is not erased if the EESAVE fuse is programmed.

32.5.13 Clock and oscillator characteristics

32.5.13.1 Calibrated 32.768kHz internal oscillator characteristics

Table 32-134. 32.768kHz internal oscillator characteristics.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
	Frequency			32.768		kHz
	Factory calibration accuracy	T = 85°C, V_{CC} = 3.0V	-0.5		0.5	%
	User calibration accuracy		-0.5		0.5	

32.5.13.2 Calibrated 2MHz RC internal oscillator characteristics

Table 32-135. 2MHz internal oscillator characteristics.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
	Frequency range	DFLL can tune to this frequency over voltage and temperature	1.8	2.0	2.2	MHz
	Factory calibrated frequency			2.0		
	Factory calibration accuracy	T = 85°C, V_{CC} = 3.0V	-1.5		1.5	%
	User calibration accuracy		-0.2		0.2	
	DFLL calibration stepsize			0.18		

32.5.13.3 Calibrated 32MHz internal oscillator characteristics

Table 32-136. 32MHz internal oscillator characteristics.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
	Frequency range	DFLL can tune to this frequency over voltage and temperature	30	32	55	MHz
	Factory calibrated frequency			32		
	Factory calibration accuracy	T = 85°C, V_{CC} = 3.0V	-1.5		1.5	%
	User calibration accuracy		-0.2		0.2	
	DFLL calibration step size			0.19		

32.5.13.4 32kHz internal ULP oscillator characteristics

Table 32-137. 32kHz internal ULP oscillator characteristics.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
	Factory calibrated frequency			32		kHz
	Factory calibration accuracy	T = 85°C, V_{CC} = 3.0V	-12		12	%

32.5.13.5 Internal Phase Locked Loop (PLL) characteristics

Table 32-138. Internal PLL characteristics.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
f_{IN}	Input frequency	Output frequency must be within f_{OUT}	0.4		64	MHz
f_{OUT}	Output frequency (1)	V_{CC} = 1.6 - 1.8V	20		48	
		V_{CC} = 2.7 - 3.6V	20		128	
	Start-up time			25		µs
	Re-lock time			25		

Note: 1. The maximum output frequency vs. supply voltage is linear between 1.8V and 2.7V, and can never be higher than four times the maximum CPU frequency.

32.5.13.6 External clock characteristics

Figure 32-31.External clock drive waveform.

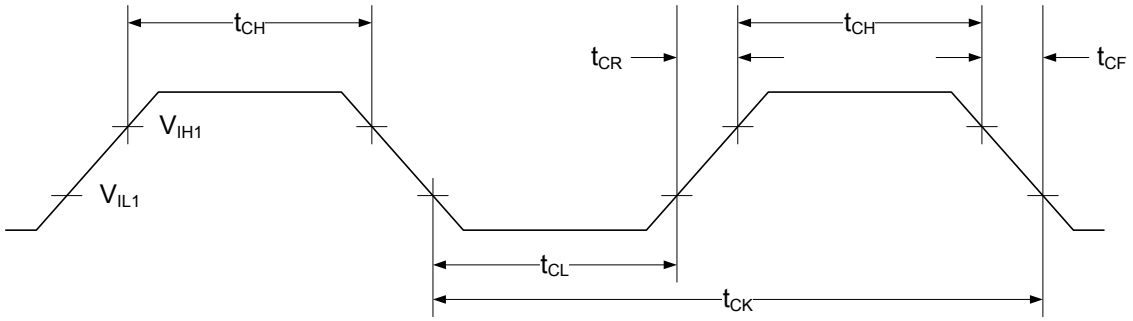


Table 32-139.External clock used as system clock without prescaling.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
$1/t_{CK}$	Clock Frequency (1)	V_{CC} = 1.6 - 1.8V	0		12	MHz
		V_{CC} = 2.7 - 3.6V	0		32	
t_{CK}	Clock Period	V_{CC} = 1.6 - 1.8V	83.3			ns
		V_{CC} = 2.7 - 3.6V	31.5			
t_{CH}	Clock High Time	V_{CC} = 1.6 - 1.8V	30.0			ns
		V_{CC} = 2.7 - 3.6V	12.5			
t_{CL}	Clock Low Time	V_{CC} = 1.6 - 1.8V	30.0			ns
		V_{CC} = 2.7 - 3.6V	12.5			
t_{CR}	Rise Time (for maximum frequency)	V_{CC} = 1.6 - 1.8V			10	ns
		V_{CC} = 2.7 - 3.6V			3	
t_{CF}	Fall Time (for maximum frequency)	V_{CC} = 1.6 - 1.8V			10	ns
		V_{CC} = 2.7 - 3.6V			3	
Δt_{CK}	Change in period from one clock cycle to the next				10	%

Note: 1. The maximum frequency vs. supply voltage is linear between 1.6V and 2.7V, and the same applies for all other parameters with supply voltage conditions.

Table 32-140.External clock with prescaler [1] for system clock.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
$1/t_{CK}$	Clock Frequency [2]	V_{CC} = 1.6 - 1.8V	0		90	MHz
		V_{CC} = 2.7 - 3.6V	0		142	
t_{CK}	Clock Period	V_{CC} = 1.6 - 1.8V	11			ns
		V_{CC} = 2.7 - 3.6V	7			
t_{CH}	Clock High Time	V_{CC} = 1.6 - 1.8V	4.5			ns
		V_{CC} = 2.7 - 3.6V	2.4			
t_{CL}	Clock Low Time	V_{CC} = 1.6 - 1.8V	4.5			ns
		V_{CC} = 2.7 - 3.6V	2.4			
t_{CR}	Rise Time (for maximum frequency)	V_{CC} = 1.6 - 1.8V			1.5	ns
		V_{CC} = 2.7 - 3.6V			1.0	
t_{CF}	Fall Time (for maximum frequency)	V_{CC} = 1.6 - 1.8V			1.5	ns
		V_{CC} = 2.7 - 3.6V			1.0	
Δt_{CK}	Change in period from one clock cycle to the next				10	%

Notes: 1. System Clock Prescalers must be set so that maximum CPU clock frequency for device is not exceeded.
2. The maximum frequency vs. supply voltage is linear between 1.6V and 2.7V, and the same applies for all other parameters with supply voltage conditions.

32.5.13.7 External 16MHz crystal oscillator and XOSC characteristics

Table 32-141. External 16MHz crystal oscillator and XOSC characteristics.

Symbol	Parameter	Condition		Min.	Typ.	Max.	Units
	Cycle to cycle jitter	XOSCPWR=0	FRQRANGE=0		0		ns
			FRQRANGE=1, 2, or 3		0		
		XOSCPWR=1			0		
	Long term jitter	XOSCPWR=0	FRQRANGE=0		0		
			FRQRANGE=1, 2, or 3		0		
		XOSCPWR=1			0		
	Frequency error	XOSCPWR=0	FRQRANGE=0		0.03		%
			FRQRANGE=1		0.03		
			FRQRANGE=2 or 3		0.03		
		XOSCPWR=1			0.003		
	Duty cycle	XOSCPWR=0	FRQRANGE=0		50		
			FRQRANGE=1		50		
			FRQRANGE=2 or 3		50		
		XOSCPWR=1			50		

Symbol	Parameter	Condition		Min.	Typ.	Max.	Units
R_Q	Negative impedance [1]	XOSCPWR=0, FRQRANGE=0	0.4MHz resonator, CL=100pF		44k		Ω
			1MHz crystal, CL=20pF		67k		
			2MHz crystal, CL=20pF		67k		
		XOSCPWR=0, FRQRANGE=1, CL=20pF	2MHz crystal		82k		
			8MHz crystal		1500		
			9MHz crystal		1500		
		XOSCPWR=0, FRQRANGE=2, CL=20pF	8MHz crystal		2700		
			9MHz crystal		2700		
			12MHz crystal		1000		
		XOSCPWR=0, FRQRANGE=3, CL=20pF	9MHz crystal		3600		
			12MHz crystal		1300		
			16MHz crystal		590		
		XOSCPWR=1, FRQRANGE=0, CL=20pF	9MHz crystal		390		
			12MHz crystal		50		
			16MHz crystal		10		
		XOSCPWR=1, FRQRANGE=1, CL=20pF	9MHz crystal		1500		
			12MHz crystal		650		
			16MHz crystal		270		
		XOSCPWR=1, FRQRANGE=2, CL=20pF	12MHz crystal		1000		
			16MHz crystal		440		
		XOSCPWR=1, FRQRANGE=3, CL=20pF	12MHz crystal		1300		
			16MHz crystal		590		ms
	Start-up time	XOSCPWR=0, FRQRANGE=0	0.4MHz resonator, CL=100pF		1.0		
		XOSCPWR=0, FRQRANGE=1	2MHz resonator, CL=20pF		2.6		
		XOSCPWR=0, FRQRANGE=2	8MHz resonator, CL=20pF		0.8		
		XOSCPWR=0, FRQRANGE=3	12MHz resonator, CL=20pF		1.0		
		XOSCPWR=1, FRQRANGE=3	16MHz resonator, CL=20pF		1.4		
C_{XTAL1}	Parasitic capacitance XTAL1 pin				5.9		pF
C_{XTAL2}	Parasitic capacitance XTAL2 pin				8.3		
C_{LOAD}	Paracitic capacitance load				3.5		

Notes: 1. Numbers for negative impedance are not tested in production but guaranteed from design and characterization.

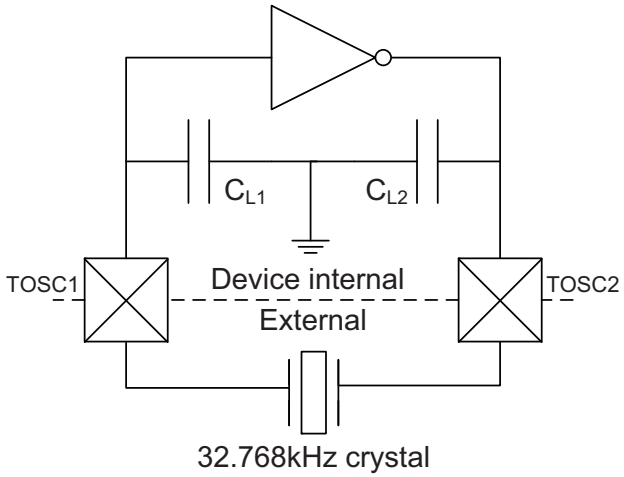
32.5.13.8 External 32.768kHz crystal oscillator and TOSC characteristics

Table 32-142. External 32.768kHz crystal oscillator and TOSC characteristics.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
ESR/R1	Recommended crystal equivalent series resistance (ESR)	Crystal load capacitance 6.5pF			60	kΩ
		Crystal load capacitance 9.0pF			35	
		Crystal load capacitance 12pF			28	
C_{TOSC1}	Parasitic capacitance TOSC1 pin			3.5		pF
C_{TOSC2}	Parasitic capacitance TOSC2 pin			3.5		
	Recommended safety factor	Capacitance load matched to crystal specification	3			

Note: See Figure 32-32 for definition.

Figure 32-32. TOSC input capacitance.



The parasitic capacitance between the TOSC pins is C_{L1} + C_{L2} in series as seen from the crystal when oscillating without external capacitors.

32.5.14 SPI characteristics

Figure 32-33. SPI timing requirements in master mode.

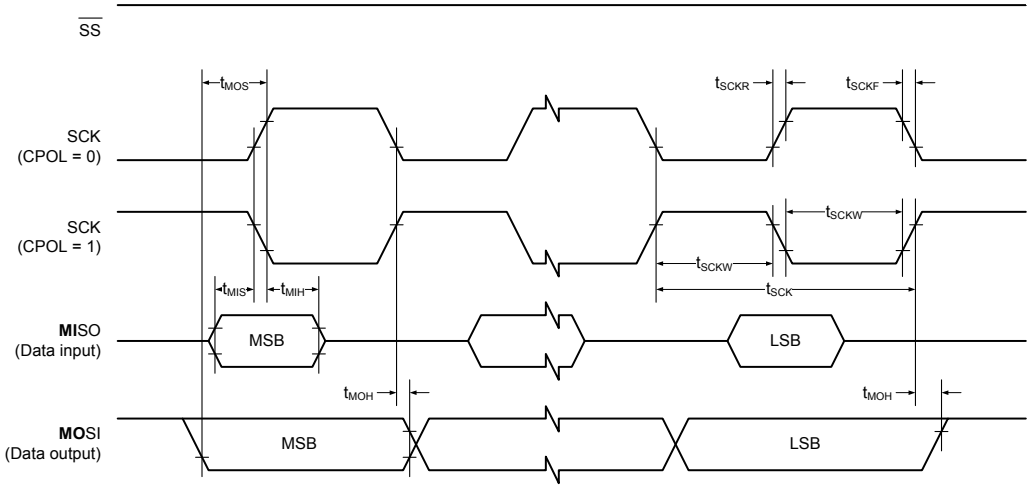


Figure 32-34. SPI timing requirements in slave mode.

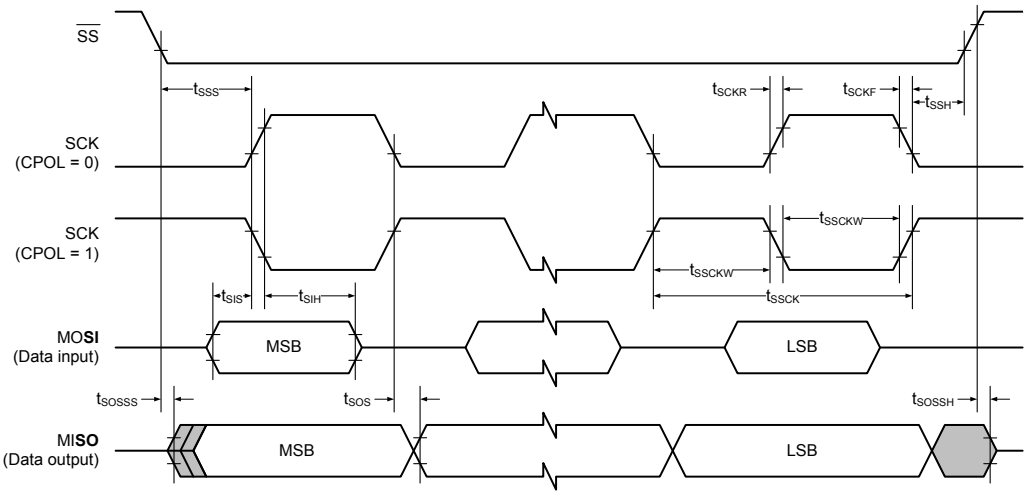


Table 32-143. SPI timing characteristics and requirements.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
t_{SCK}	SCK period	Master		(See Table 20-3 in XMEGA D manual)		ns
t_{SCKW}	SCK high/low width	Master		0.5 * SCK		
t_{SCKR}	SCK rise time	Master		2.7		
t_{SCKF}	SCK fall time	Master		2.7		
t_{MIS}	MISO setup to SCK	Master		10		
t_{MIH}	MISO hold after SCK	Master		10		
t_{MOS}	MOSI setup SCK	Master		0.5 * SCK		
t_{MOH}	MOSI hold after SCK	Master		1		
t_{SSCK}	Slave SCK Period	Slave	4 * t Clk_{PER}			
t_{SSCKW}	SCK high/low width	Slave	2 * t Clk_{PER}			
t_{SSCKR}	SCK rise time	Slave			1600	
t_{SSCKF}	SCK fall time	Slave			1600	
t_{SIS}	MOSI setup to SCK	Slave	3			
t_{SIH}	MOSI hold after SCK	Slave	t Clk_{PER}			
t_{SSS}	$\overline{SS}$ setup to SCK	Slave	21			
t_{SSH}	$\overline{SS}$ hold after SCK	Slave	20			
t_{SOS}	MISO setup SCK	Slave		8		
t_{SOH}	MISO hold after SCK	Slave		13		
t_{SOSS}	MISO setup after $\overline{SS}$ low	Slave		11		
t_{SOSH}	MISO hold after $\overline{SS}$ high	Slave		8		

32.5.15 Two-wire interface characteristics

Table 32-144 on page 155 describes the requirements for devices connected to the Two-Wire Interface Bus. The Atmel AVR XMEGA Two-Wire Interface meets or exceeds these requirements under the noted conditions. Timing symbols refer to Figure 32-35.

Figure 32-35. Two-wire interface bus timing.

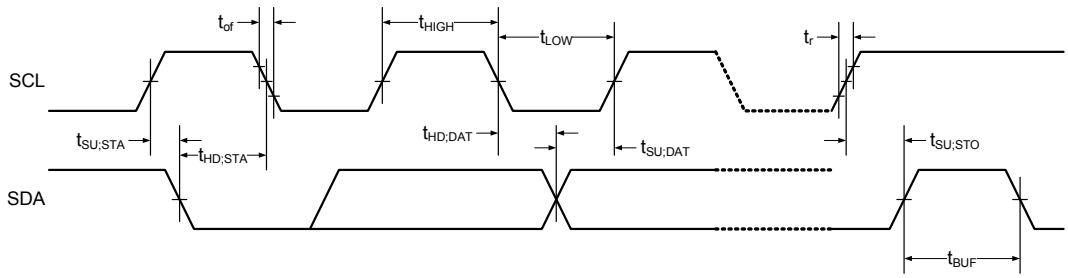


Table 32-144. Two-wire interface characteristics.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
V_{IH}	Input high voltage		$0.7V_{CC}$		V_{CC} + 0.5	V
V_{IL}	Input low voltage		-0.5		$0.3V_{CC}$	
V_{hys}	Hysteresis of Schmitt trigger inputs		$0.05V_{CC}$ (1)			
V_{OL}	Output low voltage	3mA, sink current	0		0.4	
t_r	Rise time for both SDA and SCL		$20 + 0.1C_b$ (1)(2)		300	ns
t_{of}	Output fall time from V_{IHmin} to V_{ILmax}	$10pF < C_b < 400pF$ (2)	$20 + 0.1C_b$ (1)(2)		250	
t_{SP}	Spikes suppressed by input filter		0		50	
I_I	Input current for each I/O pin	$0.1V_{CC} < V_I < 0.9V_{CC}$	-10		10	µA
C_I	Capacitance for each I/O pin				10	pF
f_{SCL}	SCL clock frequency	f_{PER} (3) > max($10f_{SCL}$, 250kHz)	0		400	kHz
R_P	Value of pull-up resistor	$f_{SCL} \leq 100kHz$	$\frac{V_{CC} - 0.4V}{3mA}$		$\frac{100ns}{C_b}$	Ω
		$f_{SCL} > 100kHz$			$\frac{300ns}{C_b}$	
$t_{HD;STA}$	Hold time (repeated) START condition	$f_{SCL} \leq 100kHz$	4.0			µs
		$f_{SCL} > 100kHz$	0.6			
t_{LOW}	Low period of SCL clock	$f_{SCL} \leq 100kHz$	4.7			
		$f_{SCL} > 100kHz$	1.3			
t_{HIGH}	High period of SCL clock	$f_{SCL} \leq 100kHz$	4.0			
		$f_{SCL} > 100kHz$	0.6			
$t_{SU;STA}$	Set-up time for a repeated START condition	$f_{SCL} \leq 100kHz$	4.7			
		$f_{SCL} > 100kHz$	0.6			
$t_{HD;DAT}$	Data hold time	$f_{SCL} \leq 100kHz$	0		3.45	µs
		$f_{SCL} > 100kHz$	0		0.9	
$t_{SU;DAT}$	Data setup time	$f_{SCL} \leq 100kHz$	250			
		$f_{SCL} > 100kHz$	100			
$t_{SU;STO}$	Setup time for STOP condition	$f_{SCL} \leq 100kHz$	4.0			
		$f_{SCL} > 100kHz$	0.6			
t_{BUF}	Bus free time between a STOP and START condition	$f_{SCL} \leq 100kHz$	4.7			
		$f_{SCL} > 100kHz$	1.3			

Notes:
1. Required only for $f_{SCL} > 100kHz$.
2. C_b = Capacitance of one bus line in pF.
3. f_{PER} = Peripheral clock frequency.

32.6 Atmel ATxmega384D3

32.6.1 Absolute maximum ratings

Stresses beyond those listed in Table 32-145 under may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Table 32-145. Absolute maximum ratings.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
V_{CC}	Power supply voltage		-0.3		4	V
I_{VCC}	Current into a V_{CC} pin				200	mA
I_{GND}	Current out of a Gnd pin				200	
V_{PIN}	Pin voltage with respect to Gnd and V_{CC}		-0.5		V_{CC} + 0.5	V
I_{PIN}	I/O pin sink/source current		-25		25	mA
T_A	Storage temperature		-65		150	°C
T_j	Junction temperature				150	

32.6.2 General operating ratings

The device must operate within the ratings listed in Table 32-146 in order for all other electrical characteristics and typical characteristics of the device to be valid.

Table 32-146. General operating conditions.

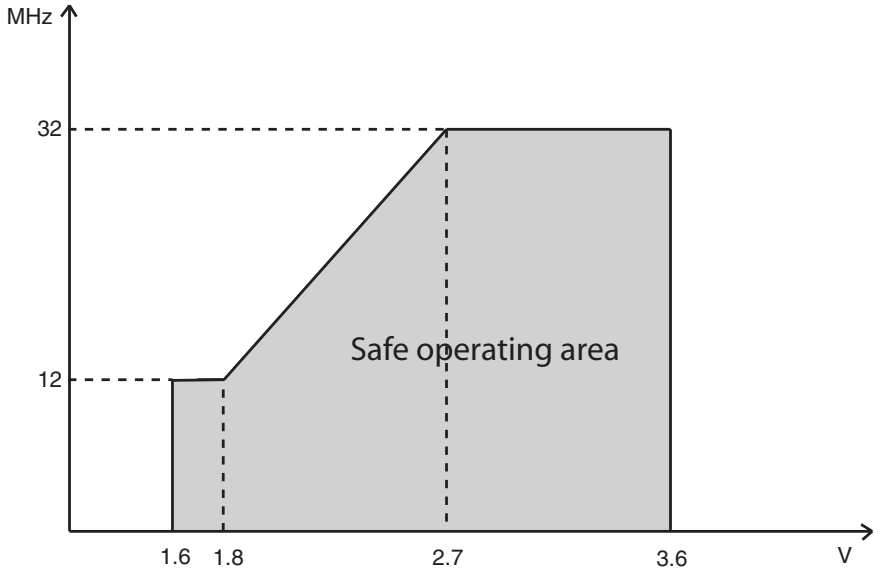
Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
V_{CC}	Power supply voltage		1.60		3.6	V
AV_{CC}	Analog supply voltage		1.60		3.6	
T_A	Temperature range		-40		85	°C
T_j	Junction temperature		-40		105	

Table 32-147. Operating voltage and frequency.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
Clk_{CPU}	CPU clock frequency	V_{CC} = 1.6V	0		12	MHz
		V_{CC} = 1.8V	0		12	
		V_{CC} = 2.7V	0		32	
		V_{CC} = 3.6V	0		32	

The maximum CPU clock frequency depends on V_{CC}. As shown in Figure 32-36 on page 157 the frequency vs. V_{CC} curve is linear between 1.8V < V_{CC} < 2.7V.

Figure 32-36. Maximum frequency vs. V_{CC}.



32.6.3 Current consumption

Table 32-148. Current consumption for Active mode and sleep modes.

Symbol	Parameter	Condition		Min.	Typ.	Max.	Units
I_{CC}	Active power consumption (1)	32kHz, Ext. Clk	V_{CC} = 1.8V		150		µA
			V_{CC} = 3.0V		320		
		1MHz, Ext. Clk	V_{CC} = 1.8V		410		
			V_{CC} = 3.0V		830		
		2MHz, Ext. Clk	V_{CC} = 1.8V		660	800	
			V_{CC} = 3.0V		1.3	1.8	mA
		32MHz, Ext. Clk			10	15	
	Idle power consumption (1)	32kHz, Ext. Clk	V_{CC} = 1.8V		4		µA
			V_{CC} = 3.0V		5		
		1MHz, Ext. Clk	V_{CC} = 1.8V		50		
			V_{CC} = 3.0V		100		
		2MHz, Ext. Clk	V_{CC} = 1.8V		100	350	
			V_{CC} = 3.0V		200	600	
		32MHz, Ext. Clk			3.3	7	mA
	Power-down power consumption	T = 25°C	V_{CC} = 3.0V		0.2	1.0	µA
		T = 85°C			3.5	6.0	
		WDT and sampled BOD enabled, T = 25°C	V_{CC} = 3.0V		1.5	2.0	
		WDT and sampled BOD enabled, T = 85°C			6	10	
	Power-save power consumption (2)	RTC from ULP clock, WDT and sampled BOD enabled, T = 25°C	V_{CC} = 1.8V		1.4		
			V_{CC} = 3.0V		1.5		
		RTC from 1.024kHz low power 32.768kHz TOSC, T = 25°C	V_{CC} = 1.8V		0.7	2	
			V_{CC} = 3.0V		0.8	2	
		RTC from low power 32.768kHz TOSC, T = 25°C	V_{CC} = 1.8V		0.9	3	
			V_{CC} = 3.0V		1.1	3	
	Reset power consumption	Current through $\overline{\text{RESET}}$ pin substracted	V_{CC} = 3.0V		300		

Notes:
1. All Power Reduction Registers set.
2. Maximum limits are based on characterization, and not tested in production.

Table 32-149. Current consumption for modules and peripherals.

Symbol	Parameter	Condition [1]		Min.	Typ.	Max.	Units
I_{CC}	ULP oscillator				0.93		µA
	32.768kHz int. oscillator				27		
	2MHz int. oscillator				85		
		DFLL enabled with 32.768kHz int. osc. as reference			115		
	32MHz int. oscillator				240		
		DFLL enabled with 32.768kHz int. osc. as reference			430		
	PLL	20× multiplication factor, 32MHz int. osc. DIV4 as reference			300		
	Watchdog timer				1		
	BOD	Continuous mode			140		
		Sampled mode, includes ULP oscillator			1.3		
	Internal 1.0V reference				220		
	Temperature sensor				215		
	ADC	16ksps, V_{REF} = Ext. ref.			1.12		mA
			CURRLIMIT = LOW		1.01		
			CURRLIMIT = MEDIUM		0.9		
			CURRLIMIT = HIGH		0.8		
		75ksps, V_{REF} = Ext. ref.	CURRLIMIT = LOW		1.7		
		300ksps, V_{REF} = Ext. ref.			3.1		
	USART	Rx and Tx enabled, 9600 BAUD			9.5		µA
	Flash memory and EEPROM programming				4		mA

Note: 1. All parameters measured as the difference in current consumption between module enabled and disabled. All data at V_{CC} = 3.0V, Clk_{SYS} = 1MHz external clock without prescaling, T = 25°C unless other conditions are given.

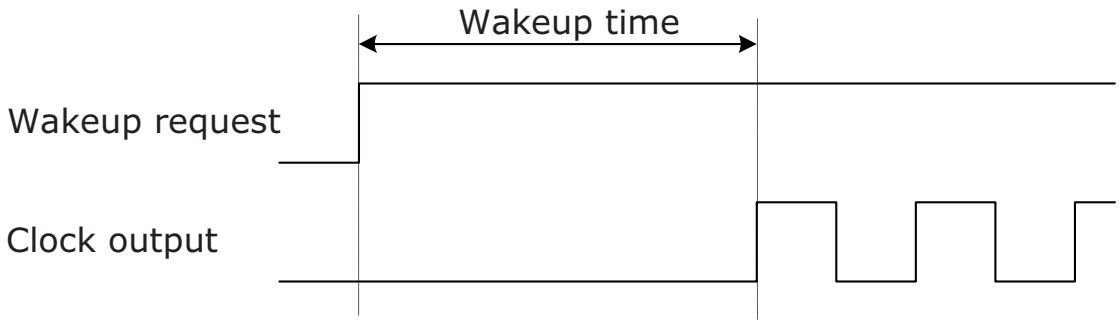
32.6.4 Wake-up time from sleep modes

Table 32-150. Device wake-up time from sleep modes with various system clock sources.

Symbol	Parameter	Condition	Min.	Typ. (1)	Max.	Units
t_{wakeup}	Wake-up time from idle, standby, and extended standby mode	External 2MHz clock		2.0		µs
		32.768kHz internal oscillator		130		
		2MHz internal oscillator		2.0		
		32MHz internal oscillator		0.2		
	Wake-up time from power-save and power-down mode	External 2MHz clock		4.5		
		32.768kHz internal oscillator		320		
		2MHz internal oscillator		9.0		
		32MHz internal oscillator		5.0		

Note: 1. The wake-up time is the time from the wake-up request is given until the peripheral clock is available on pin, see Figure 32-37 on page 160. All peripherals and modules start execution from the first clock cycle, expect the CPU that is halted for four clock cycles before program execution starts.

Figure 32-37. Wake-up time definition.



32.6.5 I/O pin characteristics

The I/O pins complies with the JEDEC LVTTL and LVCMOS specification and the high- and low level input and output voltage limits reflect or exceed this specification.

Table 32-151. I/O pin characteristics.

Symbol	Parameter	Condition		Min.	Typ.	Max.	Units
I_{OH} (1)/ I_{OL} (2)	I/O pin source/sink current			-15		15	mA
V_{IH}	High level input voltage	V_{CC} = 2.4 - 3.6V		0.7 * V_{CC}		V_{CC} + 0.5	V
		V_{CC} = 1.6 - 2.4V		0.8 * V_{CC}		V_{CC} + 0.5	
V_{IL}	Low level input voltage	V_{CC} = 2.4 - 3.6V		-0.5		0.3 * V_{CC}	
		V_{CC} = 1.6 - 2.4V		-0.5		0.2 * V_{CC}	
V_{OH}	High level output voltage	V_{CC} = 3.3V	I_{OH} = -4mA	2.6	2.9		
		V_{CC} = 3.0V	I_{OH} = -3mA	2.1	2.6		
		V_{CC} = 1.8V	I_{OH} = -1mA	1.4	1.6		
V_{OL}	Low level output voltage	V_{CC} = 3.3V	I_{OL} = 8mA		0.4	0.76	
		V_{CC} = 3.0V	I_{OL} = 5mA		0.3	0.64	
		V_{CC} = 1.8V	I_{OL} = 3mA		0.2	0.46	
I_{IN}	Input leakage current I/O pin	T = 25°C			<0.01	1	µA
R_P	Pull/buss keeper resistor				25		kΩ

Notes:
1. The sum of all I_{OH} for PORTA and PORTB must not exceed 100mA.
   The sum of all I_{OH} for PORTC, PORTD, PORTE must for each port not exceed 200mA.
   The sum of all I_{OH} for pins PF[0-5] on PORTF must not exceed 200mA.
   The sum of all I_{OL} for pins PF[6-7] on PORTF, PORTR and PDI must not exceed 100mA.
2. The sum of all I_{OL} for PORTA and PORTB must not exceed 100mA.
   The sum of all I_{OL} for PORTC, PORTD, PORTE must for each port not exceed 200mA.
   The sum of all I_{OL} for pins PF[0-5] on PORTF must not exceed 200mA.
   The sum of all I_{OL} for pins PF[6-7] on PORTF, PORTR and PDI must not exceed 100mA.

32.6.6 ADC characteristics

Table 32-152. Power supply, reference and input range.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
AV_{CC}	Analog supply voltage		V_{CC} - 0.3		V_{CC} + 0.3	V
V_{REF}	Reference voltage		1		AV_{CC} - 0.6	
R_{in}	Input resistance	Switched			4.5	kΩ
C_{in}	Input capacitance	Switched			5	pF
R_{AREF}	Reference input resistance	(leakage only)		>10		MΩ
C_{AREF}	Reference input capacitance	Static load		7		pF

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
V_{in}	Input range		0		V_{REF}	V
	Conversion range	Differential mode, Vinp - Vinn	$-V_{REF}$		V_{REF}	
	Conversion range	Single ended unsigned mode, Vinp	$-\Delta V$		$V_{REF} - \Delta V$	
ΔV	Fixed offset voltage			200		lsb

Table 32-153. Clock and timing.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
Clk_{ADC}	ADC clock frequency	Maximum is 1/4 of peripheral clock frequency	100		1800	kHz
		Measuring internal signals	100		125	
f_{ClkADC}	Sample rate		16		300	ksps
f_{ADC}	Sample rate	Current limitation (CURRLIMIT) off	16		300	
		CURRLIMIT = LOW	16		250	
		CURRLIMIT = MEDIUM	16		150	
		CURRLIMIT = HIGH	16		50	
	Sampling time	Configurable in steps of 1/2 Clk_{ADC} cycles up to 32 Clk_{ADC} cycles	0.28		320	µs
	Conversion time (latency)	(RES+1)/2 + GAIN RES (Resolution) = 8 or 12, GAIN = 0 to 3	5.5		10	Clk_{ADC} cycles
	Start-up time	ADC clock cycles		12	24	
	ADC settling time	After changing reference or input mode		7	7	

Table 32-154. Accuracy characteristics.

Symbol	Parameter	Condition [1]		Min.	Typ.	Max.	Units
RES	Resolution	12-bit resolution	Differential	8	12	12	Bits
			Single ended signed	7	11	11	
			Single ended unsigned	8	12	12	
INL [2]	Integral non-linearity	Differential mode	16ksps, V_{REF} = 3V		0.5	1	lsb
			16ksps, all V_{REF}		0.8	2	
			300ksps, V_{REF} = 3V		0.6	1	
			300ksps, all V_{REF}		1	2	
		Single ended unsigned mode	16ksps, V_{REF} = 3.0V		0.5	1	
			16ksps, all V_{REF}		1.3	2	
DNL [2]	Differential non-linearity	Differential mode	16ksps, V_{REF} = 3V		0.3	1	
			16ksps, all V_{REF}		0.5	1	
			300ksps, V_{REF} = 3V		0.35	1	
			300ksps, all V_{REF}		0.5	1	
		Single ended unsigned mode	16ksps, V_{REF} = 3.0V		0.6	1	
			16ksps, all V_{REF}		0.6	1	
	Offset error	Differential mode	300ksps, V_{REF} = 3V		-7		mV
			Temperature drift, V_{REF} = 3V		0.01		mV/K
			Operating voltage drift		0.16		mV/V
	Gain error	Differential mode	External reference		-5		mV
			AV_{CC}/1.6		-5		
			AV_{CC}/2.0		-6		
			Bandgap		±10		
			Temperature drift		0.02		mV/K
			Operating voltage drift		2		mV/V
	Gain error	Single ended unsigned mode	External reference		-8		mV
			AV_{CC}/1.6		-8		
			AV_{CC}/2.0		-8		
			Bandgap		±10		
			Temperature drift		0.03		mV/K
			Operating voltage drift		2		mV/V

Notes:
1. Unless otherwise noted all linearity, offset and gain error numbers are valid under the condition that external VREF is used.
2. Maximum numbers are based on characterisation and not tested in production, and valid for 5% to 95% input voltage range.

Table 32-155. Gain stage characteristics.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
R_{in}	Input resistance	Switched in normal mode		4.0		kΩ
C_{sample}	Input capacitance	Switched in normal mode		4.4		pF
	Signal range	Gain stage output	0		AV_{CC} - 0.6	V
	Propagation delay	ADC conversion rate	1/2	1	3	Clk_{ADC} cycles
	Clock rate	Same as ADC	100		1800	kHz
	Gain error	0.5x gain, normal mode		-1		%
		1x gain, normal mode		-1		
		8x gain, normal mode		-1		
		64x gain, normal mode		5		
	Offset error, input referred	0.5x gain, normal mode		10		mV
		1x gain, normal mode		5		
		8x gain, normal mode		-20		
		64x gain, normal mode		-126		

32.6.7 Analog comparator characteristics

Table 32-156. Analog comparator characteristics.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
V_{off}	Input offset voltage			10		mV
I_{lk}	Input leakage current			<10	50	nA
	Input voltage range		-0.1		AV_{CC}	V
	AC startup time			50		µs
V_{hys1}	Hysteresis, none	V_{CC} = 1.6V - 3.6V		0		mV
V_{hys2}	Hysteresis, small	V_{CC} = 1.6V - 3.6V		15		
V_{hys3}	Hysteresis, large	V_{CC} = 1.6V - 3.6V		30		
t_{delay}	Propagation delay	V_{CC} = 3.0V, T = 85°C		20	90	ns
		V_{CC} = 3.0V, T = 85°C		17		
	64-level voltage scaler	Integral non-linearity (INL)		0.3	0.5	lsb
	Current source accuracy after calibration			5		%
	Current source calibration range		4		6	µA

32.6.8 Bandgap and internal 1.0V reference characteristics

Table 32-157. Bandgap and internal 1.0V reference characteristics.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
	Startup time	As reference for ADC		1 Clk_{PER} + 2.5µs		µs
		As input voltage to ADC and AC		1.5		
	Bandgap voltage			1.1		V
INT1V	Internal 1.00V reference	T = 85°C, after calibration	0.99	1	1.01	
	Variation over voltage and temperature	Calibrated at T = 85°C		2		%

32.6.9 Brownout detection characteristics

Table 32-158. Brownout detection characteristics (1).

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
V_{BOT}	BOD level 0 falling V_{CC}		1.60	1.62	1.72	V
	BOD level 1 falling V_{CC}			1.9		
	BOD level 2 falling V_{CC}			2.0		
	BOD level 3 falling V_{CC}			2.2		
	BOD level 4 falling V_{CC}			2.4		
	BOD level 5 falling V_{CC}			2.6		
	BOD level 6 falling V_{CC}			2.8		
	BOD level 7 falling V_{CC}			3.0		
t_{BOD}	Detection time	Continuous mode		0.4		µs
		Sampled mode		1000		
V_{HYST}	Hysteresis			1.0		%

Note: 1. BOD is calibrated at 85°C within BOD level 0 values, and BOD level 0 is the default level.

32.6.10 External reset characteristics

Table 32-159. External reset characteristics.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
t_{EXT}	Minimum reset pulse width		1000	90		ns
V_{RST}	Reset threshold voltage	V_{CC} = 2.7 - 3.6V		0.45 * V_{CC}		V
		V_{CC} = 1.6 - 2.7V		0.42 * V_{CC}		
R_{RST}	Reset pin pull-up resistor			25		kΩ

32.6.11 Power-on reset characteristics

Table 32-160. Power-on reset characteristics.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
V_{POT-} (1)	POR threshold voltage falling V_{CC}	V_{CC} falls faster than 1V/ms	0.4	1.0		V
		V_{CC} falls at 1V/ms or slower	0.8	1.3		
V_{POT+}	POR threshold voltage rising V_{CC}			1.3	1.59	

Note: 1. V_{POT-} values are only valid when BOD is disabled. When BOD is enabled $V_{POT-} = V_{POT+}$.

32.6.12 Flash and EEPROM memory characteristics

Table 32-161. Endurance and data retention.

Symbol	Parameter	Condition		Min.	Typ.	Max.	Units
	Flash	Write/erase cycles	25°C	10K			Cycle
			85°C	10K			
		Data retention	25°C	100			Year
			55°C	25			
	EEPROM	Write/erase cycles	25°C	80K			Cycle
			85°C	30K			
		Data retention	25°C	100			Year
			55°C	25			

Table 32-162. Programming time.

Symbol	Parameter	Condition	Min.	Typ. (1)	Max.	Units
	Chip erase (2)	384KB Flash, EEPROM		130		ms
	Application erase	Section erase		6		
	Flash	Page erase		6		
		Page write		6		
		Atomic page erase and write		12		
	EEPROM	Page erase		6		
		Page write		6		
		Atomic page erase and write		12		

Notes: 1. Programming is timed from the 2MHz internal oscillator.
2. EEPROM is not erased if the EESAVE fuse is programmed.

32.6.13 Clock and oscillator characteristics

32.6.13.1 Calibrated 32.768kHz internal oscillator characteristics

Table 32-163. 32.768kHz internal oscillator characteristics.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
	Frequency			32.768		kHz
	Factory calibration accuracy	T = 85°C, V_{CC} = 3.0V	-0.5		0.5	%
	User calibration accuracy		-0.5		0.5	

32.6.13.2 Calibrated 2MHz RC internal oscillator characteristics

Table 32-164. 2MHz internal oscillator characteristics.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
	Frequency range	DFLL can tune to this frequency over voltage and temperature	1.8		2.2	MHz
	Factory calibrated frequency			2.0		
	Factory calibration accuracy	T = 85°C, V_{CC} = 3.0V	-1.5		1.5	%
	User calibration accuracy		-0.2		0.2	
	DFLL calibration stepsize			0.23		

32.6.13.3 Calibrated 32MHz internal oscillator characteristics

Table 32-165. 32MHz internal oscillator characteristics.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
	Frequency range	DFLL can tune to this frequency over voltage and temperature	30	32	35	MHz
	Factory calibrated frequency			32		
	Factory calibration accuracy	T = 85°C, V_{CC} = 3.0V	-1.5		1.5	%
	User calibration accuracy		-0.2		0.2	
	DFLL calibration step size			0.24		

32.6.13.4 32kHz internal ULP oscillator characteristics

Table 32-166. 32kHz internal ULP oscillator characteristics.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
	Factory calibrated frequency			26		kHz
	Factory calibration accuracy	T = 85°C, V_{CC} = 3.0V	-12		12	%
	Accuracy		-30		30	

32.6.13.5 Internal Phase Locked Loop (PLL) characteristics

Table 32-167. Internal PLL characteristics.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
f_{IN}	Input frequency	Output frequency must be within f_{OUT}	0.4		64	MHz
f_{OUT}	Output frequency (1)	V_{CC} = 1.6 - 1.8V	20		48	
		V_{CC} = 2.7 - 3.6V	20		128	
	Start-up time			25		µs
	Re-lock time			25		

Note: 1. The maximum output frequency vs. supply voltage is linear between 1.8V and 2.7V, and can never be higher than four times the maximum CPU frequency.

32.6.13.6 External clock characteristics

Figure 32-38. External clock drive waveform.

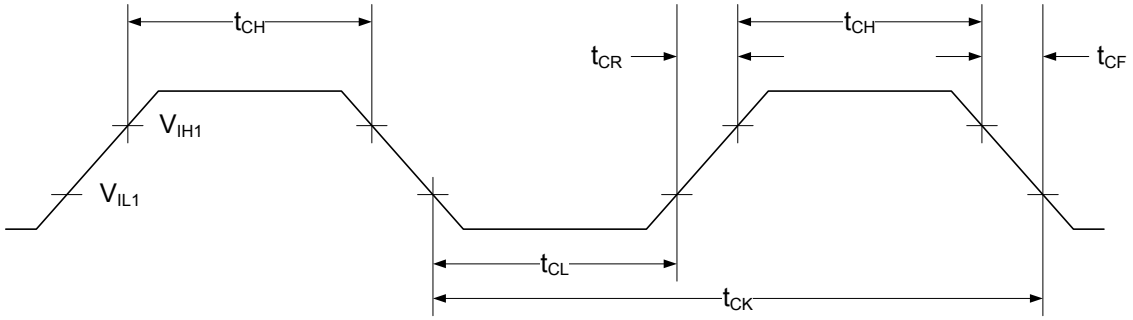


Table 32-168.External clock used as system clock without prescaling.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
$1/t_{CK}$	Clock Frequency (1)	V_{CC} = 1.6 - 1.8V	0		12	MHz
		V_{CC} = 2.7 - 3.6V	0		32	
t_{CK}	Clock Period	V_{CC} = 1.6 - 1.8V	83.3			ns
		V_{CC} = 2.7 - 3.6V	31.5			
t_{CH}	Clock High Time	V_{CC} = 1.6 - 1.8V	30.0			ns
		V_{CC} = 2.7 - 3.6V	12.5			
t_{CL}	Clock Low Time	V_{CC} = 1.6 - 1.8V	30.0			ns
		V_{CC} = 2.7 - 3.6V	12.5			
t_{CR}	Rise Time (for maximum frequency)	V_{CC} = 1.6 - 1.8V			10	ns
		V_{CC} = 2.7 - 3.6V			3	
t_{CF}	Fall Time (for maximum frequency)	V_{CC} = 1.6 - 1.8V			10	ns
		V_{CC} = 2.7 - 3.6V			3	
Δt_{CK}	Change in period from one clock cycle to the next				10	%

Note: 1. The maximum frequency vs. supply voltage is linear between 1.6V and 2.7V, and the same applies for all other parameters with supply voltage conditions.

Table 32-169.External clock with prescaler (1) for system clock.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
$1/t_{CK}$	Clock Frequency (2)	V_{CC} = 1.6 - 1.8V	0		90	MHz
		V_{CC} = 2.7 - 3.6V	0		142	
t_{CK}	Clock Period	V_{CC} = 1.6 - 1.8V	11			ns
		V_{CC} = 2.7 - 3.6V	7			
t_{CH}	Clock High Time	V_{CC} = 1.6 - 1.8V	4.5			ns
		V_{CC} = 2.7 - 3.6V	2.4			
t_{CL}	Clock Low Time	V_{CC} = 1.6 - 1.8V	4.5			ns
		V_{CC} = 2.7 - 3.6V	2.4			
t_{CR}	Rise Time (for maximum frequency)	V_{CC} = 1.6 - 1.8V			1.5	ns
		V_{CC} = 2.7 - 3.6V			1.0	
t_{CF}	Fall Time (for maximum frequency)	V_{CC} = 1.6 - 1.8V			1.5	ns
		V_{CC} = 2.7 - 3.6V			1.0	
Δt_{CK}	Change in period from one clock cycle to the next				10	%

Notes: 1. System Clock Prescalers must be set so that maximum CPU clock frequency for device is not exceeded.
2. The maximum frequency vs. supply voltage is linear between 1.6V and 2.7V, and the same applies for all other parameters with supply voltage conditions.

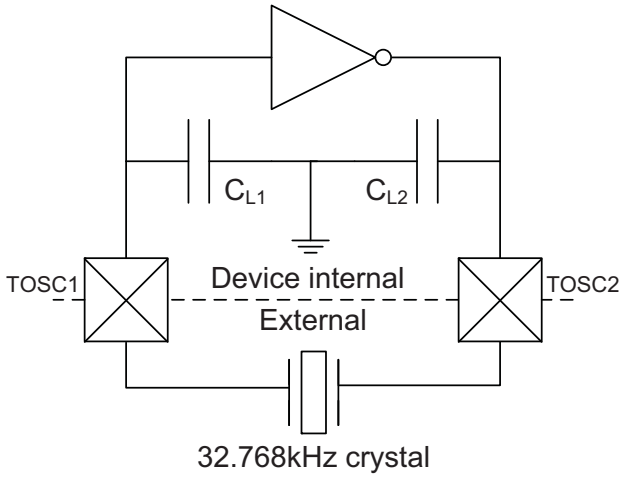
32.6.13.7 External 32.768kHz crystal oscillator and TOSC characteristics

Table 32-170. External 32.768kHz crystal oscillator and TOSC characteristics.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
ESR/R1	Recommended crystal equivalent series resistance (ESR)	Crystal load capacitance 6.5pF			60	kΩ
		Crystal load capacitance 9.0pF			35	
		Crystal load capacitance 12pF			28	
C_{TOSC1}	Parasitic capacitance TOSC1 pin			3.5		pF
C_{TOSC2}	Parasitic capacitance TOSC2 pin			3.5		
	Recommended safety factor	Capacitance load matched to crystal specification	3			

Note: See Figure 32-39 for definition.

Figure 32-39. TOSC input capacitance.



The parasitic capacitance between the TOSC pins is C_{L1} + C_{L2} in series as seen from the crystal when oscillating without external capacitors.

32.6.14 SPI characteristics

Figure 32-40. SPI timing requirements in master mode.

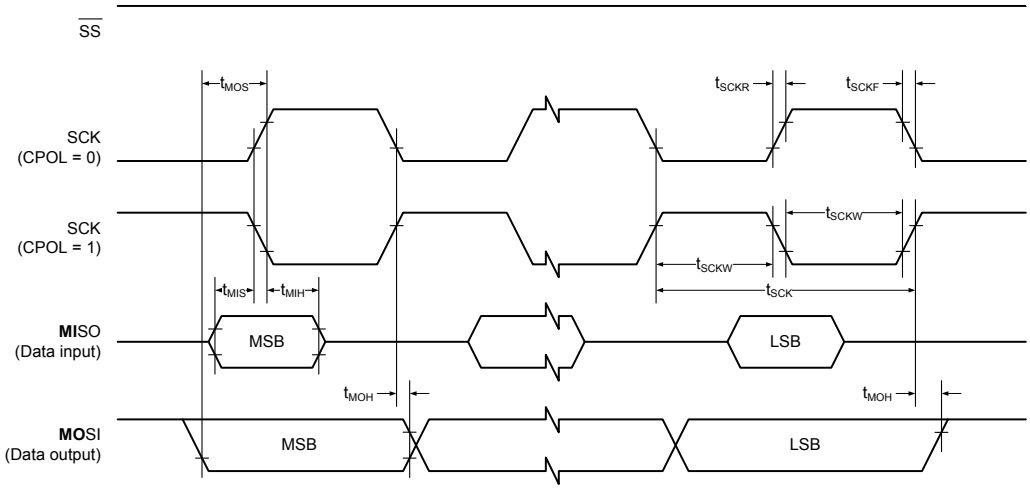


Figure 32-41. SPI timing requirements in slave mode.

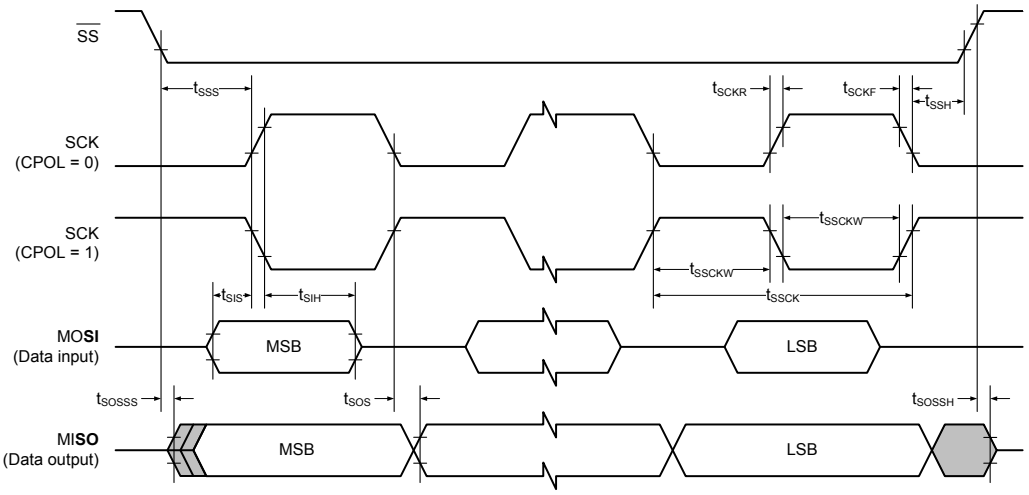


Table 32-171. SPI timing characteristics and requirements.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
t_{SCK}	SCK period	Master		(See Table 20-3 in XMEGA D manual)		ns
t_{SCKW}	SCK high/low width	Master		0.5 * SCK		
t_{SCKR}	SCK rise time	Master		2.7		
t_{SCKF}	SCK fall time	Master		2.7		
t_{MIS}	MISO setup to SCK	Master		10		
t_{MIH}	MISO hold after SCK	Master		10		
t_{MOS}	MOSI setup SCK	Master		0.5 * SCK		
t_{MOH}	MOSI hold after SCK	Master		1		
t_{SSCK}	Slave SCK Period	Slave	4 * t Clk_{PER}			
t_{SSCKW}	SCK high/low width	Slave	2 * t Clk_{PER}			
t_{SSCKR}	SCK rise time	Slave			1600	
t_{SSCKF}	SCK fall time	Slave			1600	
t_{SIS}	MOSI setup to SCK	Slave	3			
t_{SIH}	MOSI hold after SCK	Slave	t Clk_{PER}			
t_{SSS}	$\overline{SS}$ setup to SCK	Slave	21			
t_{SSH}	$\overline{SS}$ hold after SCK	Slave	20			
t_{SOS}	MISO setup SCK	Slave		8		
t_{SOH}	MISO hold after SCK	Slave		13		
t_{SOSS}	MISO setup after $\overline{SS}$ low	Slave		11		
t_{SOSH}	MISO hold after $\overline{SS}$ high	Slave		8		

32.6.15 Two-wire interface characteristics

Table 32-172 on page 172 describes the requirements for devices connected to the Two-Wire Interface Bus. The Atmel AVR XMEGA Two-Wire Interface meets or exceeds these requirements under the noted conditions. Timing symbols refer to Figure 32-42.

Figure 32-42. Two-wire interface bus timing.

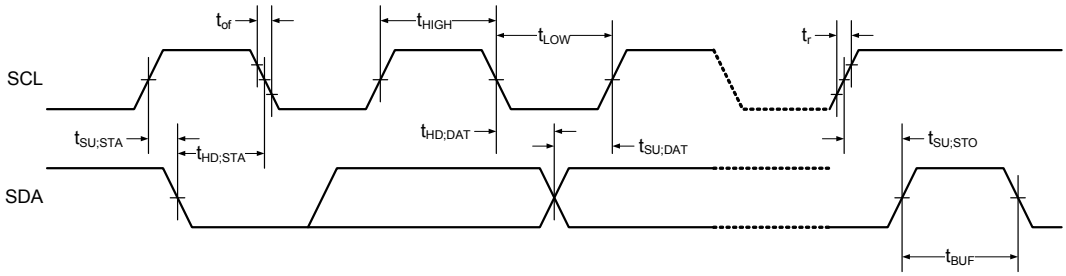


Table 32-172. Two-wire interface characteristics.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
V_{IH}	Input high voltage		$0.7V_{CC}$		V_{CC} + 0.5	V
V_{IL}	Input low voltage		-0.5		$0.3V_{CC}$	
V_{hys}	Hysteresis of Schmitt trigger inputs		$0.05V_{CC}$ (1)			
V_{OL}	Output low voltage	3mA, sink current	0		0.4	
t_r	Rise time for both SDA and SCL		$20 + 0.1C_b$ (1)(2)		300	ns
t_{of}	Output fall time from V_{IHmin} to V_{ILmax}	$10pF < C_b < 400pF$ (2)	$20 + 0.1C_b$ (1)(2)		250	
t_{SP}	Spikes suppressed by input filter		0		50	
I_I	Input current for each I/O pin	$0.1V_{CC} < V_I < 0.9V_{CC}$	-10		10	µA
C_I	Capacitance for each I/O pin				10	pF
f_{SCL}	SCL clock frequency	f_{PER} (3) > max($10f_{SCL}$, 250kHz)	0		400	kHz
R_P	Value of pull-up resistor	$f_{SCL} \leq 100kHz$	$\frac{V_{CC} - 0.4V}{3mA}$		$\frac{100ns}{C_b}$	Ω
		$f_{SCL} > 100kHz$			$\frac{300ns}{C_b}$	
$t_{HD;STA}$	Hold time (repeated) START condition	$f_{SCL} \leq 100kHz$	4.0			µs
		$f_{SCL} > 100kHz$	0.6			
t_{LOW}	Low period of SCL clock	$f_{SCL} \leq 100kHz$	4.7			
		$f_{SCL} > 100kHz$	1.3			
t_{HIGH}	High period of SCL clock	$f_{SCL} \leq 100kHz$	4.0			
		$f_{SCL} > 100kHz$	0.6			
$t_{SU;STA}$	Set-up time for a repeated START condition	$f_{SCL} \leq 100kHz$	4.7			
		$f_{SCL} > 100kHz$	0.6			

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
$t_{HD;DAT}$	Data hold time	$f_{SCL} \leq 100kHz$	0		3.45	µs
		$f_{SCL} > 100kHz$	0		0.9	
$t_{SU;DAT}$	Data setup time	$f_{SCL} \leq 100kHz$	250			
		$f_{SCL} > 100kHz$	100			
$t_{SU;STO}$	Setup time for STOP condition	$f_{SCL} \leq 100kHz$	4.0			
		$f_{SCL} > 100kHz$	0.6			
t_{BUF}	Bus free time between a STOP and START condition	$f_{SCL} \leq 100kHz$	4.7			
		$f_{SCL} > 100kHz$	1.3			

Notes:
1. Required only for $f_{SCL} > 100kHz$.
2. C_b = Capacitance of one bus line in pF.
3. f_{PER} = Peripheral clock frequency.

33. Typical characteristics

33.1 Atmel ATxmega32D3

33.1.1 Active supply current

Figure 33-1. Active supply current vs. frequency.
f_{SYS} = 0 - 1MHz external clock, T = 25°C.

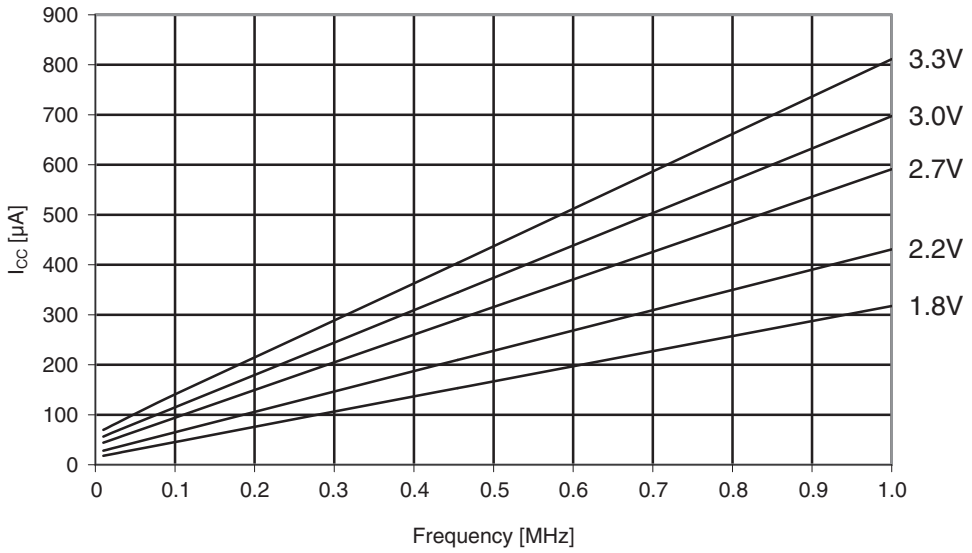


Figure 33-2. Active supply current vs. frequency.
f_{SYS} = 1 - 32MHz external clock, T = 25°C.

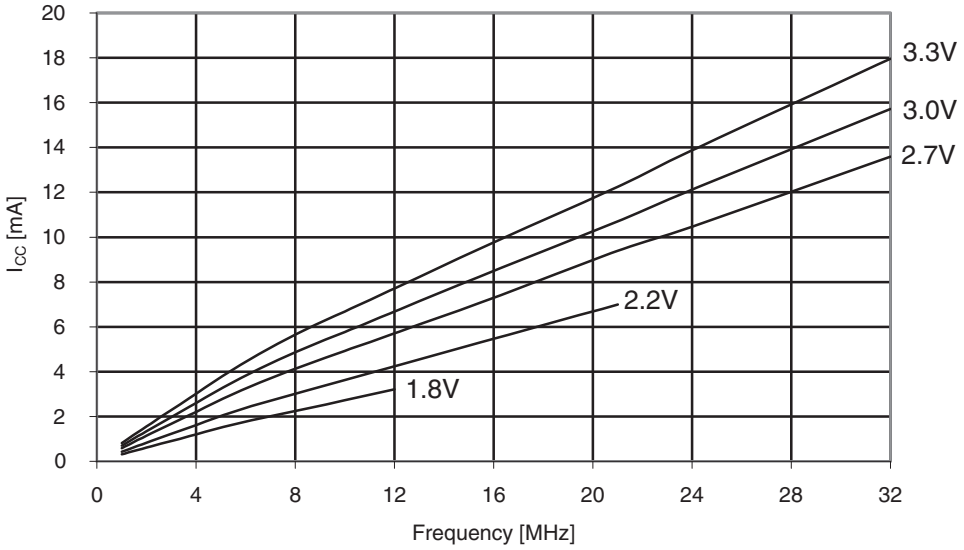


Figure 33-3. Active supply current vs. V_{CC}.

f_{SYS} = 1.0MHz external clock.

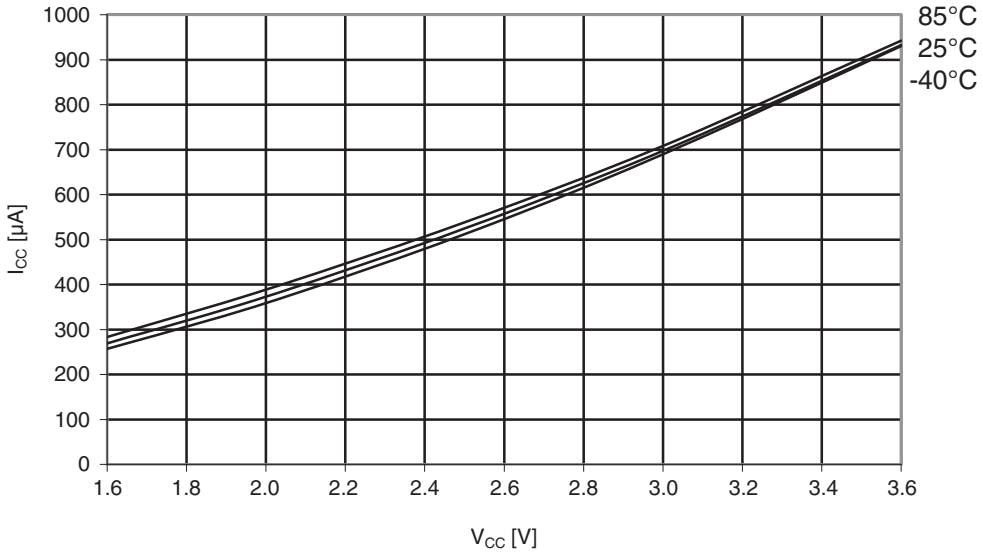


Figure 33-4. Active supply current vs. V_{CC}.

f_{SYS} = 32.768kHz internal RC.

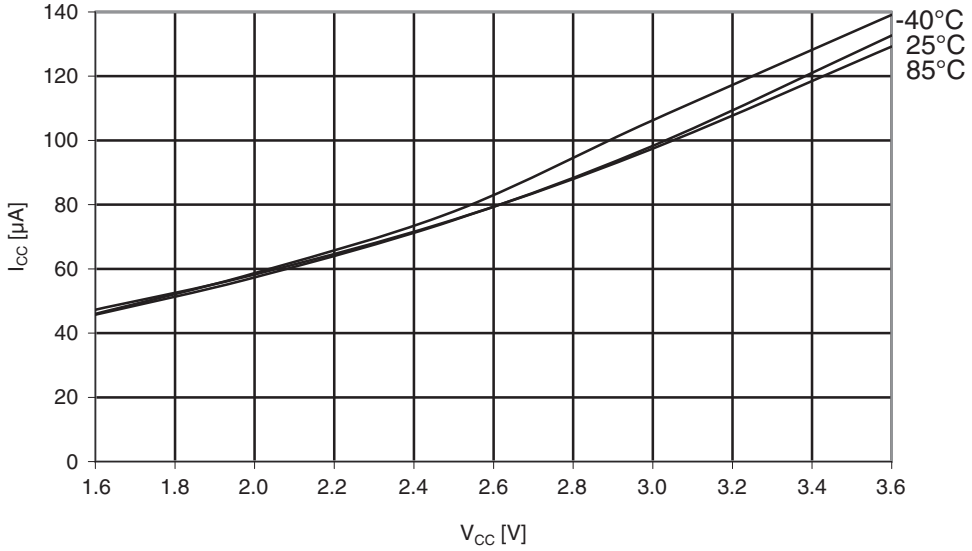


Figure 33-5. Active supply current vs. V_{CC}.

f_{SYS} = 2.0MHz internal RC.

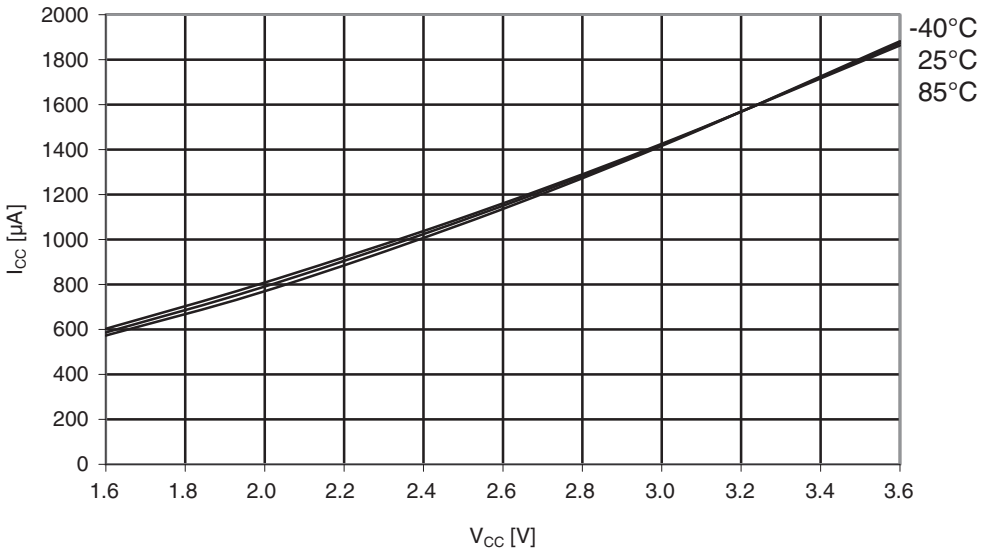


Figure 33-6. Active supply current vs. V_{CC}.

f_{SYS} = 32MHz internal RC prescaled to 8MHz.

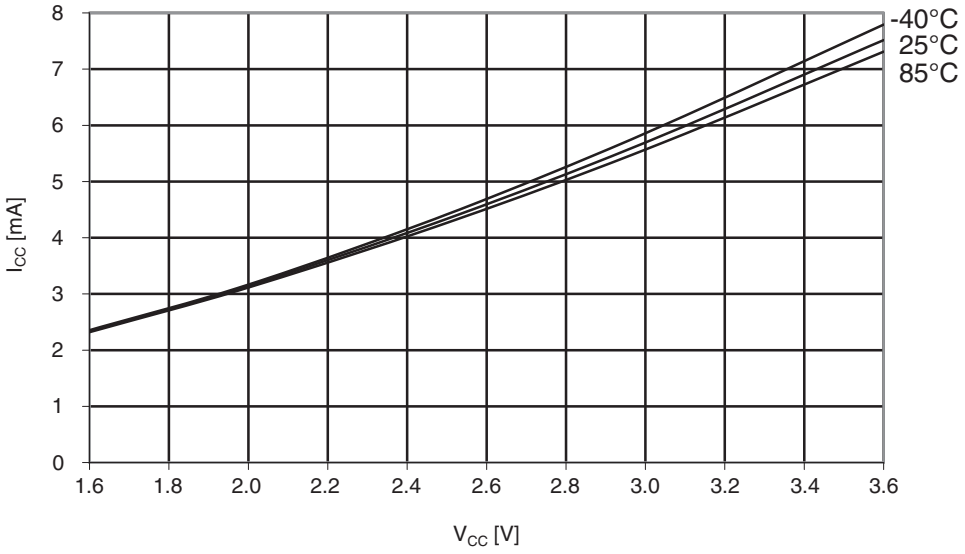
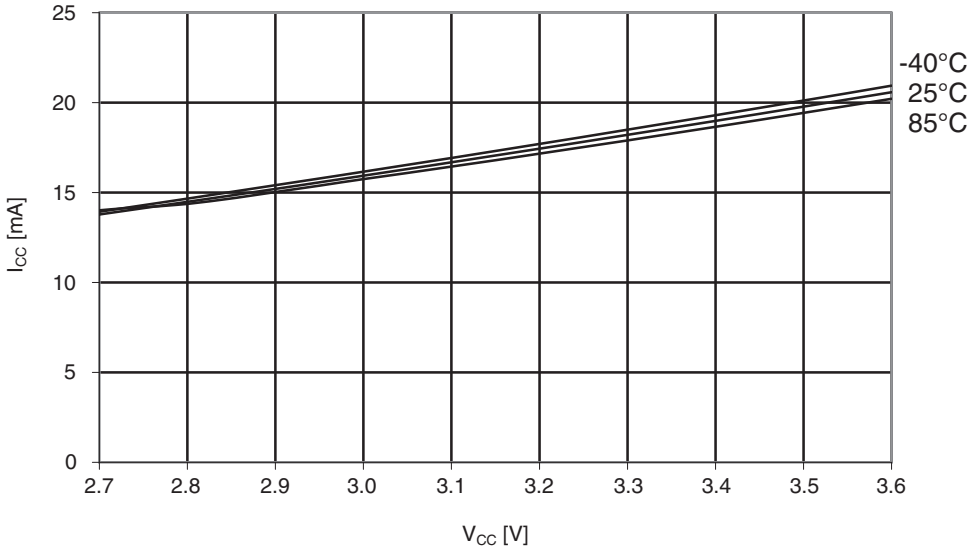


Figure 33-7. Active supply current vs. V_{CC}.

f_{SYS} = 32MHz internal RC.



33.1.2 Idle supply current

Figure 33-8. Idle supply current vs. frequency.

f_{SYS} = 0 - 1.0MHz, T = 25°C.

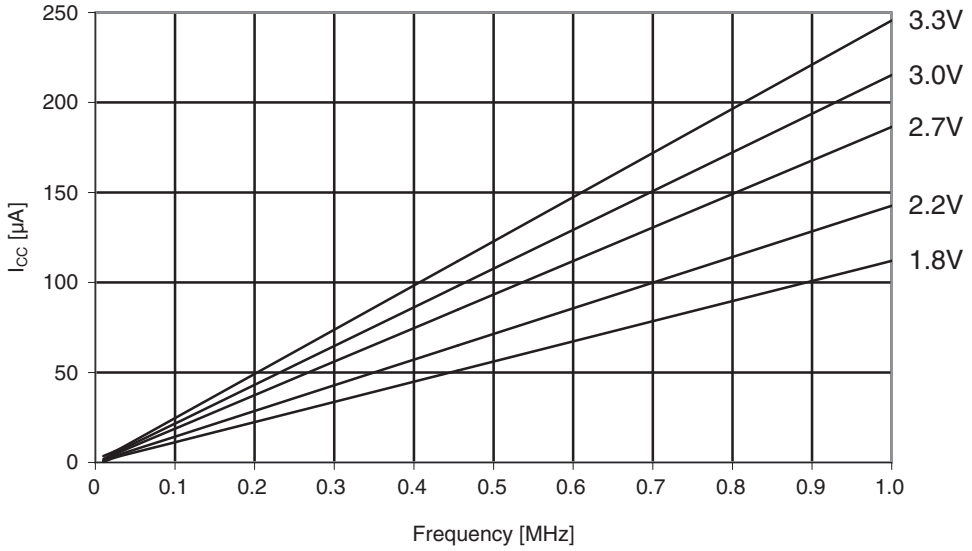


Figure 33-9. Idle supply current vs. frequency.

f_{SYS} = 1 - 32MHz, T = 25°C.

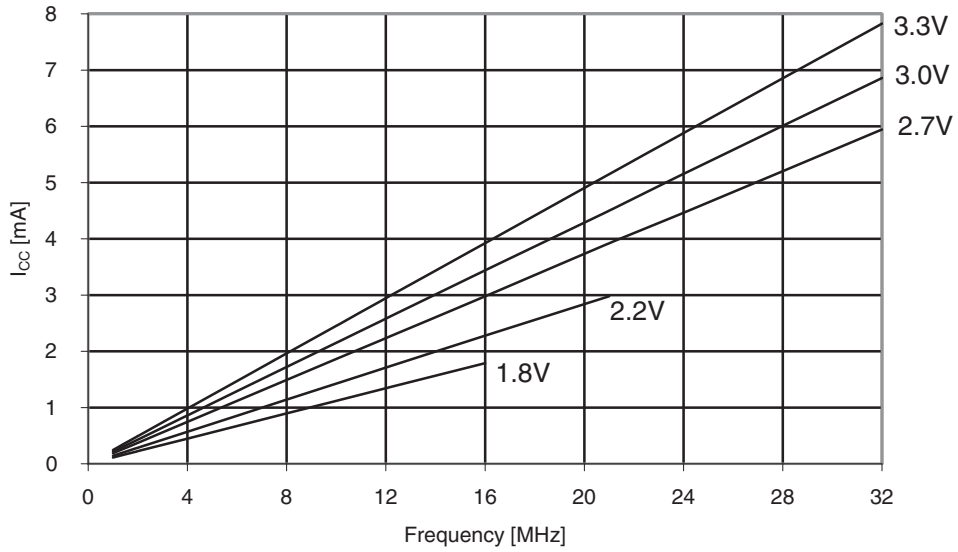


Figure 33-10. Idle supply current vs. V_{CC}.

f_{SYS} = 1.0MHz external clock.

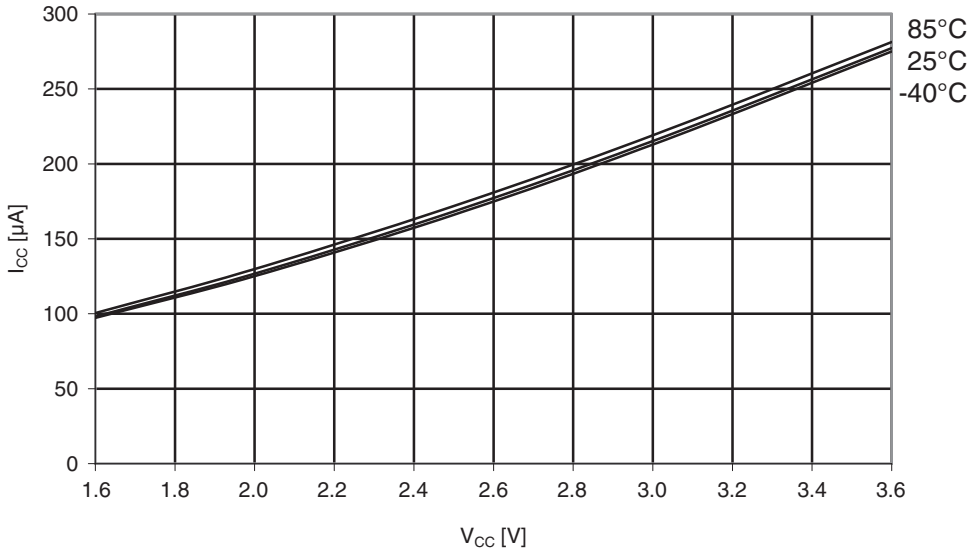


Figure 33-11. Idle supply current vs. V_{CC}.
f_{SYS} = 32.768kHz internal RC.

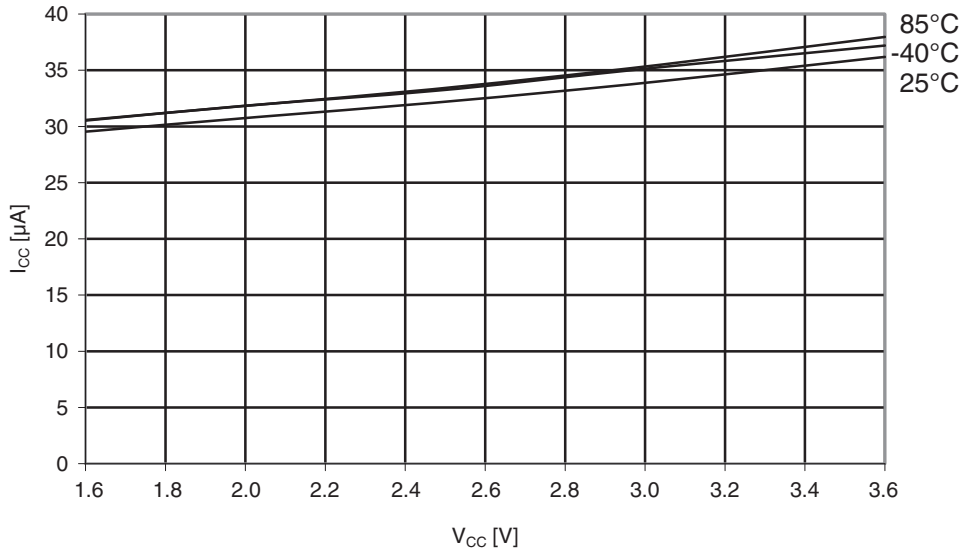


Figure 33-12. Idle supply current vs. V_{CC}.
f_{SYS} = 2.0MHz internal RC.

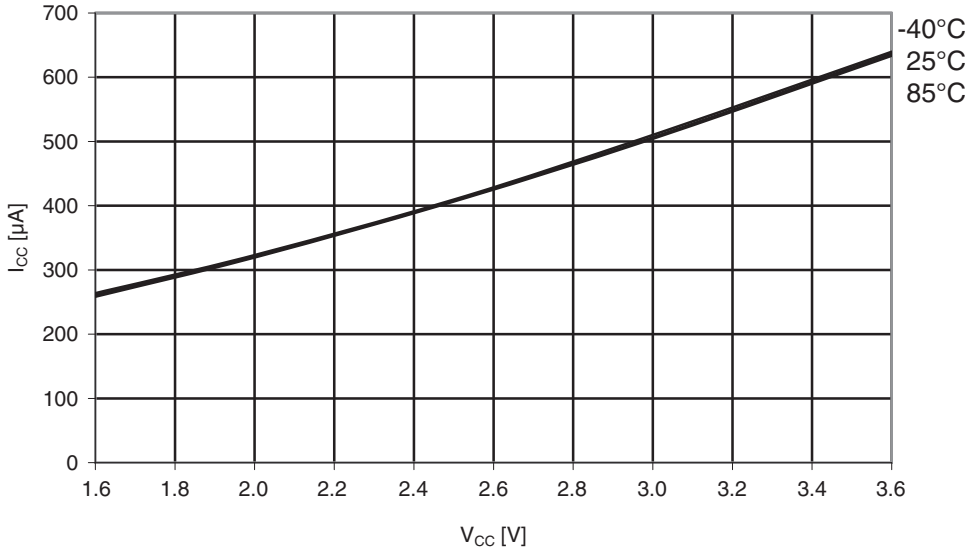


Figure 33-13. Idle supply current vs. V_{CC}.
f_{SYS} = 32MHz internal RC prescaled to 8MHz.

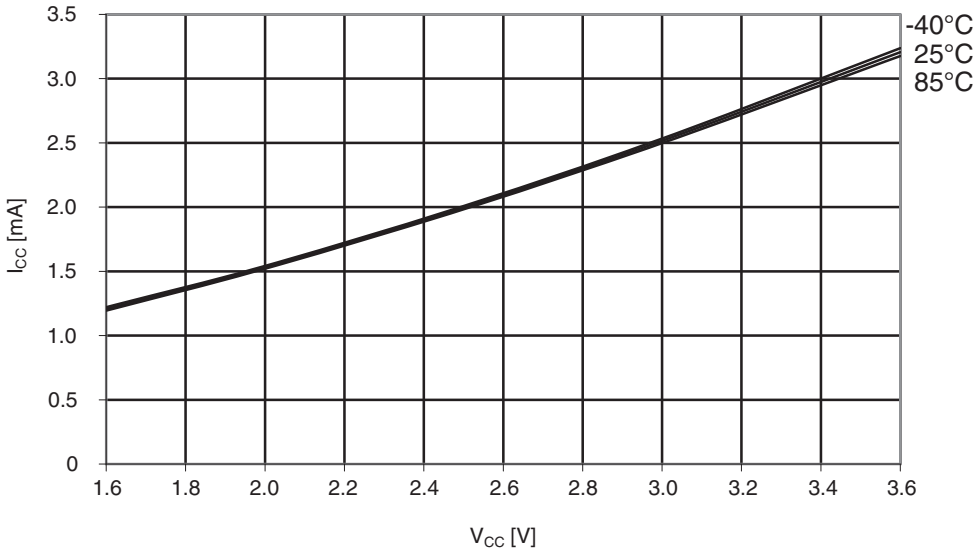
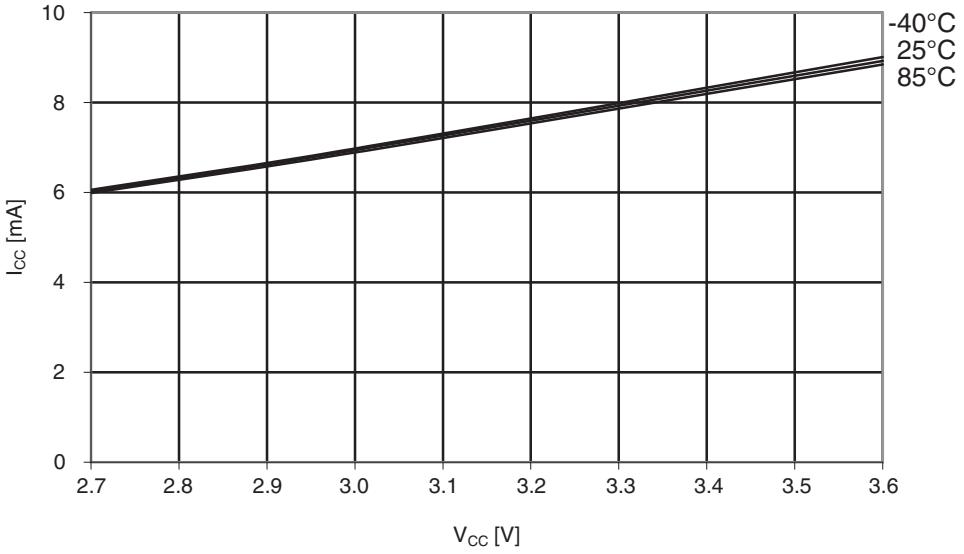


Figure 33-14. Idle supply current vs. V_{CC}.
f_{SYS} = 32MHz internal RC.



33.1.3 Power-down supply current

Figure 33-15. Power-down supply current vs. temperature.

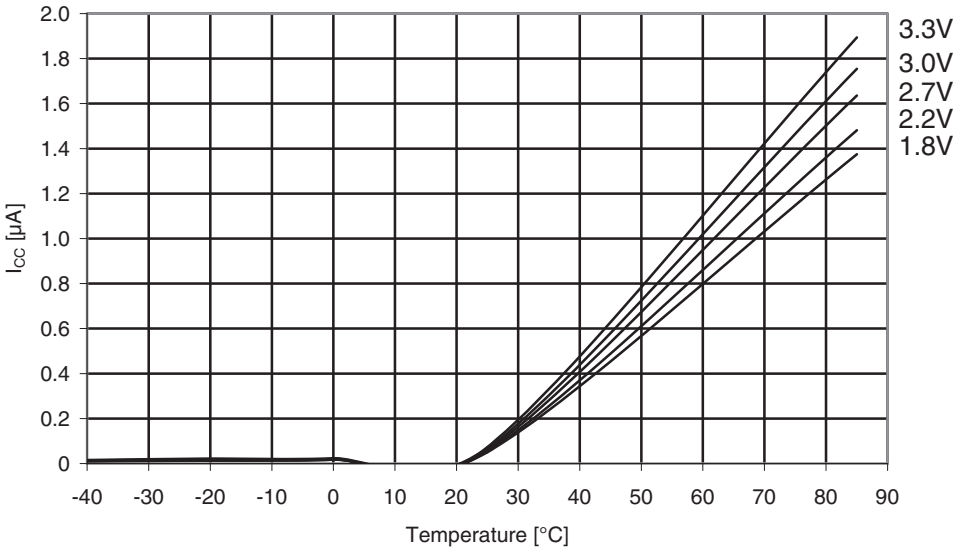
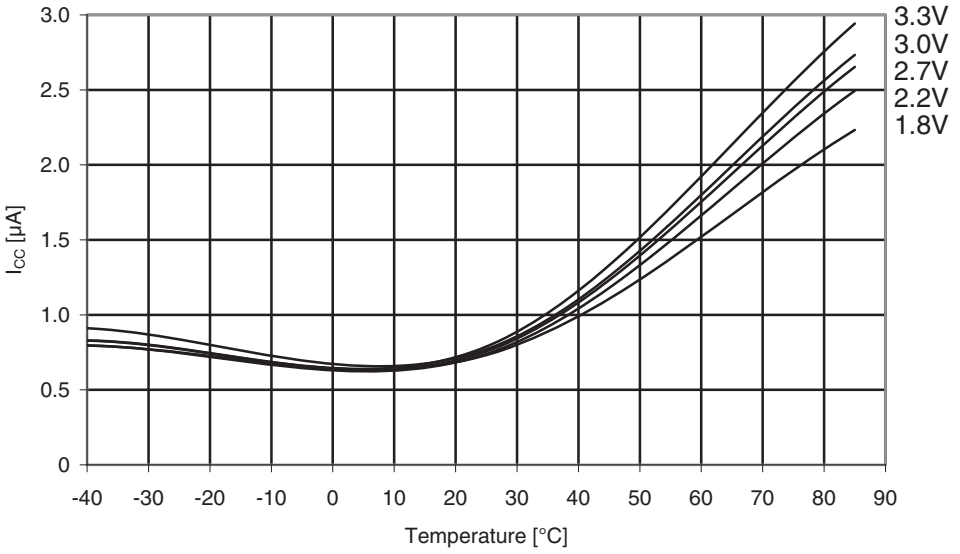
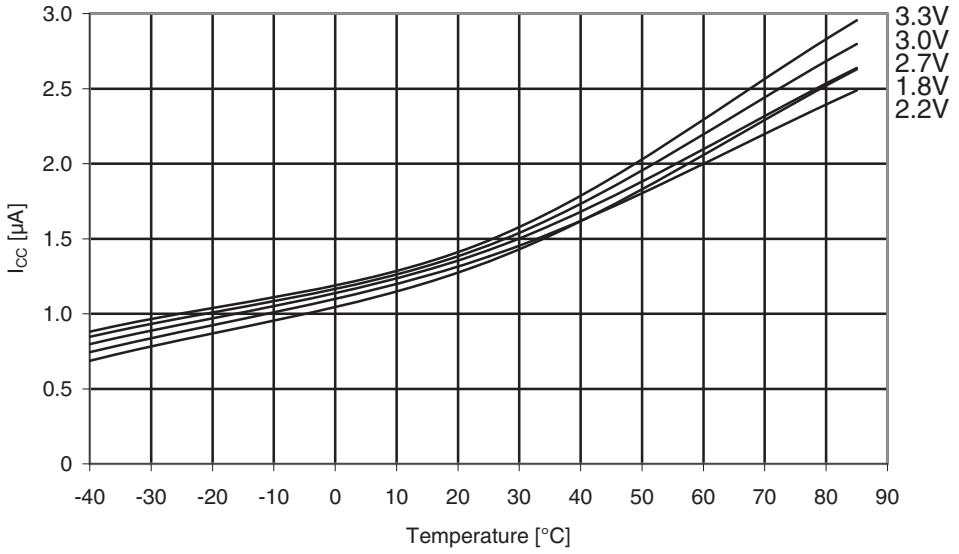


Figure 33-16. Power-down supply current vs. temperature.
With WDT and sampled BOD enabled.



33.1.4 Power-save supply current

Figure 33-17. Power-save supply current vs. temperature.
With WDT, sampled BOD, and RTC from ULP enabled.



33.1.5 Pin pull-up

Figure 33-18. Reset pull-up resistor current vs. reset pin voltage.
V_{CC} = 1.8V.

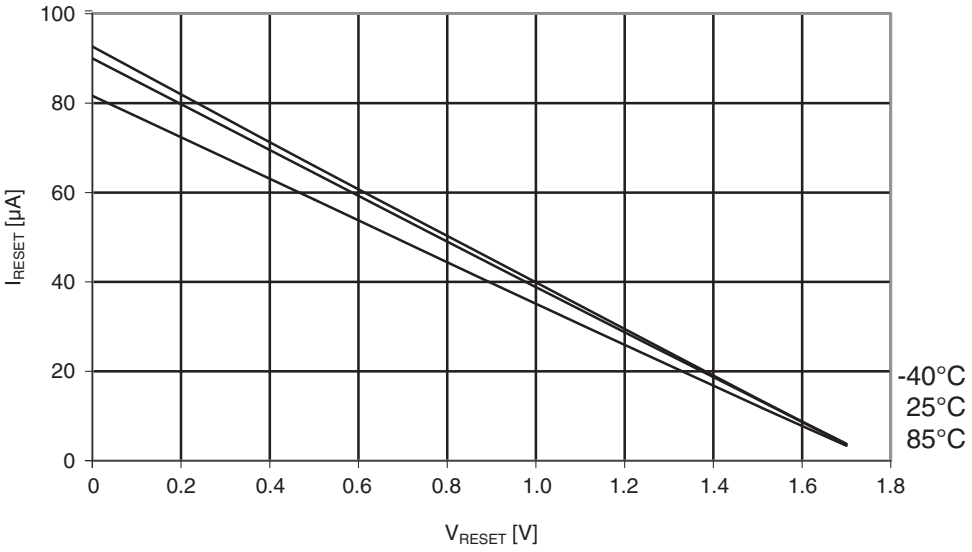


Figure 33-19. Reset pull-up resistor current vs. reset pin voltage.
V_{CC} = 3.0V.

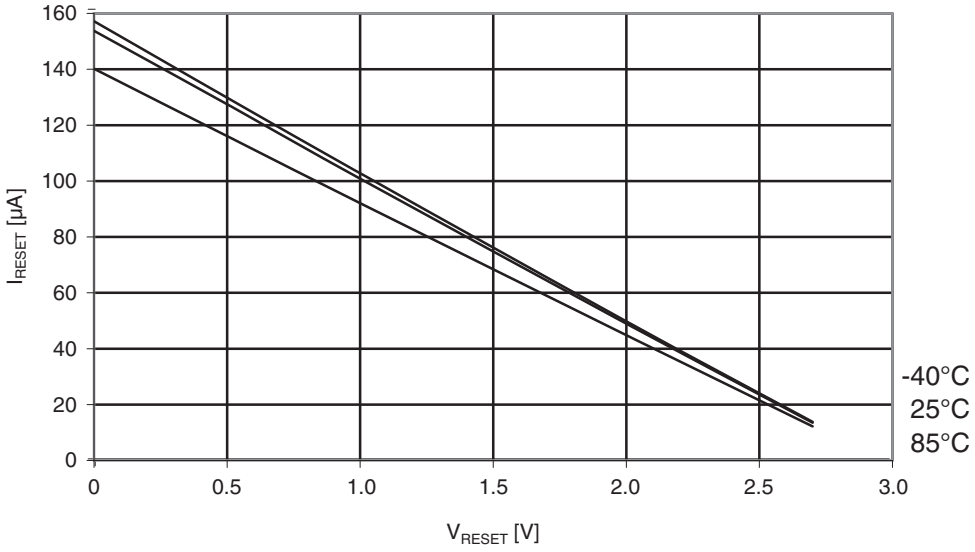
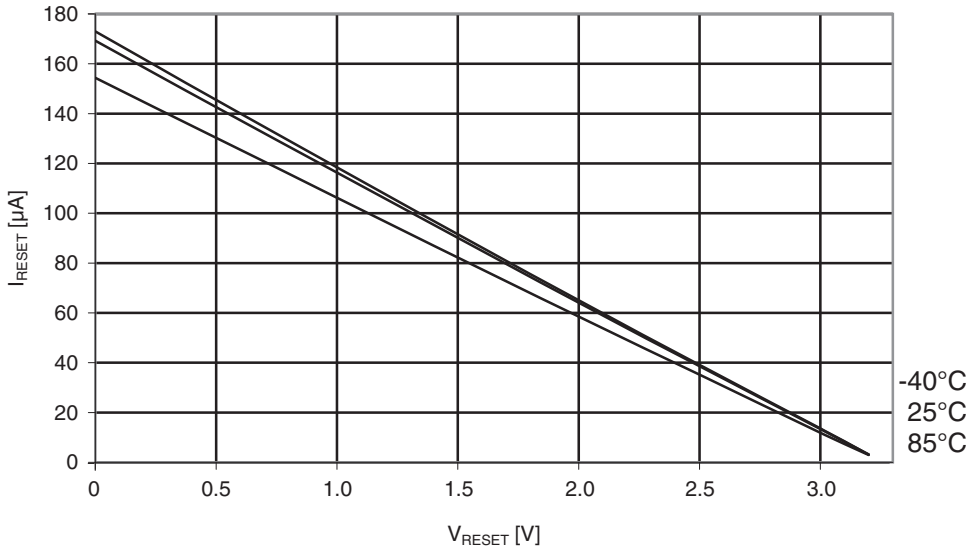


Figure 33-20. Reset pull-up resistor current vs. reset pin voltage.
V_{CC} = 3.3V.



33.1.6 Pin output voltage vs. sink/source current

Figure 33-21. I/O pin output voltage vs. source current.
V_{CC} = 1.8V.

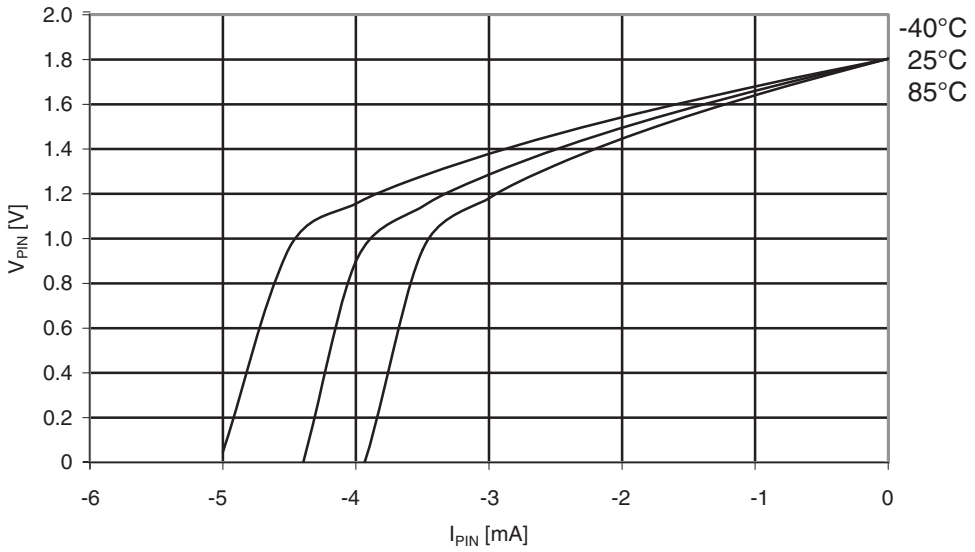


Figure 33-22. I/O pin output voltage vs. source current.
V_{CC} = 3.0V.

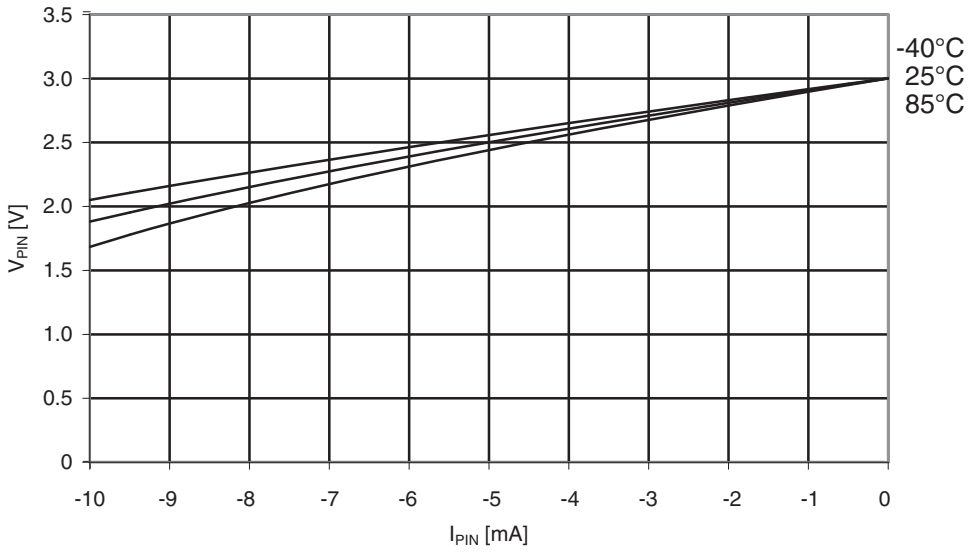


Figure 33-23. I/O pin output voltage vs. source current.
V_{CC} = 3.3V.

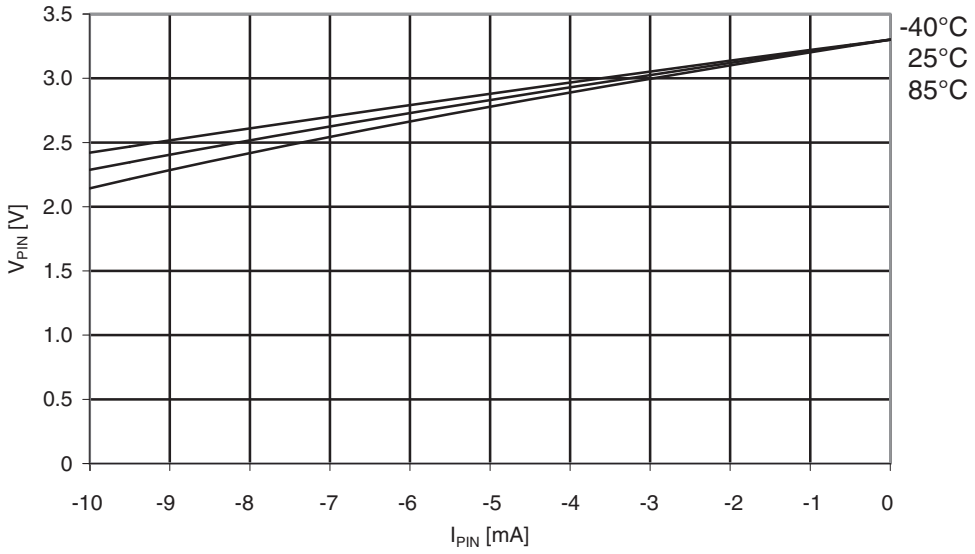


Figure 33-24. I/O pin output voltage vs. sink current.
V_{CC} = 1.8V.

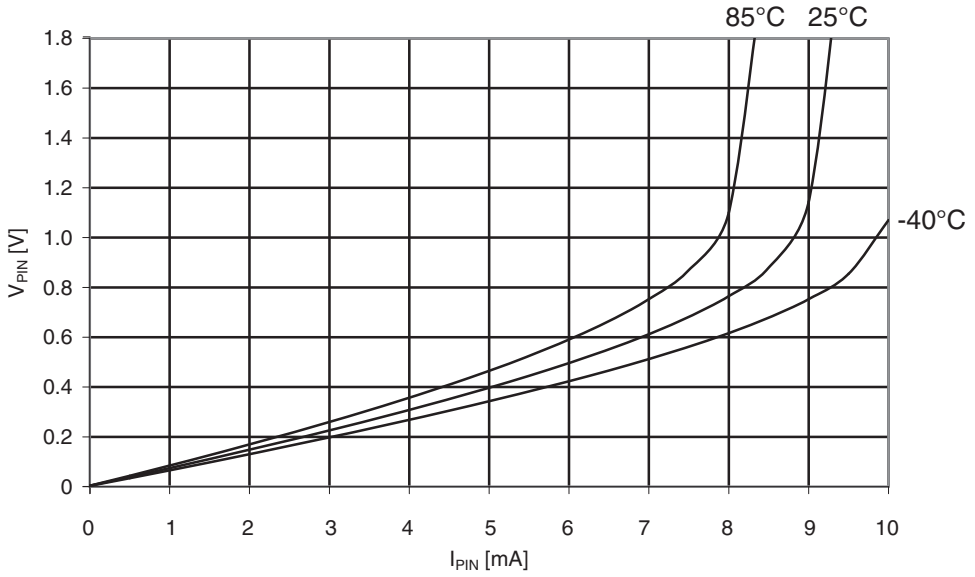


Figure 33-25. I/O pin output voltage vs. sink current.
V_{CC} = 3.0V.

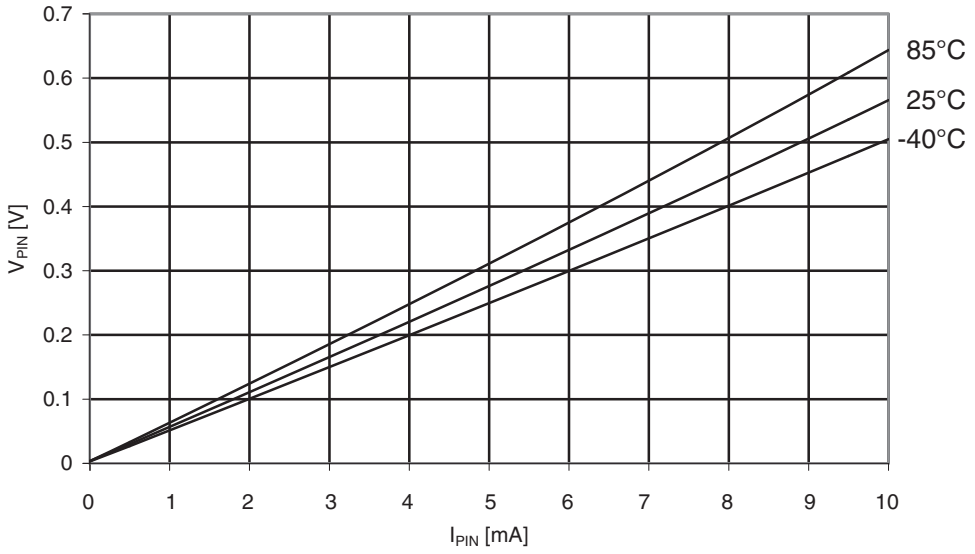
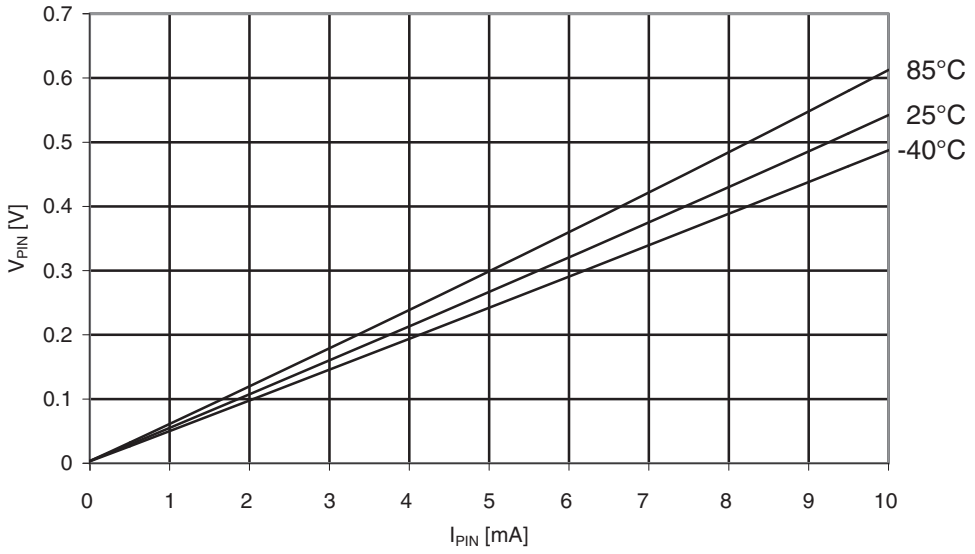


Figure 33-26. I/O pin output voltage vs. sink current.
V_{CC} = 3.3V.



33.1.7 Thresholds and hysteresis

Figure 33-27. I/O pin input threshold voltage vs. V_{CC}.
V_{IH} - I/O pin read as "1".

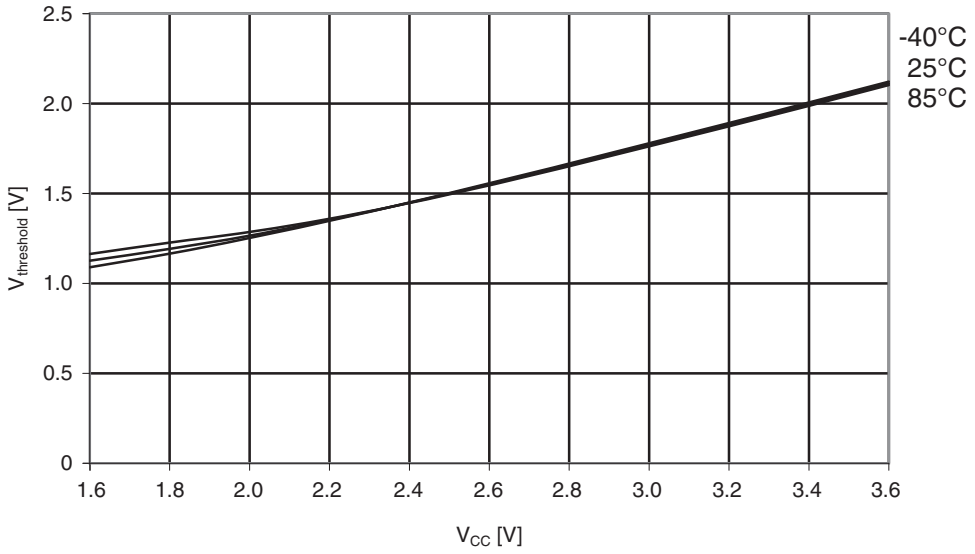


Figure 33-28. I/O pin input threshold voltage vs. V_{CC}.
V_{IL} - I/O pin read as "0".

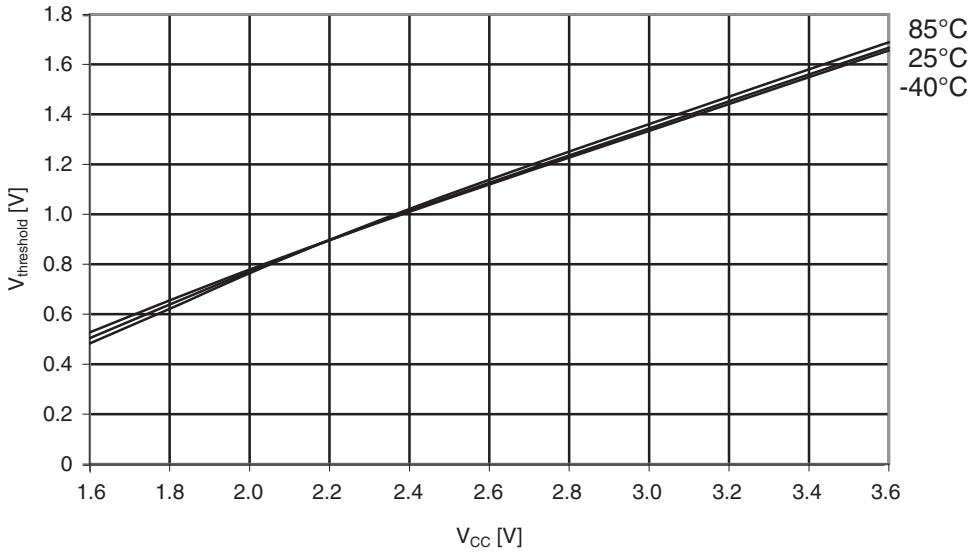


Figure 33-29. I/O pin input hysteresis vs. V_{CC}.

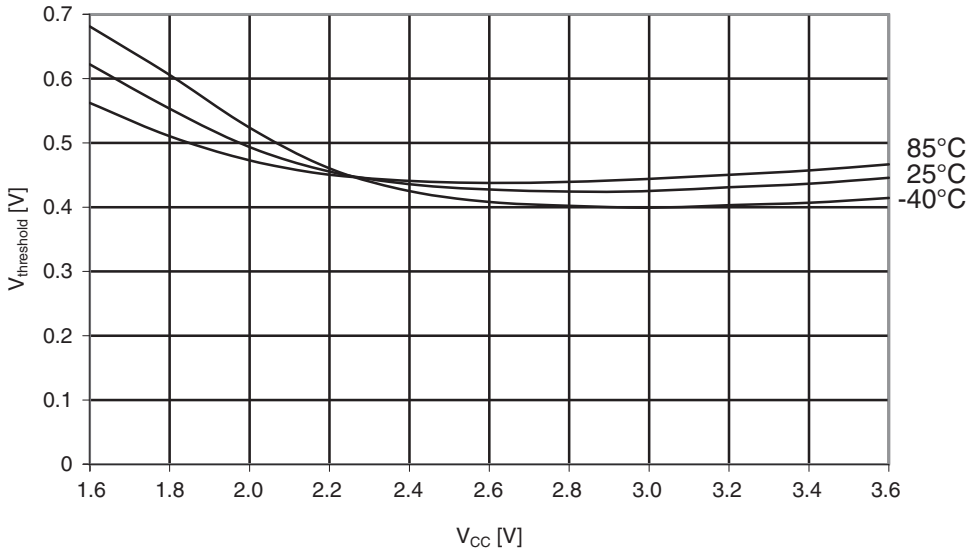


Figure 33-30. Reset input threshold voltage vs. V_{CC}.
V_{IL} - I/O pin read as "1".

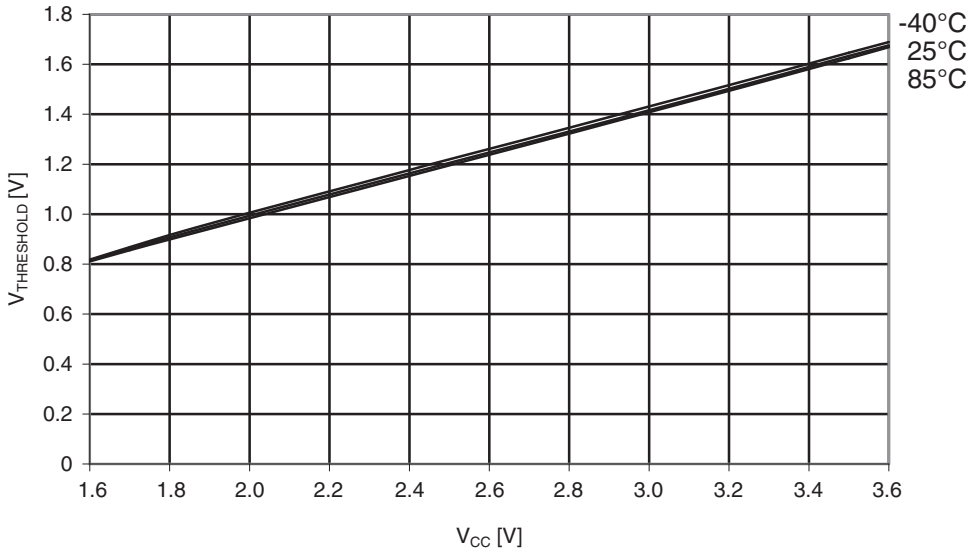
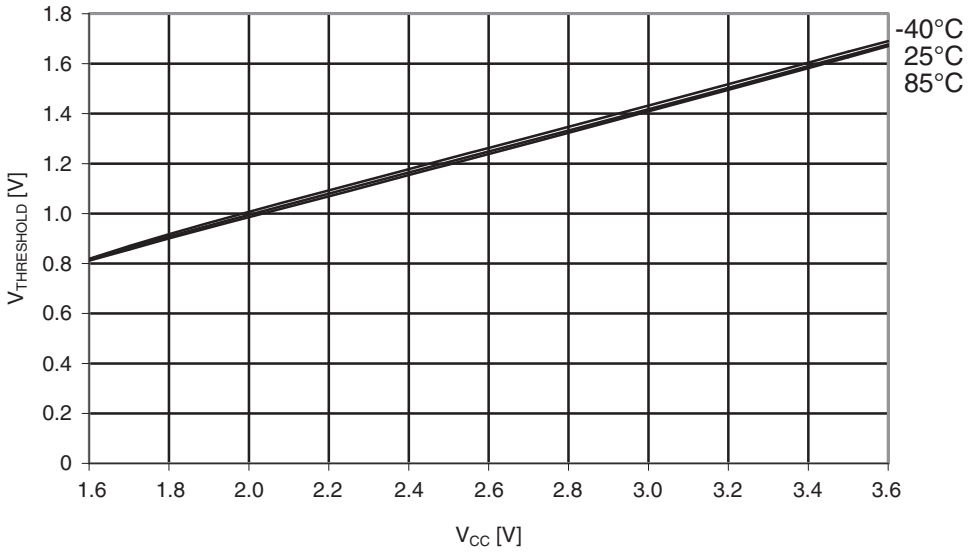


Figure 33-31. Reset input threshold voltage vs. V_{CC}.
V_{IL} - I/O pin read as "0".



33.1.8 BOD thresholds

Figure 33-32. BOD thresholds vs. temperature.
BOD level = 1.6V.

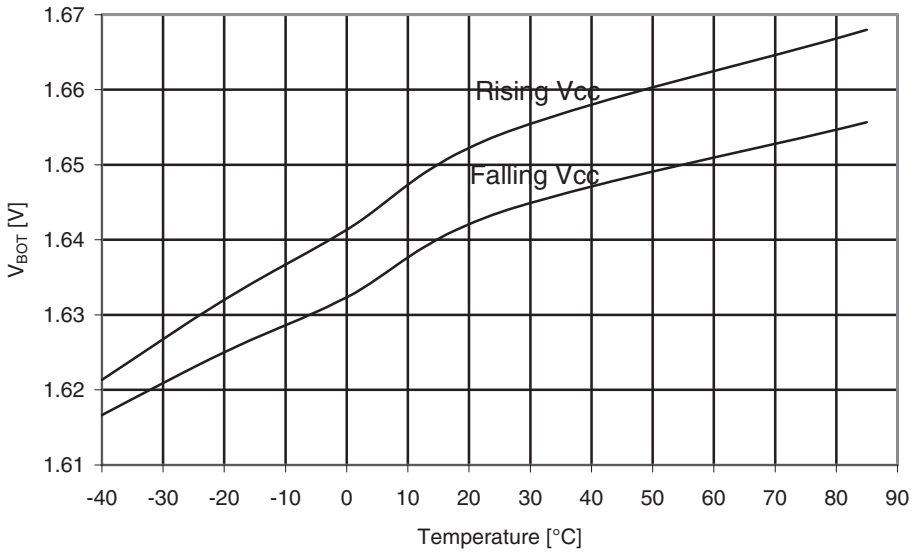
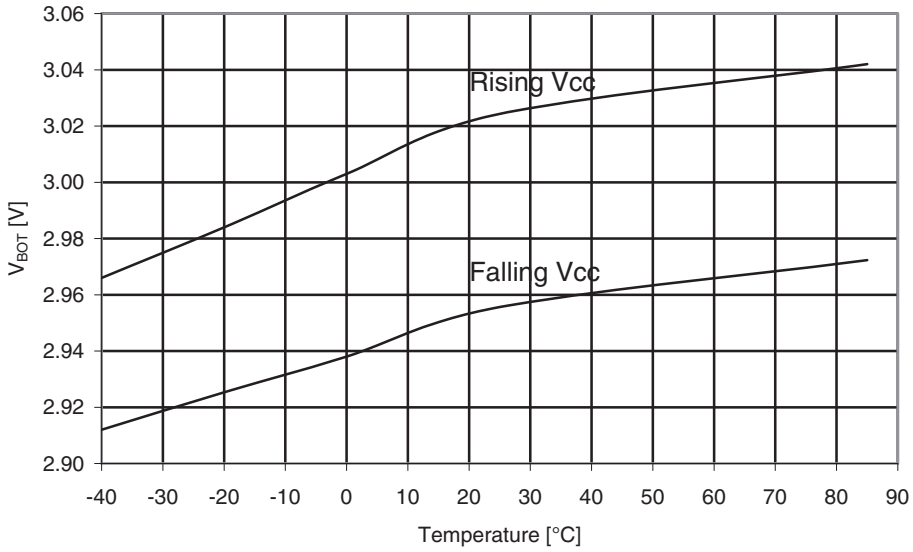


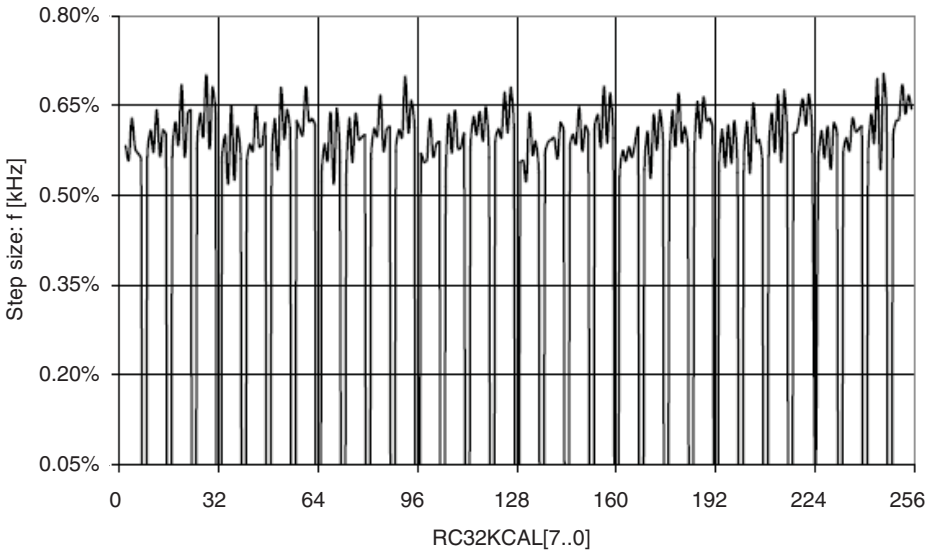
Figure 33-33. BOD thresholds vs. temperature.
BOD level = 2.9V.



33.1.9 Oscillators and wake-up time

33.1.9.1 Internal 32.768kHz oscillator

Figure 33-34. Internal 32.768kHz oscillator calibration step size.
T = -40 to 85°C, V_{CC} = 3V.



33.1.9.2 Internal 2MHz oscillator

Figure 33-35. Internal 2MHz oscillator CALA calibration step size.
T = -40 to 85°C, V_{CC} = 3V.

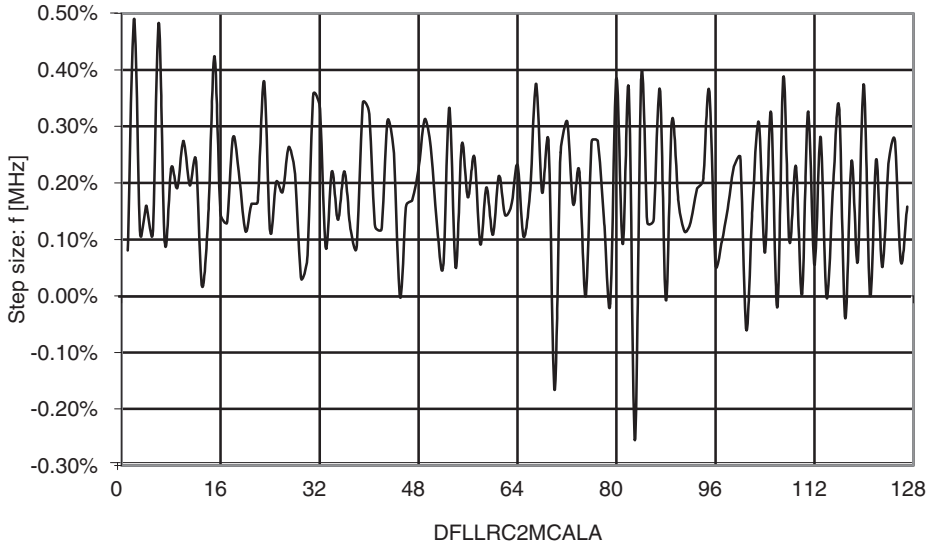
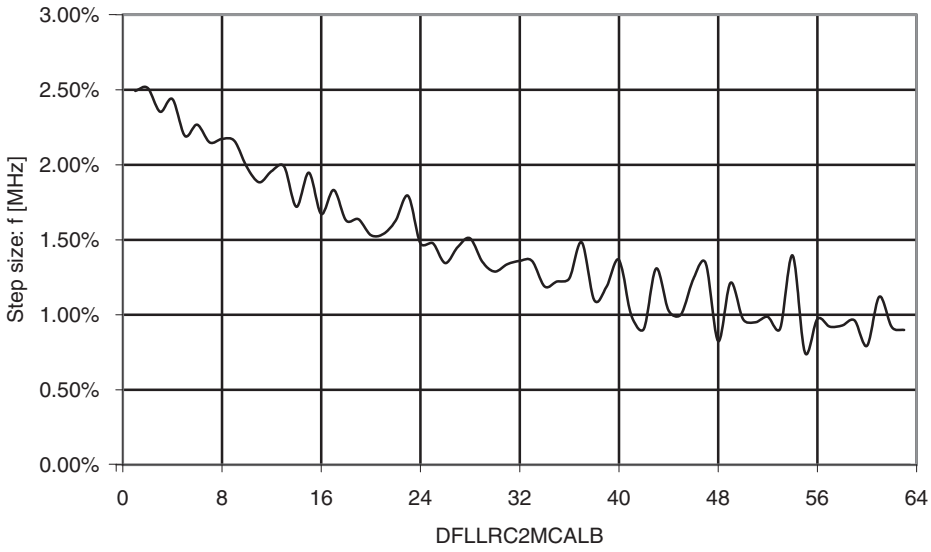


Figure 33-36. Internal 2MHz oscillator CALB calibration step size.
T = -40 to 85°C, V_{CC} = 3V.



33.1.9.3 Internal 32MHz oscillator

Figure 33-37. Internal 32MHz oscillator CALA calibration step size.
T = -40 to 85°C, V_{CC} = 3V.

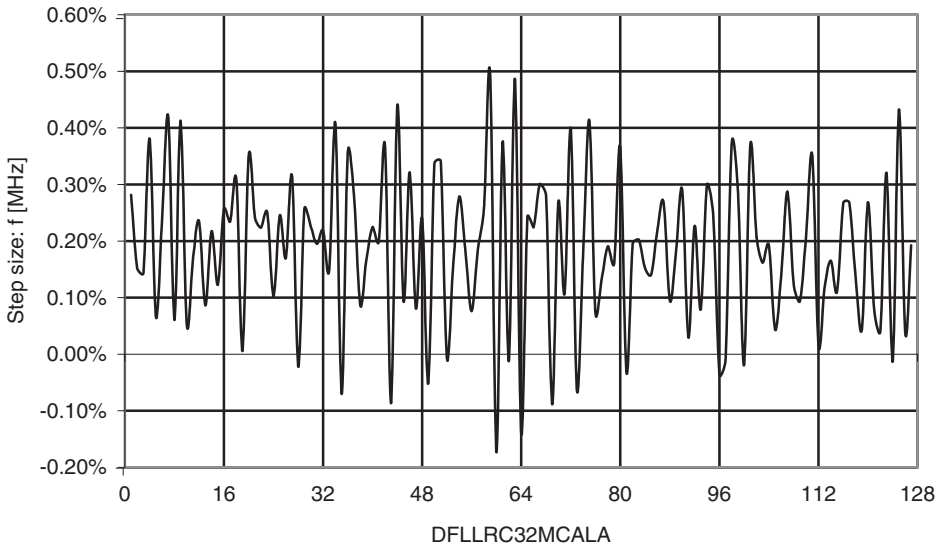
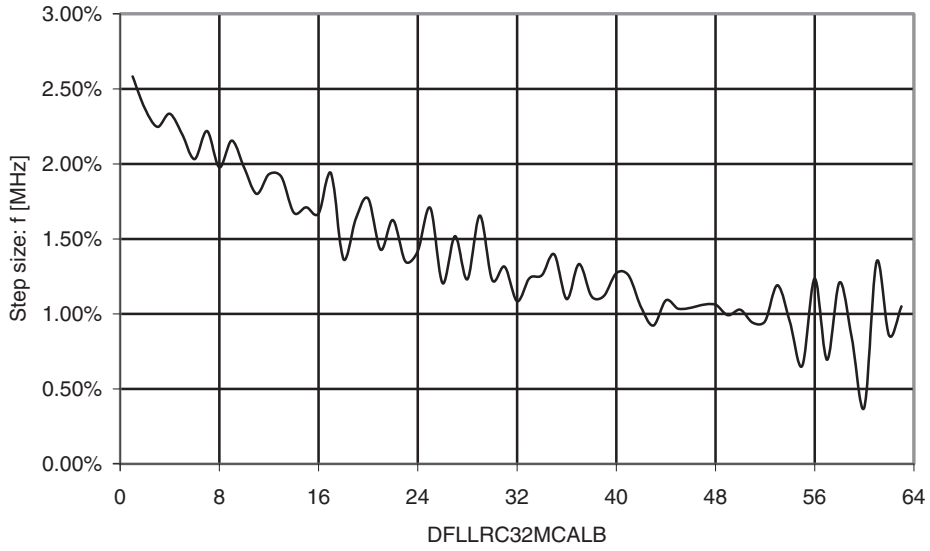


Figure 33-38. Internal 32MHz oscillator CALB calibration step size.
T = -40 to 85°C, V_{CC} = 3V.



33.1.10 Module current consumption

Figure 33-39. AC current consumption vs. V_{CC}.
***Low-power mode*.**

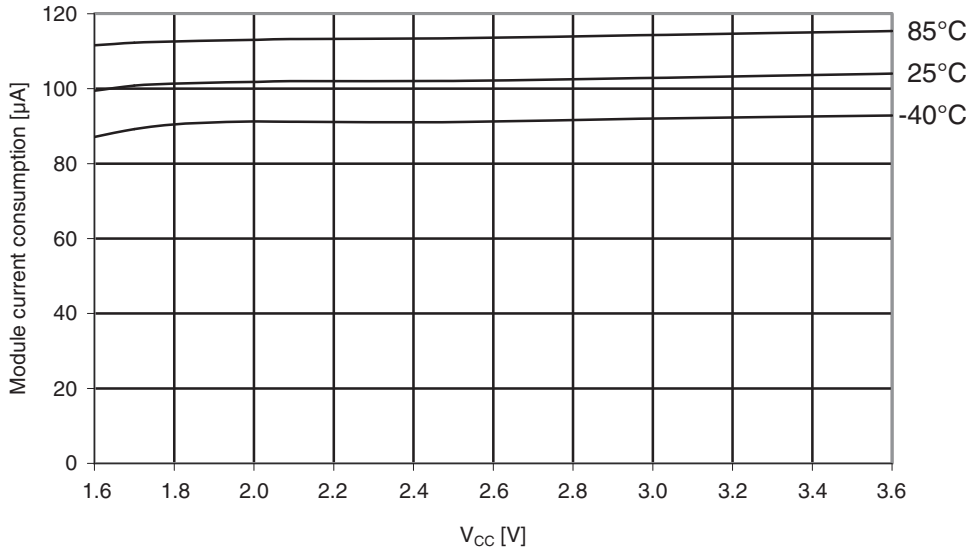
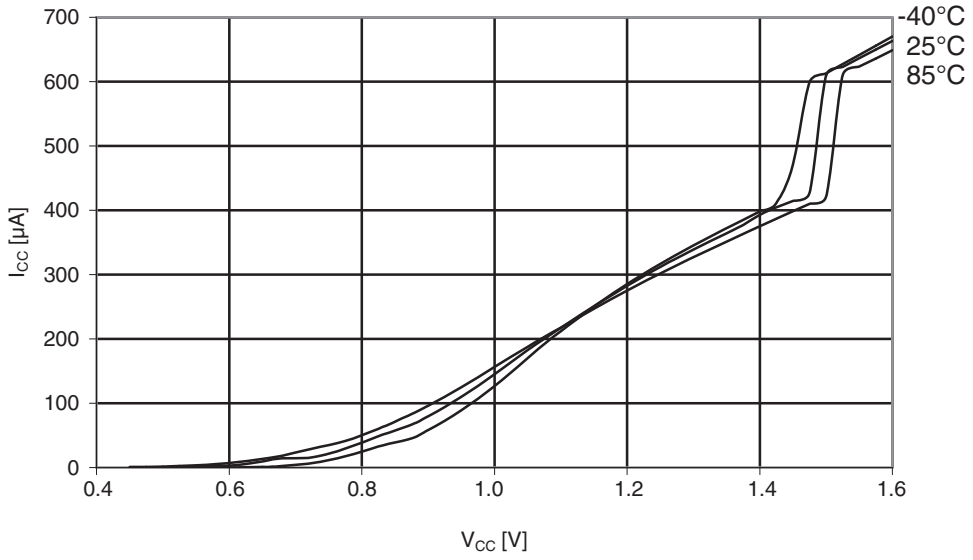
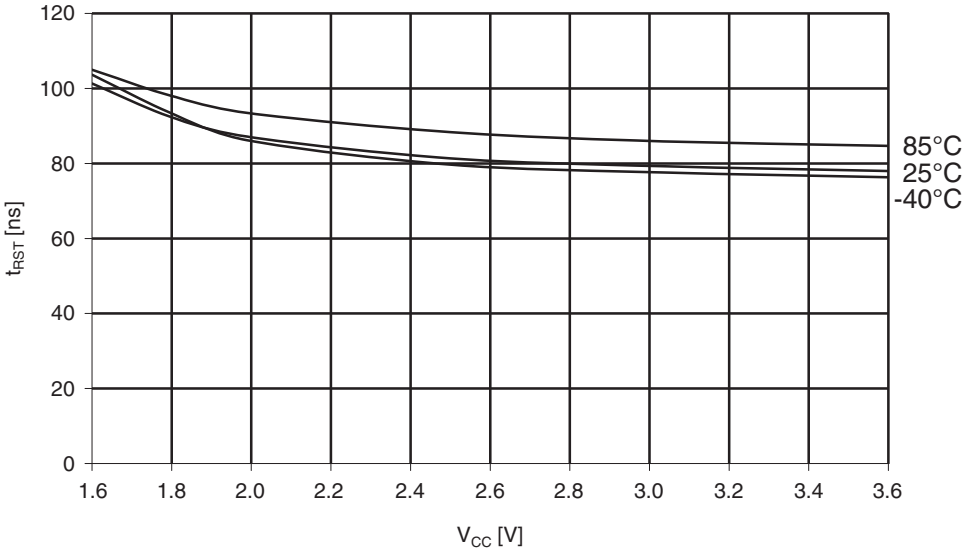


Figure 33-40. Power-up current consumption vs. V_{CC}.



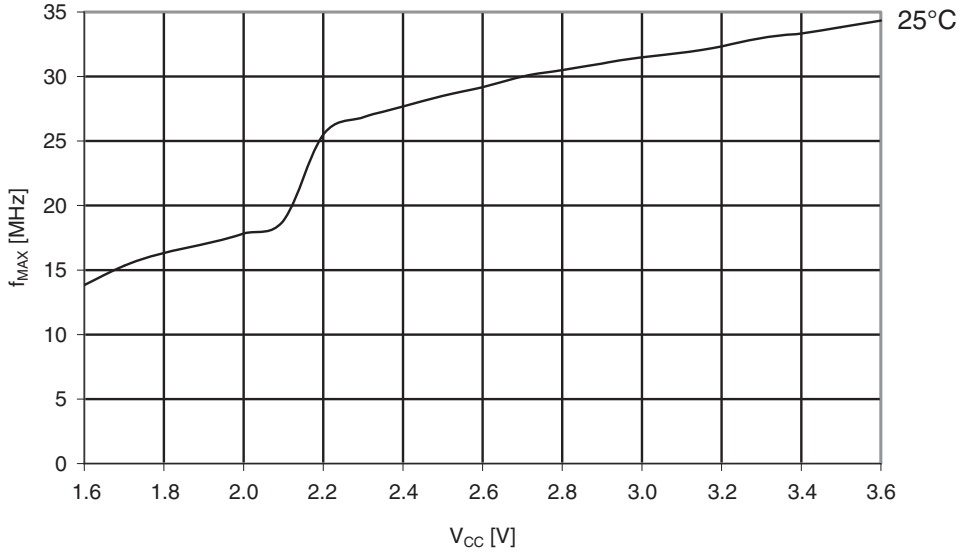
33.1.11 Reset pulse width

Figure 33-41. Minimum reset pulse width vs. V_{CC}.



33.1.12 PDI speed

Figure 33-42. PDI speed vs. V_{CC}.



33.2 Atmel ATxmega64D3

33.2.1 Active supply current

Figure 33-43. Active supply current vs. frequency.
f_{SYS} = 0 - 1MHz external clock, T = 25°C.

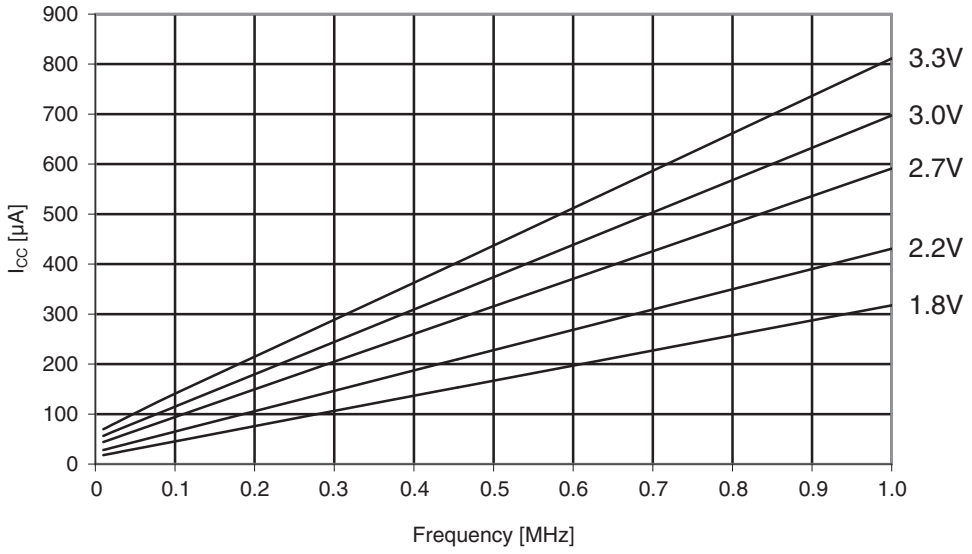


Figure 33-44. Active supply current vs. frequency.
f_{SYS} = 1 - 32MHz external clock, T = 25°C.

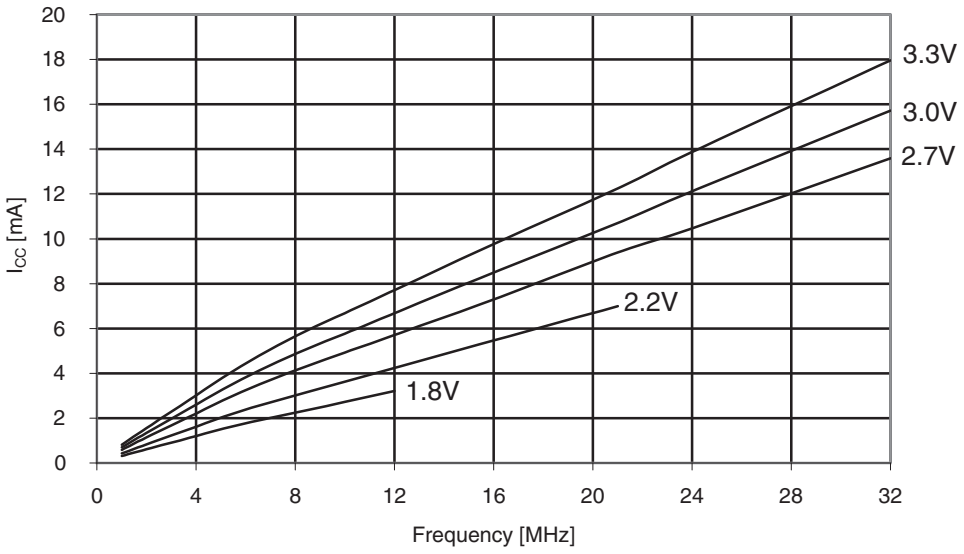


Figure 33-45. Active supply current vs. V_{CC}.
f_{SYS} = 1.0MHz external clock.

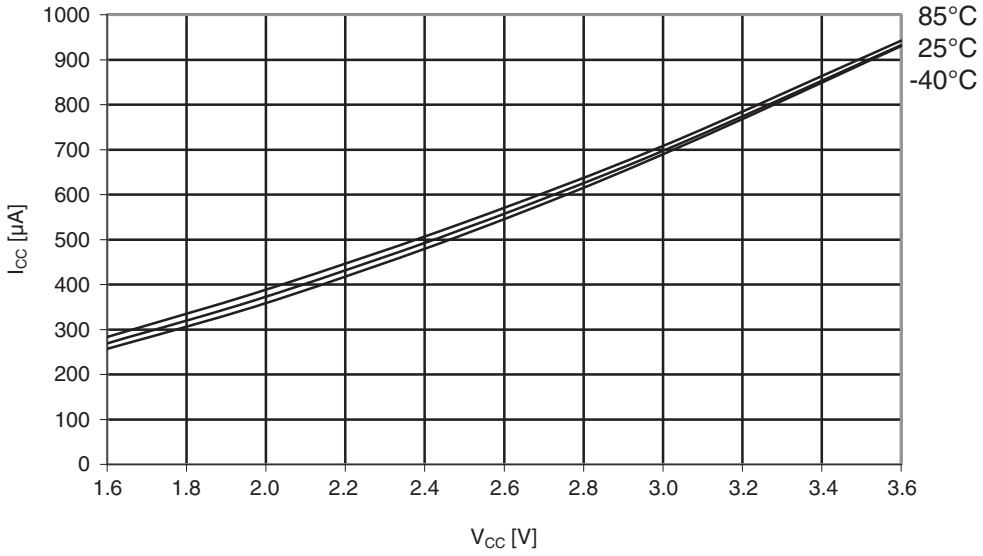


Figure 33-46. Active supply current vs. V_{CC}.
f_{SYS} = 32.768kHz internal RC.

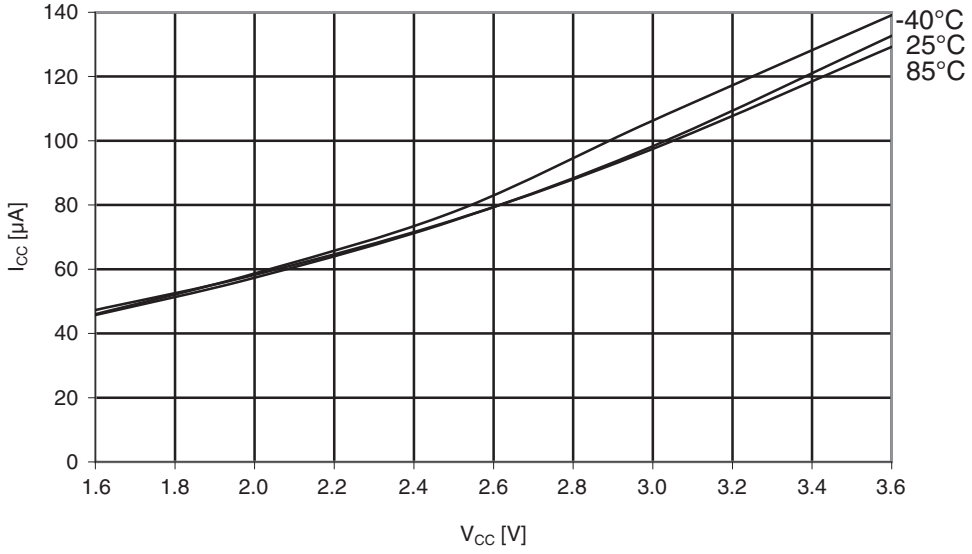


Figure 33-47. Active supply current vs. V_{CC}.
f_{SYS} = 2.0MHz internal RC.

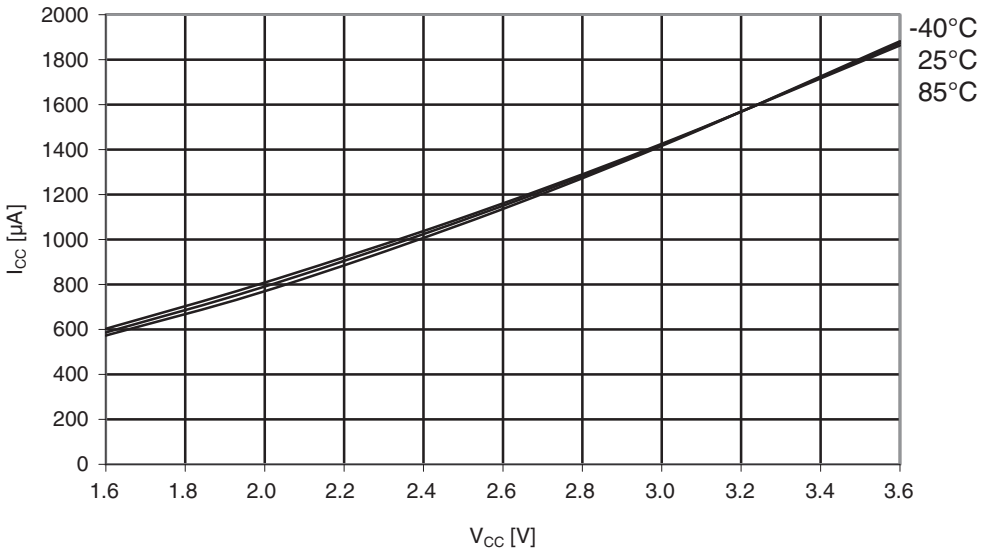


Figure 33-48. Active supply current vs. V_{CC}.
f_{SYS} = 32MHz internal RC prescaled to 8MHz.

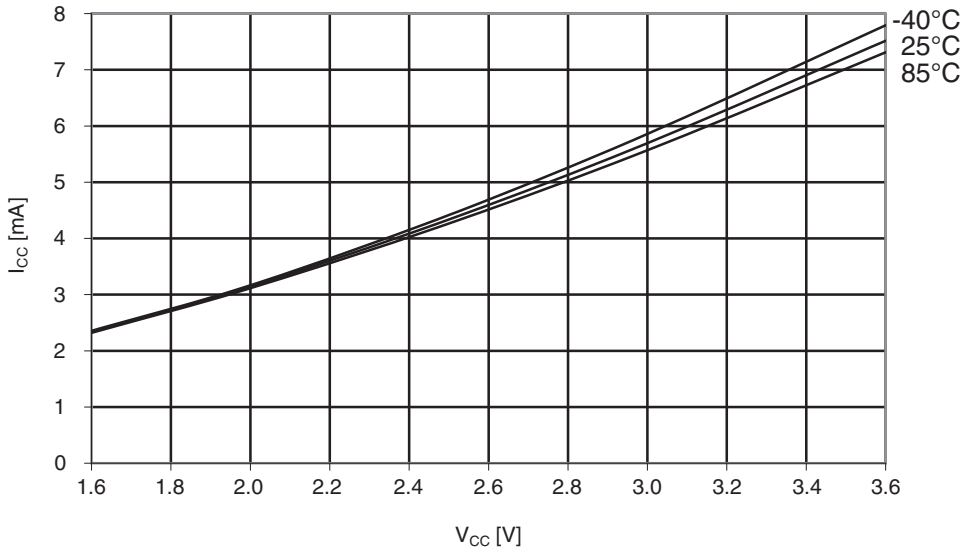
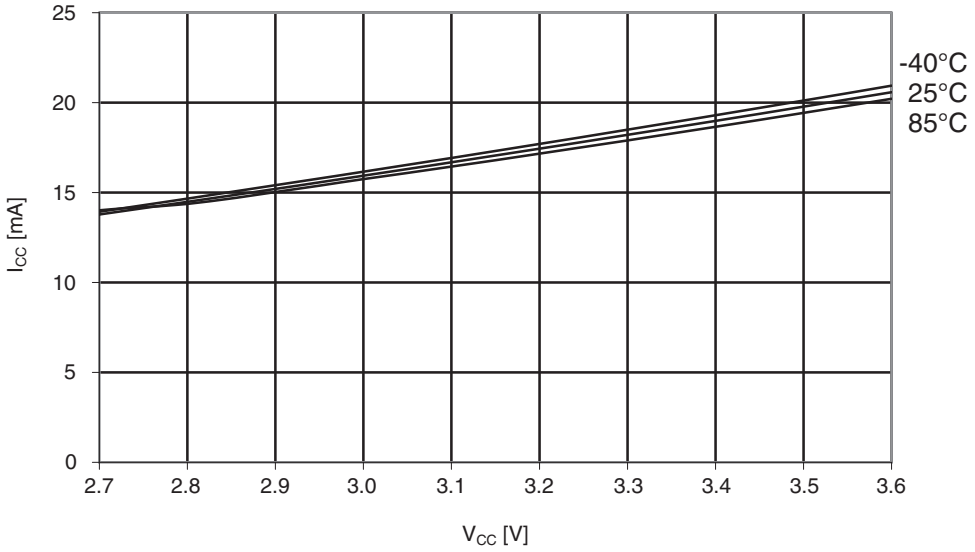


Figure 33-49. Active supply current vs. V_{CC}.
f_{SYS} = 32MHz internal RC.



33.2.2 Idle supply current

Figure 33-50. Idle supply current vs. frequency.
f_{SYS} = 0 - 1.0MHz, T = 25°C.

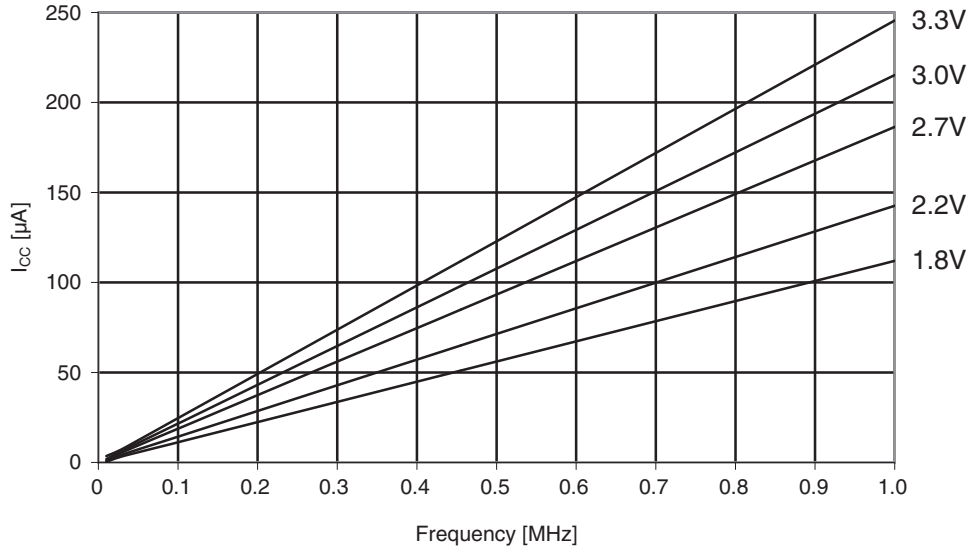


Figure 33-51. Idle supply current vs. frequency.
f_{SYS} = 1 - 32MHz, T = 25°C.

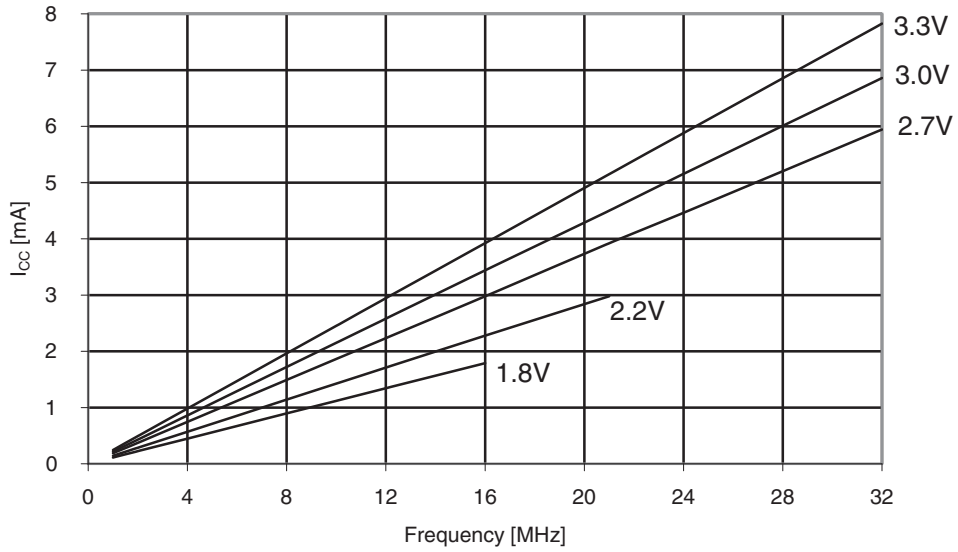


Figure 33-52. Idle supply current vs. V_{CC}.
f_{SYS} = 1.0MHz external clock.

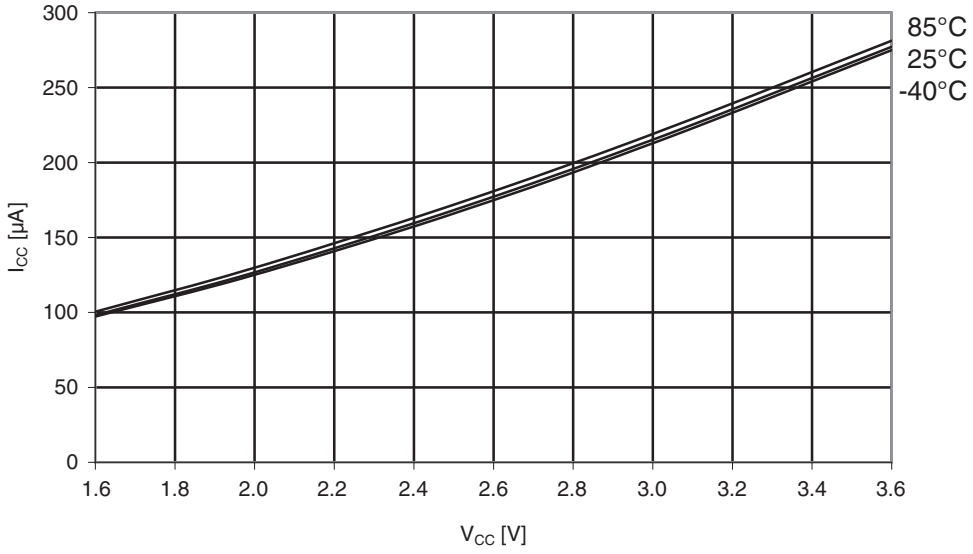


Figure 33-53. Idle supply current vs. V_{CC}.
f_{SYS} = 32.768kHz internal RC.

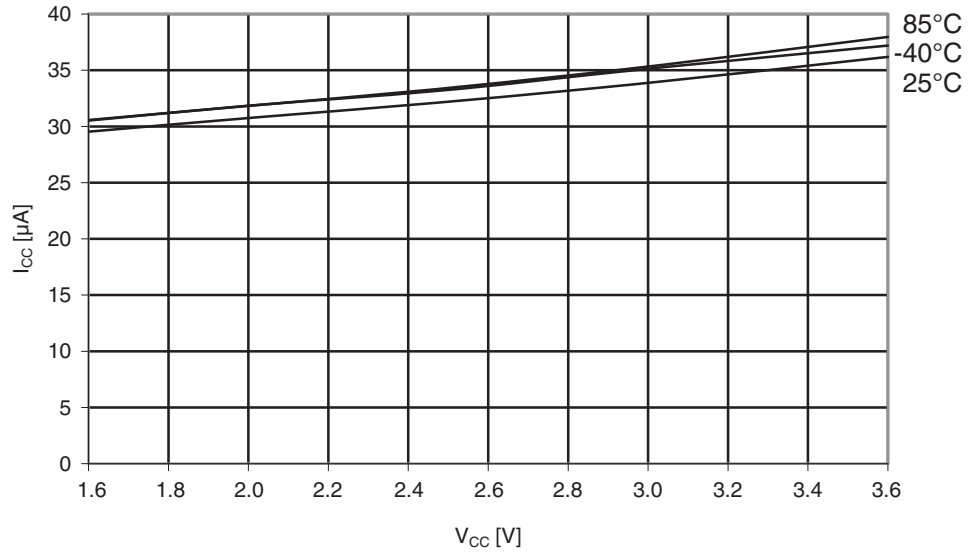


Figure 33-54. Idle supply current vs. V_{CC}.
f_{SYS} = 2.0MHz internal RC.

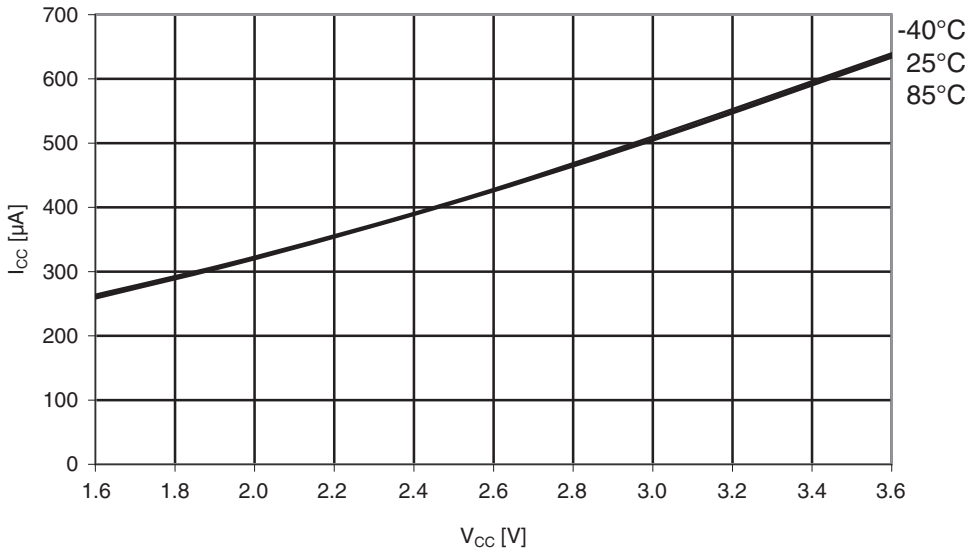


Figure 33-55. Idle supply current vs. V_{CC}.
f_{SYS} = 32MHz internal RC prescaled to 8MHz.

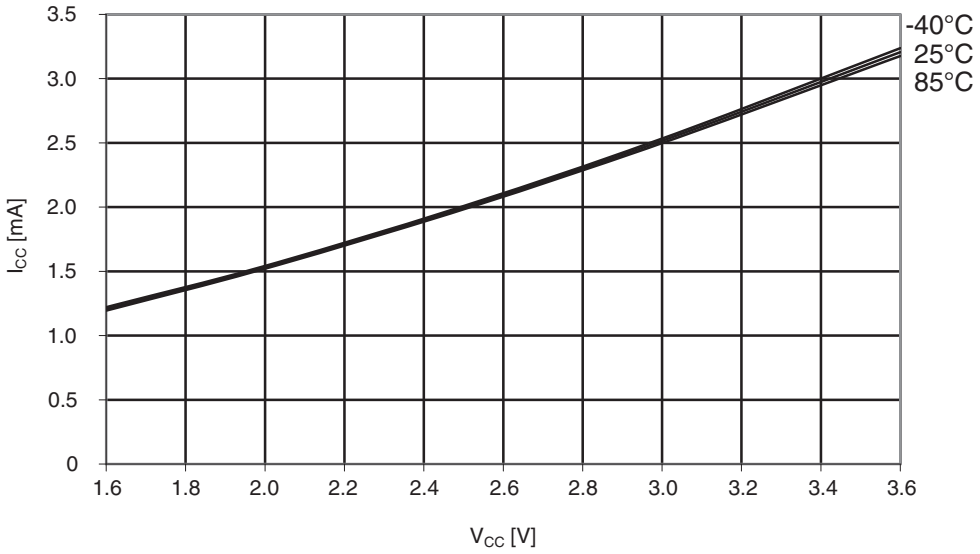
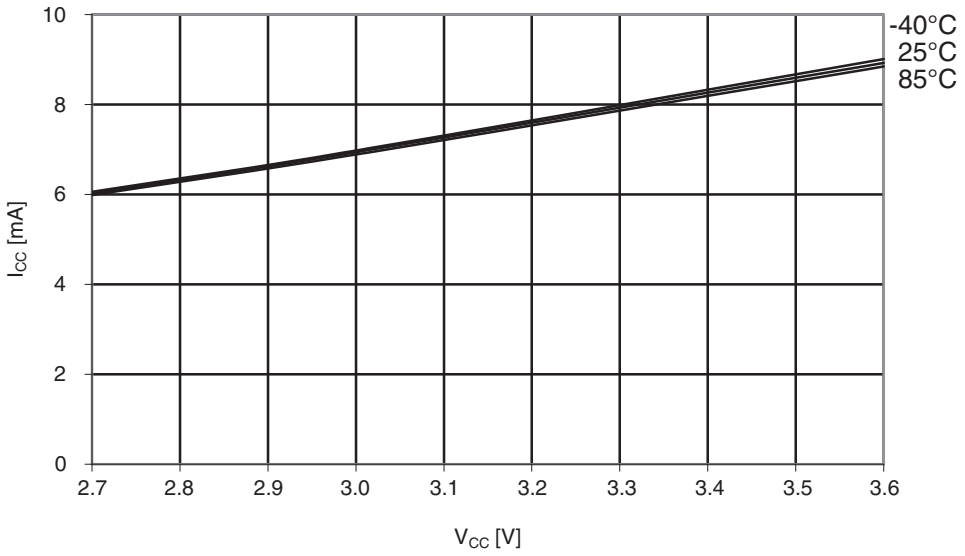


Figure 33-56. Idle supply current vs. V_{CC}.
f_{SYS} = 32MHz internal RC.



33.2.3 Power-down supply current

Figure 33-57. Power-down supply current vs. temperature.

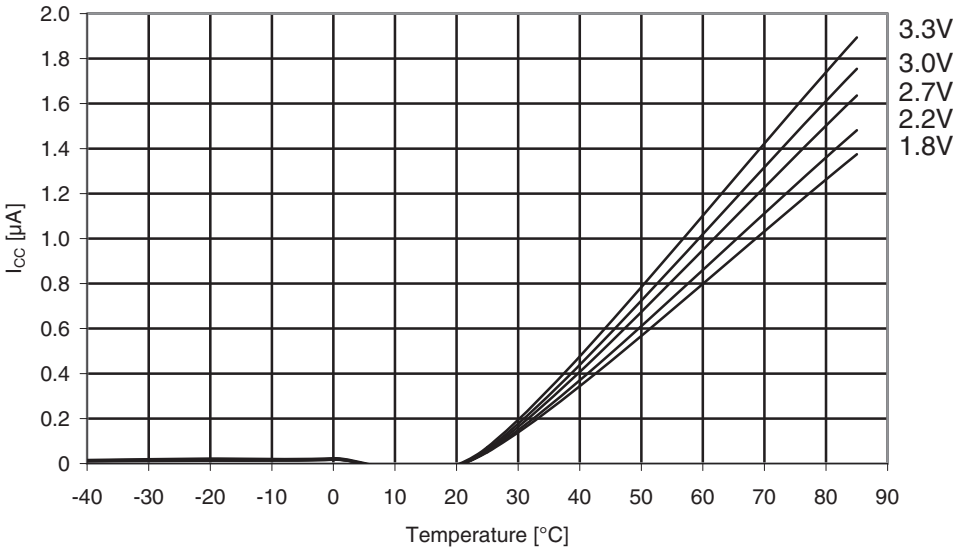
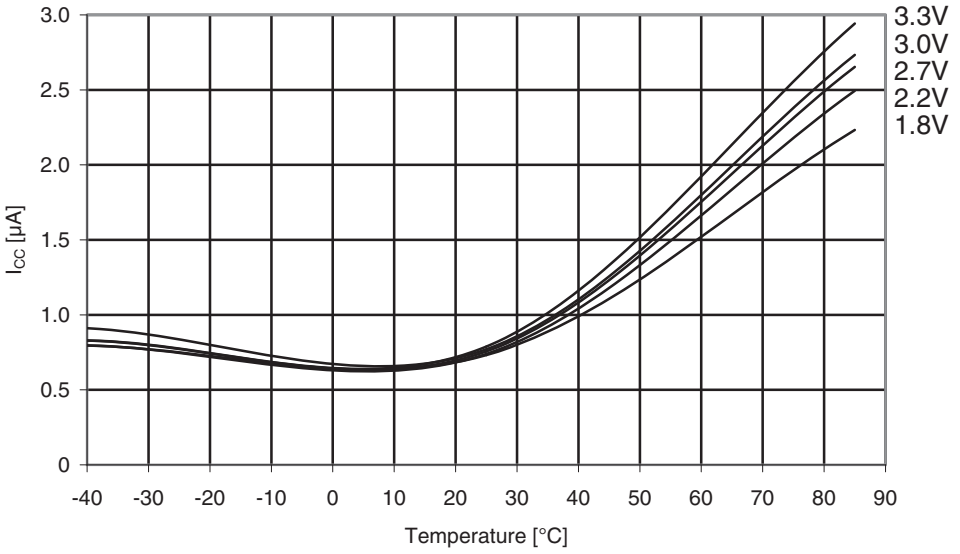
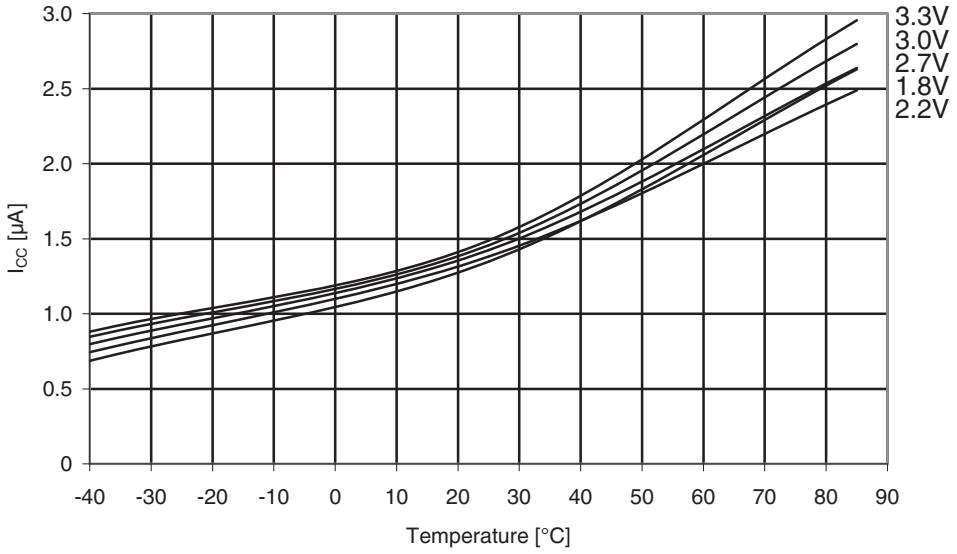


Figure 33-58. Power-down supply current vs. temperature.
With WDT and sampled BOD enabled.



33.2.4 Power-save supply current

Figure 33-59. Power-save supply current vs. temperature.
With WDT, sampled BOD, and RTC from ULP enabled.



33.2.5 Pin pull-up

Figure 33-60. Reset pull-up resistor current vs. reset pin voltage.
V_{CC} = 1.8V.

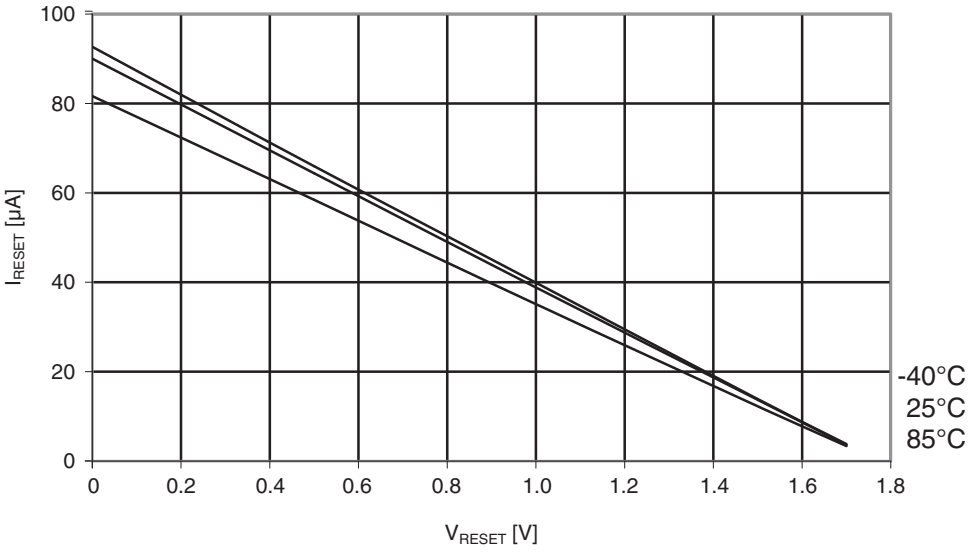


Figure 33-61. Reset pull-up resistor current vs. reset pin voltage.
V_{CC} = 3.0V.

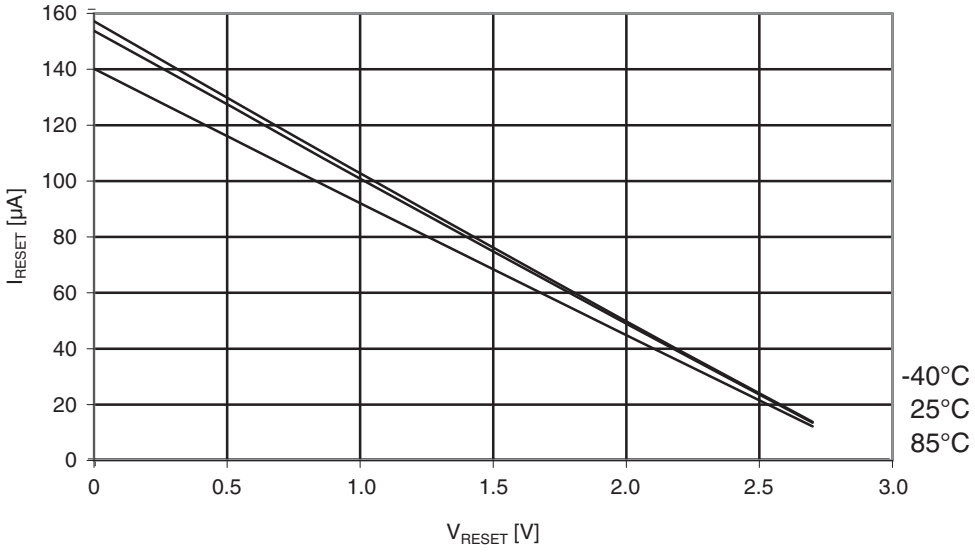
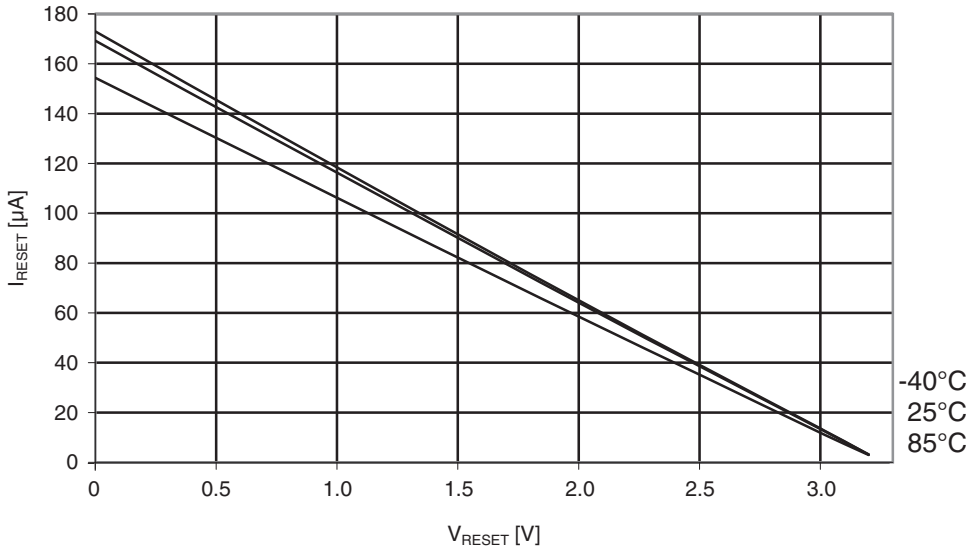


Figure 33-62. Reset pull-up resistor current vs. reset pin voltage.
V_{CC} = 3.3V.



33.2.6 Pin output voltage vs. sink/source current

Figure 33-63. I/O pin output voltage vs. source current.
V_{CC} = 1.8V.

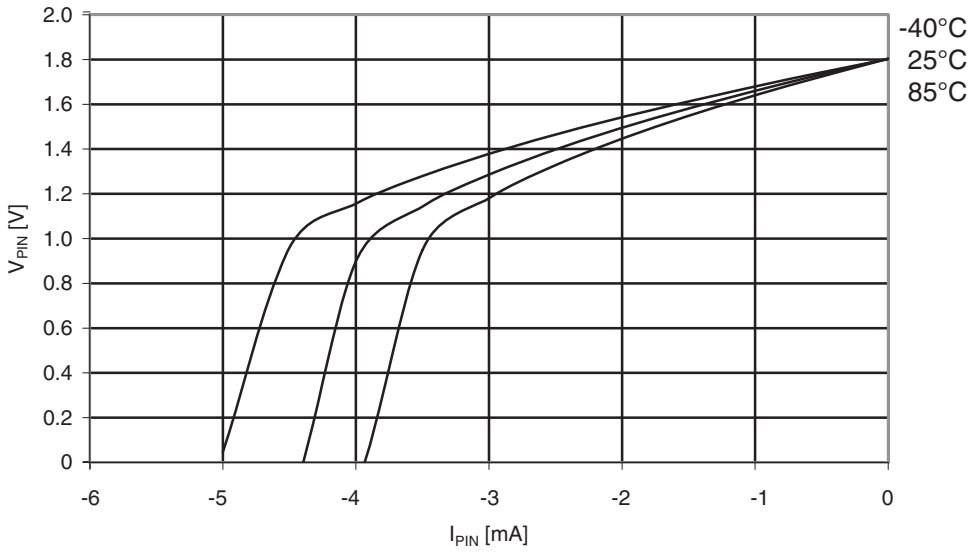


Figure 33-64. I/O pin output voltage vs. source current.
V_{CC} = 3.0V.

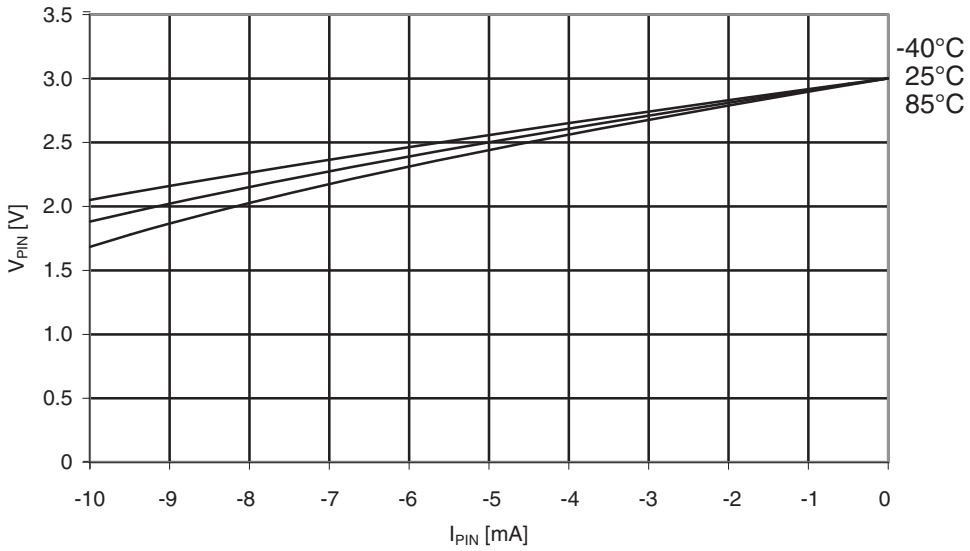


Figure 33-65. I/O pin output voltage vs. source current.
V_{CC} = 3.3V.

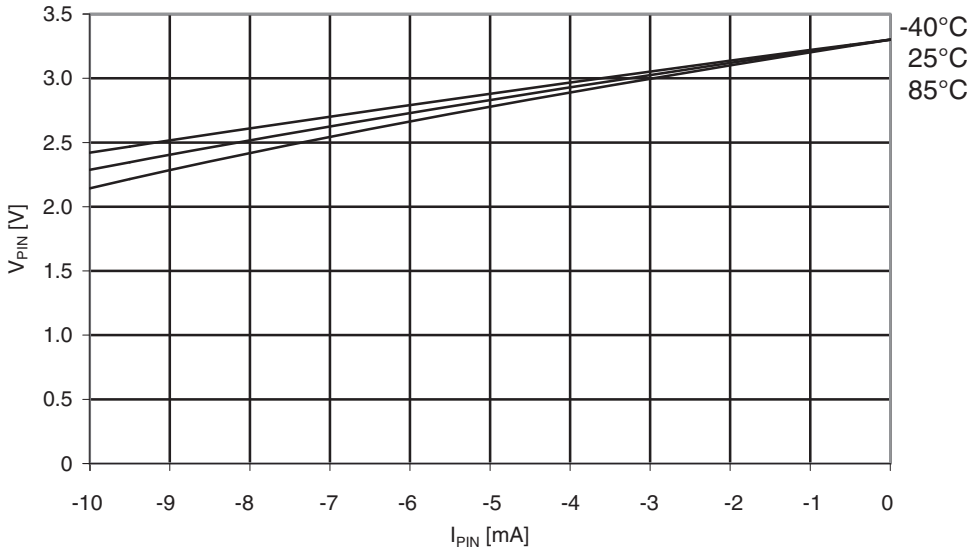


Figure 33-66. I/O pin output voltage vs. sink current.
V_{CC} = 1.8V.

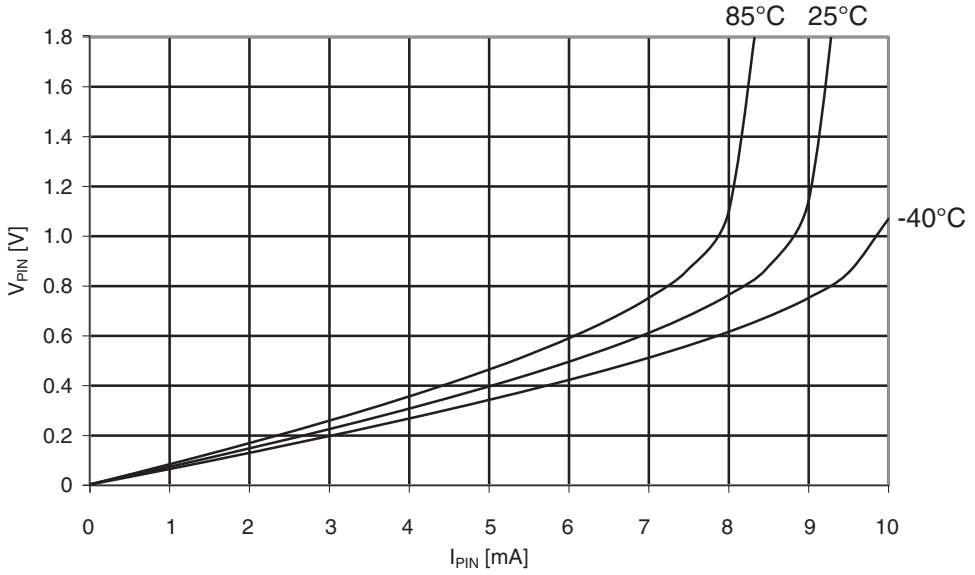


Figure 33-67. I/O pin output voltage vs. sink current.
V_{CC} = 3.0V.

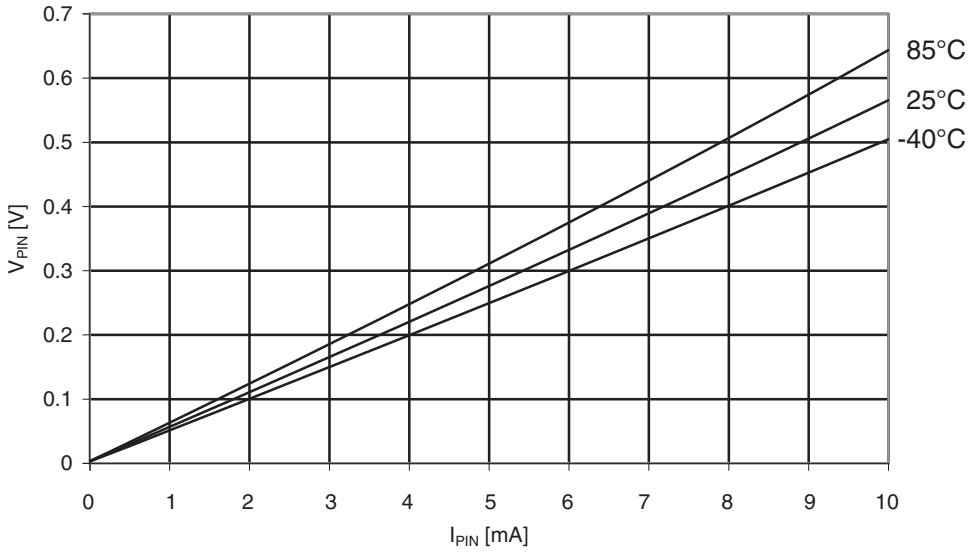
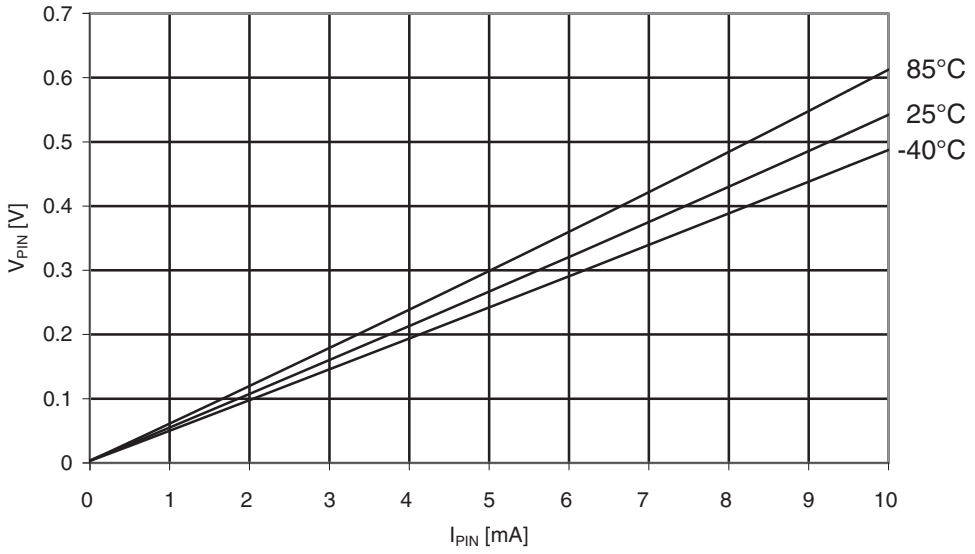


Figure 33-68. I/O pin output voltage vs. sink current.
V_{CC} = 3.3V.



33.2.7 Thresholds and hysteresis

Figure 33-69. I/O pin input threshold voltage vs. V_{CC}.
V_{IH} - I/O pin read as "1".

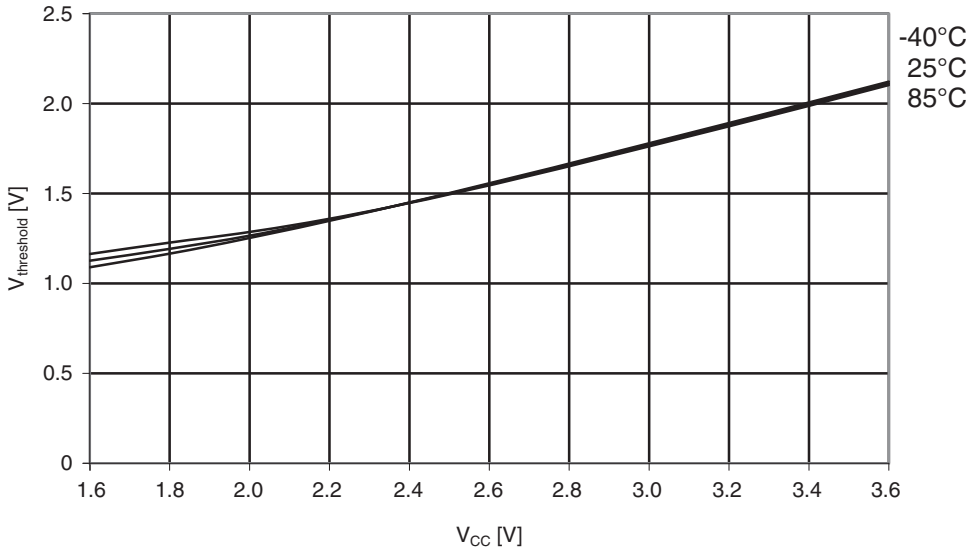


Figure 33-70. I/O pin input threshold voltage vs. V_{CC}.
V_{IL} - I/O pin read as "0".

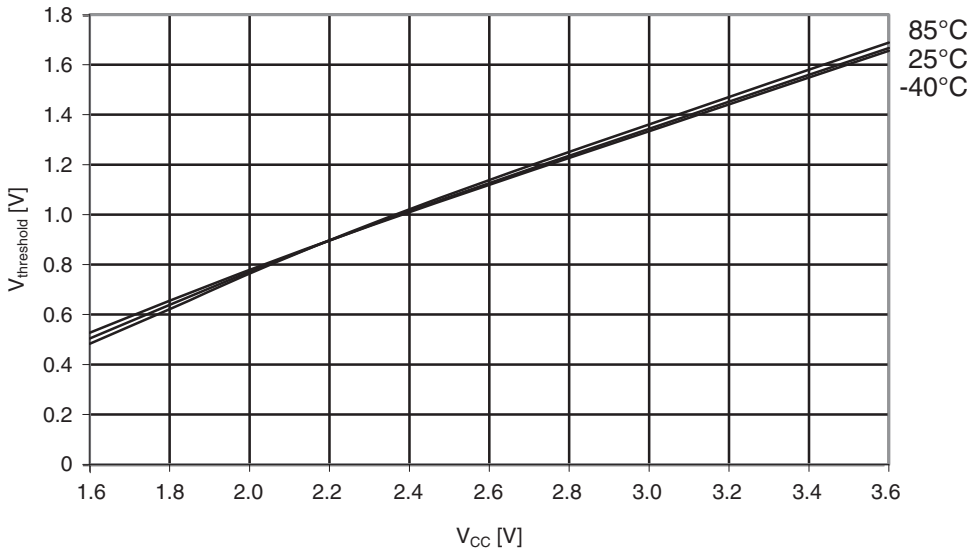


Figure 33-71. I/O pin input hysteresis vs. V_{CC}.

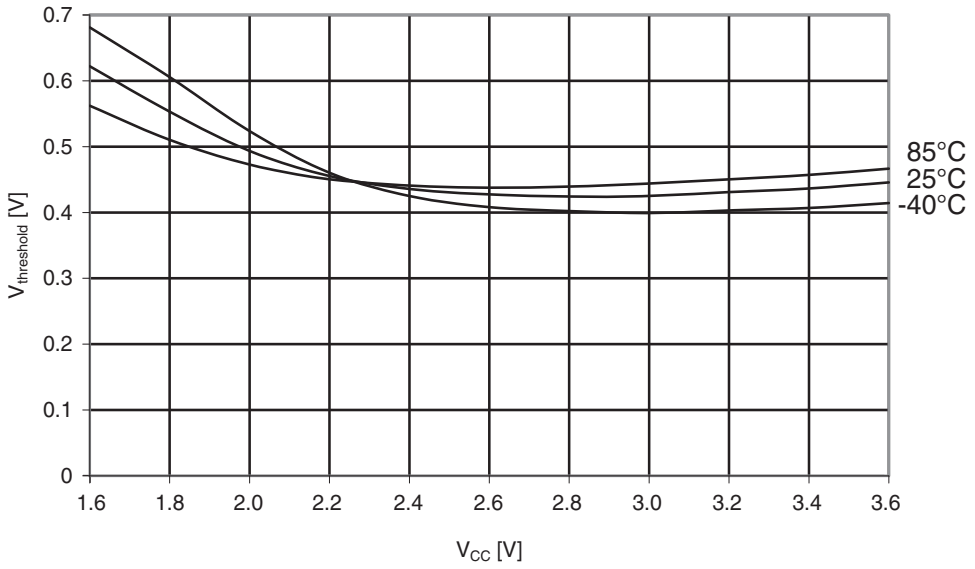


Figure 33-72. Reset input threshold voltage vs. V_{CC}.
V_{IL} - I/O pin read as "1".

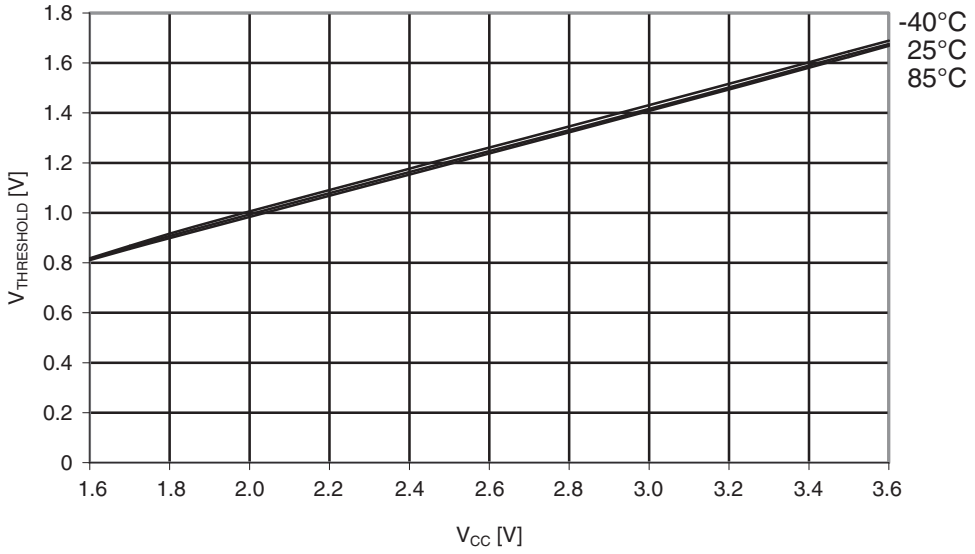
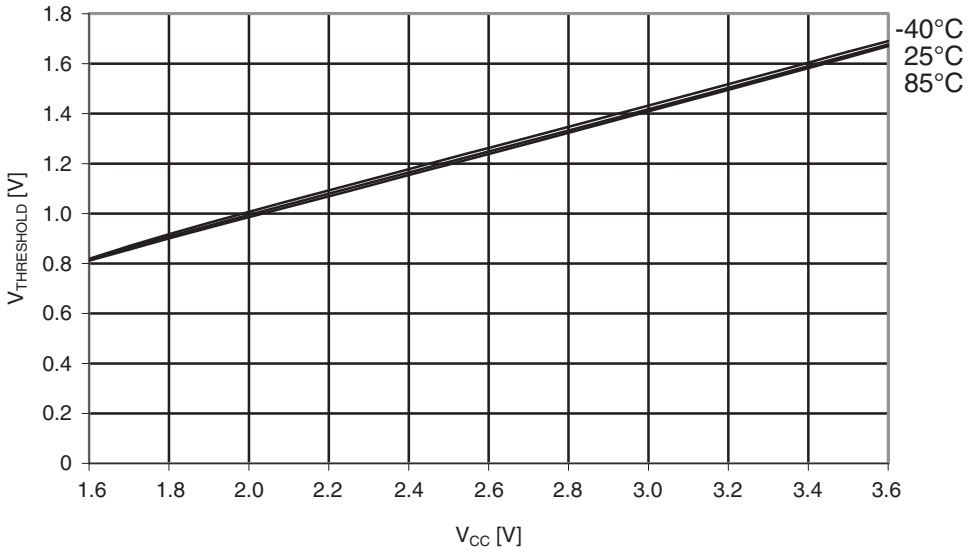


Figure 33-73. Reset input threshold voltage vs. V_{CC}.
V_{IL} - I/O pin read as "0".



33.2.8 BOD thresholds

Figure 33-74. BOD thresholds vs. temperature.
BOD level = 1.6V.

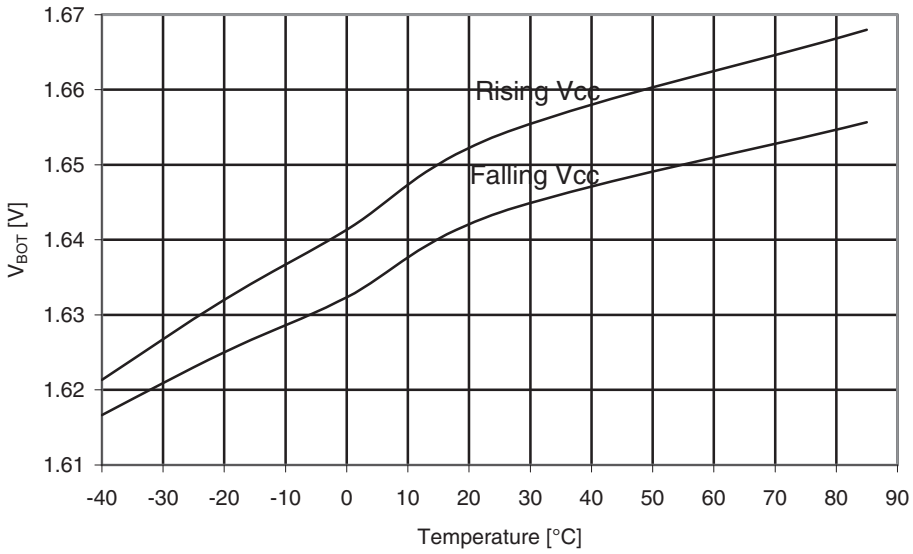
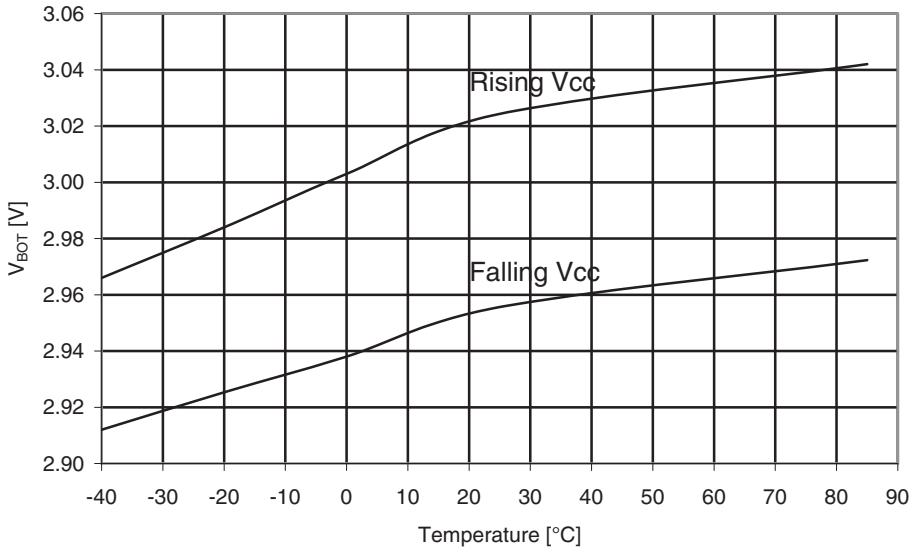


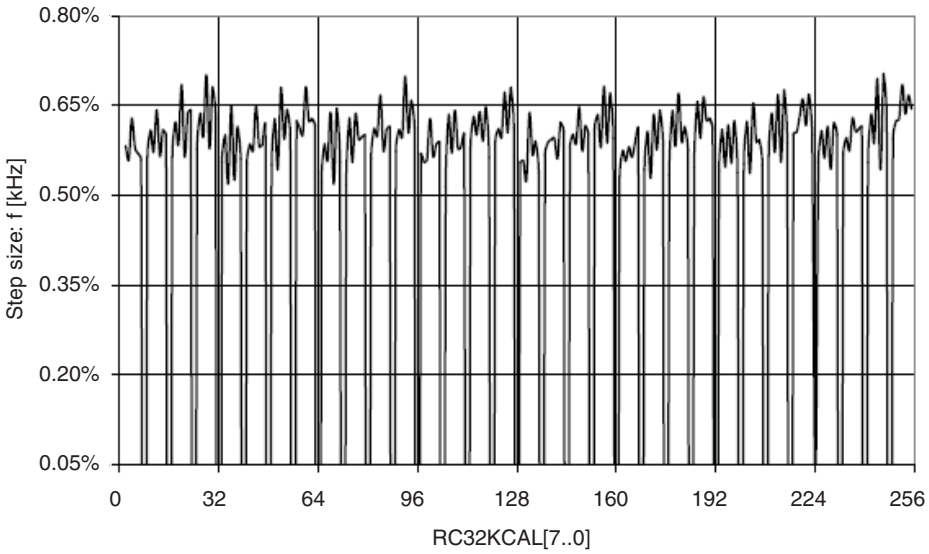
Figure 33-75. BOD thresholds vs. temperature.
BOD level = 2.9V.



33.2.9 Oscillators and wake-up time

33.2.9.1 Internal 32.768kHz oscillator

Figure 33-76. Internal 32.768kHz oscillator calibration step size.
T = -40 to 85°C, V_{CC} = 3V.



33.2.9.2 Internal 2MHz oscillator

Figure 33-77. Internal 2MHz oscillator CALA calibration step size.
T = -40 to 85°C, V_{CC} = 3V.

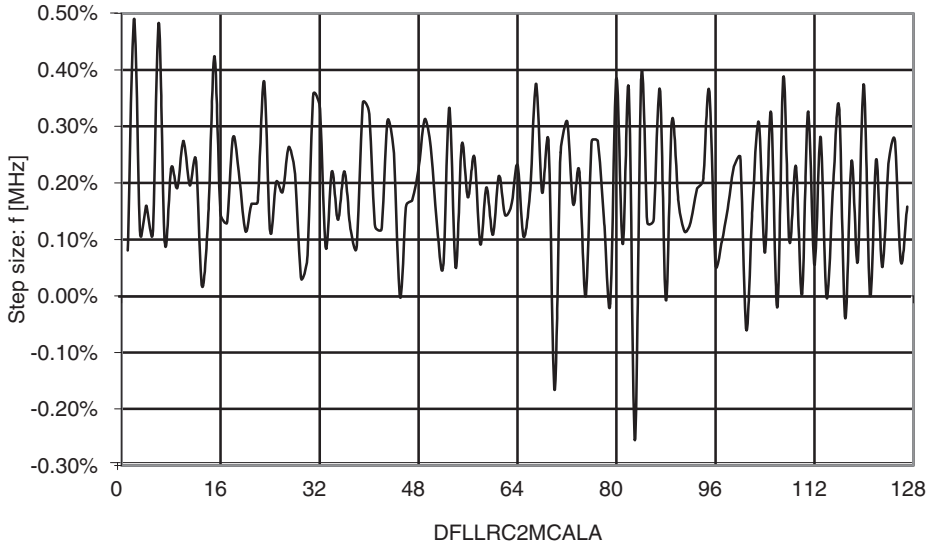
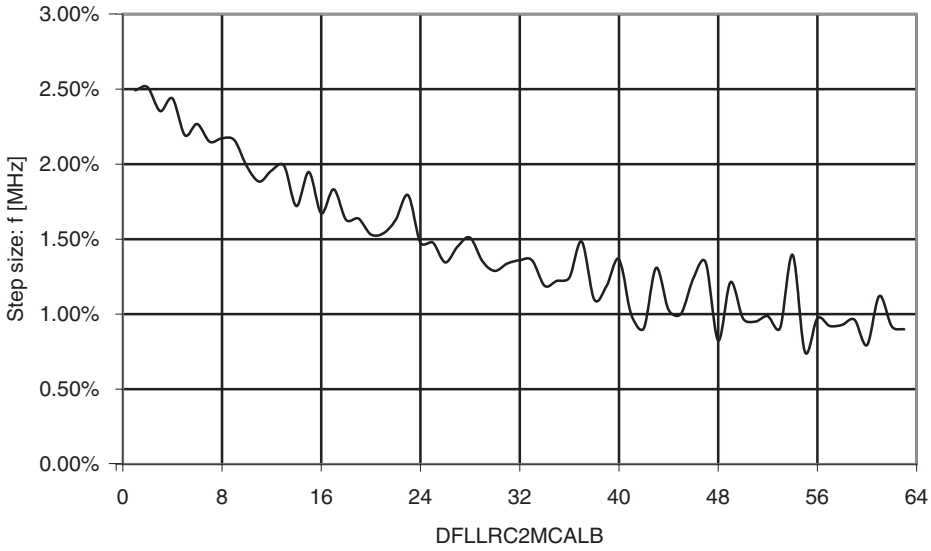


Figure 33-78. Internal 2MHz oscillator CALB calibration step size.
T = -40 to 85°C, V_{CC} = 3V.



33.2.9.3 Internal 32MHz oscillator

Figure 33-79. Internal 32MHz oscillator CALA calibration step size.
T = -40 to 85°C, V_{CC} = 3V.

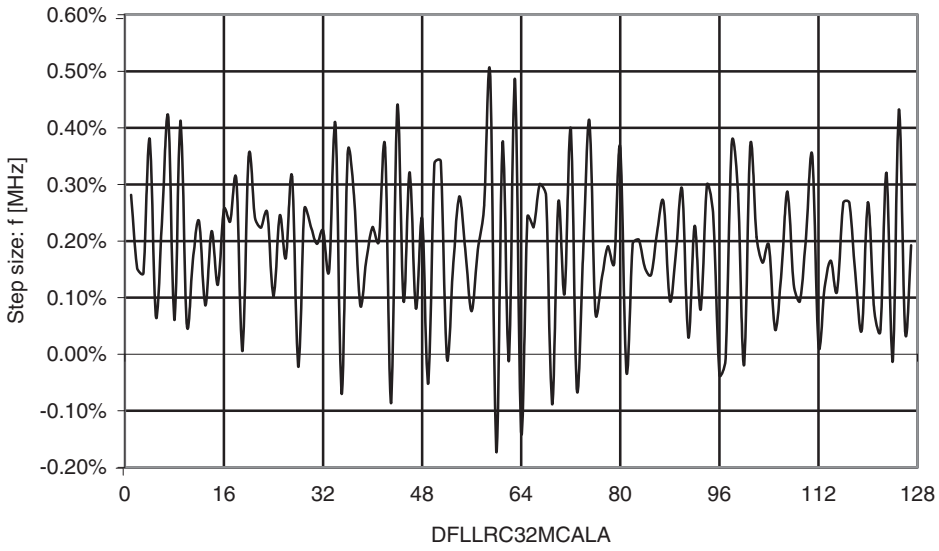
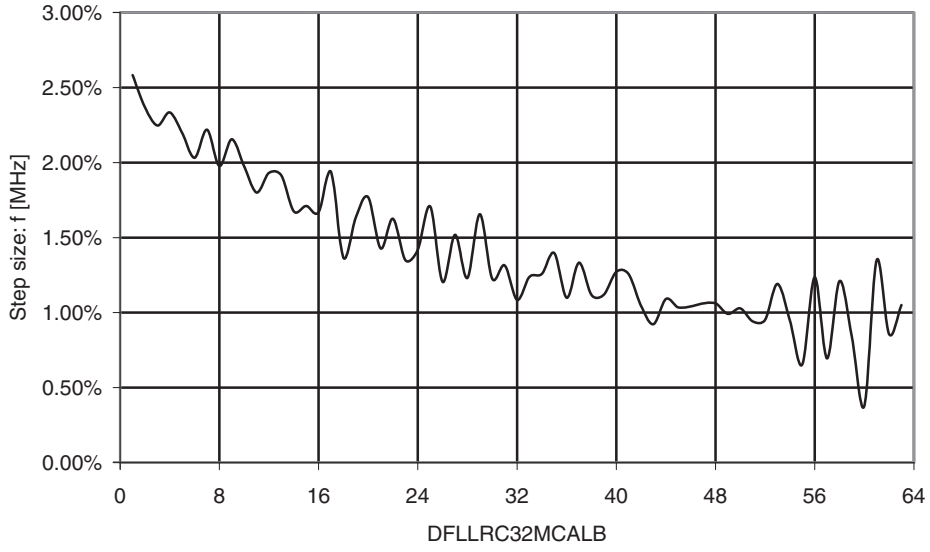


Figure 33-80. Internal 32MHz oscillator CALB calibration step size.
T = -40 to 85°C, V_{CC} = 3V.



33.2.10 Module current consumption

Figure 33-81. AC current consumption vs. V_{CC}.
***Low-power mode*.**

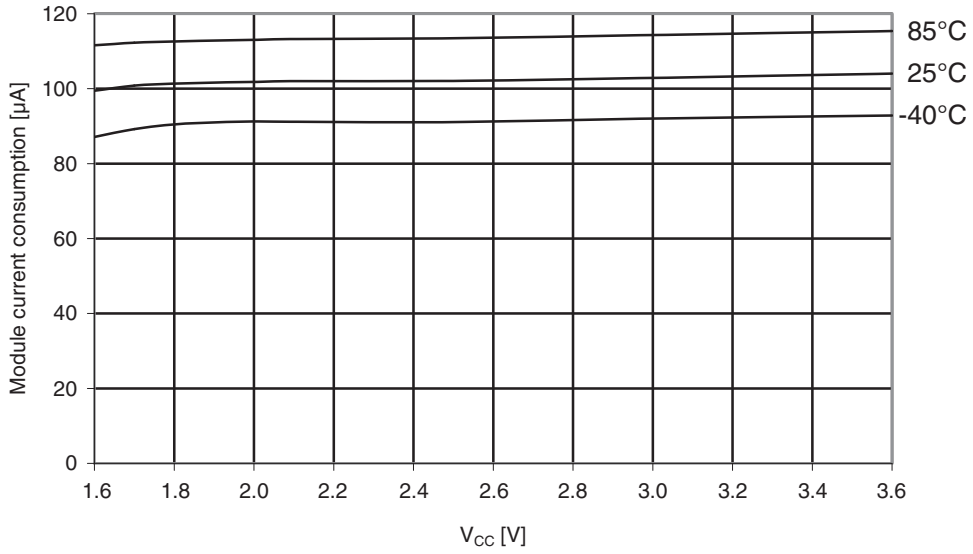
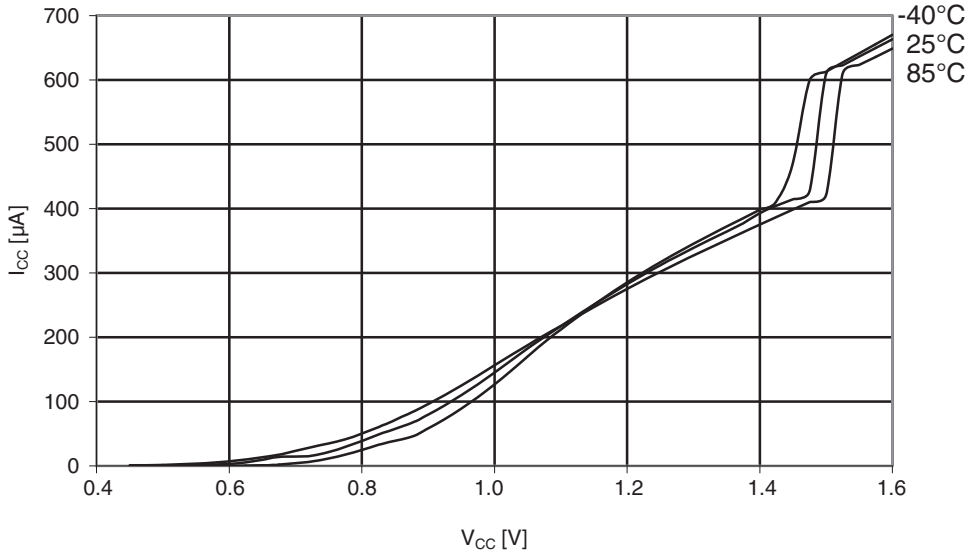
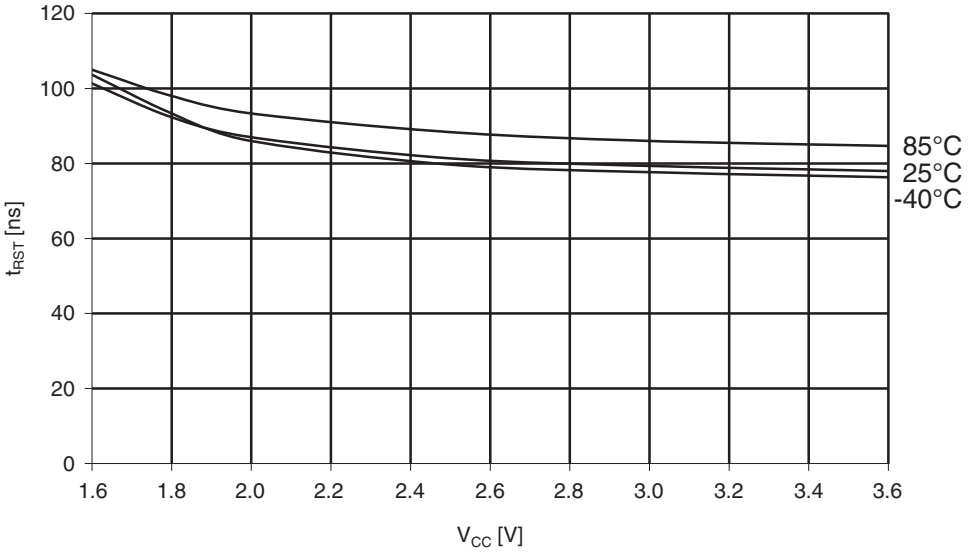


Figure 33-82. Power-up current consumption vs. V_{CC}.



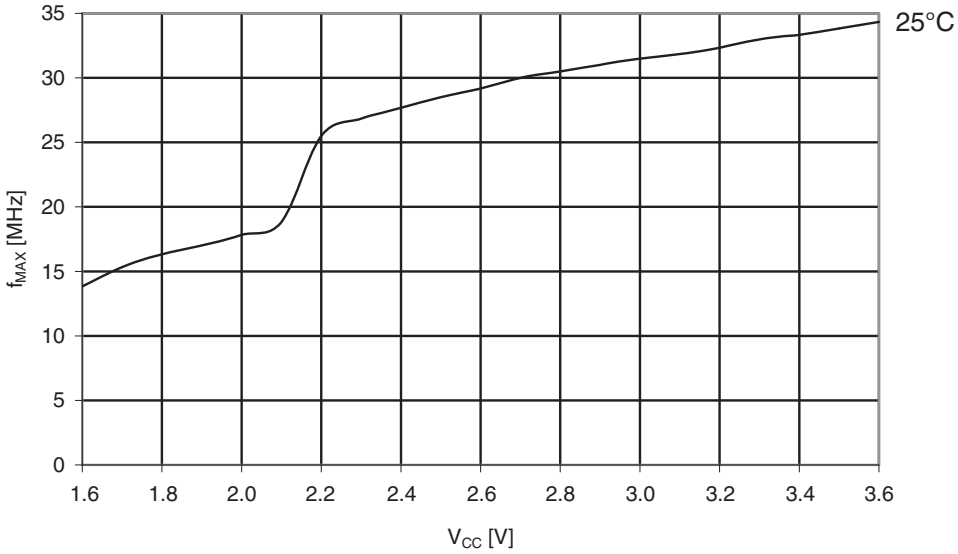
33.2.11 Reset pulse width

Figure 33-83. Minimum reset pulse width vs. V_{CC}.



33.2.12 PDI speed

Figure 33-84. PDI speed vs. V_{CC}.



33.3 Atmel ATxmega128D3

33.3.1 Current consumption

33.3.1.1 Active supply current

Figure 33-85. Active supply current vs. frequency.
f_{SYS} = 0 - 1MHz external clock, T = 25°C.

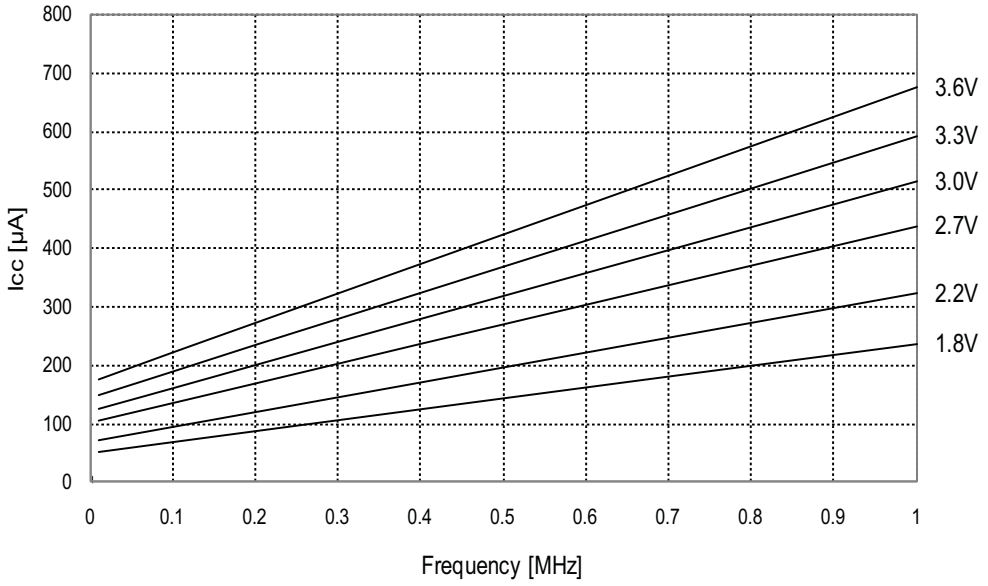


Figure 33-86. Active supply current vs. frequency.
f_{SYS} = 1 - 32MHz external clock, T = 25°C.

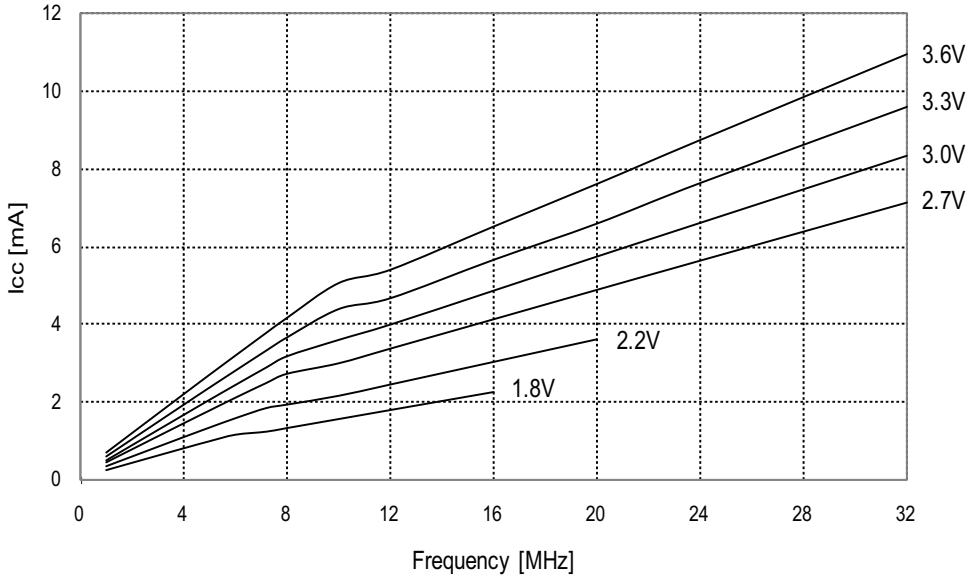


Figure 33-87. Active supply current vs. V_{CC}.
f_{SYS} = 32.768kHz internal RC.

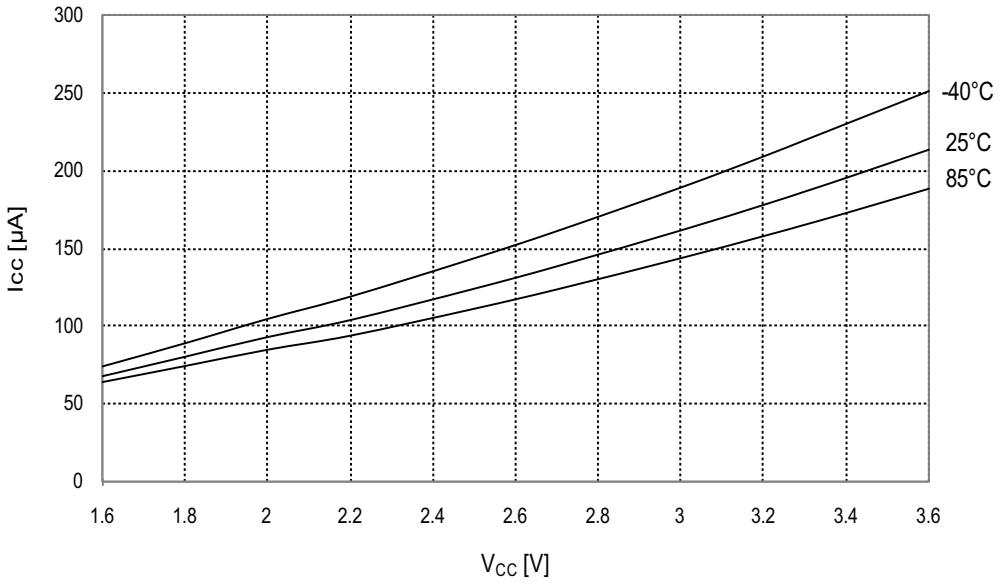


Figure 33-88. Active supply current vs. V_{CC}.
f_{SYS} = 1.0MHz external clock.

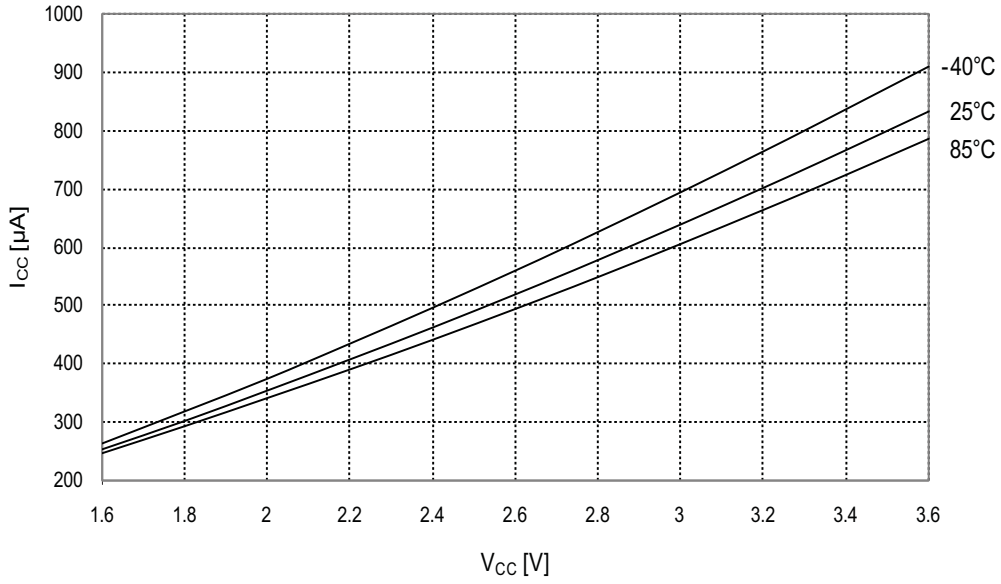


Figure 33-89. Active supply current vs. V_{CC}.

f_{SYS} = 2.0MHz internal RC.

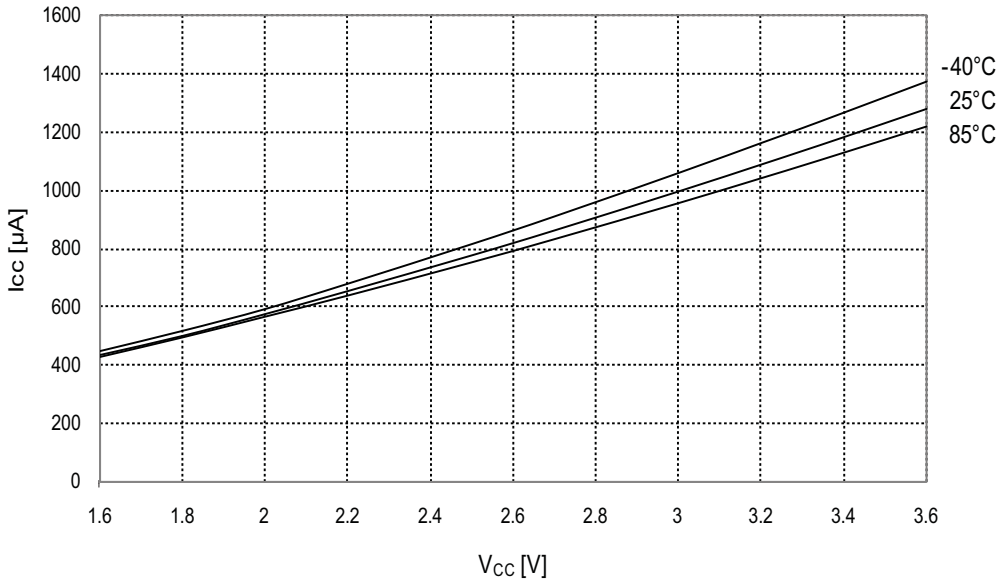


Figure 33-90. Active supply current vs. V_{CC}.

f_{SYS} = 32MHz internal RC prescaled to 8MHz.

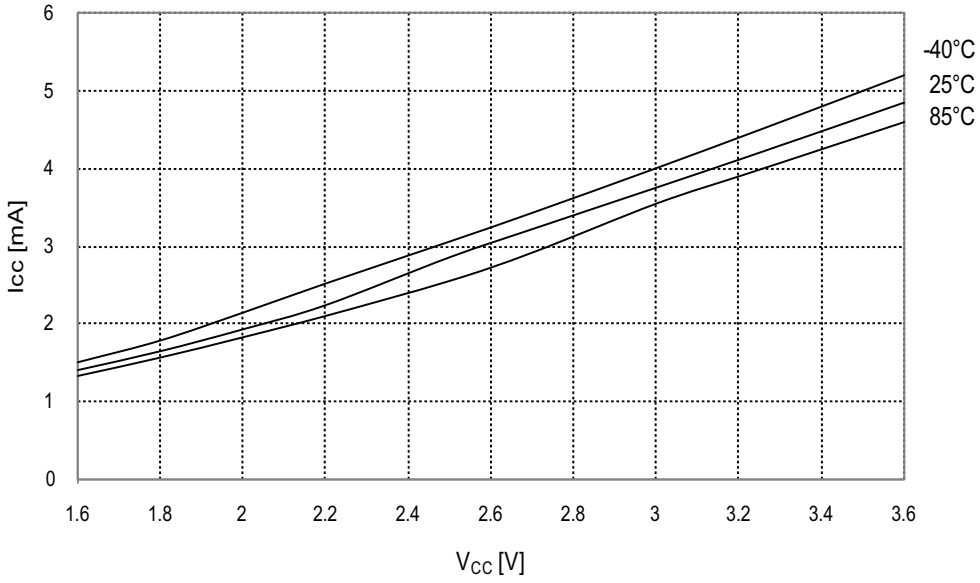
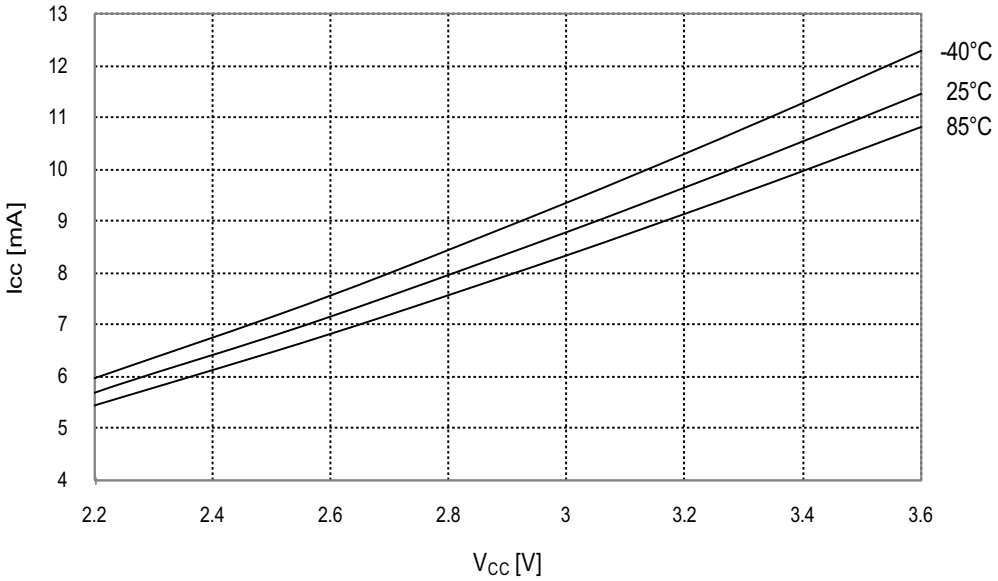


Figure 33-91. Active supply current vs. V_{CC}.
f_{SYS} = 32MHz internal RC.



33.3.1.2 Idle supply current

Figure 33-92. Idle supply current vs. frequency.
f_{SYS} = 0 - 1.0MHz, T = 25°C.

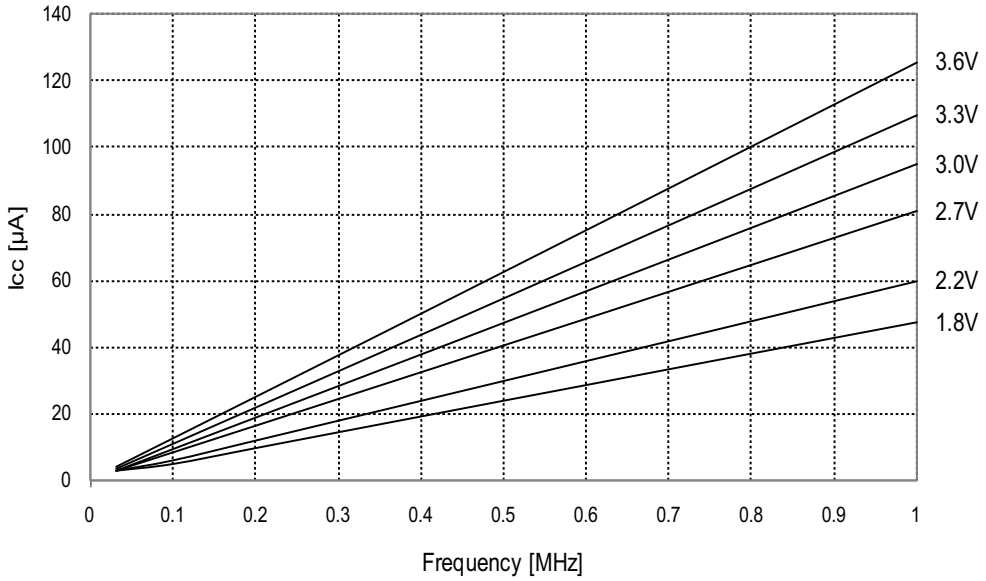


Figure 33-93. Idle supply current vs. frequency.
f_{SYS} = 1 - 32MHz, T = 25°C.

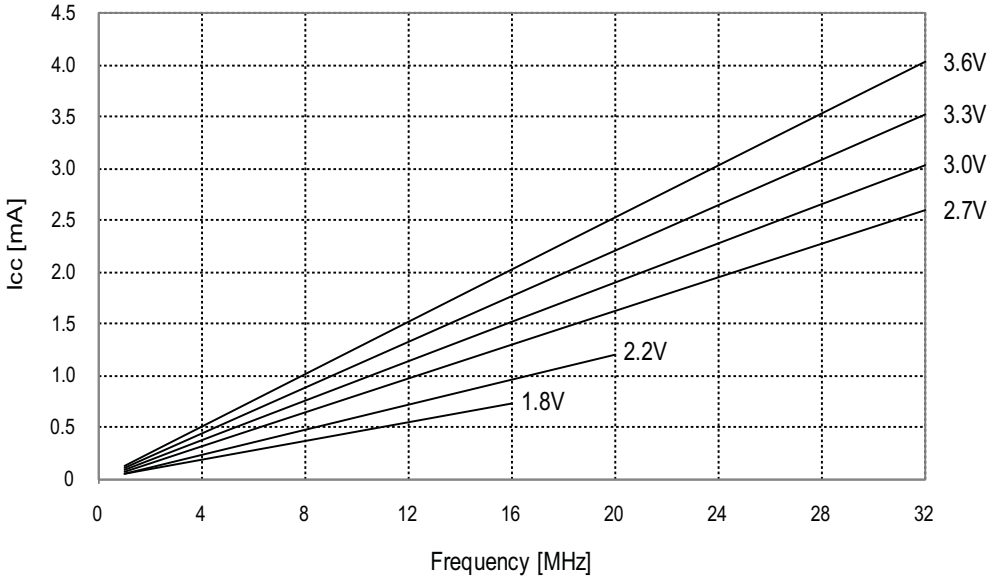


Figure 33-94. Idle supply current vs. V_{CC}.
f_{SYS} = 32.768kHz internal RC.

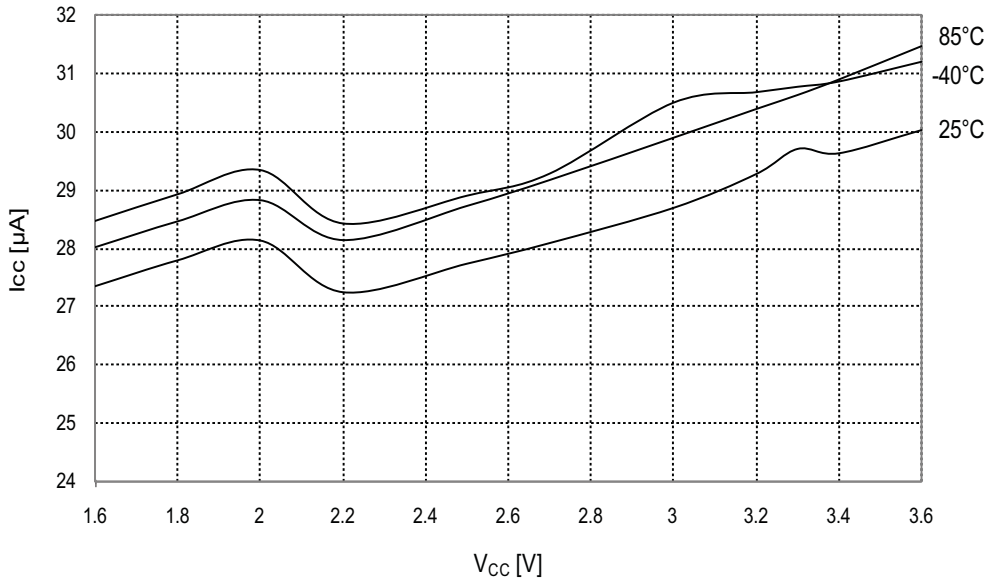


Figure 33-95. Idle supply current vs. V_{CC}.
f_{SYS} = 1.0MHz external clock.

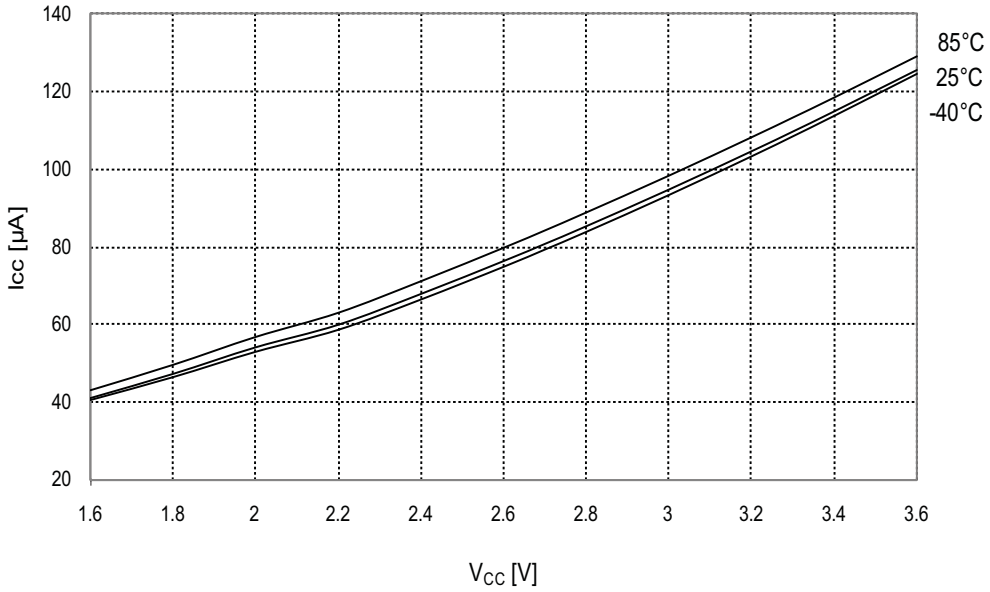


Figure 33-96. Idle supply current vs. V_{CC}.
f_{SYS} = 2.0MHz internal RC.

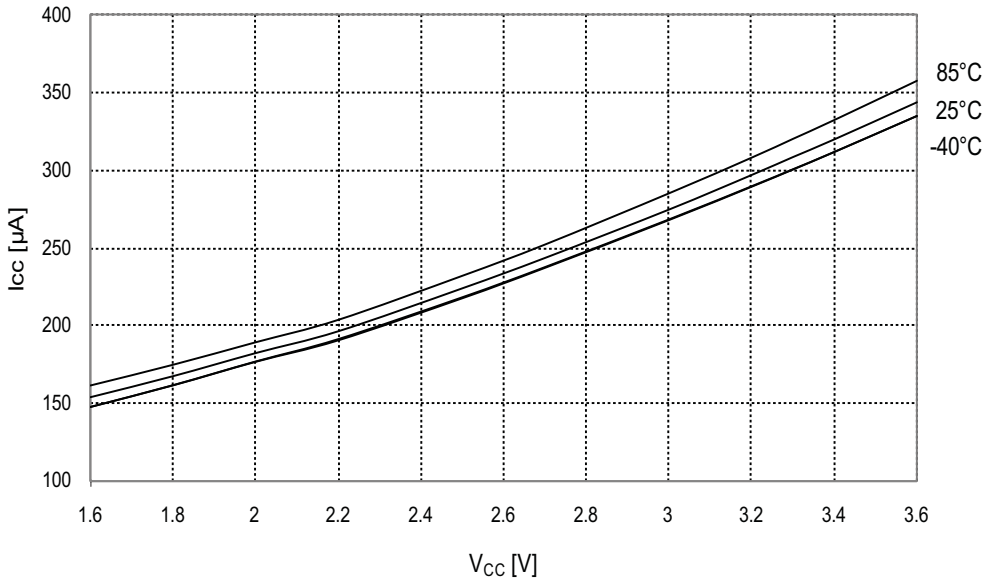


Figure 33-97. Idle supply current vs. V_{CC}.
f_{SYS} = 32MHz internal RC prescaled to 8MHz.

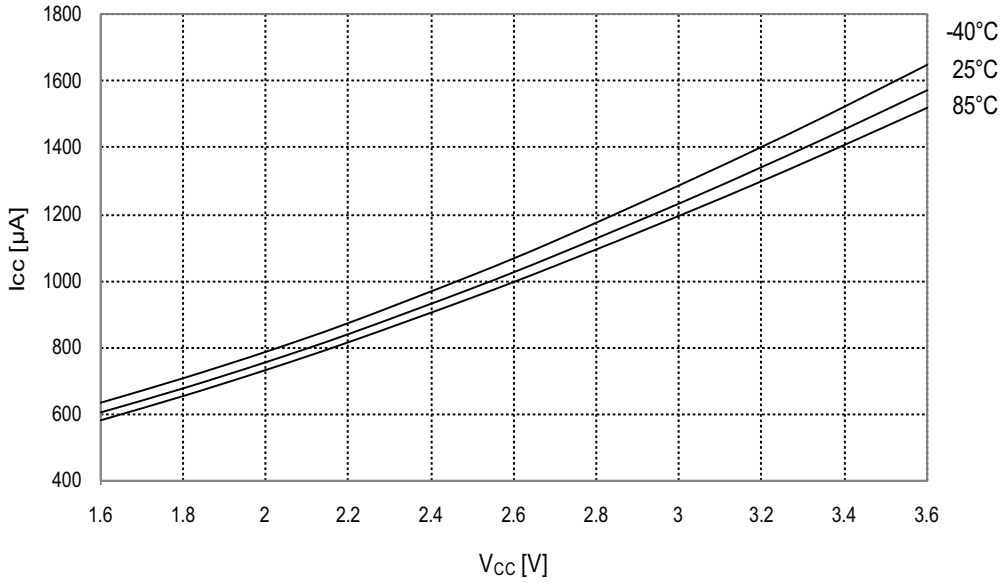
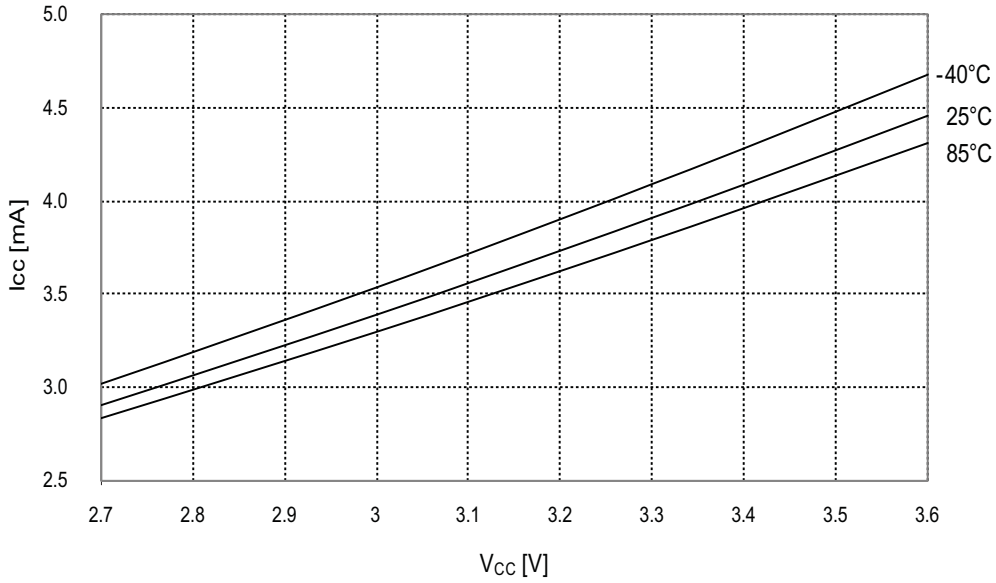


Figure 33-98. Idle supply current vs. V_{CC}.
f_{SYS} = 32MHz internal RC.



33.3.1.3 Power-down supply current

Figure 33-99. Power-down supply current vs. V_{CC}.
All functions disabled.

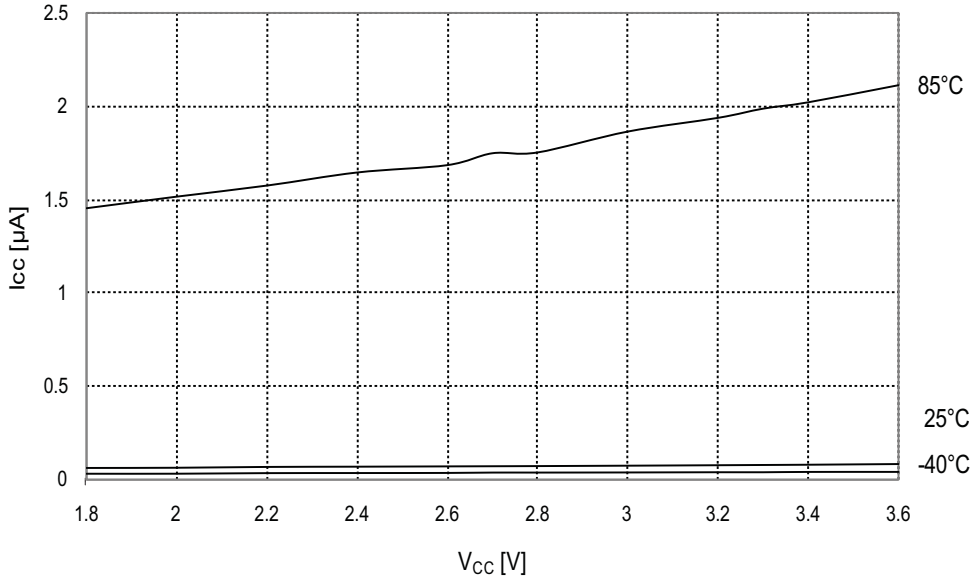


Figure 33-100. Power-down supply current vs. V_{CC}.
Watchdog and sampled BOD enabled.

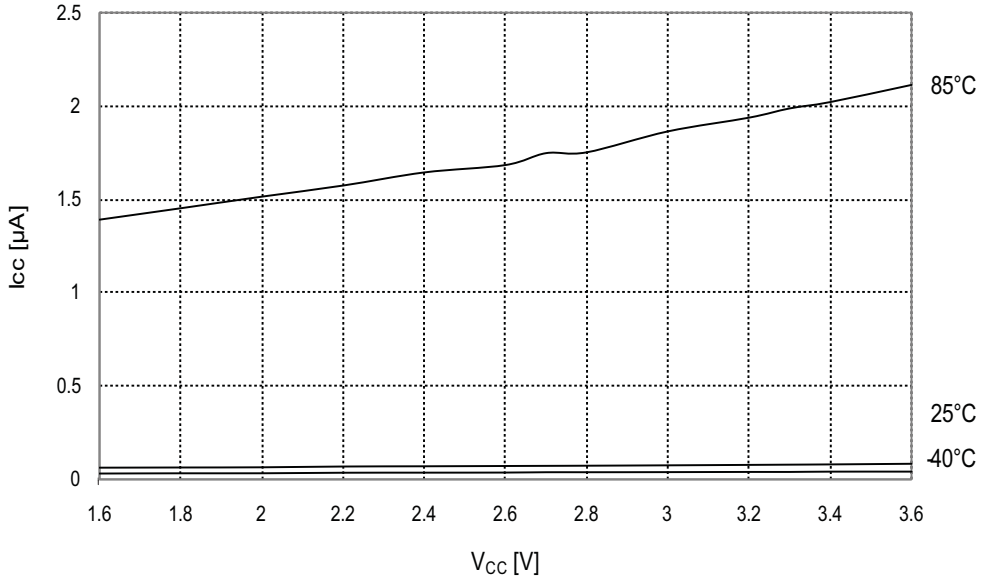
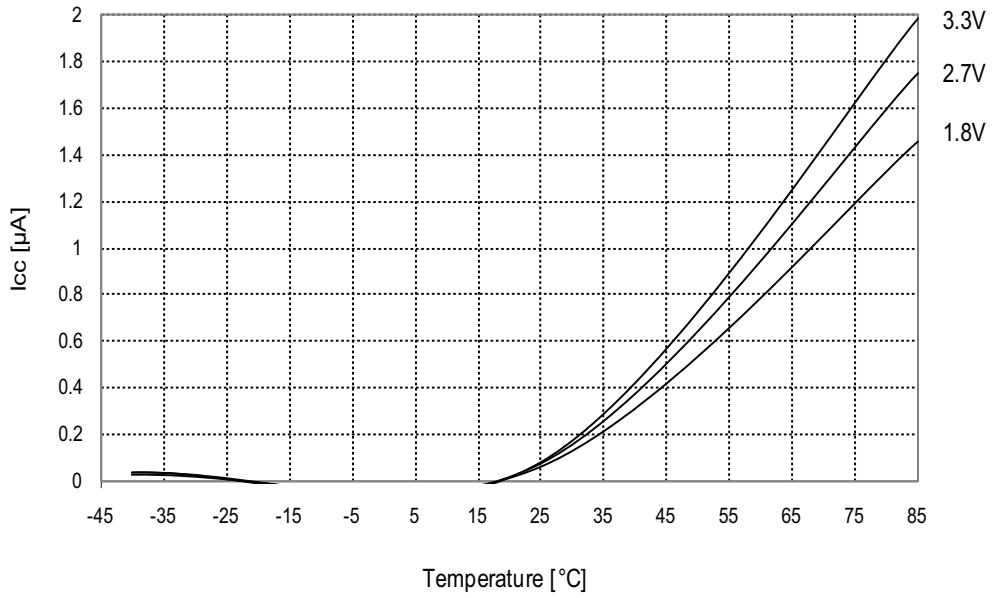


Figure 33-101. Power-down supply current vs. Temperature.

Watchdog and sampled BOD enabled and running from internal ULP oscillator.



33.3.2 I/O pin characteristics

The I/O pins complies with the JEDEC LVTTL and LVCMOS specification and the high- and low level input and output voltage limits reflect or exceed this specification.

33.3.2.1 Pull-up

Figure 33-102. I/O pin pull-up resistor current vs. input voltage.

V_{CC} = 1.8V.

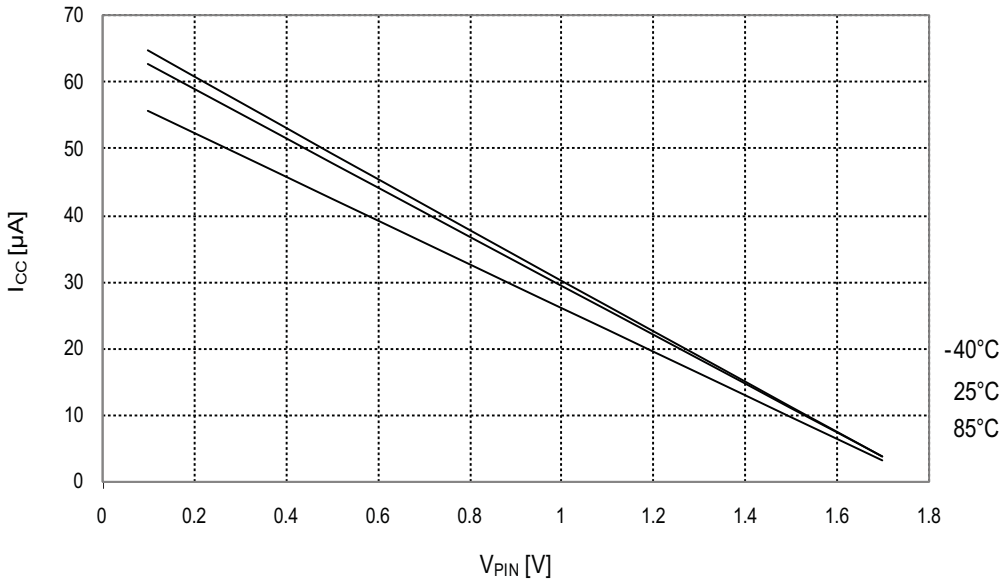


Figure 33-103. I/O pin pull-up resistor current vs. input voltage.
V_{CC} = 3.0V.

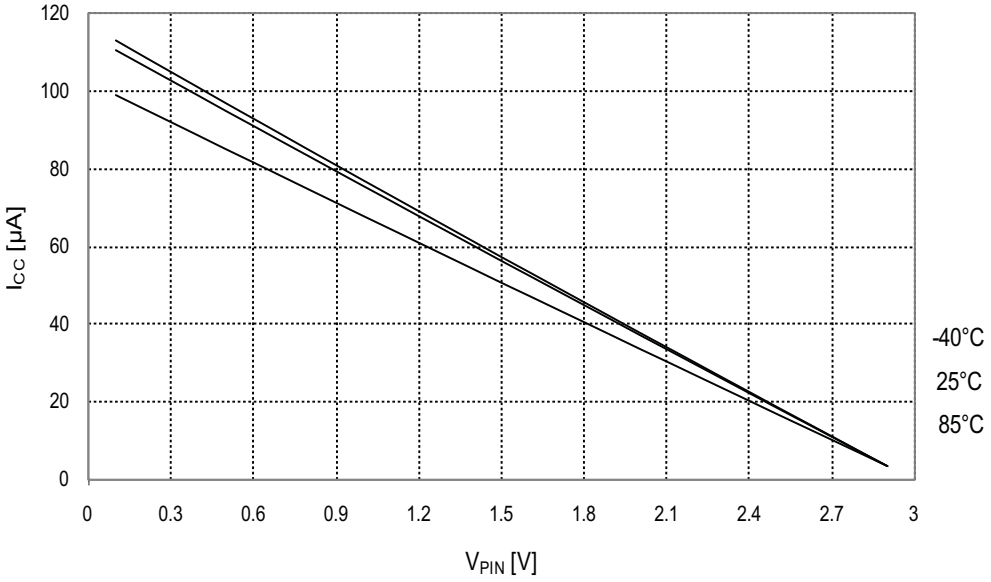
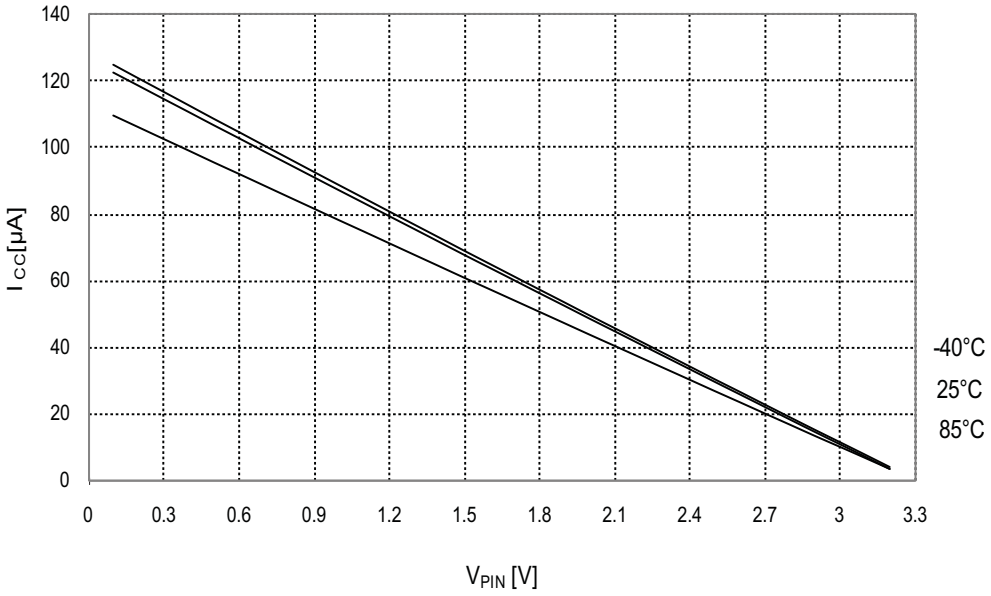


Figure 33-104. I/O pin pull-up resistor current vs. input voltage.
V_{CC} = 3.3V.



33.3.2.2 Output voltage vs. sink/source current

Figure 33-105. I/O pin output voltage vs. source current.
V_{CC} = 1.8V.

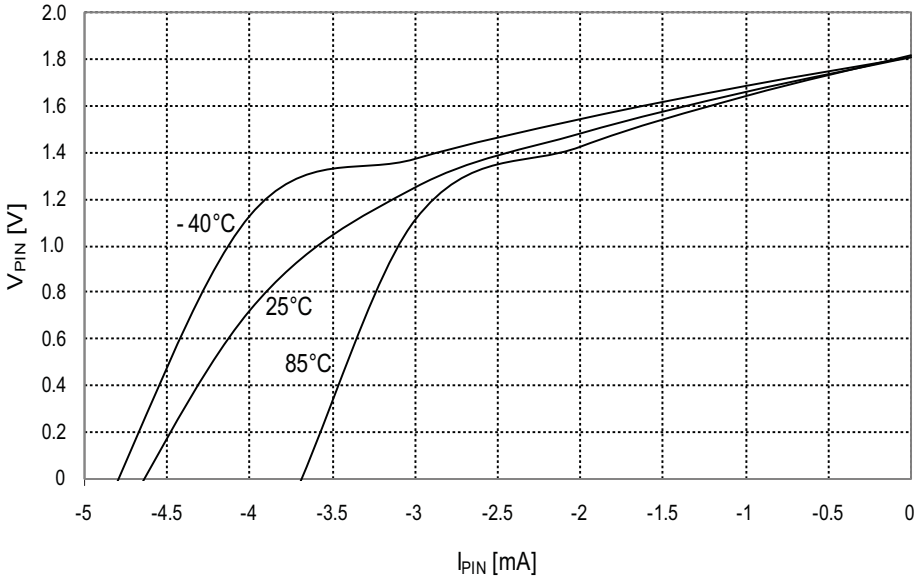


Figure 33-106. I/O pin output voltage vs. source current.
V_{CC} = 3.0V.

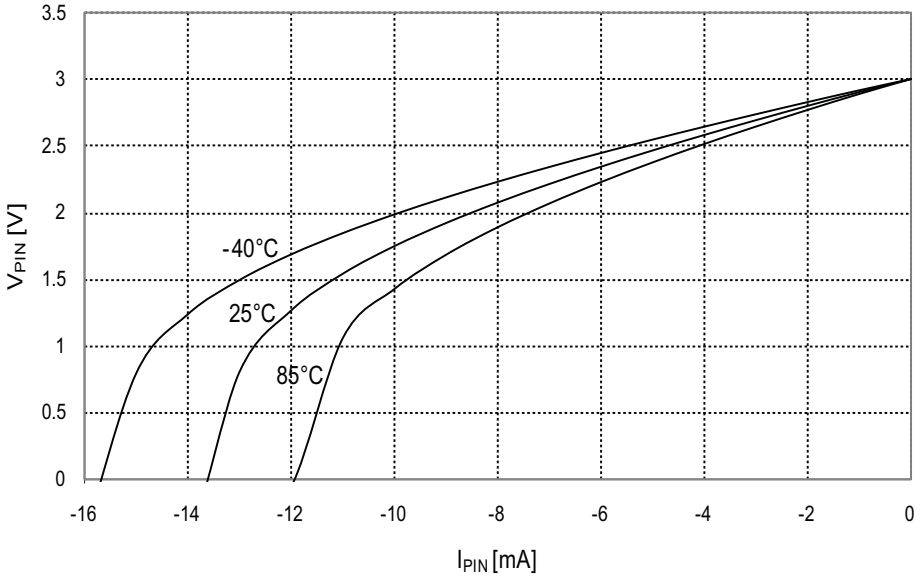


Figure 33-107. I/O pin output voltage vs. source current.

V_{CC} = 3.3V.

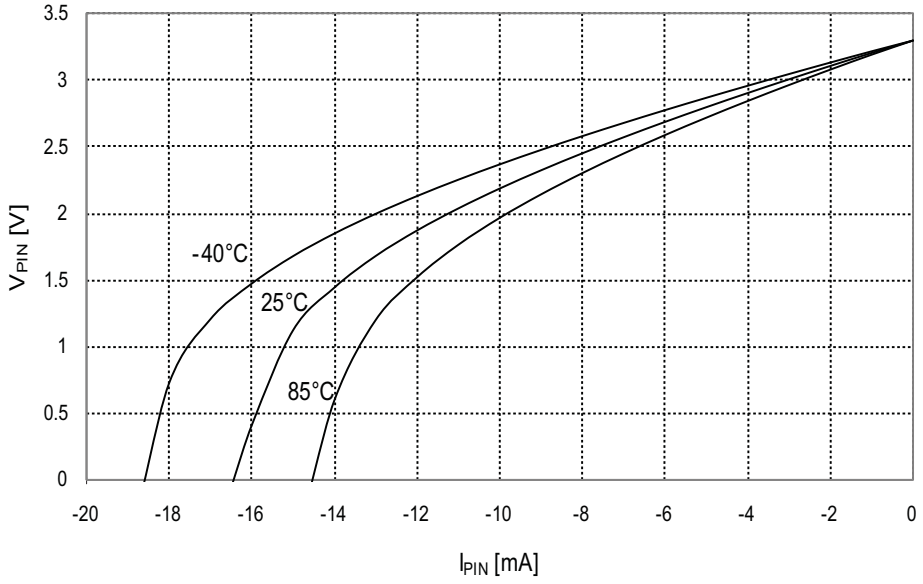


Figure 33-108. I/O pin output voltage vs. sink current.

V_{CC} = 1.8V.

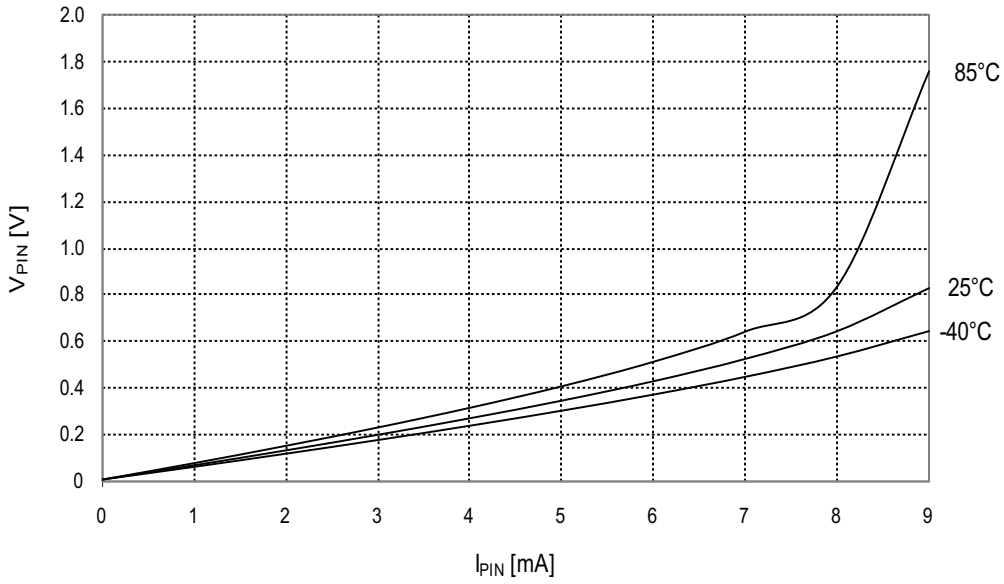


Figure 33-109. I/O pin output voltage vs. sink current.

V_{CC} = 3.0V.

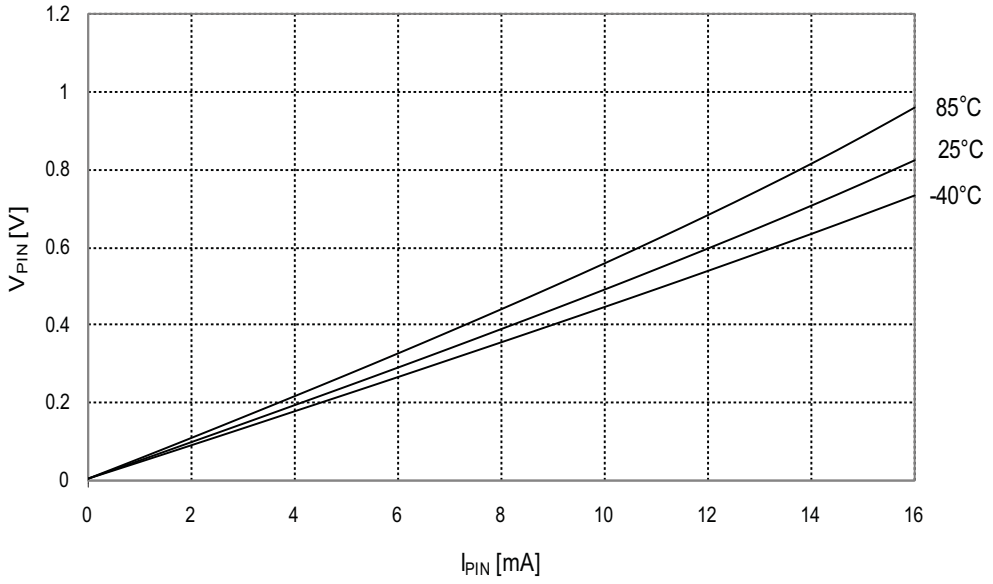
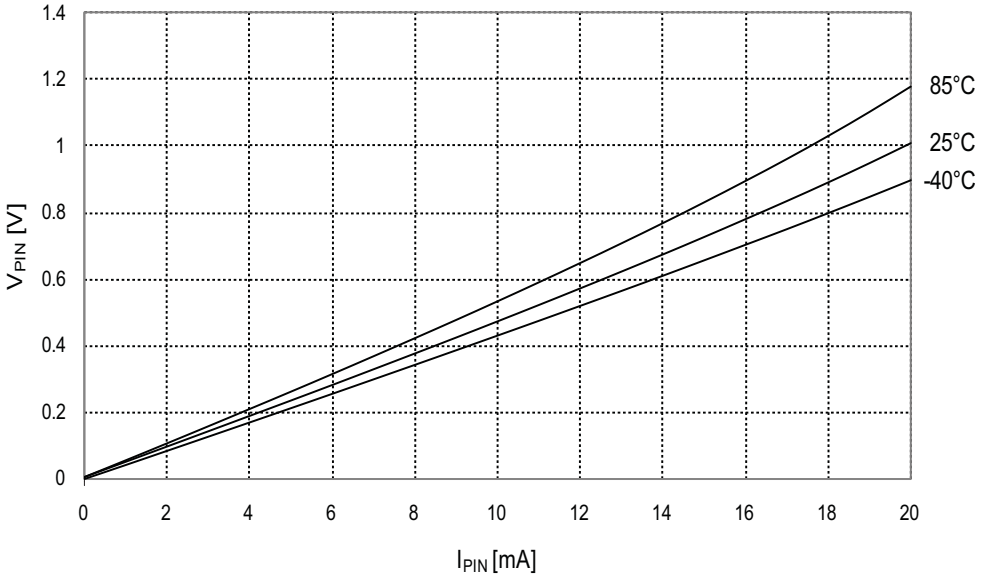


Figure 33-110. I/O pin output voltage vs. sink current.

V_{CC} = 3.3V.



33.3.2.3 Thresholds and hysteresis

Figure 33-111. I/O pin input threshold voltage vs. V_{CC}.
V_{IH} I/O pin read as "1".

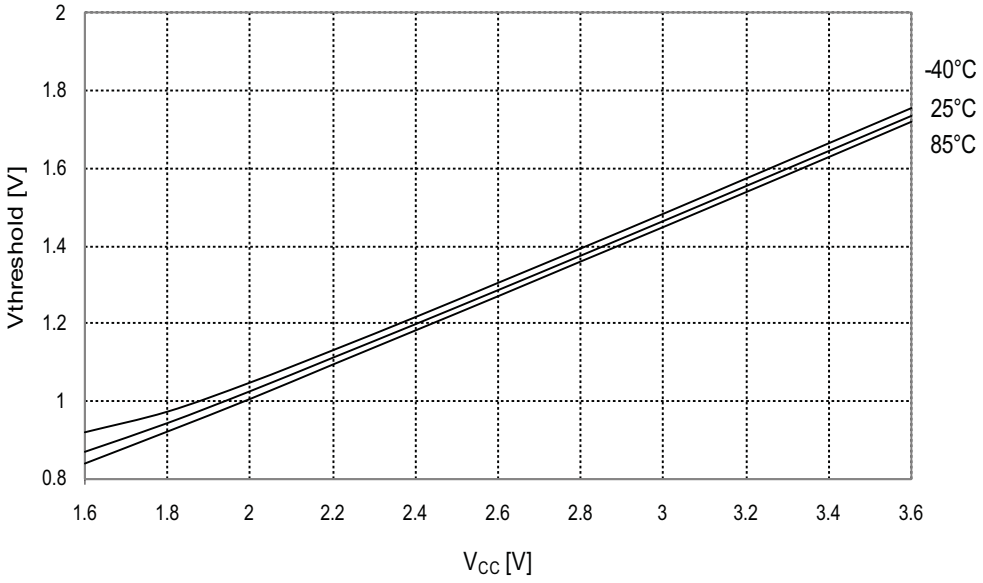


Figure 33-112. I/O pin input threshold voltage vs. V_{CC}.
V_{IL} I/O pin read as "0".

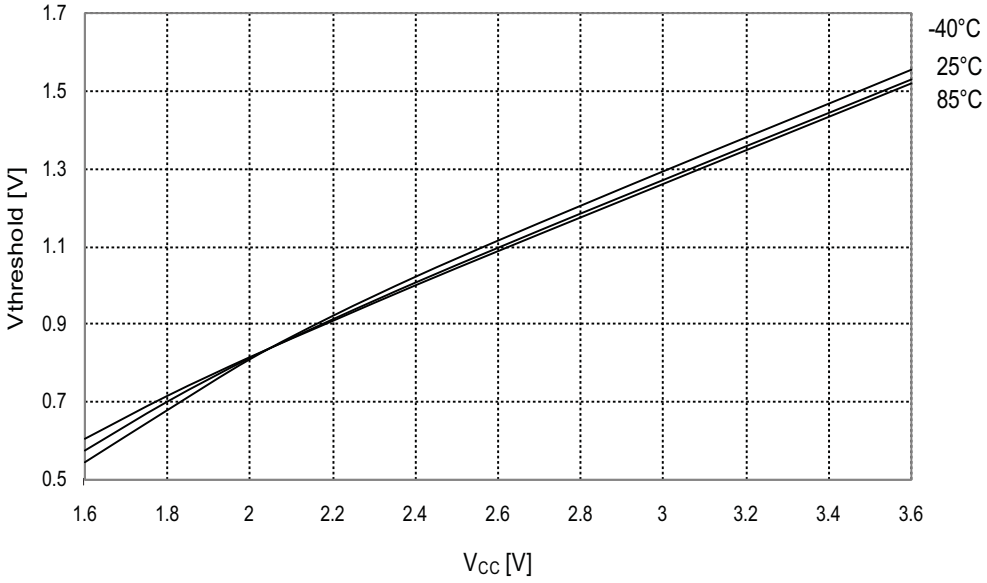
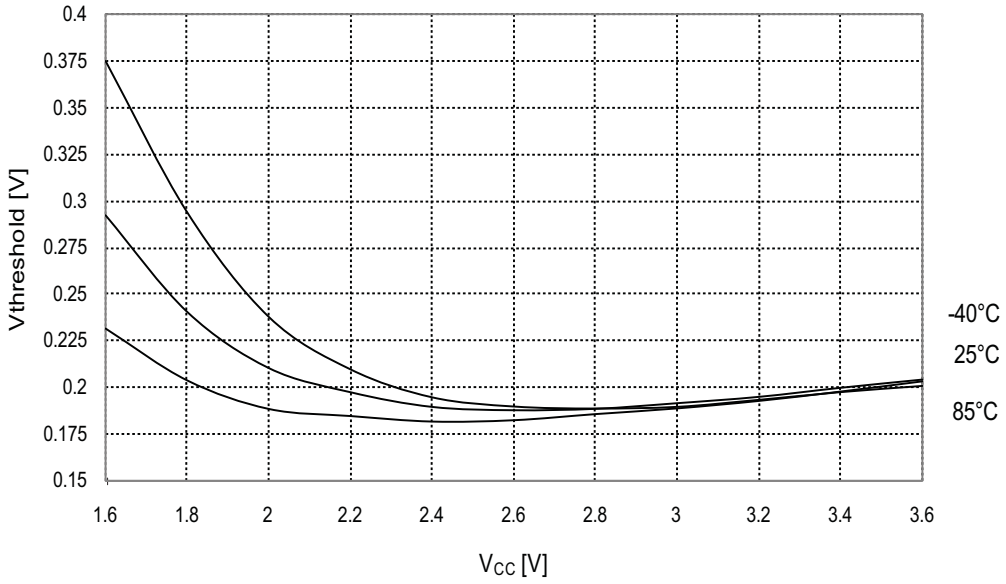


Figure 33-113. I/O pin input hysteresis vs. V_{CC}.



33.3.3 ADC characteristics

Figure 33-114. INL error vs. external V_{REF}.

T = 25°C, V_{CC} = 3.6V, external reference.

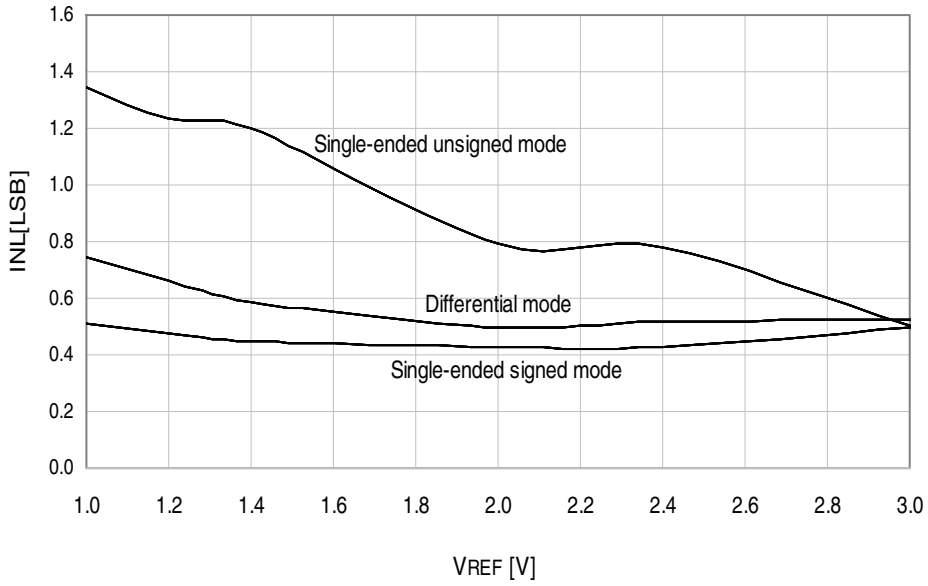


Figure 33-115. INL error vs. sample rate.

T = 25°C, V_{CC} = 3.6V, V_{REF} = 3.0V external.

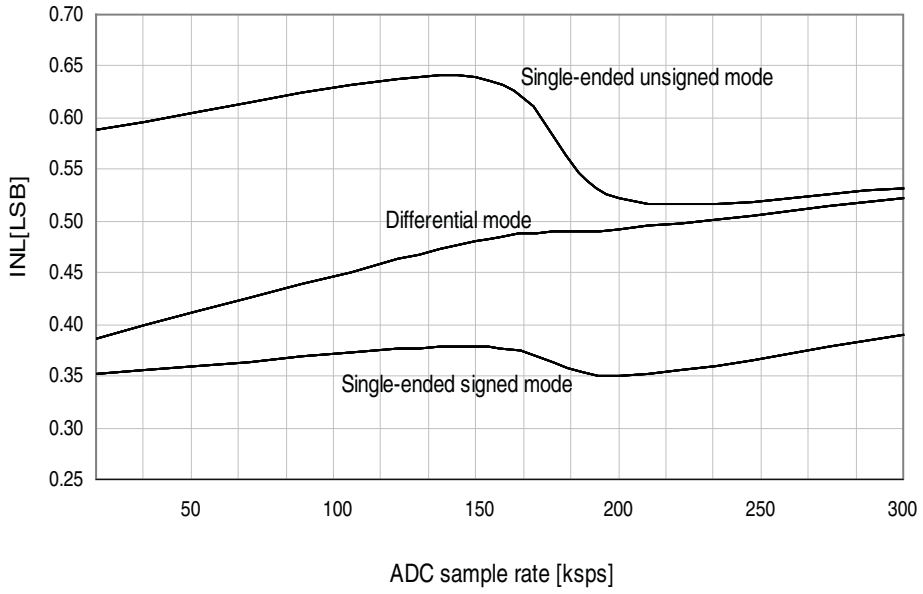


Figure 33-116. INL error vs. input code.

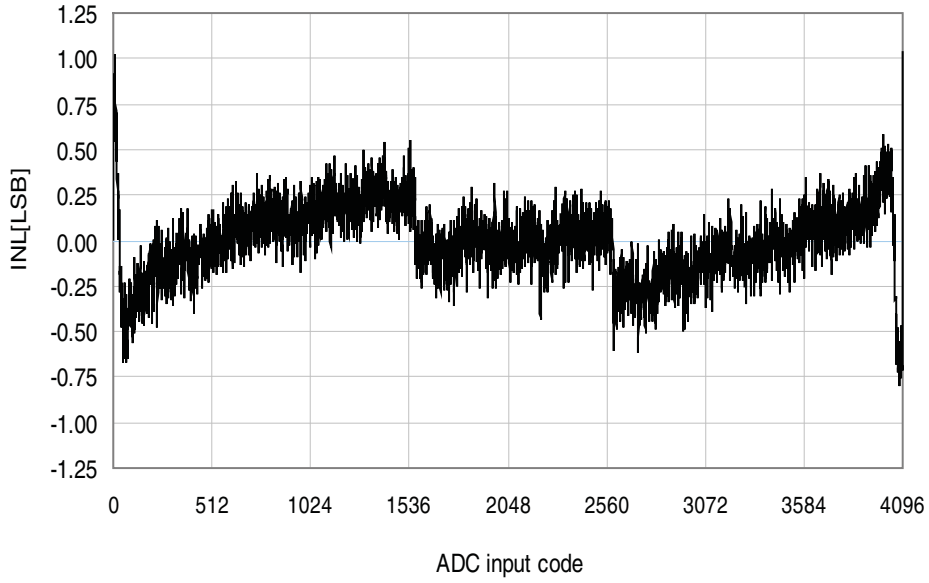


Figure 33-117. DNL error vs. external V_{REF}.

T = 25°C, V_{CC} = 3.6V, external reference.

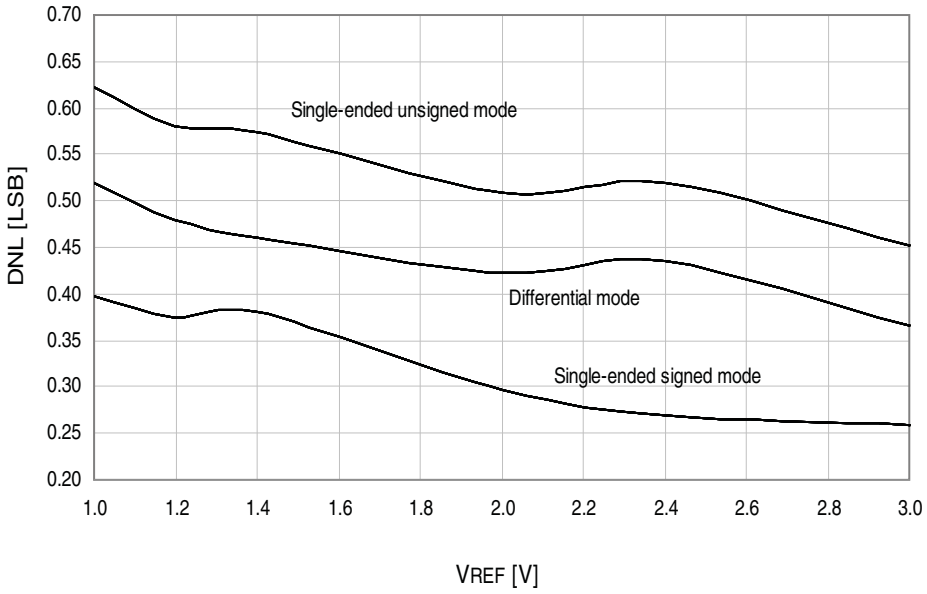


Figure 33-118. I/O pin input threshold voltage vs. V_{CC}.

T = 25°C, V_{CC} = 3.6V, V_{REF} = 3.0V external.

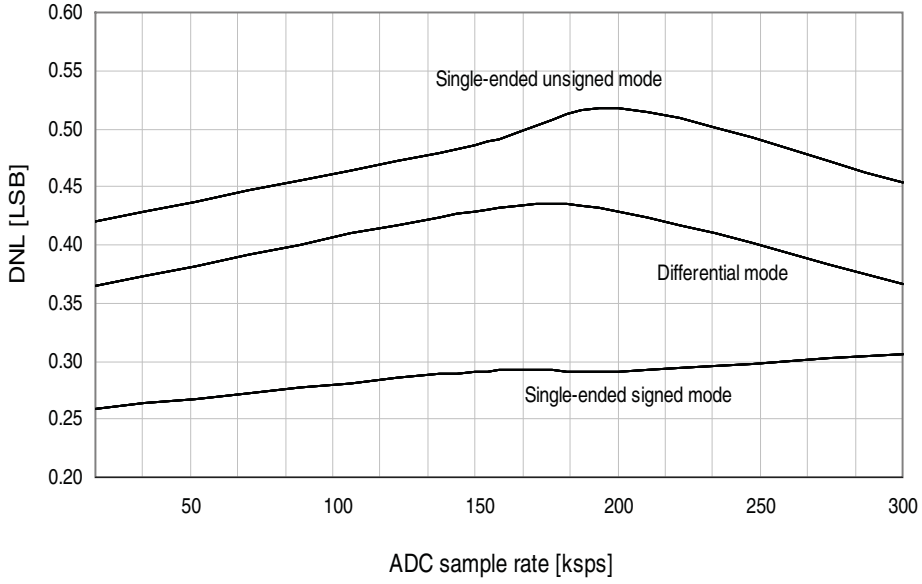


Figure 33-119. DNL error vs. input code.

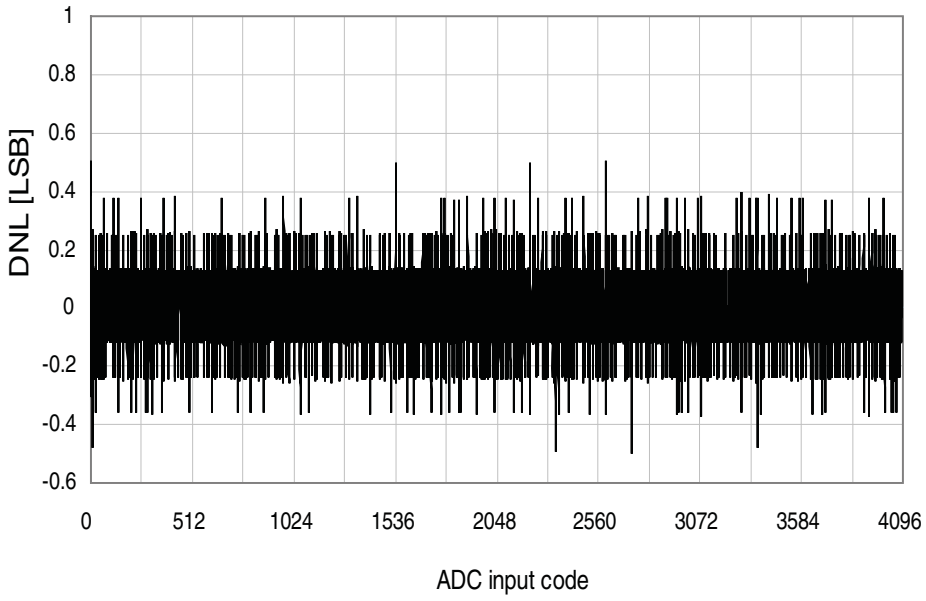


Figure 33-120. Gain error vs. V_{REF}.

T = 25°C, V_{CC} = 3.6V, ADC sample rate = 300ksps.

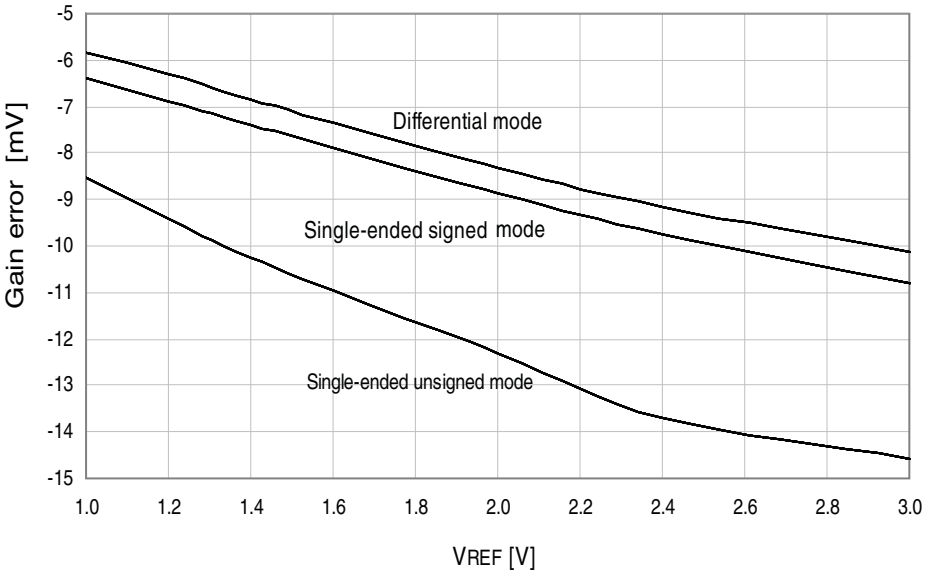


Figure 33-121. Gain error vs. V_{CC}.

T = 25°C, V_{REF} = external 1.0V, ADC sample rate = 300ksps.

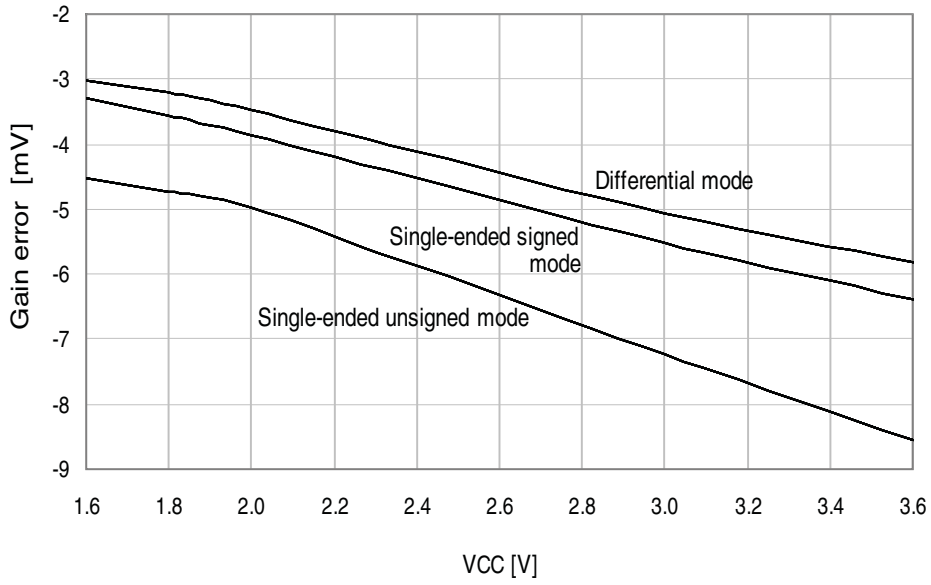


Figure 33-122. Offset error vs. V_{REF}.

T = 25°C, V_{CC} = 3.6V, ADC sample rate = 300ksps.

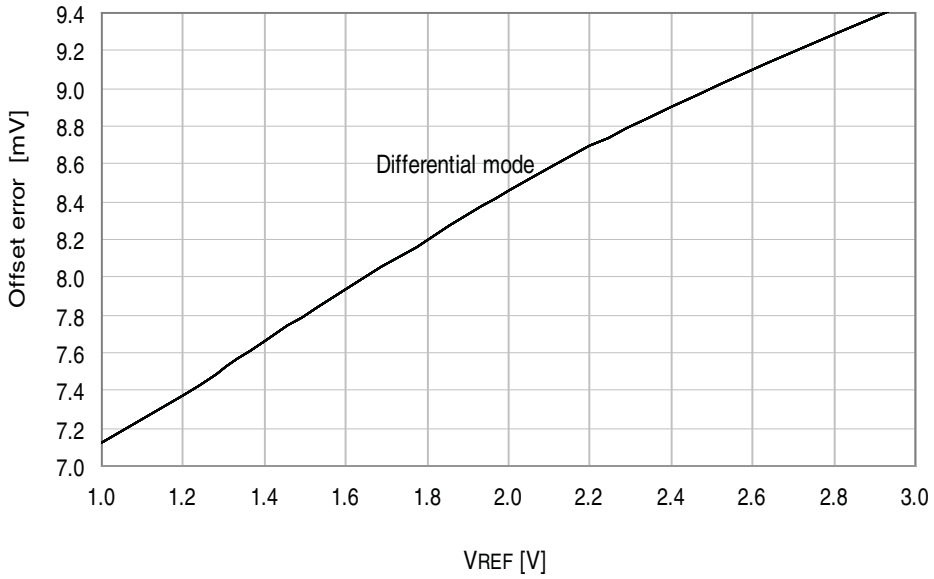


Figure 33-123. Gain error vs. temperature.

V_{CC} = 3.0V, V_{REF} = external 2.0V.

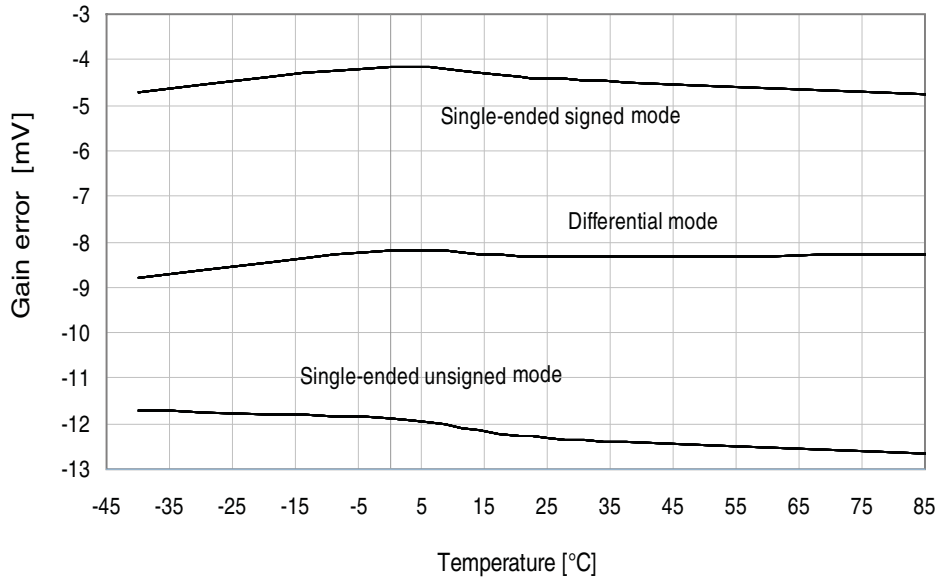
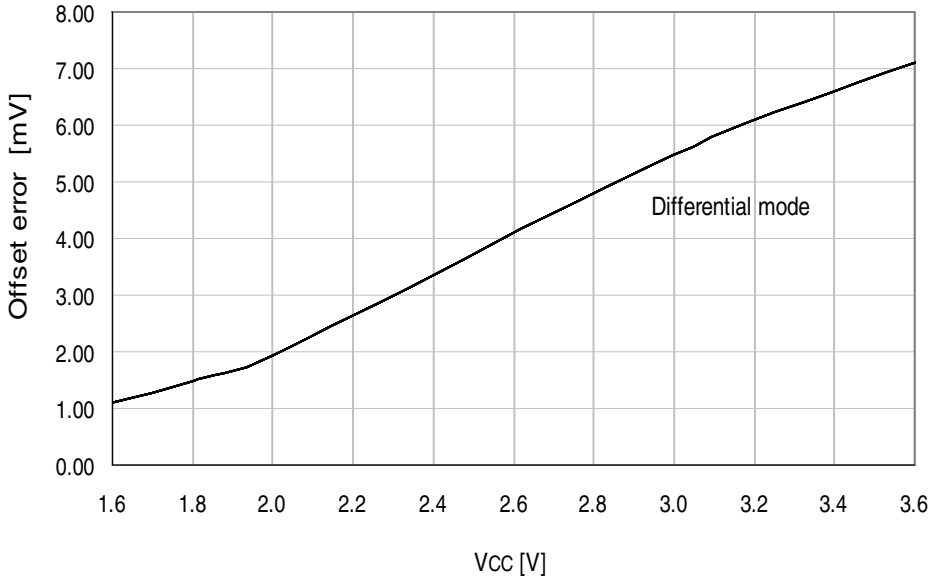


Figure 33-124. Offset error vs. V_{CC}.

T = 25°C, V_{REF} = external 1.0V, ADC sample rate = 300ksps.



33.3.4 Analog Comparator characteristics

Figure 33-125. Analog comparator hysteresis vs. V_{CC}.
Small hysteresis.

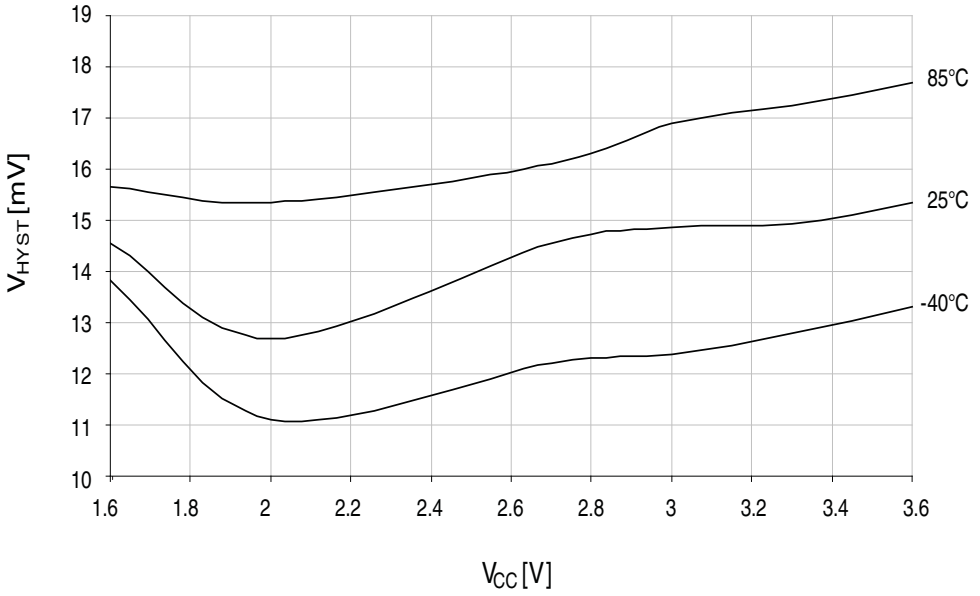


Figure 33-126. Analog comparator hysteresis vs. V_{CC}.
Large hysteresis.

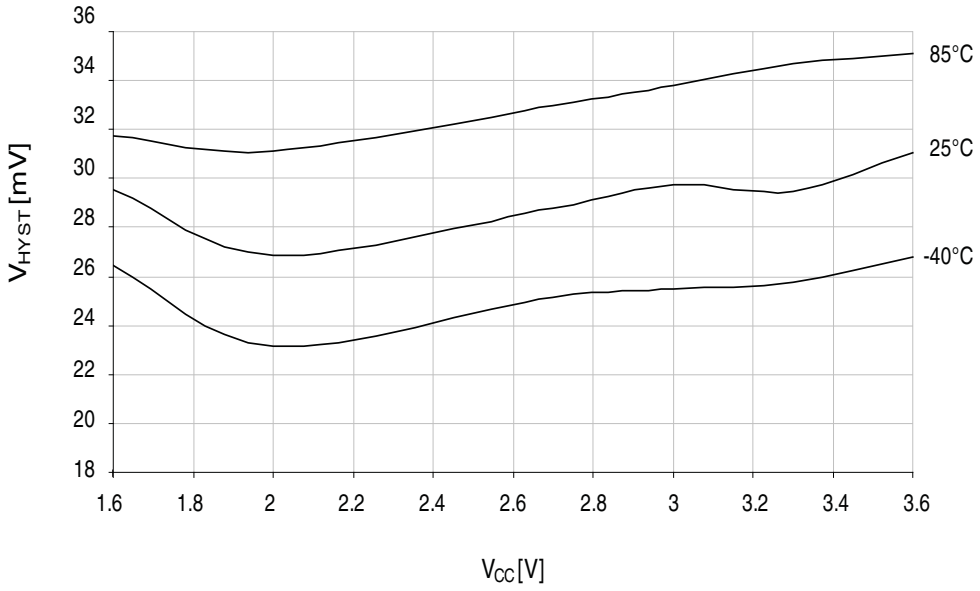


Figure 33-127. Analog comparator current source vs. calibration value.

V_{CC} = 3.0V.

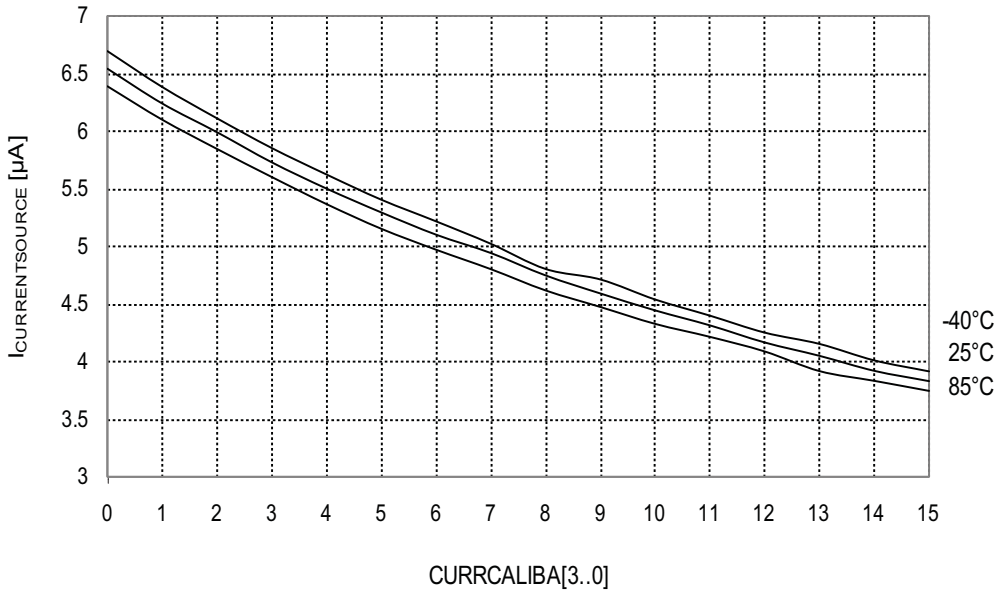
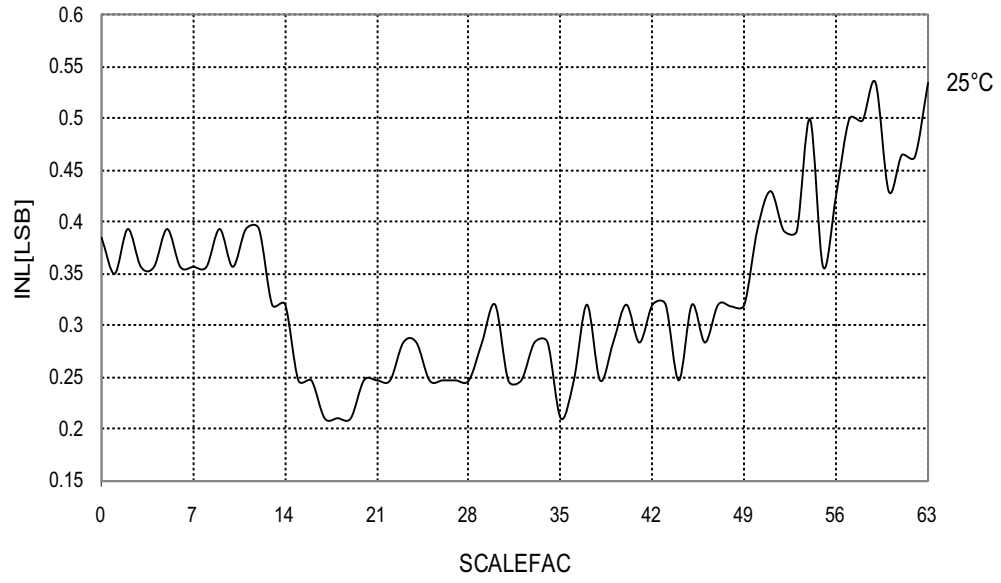


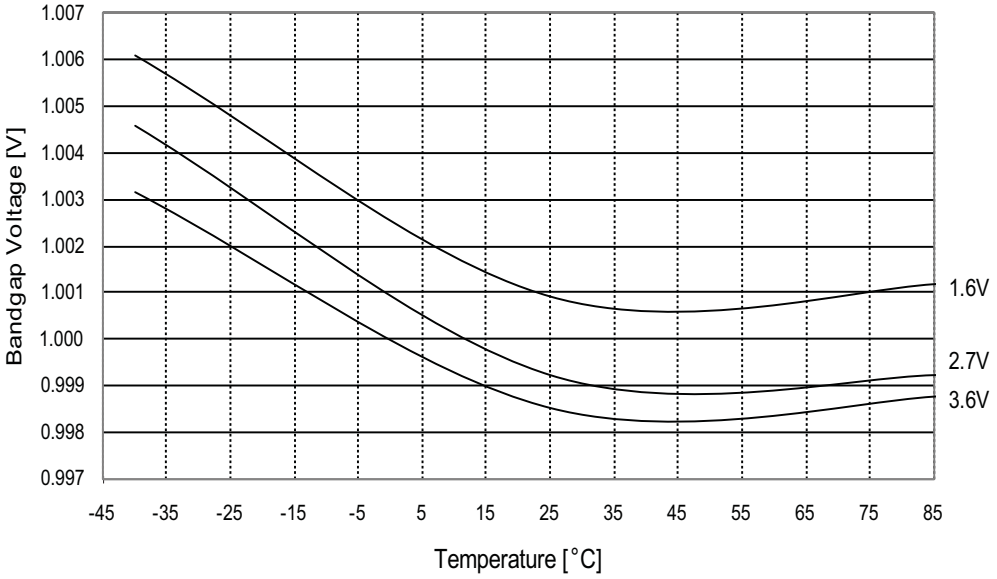
Figure 33-128. Voltage scaler INL vs. SCALEFAC.

T = 25°C, V_{CC} = 3.0V.



33.3.5 Internal 1.0V reference characteristics

Figure 33-129. ADC internal 1.0V reference vs. temperature.



33.3.6 BOD characteristics

Figure 33-130. BOD thresholds vs. temperature.
BOD level = 1.6V.

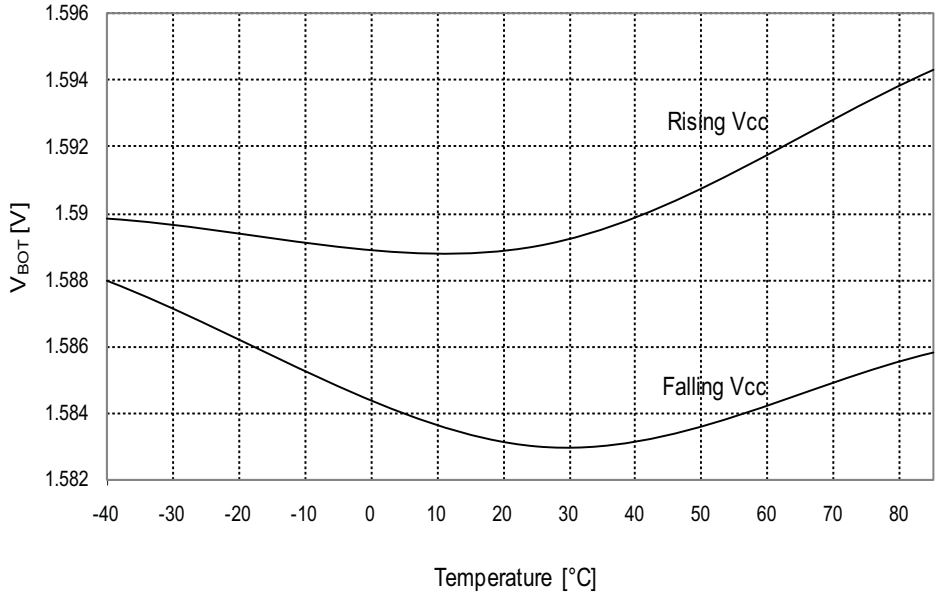
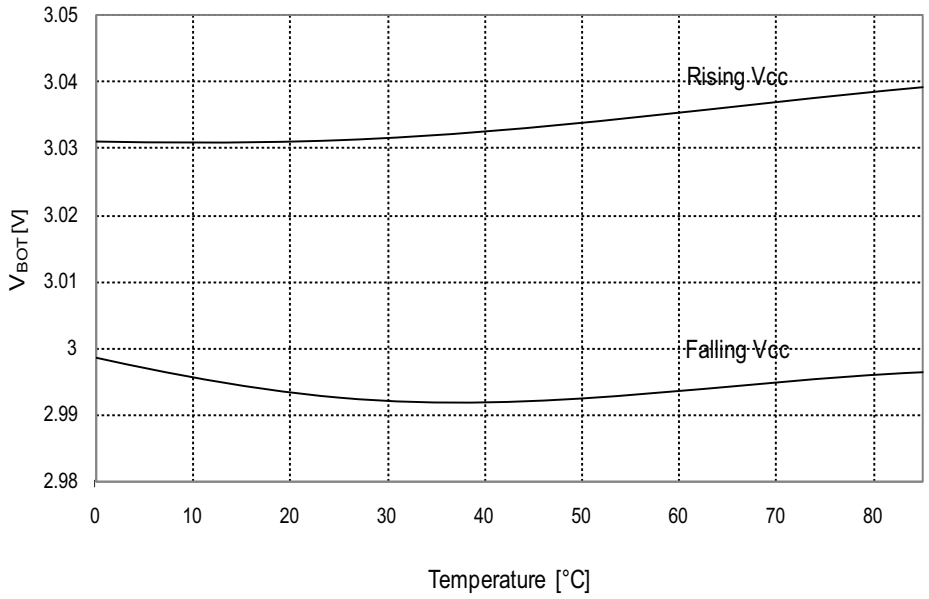


Figure 33-131. BOD thresholds vs. temperature.

BOD level = 3.0V.



33.3.7 External reset characteristics

Figure 33-132. Minimum reset pin pulse width vs. V_{CC}.

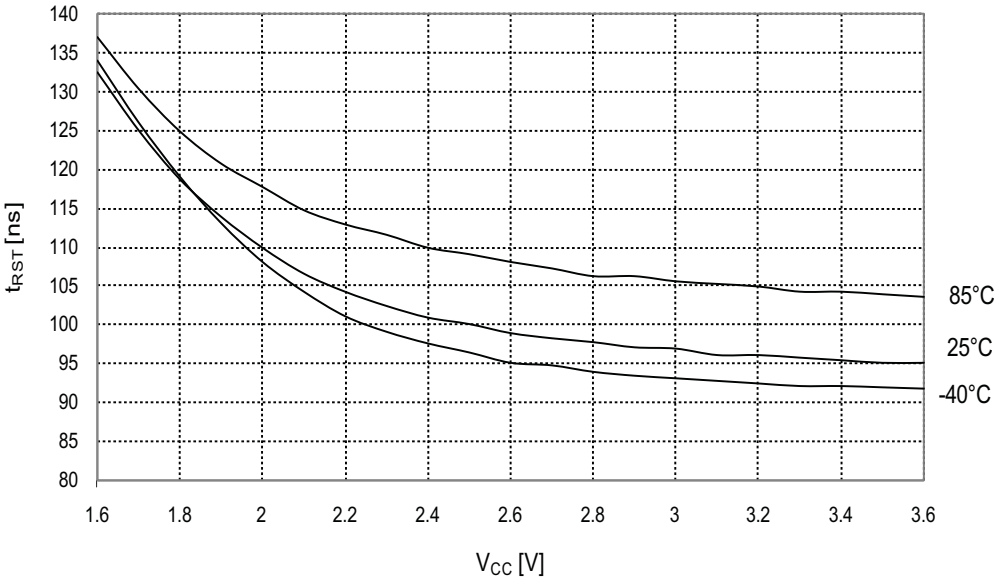


Figure 33-133. Reset pin pull-up resistor current vs. reset pin voltage.
V_{CC} = 1.8V.

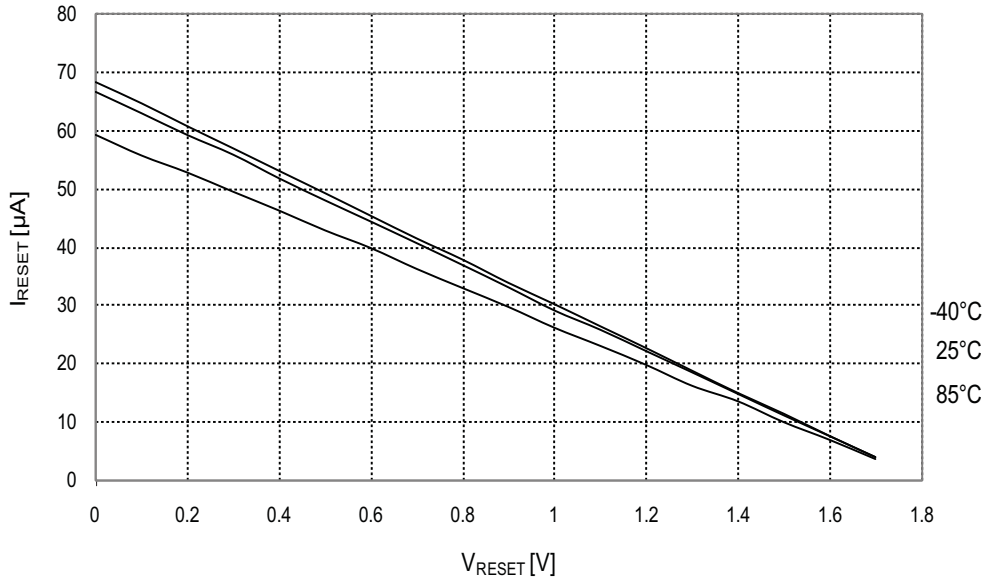


Figure 33-134. Reset pin pull-up resistor current vs. reset pin voltage.
V_{CC} = 3.0V.

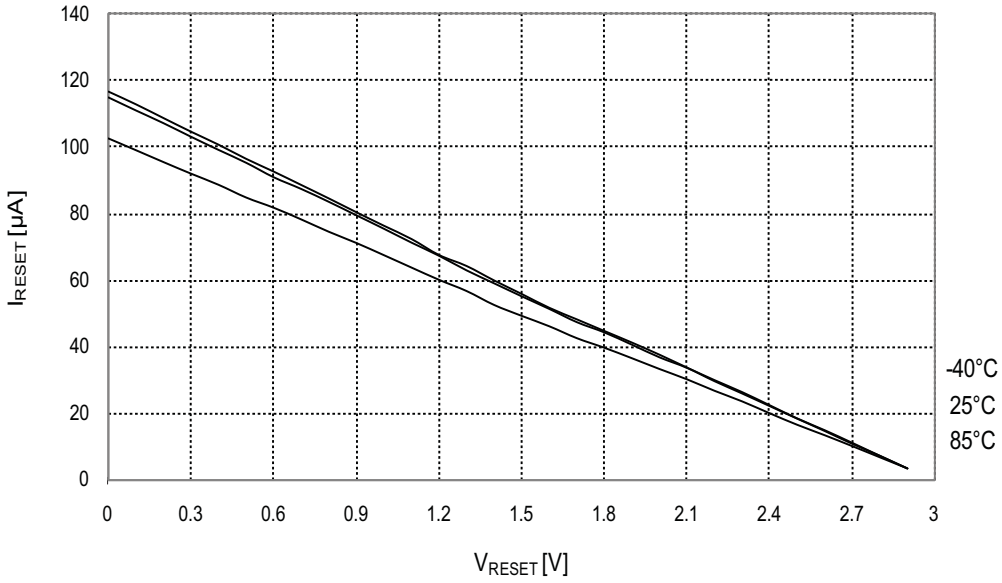


Figure 33-135. Reset pin pull-up resistor current vs. reset pin voltage.

V_{CC} = 3.3V.

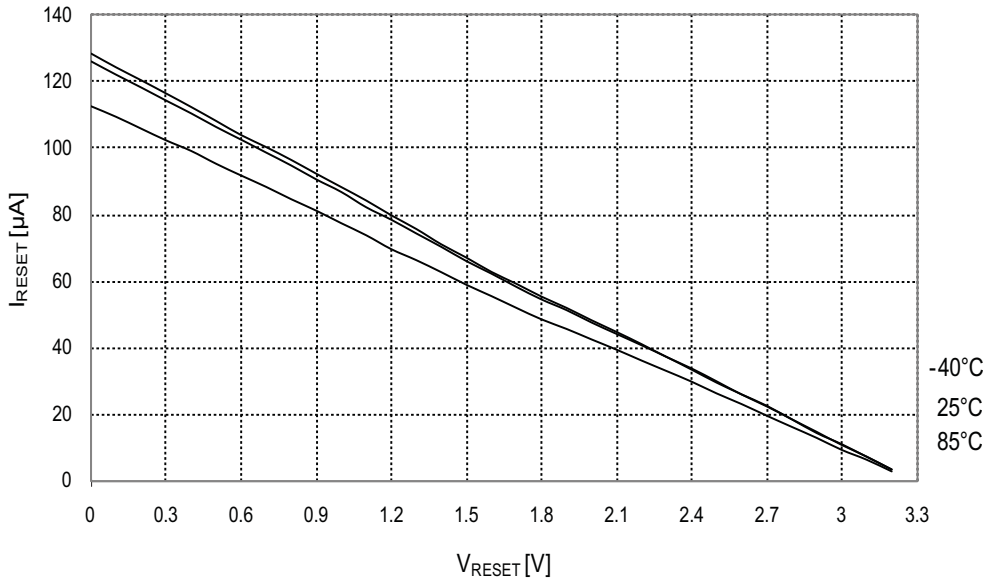
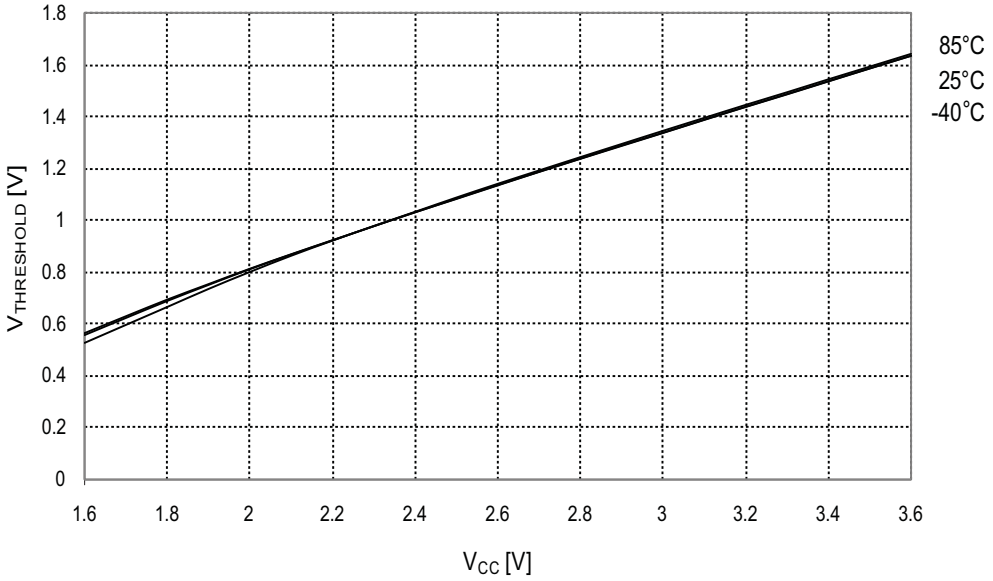


Figure 33-136. Reset pin input threshold voltage vs. V_{CC}.

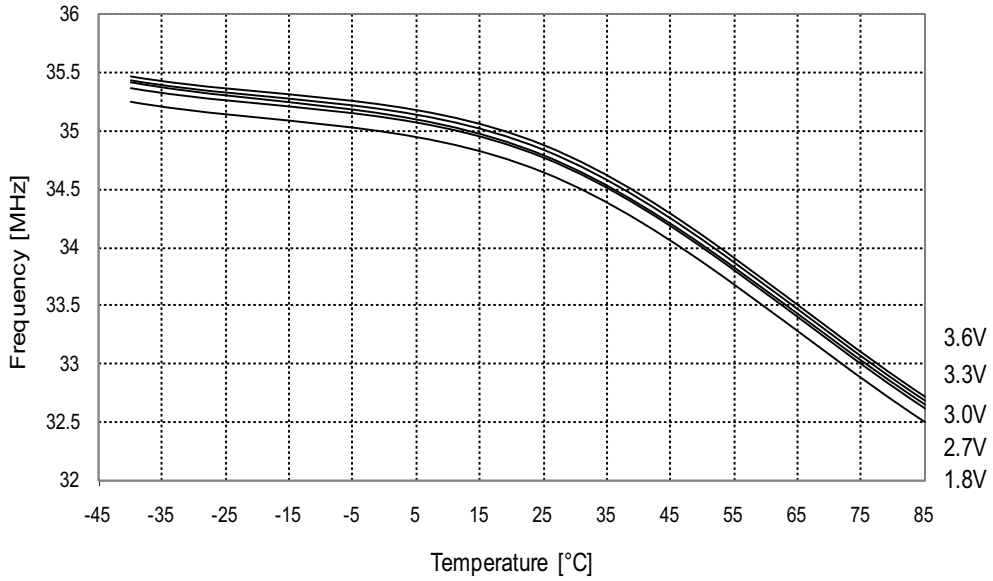
V_{IH} - Reset pin read as "1".



33.3.8 Oscillator characteristics

33.3.8.1 Ultra low-power internal oscillator

Figure 33-137. Ultra low-power internal oscillator frequency vs. temperature.



33.3.8.2 32.768kHz internal oscillator

Figure 33-138. 32.768kHz internal oscillator frequency vs. temperature.

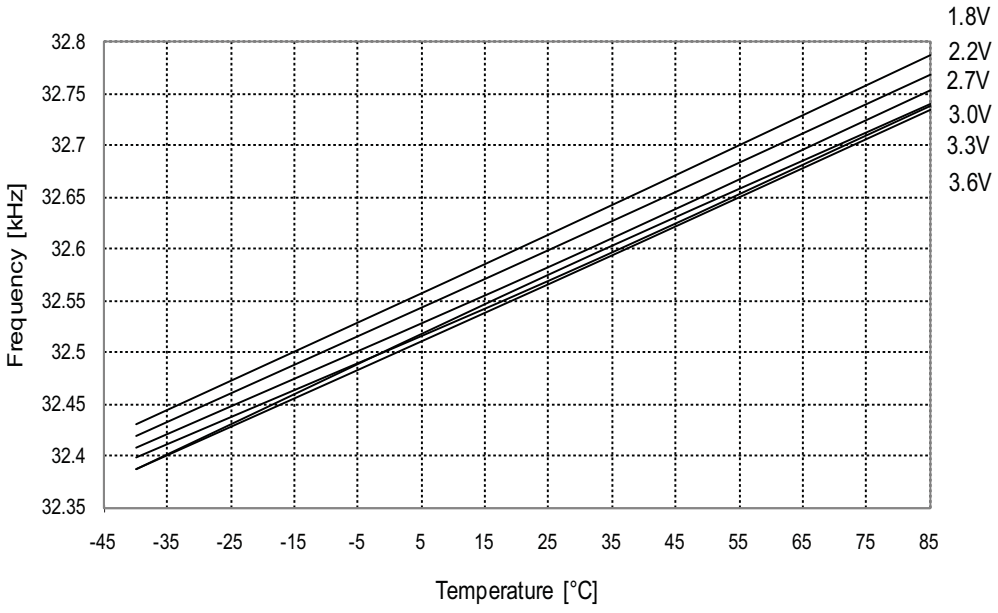
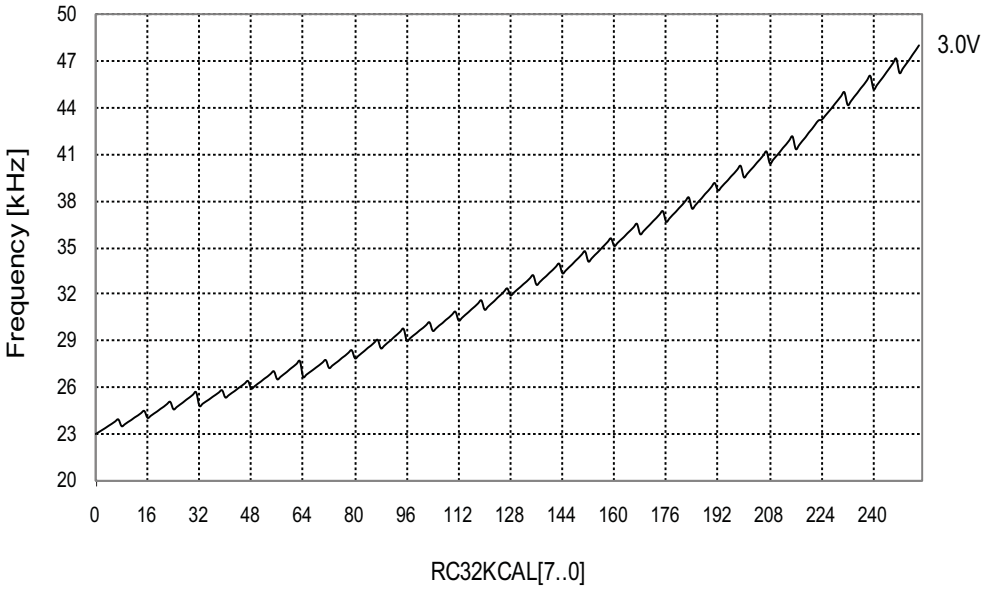


Figure 33-139. 32.768kHz internal oscillator frequency vs. calibration value.

V_{CC} = 3.0V, T = 25°C.



33.3.8.3 2MHz internal oscillator

Figure 33-140. 2MHz internal oscillator frequency vs. temperature.

DFLL disabled.

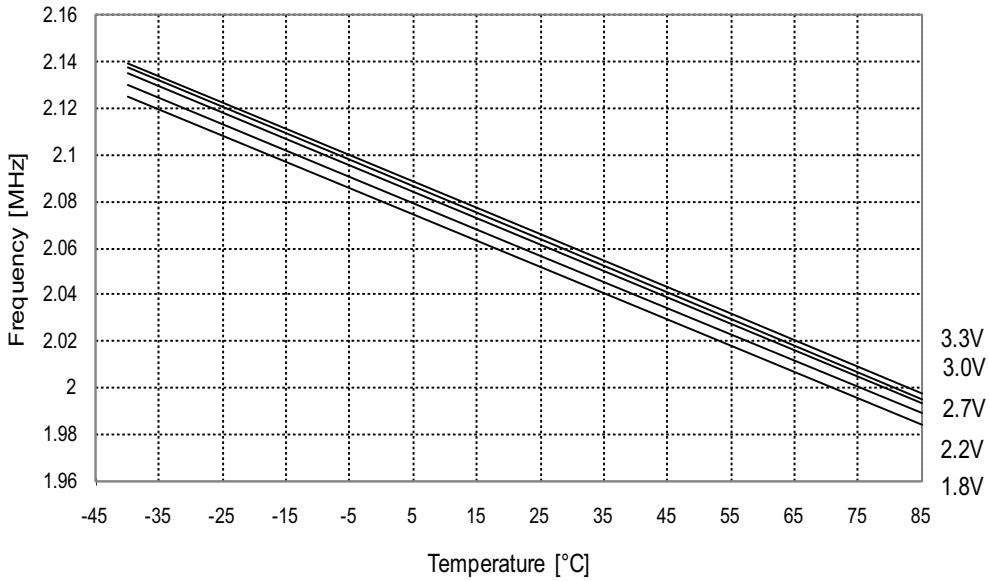


Figure 33-141. 2MHz internal oscillator frequency vs. temperature.

DFLL enabled, from the 32.678kHz internal oscillator.

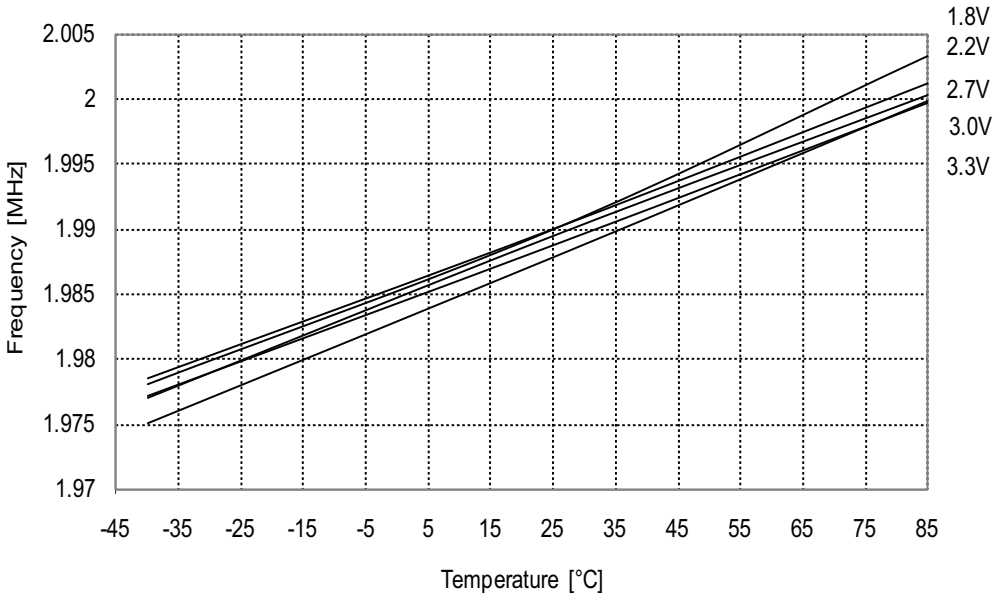
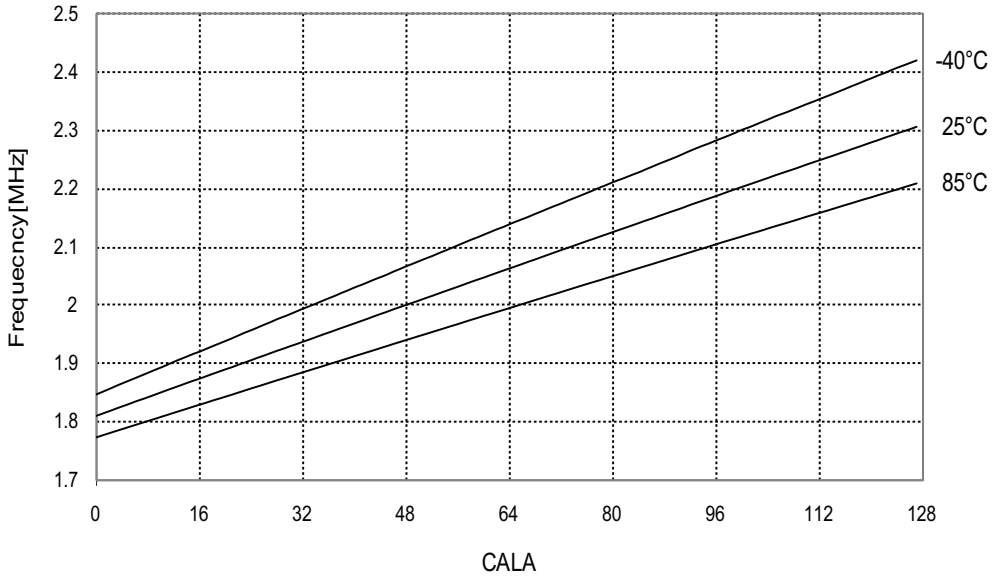


Figure 33-142. 2MHz internal oscillator frequency vs. CALA calibration value.

V_{CC} = 3.0V.



33.3.8.4 32MHz internal oscillator

Figure 33-143. 32MHz internal oscillator frequency vs. temperature.
DFLL disabled.

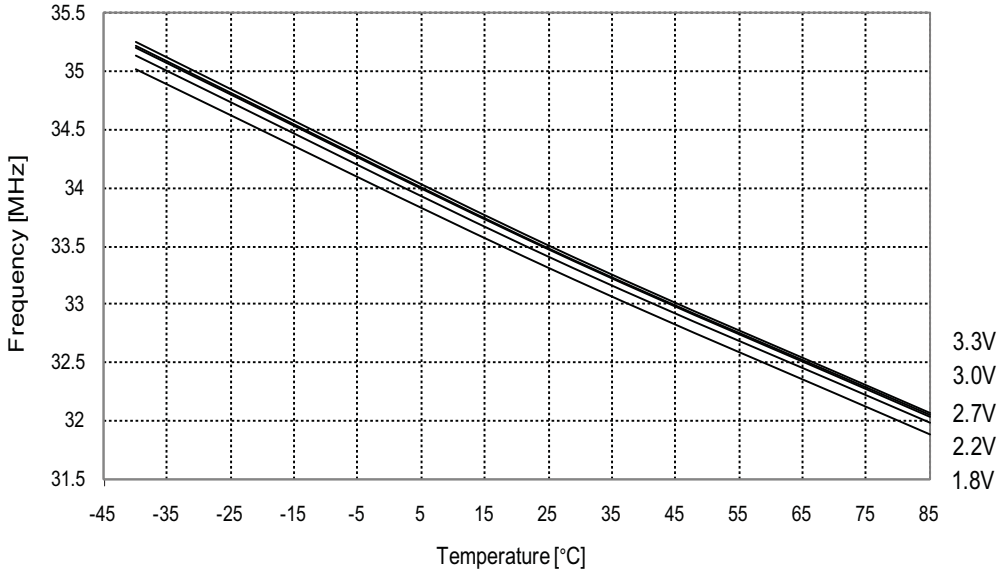


Figure 33-144. 32MHz internal oscillator frequency vs. temperature.
DFLL enabled, from the 32.678kHz internal oscillator.

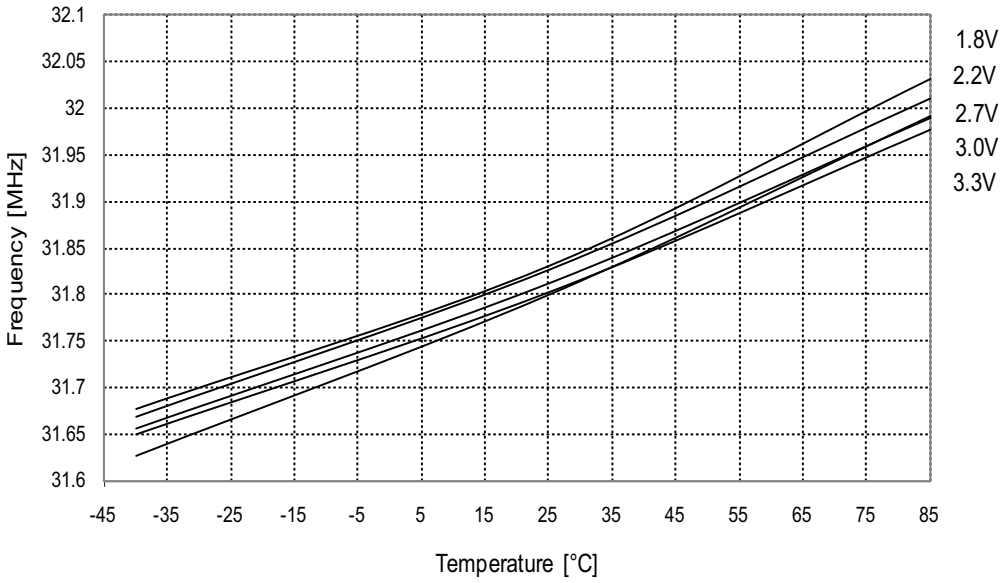


Figure 33-145. 32MHz internal oscillator CALA calibration step value.

V_{CC} = 3.0V.

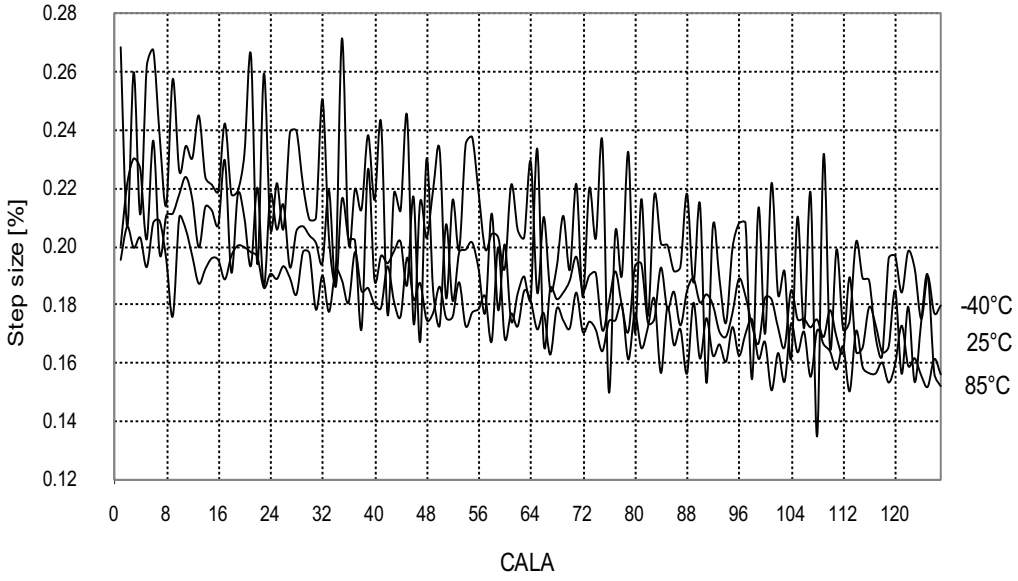
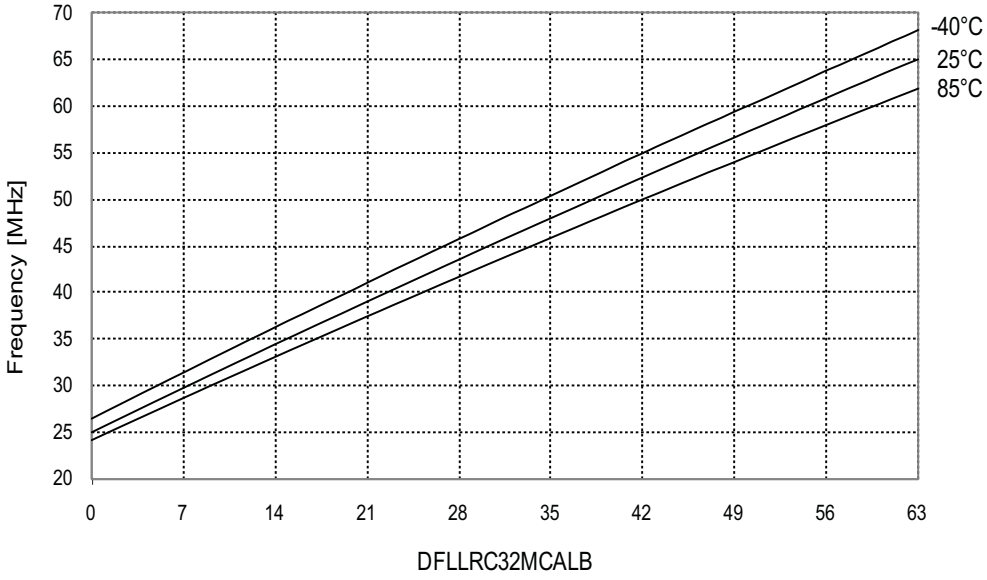


Figure 33-146. 32MHz internal oscillator frequency vs. CALB calibration step value.

V_{CC} = 3.0V.



33.3.8.5 32MHz internal oscillator calibrated to 48MHz

Figure 33-147. 48MHz internal oscillator frequency vs. temperature.
DFLL disabled.

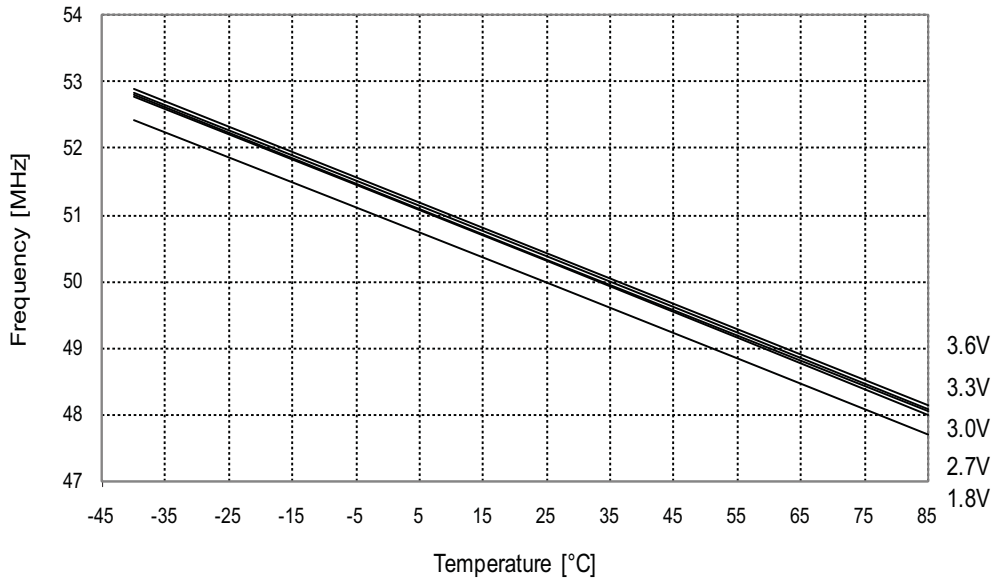
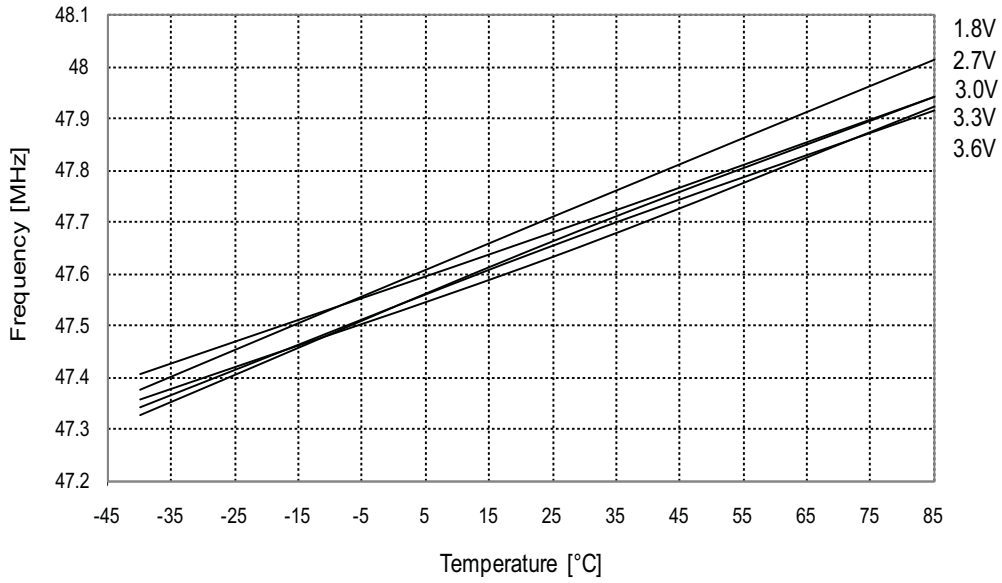


Figure 33-148. 48MHz internal oscillator frequency vs. temperature.
DFLL enabled, from the 32.678kHz internal oscillator.



33.3.9 Two-wire interface characteristics

Figure 33-149. SDA hold time vs. temperature.

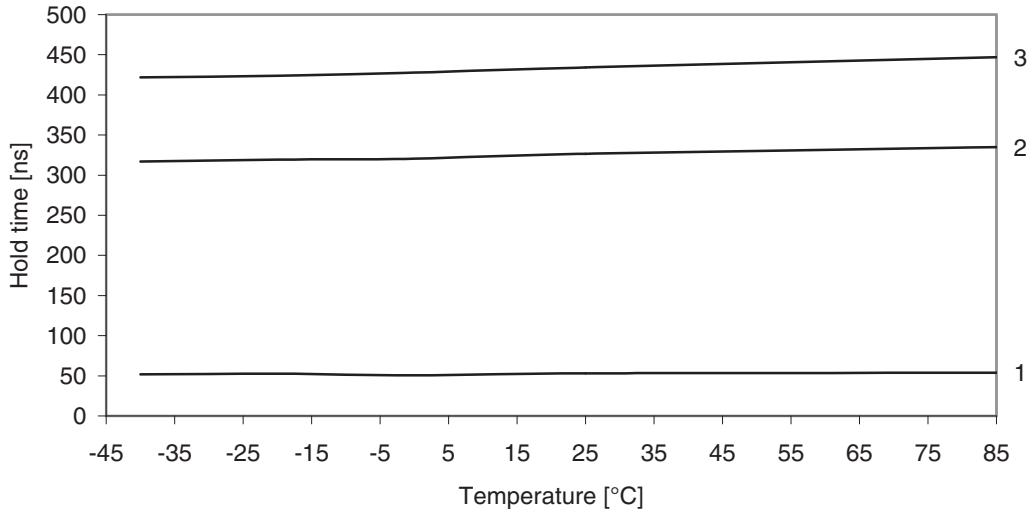
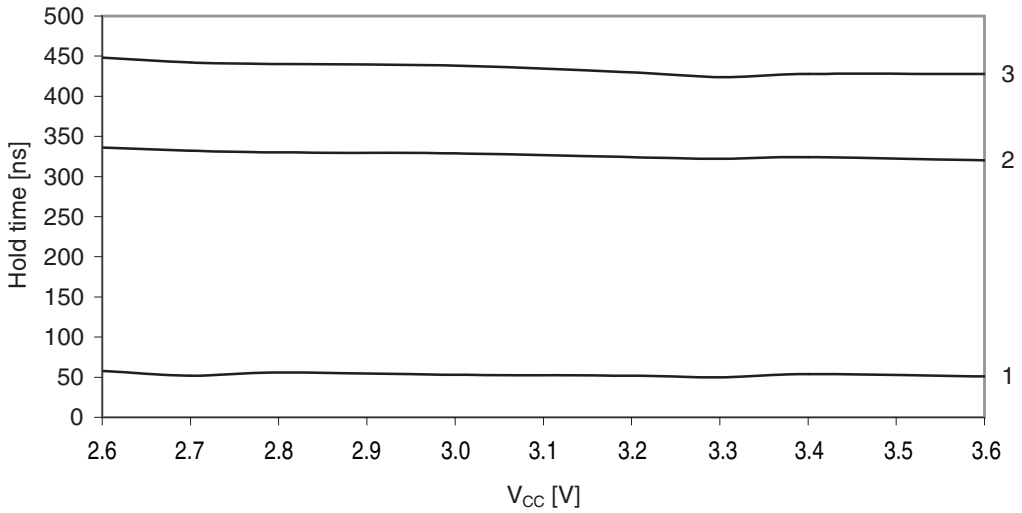
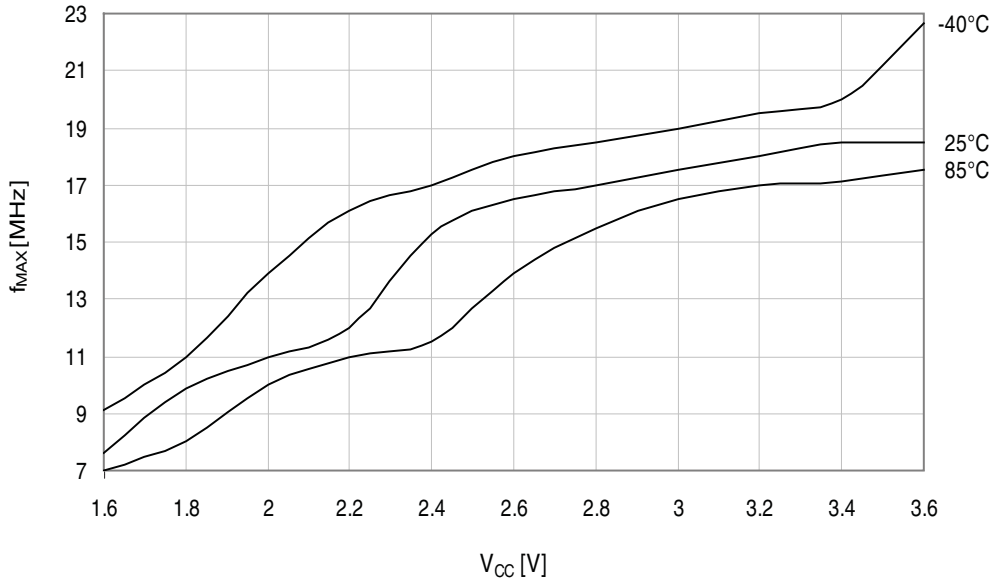


Figure 33-150. SDA hold time vs. supply voltage.



33.3.10 PDI characteristics

Figure 33-151. Maximum PDI frequency vs. V_{CC}.



33.4 Atmel ATxmega192D3

33.4.1 Current consumption

33.4.1.1 Active mode supply current

Figure 33-152. Active supply current vs. frequency.
f_{SYS} = 0 - 1MHz external clock, T = 25°C.

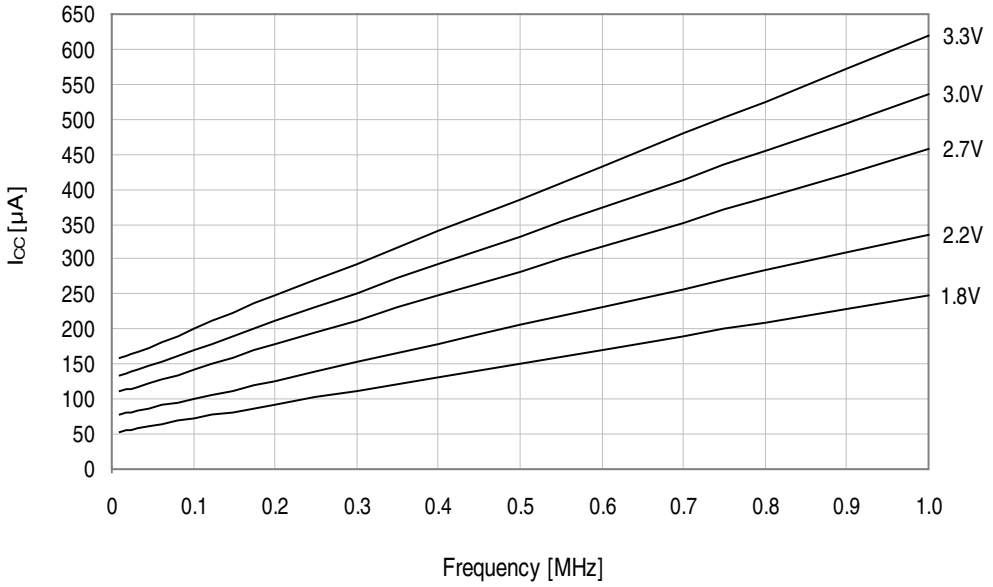


Figure 33-153. Active supply current vs. frequency.
f_{SYS} = 1 - 32MHz external clock, T = 25°C.

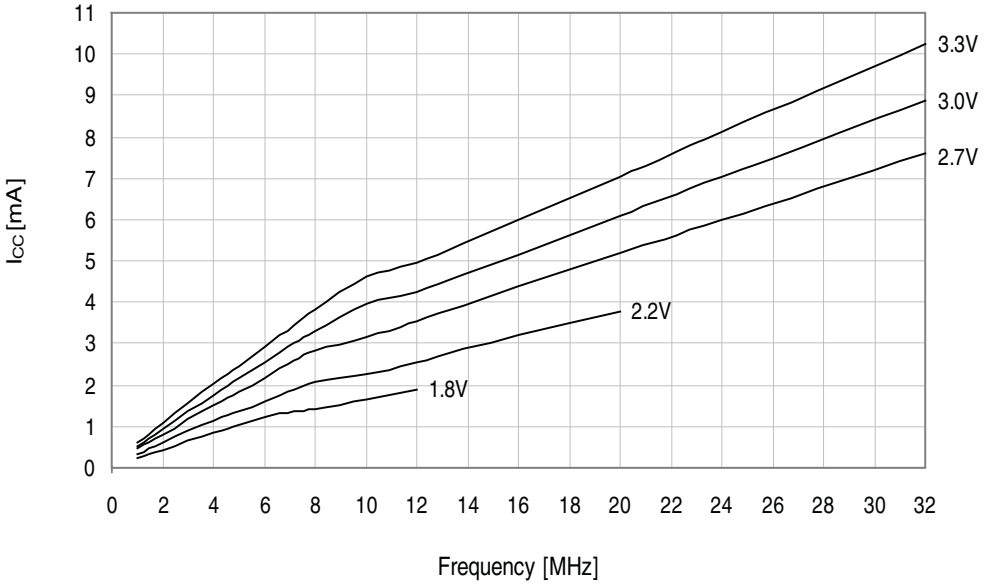


Figure 33-154. Active mode supply current vs. V_{CC}.

f_{SYS} = 32.768kHz internal oscillator.

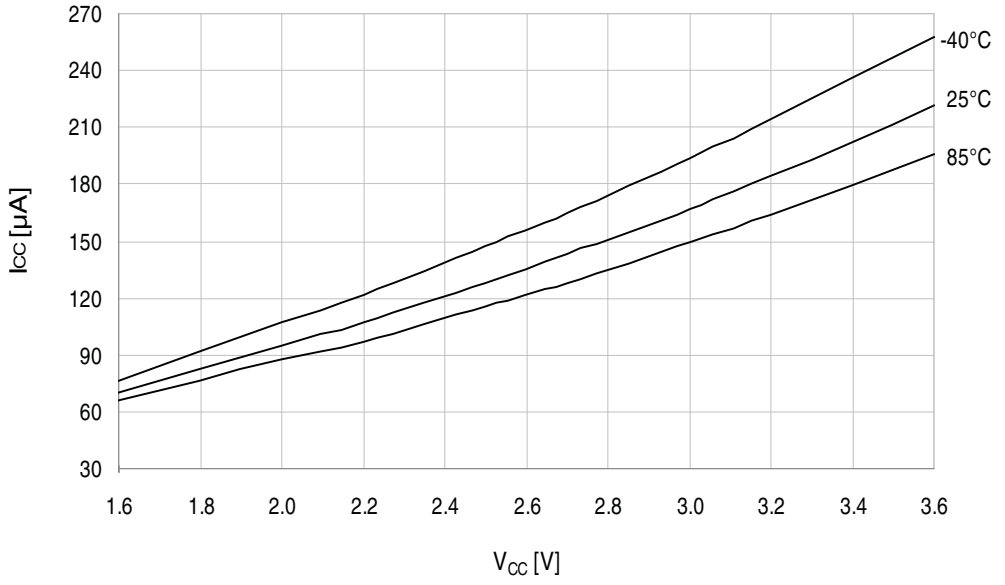


Figure 33-155. Active mode supply current vs. V_{CC}.

f_{SYS} = 1MHz external clock.

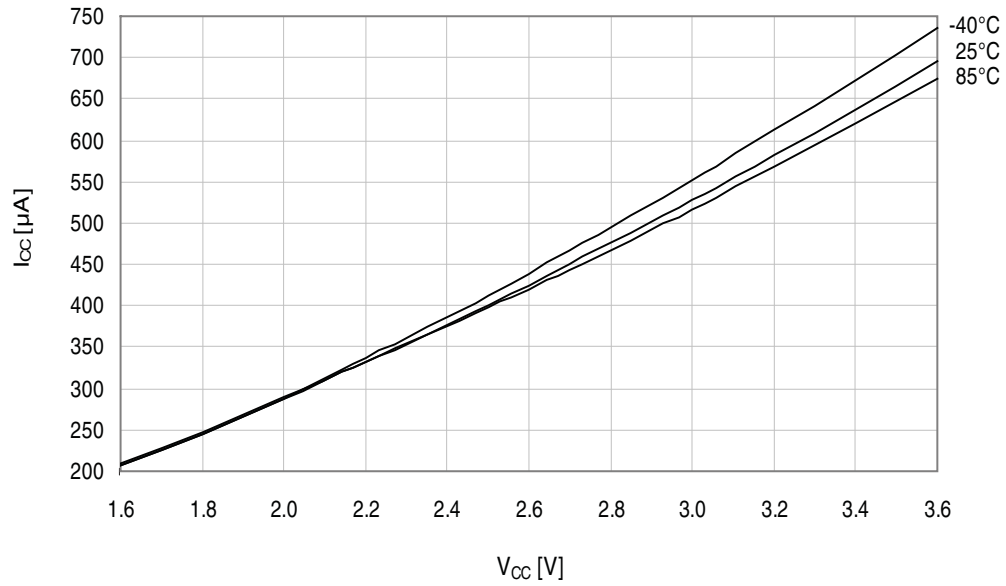


Figure 33-156. Active mode supply current vs. V_{CC}.

f_{SYS} = 2MHz internal oscillator.

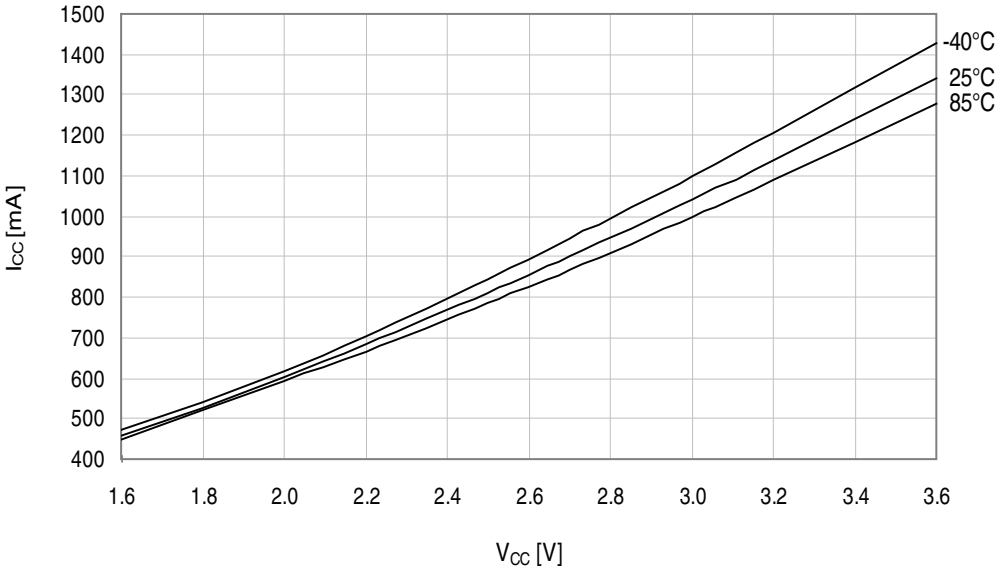


Figure 33-157. Active mode supply current vs. V_{CC}.

f_{SYS} = 32MHz internal oscillator prescaled to 8MHz.

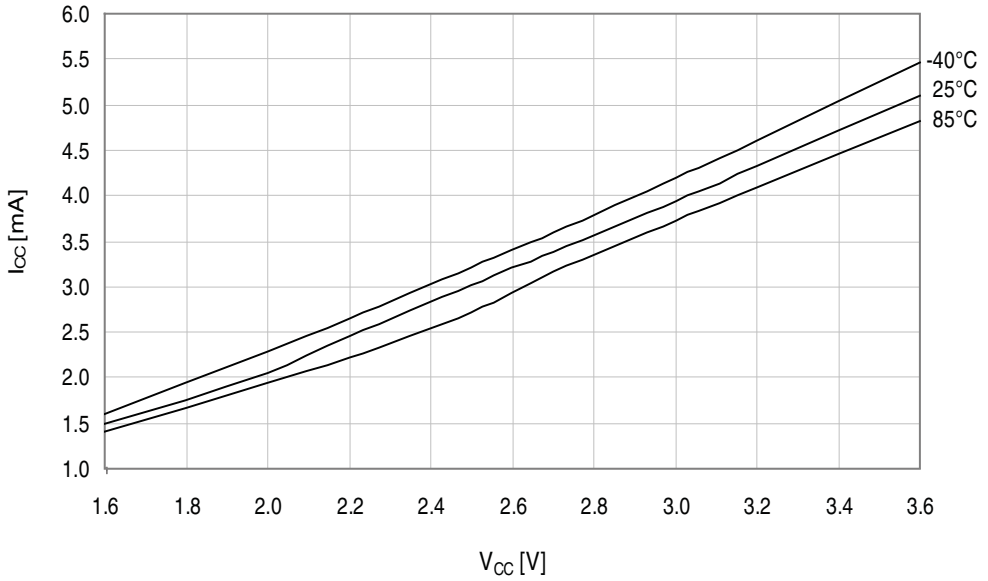
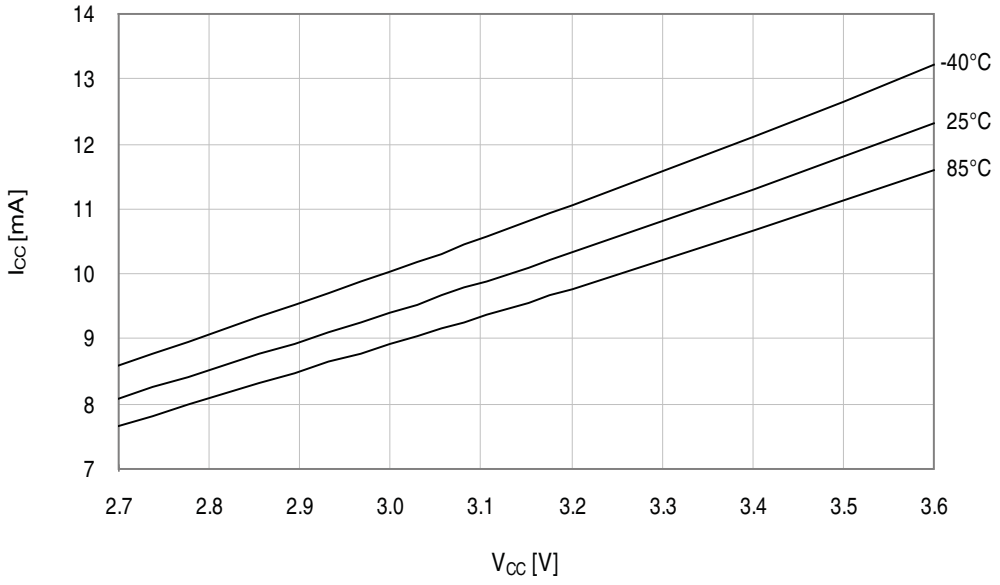


Figure 33-158. Active mode supply current vs. V_{CC}.

f_{SYS} = 32MHz internal oscillator.



33.4.1.2 Idle mode supply current

Figure 33-159. Idle mode supply current vs. frequency.

f_{SYS} = 0 - 1MHz external clock, T = 25°C.

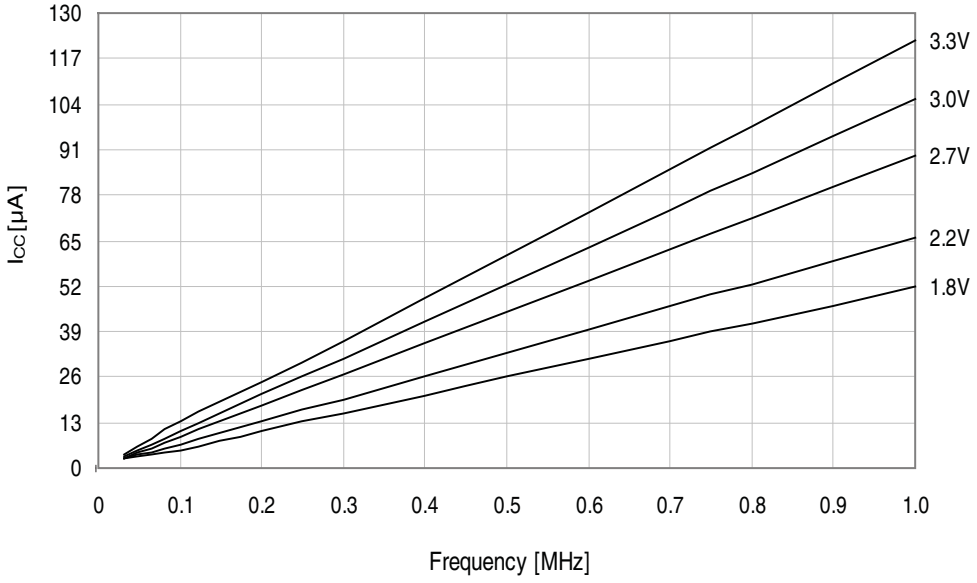


Figure 33-160. Idle mode supply current vs. frequency.

f_{SYS} = 1 - 32MHz external clock, T = 25°C.

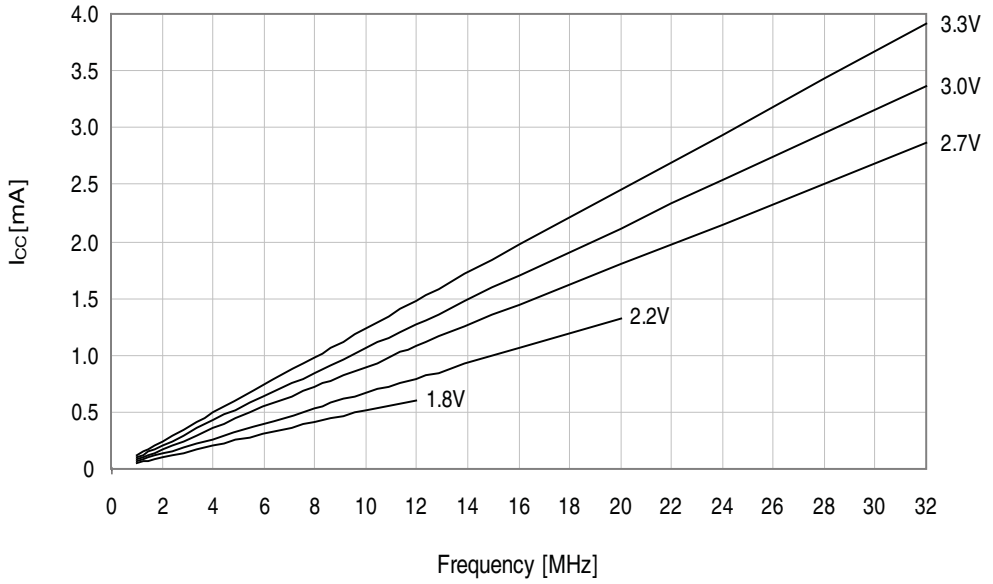


Figure 33-161. Idle mode supply current vs. V_{CC}.

f_{SYS} = 32.768kHz internal oscillator.

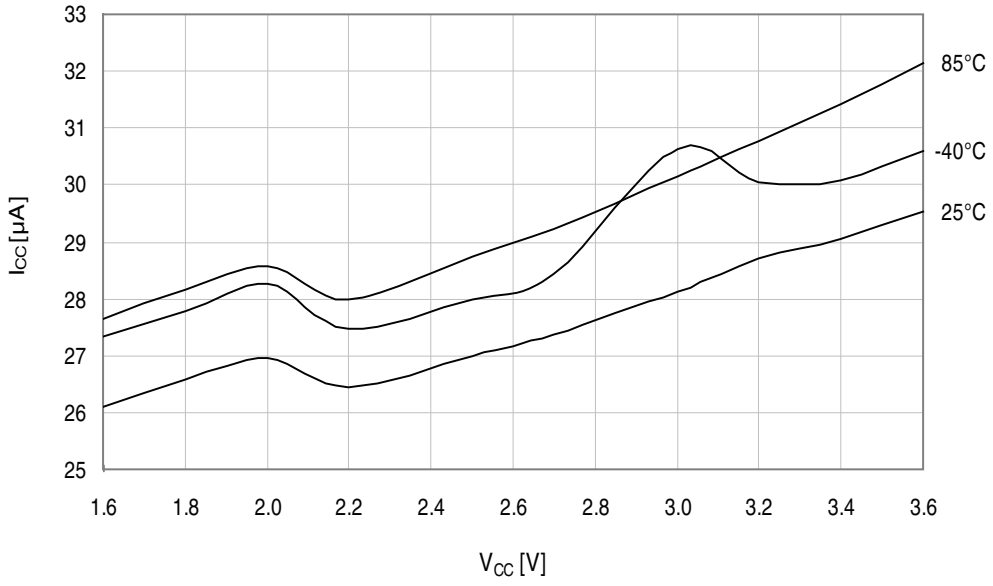


Figure 33-162. Idle mode supply current vs. V_{CC}.

f_{SYS} = 1MHz external clock.

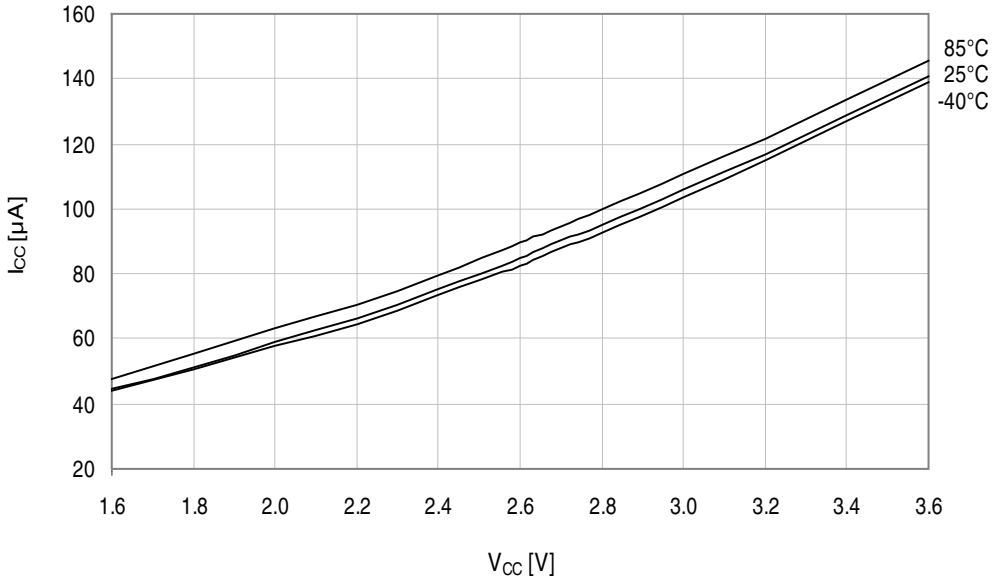


Figure 33-163. Idle mode supply current vs. V_{CC}.

f_{SYS} = 2MHz internal oscillator.

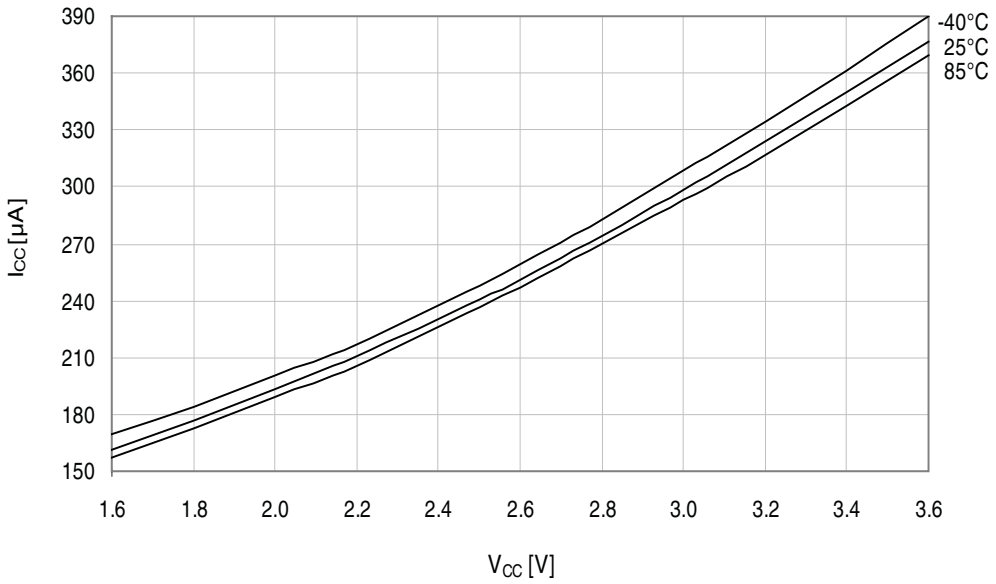


Figure 33-164. Idle mode supply current vs. V_{CC}.

f_{SYS} = 32MHz internal oscillator prescaled to 8MHz.

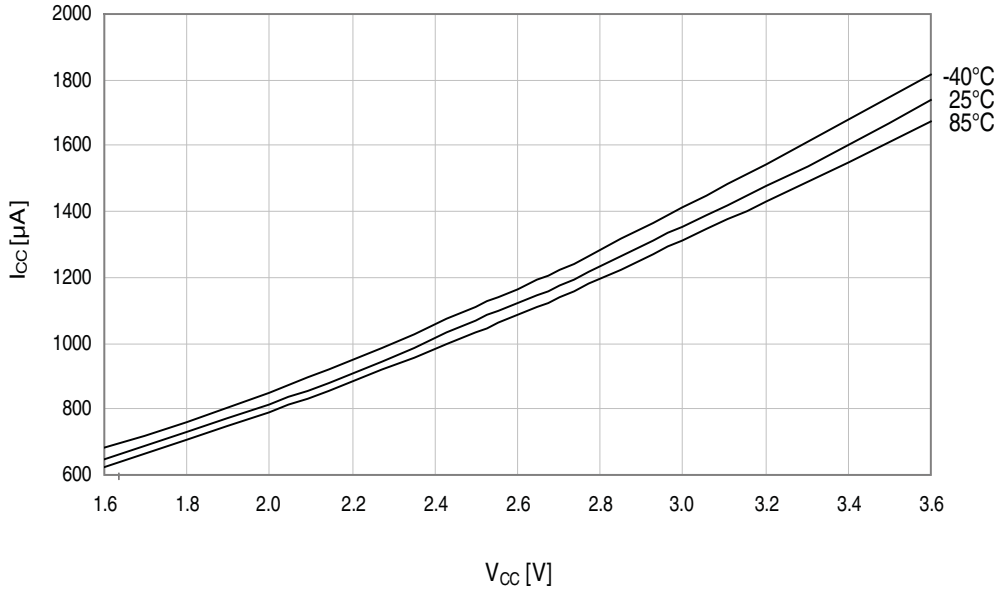
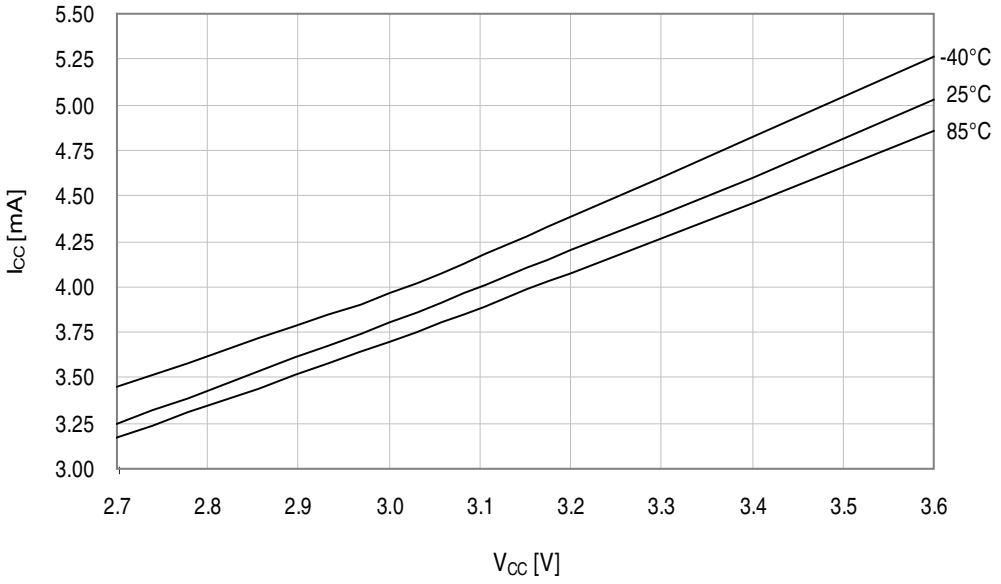


Figure 33-165. Idle mode current vs. V_{CC}.

f_{SYS} = 32MHz internal oscillator.



33.4.1.3 Power-down mode supply current

Figure 33-166. Power-down mode supply current vs. V_{CC}.
All functions disabled.

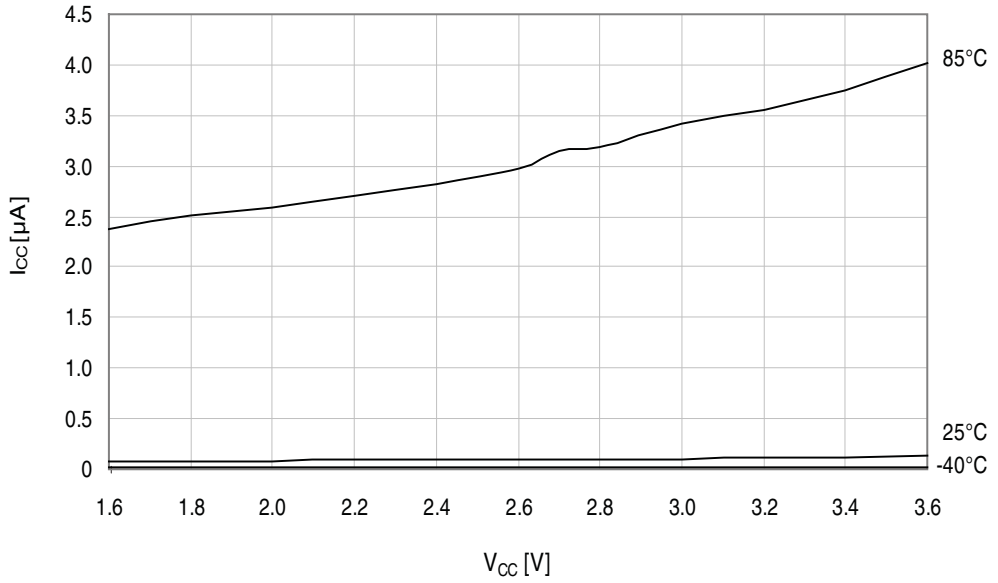


Figure 33-167. Power-down mode supply current vs. V_{CC}.
Watchdog and sampled BOD enabled.

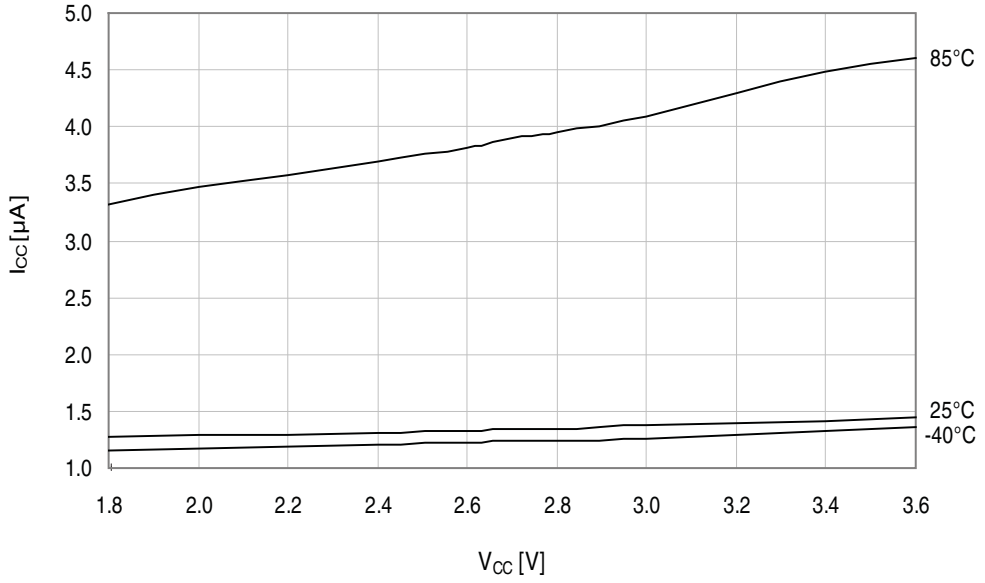
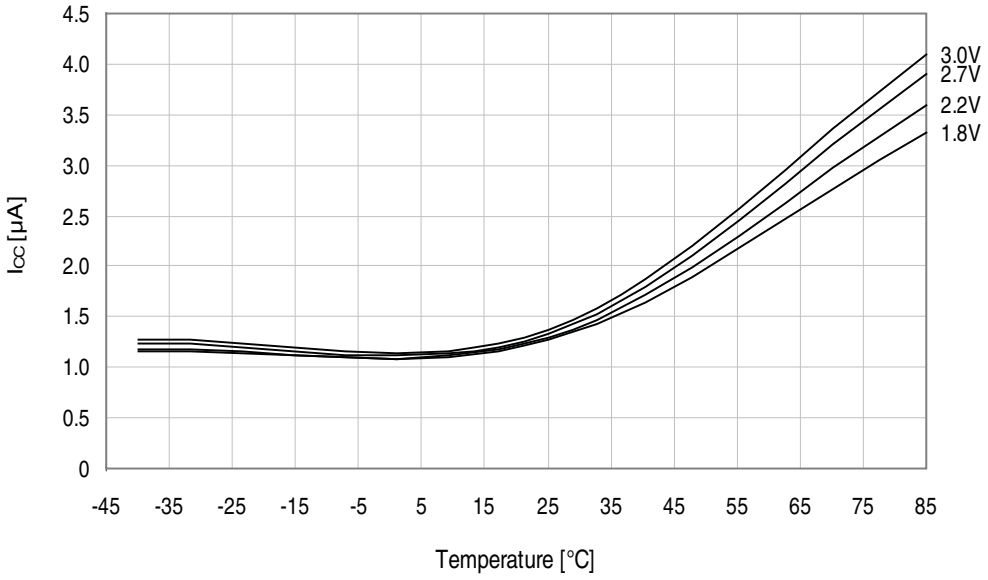


Figure 33-168. Power-down mode supply current vs. temperature.

Watchdog and sampled BOD enabled and running from internal ULP oscillator.



33.4.2 I/O pin characteristics

The I/O pins complies with the JEDEC LVTTL and LVCMOS specification and the high- and low level input and output voltage limits reflect or exceed this specification.

33.4.2.1 Pull-up

Figure 33-169. I/O pin pull-up resistor current vs. input voltage.

V_{CC} = 1.8V.

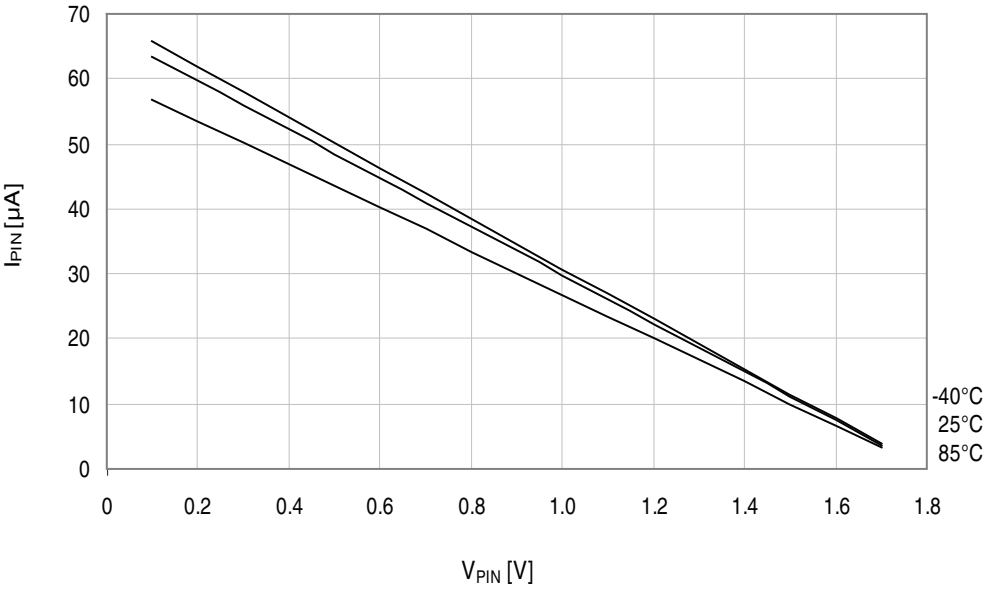


Figure 33-170. I/O pin pull-up resistor current vs. input voltage.
V_{CC} = 3.0V.

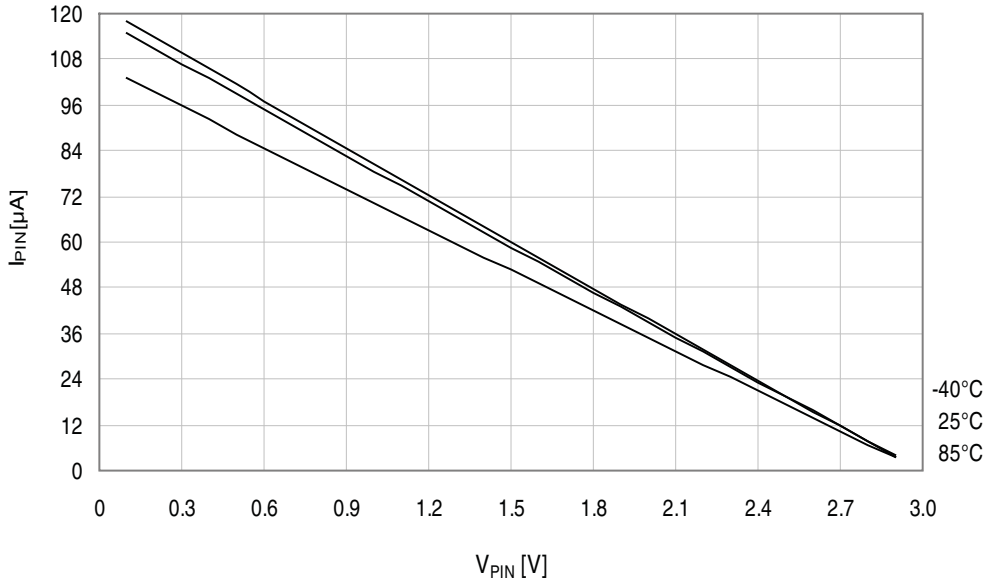
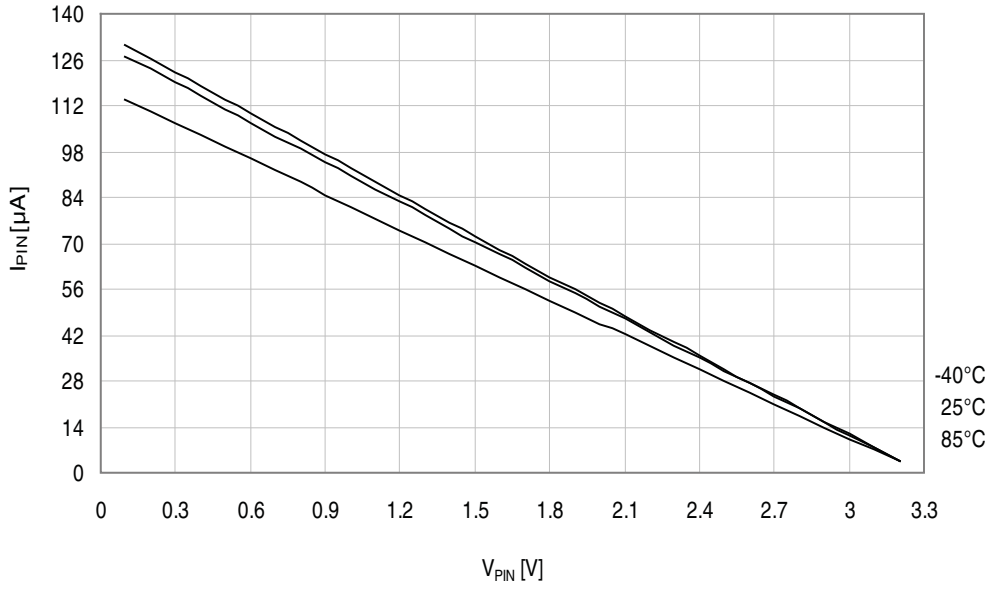


Figure 33-171. I/O pin pull-up resistor current vs. input voltage.
V_{CC} = 3.3V.



33.4.2.2 Output voltage vs. sink/source current

Figure 33-172. I/O pin output voltage vs. source current.
V_{CC} = 1.8V.

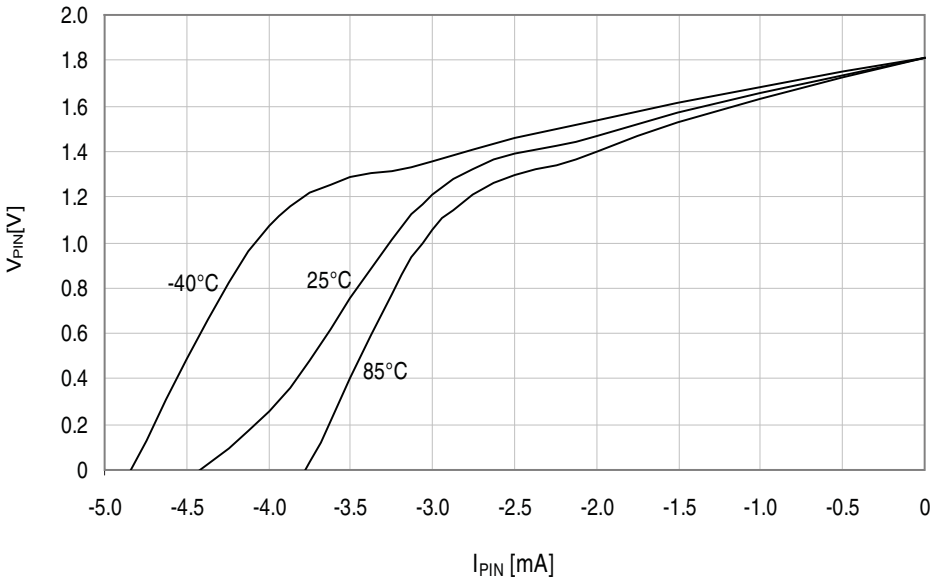


Figure 33-173. I/O pin output voltage vs. source current.
V_{CC} = 3.0V.

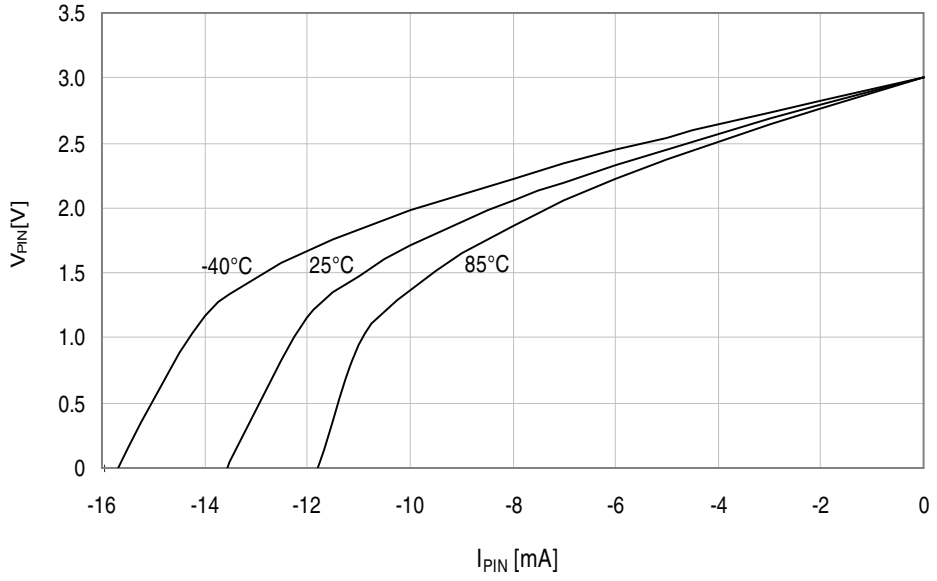


Figure 33-174. I/O pin output voltage vs. source current.

V_{CC} = 3.3V.

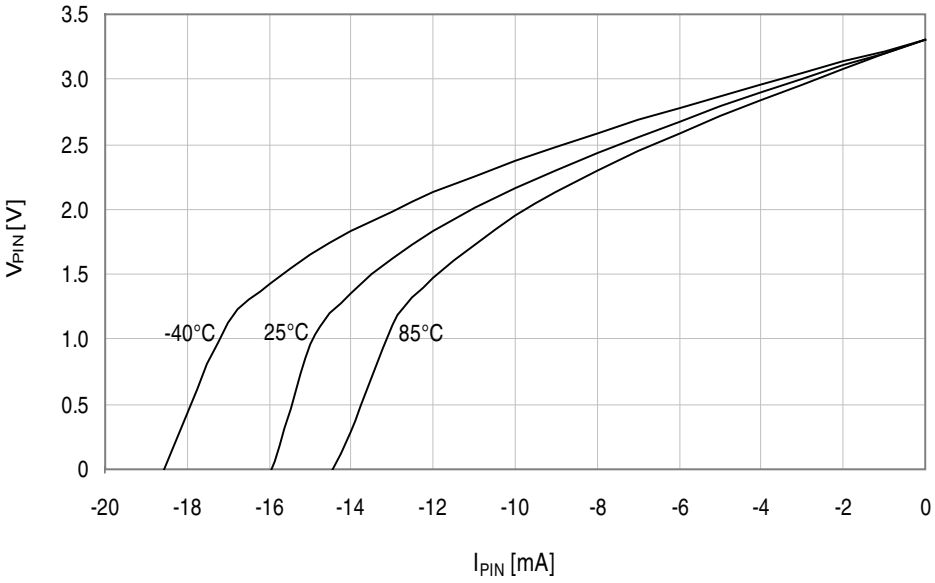


Figure 33-175. I/O pin output voltage vs. sink current.

V_{CC} = 1.8V.

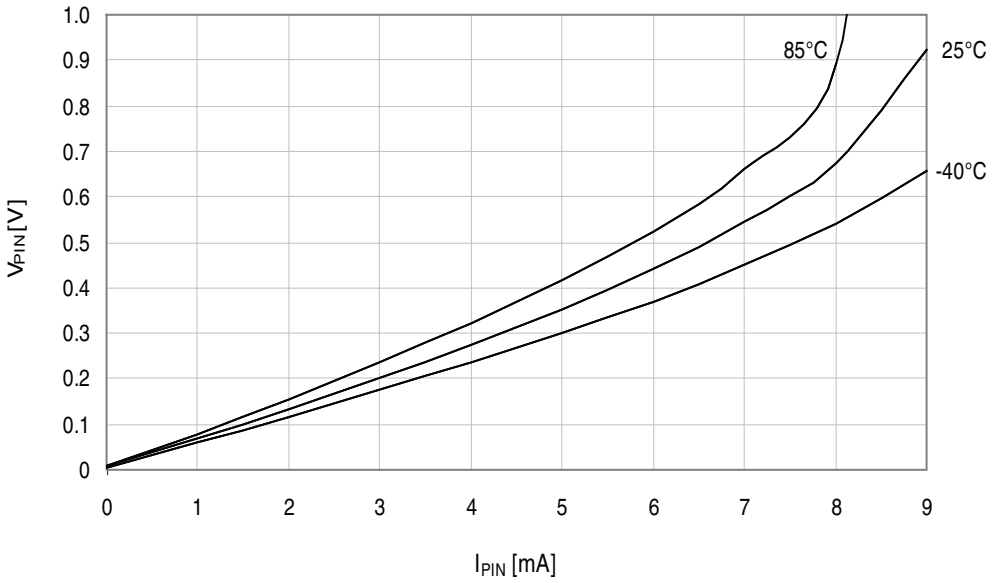


Figure 33-176. I/O pin output voltage vs. sink current.

V_{CC} = 3.0V.

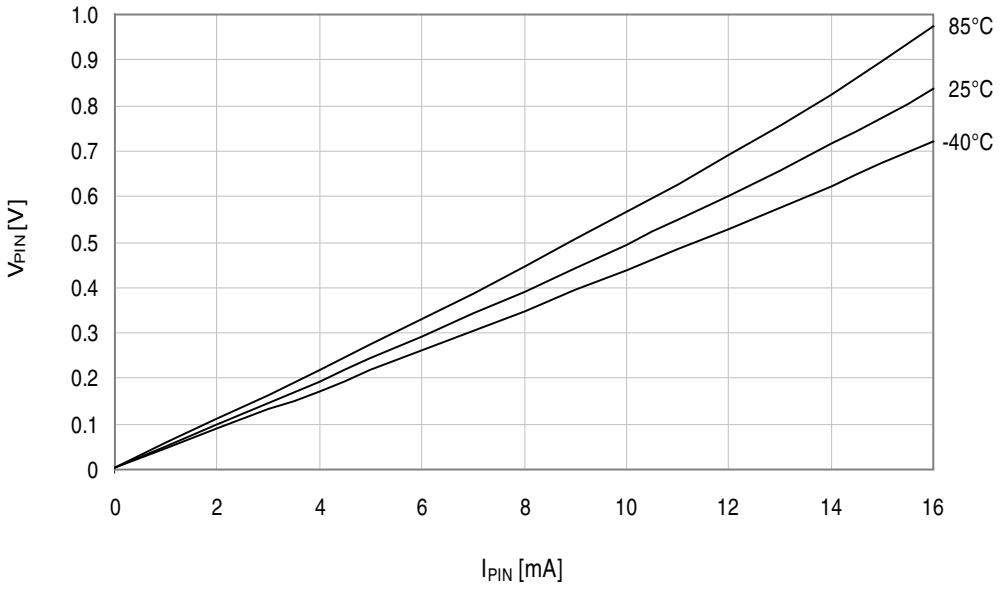
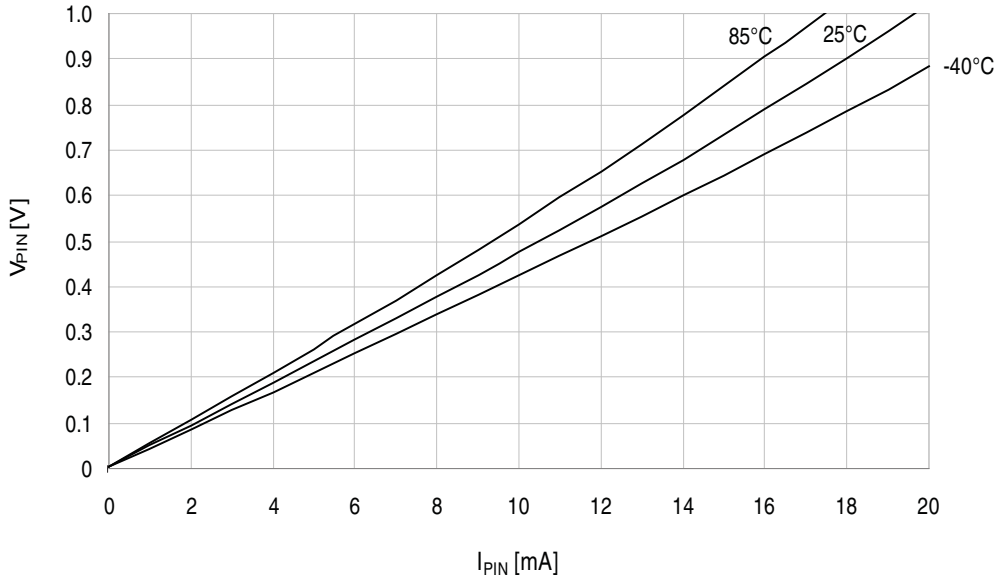


Figure 33-177. I/O pin output voltage vs. sink current.

V_{CC} = 3.3V.



33.4.2.3 Thresholds and hysteresis

Figure 33-178. I/O pin input threshold voltage vs. V_{CC}.
V_{IH} I/O pin read as "1".

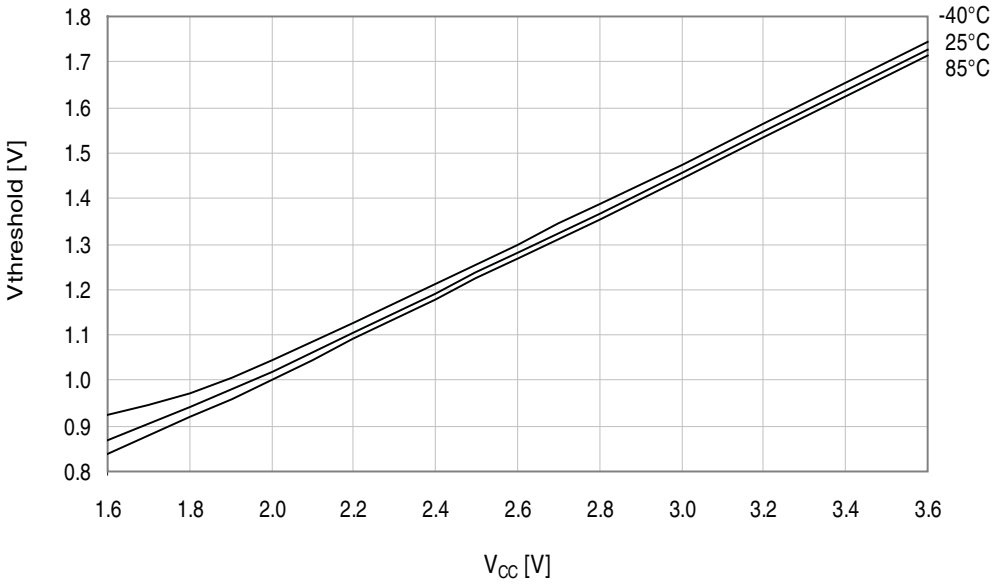


Figure 33-179. I/O pin input threshold voltage vs. V_{CC}.
V_{IL} I/O pin read as "0".

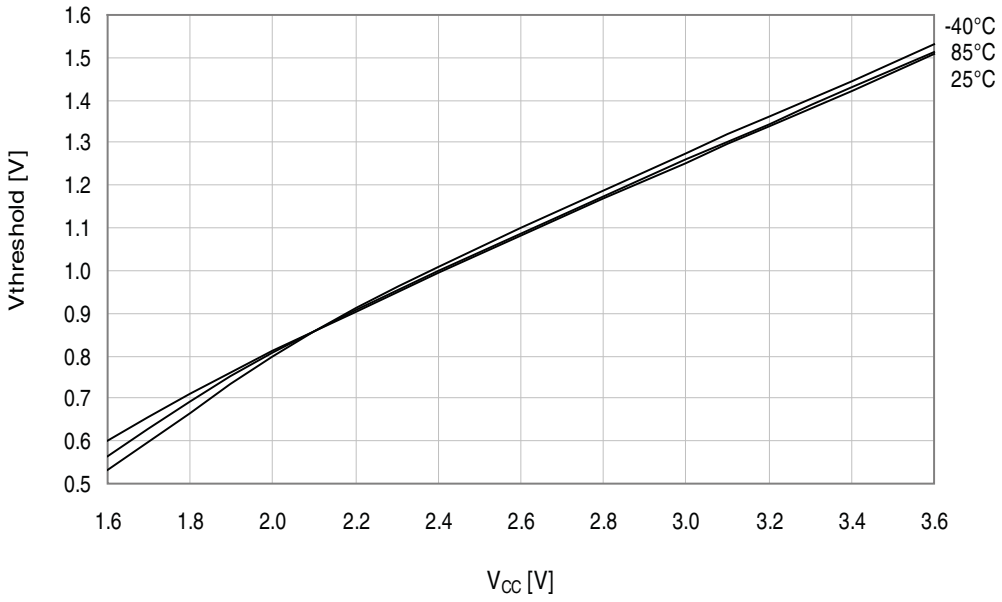
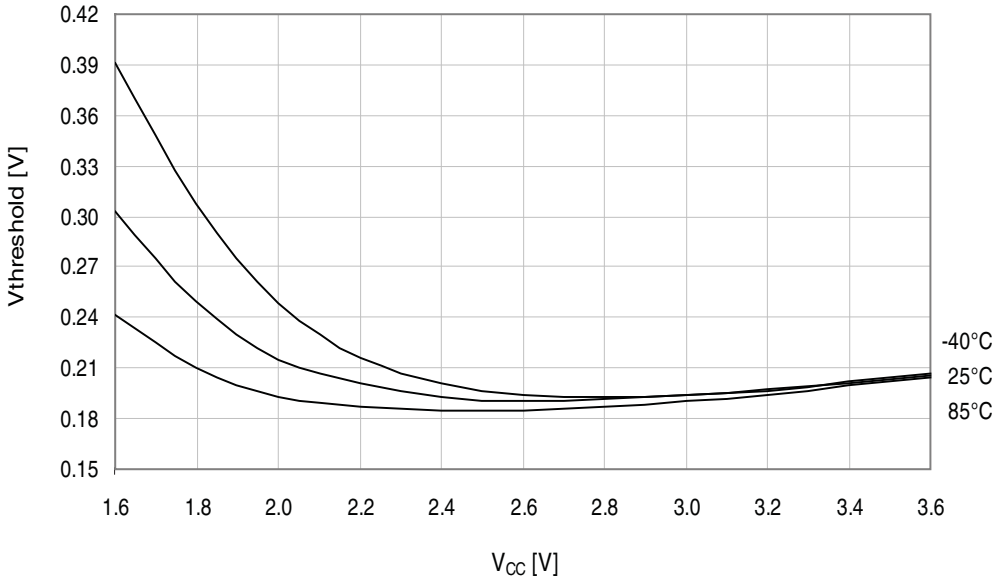


Figure 33-180. I/O pin input hysteresis vs. V_{CC}.



33.4.3 ADC characteristics

Figure 33-181. INL error vs. external V_{REF}.

T = 25°C, V_{CC} = 3.6V, external reference.

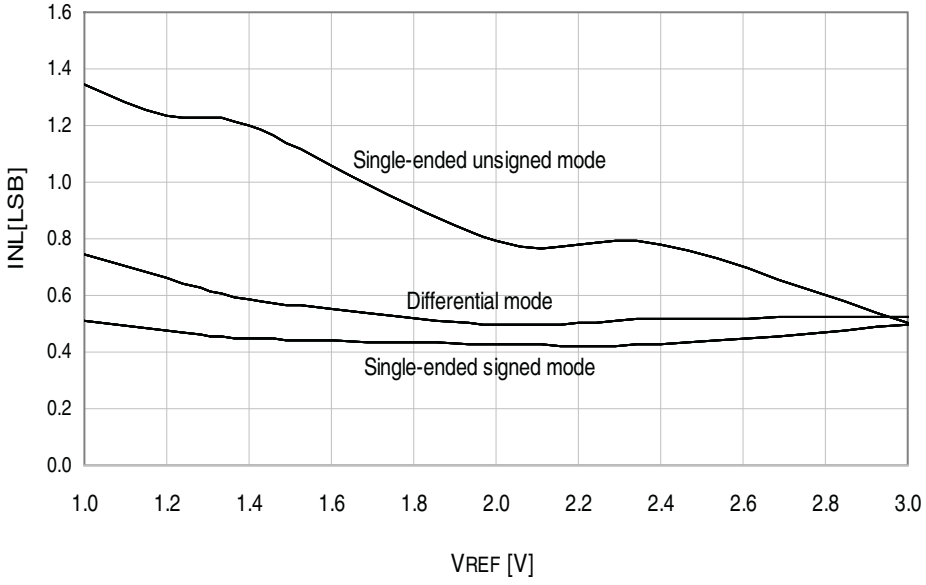


Figure 33-182. INL error vs. sample rate.

T = 25°C, V_{CC} = 3.6V, V_{REF} = 3.0V external.

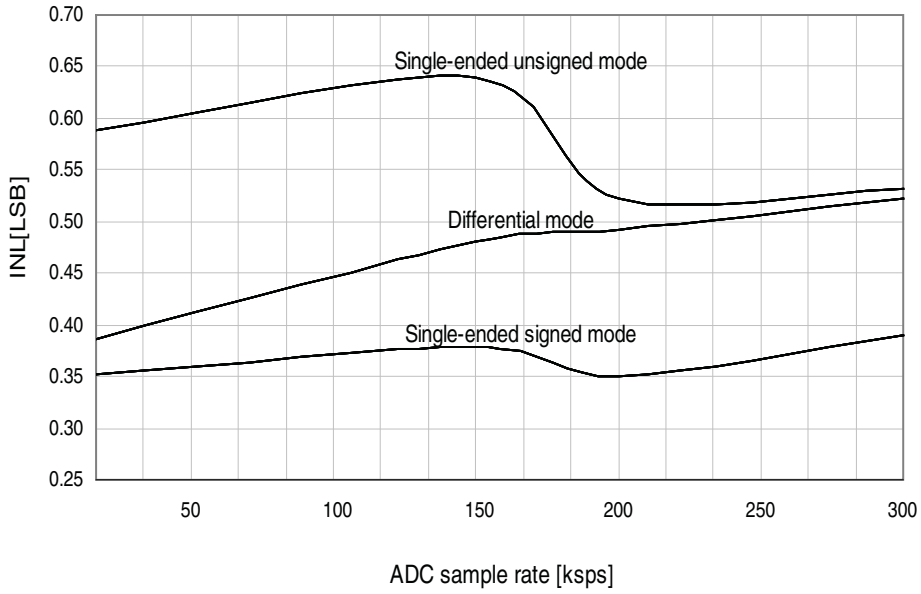


Figure 33-183. INL error vs. input code.

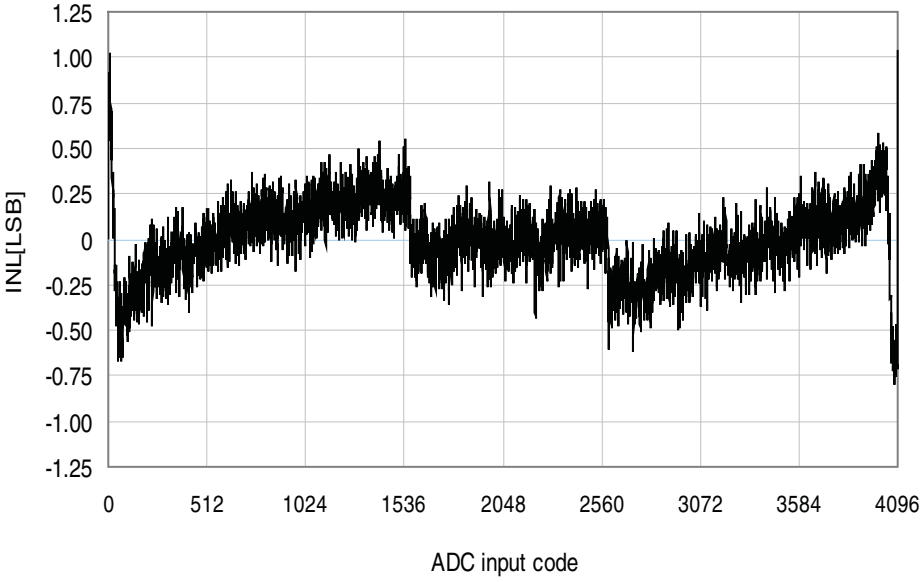


Figure 33-184. DNL error vs. external V_{REF}.

T = 25°C, V_{CC} = 3.6V, external reference.

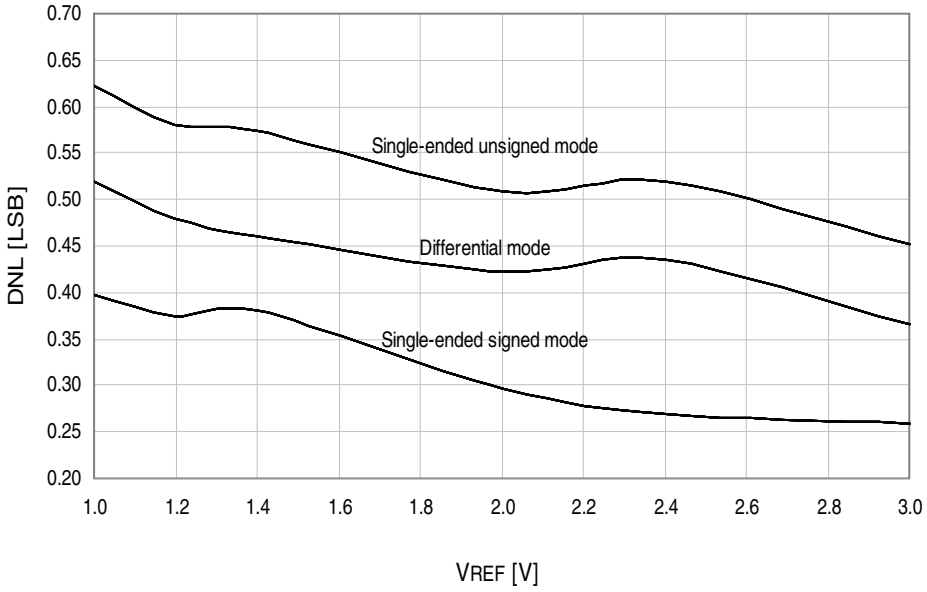


Figure 33-185. DNL error vs. sample rate.

T = 25°C, V_{CC} = 3.6V, V_{REF} = 3.0V external.

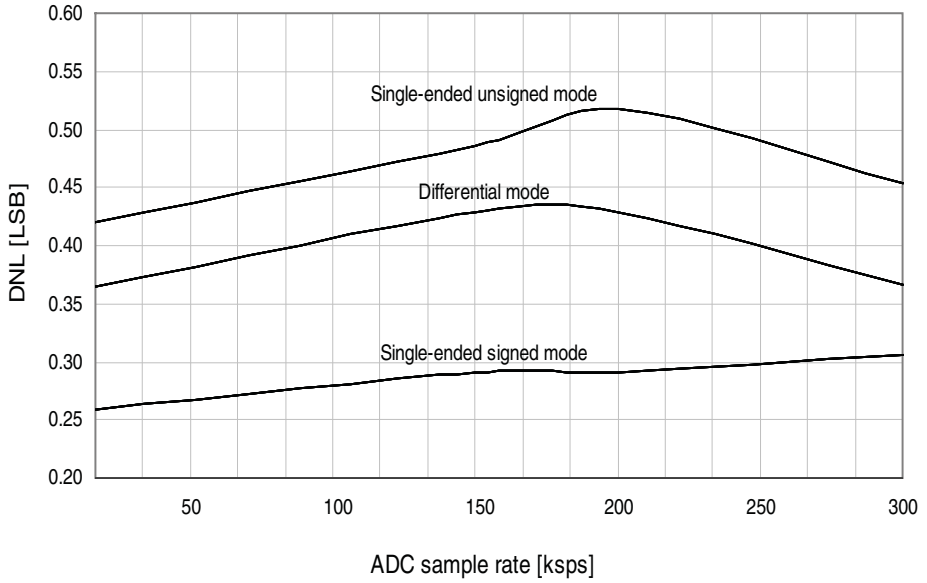


Figure 33-186. DNL error vs. input code.

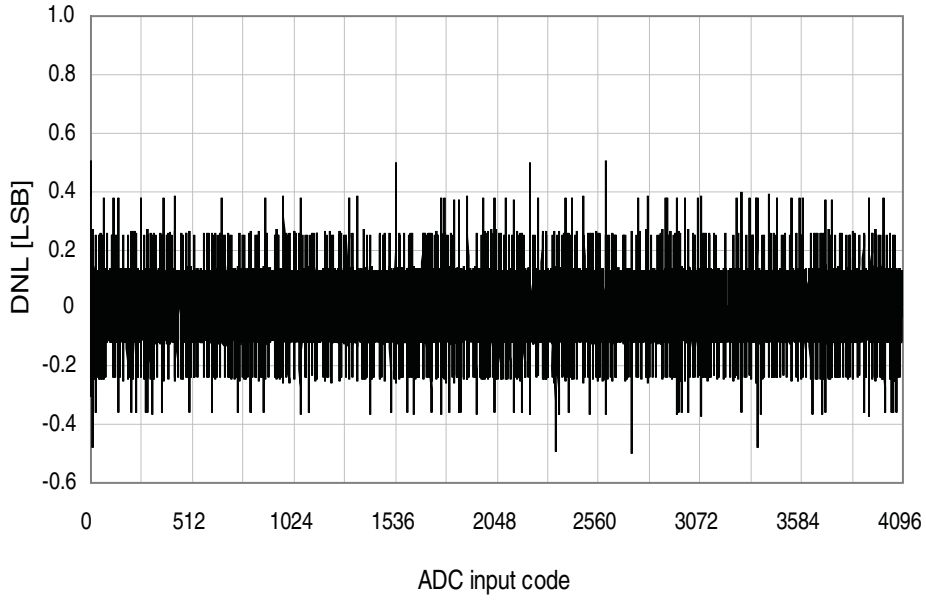


Figure 33-187. Gain error vs. V_{REF}.

T = 25°C, V_{CC} = 3.6V, ADC sample rate = 300ksps.

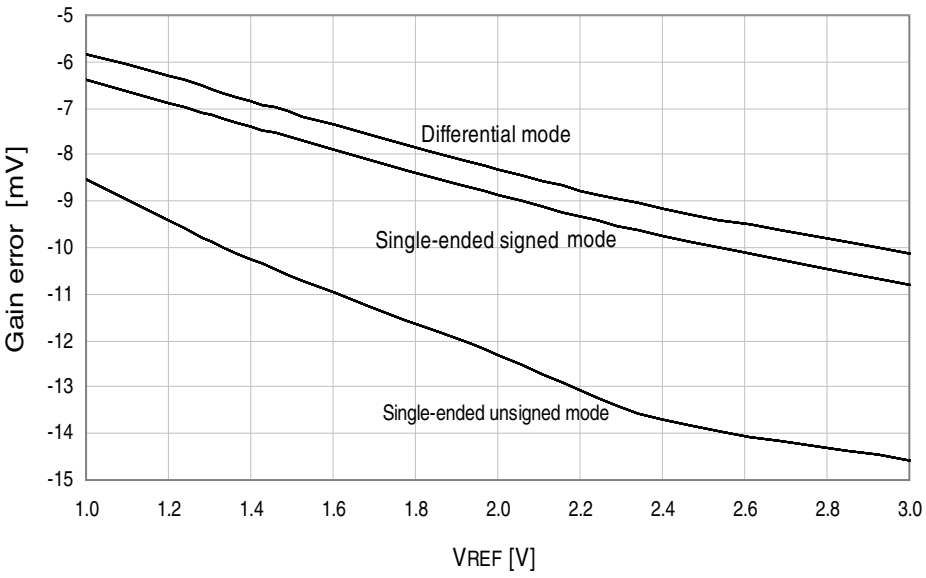


Figure 33-188. Gain error vs. V_{CC}.

T = 25°C, V_{REF} = external 1.0V, ADC sample rate = 300ksps.

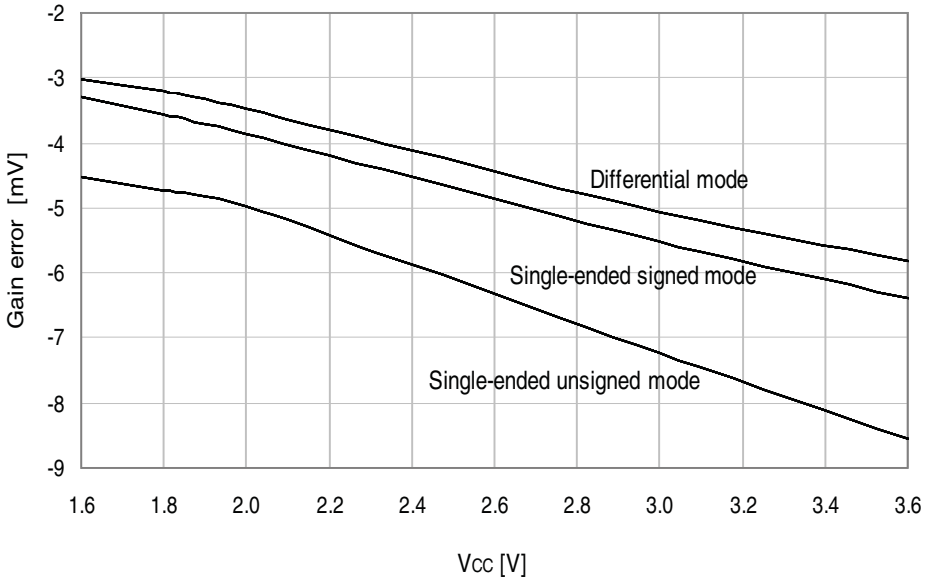


Figure 33-189. Offset error vs. V_{REF}.

T = 25°C, V_{CC} = 3.6V, ADC sample rate = 300ksps.

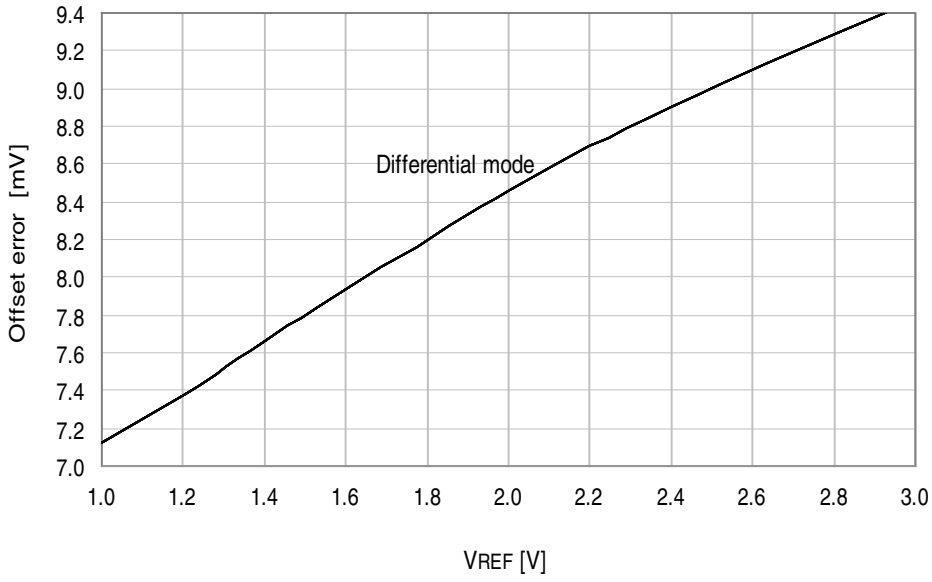


Figure 33-190. Gain error vs. temperature.

V_{CC} = 3.0V, V_{REF} = external 2.0V.

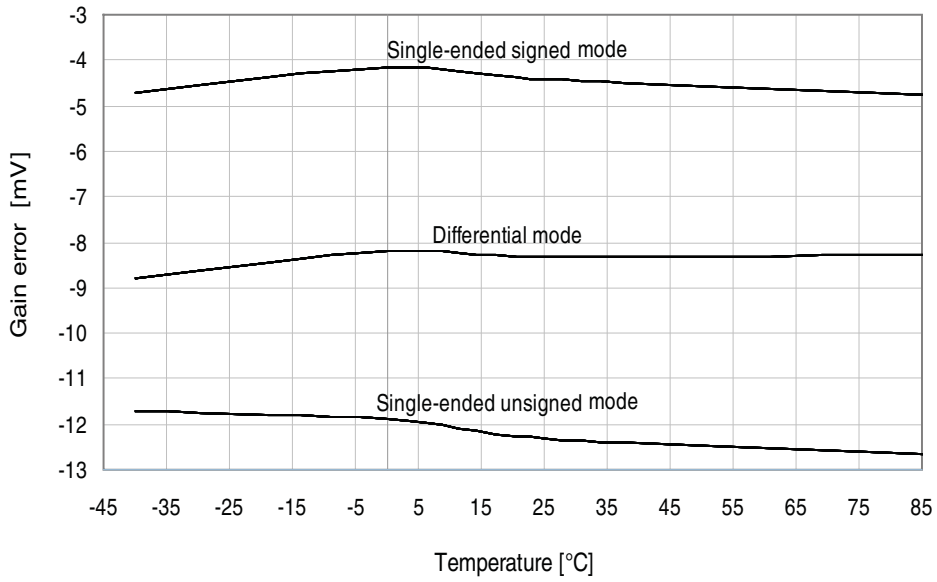
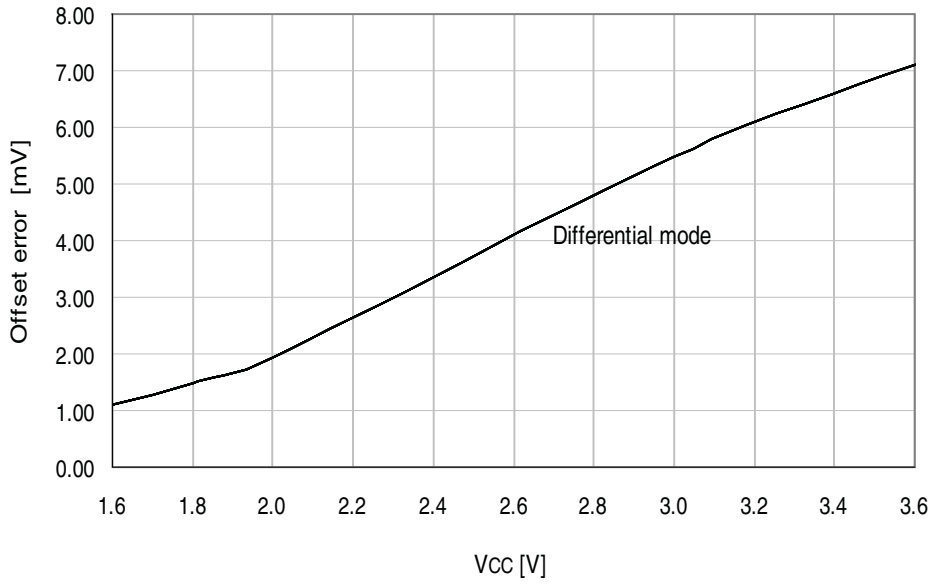


Figure 33-191. Offset error vs. V_{CC}.

T = 25°C, V_{REF} = external 1.0V, ADC sample rate = 300ksps.



33.4.4 Analog comparator characteristics

Figure 33-192. Analog comparator hysteresis vs. V_{CC}.
Small hysteresis.

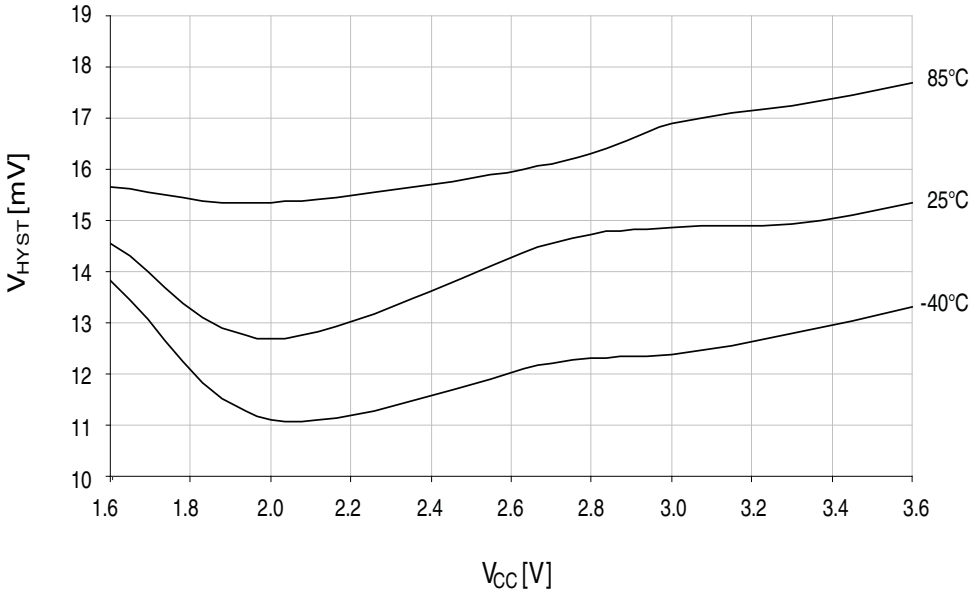


Figure 33-193. Analog comparator hysteresis vs. V_{CC}.
Large hysteresis.

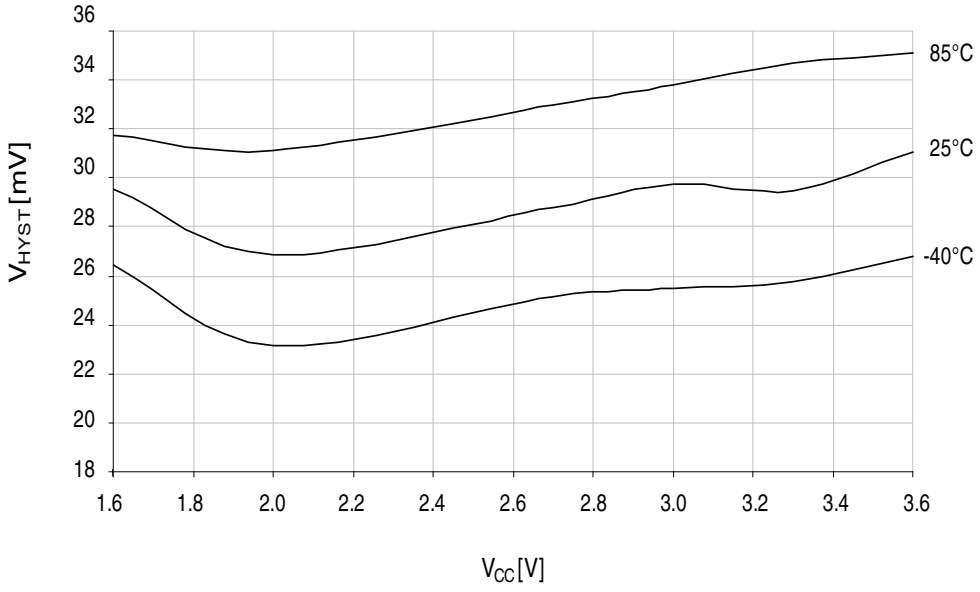


Figure 33-194. Analog comparator current source vs. calibration value.

V_{CC} = 3.0V.

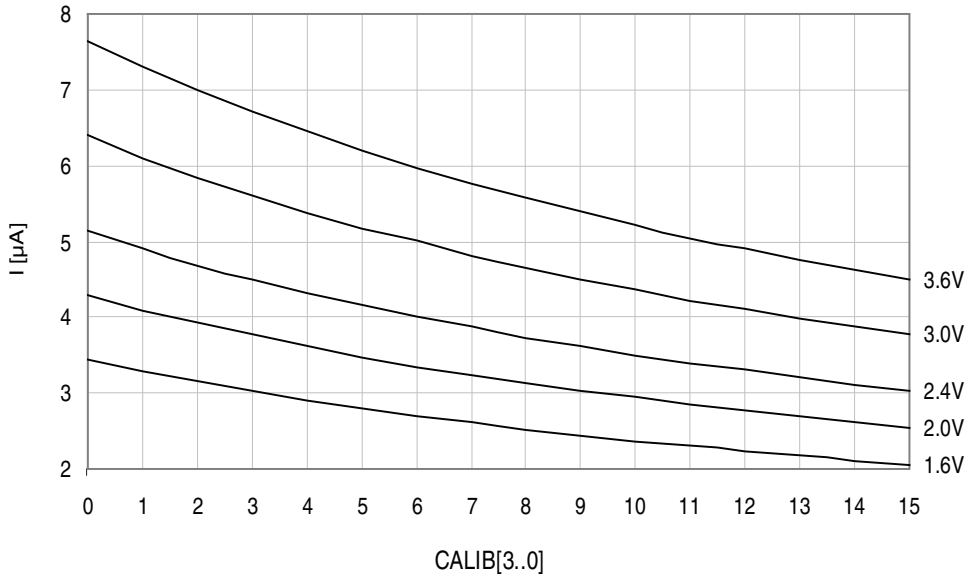
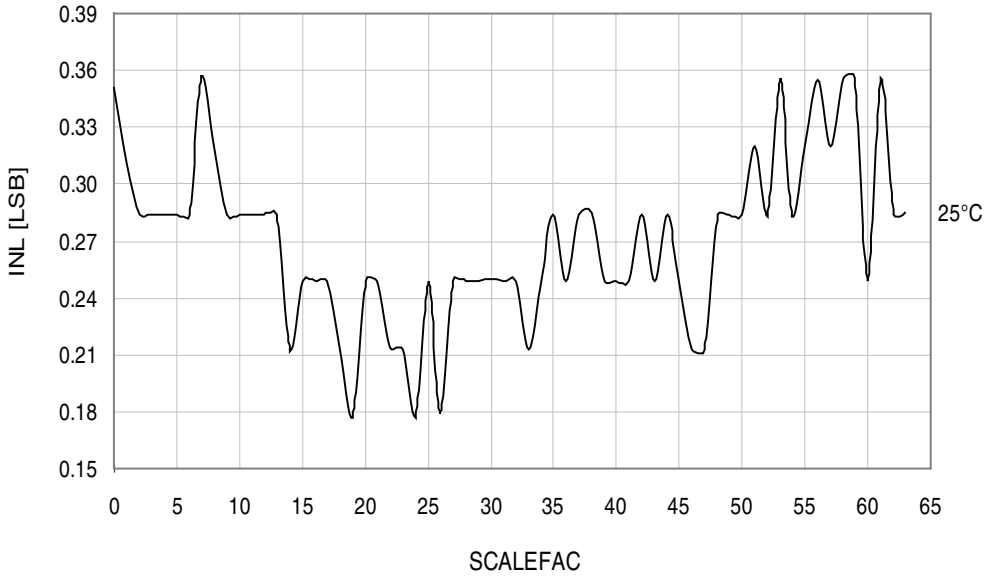


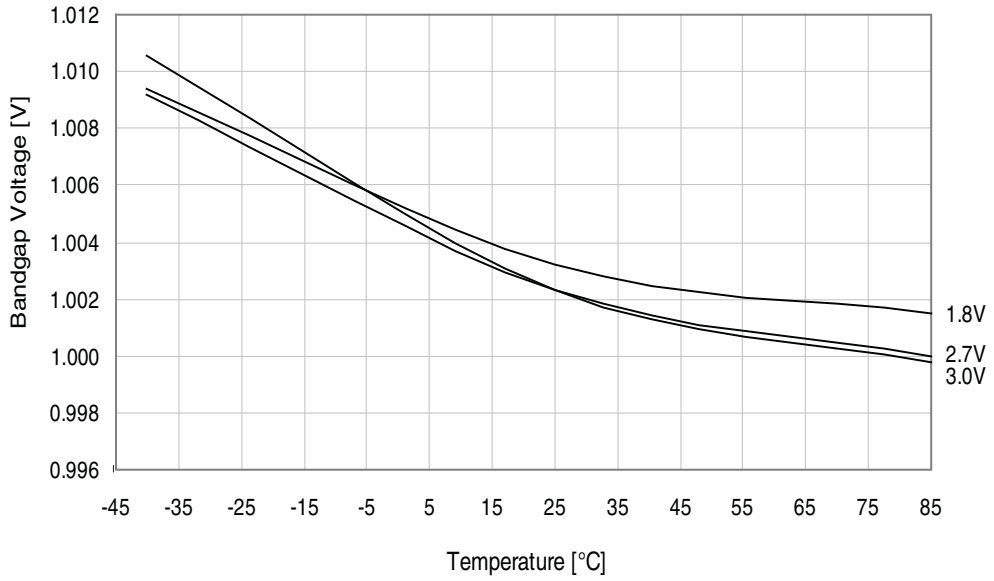
Figure 33-195. Voltage scaler INL vs. SCALEFAC.

T = 25°C, V_{CC} = 3.0V.



33.4.5 Internal 1.0V reference characteristics

Figure 33-196. ADC Internal 1.0V reference vs. temperature.



33.4.6 BOD characteristics

Figure 33-197. BOD thresholds vs. temperature.
BOD level = 1.6V.

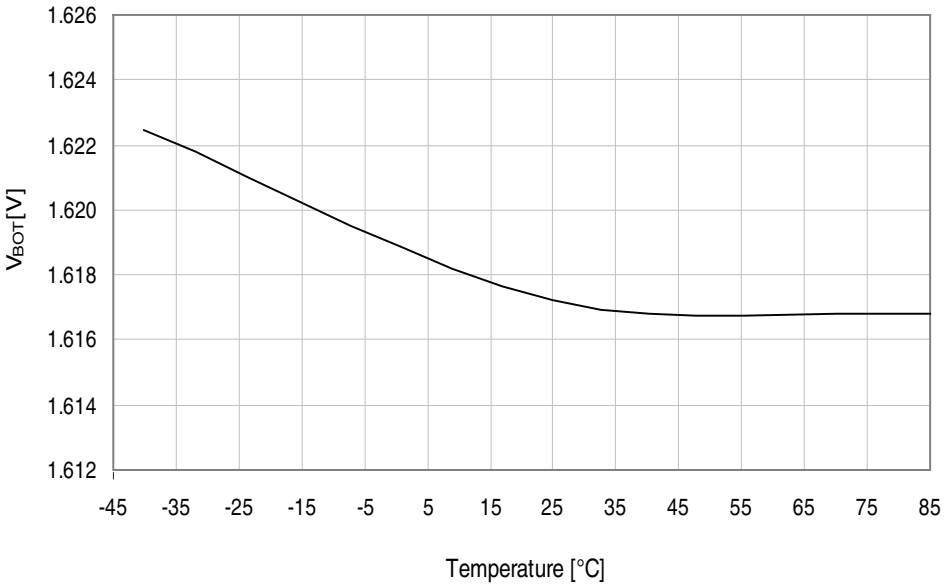
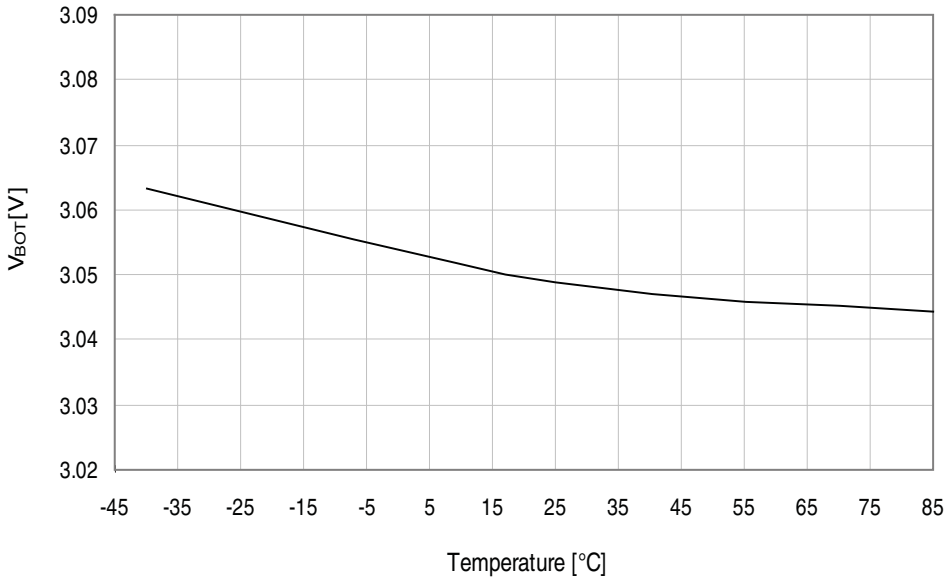


Figure 33-198. BOD thresholds vs. temperature.
BOD level = 3.0V.



33.4.7 External reset characteristics

Figure 33-199. Minimum reset pin pulse width vs. V_{CC}.

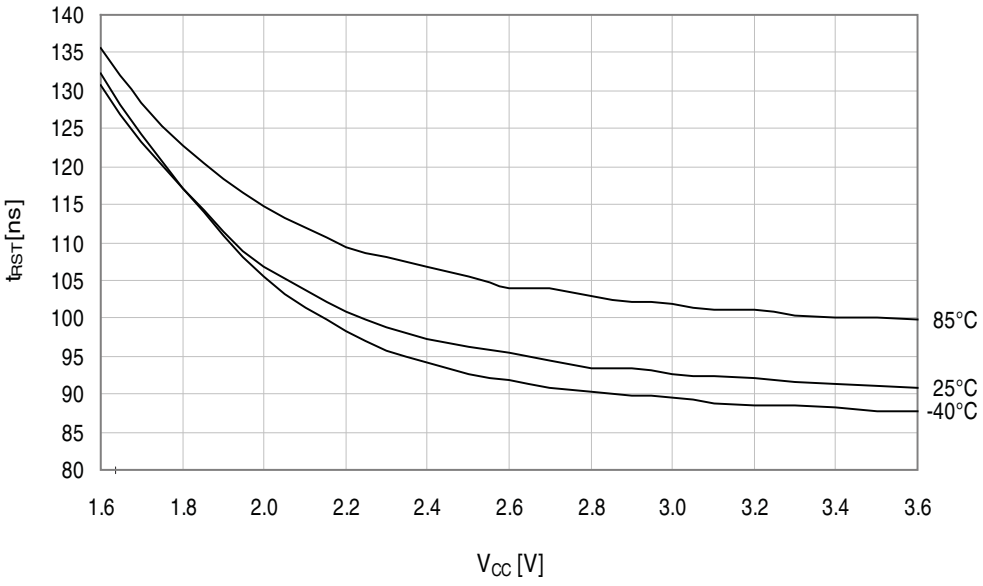


Figure 33-200. Reset pin pull-up resistor current vs. reset pin voltage.
V_{CC} = 1.8V.

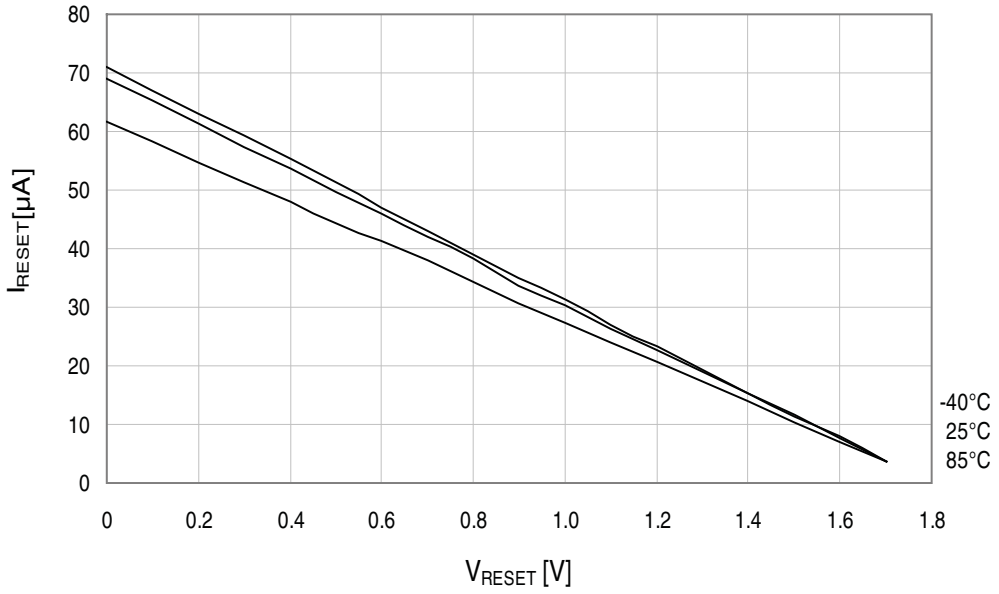


Figure 33-201. Reset pin pull-up resistor current vs. reset pin voltage.
V_{CC} = 3.0V.

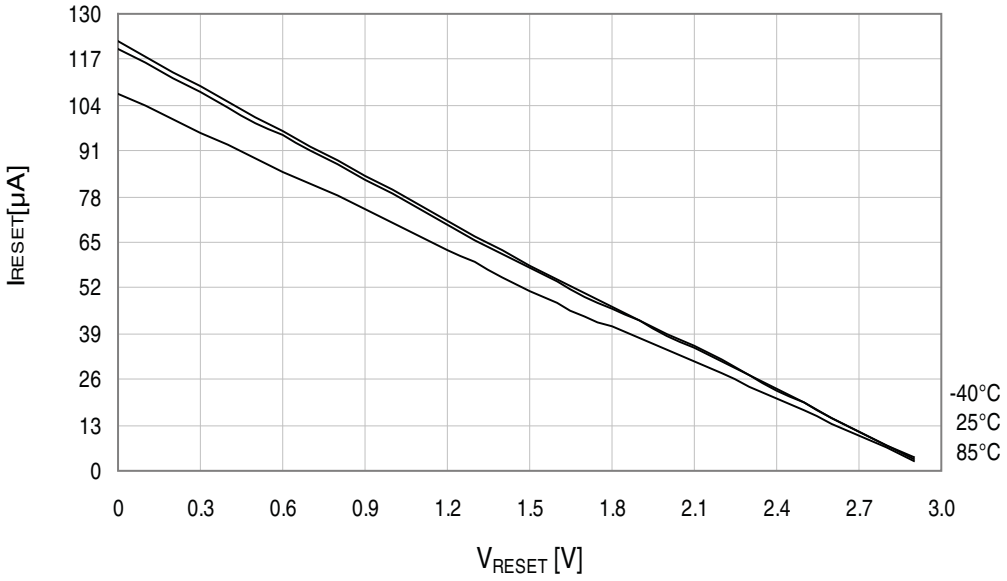


Figure 33-202. Reset pin pull-up resistor current vs. reset pin voltage.
V_{CC} = 3.3V.

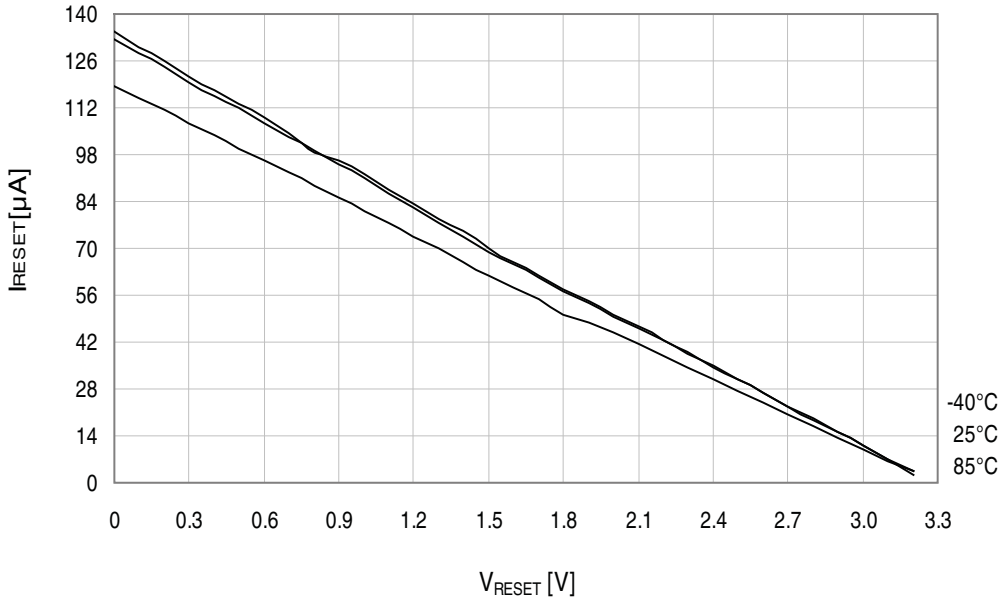
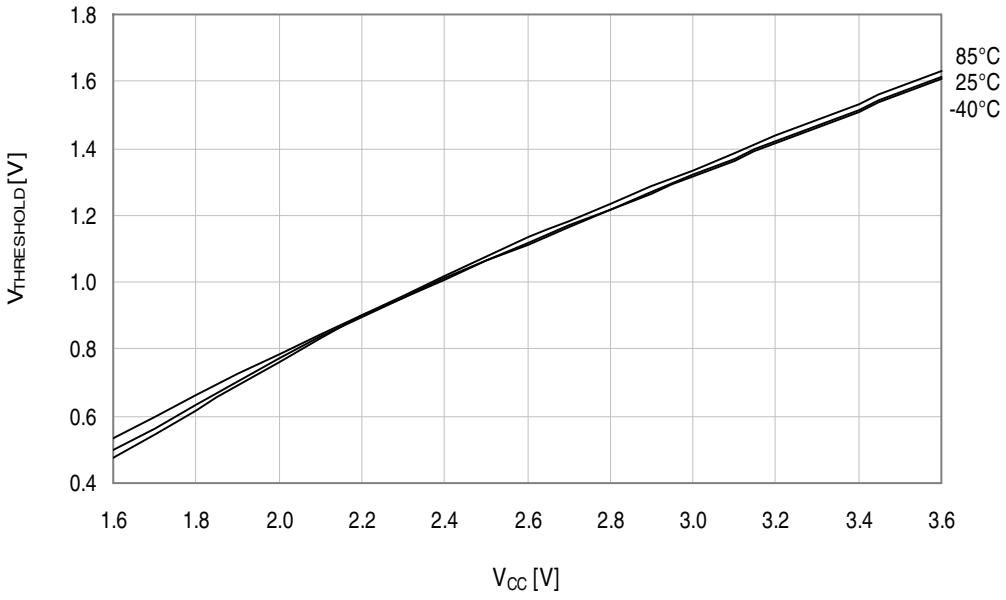


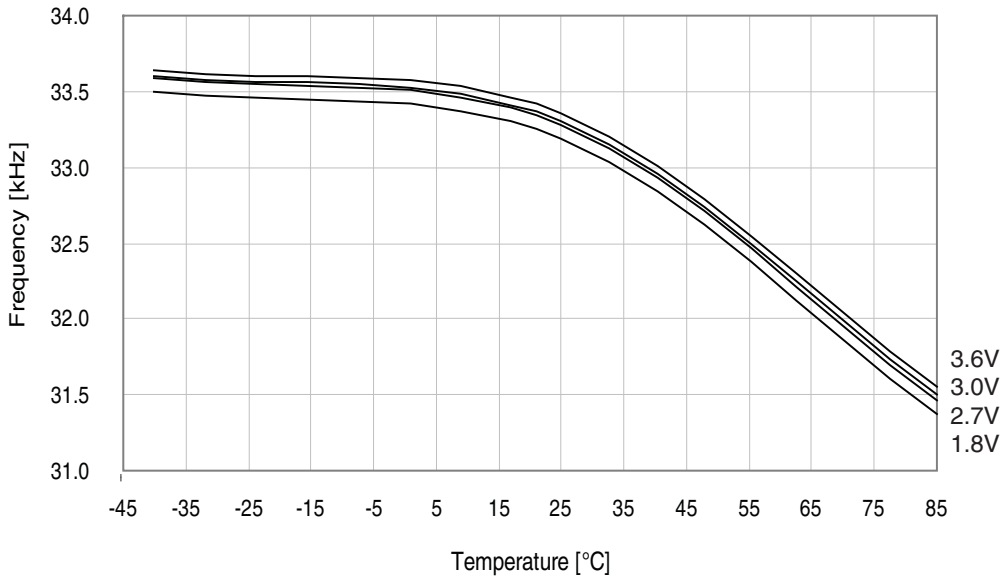
Figure 33-203. Reset pin input threshold voltage vs. V_{CC}.
V_{IH} - Reset pin read as "1".



33.4.8 Oscillator characteristics

33.4.8.1 Ultra Low-Power internal oscillator

Figure 33-204. Ultra Low-Power internal oscillator frequency vs. temperature.



33.4.8.2 32.768kHz internal oscillator

Figure 33-205. 32.768kHz internal oscillator frequency vs. temperature.

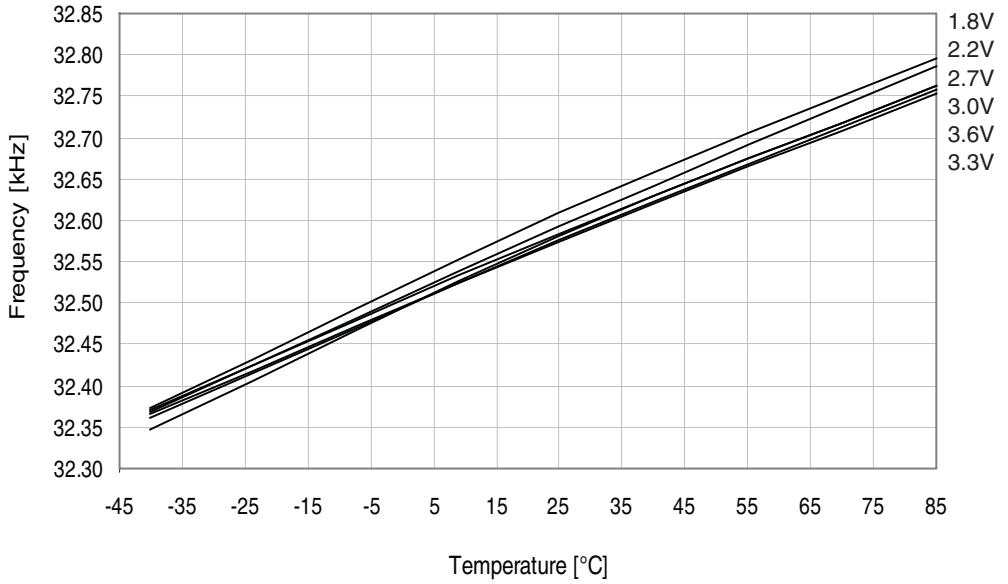
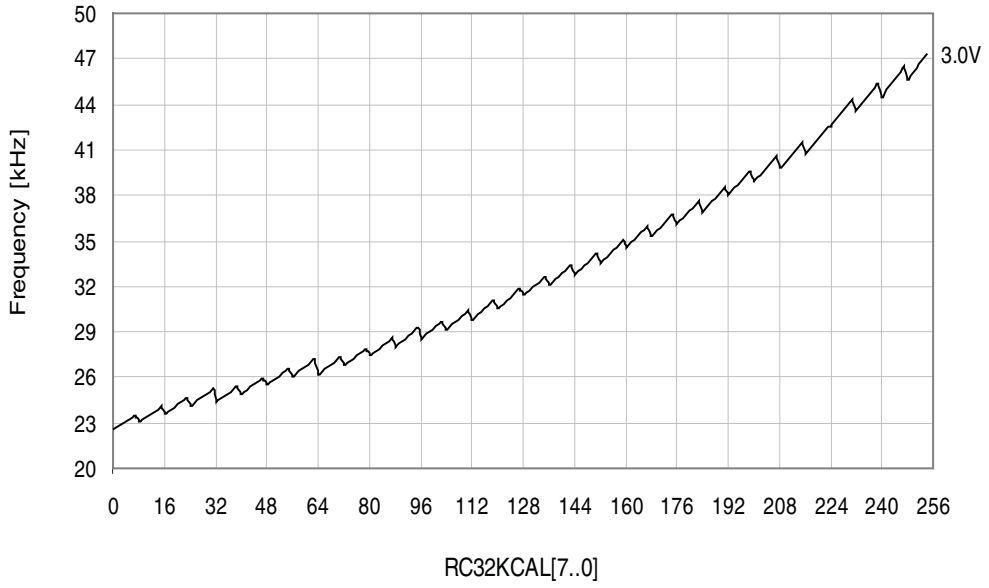


Figure 33-206. 32.768kHz internal oscillator frequency vs. calibration value.
V_{CC} = 3.0V, T = 25°C.



33.4.8.3 2MHz internal oscillator

Figure 33-207. 2MHz internal oscillator frequency vs. temperature.
DFLL disabled.

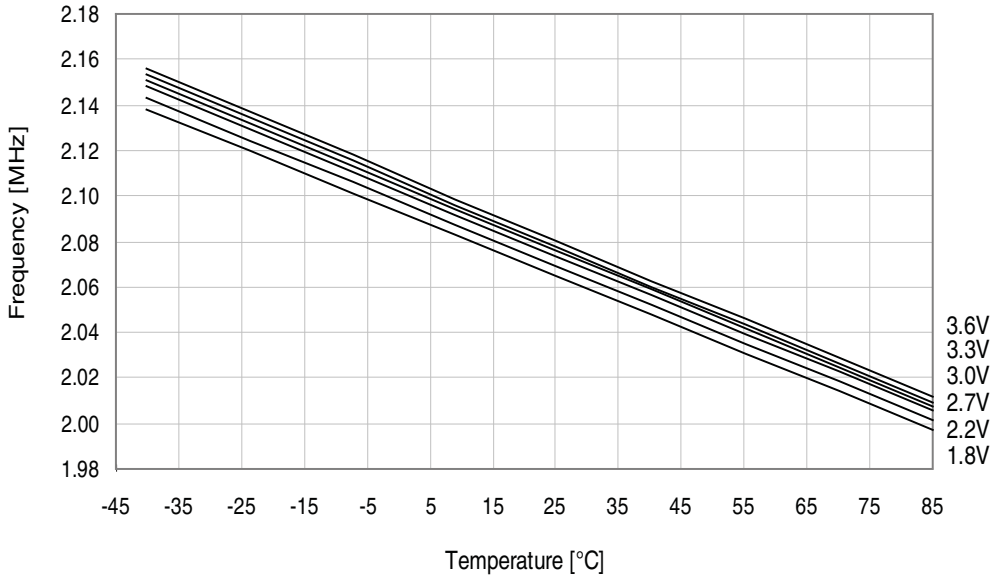


Figure 33-208. 2MHz internal oscillator frequency vs. temperature.
DFLL enabled, from the 32.768kHz internal oscillator.

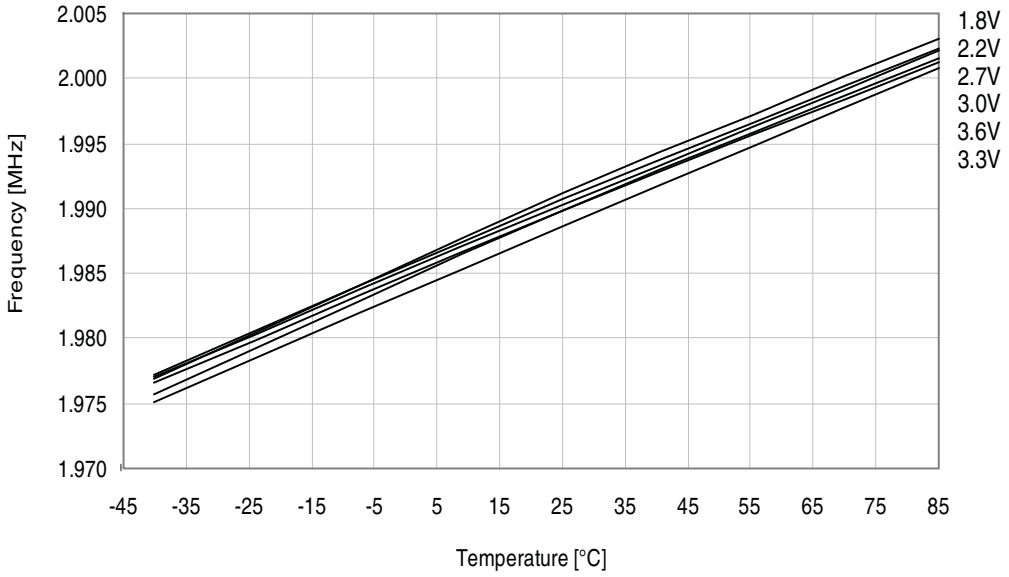
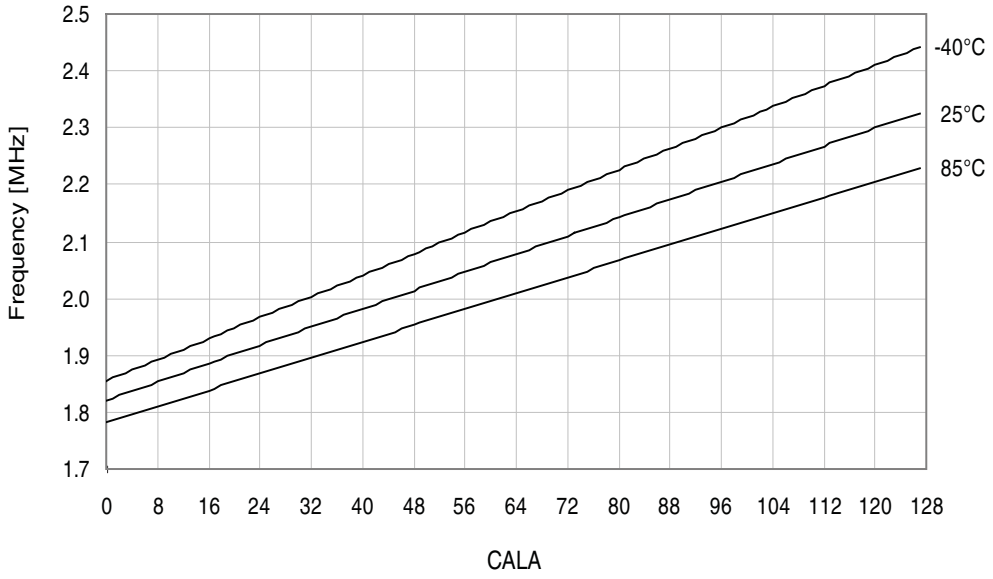


Figure 33-209. 2MHz internal oscillator frequency vs. CALA calibration value.
V_{CC} = 3V.



33.4.8.4 32MHz internal oscillator

Figure 33-210. 32MHz internal oscillator frequency vs. temperature.
DFLL disabled.

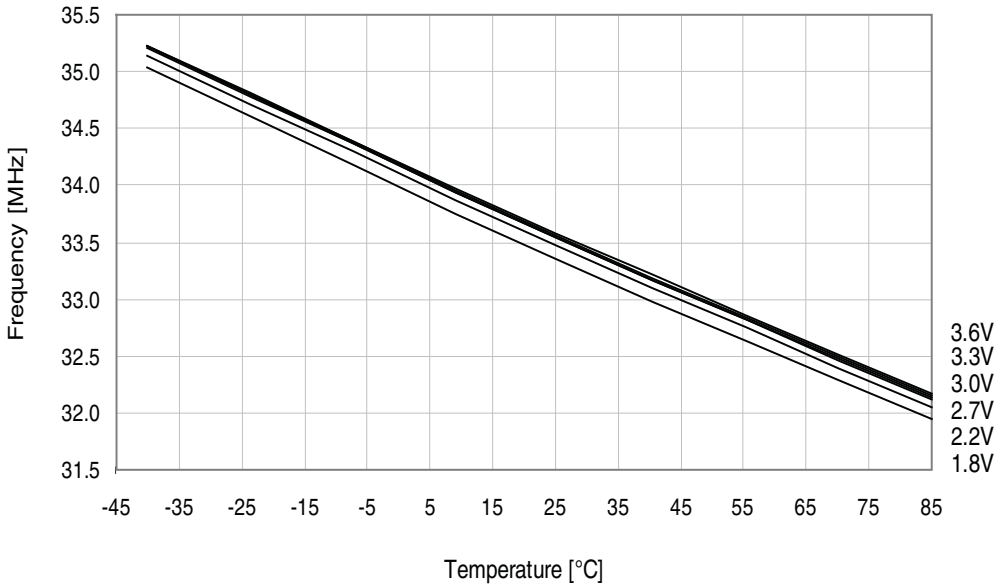


Figure 33-211. 32MHz internal oscillator frequency vs. temperature.
DFLL enabled, from the 32.768kHz internal oscillator.

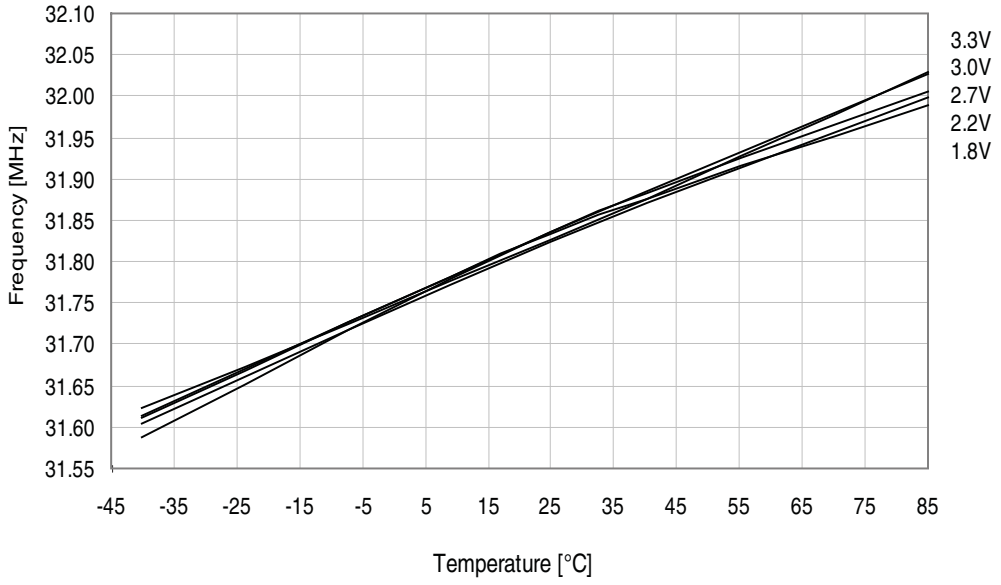


Figure 33-212. 32MHz internal oscillator CALA calibration step size.
V_{CC} = 3.0V.

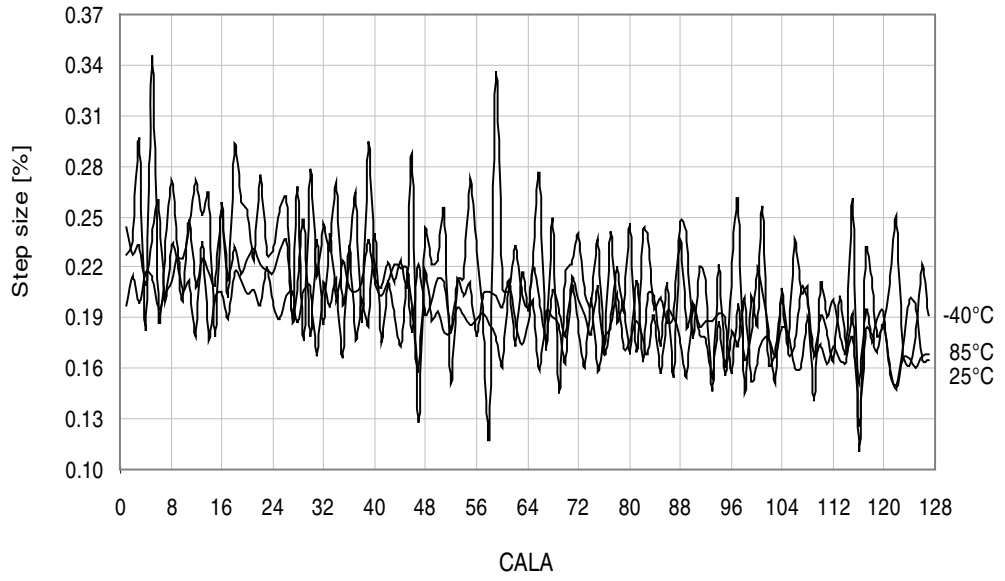
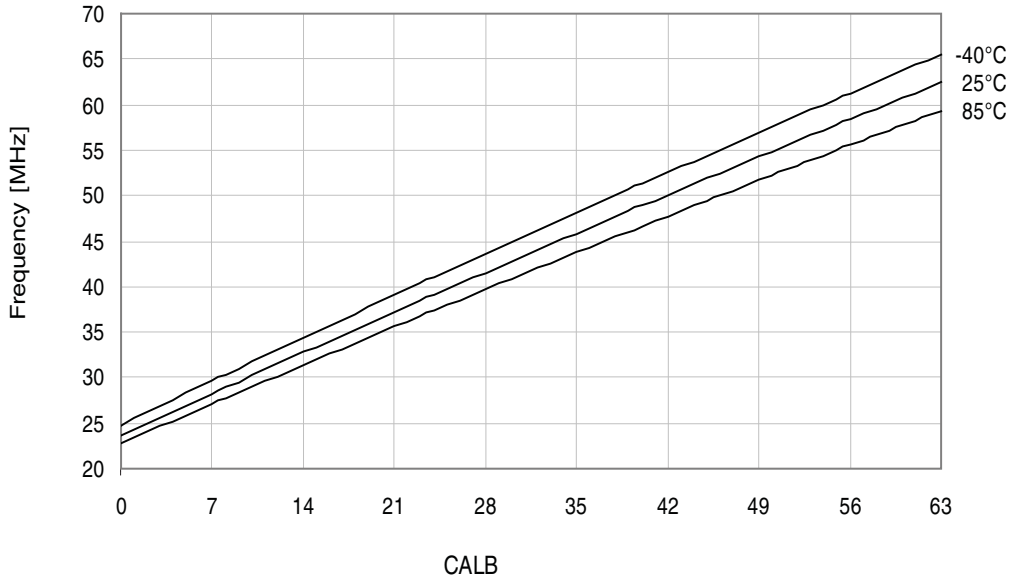


Figure 33-213. 32MHz internal oscillator frequency vs. CALB calibration value.
V_{CC} = 3.0V.



33.4.8.5 32MHz internal oscillator calibrated to 48MHz

Figure 33-214. 48MHz internal oscillator frequency vs. temperature.
DFLL disabled.

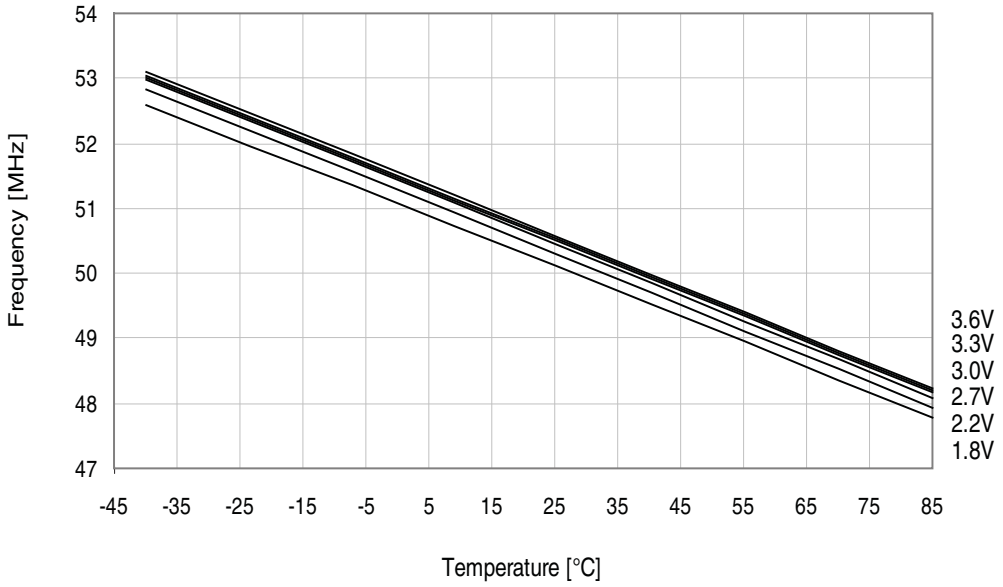
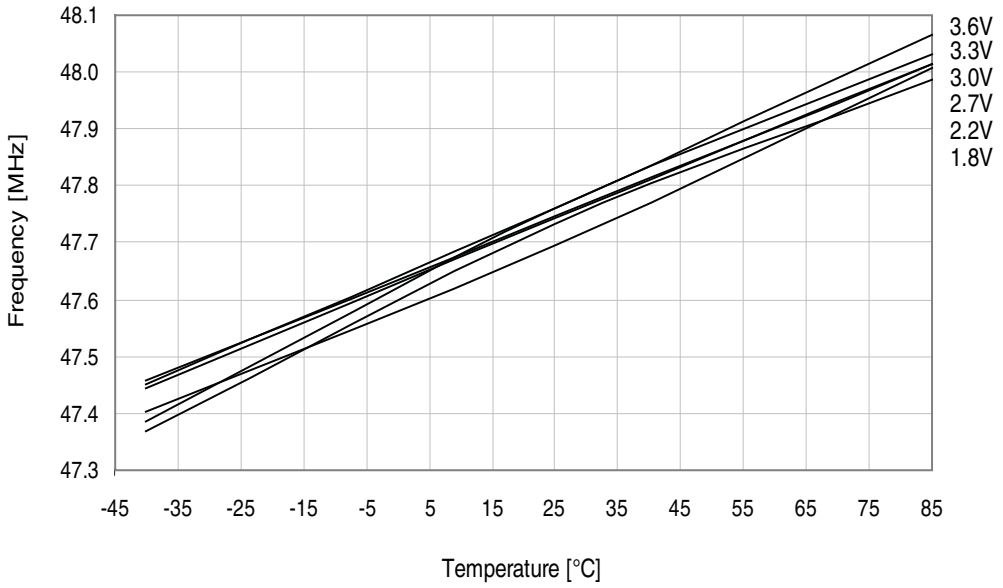


Figure 33-215. 48MHz internal oscillator frequency vs. temperature.
DFLL enabled, from the 32.768kHz internal oscillator.



33.4.9 Two-wire interface characteristics

Figure 33-216. SDA hold time vs. temperature.

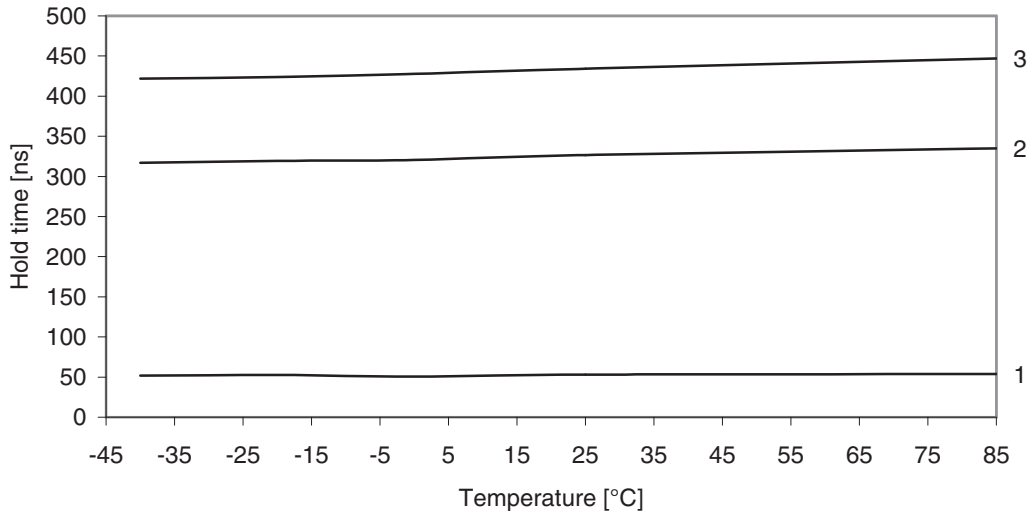
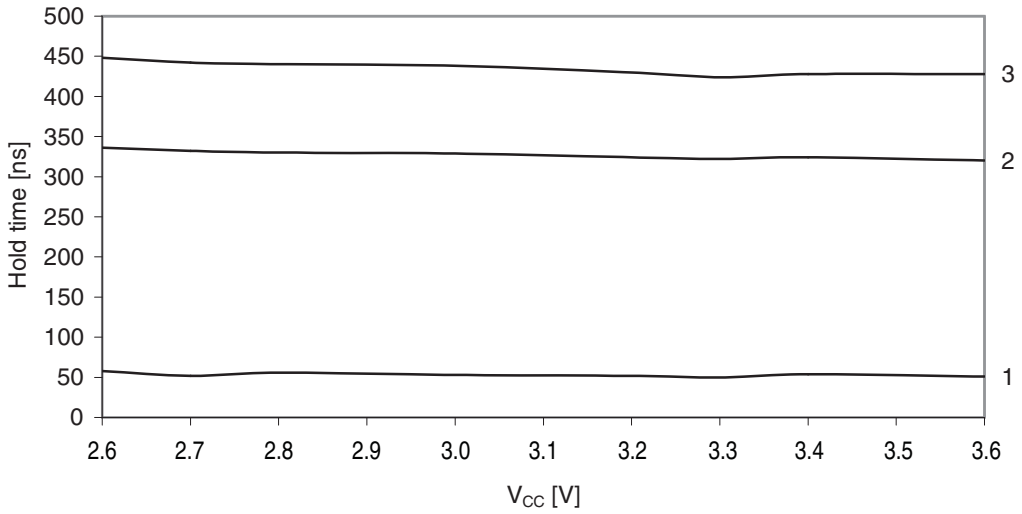
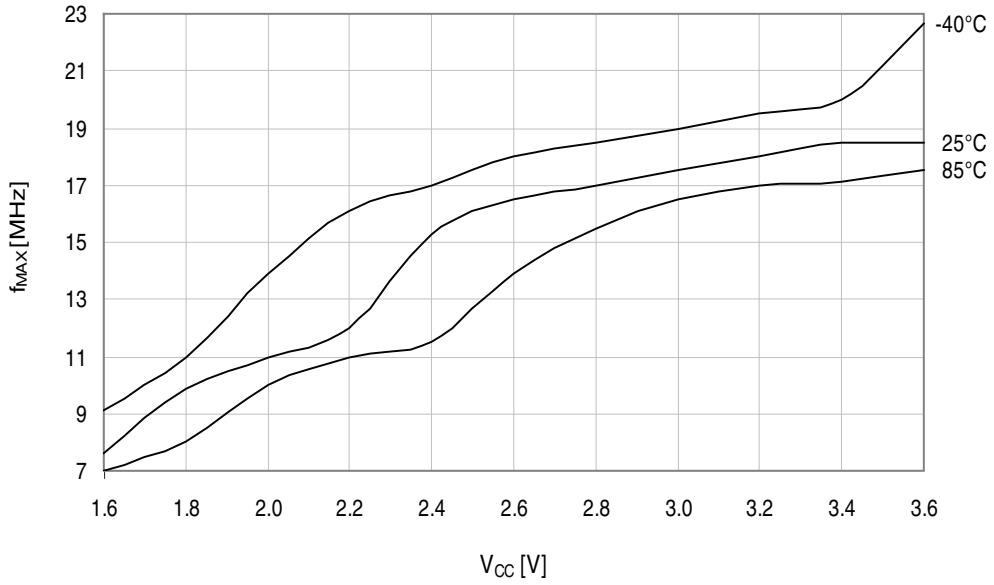


Figure 33-217. SDA hold time vs. supply voltage.



33.4.10 PDI characteristics

Figure 33-218. Maximum PDI frequency vs. V_{CC}.



33.5 Atmel ATxmega256D3

33.5.1 Current consumption

33.5.1.1 Active mode supply current

Figure 33-219. Active supply current vs. frequency.
f_{SYS} = 0 - 1MHz external clock, T = 25°C.

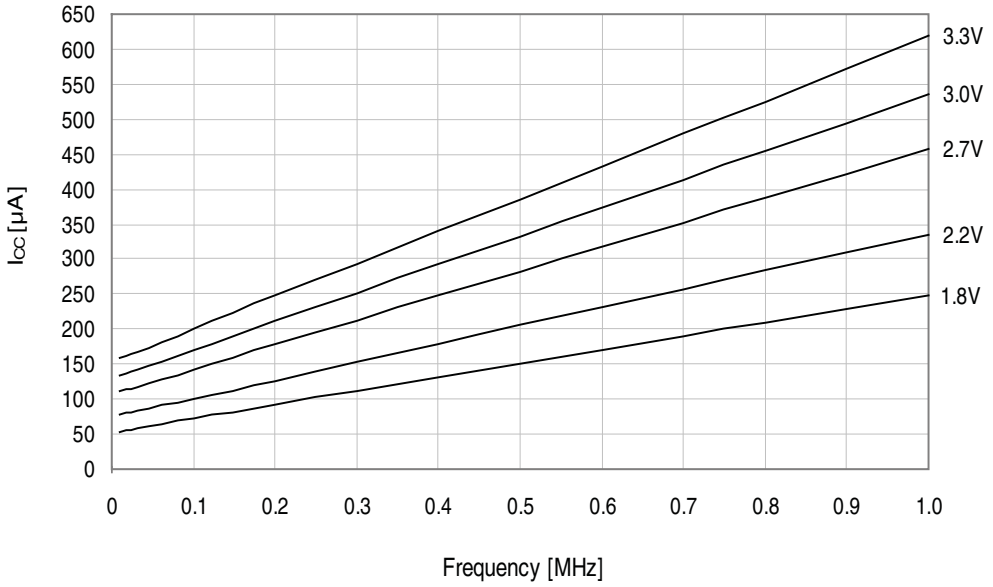


Figure 33-220. Active supply current vs. frequency.
f_{SYS} = 1 - 32MHz external clock, T = 25°C.

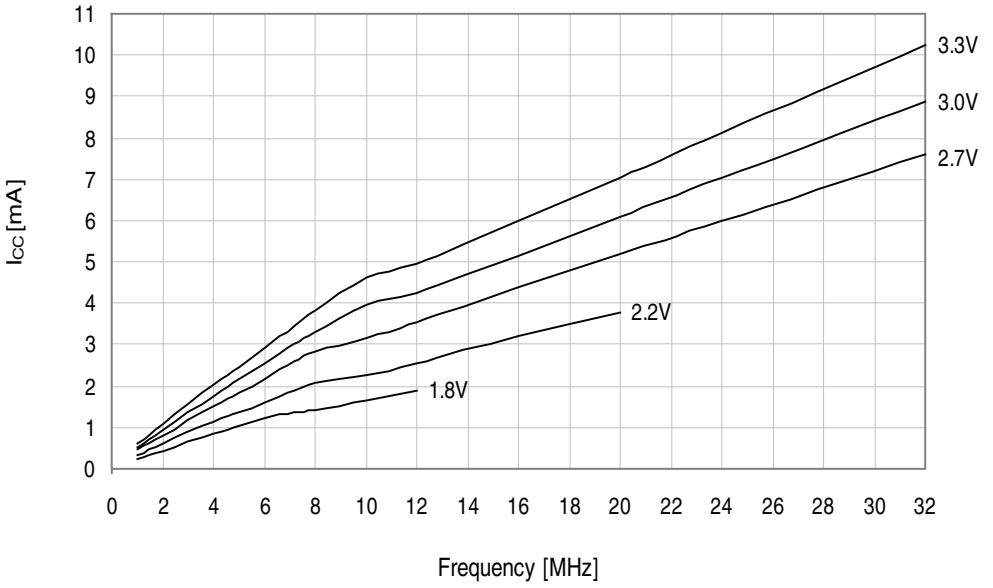


Figure 33-221. Active mode supply current vs. V_{CC}.
f_{SYS} = 32.768kHz internal oscillator.

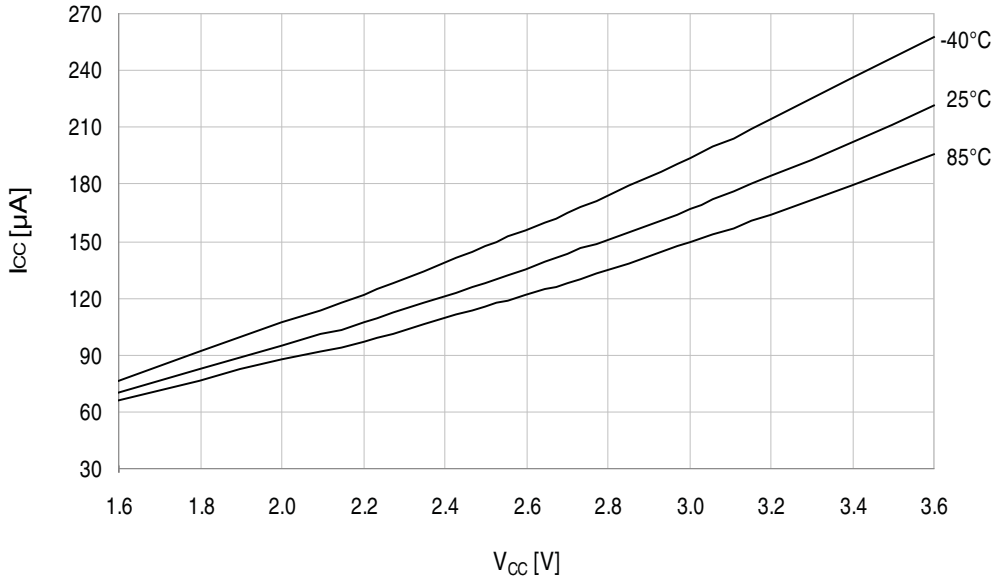


Figure 33-222. Active mode supply current vs. V_{CC}.
f_{SYS} = 1MHz external clock.

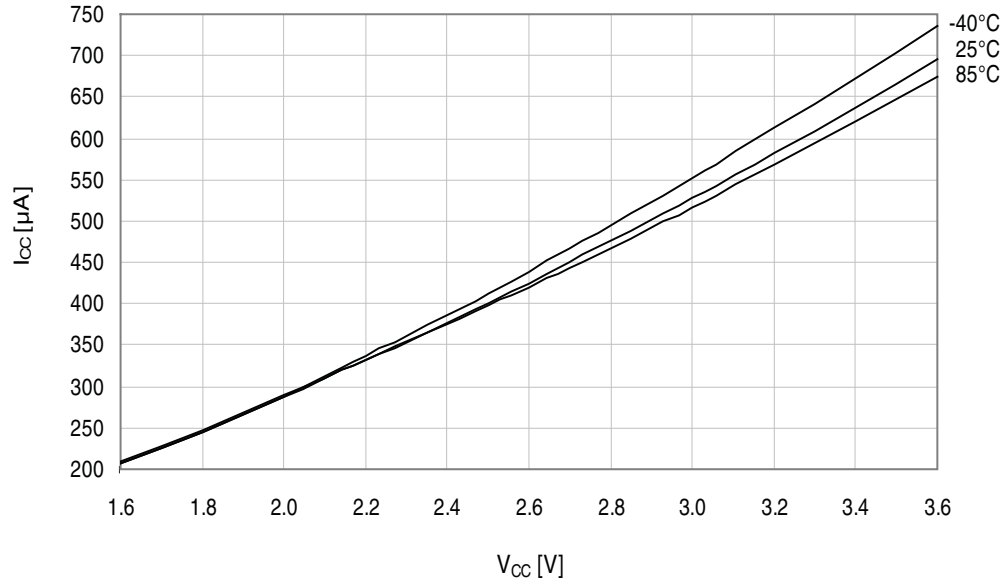


Figure 33-223. Active mode supply current vs. V_{CC}.
f_{SYS} = 2MHz internal oscillator.

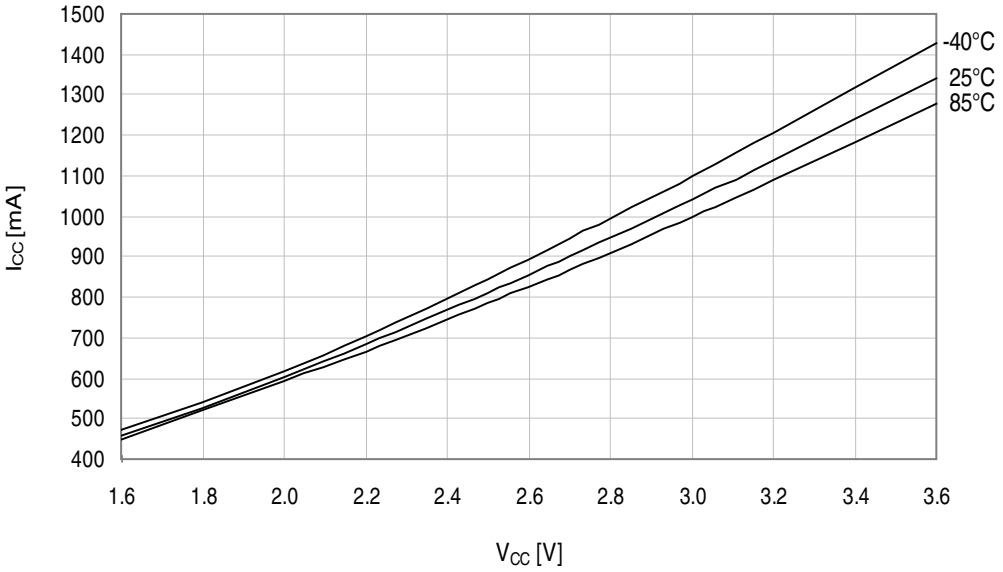


Figure 33-224. Active mode supply current vs. V_{CC}.
f_{SYS} = 32MHz internal oscillator prescaled to 8MHz.

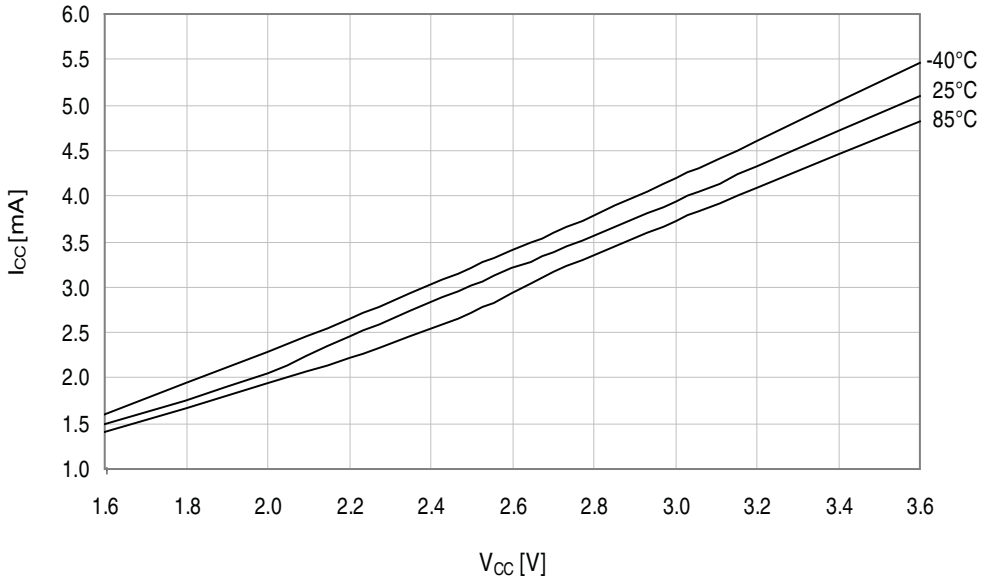
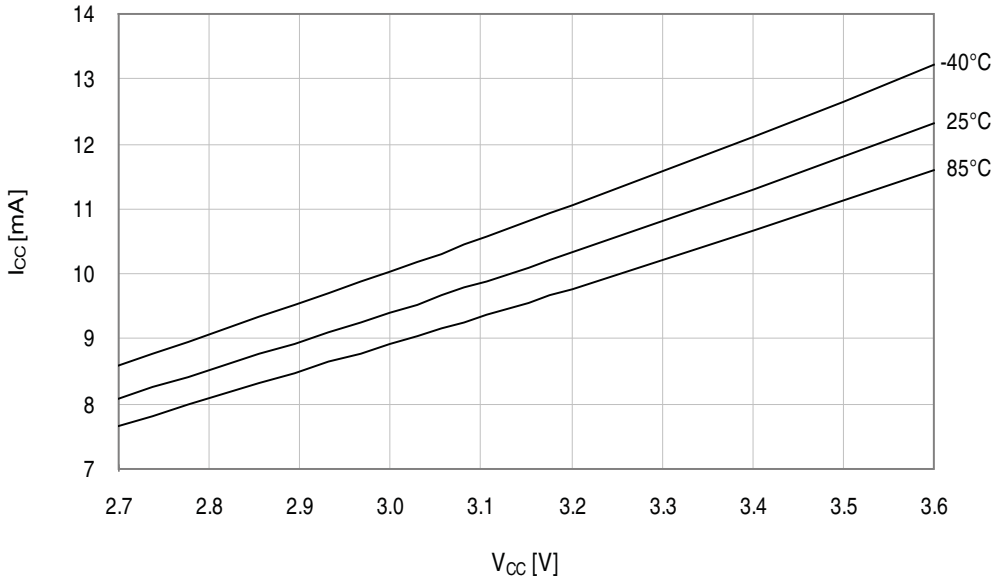


Figure 33-225. Active mode supply current vs. V_{CC}.
f_{SYS} = 32MHz internal oscillator.



33.5.1.2 Idle mode supply current

Figure 33-226. Idle mode supply current vs. frequency.
f_{SYS} = 0 - 1MHz external clock, T = 25°C.

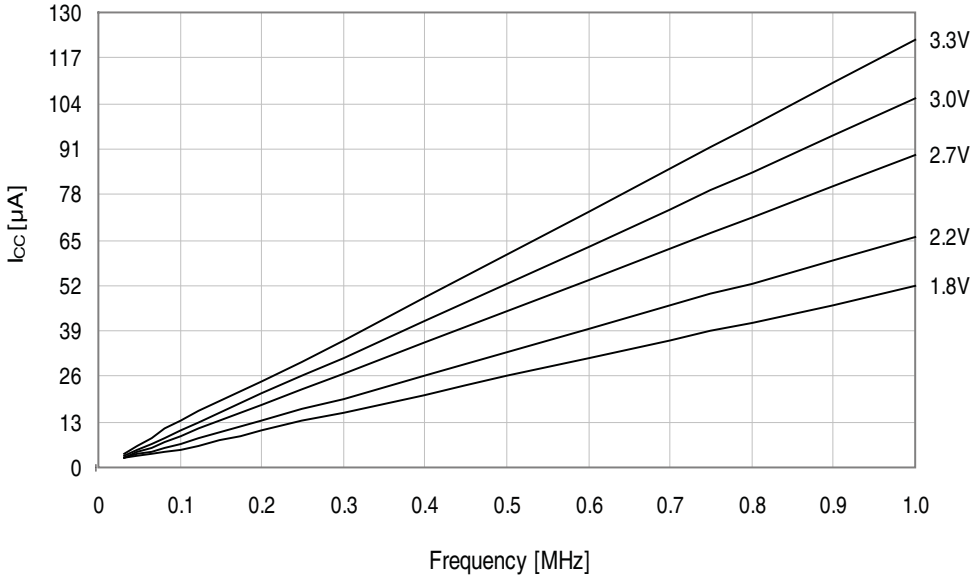


Figure 33-227. Idle mode supply current vs. frequency.
f_{SYS} = 1 - 32MHz external clock, T = 25°C.

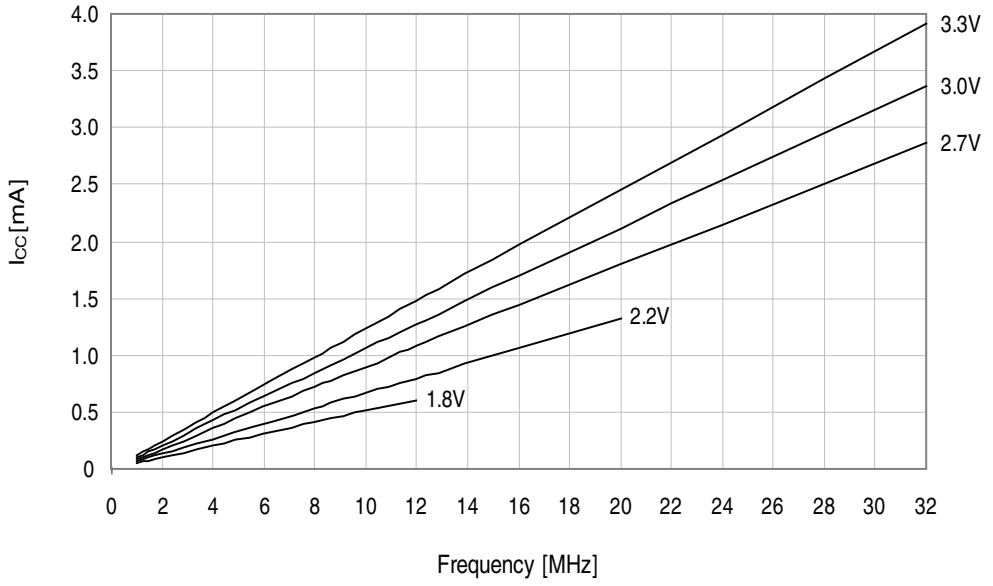


Figure 33-228. Idle mode supply current vs. V_{CC}.
f_{SYS} = 32.768kHz internal oscillator.

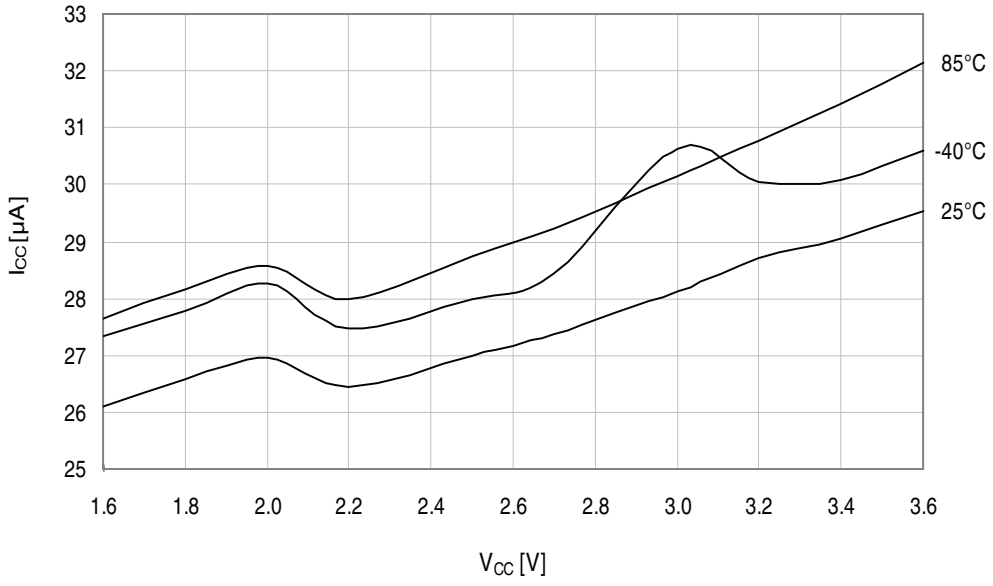


Figure 33-229. Idle mode supply current vs. V_{CC}.
f_{SYS} = 1MHz external clock.

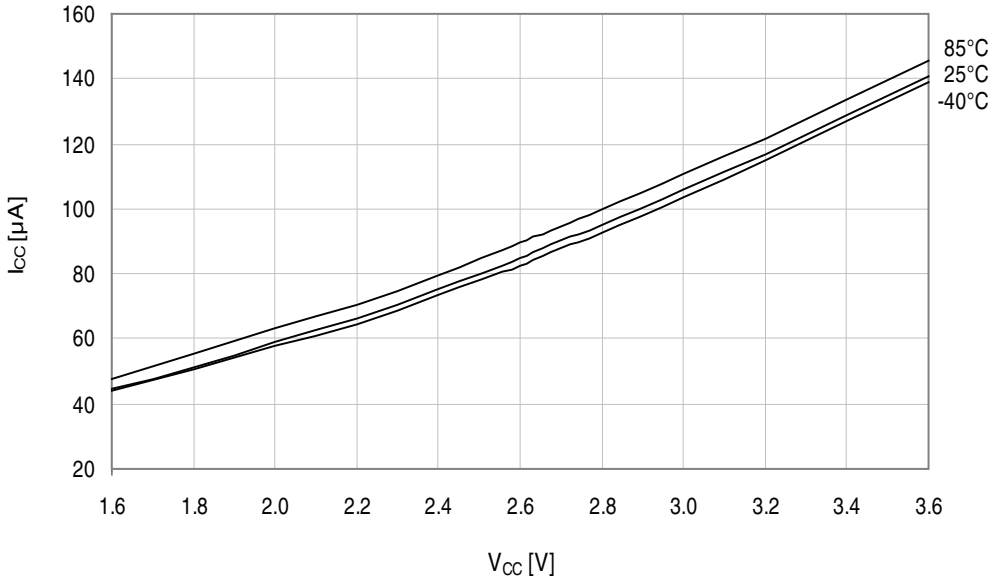


Figure 33-230. Idle mode supply current vs. V_{CC}.
f_{SYS} = 2MHz internal oscillator.

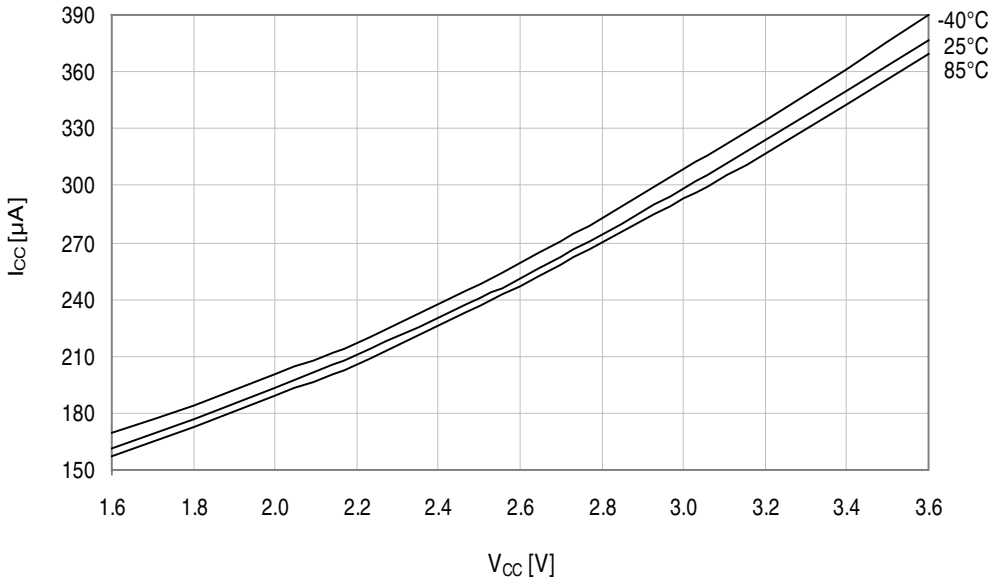


Figure 33-231. Idle mode supply current vs. V_{CC}.
f_{SYS} = 32MHz internal oscillator prescaled to 8MHz.

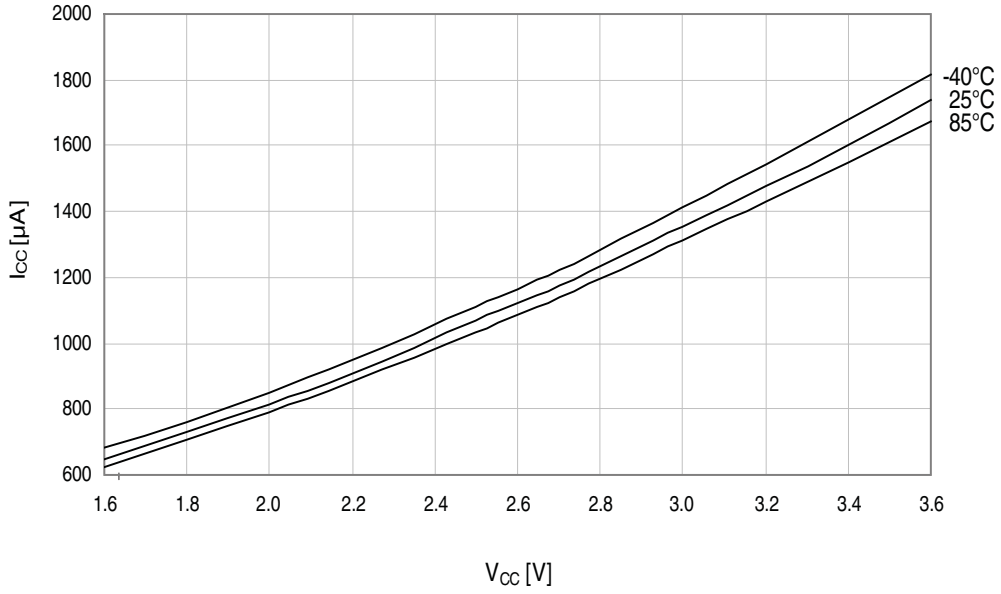
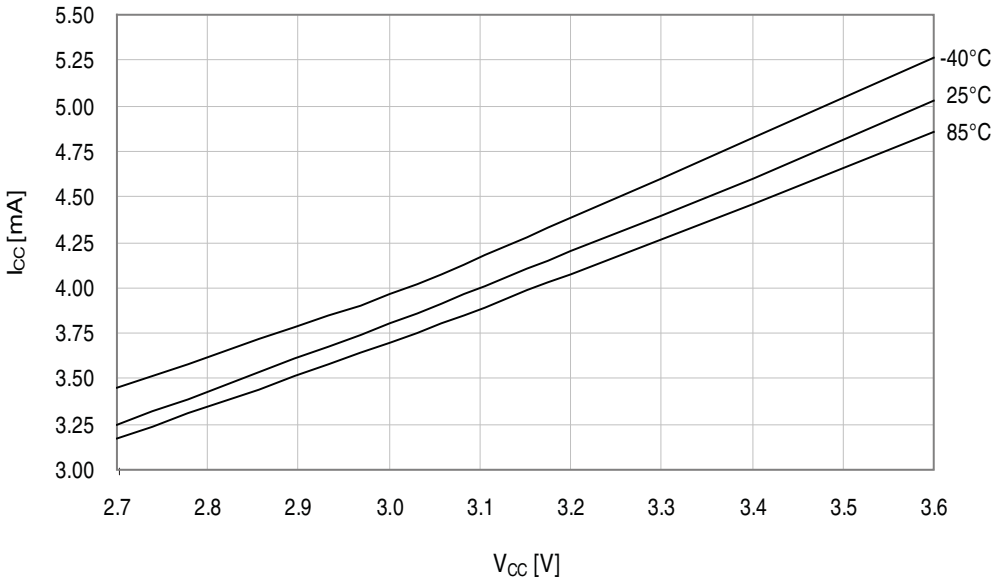


Figure 33-232. Idle mode current vs. V_{CC}.
f_{SYS} = 32MHz internal oscillator.



33.5.1.3 Power-down mode supply current

Figure 33-233. Power-down mode supply current vs. V_{CC}.
All functions disabled.

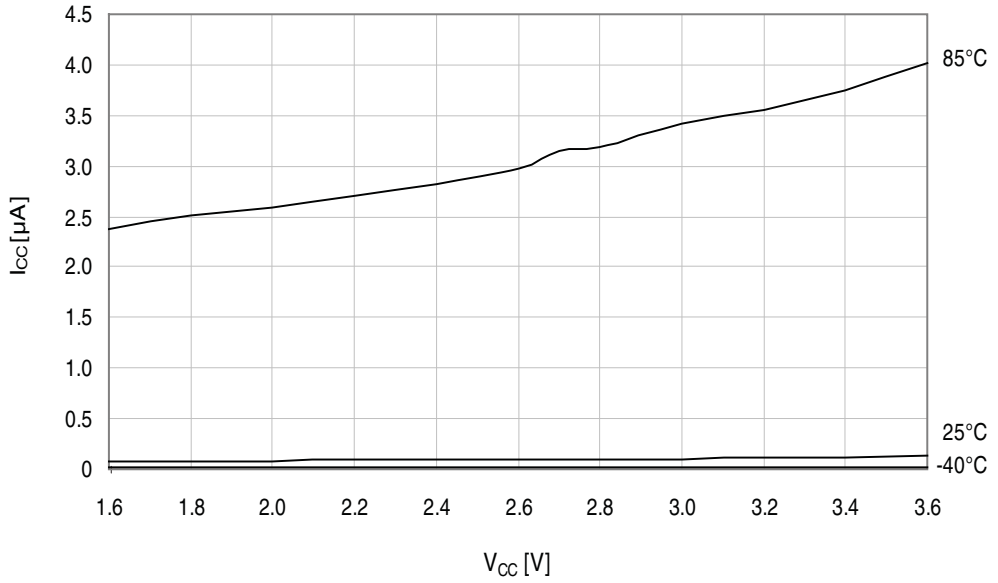


Figure 33-234. Power-down mode supply current vs. V_{CC}.
Watchdog and sampled BOD enabled.

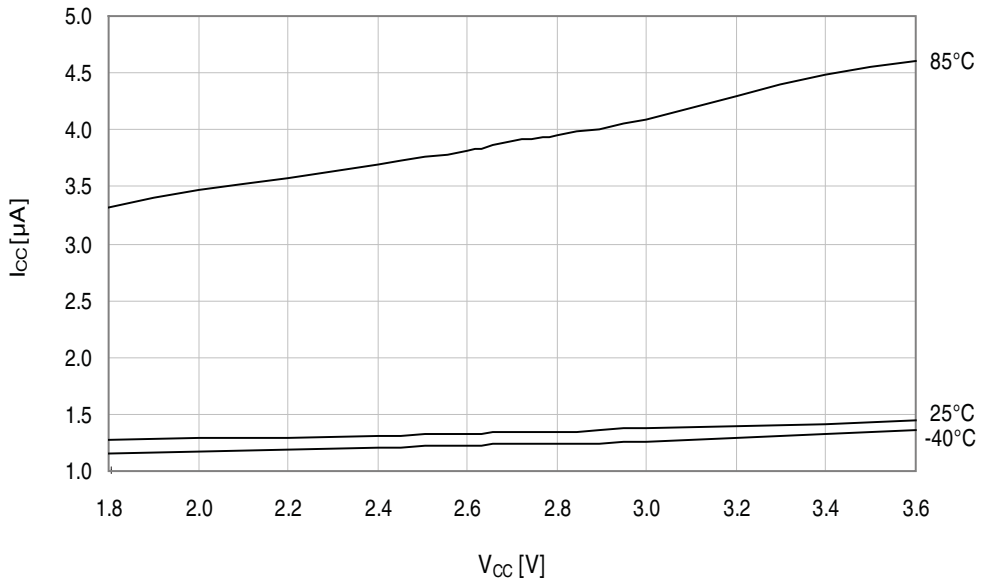
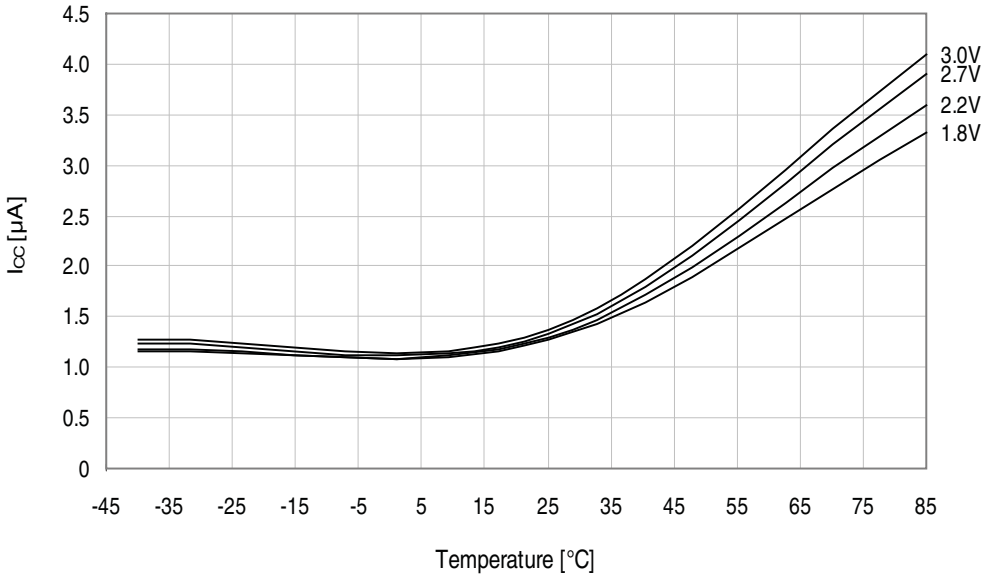


Figure 33-235. Power-down mode supply current vs. temperature.
Watchdog and sampled BOD enabled and running from internal ULP oscillator.



33.5.2 I/O pin characteristics

The I/O pins complies with the JEDEC LVTTL and LVCMOS specification and the high- and low level input and output voltage limits reflect or exceed this specification.

33.5.2.1 Pull-up

Figure 33-236. I/O pin pull-up resistor current vs. input voltage.
V_{CC} = 1.8V.

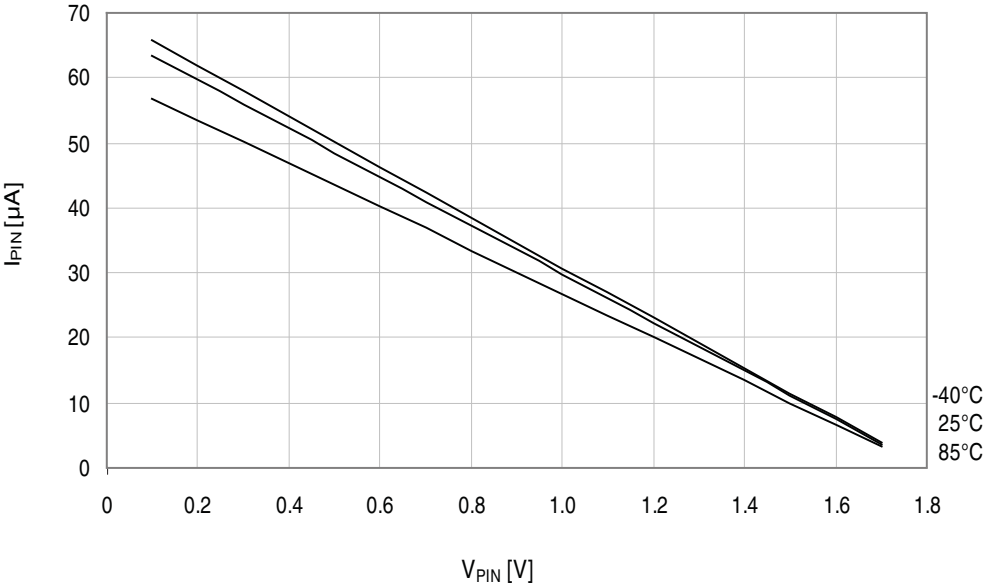


Figure 33-237. I/O pin pull-up resistor current vs. input voltage.
V_{CC} = 3.0V.

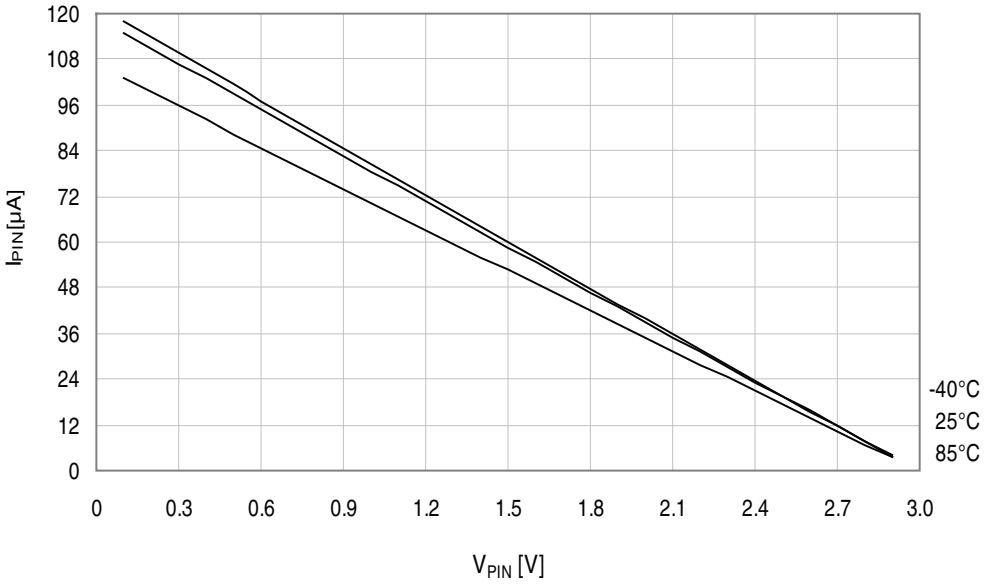
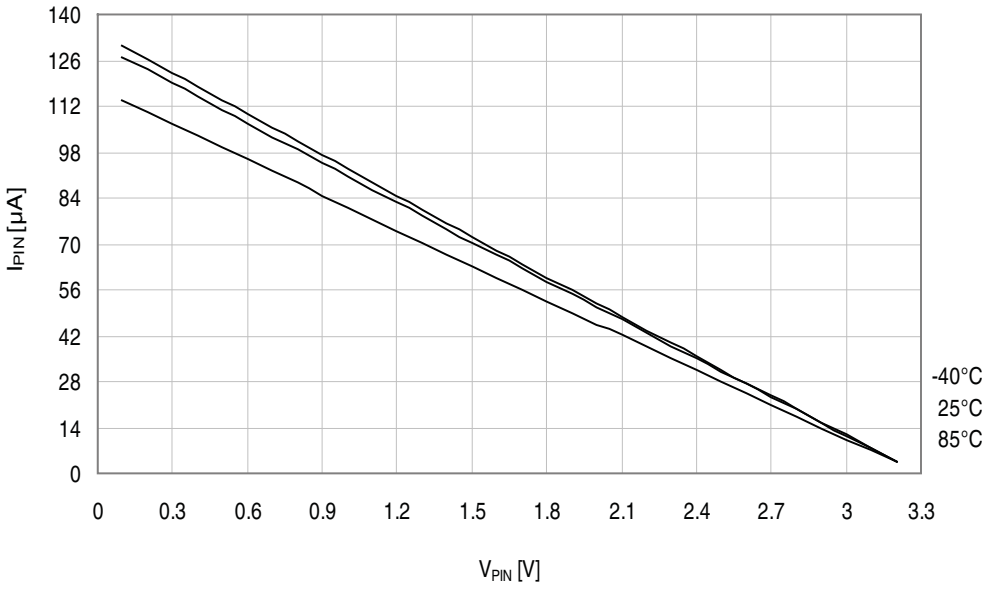


Figure 33-238. I/O pin pull-up resistor current vs. input voltage.
V_{CC} = 3.3V.



33.5.2.2 Output voltage vs. sink/source current

Figure 33-239. I/O pin output voltage vs. source current.
V_{CC} = 1.8V.

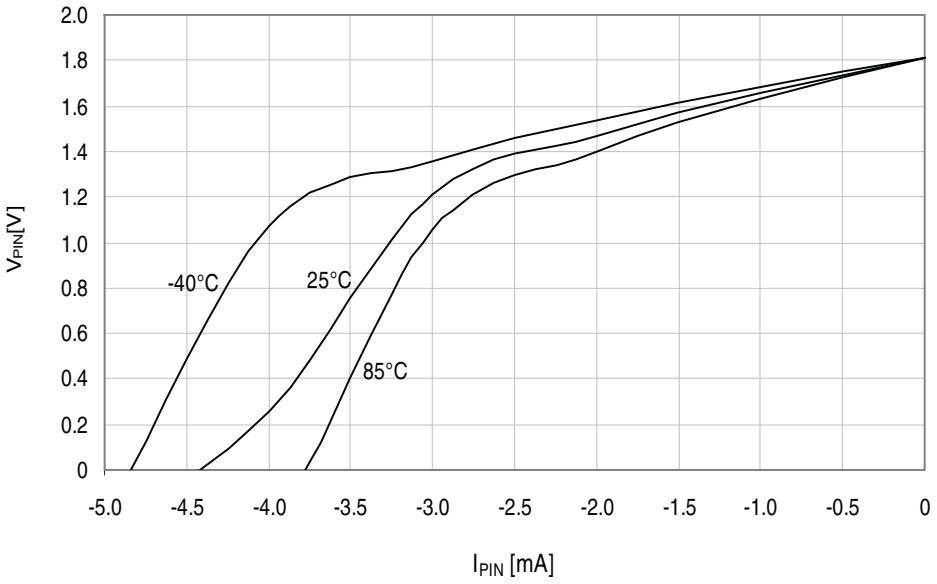


Figure 33-240. I/O pin output voltage vs. source current.
V_{CC} = 3.0V.

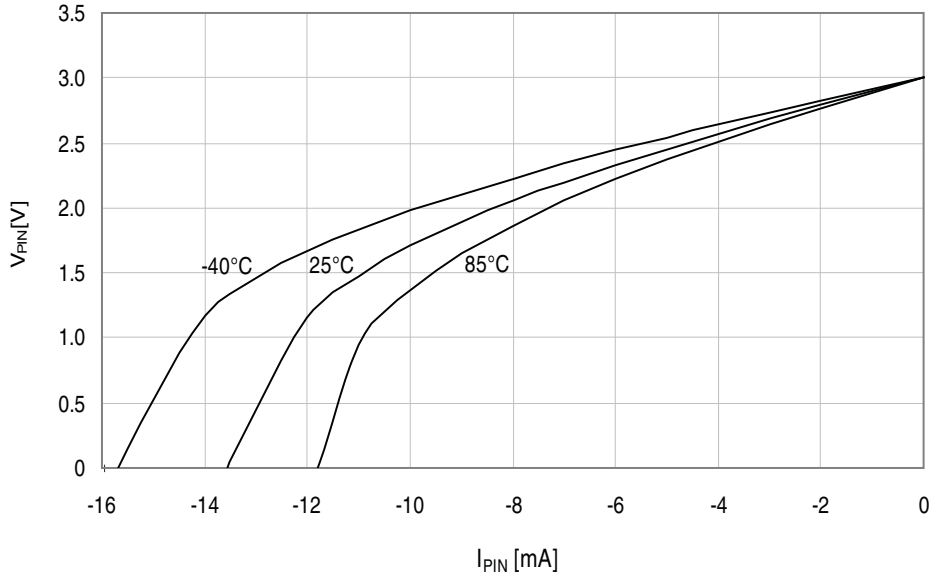


Figure 33-241. I/O pin output voltage vs. source current.
V_{CC} = 3.3V.

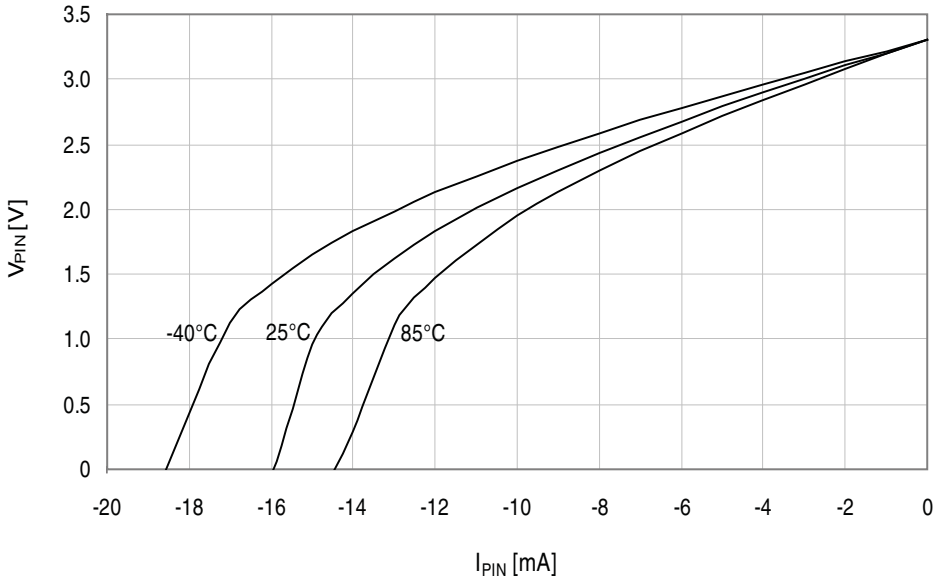


Figure 33-242. I/O pin output voltage vs. sink current.
V_{CC} = 1.8V.

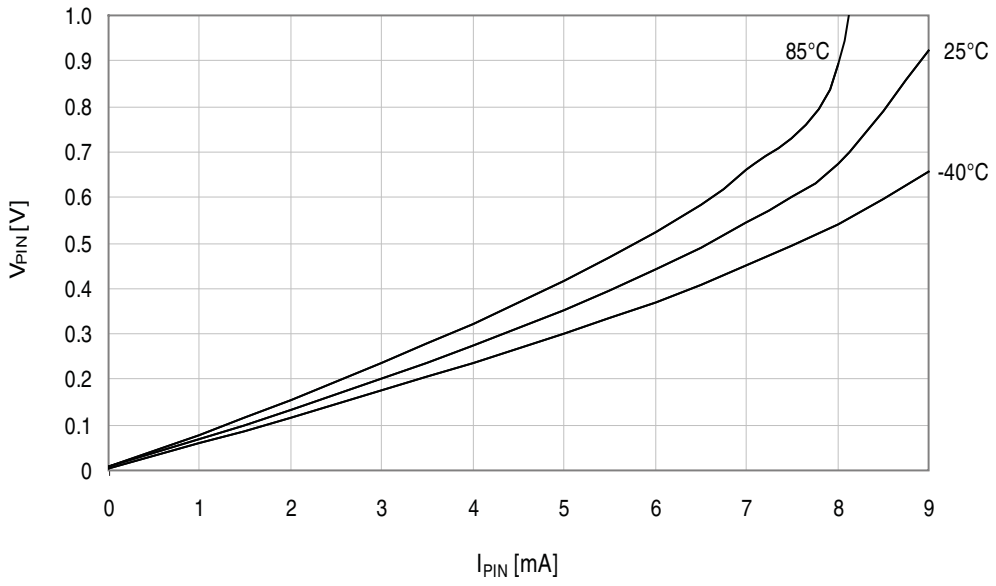


Figure 33-243. I/O pin output voltage vs. sink current.
V_{CC} = 3.0V.

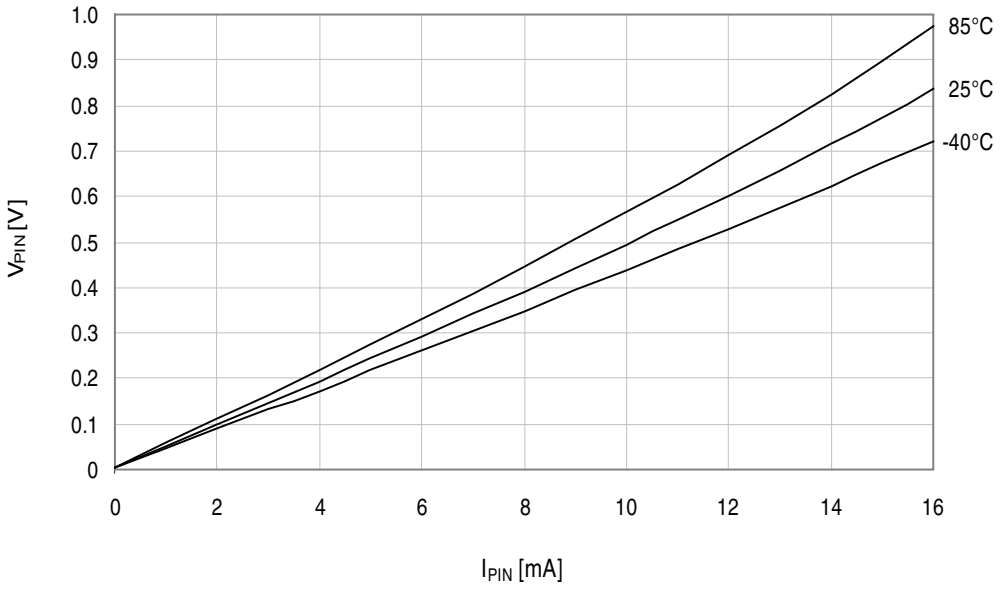
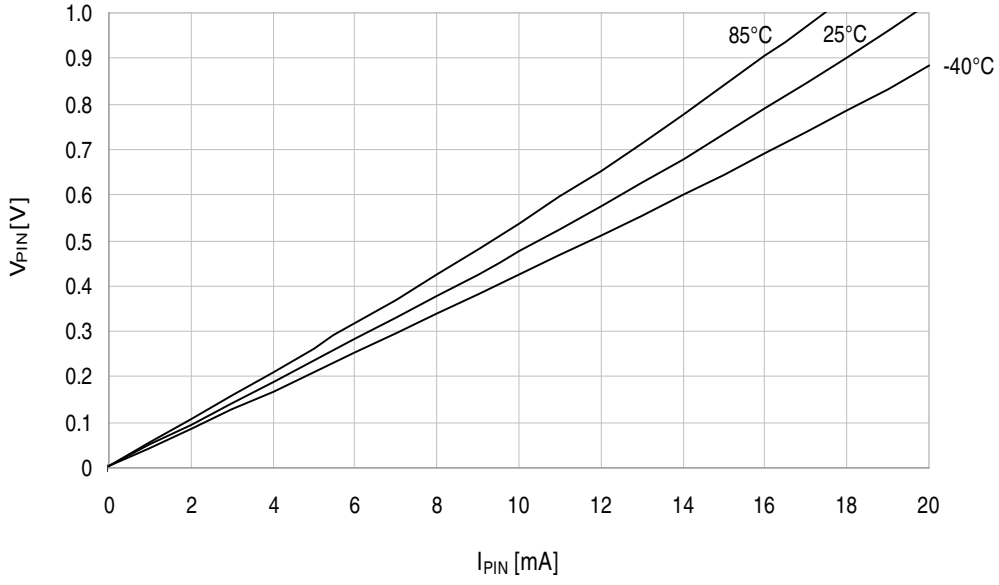


Figure 33-244. I/O pin output voltage vs. sink current.
V_{CC} = 3.3V.



33.5.2.3 Thresholds and hysteresis

Figure 33-245. I/O pin input threshold voltage vs. V_{CC}.
V_{IH} I/O pin read as "1".

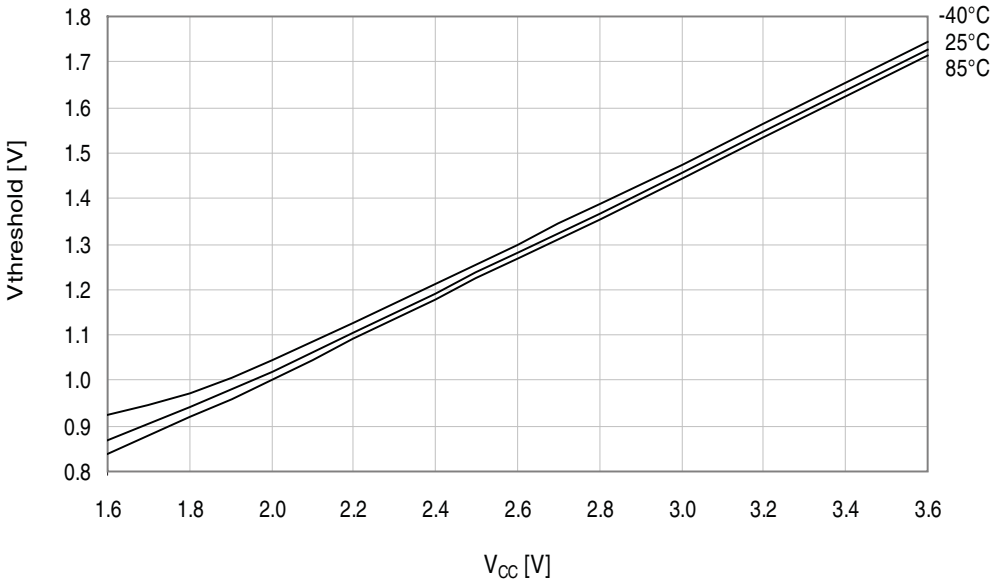


Figure 33-246. I/O pin input threshold voltage vs. V_{CC}.
V_{IL} I/O pin read as "0".

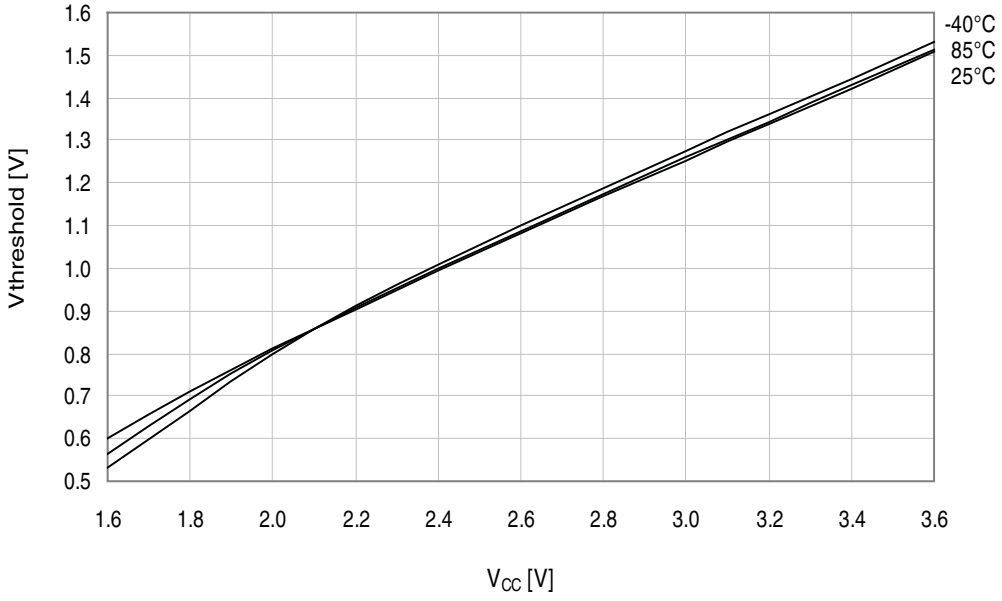
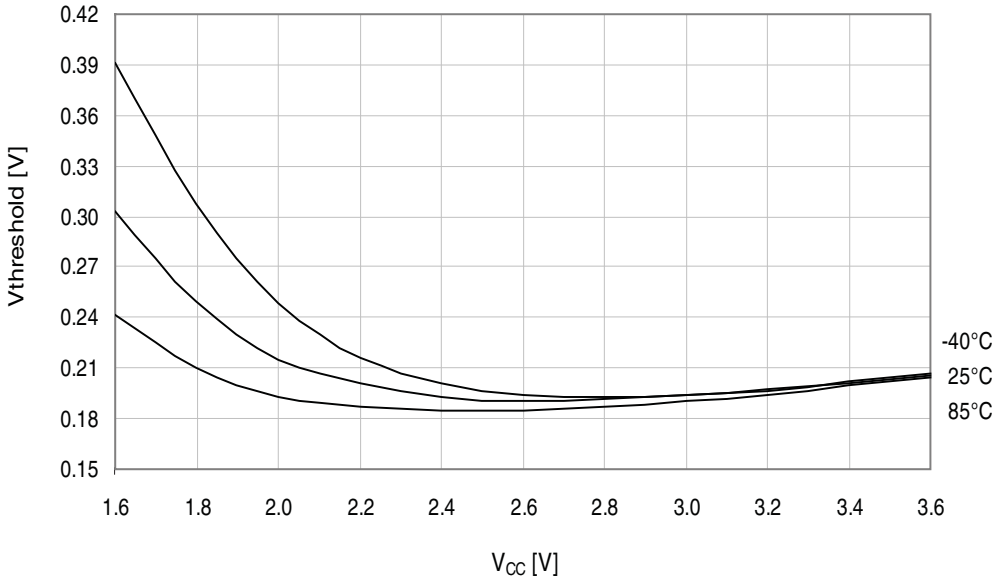


Figure 33-247. I/O pin input hysteresis vs. V_{CC}.



33.5.3 ADC characteristics

Figure 33-248. INL error vs. external V_{REF}.
T = 25°C, V_{CC} = 3.6V, external reference.

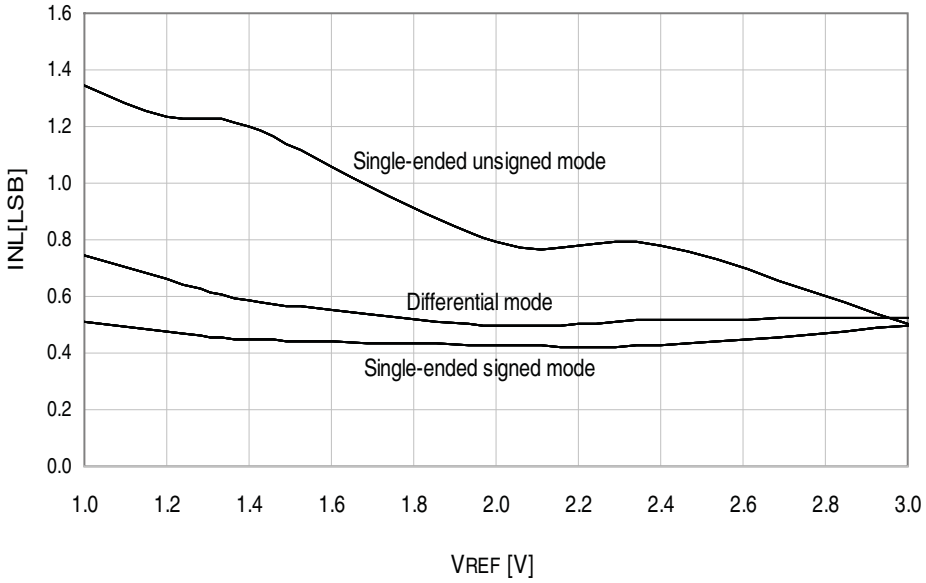


Figure 33-249. INL error vs. sample rate.

T = 25°C, V_{CC} = 3.6V, V_{REF} = 3.0V external.

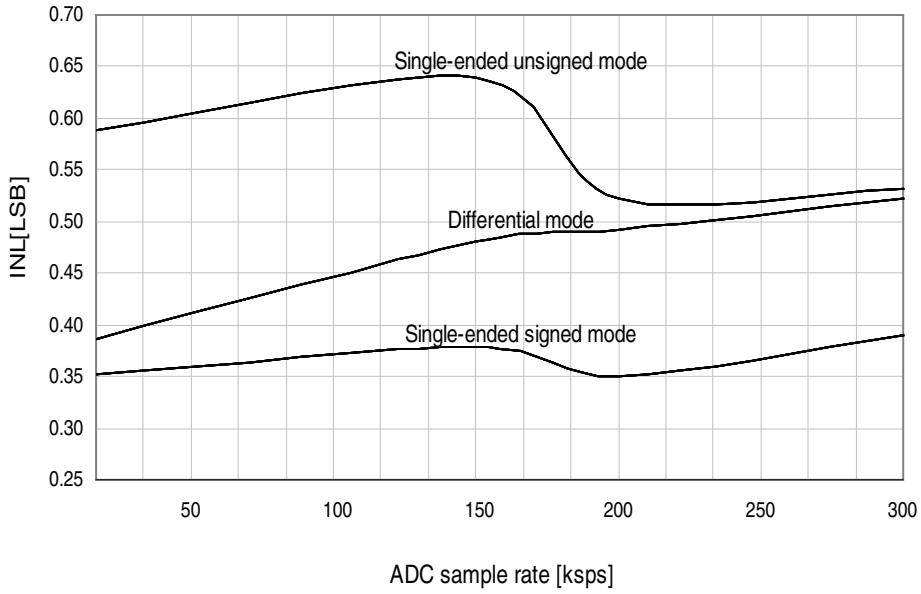


Figure 33-250. INL error vs. input code.

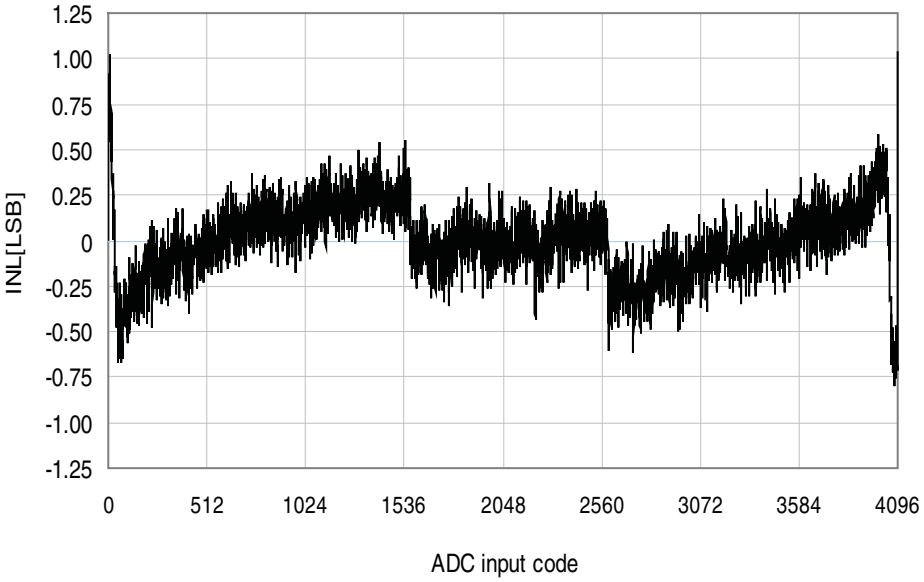


Figure 33-251. DNL error vs. external V_{REF}.

T = 25°C, V_{CC} = 3.6V, external reference.

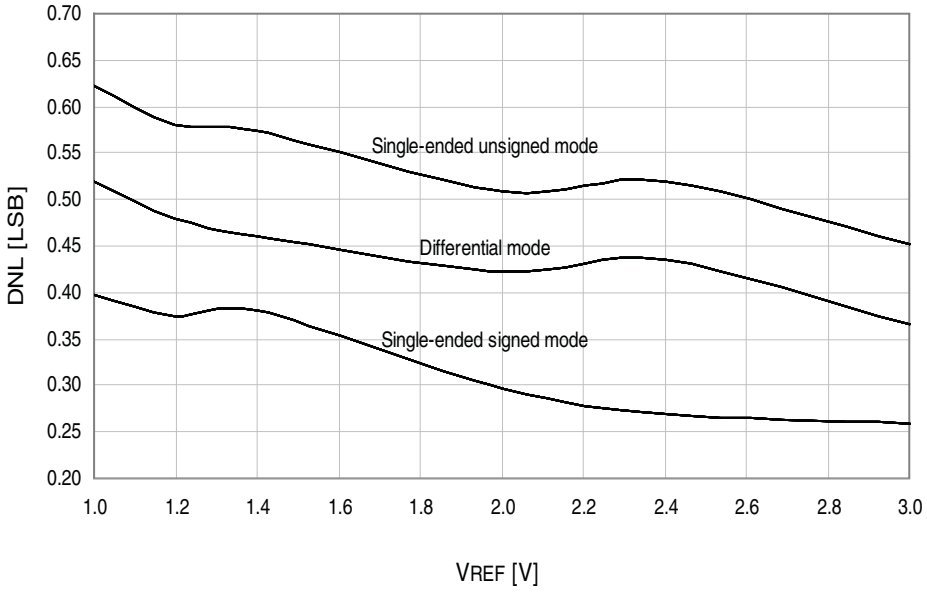


Figure 33-252. DNL error vs. sample rate.

T = 25°C, V_{CC} = 3.6V, V_{REF} = 3.0V external.

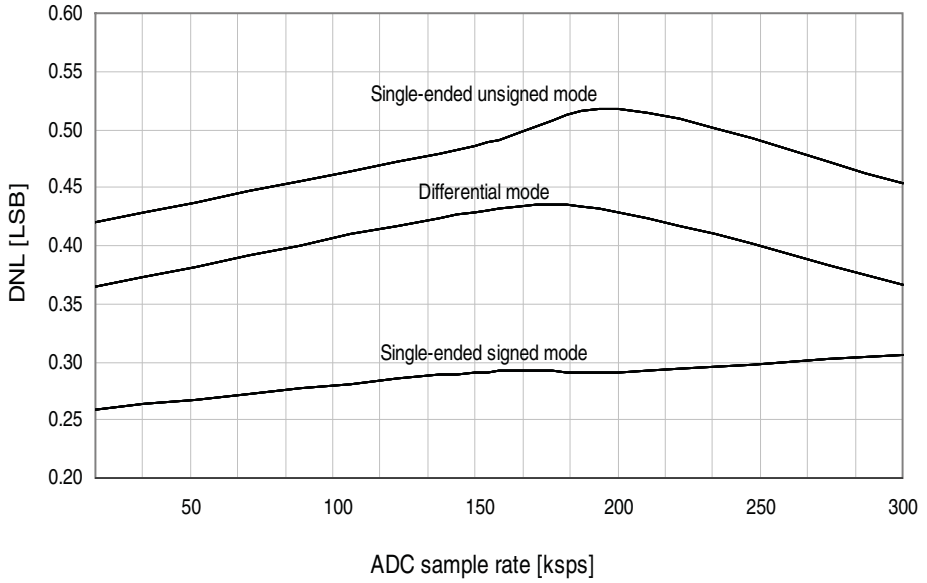


Figure 33-253. DNL error vs. input code.

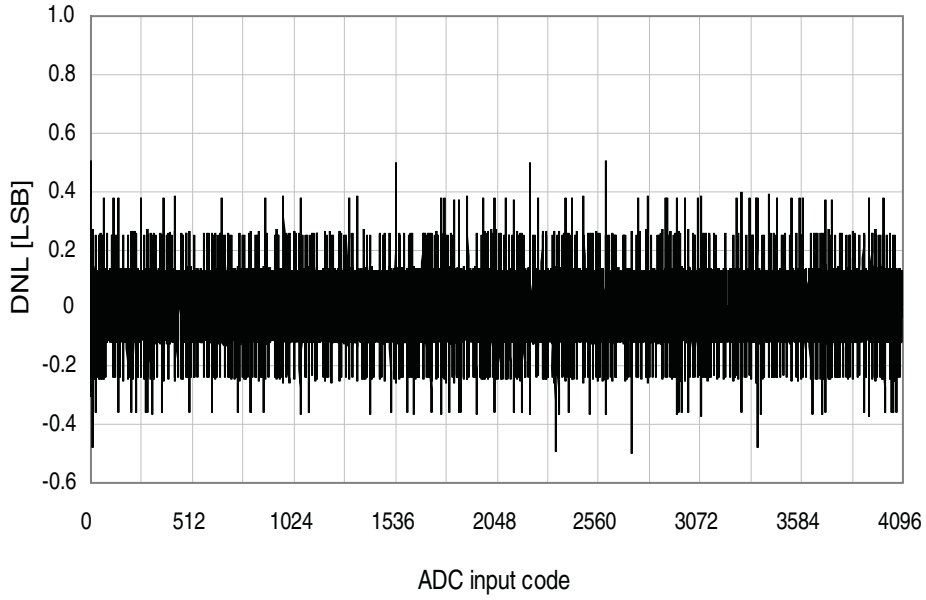


Figure 33-254. Gain error vs. V_{REF}.
T = 25°C, V_{CC} = 3.6V, ADC sample rate = 300ksps.

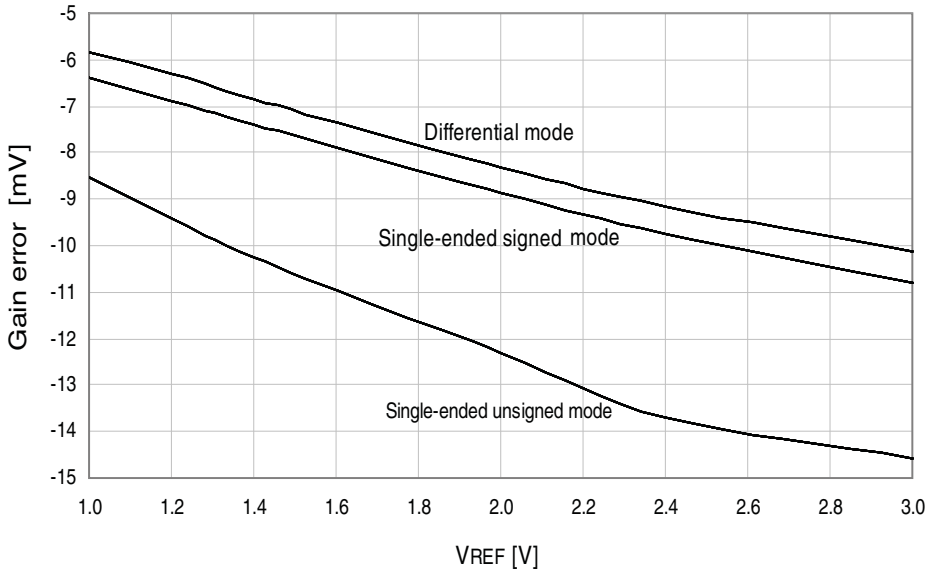


Figure 33-255. Gain error vs. V_{CC}.

T = 25°C, V_{REF} = external 1.0V, ADC sample rate = 300ksps.

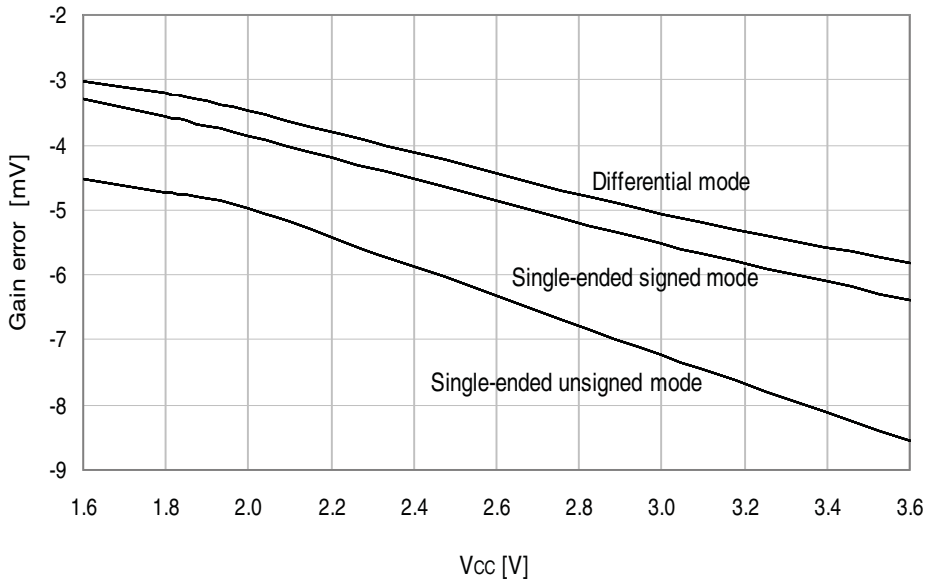


Figure 33-256. Offset error vs. V_{REF}.

T = 25°C, V_{CC} = 3.6V, ADC sample rate = 300ksps.

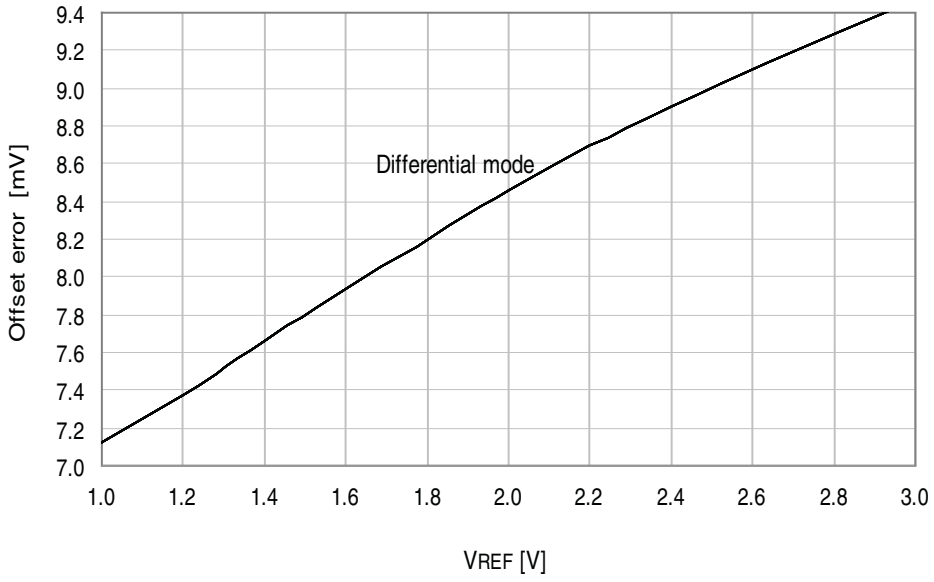


Figure 33-257. Gain error vs. temperature.

V_{CC} = 3.0V, V_{REF} = external 2.0V.

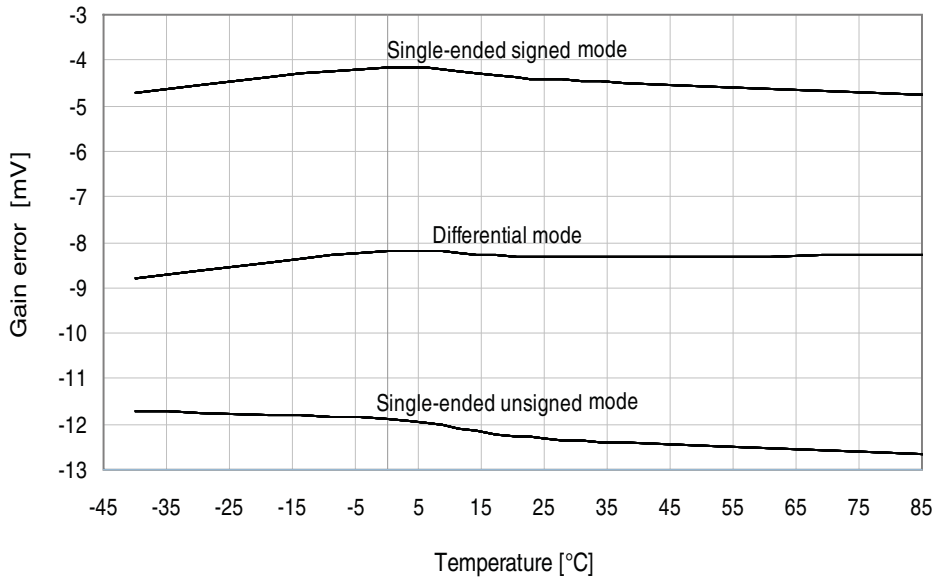
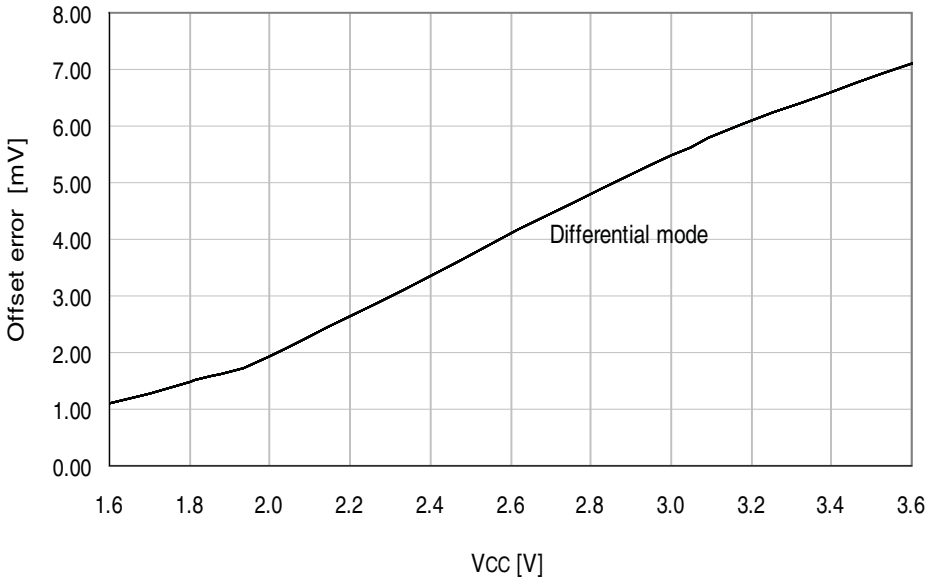


Figure 33-258. Offset error vs. V_{CC}.

T = 25°C, V_{REF} = external 1.0V, ADC sample rate = 300ksps.



33.5.4 Analog comparator characteristics

Figure 33-259. Analog comparator hysteresis vs. V_{CC}.
Small hysteresis.

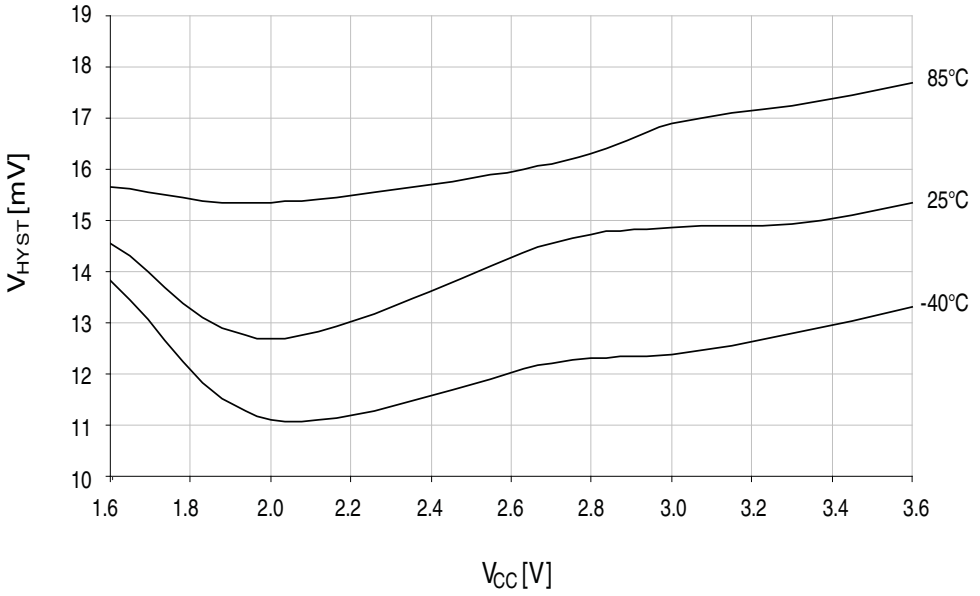


Figure 33-260. Analog comparator hysteresis vs. V_{CC}.
Large hysteresis.

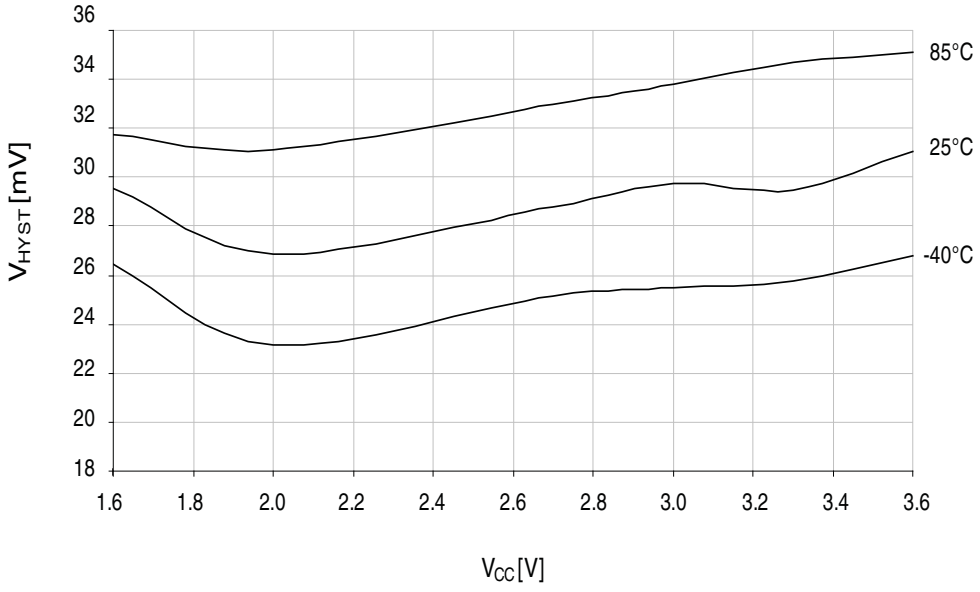


Figure 33-261. Analog comparator current source vs. calibration value.
V_{CC} = 3.0V.

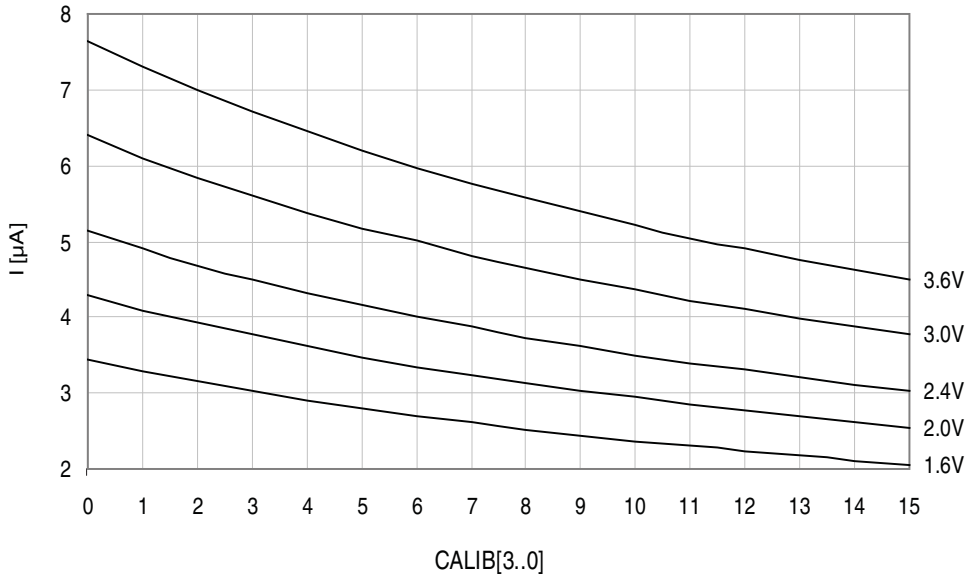
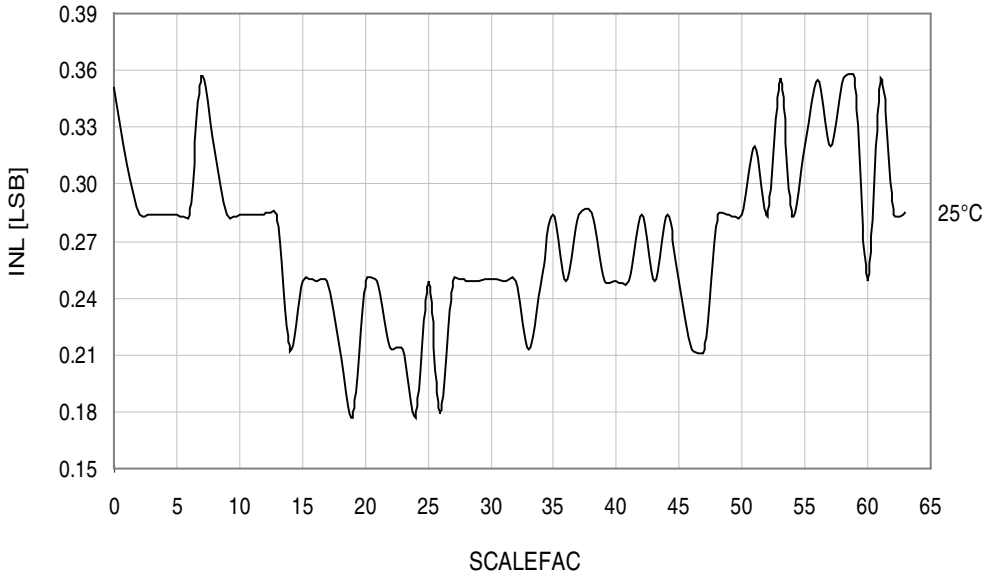
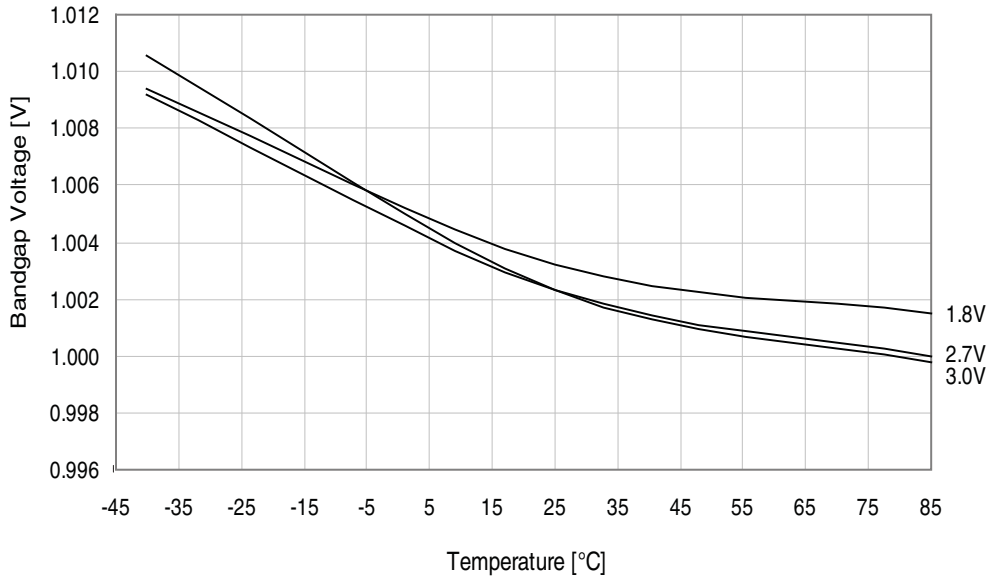


Figure 33-262. Voltage scaler INL vs. SCALEFAC.
T = 25°C, V_{CC} = 3.0V.



33.5.5 Internal 1.0V reference characteristics

Figure 33-263. ADC Internal 1.0V reference vs. temperature.



33.5.6 BOD characteristics

Figure 33-264. BOD thresholds vs. temperature.
BOD level = 1.6V.

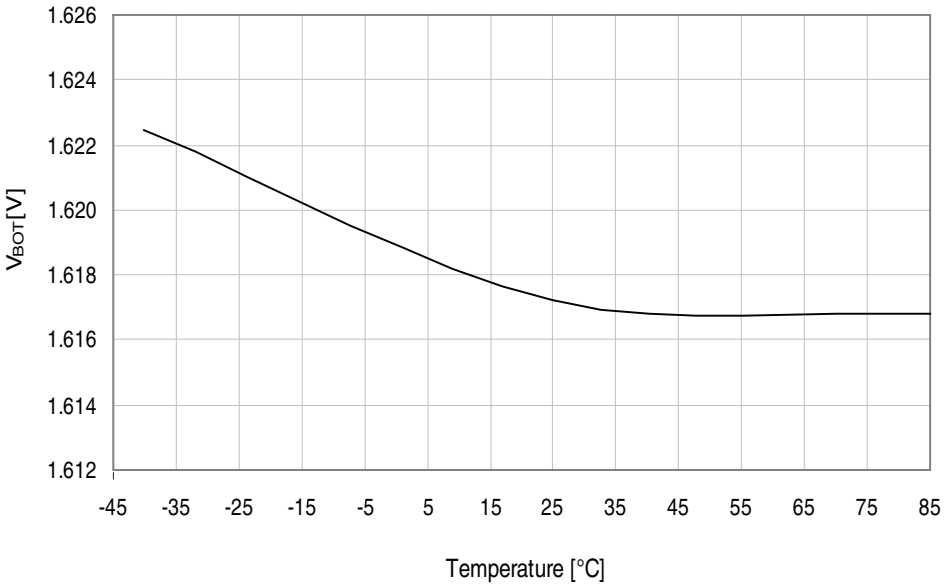
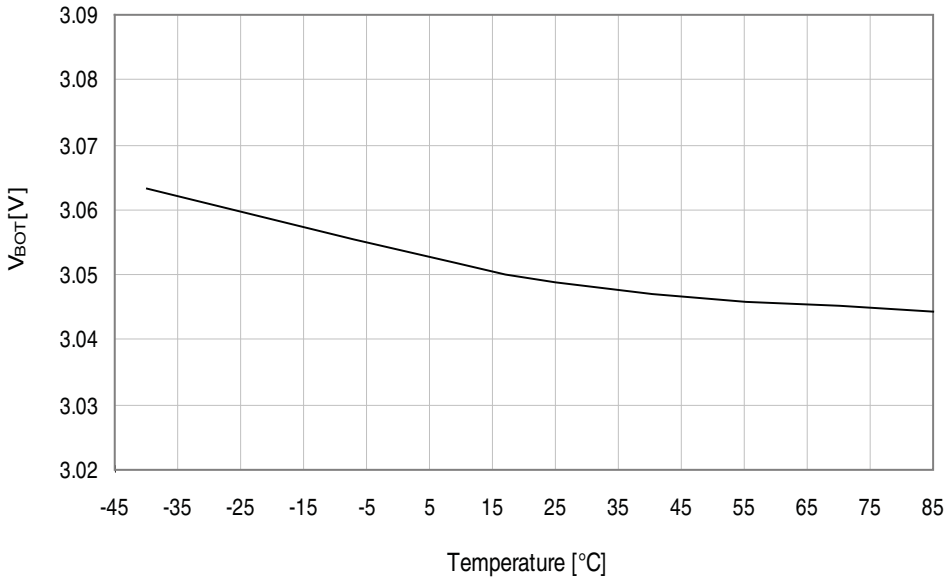


Figure 33-265. BOD thresholds vs. temperature.
BOD level = 3.0V.



33.5.7 External reset characteristics

Figure 33-266. Minimum reset pin pulse width vs. V_{CC}.

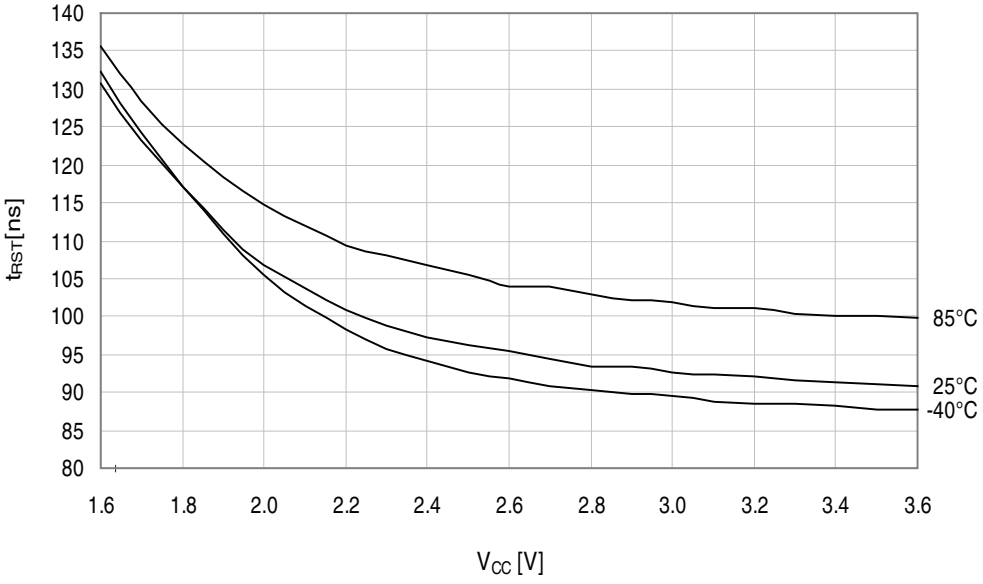


Figure 33-267. Reset pin pull-up resistor current vs. reset pin voltage.
V_{CC} = 1.8V.

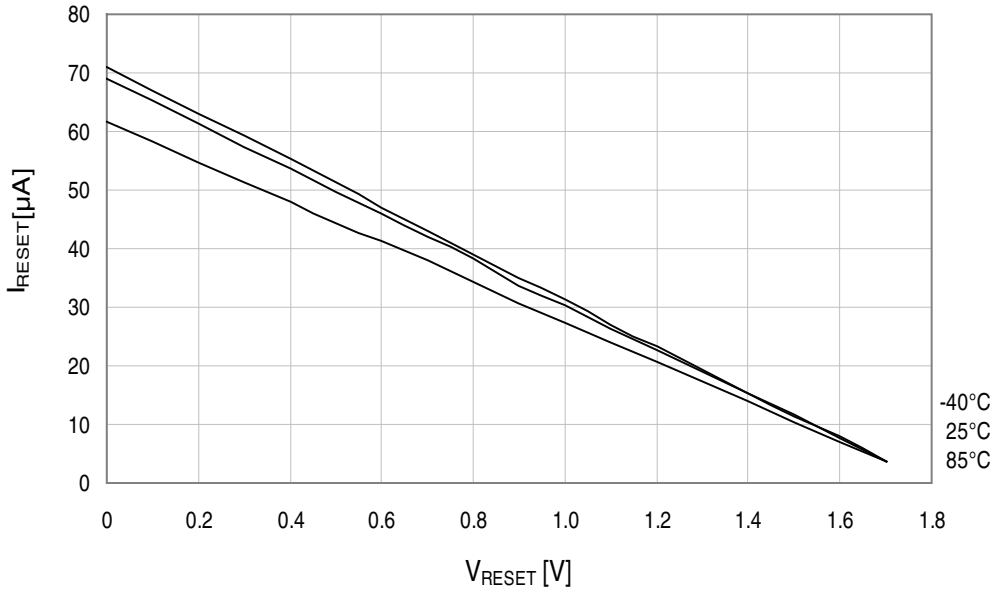


Figure 33-268. Reset pin pull-up resistor current vs. reset pin voltage.
V_{CC} = 3.0V.

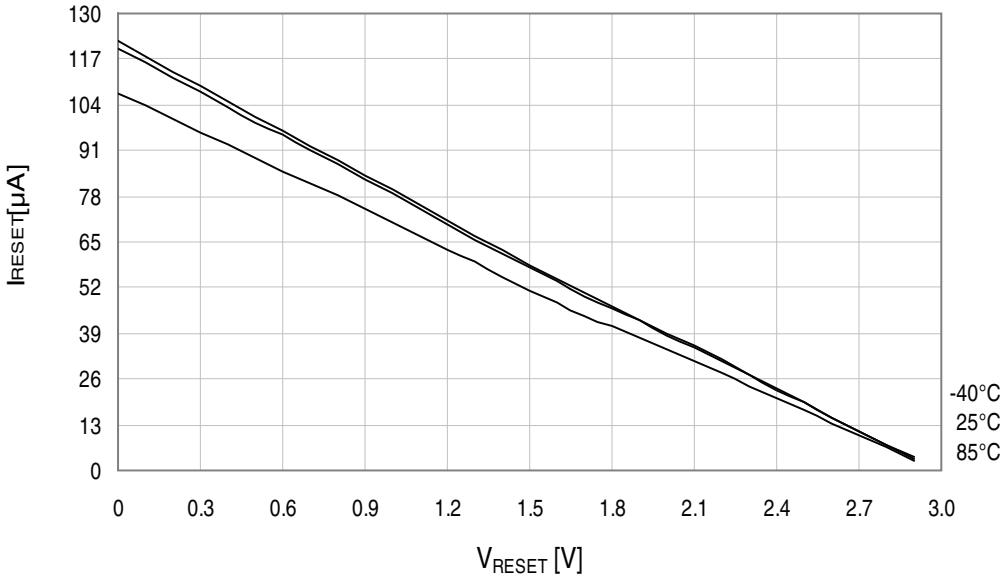


Figure 33-269. Reset pin pull-up resistor current vs. reset pin voltage.
V_{CC} = 3.3V.

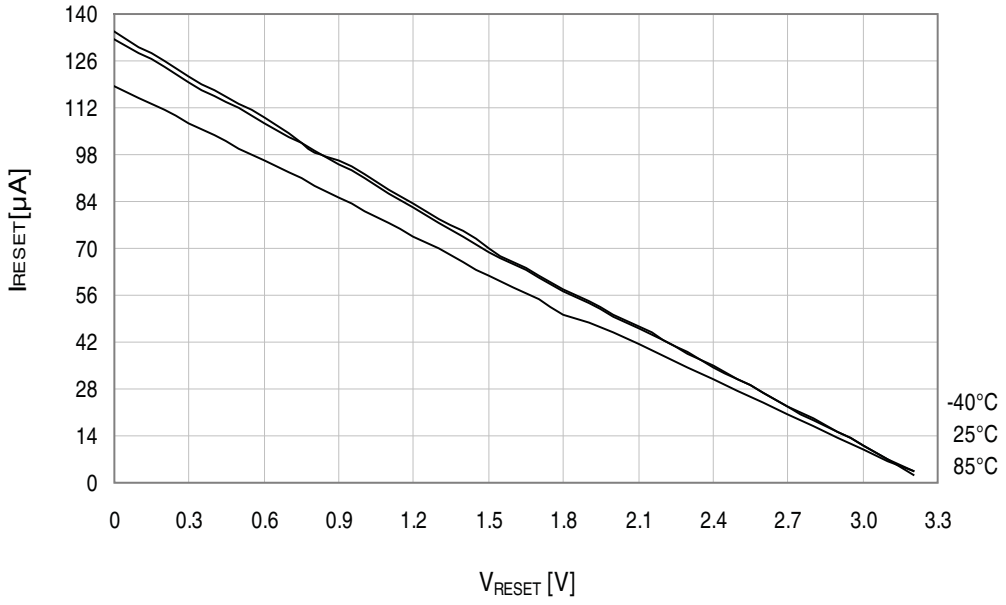
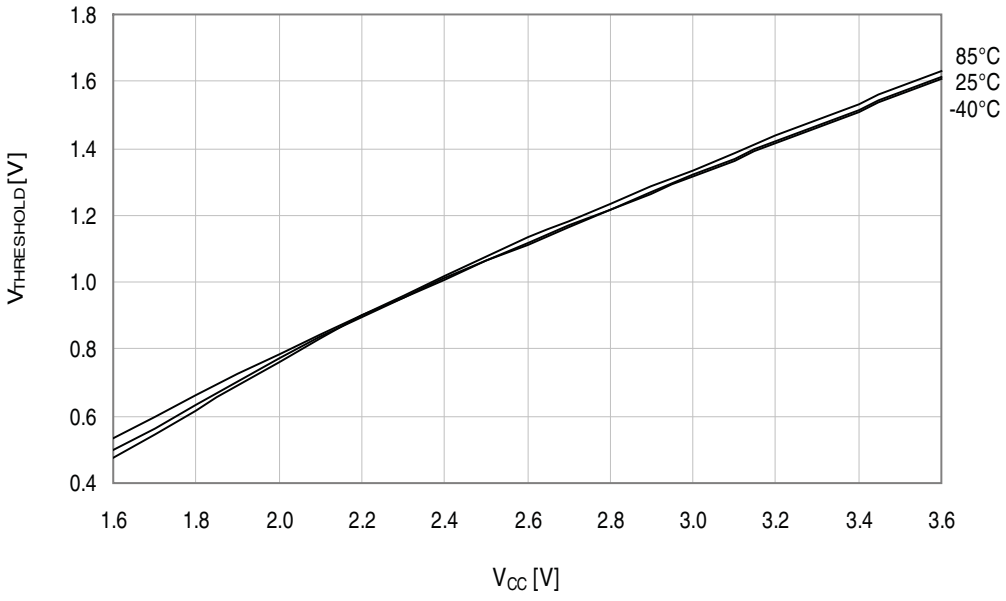


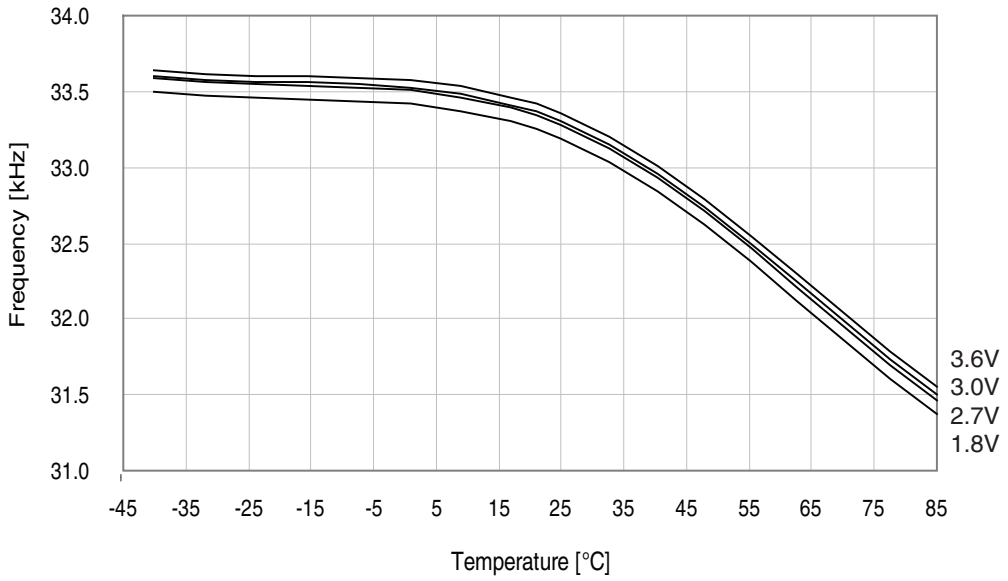
Figure 33-270. Reset pin input threshold voltage vs. V_{CC}.
V_{IH} - Reset pin read as "1".



33.5.8 Oscillator characteristics

33.5.8.1 Ultra Low-Power internal oscillator

Figure 33-271. Ultra Low-Power internal oscillator frequency vs. temperature.



33.5.8.2 32.768kHz internal oscillator

Figure 33-272. 32.768kHz internal oscillator frequency vs. temperature.

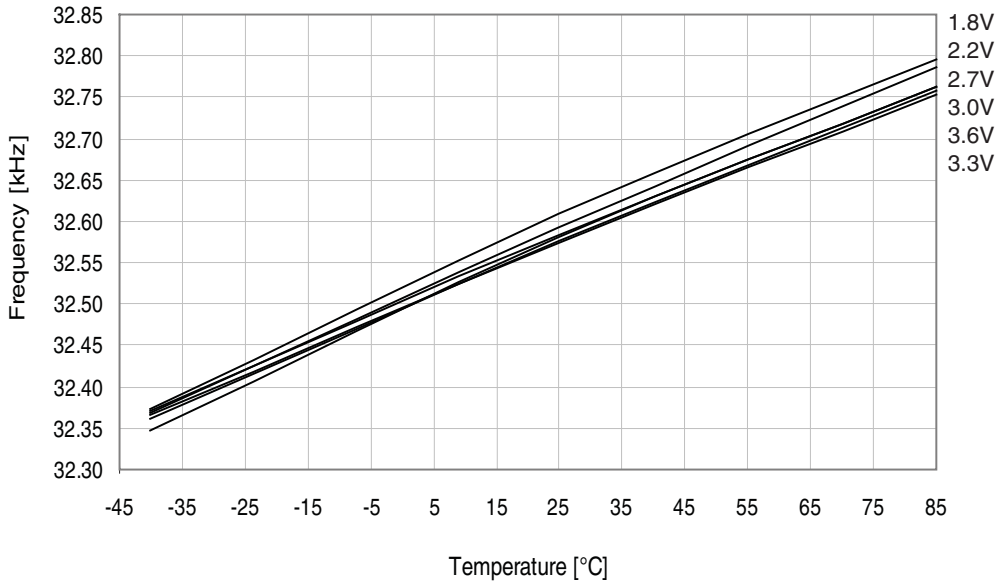
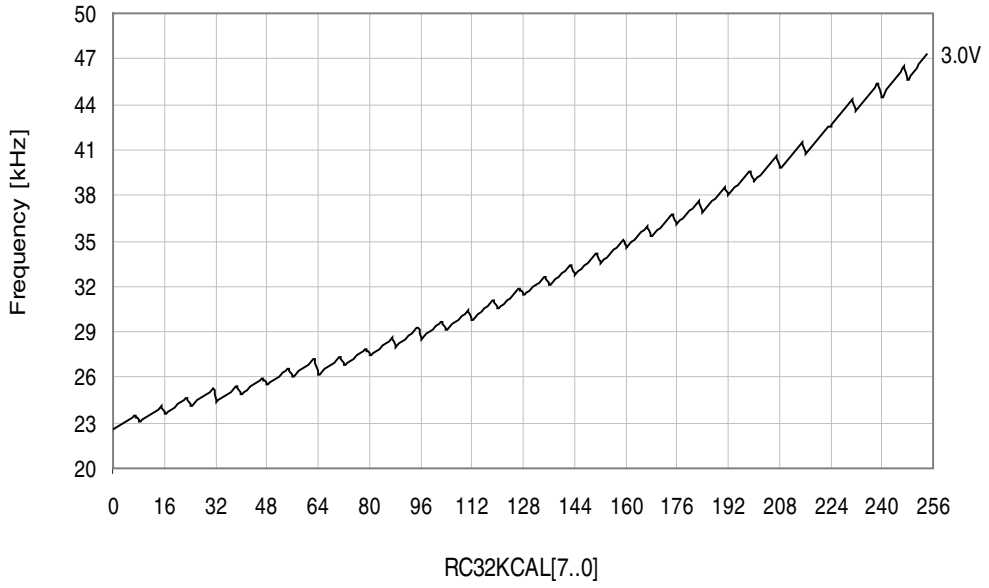


Figure 33-273. 32.768kHz internal oscillator frequency vs. calibration value.
V_{CC} = 3.0V, T = 25°C.



33.5.8.3 2MHz internal oscillator

Figure 33-274. 2MHz internal oscillator frequency vs. temperature.
DFLL disabled.

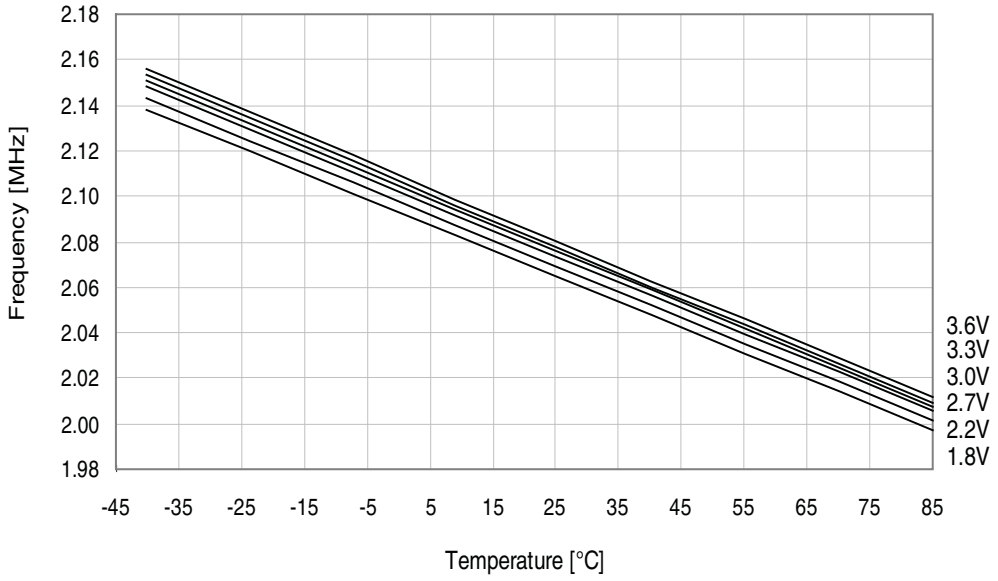


Figure 33-275. 2MHz internal oscillator frequency vs. temperature.
DFLL enabled, from the 32.768kHz internal oscillator .

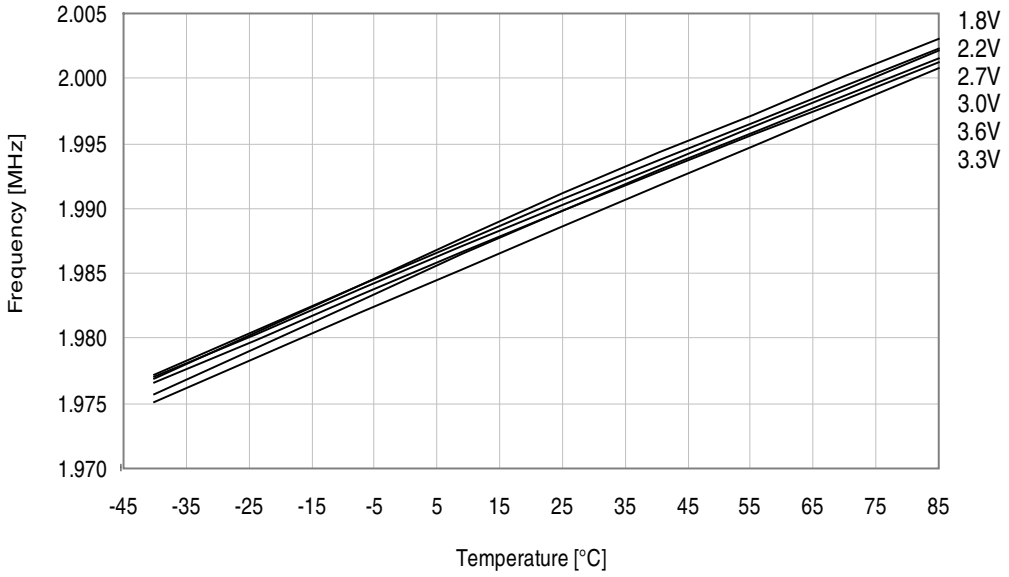
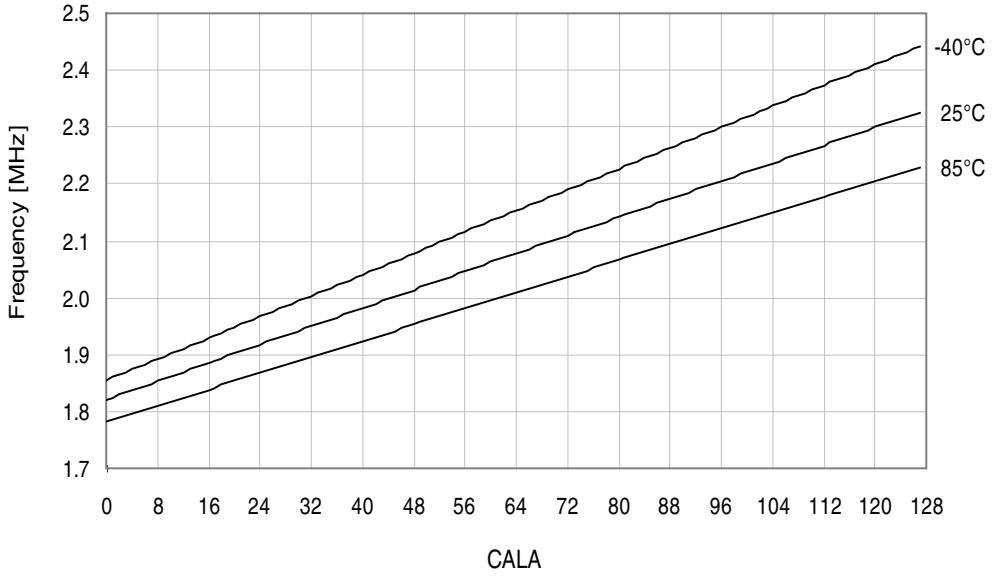


Figure 33-276. 2MHz internal oscillator frequency vs. CALA calibration value.
V_{CC} = 3V.



33.5.8.4 32MHz internal oscillator

Figure 33-277. 32MHz internal oscillator frequency vs. temperature.
DFLL disabled.

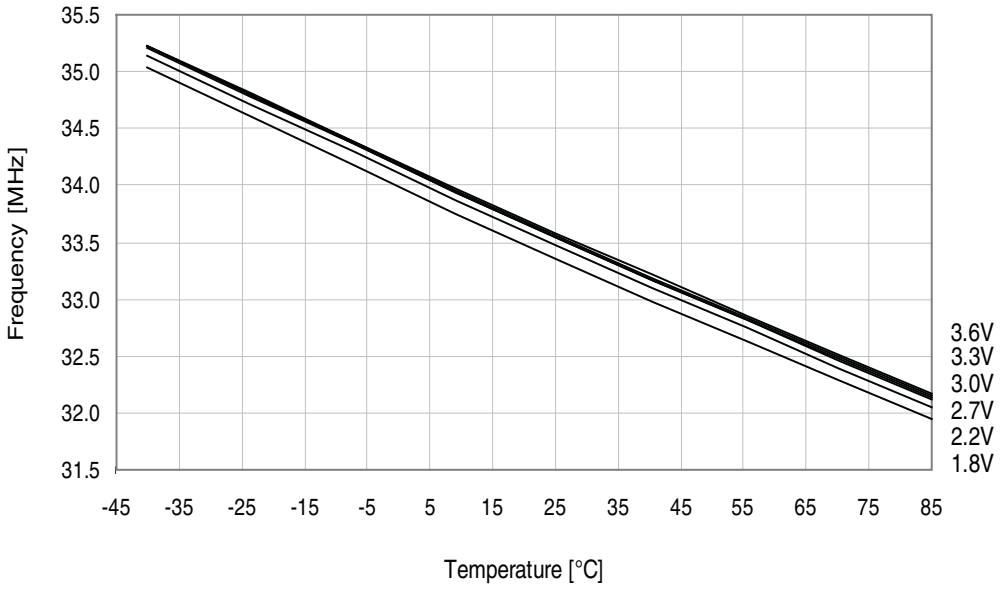


Figure 33-278. 32MHz internal oscillator frequency vs. temperature.
DFLL enabled, from the 32.768kHz internal oscillator.

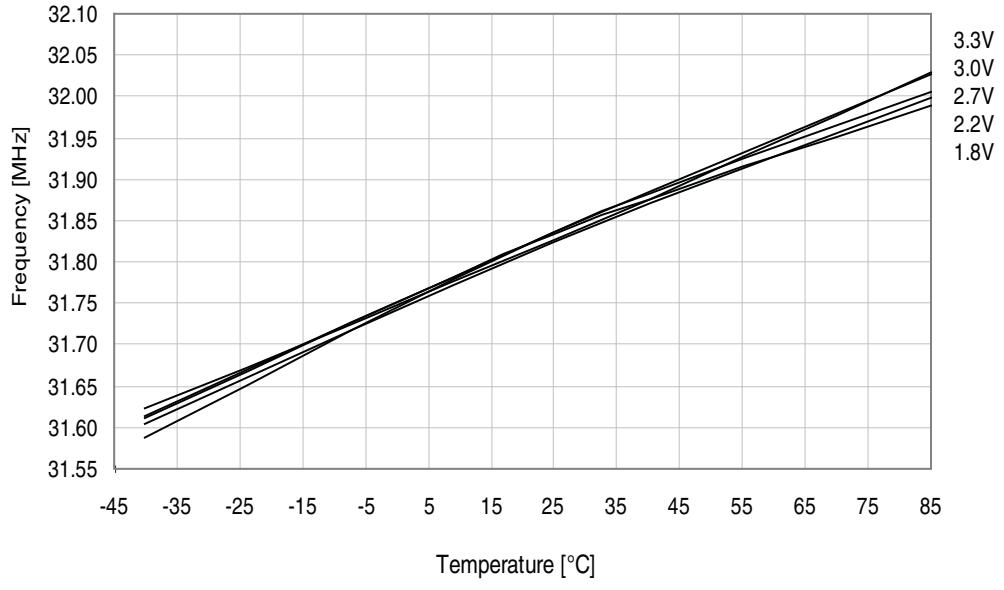


Figure 33-279. 32MHz internal oscillator CALA calibration step size.
V_{CC} = 3.0V.

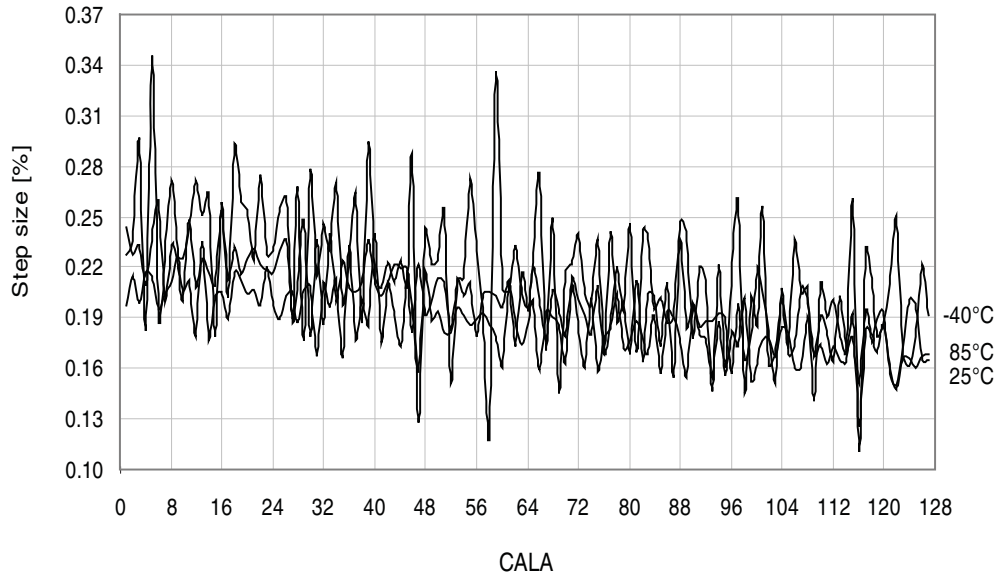
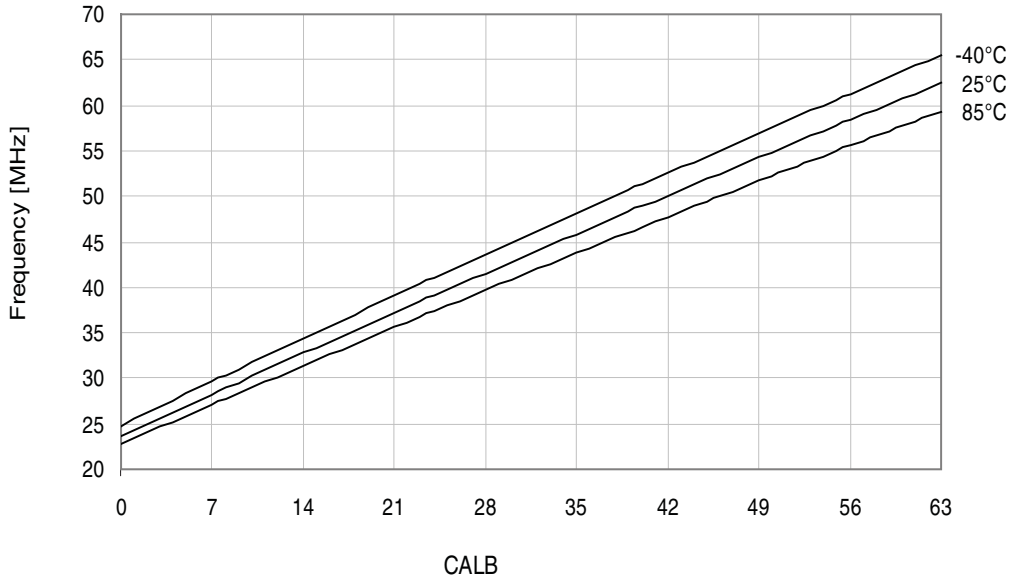


Figure 33-280. 32MHz internal oscillator frequency vs. CALB calibration value.
V_{CC} = 3.0V.



33.5.8.5 32MHz internal oscillator calibrated to 48MHz

Figure 33-281. 48MHz internal oscillator frequency vs. temperature.
DFLL disabled.

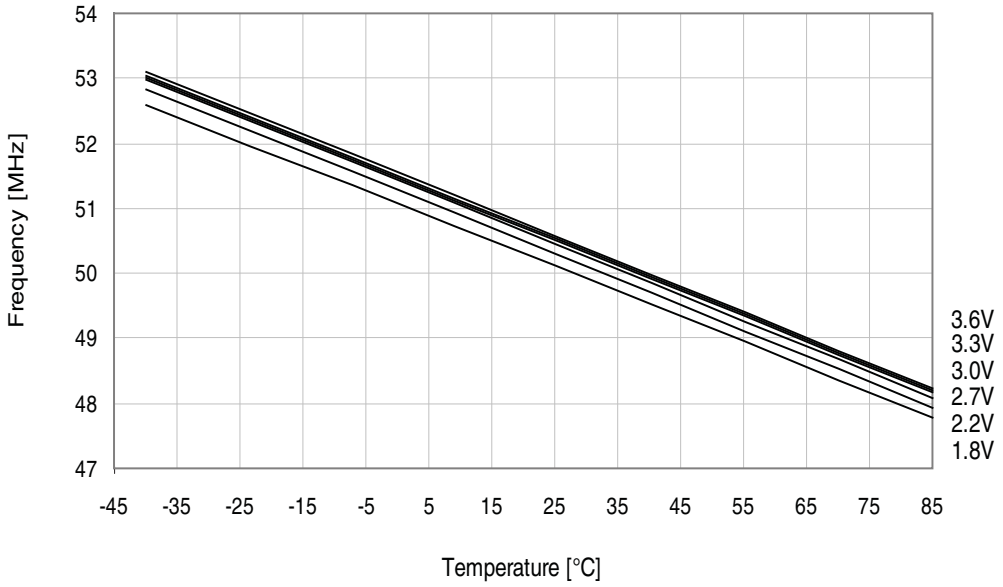
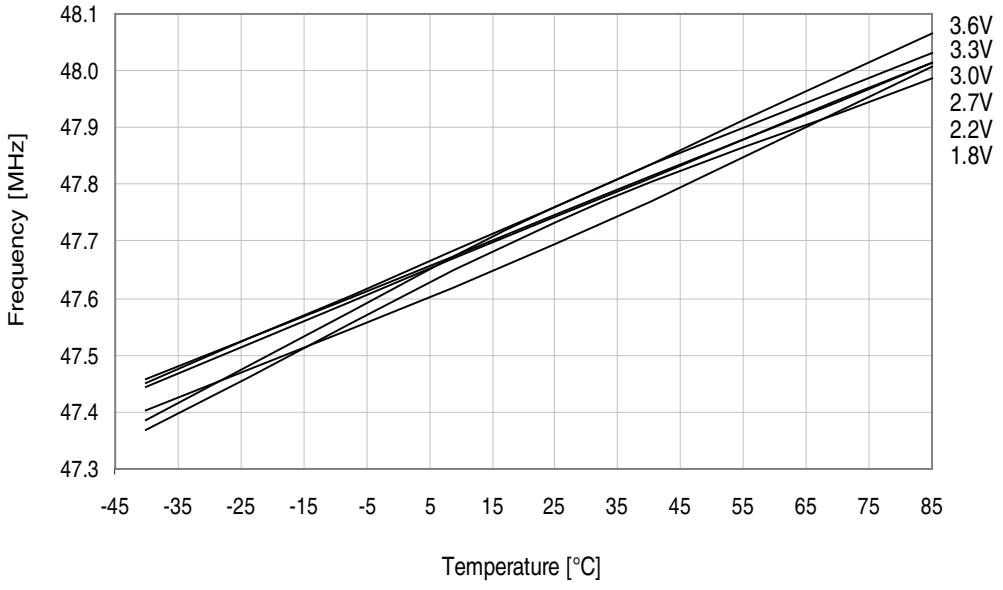


Figure 33-282. 48MHz internal oscillator frequency vs. temperature.
DFLL enabled, from the 32.768kHz internal oscillator.



33.5.9 Two-wire interface characteristics

Figure 33-283. SDA hold time vs. temperature.

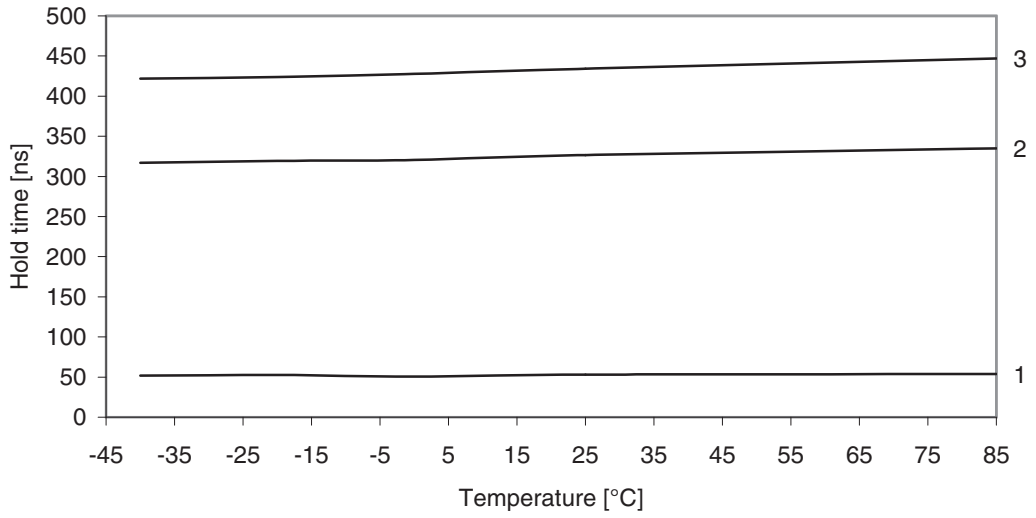
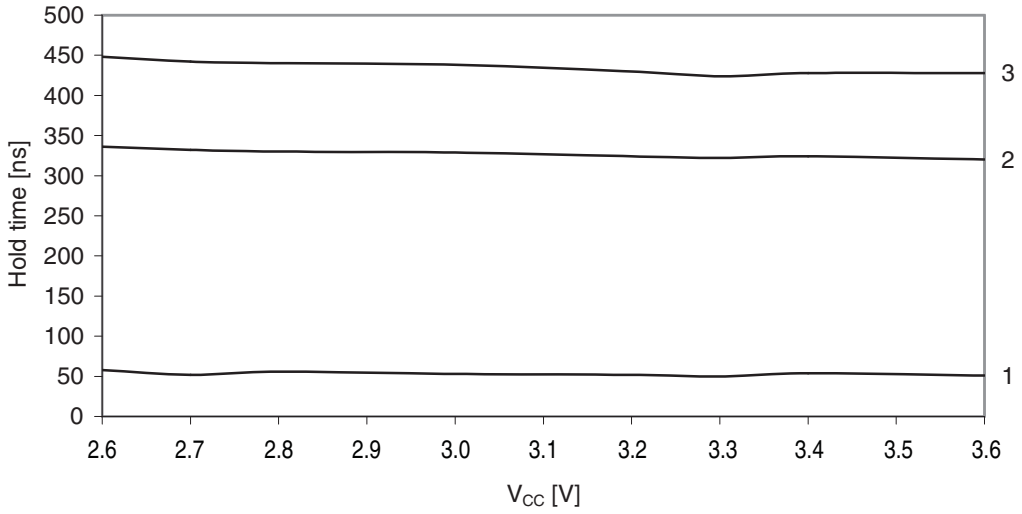
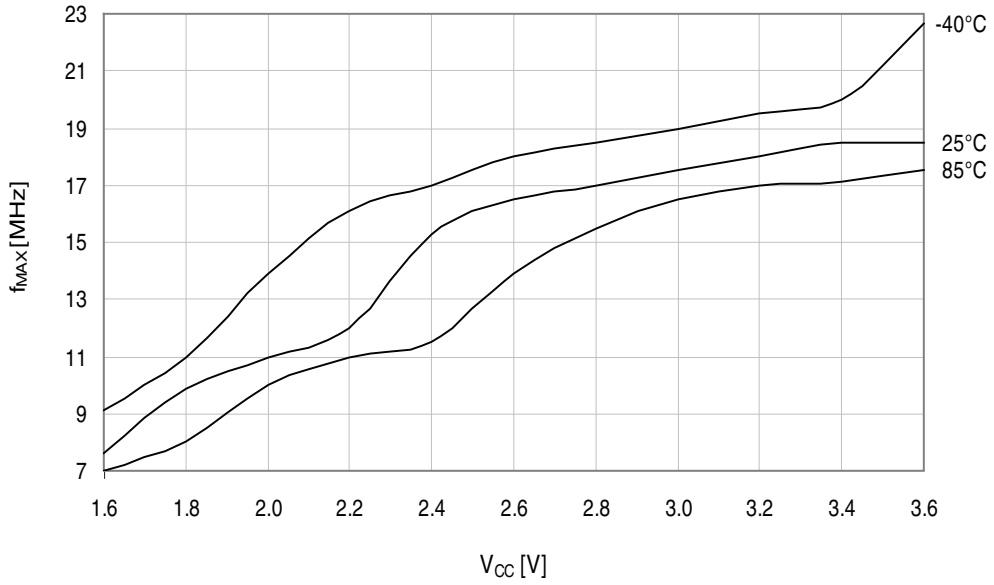


Figure 33-284. SDA hold time vs. supply voltage.



33.5.10 PDI characteristics

Figure 33-285. Maximum PDI frequency vs. V_{CC}.



33.6 Atmel ATxmega384D3

33.6.1 Current consumption

33.6.1.1 Active mode supply current

Figure 33-286. Active supply current vs. frequency.
f_{SYS} = 0 - 1MHz external clock, T = 25°C.

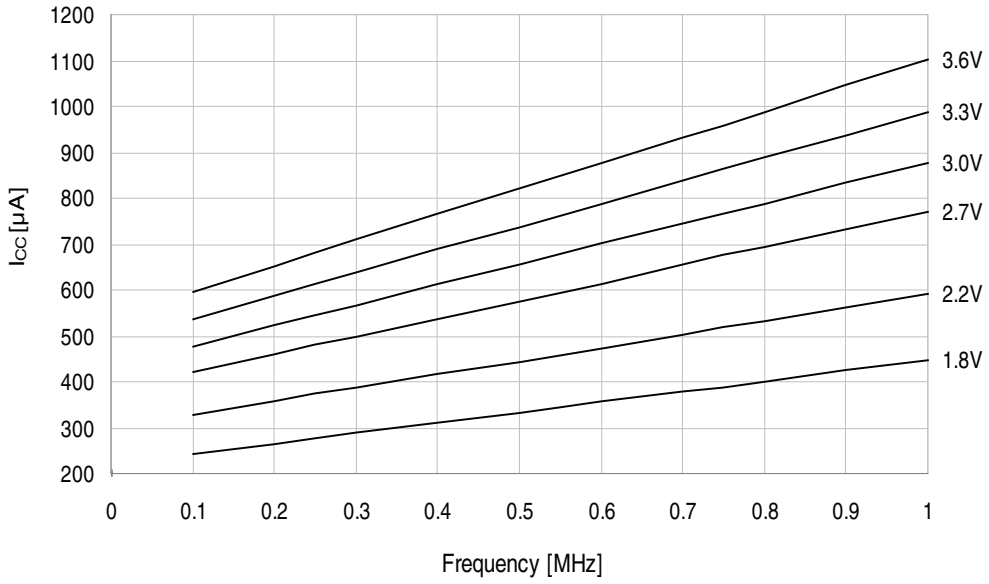


Figure 33-287. Active supply current vs. frequency.
f_{SYS} = 1 - 32MHz external clock, T = 25°C.

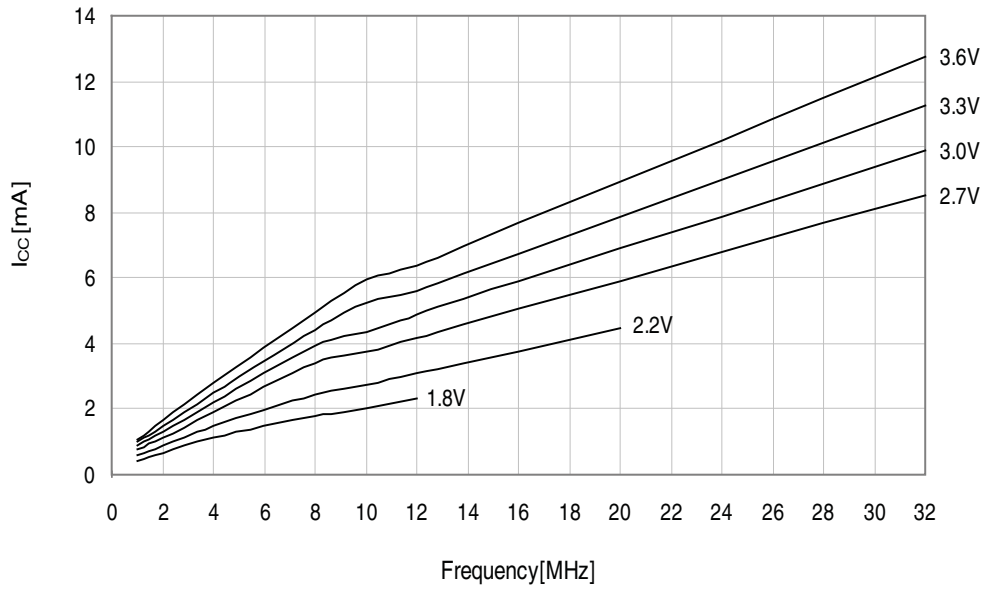


Figure 33-288. Active mode supply current vs. V_{CC}.
f_{SYS} = 32.768kHz internal oscillator.

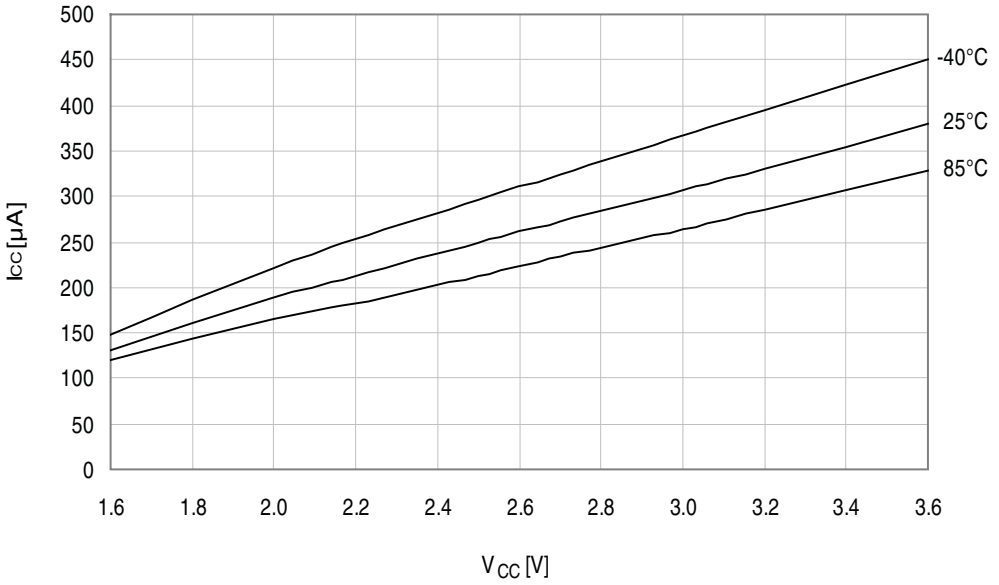


Figure 33-289. Active mode supply current vs. V_{CC}.
f_{SYS} = 1MHz external clock.

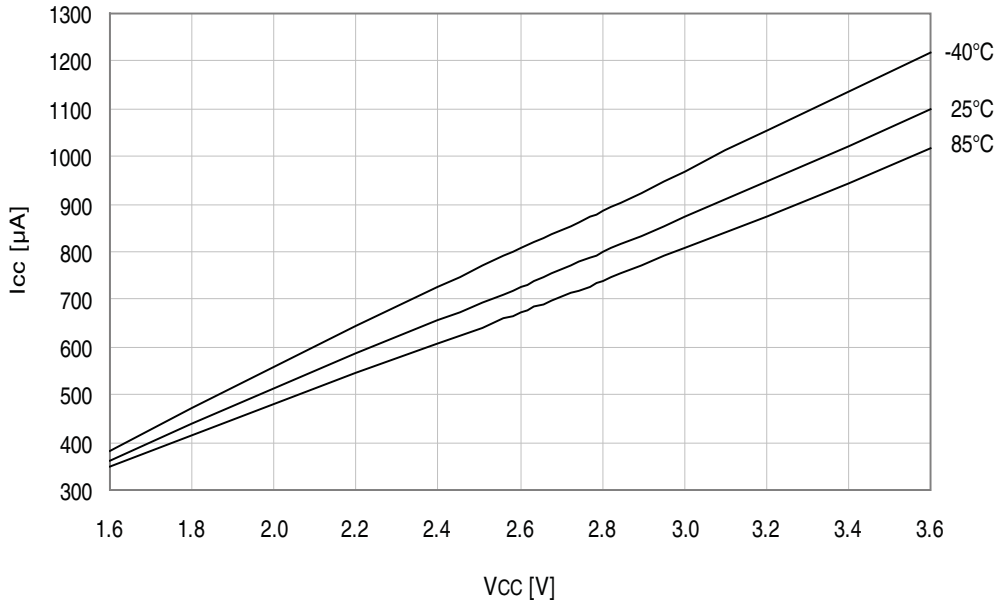


Figure 33-290. Active mode supply current vs. V_{CC}.
f_{SYS} = 2MHz internal oscillator.

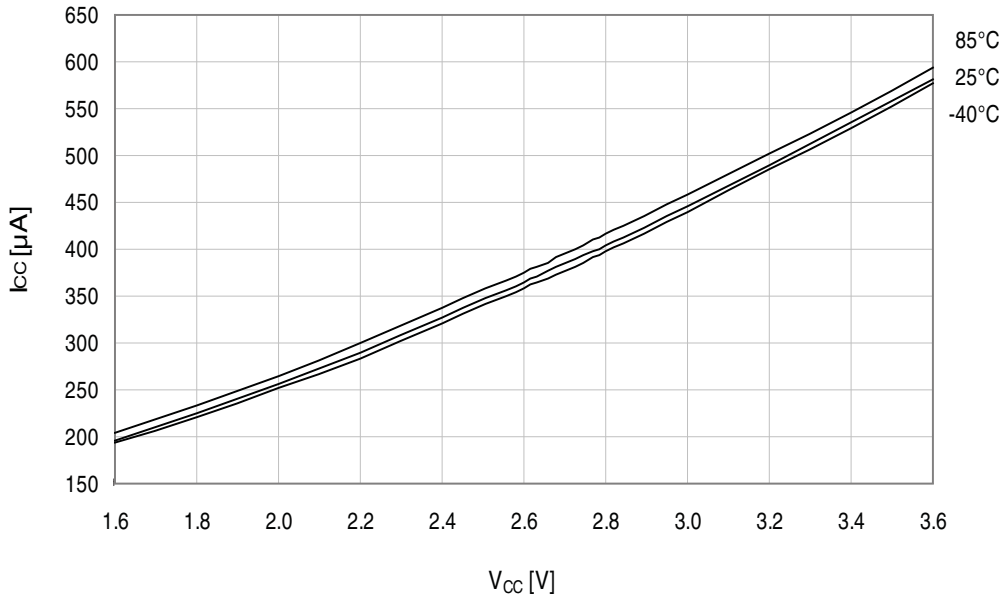


Figure 33-291. Active mode supply current vs. V_{CC}.
f_{SYS} = 32MHz internal oscillator prescaled to 8MHz.

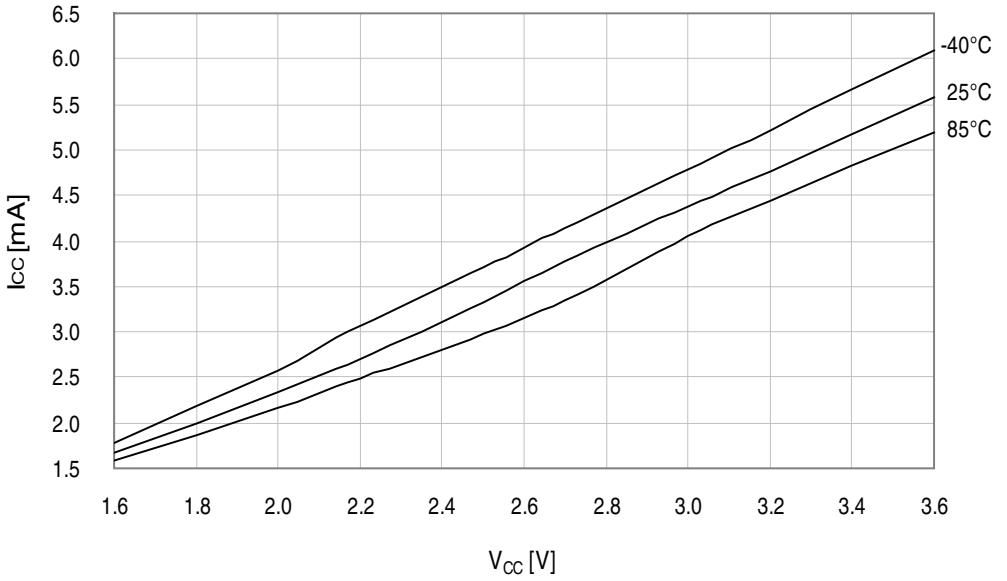
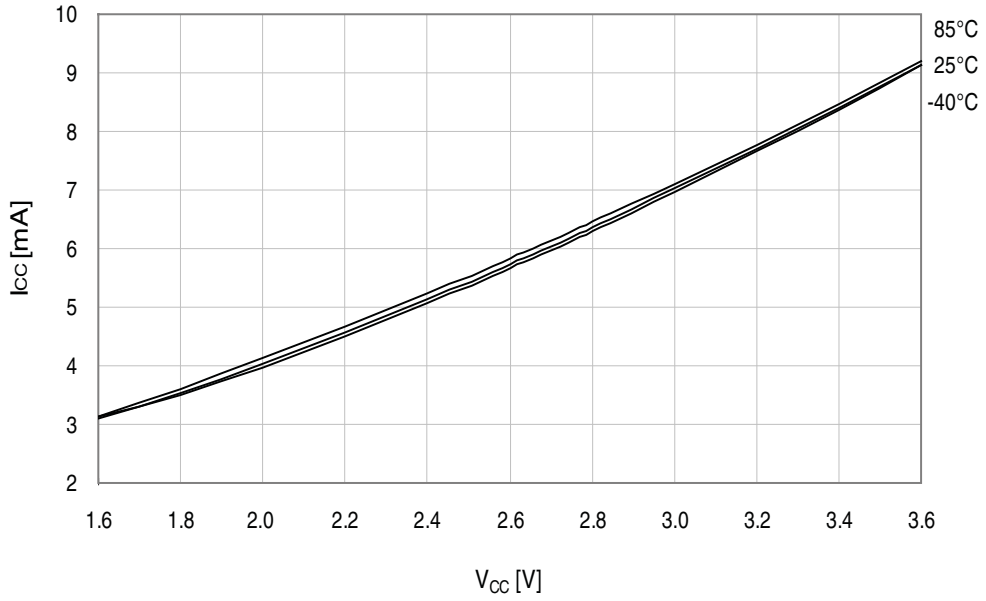


Figure 33-292. Active mode supply current vs. V_{CC}.
f_{SYS} = 32MHz internal oscillator.



33.6.1.2 Idle mode supply current

Figure 33-293. Idle mode supply current vs. frequency.
f_{SYS} = 0 - 1MHz external clock, T = 25°C.

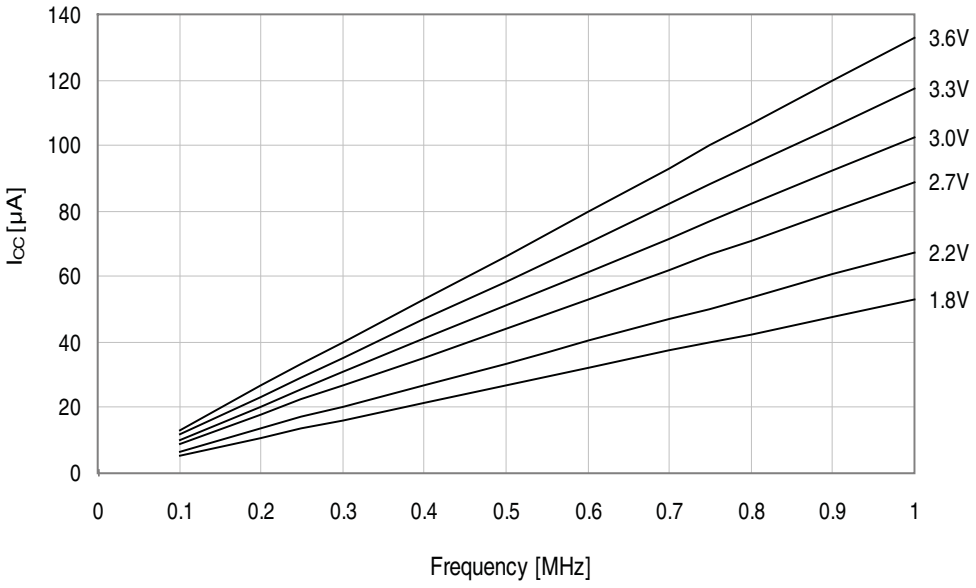


Figure 33-294. Idle mode supply current vs. frequency.
f_{SYS} = 1 - 32MHz external clock, T = 25°C.

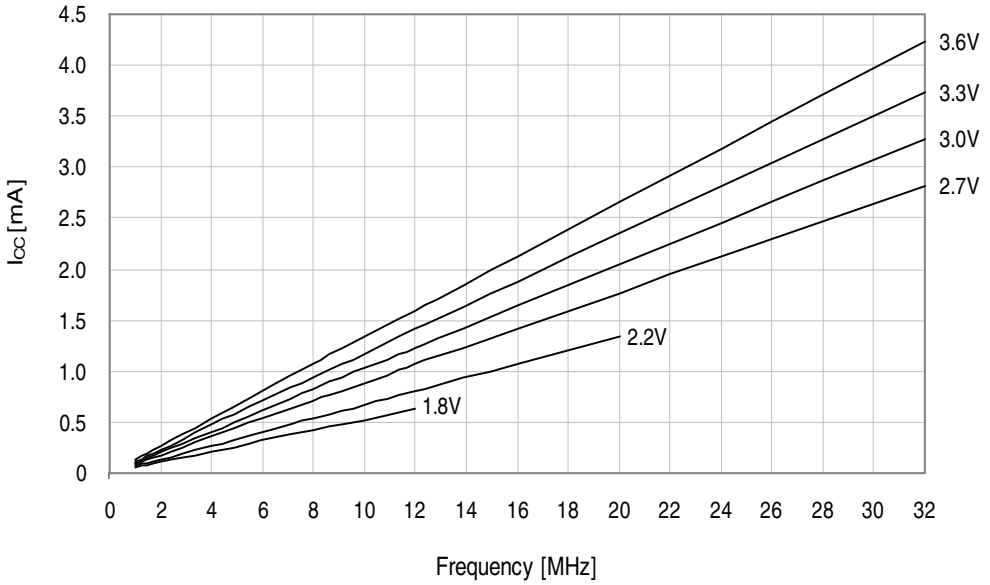


Figure 33-295. Idle mode supply current vs. V_{CC}.
f_{SYS} = 32.768kHz internal oscillator.

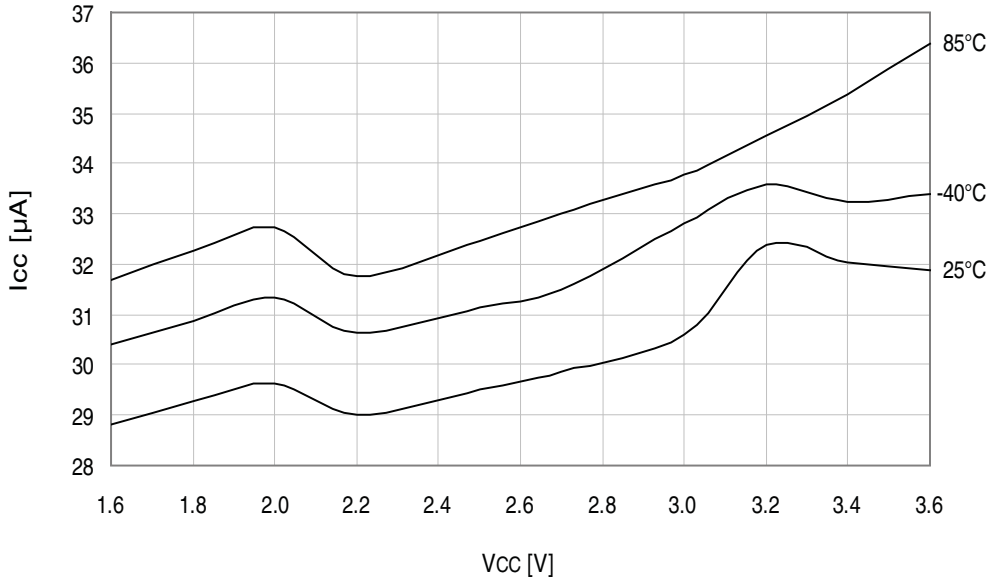


Figure 33-296. Idle mode supply current vs. V_{CC}.
f_{SYS} = 1MHz external clock.

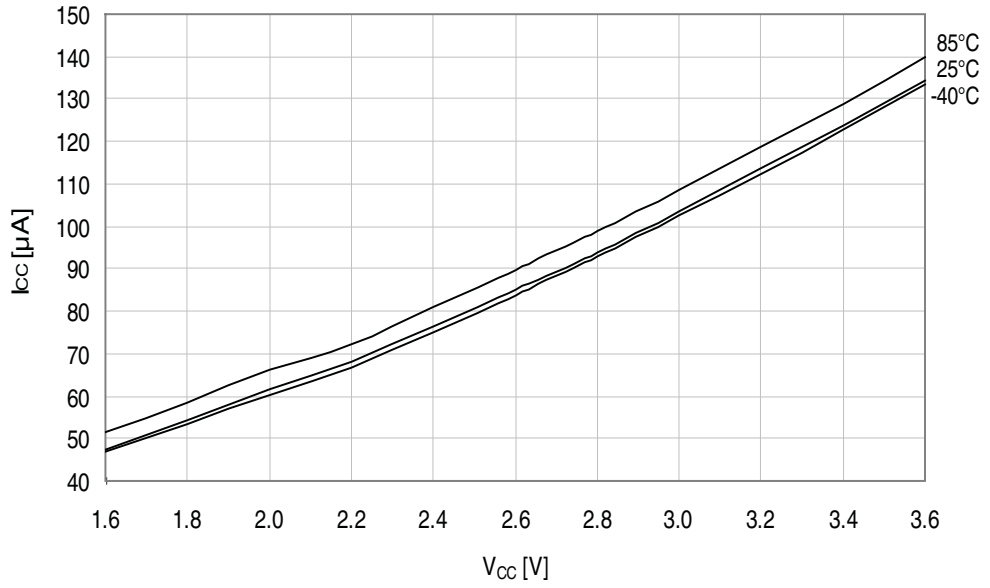


Figure 33-297. Idle mode supply current vs. V_{CC}.
f_{SYS} = 2MHz internal oscillator.

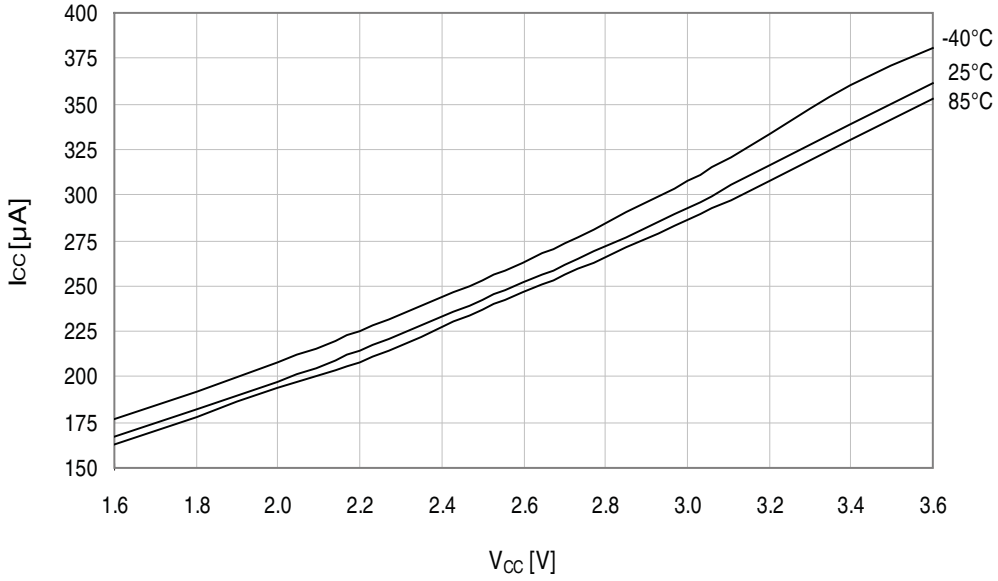


Figure 33-298. Idle mode supply current vs. V_{CC}.
f_{SYS} = 32MHz internal oscillator prescaled to 8MHz.

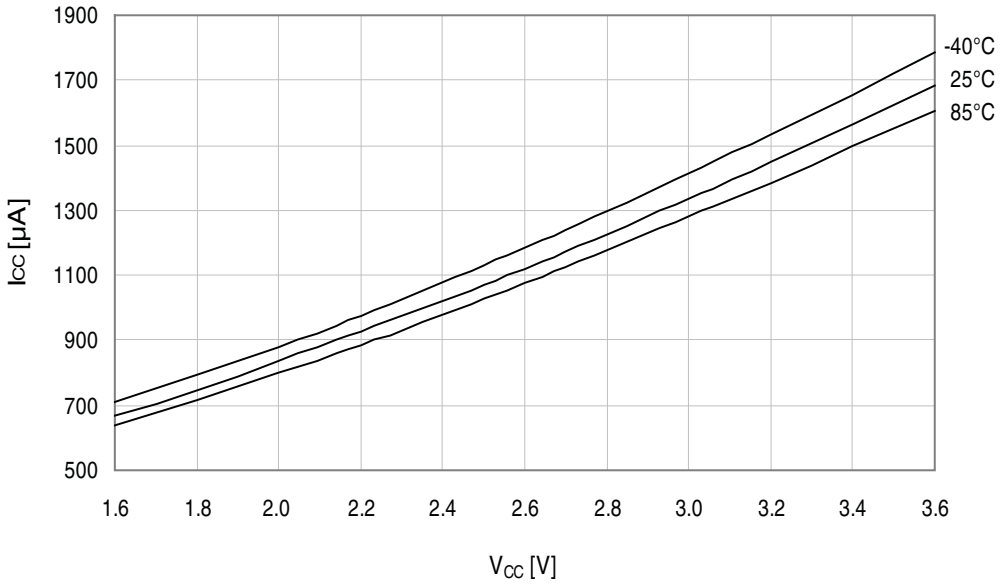
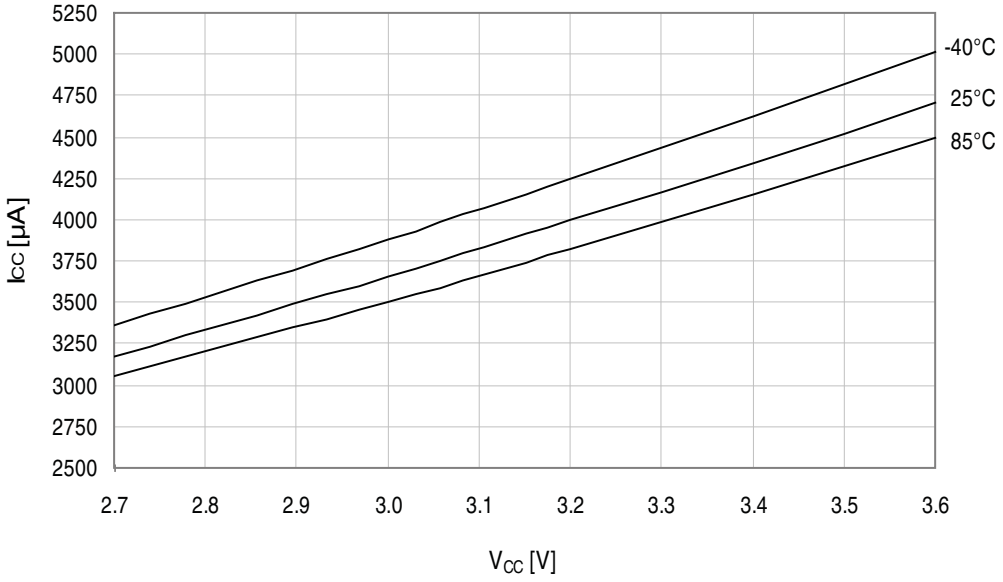


Figure 33-299. Idle mode current vs. V_{CC}.
f_{SYS} = 32MHz internal oscillator.



33.6.1.3 Power-down mode supply current

Figure 33-300. Power-down mode supply current vs. V_{CC}.
All functions disabled.

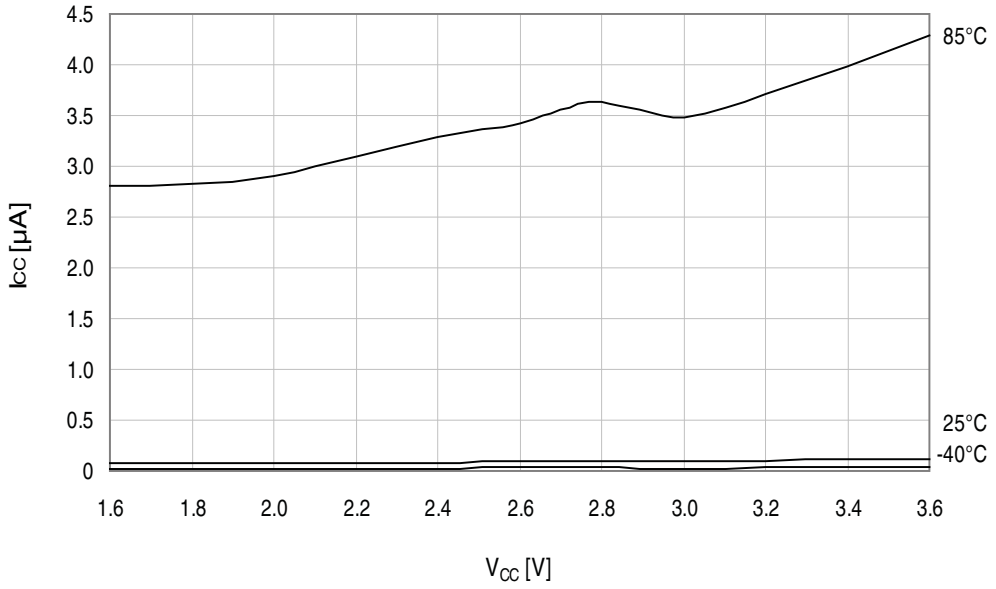


Figure 33-301. Power-down mode supply current vs. V_{CC}.
Watchdog and sampled BOD enabled.

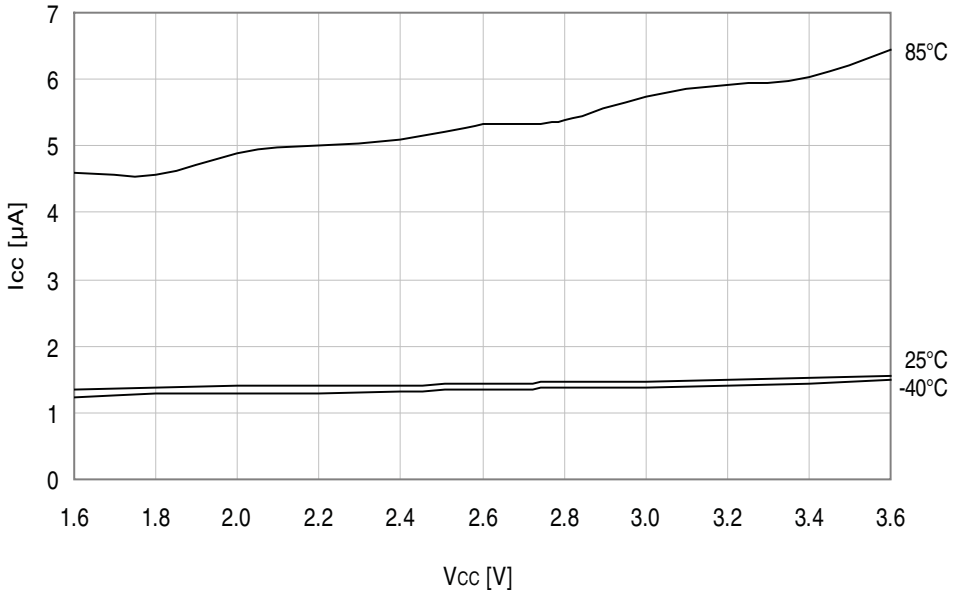
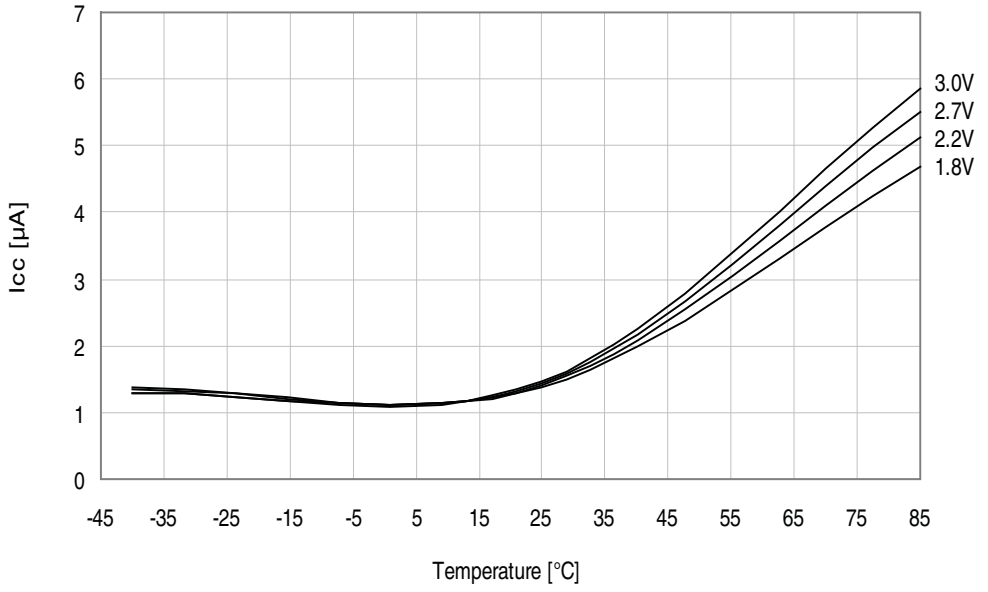


Figure 33-302. Power-down mode supply current vs. temperature.
Watchdog and sampled BOD enabled and running from internal ULP oscillator.



33.6.2 I/O pin characteristics

The I/O pins complies with the JEDEC LVTTL and LVCMOS specification and the high- and low level input and output voltage limits reflect or exceed this specification.

33.6.2.1 Pull-up

Figure 33-303. I/O pin pull-up resistor current vs. input voltage.
V_{CC} = 1.8V.

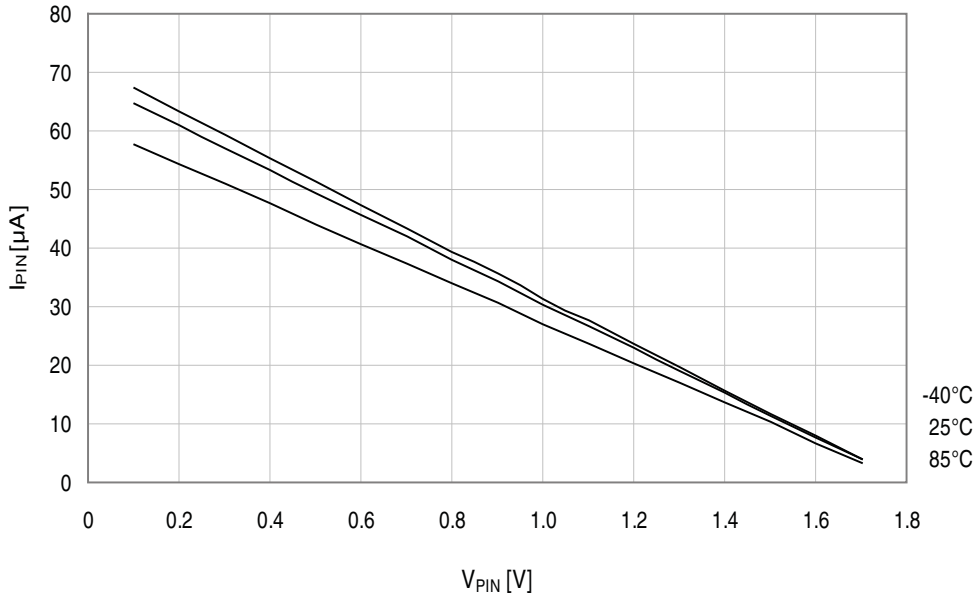


Figure 33-304. I/O pin pull-up resistor current vs. input voltage.
V_{CC} = 3.0V.

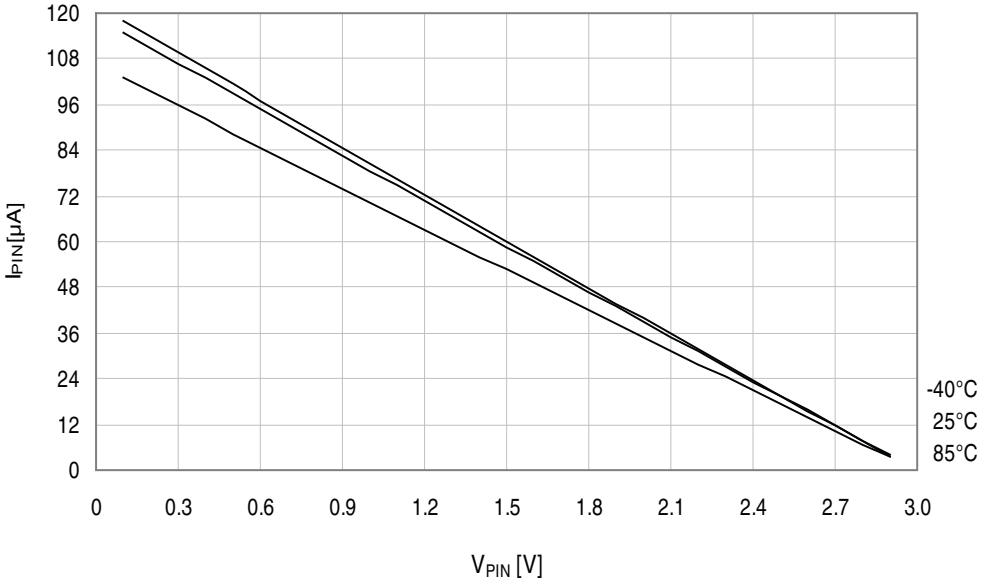
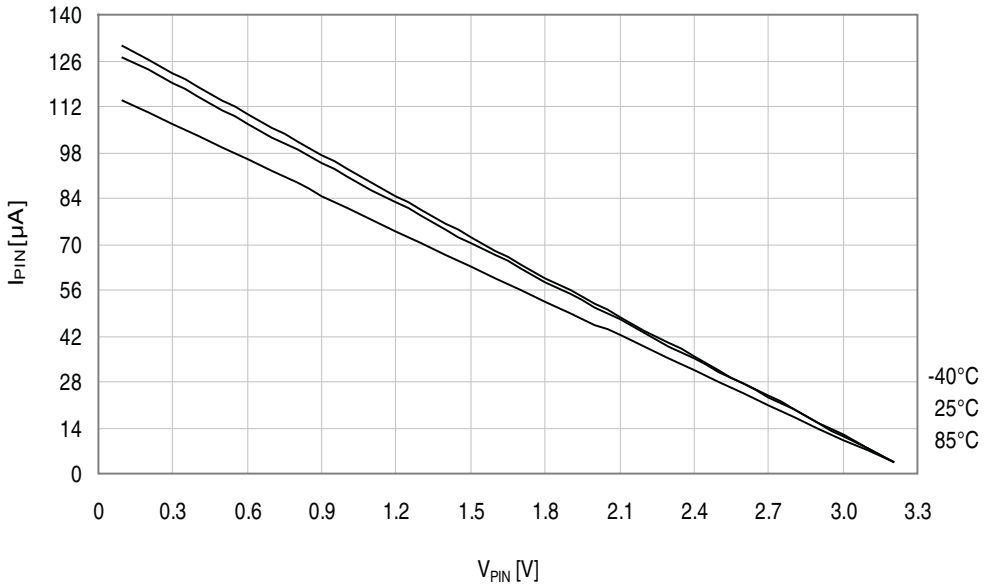


Figure 33-305. I/O pin pull-up resistor current vs. input voltage.
V_{CC} = 3.3V.



33.6.2.2 Output voltage vs. sink/source current

Figure 33-306. I/O pin output voltage vs. source current.
V_{CC} = 1.8V.

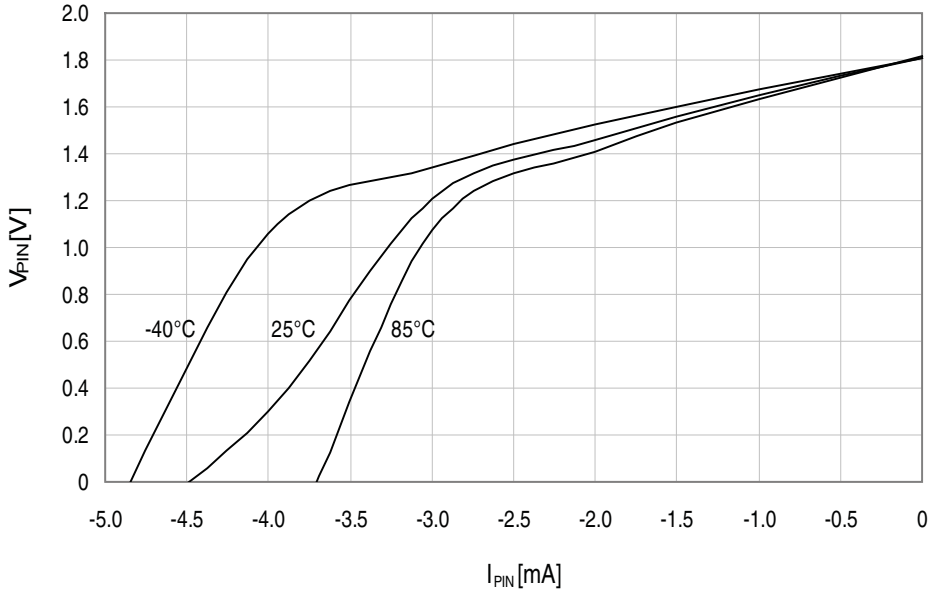


Figure 33-307. I/O pin output voltage vs. source current.
V_{CC} = 3.0V.

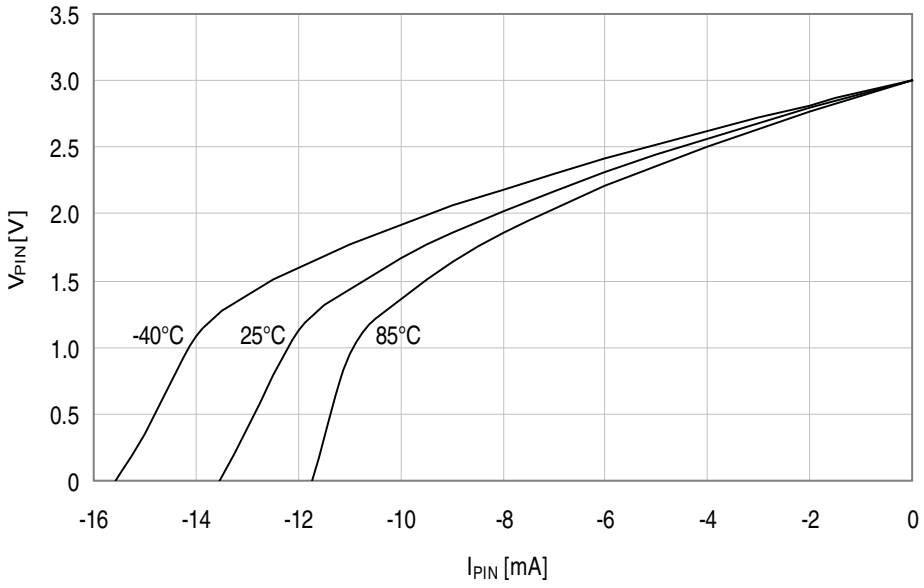


Figure 33-308. I/O pin output voltage vs. source current.
V_{CC} = 3.3V.

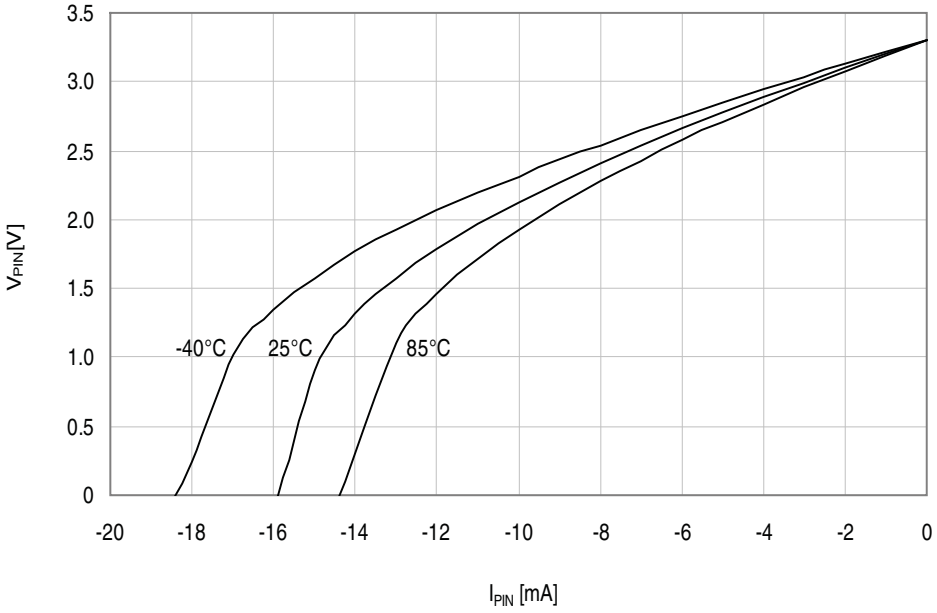


Figure 33-309. I/O pin output voltage vs. sink current.
V_{CC} = 1.8V.

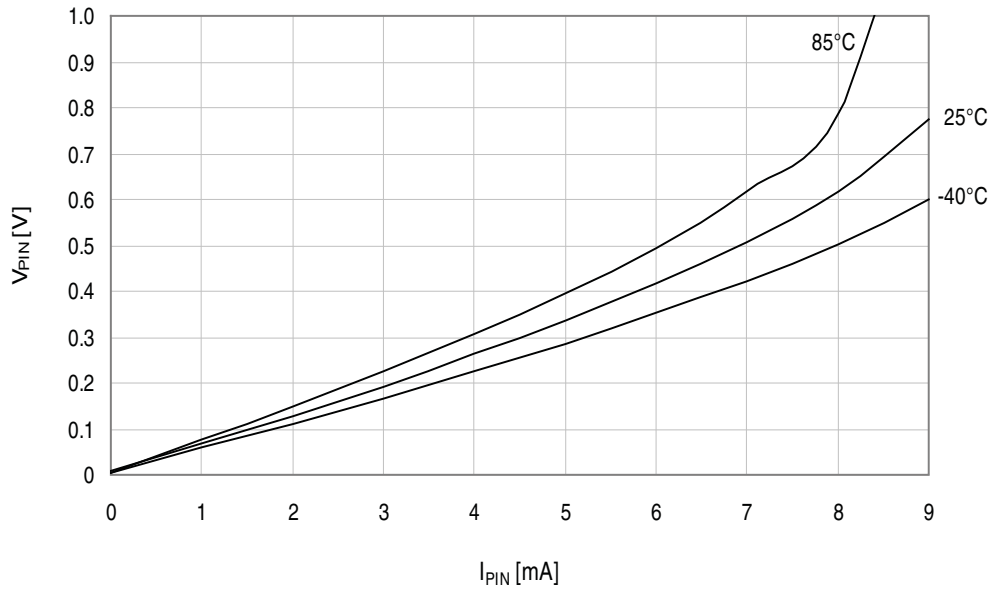


Figure 33-310. I/O pin output voltage vs. sink current.
V_{CC} = 3.0V.

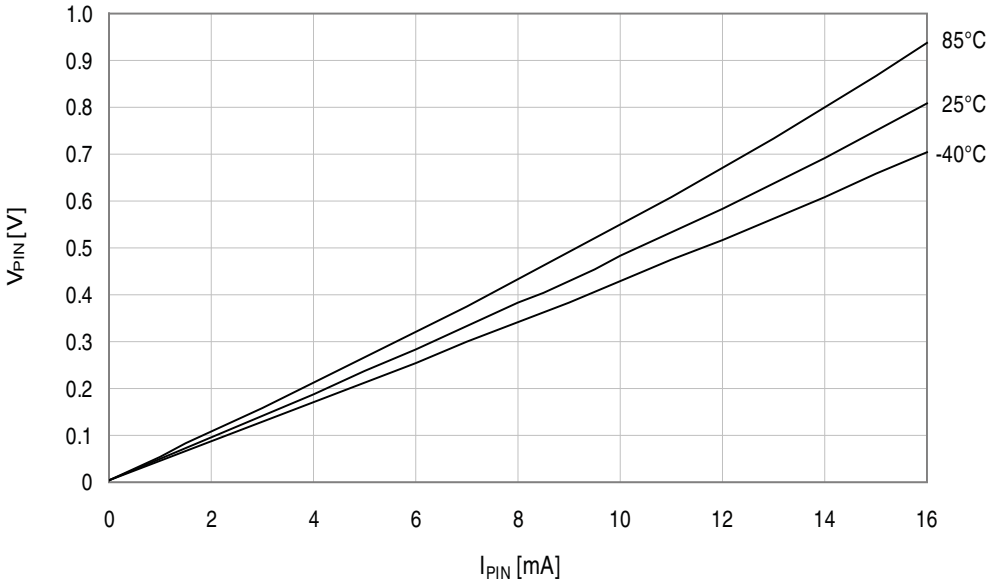
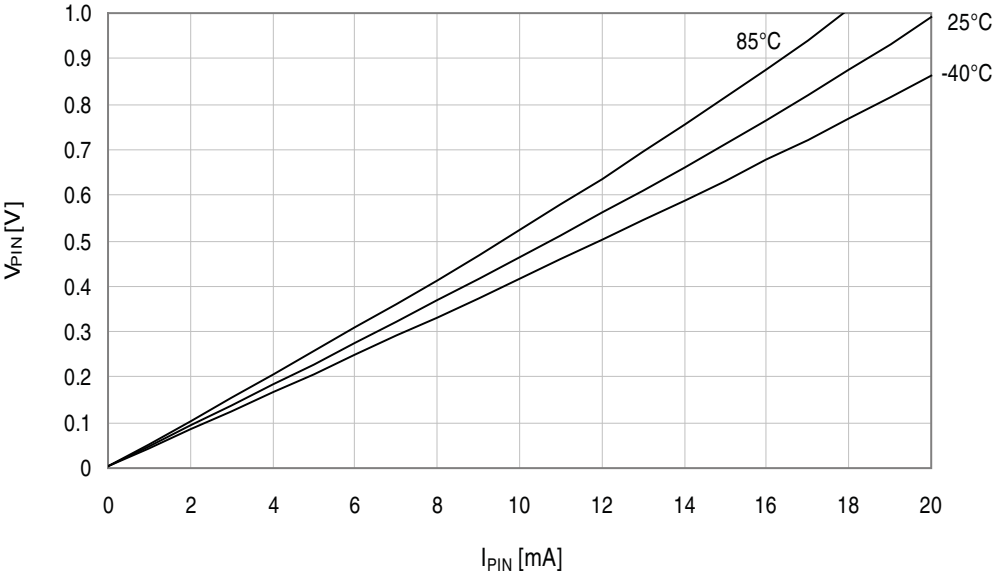


Figure 33-311. I/O pin output voltage vs. sink current.
V_{CC} = 3.3V.



33.6.2.3 Thresholds and hysteresis

Figure 33-312. I/O pin input threshold voltage vs. V_{CC}.
V_{IH} I/O pin read as "1".

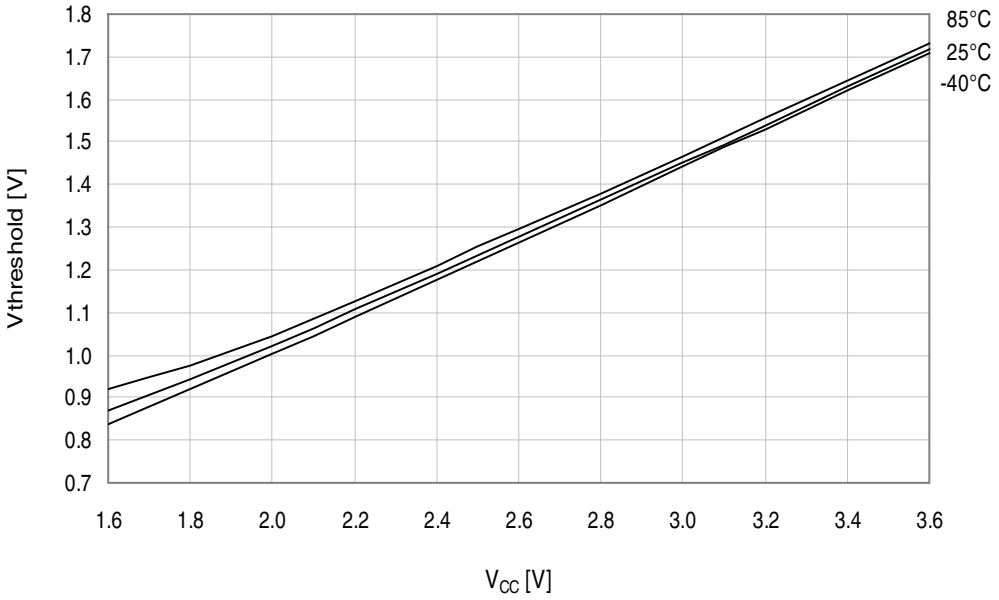


Figure 33-313. I/O pin input threshold voltage vs. V_{CC}.
V_{IL} I/O pin read as "0".

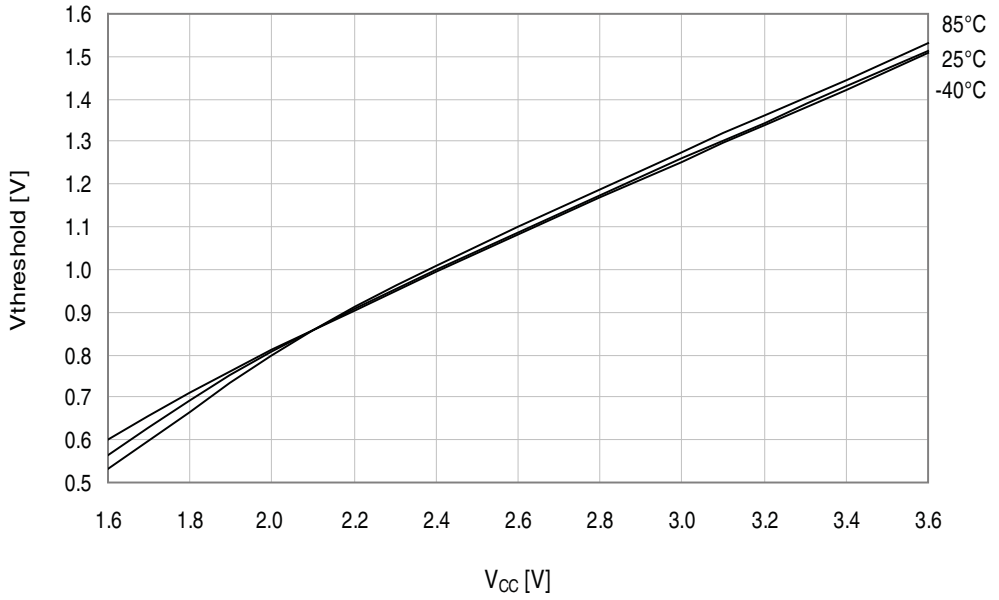
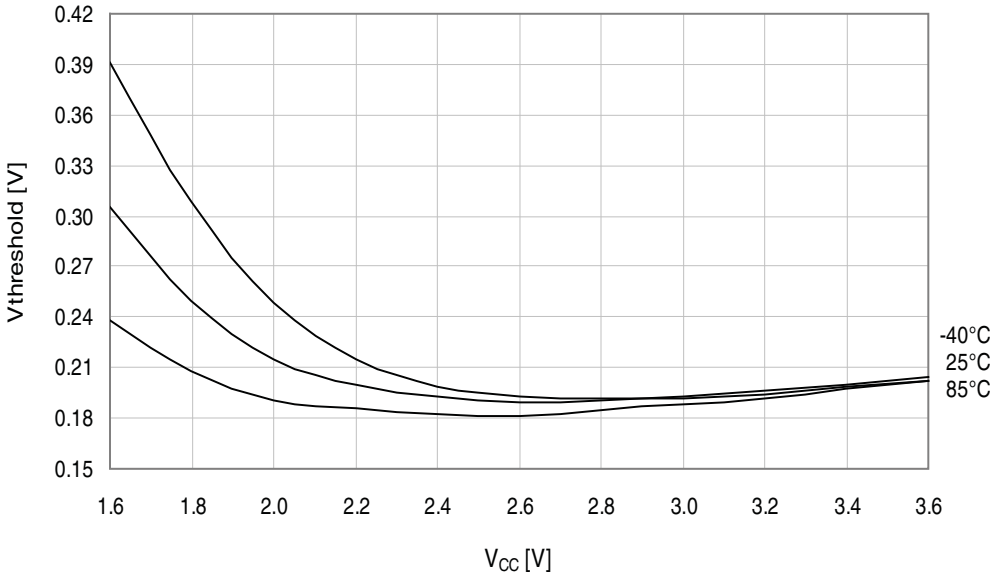


Figure 33-314. I/O pin input hysteresis vs. V_{CC}.



33.6.3 ADC characteristics

Figure 33-315. INL error vs. external V_{REF}.

T = 25°C, V_{CC} = 3.6V, external reference.

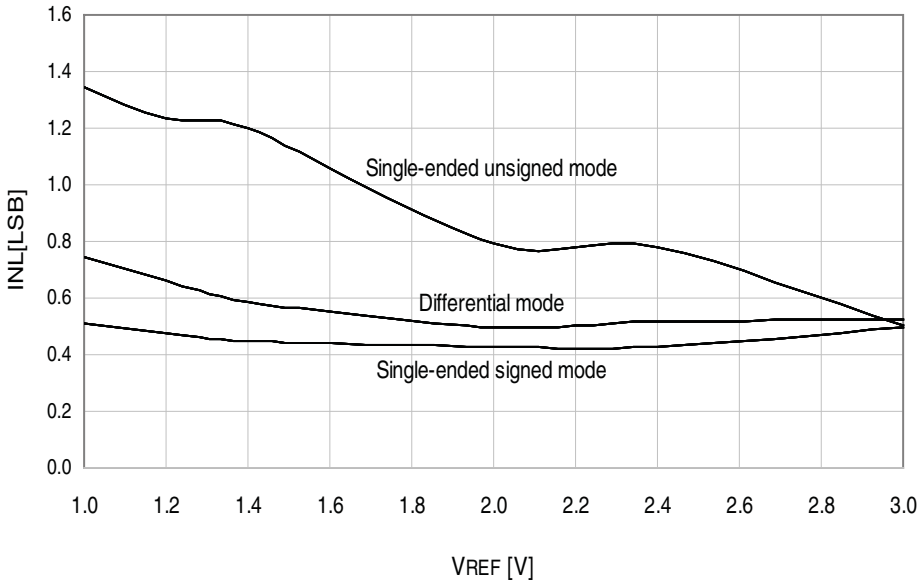


Figure 33-316. INL error vs. sample rate.

T = 25°C, V_{CC} = 3.6V, V_{REF} = 3.0V external.

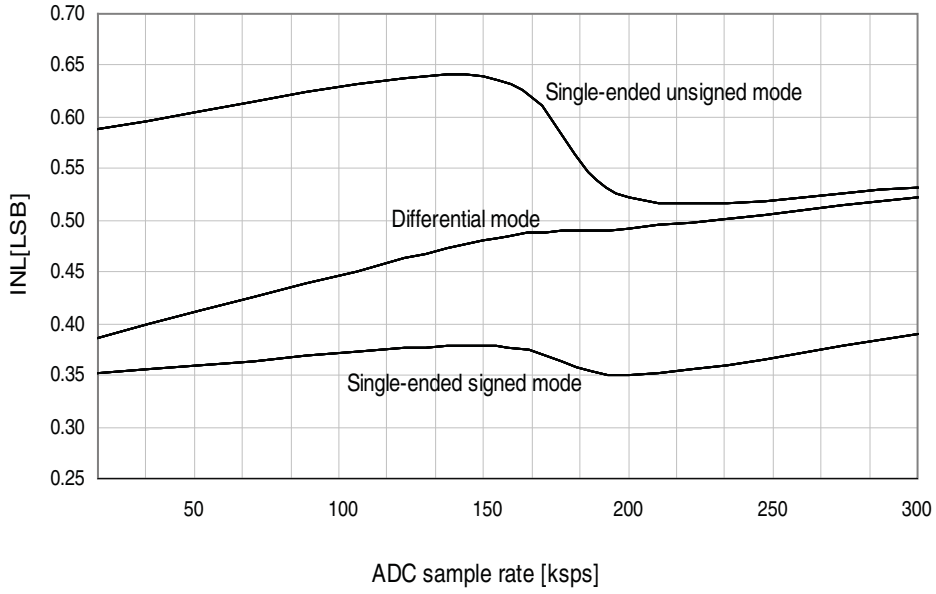


Figure 33-317. INL error vs. input code.

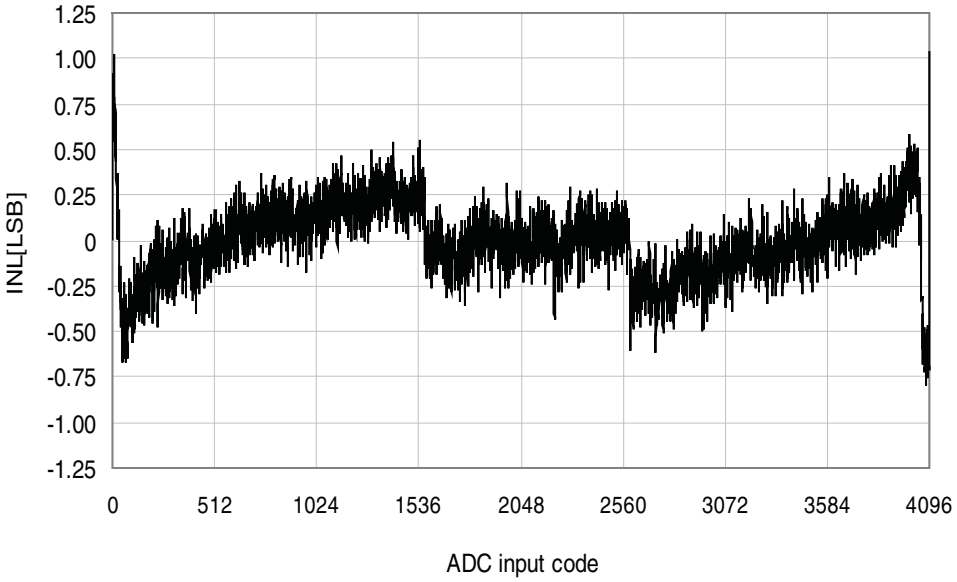


Figure 33-318. DNL error vs. external V_{REF}.

T = 25°C, V_{CC} = 3.6V, external reference.

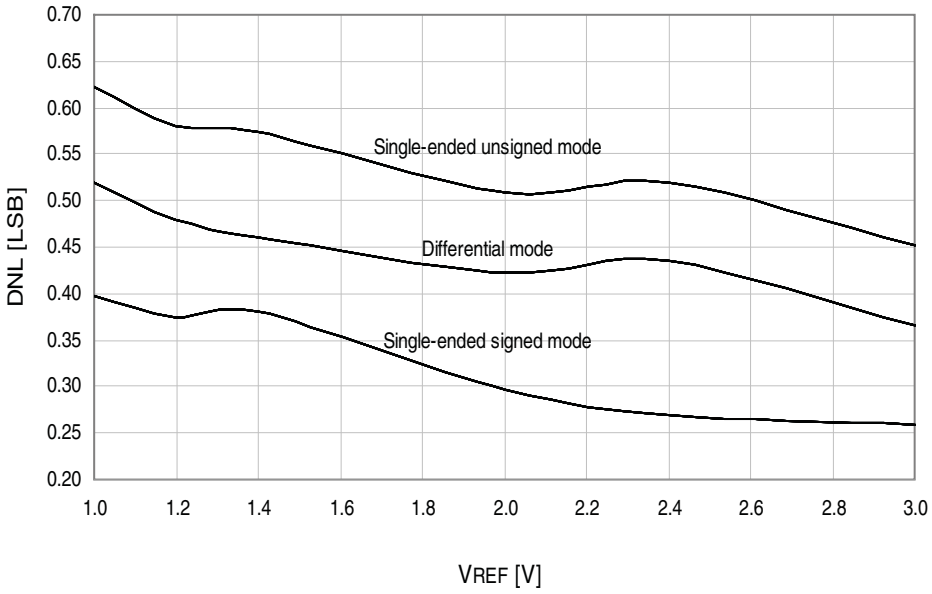


Figure 33-319. DNL error vs. sample rate.

T = 25°C, V_{CC} = 3.6V, V_{REF} = 3.0V external.

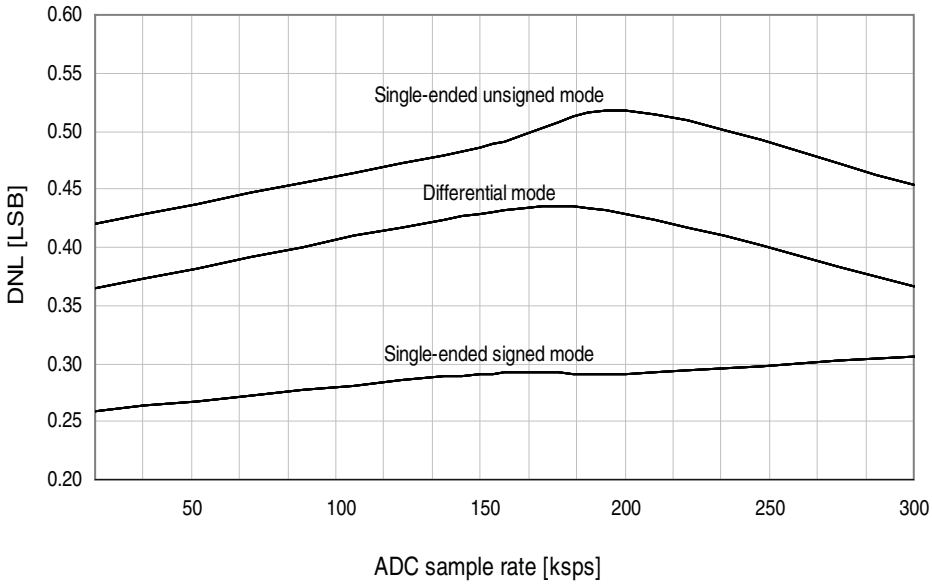


Figure 33-320. DNL error vs. input code.

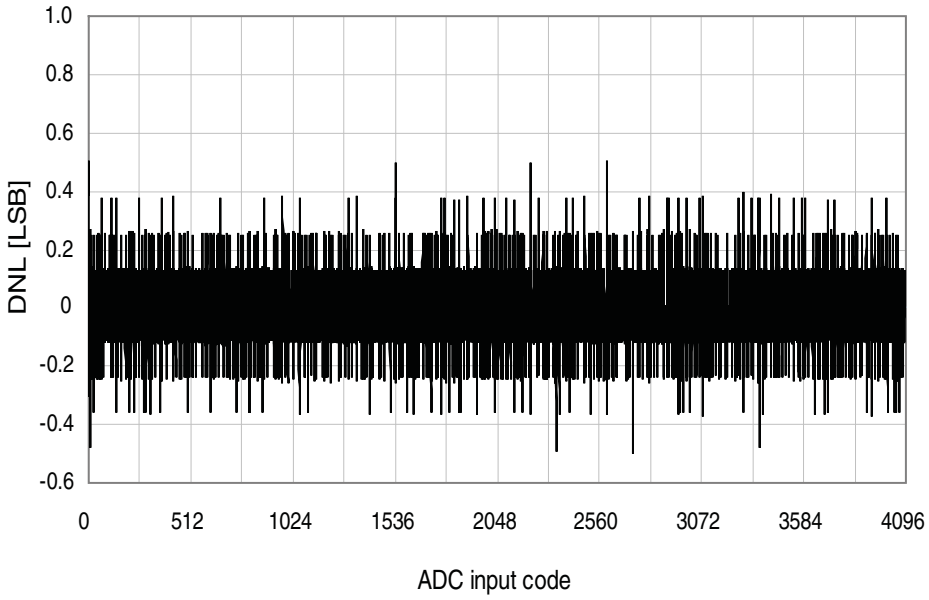


Figure 33-321. Gain error vs. V_{REF}.

T = 25°C, V_{CC} = 3.6V, ADC sample rate = 300ksps.

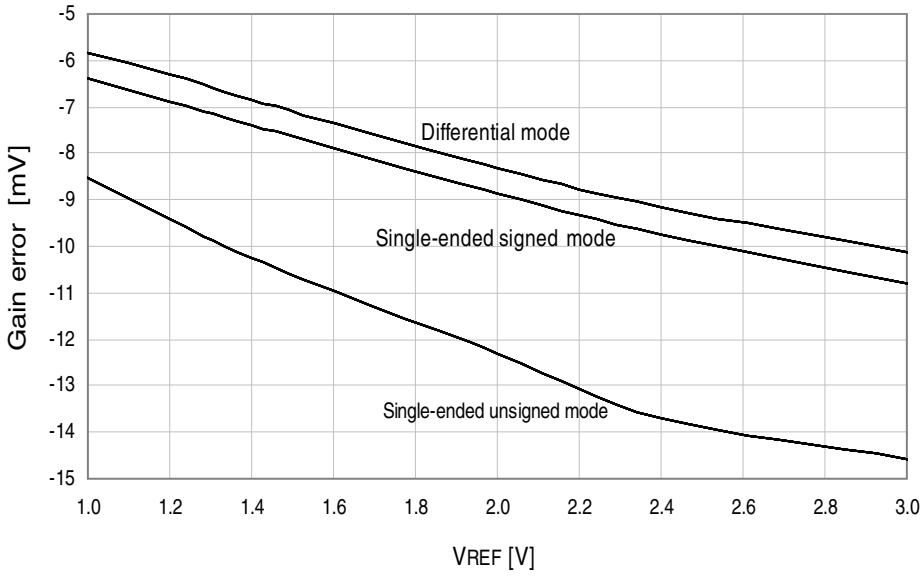


Figure 33-322. Gain error vs. V_{CC}.

T = 25°C, V_{REF} = external 1.0V, ADC sample rate = 300ksps.

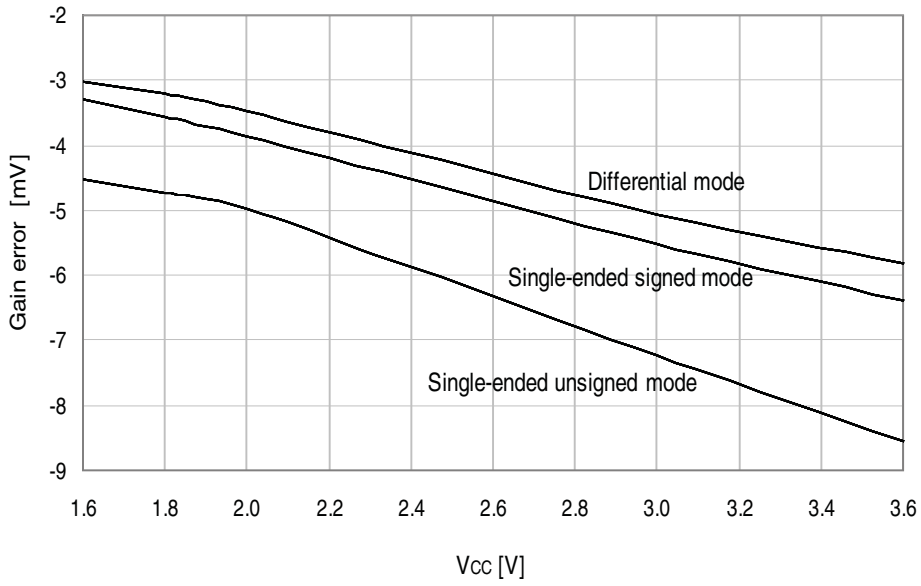


Figure 33-323. Offset error vs. V_{REF}.

T = 25°C, V_{CC} = 3.6V, ADC sample rate = 300ksps.

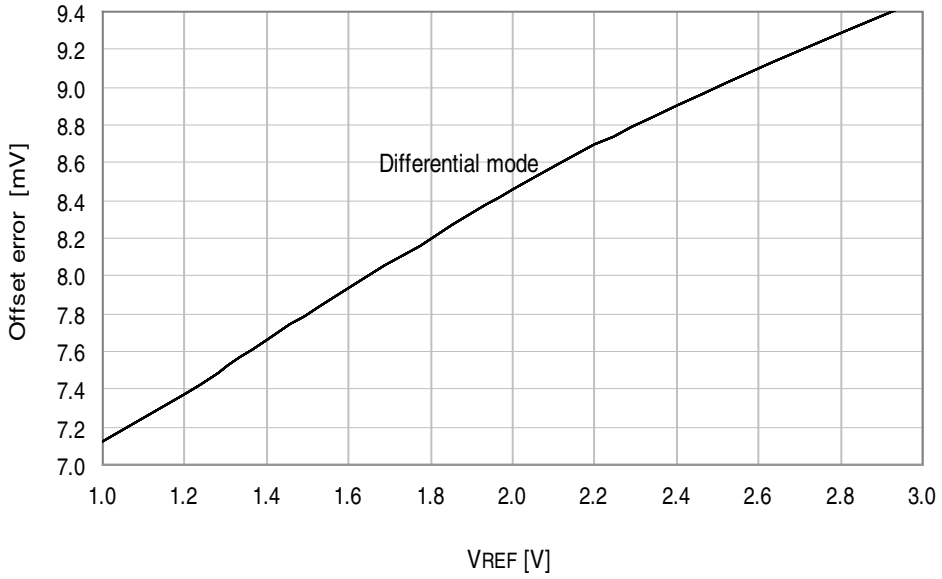


Figure 33-324. Gain error vs. temperature.
V_{CC} = 3.0V, V_{REF} = external 2.0V.

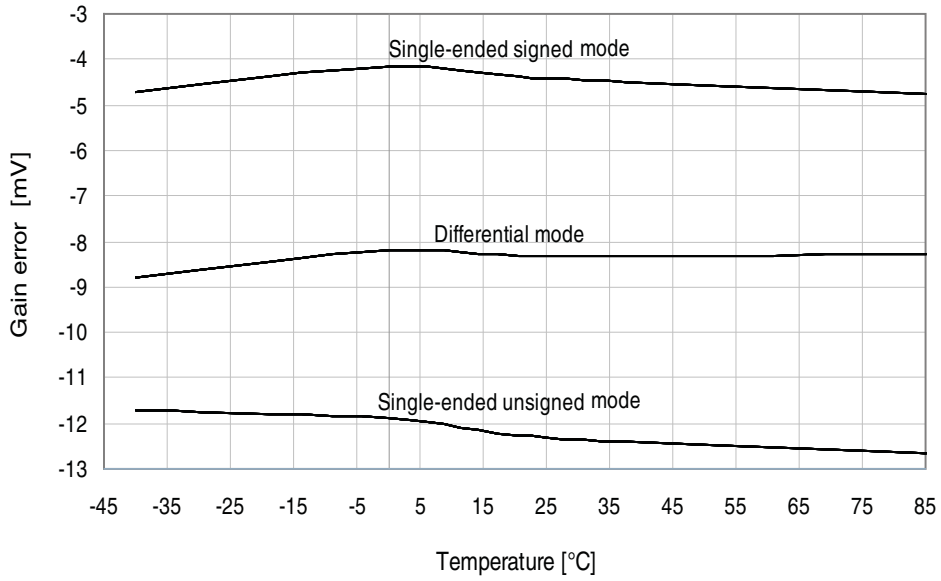
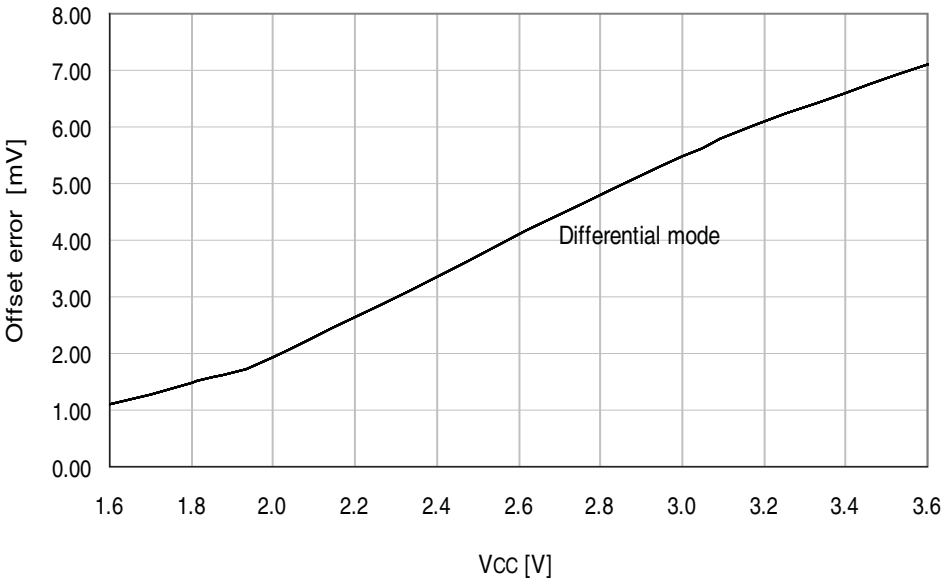


Figure 33-325. Offset error vs. V_{CC}.
T = 25°C, V_{REF} = external 1.0V, ADC sample rate = 300ksps.



33.6.4 Analog comparator characteristics

Figure 33-326. Analog comparator hysteresis vs. V_{CC}.
***Small hysteresis*.**

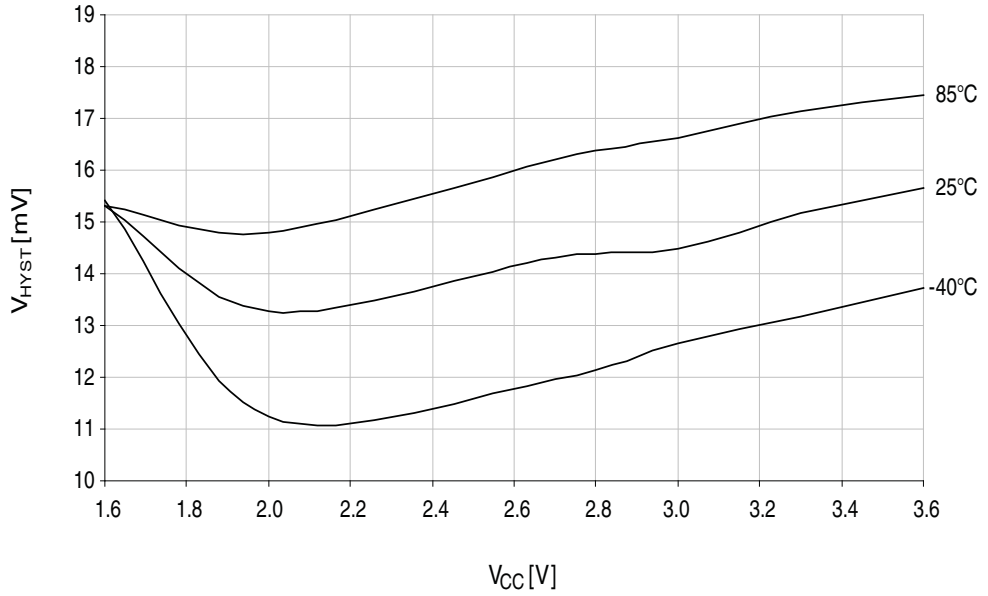


Figure 33-327. Analog comparator hysteresis vs. V_{CC}.
***Large hysteresis*.**

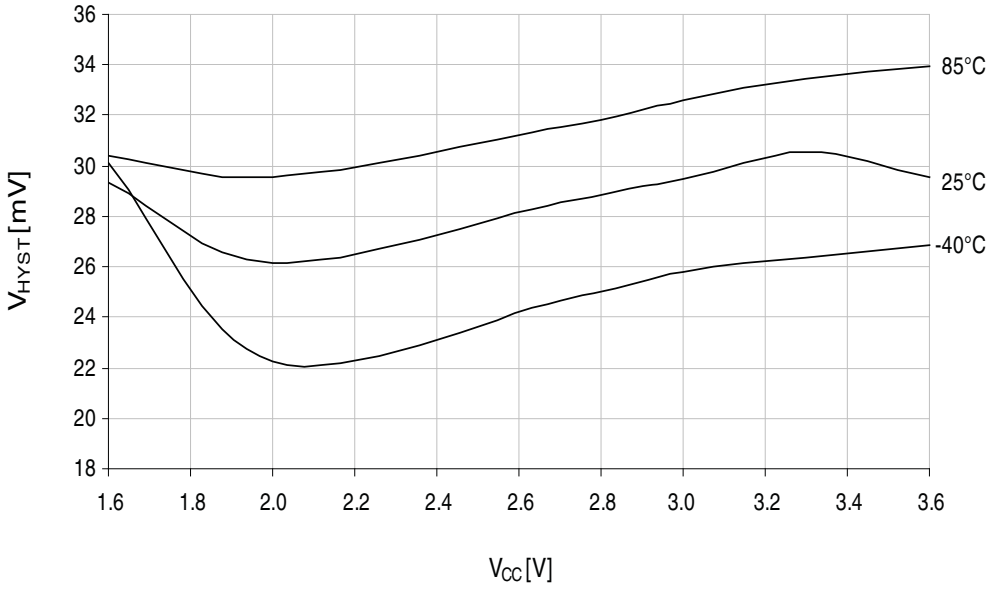


Figure 33-328. Analog comparator current source vs. calibration value.
V_{CC} = 3.0V.

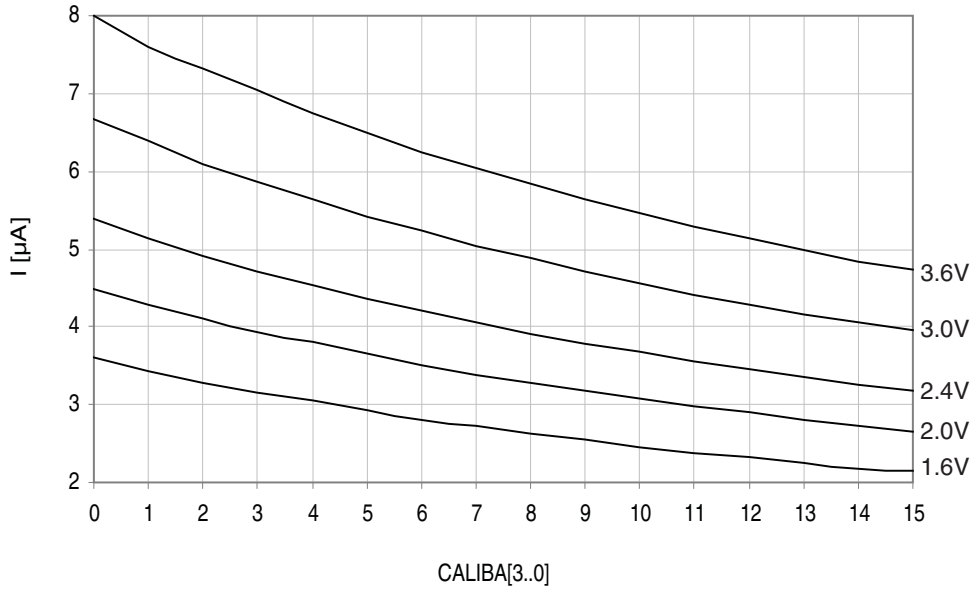
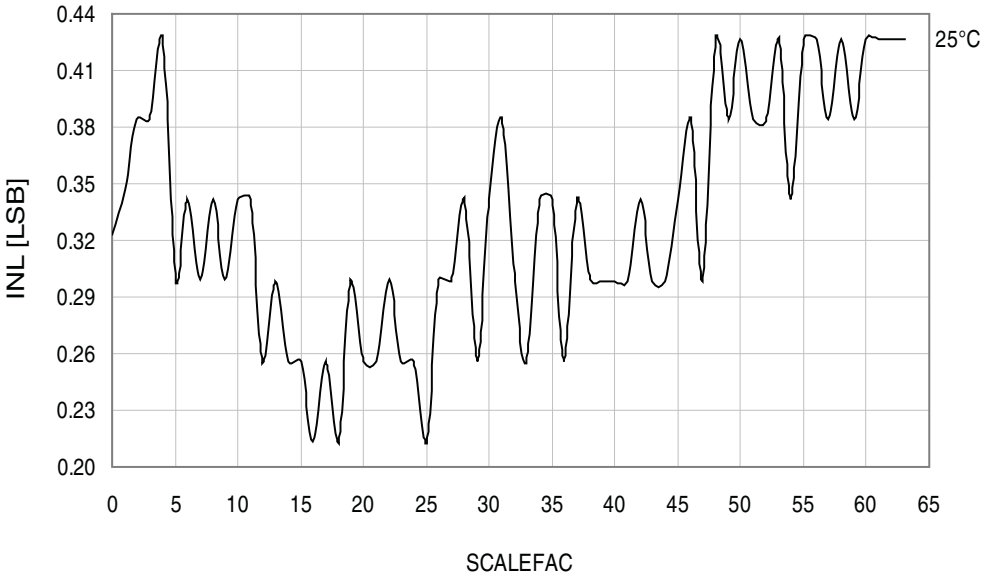
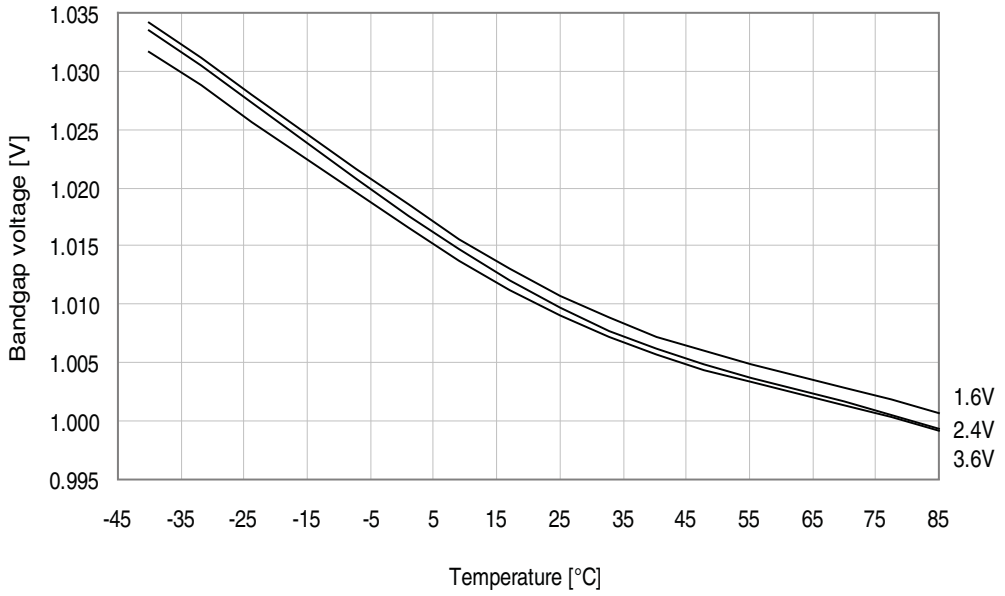


Figure 33-329. Voltage scaler INL vs. SCALEFAC.
T = 25°C, V_{CC} = 3.0V.



33.6.5 Internal 1.0V reference characteristics

Figure 33-330. ADC Internal 1.0V reference vs. temperature.



33.6.6 BOD characteristics

Figure 33-331. BOD thresholds vs. temperature.
BOD level = 1.6V.

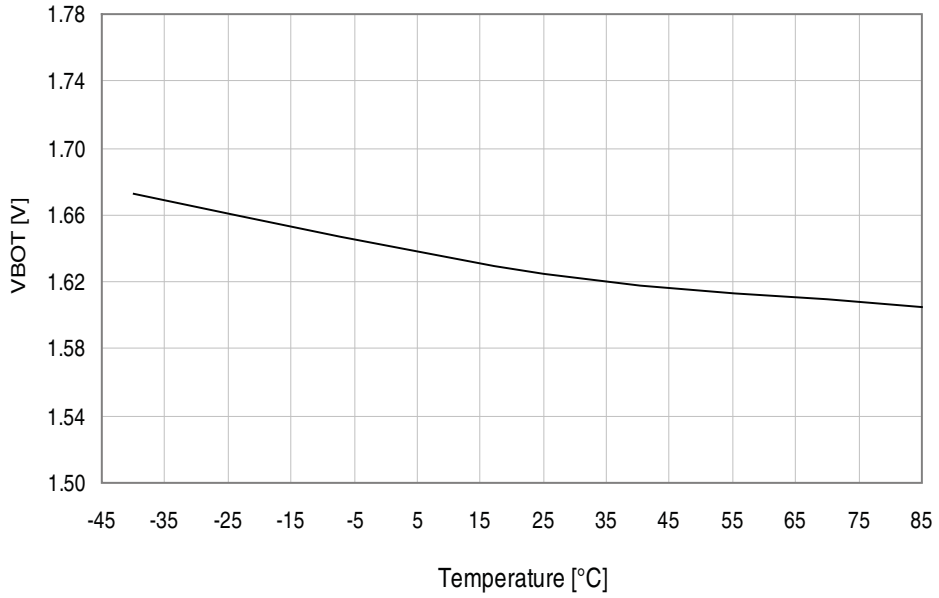
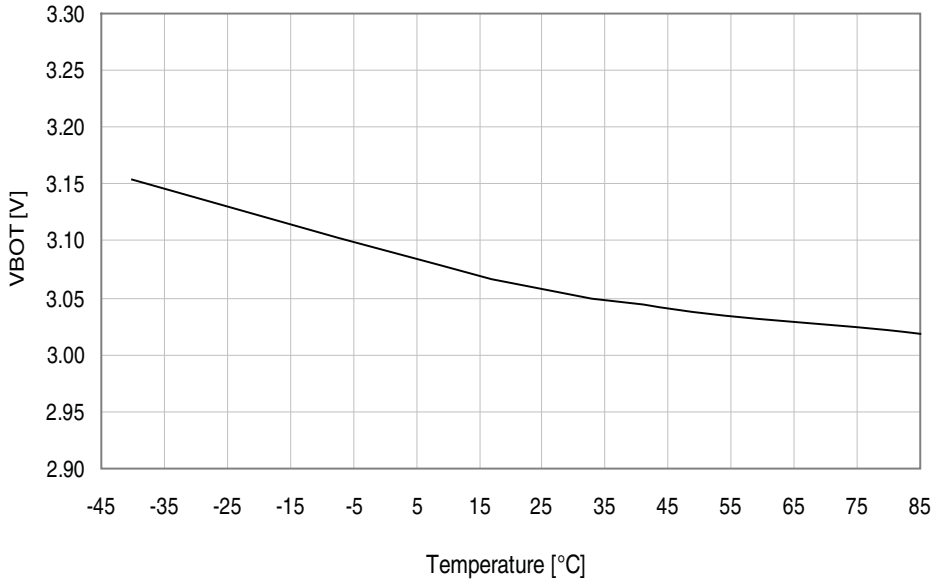


Figure 33-332. BOD thresholds vs. temperature.
BOD level = 3.0V.



33.6.7 External reset characteristics

Figure 33-333. Minimum reset pin pulse width vs. V_{CC}.

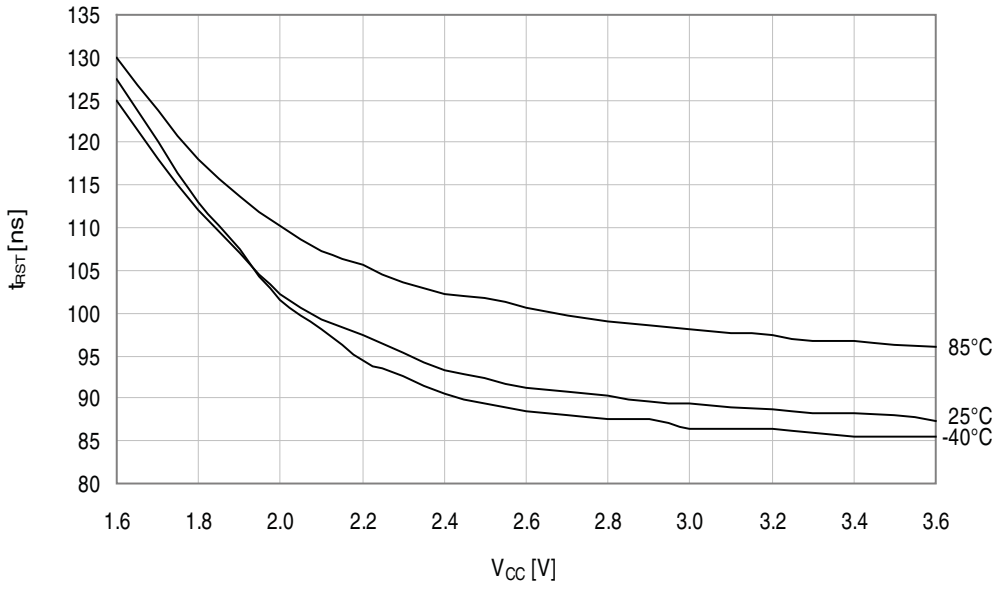


Figure 33-334. Reset pin pull-up resistor current vs. reset pin voltage.
V_{CC} = 1.8V.

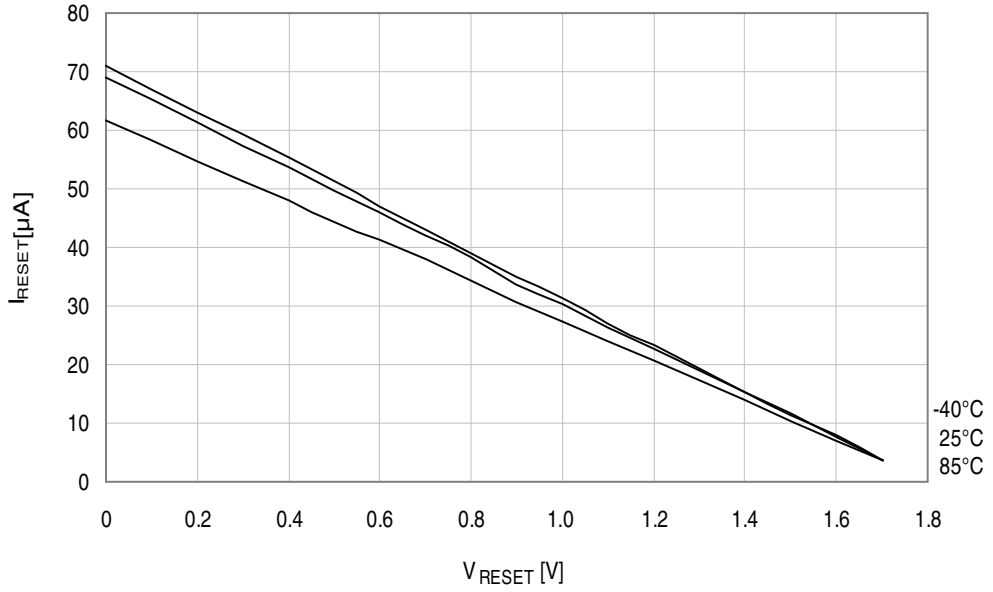


Figure 33-335. Reset pin pull-up resistor current vs. reset pin voltage.
V_{CC} = 3.0V.

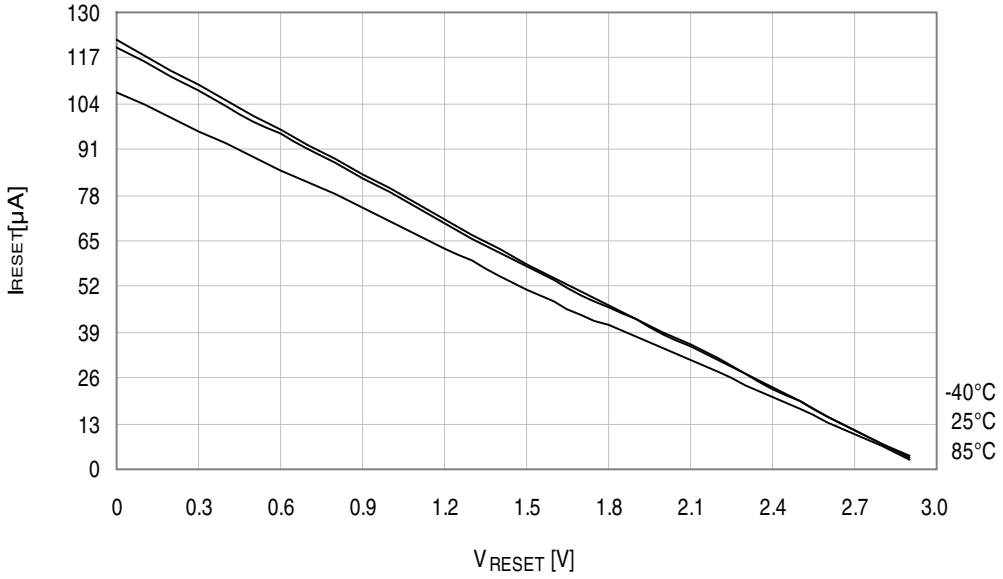


Figure 33-336. Reset pin pull-up resistor current vs. reset pin voltage.
V_{CC} = 3.3V.

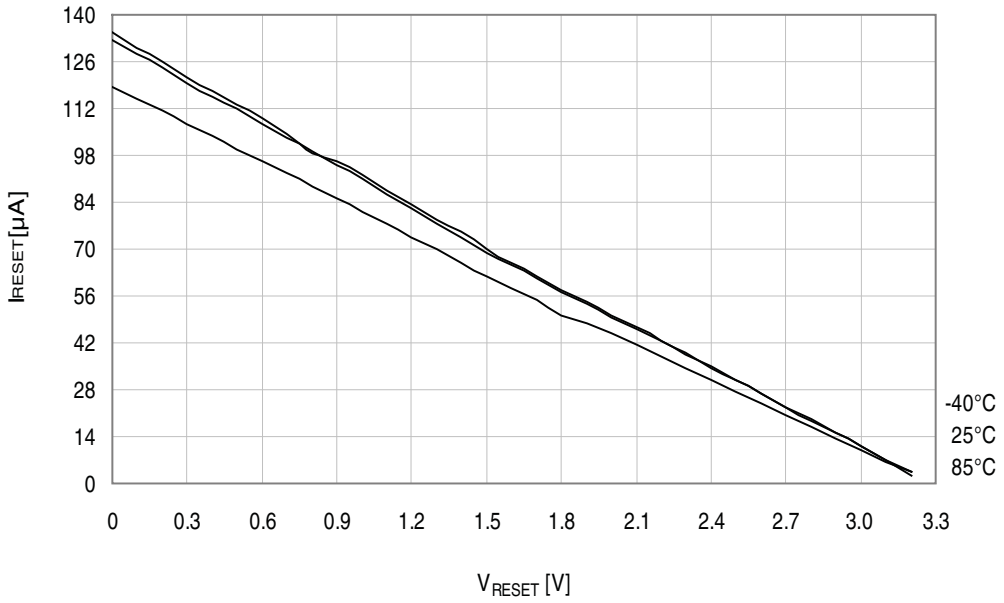
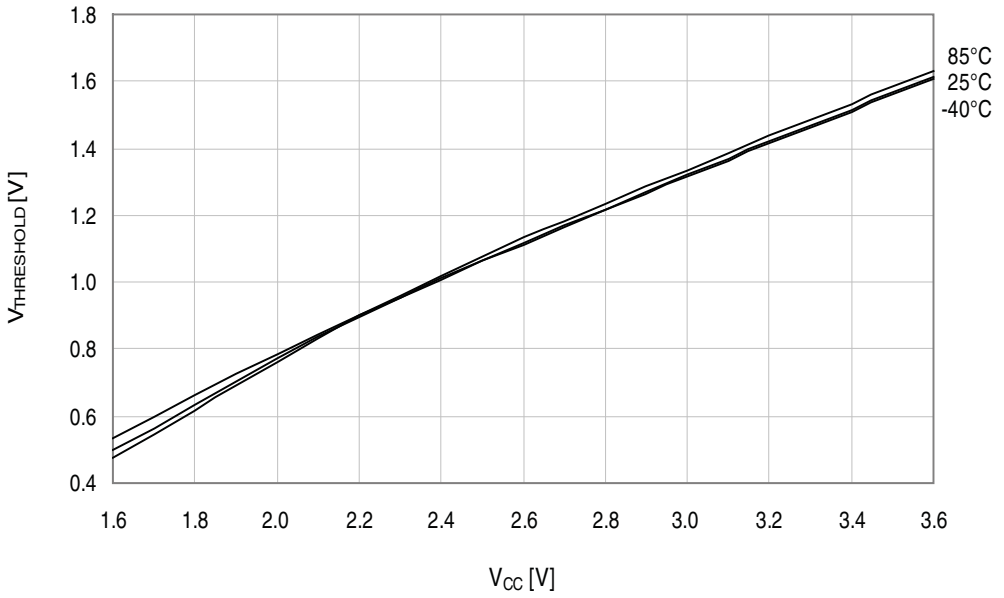


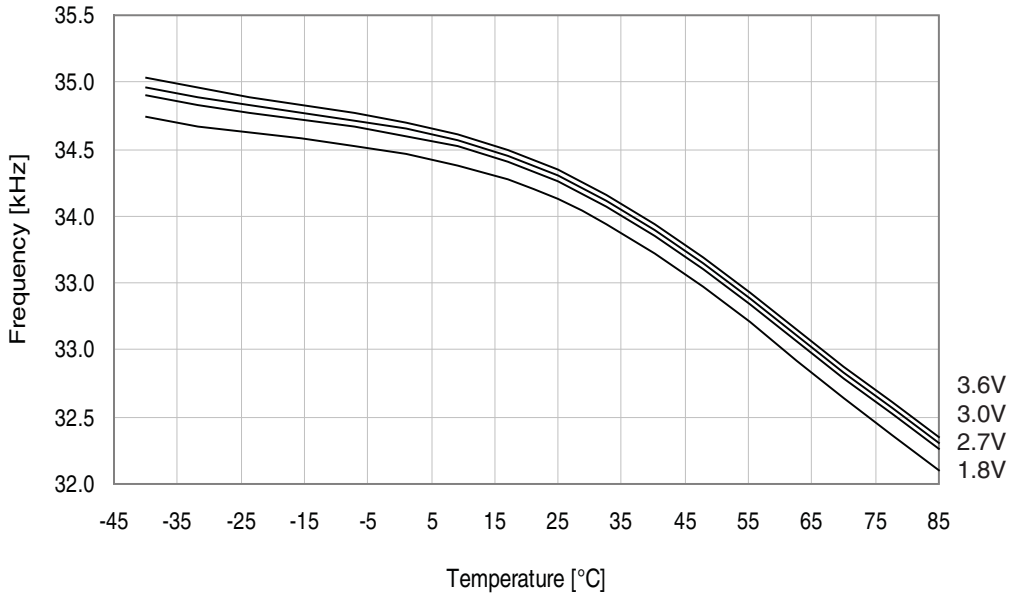
Figure 33-337. Reset pin input threshold voltage vs. V_{CC}.
V_{IH} - Reset pin read as "1".



33.6.8 Oscillator characteristics

33.6.8.1 Ultra Low-Power internal oscillator

Figure 33-338. Ultra Low-Power internal oscillator frequency vs. temperature.



33.6.8.2 32.768kHz internal oscillator

Figure 33-339. 32.768kHz internal oscillator frequency vs. temperature.

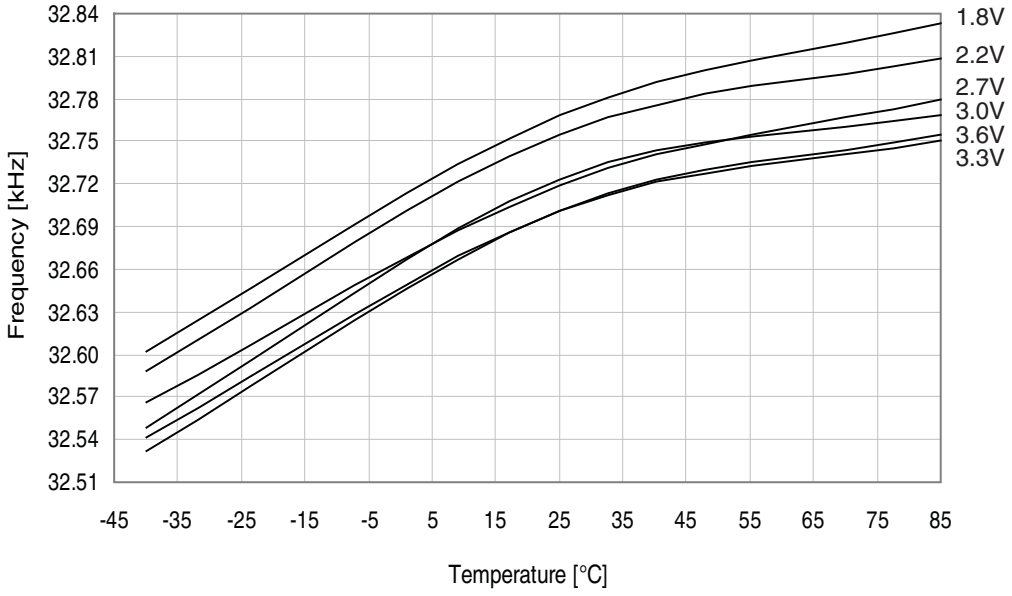
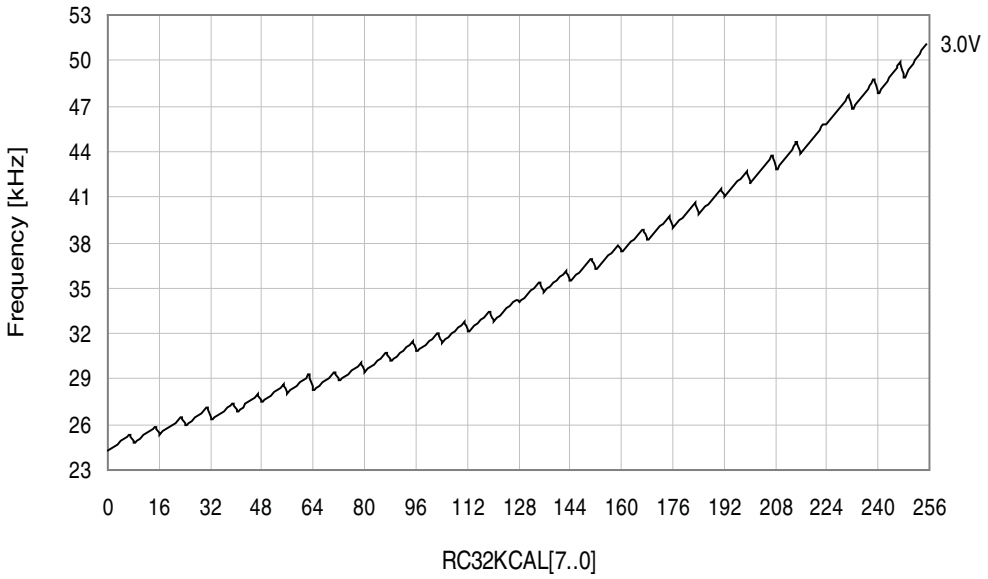


Figure 33-340. 32.768kHz internal oscillator frequency vs. calibration value.
V_{CC} = 3.0V, T = 25°C.



33.6.8.3 2MHz internal oscillator

Figure 33-341. 2MHz internal oscillator frequency vs. temperature.
DFLL disabled.

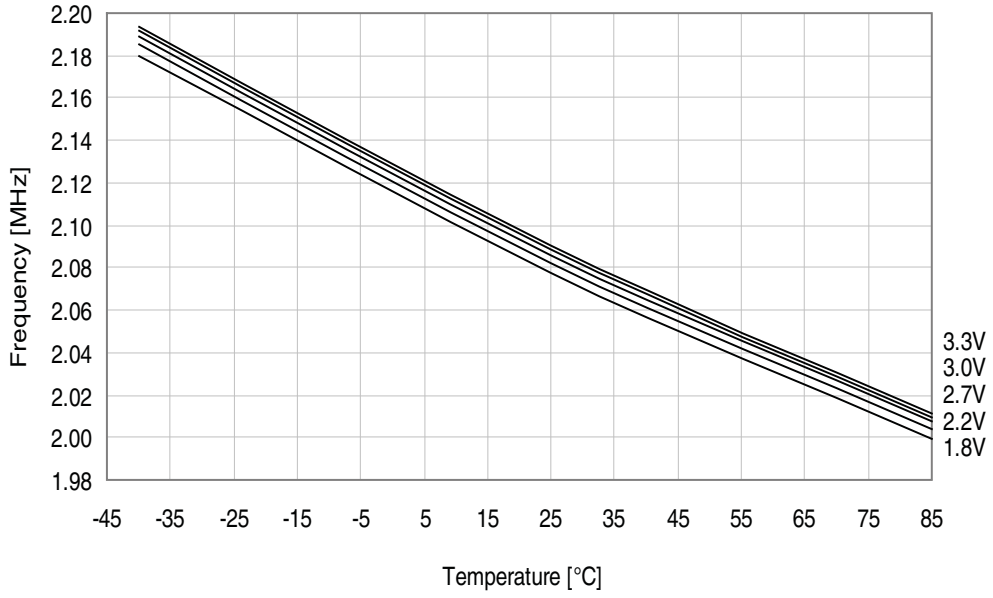


Figure 33-342. 2MHz internal oscillator frequency vs. temperature.
DFLL enabled, from the 32.768kHz internal oscillator .

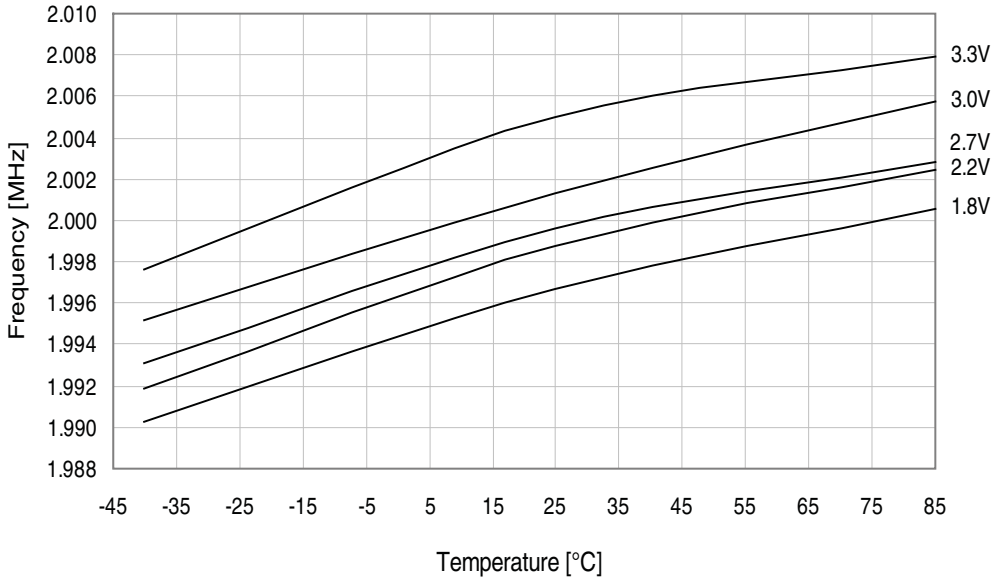
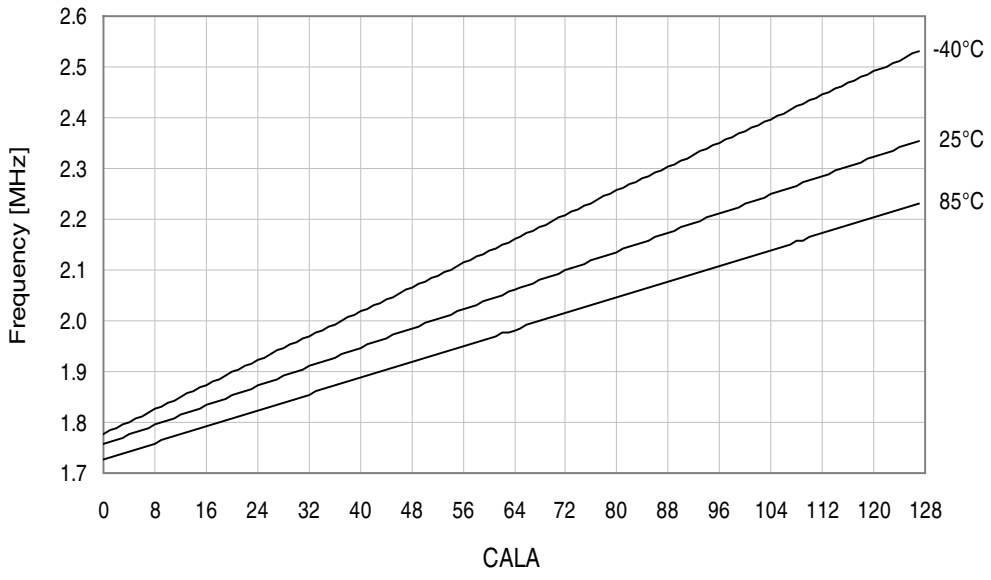


Figure 33-343. 2MHz internal oscillator frequency vs. CALA calibration value.
V_{CC} = 3V.



33.6.8.4 32MHz internal oscillator

Figure 33-344. 32MHz internal oscillator frequency vs. temperature.
DFLL disabled.

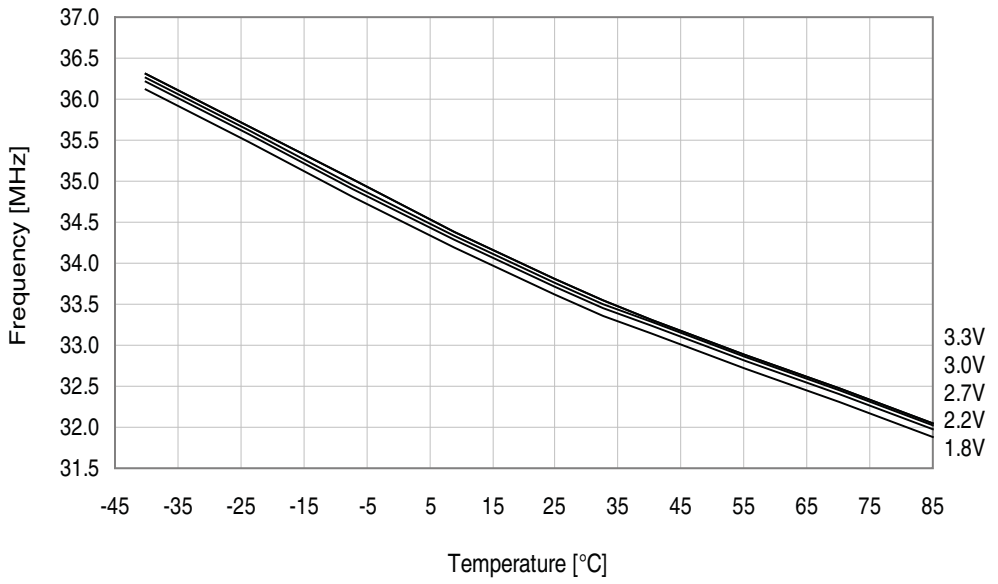


Figure 33-345. 32MHz internal oscillator frequency vs. temperature.
DFLL enabled, from the 32.768kHz internal oscillator.

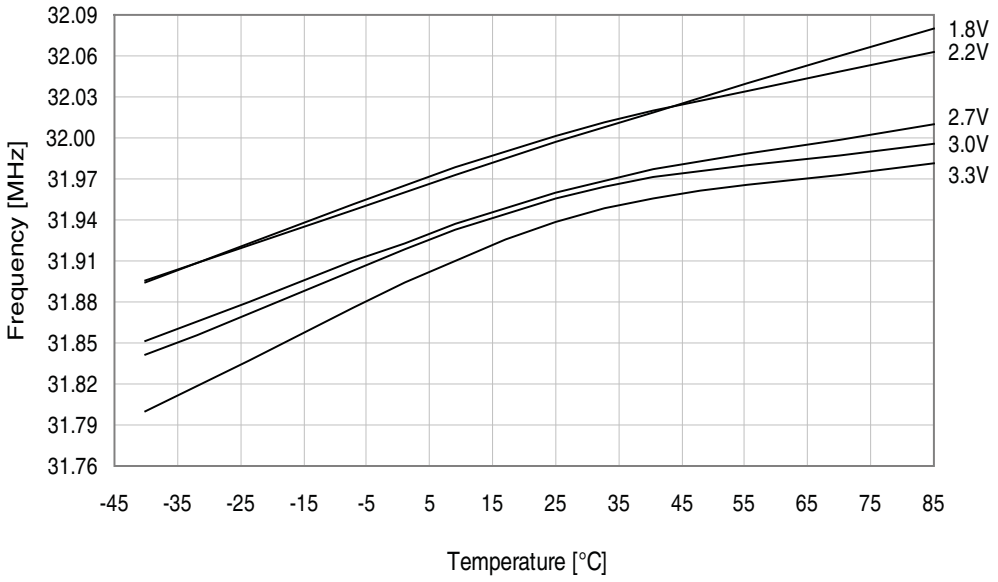


Figure 33-346. 32MHz internal oscillator CALA calibration step size.
V_{CC} = 3.0V.

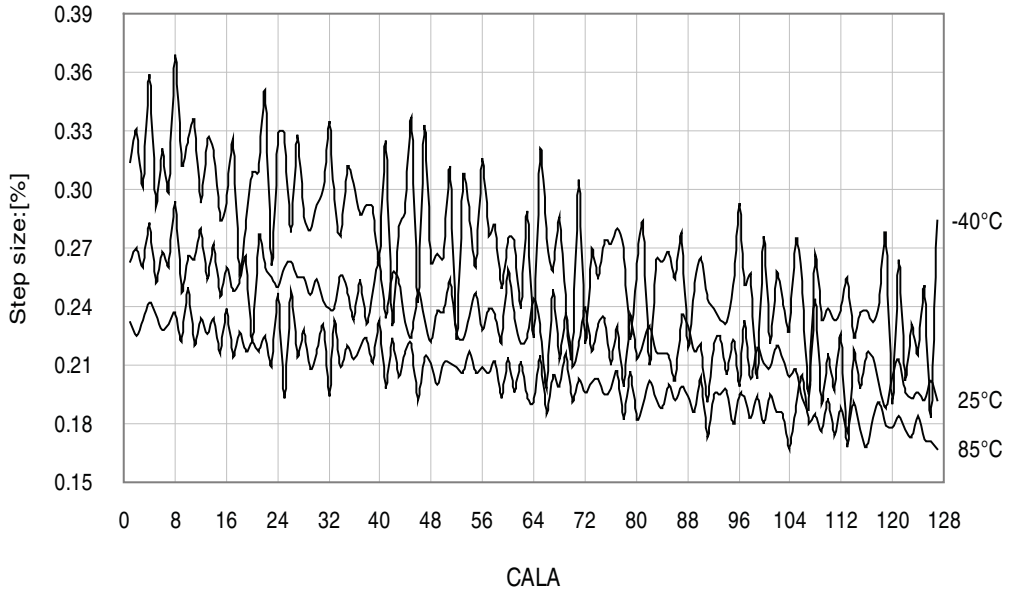
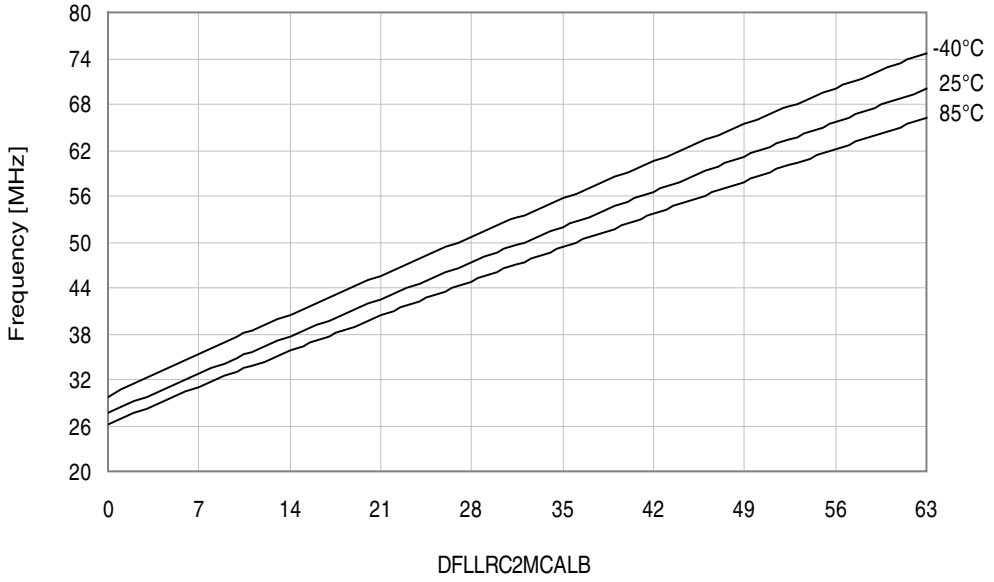


Figure 33-347. 32MHz internal oscillator frequency vs. CALB calibration value.
V_{CC} = 3.0V.



33.6.8.5 32MHz internal oscillator calibrated to 48MHz

Figure 33-348. 48MHz internal oscillator frequency vs. temperature.
DFLL disabled.

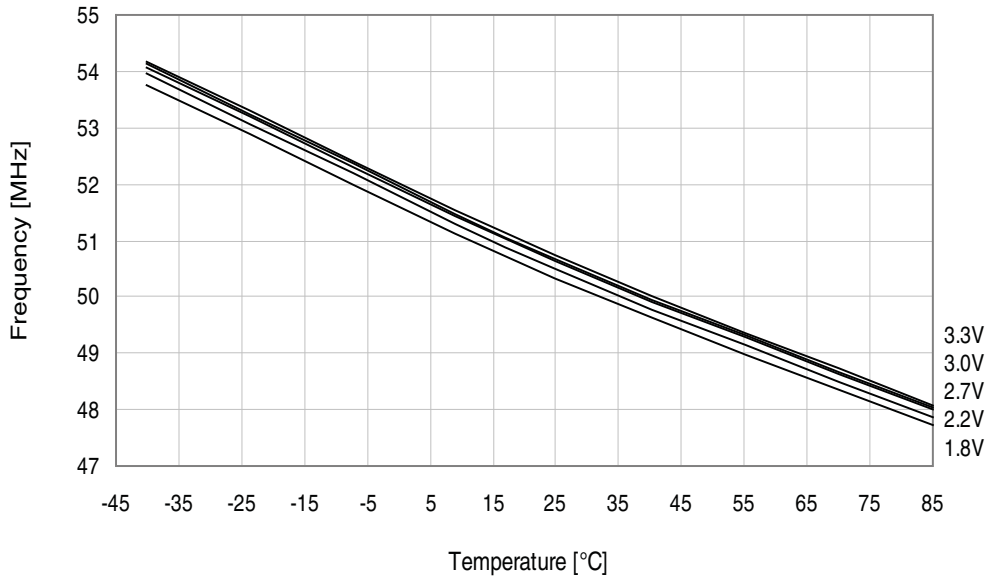
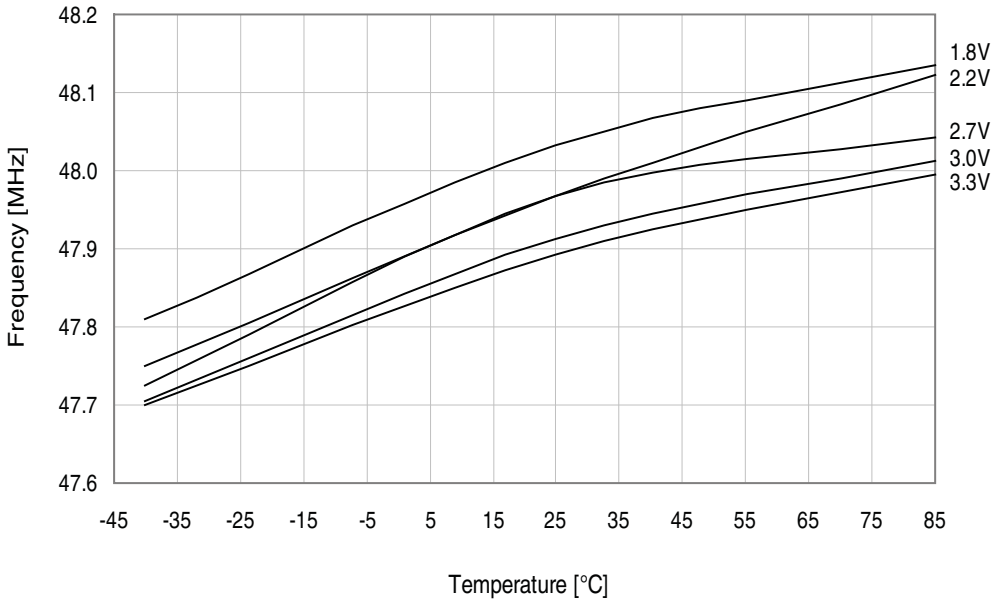


Figure 33-349. 48MHz internal oscillator frequency vs. temperature.
***DFLL enabled, from the 32.768kHz internal oscillator*.**



33.6.9 Two-wire interface characteristics

Figure 33-350. SDA hold time vs. temperature.

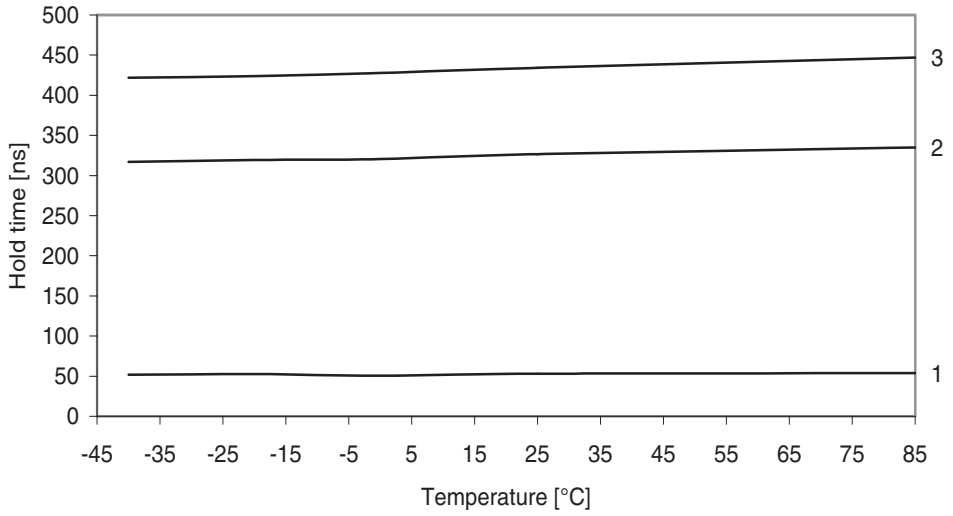
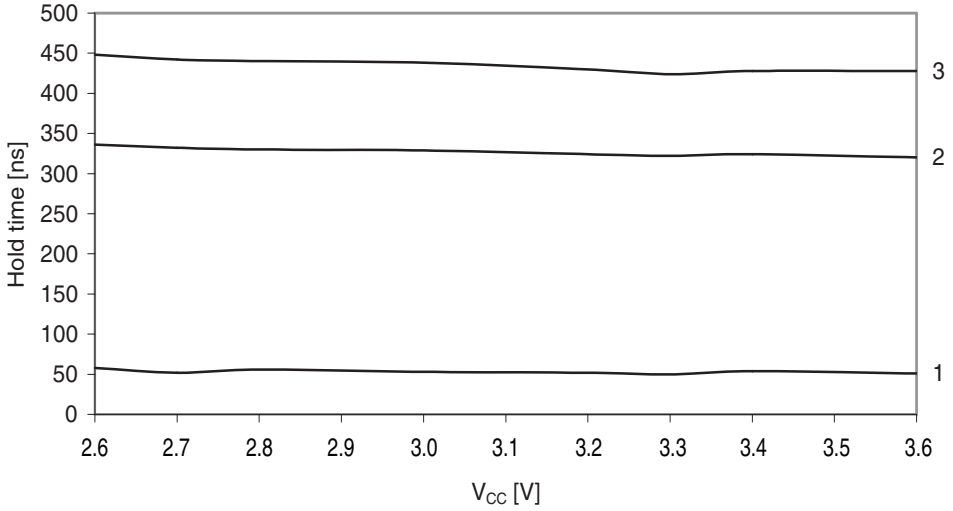
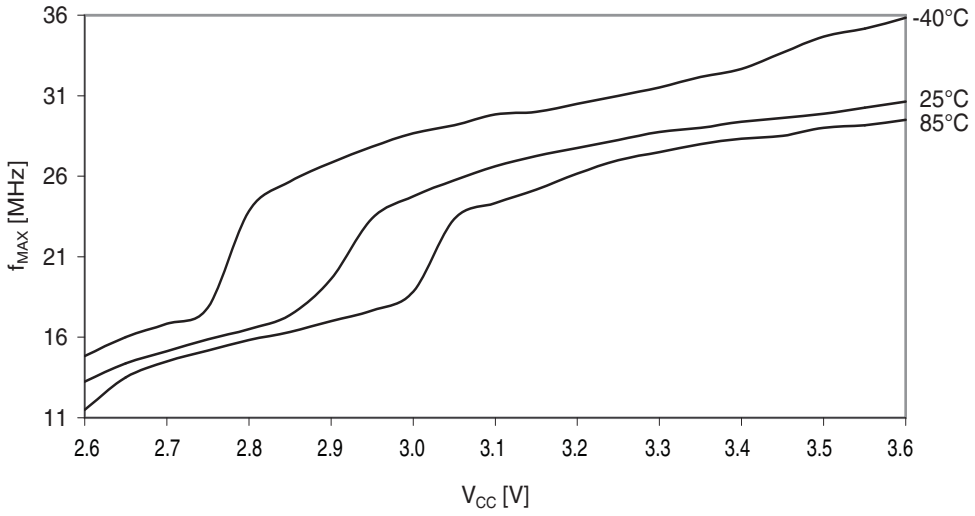


Figure 33-351. SDA hold time vs. supply voltage.



33.6.10 PDI characteristics

Figure 33-352. Maximum PDI frequency vs. V_{CC}.



34. Errata

34.1 Atmel ATxmega64D3

34.1.1 Rev. I

- AC system status flags are only valid if AC-system is enabled.

1. AC system status flags are only valid if AC-system is enabled

The status flags for the ac-output are updated even though the AC is not enabled which is invalid. Also, it is not possible to clear the AC interrupt flags without enabling either of the Analog comparators.

Problem fix/Workaround

Software should clear the AC system flags once, after enabling the AC system before using the AC system status flags.

34.1.2 Rev. H

Not sampled.

34.1.3 Rev. G

Not sampled.

34.1.4 Rev. F

Not sampled.

34.1.5 Rev. E

- Bandgap voltage input for the ACs can not be changed when used for both ACs simultaneously
- V_{CC} voltage scaler for AC is non-linear
- ADC gain stage cannot be used for single conversion
- ADC has increased INL error for some operating conditions
- ADC gain stage output range is limited to 2.4V
- ADC Event on compare match non-functional
- ADC propagation delay is not correct when 8× – 64× gain is used
- Bandgap measurement with the ADC is non-functional when V_{CC} is below 2.7V
- Accuracy lost on first three samples after switching input to ADC gain stage
- Configuration of PGM and CWCM not as described in XMEGA D Manual
- PWM is not restarted properly after a fault in cycle-by-cycle mode
- BOD will be enabled at any reset
- EEPROM page buffer always written when NVM DATA0 is written
- Pending full asynchronous pin change interrupts will not wake the device
- Pin configuration does not affect Analog Comparator Output
- NMI Flag for Crystal Oscillator Failure automatically cleared
- Crystal start-up time required after power-save even if crystal is source for RTC
- RTC Counter value not correctly read after sleep
- Pending asynchronous RTC-interrupts will not wake up device
- TWI Transmit collision flag not cleared on repeated start

- Clearing TWI Stop Interrupt Flag may lock the bus
- TWI START condition at bus timeout will cause transaction to be dropped
- TWI Data Interrupt Flag (DIF) erroneously read as set
- WDR instruction inside closed window will not issue reset
- Non available functions and options

1. Bandgap voltage input for the ACs cannot be changed when used for both ACs simultaneously

If the Bandgap voltage is selected as input for one Analog Comparator (AC) and then selected/deselected as input for another AC, the first comparator will be affected for up to 1µs and could potentially give a wrong comparison result.

Problem fix/Workaround

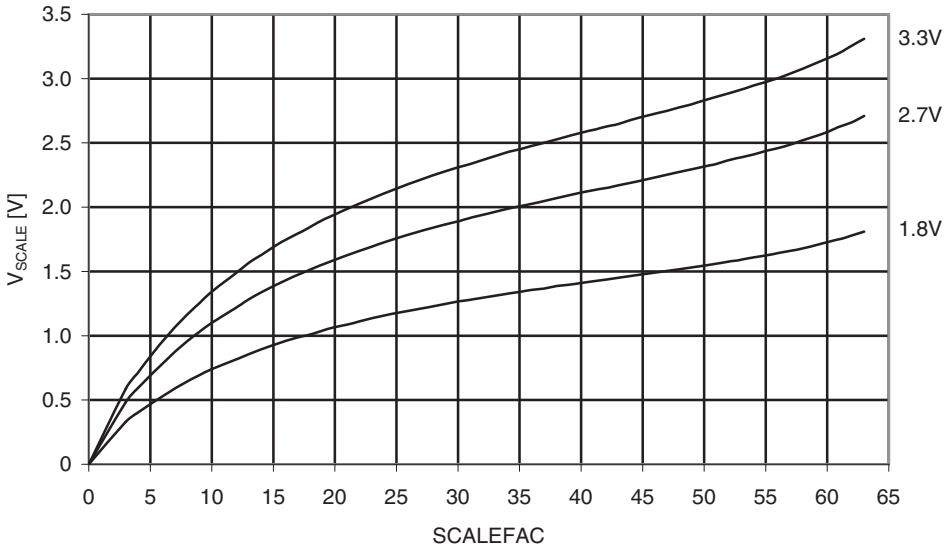
If the Bandgap is required for both ACs simultaneously, configure the input selection for both ACs before enabling any of them.

2. VCC voltage scaler for AC is non-linear

The 6-bit V_{CC} voltage scaler in the Analog Comparators is non-linear.

Figure 34-1. Analog comparator voltage scaler vs. scalefac.

T = 25°C.



Problem fix/Workaround

Use external voltage input for the analog comparator if accurate voltage levels are needed.

3. ADC gain stage cannot be used for single conversion

The ADC gain stage will not output correct result for single conversion that is triggered and started from software or event system.

Problem fix/Workaround

When the gain stage is used, the ADC must be set in free running mode for correct results.

4. **ADC has increased INL error for some operating conditions**

   Some ADC configurations or operating condition will result in increased INL error.

   In signed mode INL is increased to:

   6LSB for sample rates above 130ksps, and up to 8LSB for 200ksps sample rate.

   6LSB for reference voltage below 1.1V when V_{CC} is above 3.0V.

   20LSB for ambient temperature below 0°C and reference voltage below 1.3V.

   In unsigned mode, the INL error cannot be guaranteed, and this mode should not be used.

   Problem fix/Workaround

   None, avoid using the ADC in the above configurations in order to prevent increased INL error. Use the ADC in signed mode also for single ended measurements.

5. **ADC gain stage output range is limited to 2.4V**

   The amplified output of the ADC gain stage will never go above 2.4V, hence the differential input will only give correct output when below 2.4V/gain. For the available gain settings, this gives a differential input range of:

   - 1× gain: 2.4 V
   - 2× gain: 1.2 V
   - 4× gain: 0.6 V
   - 8× gain: 300 mV
   - 16× gain: 150 mV
   - 32× gain: 75 mV
   - 64× gain: 38 mV

   Problem fix/Workaround

   Keep the amplified voltage output from the ADC gain stage below 2.4V in order to get a correct result, or keep ADC voltage reference below 2.4V.

6. **ADC Event on compare match non-functional**

   ADC signalling event will be given at every conversion complete even if Interrupt mode (INTMODE) is set to BELOW or ABOVE.

   Problem fix/Workaround

   Enable and use interrupt on compare match when using the compare function.

7. **ADC propagation delay is not correct when 8× – 64× gain is used**

   The propagation delay will increase by only one ADC clock cycle for all gain settings.

   Problem fix/Workaround

   None.

8. **Bandgap measurement with the ADC is non-functional when V_{CC} is below 2.7V**

   The ADC can not be used to do bandgap measurements when V_{CC} is below 2.7V.

Problem fix/Workaround

None.

9. Accuracy lost on first three samples after switching input to ADC gain stage

Due to memory effect in the ADC gain stage, the first three samples after changing input channel must be disregarded to achieve 12-bit accuracy.

Problem fix/Workaround

Run three ADC conversions and discard these results after changing input channels to ADC gain stage.

10. Configuration of PGM and CWCM not as described in XMEGA D Manual

Enabling Common Waveform Channel Mode will enable Pattern generation mode (PGM), but not Common Waveform Channel Mode.

Enabling Pattern Generation Mode (PGM) and not Common Waveform Channel Mode (CWCM) will enable both Pattern Generation Mode and Common Waveform Channel Mode.

Problem fix/Workaround

Table 34-1. Configure PWM and CWCM according to this table:

PGM	CWCM	Description
0	0	PGM and CWCM disabled
0	1	PGM enabled
1	0	PGM and CWCM enabled
1	1	PGM enabled

11. PWM is not restarted properly after a fault in cycle-by-cycle mode

When the AWeX fault restore mode is set to cycle-by-cycle, the waveform output will not return to normal operation at first update after fault condition is no longer present.

Problem fix/Workaround

Do a write to any AWeX I/O register to re-enable the output.

12. BOD will be enabled after any reset

If any reset source goes active, the BOD will be enabled and keep the device in reset if the V_{CC} voltage is below the programmed BOD level. During Power-On Reset, reset will not be released until V_{CC} is above the programmed BOD level even if the BOD is disabled.

Problem fix/Workaround

Do not set the BOD level higher than V_{CC} even if the BOD is not used.

13. EEPROM page buffer always written when NVM DATA0 is written

If the EEPROM is memory mapped, writing to NVM DATA0 will corrupt data in the EEPROM page buffer.

Problem fix/Workaround

Before writing to NVM DATA0, for example when doing software CRC or flash page buffer write, check if EEPROM page buffer active loading flag (EELOAD) is set. Do not write NVM DATA0 when EELOAD is set.

14. Pending full asynchronous pin change interrupts will not wake the device

Any full asynchronous pin-change Interrupt from pin 2, on any port, that is pending when the sleep instruction is executed, will be ignored until the device is woken from another source or the source triggers again. This applies when entering all sleep modes where the System Clock is stopped.

Problem fix/Workaround

None.

15. Pin configuration does not affect Analog Comparator output

The Output/Pull and inverted pin configuration does not affect the Analog Comparator output.

Problem fix/Workaround

None for Output/Pull configuration.

For inverted I/O, configure the Analog Comparator to give an inverted result (that is, connect positive input to the negative AC input and vice versa), or use and external inverter to change polarity of Analog Comparator output.

16. NMI Flag for Crystal Oscillator Failure automatically cleared

NMI flag for Crystal Oscillator Failure (XOSCFDIF) will be automatically cleared when executing the NMI interrupt handler.

Problem fix/Workaround

This device revision has only one NMI interrupt source, so checking the interrupt source in software is not required.

17. Crystal start-up time required after power-save even if crystal is source for RTC

Even if 32.768kHz crystal is used for RTC during sleep, the clock from the crystal will not be ready for the system before the specified start-up time. See "XOSCSEL[3:0]: Crystal Oscillator Selection" in XMEGA D Manual. If BOD is used in active mode, the BOD will be on during this period (0.5s).

Problem fix/Workaround

If faster start-up is required, go to sleep with internal oscillator as system clock.

18. RTC Counter value not correctly read after sleep

If the RTC is set to wake up the device on RTC Overflow and bit 0 of RTC CNT is identical to bit 0 of RTC PER as the device is entering sleep, the value in the RTC count register can not be read correctly within the first prescaled RTC clock cycle after wakeup. The value read will be the same as the value in the register when entering sleep.

The same applies if RTC Compare Match is used as wake-up source.

Problem fix/Workaround

Wait at least one prescaled RTC clock cycle before reading the RTC CNT value.

19. Pending asynchronous RTC-interrupts will not wake up device

Asynchronous Interrupts from the Real-Time-Counter that is pending when the sleep instruction is executed, will be ignored until the device is woken from another source or the source triggers again.

Problem fix/Workaround

None.

20. TWI Transmit collision flag not cleared on repeated start

The TWI transmit collision flag should be automatically cleared on start and repeated start, but is only cleared on start.

Problem fix/Workaround

Clear the flag in software after address interrupt.

21. Clearing TWI Stop Interrupt Flag may lock the bus

If software clears the STOP Interrupt Flag (APIF) on the same Peripheral Clock cycle as the hardware sets this flag due to a new address received, CLKHOLD is not cleared and the SCL line is not released. This will lock the bus.

Problem fix/Workaround

Check if the bus state is IDLE. If this is the case, it is safe to clear APIF. If the bus state is not IDLE, wait for the SCL pin to be low before clearing APIF.

Code:

```
/* Only clear the interrupt flag if within a "safe zone". */
while ( /* Bus not IDLE: */
       ((COMMS_TWI.MASTER.STATUS & TWI_MASTER_BUSSTATE_gm) !=
         TWI_MASTER_BUSSTATE_IDLE_gc)) &&
         /* SCL not held by slave: */
         !(COMMS_TWI.SLAVE.STATUS & TWI_SLAVE_CLKHOLD_bm)
      )
{
    /* Ensure that the SCL line is low */
    if ( !(COMMS_PORT.IN & PIN1_bm) )
        if ( !(COMMS_PORT.IN & PIN1_bm) )
            break;
}
/* Check for an pending address match interrupt */
if ( !(COMMS_TWI.SLAVE.STATUS & TWI_SLAVE_CLKHOLD_bm) )
{
    /* Safely clear interrupt flag */
    COMMS_TWI.SLAVE.STATUS |= (uint8_t)TWI_SLAVE_APIF_bm;
}
```

22. TWI START condition at bus timeout will cause transaction to be dropped

If Bus Timeout is enabled and a timeout occurs on the same Peripheral Clock cycle as a START is detected, the transaction will be dropped.

Problem fix/Workaround

None.

23. TWI Data Interrupt Flag erroneously read as set

When issuing the TWI slave response command CMD=0b11, it takes one Peripheral Clock cycle to clear the data interrupt flag (DIF). A read of DIF directly after issuing the command will show the DIF still set.

Problem fix/Workaround

Add one NOP instruction before checking DIF.

24. WDR instruction inside closed window will not issue reset

When a WDR instruction is execute within one ULP clock cycle after updating the window control register, the counter can be cleared without giving a system reset.

Problem fix/Workaround

Wait at least one ULP clock cycle before executing a WDR instruction.

25. Non available functions and options

The below function and options are not available. Writing to any registers or fuse to try and enable or configure these functions or options will have no effect, and will be as writing to a reserved address location.

- TWIE, the TWI module on PORTE
- TWI SDAHOLD option in the TWI CTRL register is one bit
- CRC generator module
- ADC 1/2× gain option, and this configuration option in the GAIN bits in the ADC Channel CTRL register
- ADC VCC/2 reference option and this configuration option in the REFSEL bits on the ADC REFCTRL register
- ADC option to use internal Gnd as negative input in differential measurements and this configuration option in the MUXNEG bits in the ADC Channel MUXCTRL register
- ADC channel scan and the ADC SCAN register
- ADC current limitation option, and the CURRLIMIT bits in the ADC CTRLB register
- ADC impedance mode selection for the gain stage, and the IMPMODE bit in the ADC CTRLB register
- Timer/Counter 2 and the SPLITMODE configuration option in the BYTEM bits in the Timer/Counter 0 CTRLE register
- Analog Comparator (AC) current output option, and the AC CURRCTRL and CURRCALIB registers
- PORT remap functions with alternate pin locations for Timer/Counter output compare channels, USART0 and SPI, and the PORT REMAP register
- PORT RTC clock output option and the RTCOUT bit in the PORT CLKEVOUT register
- PORT remap functions with alternate pin locations for the clock and event output, and the CLKEVPIN bit in the PORT CLKEVOUT register
- TOSC alternate pin locations, and TOSCSEL bit in FUSEBYTE2
- Real Time Counter clock source options of external clock from TOSC1, and 32.768kHz from TOSC, and 32.768kHz from the 32.768kHz internal oscillator, and these configuration options in the RTCSRC bits in the Clock RTCTRL register
- PLL divide by two option, and the PLLDIV bit in the Clock PLLCTRL register
- PLL lock detection failure function and the PLLDIF and PLLFDEN bits in the Clock XOSCFAIL register
- The high drive option for external crystal and the XOSCPWR bit on the Oscillator XOSCCTRL register
- The option to enable sequential startup of the analog modules and the ANAINIT register in MCU Control memory

Problem fix/Workaround

None.

34.1.6 Rev. D

Not sampled.

34.1.7 Rev. C

Not sampled.

34.1.8 Rev. B

- Bandgap voltage input for the ACs can not be changed when used for both ACs simultaneously
- VCC voltage scaler for AC is non-linear
- ADC gain stage cannot be used for single conversion
- ADC has increased INL error for some operating conditions
- ADC gain stage output range is limited to 2.4V
- ADC Event on compare match non-functional
- ADC propagation delay is not correct when 8× – 64× gain is used
- Bandgap measurement with the ADC is non-functional when VCC is below 2.7V
- Accuracy lost on first three samples after switching input to ADC gain stage
- Configuration of PGM and CWCM not as described in XMEGA D Manual
- PWM is not restarted properly after a fault in cycle-by-cycle mode
- BOD will be enabled at any reset
- EEPROM page buffer always written when NVM DATA0 is written
- Pending full asynchronous pin change interrupts will not wake the device
- Pin configuration does not affect Analog Comparator Output
- NMI Flag for Crystal Oscillator Failure automatically cleared
- Writing EEPROM or Flash while reading any of them will not work
- Crystal start-up time required after power-save even if crystal is source for RTC
- RTC Counter value not correctly read after sleep
- Pending asynchronous RTC-interrupts will not wake up device
- TWI Transmit collision flag not cleared on repeated start
- Clearing TWI Stop Interrupt Flag may lock the bus
- TWI START condition at bus timeout will cause transaction to be dropped
- TWI Data Interrupt Flag (DIF) erroneously read as set
- WDR instruction inside closed window will not issue reset
- Non available functions and options

1. Bandgap voltage input for the ACs cannot be changed when used for both ACs simultaneously

If the Bandgap voltage is selected as input for one Analog Comparator (AC) and then selected/deselected as input for another AC, the first comparator will be affected for up to 1µs and could potentially give a wrong comparison result.

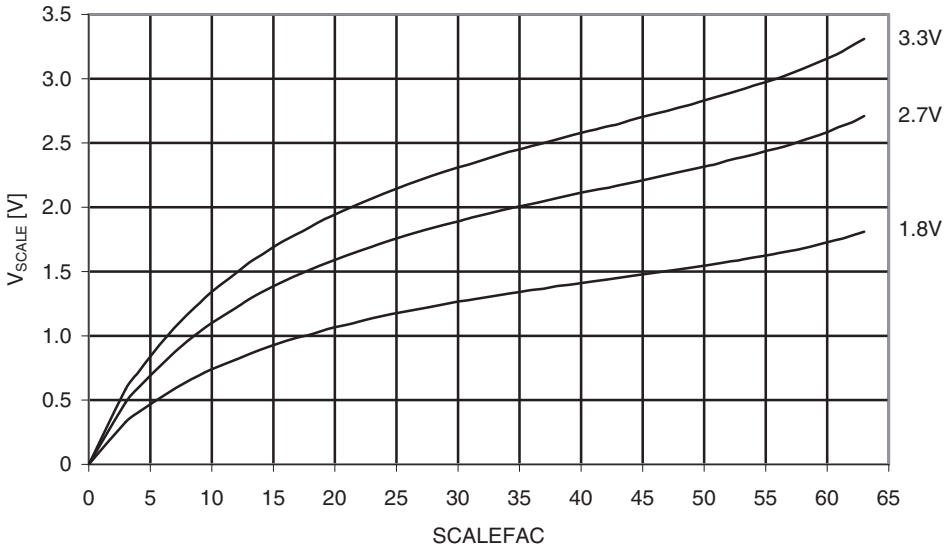
Problem fix/Workaround

If the Bandgap is required for both ACs simultaneously, configure the input selection for both ACs before enabling any of them.

2. VCC voltage scaler for AC is non-linear

The 6-bit V_{CC} voltage scaler in the Analog Comparators is non-linear.

Figure 34-2. Analog comparator voltage scaler vs. scalefac.
T = 25°C.



Problem fix/Workaround

Use external voltage input for the analog comparator if accurate voltage levels are needed.

3. ADC gain stage cannot be used for single conversion

The ADC gain stage will not output correct result for single conversion that is triggered and started from software or event system.

Problem fix/Workaround

When the gain stage is used, the ADC must be set in free running mode for correct results.

4. ADC has increased INL error for some operating conditions

Some ADC configurations or operating condition will result in increased INL error.

In signed mode INL is increased to:

6LSB for sample rates above 130ksps, and up to 8LSB for 200ksps sample rate.

6LSB for reference voltage below 1.1V when V_{CC} is above 3.0V.

20LSB for ambient temperature below 0°C and reference voltage below 1.3V.

In unsigned mode, the INL error cannot be guaranteed, and this mode should not be used.

Problem fix/Workaround

None, avoid using the ADC in the above configurations in order to prevent increased INL error. Use the ADC in signed mode also for single ended measurements.

5. **ADC gain stage output range is limited to 2.4V**

   The amplified output of the ADC gain stage will never go above 2.4V, hence the differential input will only give correct output when below 2.4V/gain. For the available gain settings, this gives a differential input range of:

   - 1× gain: 2.4 V
   - 2× gain: 1.2 V
   - 4× gain: 0.6 V
   - 8× gain: 300 mV
   - 16× gain: 150 mV
   - 32× gain: 75 mV
   - 64× gain: 38 mV

   Problem fix/Workaround

   Keep the amplified voltage output from the ADC gain stage below 2.4V in order to get a correct result, or keep ADC voltage reference below 2.4V.

6. **ADC Event on compare match non-functional**

   ADC signalling event will be given at every conversion complete even if Interrupt mode (INTMODE) is set to BELOW or ABOVE.

   Problem fix/Workaround

   Enable and use interrupt on compare match when using the compare function.

7. **ADC propagation delay is not correct when 8× – 64× gain is used**

   The propagation delay will increase by only one ADC clock cycle for all gain settings.

   Problem fix/Workaround

   None.

8. **Bandgap measurement with the ADC is non-functional when V_{CC} is below 2.7V**

   The ADC can not be used to do bandgap measurements when V_{CC} is below 2.7V.

   Problem fix/Workaround

   None.

9. **Accuracy lost on first three samples after switching input to ADC gain stage**

   Due to memory effect in the ADC gain stage, the first three samples after changing input channel must be disregarded to achieve 12-bit accuracy.

   Problem fix/Workaround

   Run three ADC conversions and discard these results after changing input channels to ADC gain stage.

10. Configuration of PGM and CWCM not as described in XMEGA D Manual

Enabling Common Waveform Channel Mode will enable Pattern generation mode (PGM), but not Common Waveform Channel Mode.

Enabling Pattern Generation Mode (PGM) and not Common Waveform Channel Mode (CWCM) will enable both Pattern Generation Mode and Common Waveform Channel Mode.

Problem fix/Workaround

Table 34-2. Configure PWM and CWCM according to this table:

PGM	CWCM	Description
0	0	PGM and CWCM disabled
0	1	PGM enabled
1	0	PGM and CWCM enabled
1	1	PGM enabled

11. PWM is not restarted properly after a fault in cycle-by-cycle mode

When the AWeX fault restore mode is set to cycle-by-cycle, the waveform output will not return to normal operation at first update after fault condition is no longer present.

Problem fix/Workaround

Do a write to any AWeX I/O register to re-enable the output.

12. BOD will be enabled after any reset

If any reset source goes active, the BOD will be enabled and keep the device in reset if the V_{CC} voltage is below the programmed BOD level. During Power-On Reset, reset will not be released until V_{CC} is above the programmed BOD level even if the BOD is disabled.

Problem fix/Workaround

Do not set the BOD level higher than V_{CC} even if the BOD is not used.

13. EEPROM page buffer always written when NVM DATA0 is written

If the EEPROM is memory mapped, writing to NVM DATA0 will corrupt data in the EEPROM page buffer.

Problem fix/Workaround

Before writing to NVM DATA0, for example when doing software CRC or flash page buffer write, check if EEPROM page buffer active loading flag (EELOAD) is set. Do not write NVM DATA0 when EELOAD is set.

14. Pending full asynchronous pin change interrupts will not wake the device

Any full asynchronous pin-change Interrupt from pin 2, on any port, that is pending when the sleep instruction is executed, will be ignored until the device is woken from another source or the source triggers again. This applies when entering all sleep modes where the System Clock is stopped.

Problem fix/Workaround

None.

15. Pin configuration does not affect Analog Comparator output

The Output/Pull and inverted pin configuration does not affect the Analog Comparator output.

Problem fix/Workaround

None for Output/Pull configuration.

For inverted I/O, configure the Analog Comparator to give an inverted result (that is, connect positive input to the negative AC input and vice versa), or use and external inverter to change polarity of Analog Comparator output.

16. NMI Flag for Crystal Oscillator Failure automatically cleared

NMI flag for Crystal Oscillator Failure (XOSCFDIF) will be automatically cleared when executing the NMI interrupt handler.

Problem fix/Workaround

This device revision has only one NMI interrupt source, so checking the interrupt source in software is not required.

17. Writing EEPROM or Flash while reading any of them will not work

The EEPROM and Flash cannot be written while reading EEPROM or Flash, or while executing code in Active mode.

Problem fix/Workaround

Enter IDLE sleep mode within 2.5µs (five 2MHz clock cycles and 80 32MHz clock cycles) after starting an EEPROM or flash write operation. Wake-up source must either be EEPROM ready or NVM ready interrupt. Alternatively set up a Timer/Counter to give an overflow interrupt 7ms after the erase or write operation has started, or 13ms after atomic erase-and-write operation has started, and then enter IDLE sleep mode.

18. Crystal start-up time required after power-save even if crystal is source for RTC

Even if 32.768kHz crystal is used for RTC during sleep, the clock from the crystal will not be ready for the system before the specified start-up time. See “XOSCSEL[3:0]: Crystal Oscillator Selection” in XMEGA D Manual. If BOD is used in active mode, the BOD will be on during this period (0.5s).

Problem fix/Workaround

If faster start-up is required, go to sleep with internal oscillator as system clock.

19. RTC Counter value not correctly read after sleep

If the RTC is set to wake up the device on RTC Overflow and bit 0 of RTC CNT is identical to bit 0 of RTC PER as the device is entering sleep, the value in the RTC count register can not be read correctly within the first prescaled RTC clock cycle after wakeup. The value read will be the same as the value in the register when entering sleep.

The same applies if RTC Compare Match is used as wake-up source.

Problem fix/Workaround

Wait at least one prescaled RTC clock cycle before reading the RTC CNT value.

20. Pending asynchronous RTC-interrupts will not wake up device

Asynchronous Interrupts from the Real-Time-Counter that is pending when the sleep instruction is executed, will be ignored until the device is woken from another source or the source triggers again.

Problem fix/Workaround

None.

21. TWI Transmit collision flag not cleared on repeated start

The TWI transmit collision flag should be automatically cleared on start and repeated start, but is only cleared on start.

Problem fix/Workaround

Clear the flag in software after address interrupt.

22. Clearing TWI Stop Interrupt Flag may lock the bus

If software clears the STOP Interrupt Flag (APIF) on the same Peripheral Clock cycle as the hardware sets this flag due to a new address received, CLKHOLD is not cleared and the SCL line is not released. This will lock the bus.

Problem fix/Workaround

Check if the bus state is IDLE. If this is the case, it is safe to clear APIF. If the bus state is not IDLE, wait for the SCL pin to be low before clearing APIF.

Code:

```
/* Only clear the interrupt flag if within a "safe zone". */
while ( /* Bus not IDLE: */
       ((COMMS_TWI.MASTER.STATUS & TWI_MASTER_BUSSTATE_gm) !=
         TWI_MASTER_BUSSTATE_IDLE_gc)) &&
         /* SCL not held by slave: */
         !(COMMS_TWI.SLAVE.STATUS & TWI_SLAVE_CLKHOLD_bm)
      )
{
    /* Ensure that the SCL line is low */
    if ( !(COMMS_PORT.IN & PIN1_bm) )
        if ( !(COMMS_PORT.IN & PIN1_bm) )
            break;
}
/* Check for an pending address match interrupt */
if ( !(COMMS_TWI.SLAVE.STATUS & TWI_SLAVE_CLKHOLD_bm) )
{
    /* Safely clear interrupt flag */
    COMMS_TWI.SLAVE.STATUS |= (uint8_t)TWI_SLAVE_APIF_bm;
}
```

23. TWI START condition at bus timeout will cause transaction to be dropped

If Bus Timeout is enabled and a timeout occurs on the same Peripheral Clock cycle as a START is detected, the transaction will be dropped.

Problem fix/Workaround

None.

24. TWI Data Interrupt Flag erroneously read as set

When issuing the TWI slave response command CMD=0b11, it takes one Peripheral Clock cycle to clear the data interrupt flag (DIF). A read of DIF directly after issuing the command will show the DIF still set.

Problem fix/Workaround

Add one NOP instruction before checking DIF.

25. WDR instruction inside closed window will not issue reset

When a WDR instruction is execute within one ULP clock cycle after updating the window control register, the counter can be cleared without giving a system reset.

Problem fix/Workaround

Wait at least one ULP clock cycle before executing a WDR instruction.

26. Non available functions and options

The below function and options are not available. Writing to any registers or fuse to try and enable or configure these functions or options will have no effect, and will be as writing to a reserved address location.

- TWIE, the TWI module on PORTE
- TWI SDAHOLD option in the TWI CTRL register is one bit
- CRC generator module
- ADC 1/2× gain option, and this configuration option in the GAIN bits in the ADC Channel CTRL register
- ADC VCC/2 reference option and this configuration option in the REFSEL bits on the ADC REFCTRL register
- ADC option to use internal Gnd as negative input in differential measurements and this configuration option in the MUXNEG bits in the ADC Channel MUXCTRL register
- ADC channel scan and the ADC SCAN register
- ADC current limitation option, and the CURRLIMIT bits in the ADC CTRLB register
- ADC impedance mode selection for the gain stage, and the IMPMODE bit in the ADC CTRLB register
- Timer/Counter 2 and the SPLITMODE configuration option in the BYTEM bits in the Timer/Counter 0 CTRLE register
- Analog Comparator (AC) current output option, and the AC CURRCTRL and CURRCALIB registers
- PORT remap functions with alternate pin locations for Timer/Counter output compare channels, USART0 and SPI, and the PORT REMAP register
- PORT RTC clock output option and the RTCOUT bit in the PORT CLKEVOUT register
- PORT remap functions with alternate pin locations for the clock and event output, and the CLKEVPIN bit in the PORT CLKEVOUT register.
- TOSC alternate pin locations, and TOSCSEL bit in FUSEBYTE2
- Real Time Counter clock source options of external clock from TOSC1, and 32.768kHz from TOSC, and 32.768kHz from the 32.768kHz internal oscillator, and these configuration options in the RTCSRC bits in the Clock RTCTRL register
- PLL divide by two option, and the PLLDIV bit in the Clock PLLCTRL register

- PLL lock detection failure function and the PLLDIF and PLLFDEN bits in the Clock XOSCFAIL register
- The high drive option for external crystal and the XOSCPWR bit on the Oscillator XOSCCTRL register
- The option to enable sequential startup of the analog modules and the ANAINIT register in MCU Control memory

Problem fix/Workaround

None.

34.1.9 Rev. A

Not sampled.

34.2 Atmel ATxmega128D3

34.2.1 Rev. J

- AC system status flags are only valid if AC-system is enabled.

1. AC system status flags are only valid if AC-system is enabled

The status flags for the ac-output are updated even though the AC is not enabled which is invalid. Also, it is not possible to clear the AC interrupt flags without enabling either of the Analog comparators.

Problem fix/Workaround

Software should clear the AC system flags once, after enabling the AC system before using the AC system status flags.

34.2.2 Rev. I

Not sampled.

34.2.3 Rev. H

Not sampled.

34.2.4 Rev. G

Not sampled.

34.2.5 Rev. F

Not sampled.

34.2.6 Rev. E

- Bandgap voltage input for the ACs can not be changed when used for both ACs simultaneously
- V_{CC} voltage scaler for AC is non-linear
- ADC gain stage cannot be used for single conversion
- ADC has increased INL error for some operating conditions
- ADC gain stage output range is limited to 2.4V
- ADC Event on compare match non-functional
- ADC propagation delay is not correct when 8× – 64× gain is used
- Bandgap measurement with the ADC is non-functional when V_{CC} is below 2.7V
- Accuracy lost on first three samples after switching input to ADC gain stage
- Configuration of PGM and CWCM not as described in XMEGA D Manual
- PWM is not restarted properly after a fault in cycle-by-cycle mode
- BOD will be enabled at any reset
- EEPROM page buffer always written when NVM DATA0 is written
- Pending full asynchronous pin change interrupts will not wake the device
- Pin configuration does not affect Analog Comparator Output
- NMI Flag for Crystal Oscillator Failure automatically cleared
- Crystal start-up time required after power-save even if crystal is source for RTC
- RTC Counter value not correctly read after sleep
- Pending asynchronous RTC-interrupts will not wake up device
- TWI Transmit collision flag not cleared on repeated start

- Clearing TWI Stop Interrupt Flag may lock the bus
- TWI START condition at bus timeout will cause transaction to be dropped
- TWI Data Interrupt Flag (DIF) erroneously read as set
- WDR instruction inside closed window will not issue reset
- Non available functions and options

1. Bandgap voltage input for the ACs cannot be changed when used for both ACs simultaneously

If the Bandgap voltage is selected as input for one Analog Comparator (AC) and then selected/deselected as input for another AC, the first comparator will be affected for up to 1µs and could potentially give a wrong comparison result.

Problem fix/Workaround

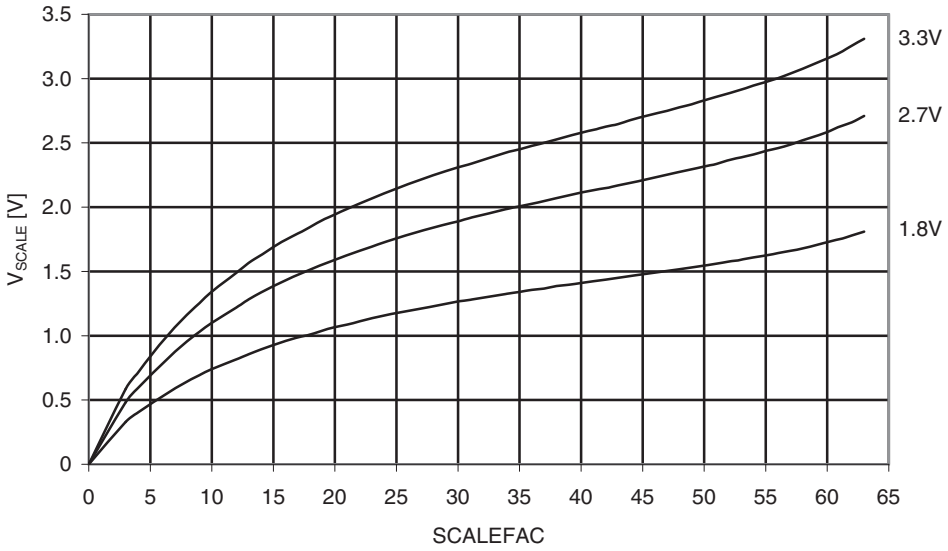
If the Bandgap is required for both ACs simultaneously, configure the input selection for both ACs before enabling any of them.

2. VCC voltage scaler for AC is non-linear

The 6-bit V_{CC} voltage scaler in the Analog Comparators is non-linear.

Figure 34-3. Analog comparator voltage scaler vs. scalefac.

T = 25°C.



Problem fix/Workaround

Use external voltage input for the analog comparator if accurate voltage levels are needed

3. ADC gain stage cannot be used for single conversion

The ADC gain stage will not output correct result for single conversion that is triggered and started from software or event system.

Problem fix/Workaround

When the gain stage is used, the ADC must be set in free running mode for correct results.

4. **ADC has increased INL error for some operating conditions**

Some ADC configurations or operating condition will result in increased INL error.

In signed mode INL is increased to:

6LSB for sample rates above 130ksps, and up to 8LSB for 200ksps sample rate.

6LSB for reference voltage below 1.1V when V_{CC} is above 3.0V.

20LSB for ambient temperature below 0°C and reference voltage below 1.3V.

In unsigned mode, the INL error cannot be guaranteed, and this mode should not be used.

Problem fix/Workaround

None, avoid using the ADC in the above configurations in order to prevent increased INL error. Use the ADC in signed mode also for single ended measurements.

5. **ADC gain stage output range is limited to 2.4V**

The amplified output of the ADC gain stage will never go above 2.4V, hence the differential input will only give correct output when below 2.4V/gain. For the available gain settings, this gives a differential input range of:

- 1× gain: 2.4 V
- 2× gain: 1.2 V
- 4× gain: 0.6 V
- 8× gain: 300 mV
- 16× gain: 150 mV
- 32× gain: 75 mV
- 64× gain: 38 mV

Problem fix/Workaround

Keep the amplified voltage output from the ADC gain stage below 2.4V in order to get a correct result, or keep ADC voltage reference below 2.4V.

6. **ADC Event on compare match non-functional**

ADC signalling event will be given at every conversion complete even if Interrupt mode (INTMODE) is set to BELOW or ABOVE.

Problem fix/Workaround

Enable and use interrupt on compare match when using the compare function.

7. **ADC propagation delay is not correct when 8× – 64× gain is used**

The propagation delay will increase by only one ADC clock cycle for all gain settings.

Problem fix/Workaround

None.

8. **Bandgap measurement with the ADC is non-functional when V_{CC} is below 2.7V**

The ADC can not be used to do bandgap measurements when V_{CC} is below 2.7V.

Problem fix/Workaround

None.

9. Accuracy lost on first three samples after switching input to ADC gain stage

Due to memory effect in the ADC gain stage, the first three samples after changing input channel must be disregarded to achieve 12-bit accuracy.

Problem fix/Workaround

Run three ADC conversions and discard these results after changing input channels to ADC gain stage.

10. Configuration of PGM and CWCM not as described in XMEGA D Manual

Enabling Common Waveform Channel Mode will enable Pattern generation mode (PGM), but not Common Waveform Channel Mode.

Enabling Pattern Generation Mode (PGM) and not Common Waveform Channel Mode (CWCM) will enable both Pattern Generation Mode and Common Waveform Channel Mode.

Problem fix/Workaround

Table 34-3. Configure PWM and CWCM according to this table:

PGM	CWCM	Description
0	0	PGM and CWCM disabled
0	1	PGM enabled
1	0	PGM and CWCM enabled
1	1	PGM enabled

11. PWM is not restarted properly after a fault in cycle-by-cycle mode

When the AWeX fault restore mode is set to cycle-by-cycle, the waveform output will not return to normal operation at first update after fault condition is no longer present.

Problem fix/Workaround

Do a write to any AWeX I/O register to re-enable the output.

12. BOD will be enabled after any reset

If any reset source goes active, the BOD will be enabled and keep the device in reset if the V_{CC} voltage is below the programmed BOD level. During Power-On Reset, reset will not be released until V_{CC} is above the programmed BOD level even if the BOD is disabled.

Problem fix/Workaround

Do not set the BOD level higher than V_{CC} even if the BOD is not used.

13. EEPROM page buffer always written when NVM DATA0 is written

If the EEPROM is memory mapped, writing to NVM DATA0 will corrupt data in the EEPROM page buffer.

Problem fix/Workaround

Before writing to NVM DATA0, for example when doing software CRC or flash page buffer write, check if EEPROM page buffer active loading flag (EELOAD) is set. Do not write NVM DATA0 when EELOAD is set.

14. Pending full asynchronous pin change interrupts will not wake the device

Any full asynchronous pin-change Interrupt from pin 2, on any port, that is pending when the sleep instruction is executed, will be ignored until the device is woken from another source or the source triggers again. This applies when entering all sleep modes where the System Clock is stopped.

Problem fix/Workaround

None.

15. Pin configuration does not affect Analog Comparator output

The Output/Pull and inverted pin configuration does not affect the Analog Comparator output.

Problem fix/Workaround

None for Output/Pull configuration.

For inverted I/O, configure the Analog Comparator to give an inverted result (that is, connect positive input to the negative AC input and vice versa), or use and external inverter to change polarity of Analog Comparator output.

16. NMI Flag for Crystal Oscillator Failure automatically cleared

NMI flag for Crystal Oscillator Failure (XOSCFDIF) will be automatically cleared when executing the NMI interrupt handler.

Problem fix/Workaround

This device revision has only one NMI interrupt source, so checking the interrupt source in software is not required.

17. Crystal start-up time required after power-save even if crystal is source for RTC

Even if 32.768kHz crystal is used for RTC during sleep, the clock from the crystal will not be ready for the system before the specified start-up time. See "XOSCSEL[3:0]: Crystal Oscillator Selection" in XMEGA D Manual. If BOD is used in active mode, the BOD will be on during this period (0.5s).

Problem fix/Workaround

If faster start-up is required, go to sleep with internal oscillator as system clock.

18. RTC Counter value not correctly read after sleep

If the RTC is set to wake up the device on RTC Overflow and bit 0 of RTC CNT is identical to bit 0 of RTC PER as the device is entering sleep, the value in the RTC count register can not be read correctly within the first prescaled RTC clock cycle after wakeup. The value read will be the same as the value in the register when entering sleep.

The same applies if RTC Compare Match is used as wake-up source.

Problem fix/Workaround

Wait at least one prescaled RTC clock cycle before reading the RTC CNT value.

19. Pending asynchronous RTC-interrupts will not wake up device

Asynchronous Interrupts from the Real-Time-Counter that is pending when the sleep instruction is executed, will be ignored until the device is woken from another source or the source triggers again.

Problem fix/Workaround

None.

20. TWI Transmit collision flag not cleared on repeated start

The TWI transmit collision flag should be automatically cleared on start and repeated start, but is only cleared on start.

Problem fix/Workaround

Clear the flag in software after address interrupt.

21. Clearing TWI Stop Interrupt Flag may lock the bus

If software clears the STOP Interrupt Flag (APIF) on the same Peripheral Clock cycle as the hardware sets this flag due to a new address received, CLKHOLD is not cleared and the SCL line is not released. This will lock the bus.

Problem fix/Workaround

Check if the bus state is IDLE. If this is the case, it is safe to clear APIF. If the bus state is not IDLE, wait for the SCL pin to be low before clearing APIF.

Code:

```
/* Only clear the interrupt flag if within a "safe zone". */
while ( /* Bus not IDLE: */
       ((COMMS_TWI.MASTER.STATUS & TWI_MASTER_BUSSTATE_gm) !=
         TWI_MASTER_BUSSTATE_IDLE_gc)) &&
         /* SCL not held by slave: */
         !(COMMS_TWI.SLAVE.STATUS & TWI_SLAVE_CLKHOLD_bm)
      )
{
    /* Ensure that the SCL line is low */
    if ( !(COMMS_PORT.IN & PIN1_bm) )
        if ( !(COMMS_PORT.IN & PIN1_bm) )
            break;
}
/* Check for an pending address match interrupt */
if ( !(COMMS_TWI.SLAVE.STATUS & TWI_SLAVE_CLKHOLD_bm) )
{
    /* Safely clear interrupt flag */
    COMMS_TWI.SLAVE.STATUS |= (uint8_t)TWI_SLAVE_APIF_bm;
}
```

22. TWI START condition at bus timeout will cause transaction to be dropped

If Bus Timeout is enabled and a timeout occurs on the same Peripheral Clock cycle as a START is detected, the transaction will be dropped.

Problem fix/Workaround

None.

23. TWI Data Interrupt Flag erroneously read as set

When issuing the TWI slave response command CMD=0b11, it takes one Peripheral Clock cycle to clear the data interrupt flag (DIF). A read of DIF directly after issuing the command will show the DIF still set.

Problem fix/Workaround

Add one NOP instruction before checking DIF.

24. WDR instruction inside closed window will not issue reset

When a WDR instruction is execute within one ULP clock cycle after updating the window control register, the counter can be cleared without giving a system reset.

Problem fix/Workaround

Wait at least one ULP clock cycle before executing a WDR instruction.

25. Non available functions and options

The below function and options are not available. Writing to any registers or fuse to try and enable or configure these functions or options will have no effect, and will be as writing to a reserved address location.

- TWIE, the TWI module on PORTE
- TWI SDAHOLD option in the TWI CTRL register is one bit
- CRC generator module
- ADC 1/2× gain option, and this configuration option in the GAIN bits in the ADC Channel CTRL register
- ADC VCC/2 reference option and this configuration option in the REFSEL bits on the ADC REFCTRL register
- ADC option to use internal Gnd as negative input in differential measurements and this configuration option in the MUXNEG bits in the ADC Channel MUXCTRL register
- ADC channel scan and the ADC SCAN register
- ADC current limitation option, and the CURRLIMIT bits in the ADC CTRLB register
- ADC impedance mode selection for the gain stage, and the IMPMODE bit in the ADC CTRLB register
- Timer/Counter 2 and the SPLITMODE configuration option in the BYTEM bits in the Timer/Counter 0 CTRLE register
- Analog Comparator (AC) current output option, and the AC CURRCTRL and CURRCALIB registers
- PORT remap functions with alternate pin locations for Timer/Counter output compare channels, USART0 and SPI, and the PORT REMAP register
- PORT RTC clock output option and the RTCOUT bit in the PORT CLKEVOUT register
- PORT remap functions with alternate pin locations for the clock and event output, and the CLKEVPIN bit in the PORT CLKEVOUT register
- TOSC alternate pin locations, and TOSCSEL bit in FUSEBYTE2
- Real Time Counter clock source options of external clock from TOSC1, and 32.768kHz from TOSC, and 32.768kHz from the 32.768kHz internal oscillator, and these configuration options in the RTCSRC bits in the Clock RTCTRL register
- PLL divide by two option, and the PLLDIV bit in the Clock PLLCTRL register
- PLL lock detection failure function and the PLLDIF and PLLFDEN bits in the Clock XOSCFAIL register
- The high drive option for external crystal and the XOSCPWR bit on the Oscillator XOSCCTRL register
- The option to enable sequential startup of the analog modules and the ANAINIT register in MCU Control memory

Problem fix/Workaround

None.

34.2.7 Rev. D

Not sampled.

34.2.8 Rev. C

Not sampled.

34.2.9 Rev. B

- Bandgap voltage input for the ACs can not be changed when used for both ACs simultaneously
- VCC voltage scaler for AC is non-linear
- ADC gain stage cannot be used for single conversion
- ADC has increased INL error for some operating conditions
- ADC gain stage output range is limited to 2.4V
- ADC Event on compare match non-functional
- ADC propagation delay is not correct when 8× – 64× gain is used
- Bandgap measurement with the ADC is non-functional when VCC is below 2.7V
- Accuracy lost on first three samples after switching input to ADC gain stage
- Configuration of PGM and CWCM not as described in XMEGA D Manual
- PWM is not restarted properly after a fault in cycle-by-cycle mode
- BOD will be enabled at any reset
- EEPROM page buffer always written when NVM DATA0 is written
- Pending full asynchronous pin change interrupts will not wake the device
- Pin configuration does not affect Analog Comparator Output
- NMI Flag for Crystal Oscillator Failure automatically cleared
- Writing EEPROM or Flash while reading any of them will not work
- Crystal start-up time required after power-save even if crystal is source for RTC
- RTC Counter value not correctly read after sleep
- Pending asynchronous RTC-interrupts will not wake up device
- TWI Transmit collision flag not cleared on repeated start
- Clearing TWI Stop Interrupt Flag may lock the bus
- TWI START condition at bus timeout will cause transaction to be dropped
- TWI Data Interrupt Flag (DIF) erroneously read as set
- WDR instruction inside closed window will not issue reset
- Non available functions and options

1. Bandgap voltage input for the ACs cannot be changed when used for both ACs simultaneously

If the Bandgap voltage is selected as input for one Analog Comparator (AC) and then selected/deselected as input for another AC, the first comparator will be affected for up to 1µs and could potentially give a wrong comparison result.

Problem fix/Workaround

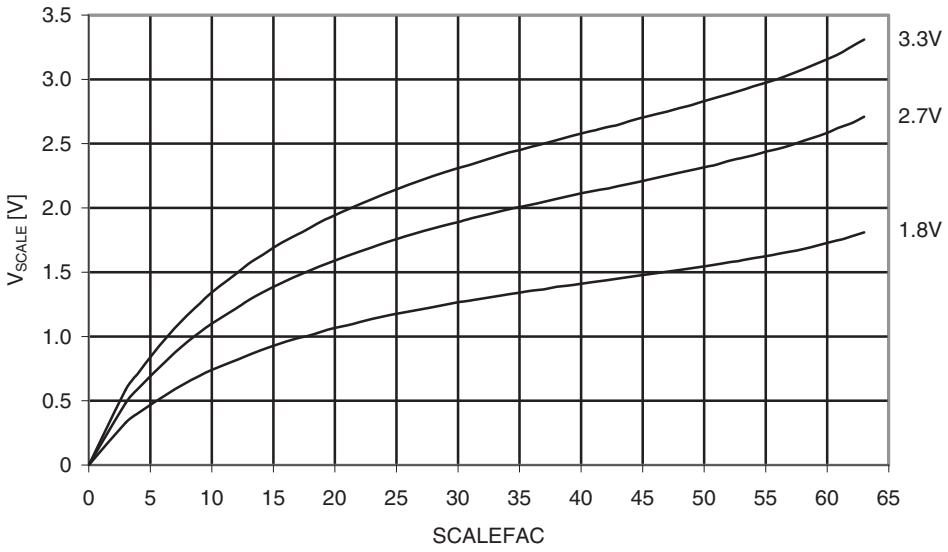
If the Bandgap is required for both ACs simultaneously, configure the input selection for both ACs before enabling any of them.

2. VCC voltage scaler for AC is non-linear

The 6-bit V_{CC} voltage scaler in the Analog Comparators is non-linear.

Figure 34-4. Analog comparator voltage scaler vs. scalefac.

T = 25°C.



Problem fix/Workaround

Use external voltage input for the analog comparator if accurate voltage levels are needed

3. ADC gain stage cannot be used for single conversion

The ADC gain stage will not output correct result for single conversion that is triggered and started from software or event system.

Problem fix/Workaround

When the gain stage is used, the ADC must be set in free running mode for correct results.

4. ADC has increased INL error for some operating conditions

Some ADC configurations or operating condition will result in increased INL error.

In signed mode INL is increased to:

6LSB for sample rates above 130ksps, and up to 8LSB for 200ksps sample rate.

6LSB for reference voltage below 1.1V when V_{CC} is above 3.0V.

20LSB for ambient temperature below 0°C and reference voltage below 1.3V.

In unsigned mode, the INL error cannot be guaranteed, and this mode should not be used.

Problem fix/Workaround

None, avoid using the ADC in the above configurations in order to prevent increased INL error. Use the ADC in signed mode also for single ended measurements.

5. **ADC gain stage output range is limited to 2.4V**

The amplified output of the ADC gain stage will never go above 2.4V, hence the differential input will only give correct output when below 2.4V/gain. For the available gain settings, this gives a differential input range of:

—	1×	gain:	2.4	V
—	2×	gain:	1.2	V
—	4×	gain:	0.6	V
—	8×	gain:	300	mV
—	16×	gain:	150	mV
—	32×	gain:	75	mV
—	64×	gain:	38	mV

Problem fix/Workaround

Keep the amplified voltage output from the ADC gain stage below 2.4V in order to get a correct result, or keep ADC voltage reference below 2.4V.

6. **ADC Event on compare match non-functional**

ADC signalling event will be given at every conversion complete even if Interrupt mode (INTMODE) is set to BELOW or ABOVE.

Problem fix/Workaround

Enable and use interrupt on compare match when using the compare function.

7. **ADC propagation delay is not correct when 8× – 64× gain is used**

The propagation delay will increase by only one ADC clock cycle for all gain settings.

Problem fix/Workaround

None.

8. **Bandgap measurement with the ADC is non-functional when V_{CC} is below 2.7V**

The ADC can not be used to do bandgap measurements when V_{CC} is below 2.7V.

Problem fix/Workaround

None.

9. **Accuracy lost on first three samples after switching input to ADC gain stage**

Due to memory effect in the ADC gain stage, the first three samples after changing input channel must be disregarded to achieve 12-bit accuracy.

Problem fix/Workaround

Run three ADC conversions and discard these results after changing input channels to ADC gain stage.

10. Configuration of PGM and CWCM not as described in XMEGA D Manual

Enabling Common Waveform Channel Mode will enable Pattern generation mode (PGM), but not Common Waveform Channel Mode.

Enabling Pattern Generation Mode (PGM) and not Common Waveform Channel Mode (CWCM) will enable both Pattern Generation Mode and Common Waveform Channel Mode.

Problem fix/Workaround

Table 34-4. Configure PWM and CWCM according to this table:

PGM	CWCM	Description
0	0	PGM and CWCM disabled
0	1	PGM enabled
1	0	PGM and CWCM enabled
1	1	PGM enabled

11. PWM is not restarted properly after a fault in cycle-by-cycle mode

When the AWeX fault restore mode is set to cycle-by-cycle, the waveform output will not return to normal operation at first update after fault condition is no longer present.

Problem fix/Workaround

Do a write to any AWeX I/O register to re-enable the output.

12. BOD will be enabled after any reset

If any reset source goes active, the BOD will be enabled and keep the device in reset if the V_{CC} voltage is below the programmed BOD level. During Power-On Reset, reset will not be released until V_{CC} is above the programmed BOD level even if the BOD is disabled.

Problem fix/Workaround

Do not set the BOD level higher than V_{CC} even if the BOD is not used.

13. EEPROM page buffer always written when NVM DATA0 is written

If the EEPROM is memory mapped, writing to NVM DATA0 will corrupt data in the EEPROM page buffer.

Problem fix/Workaround

Before writing to NVM DATA0, for example when doing software CRC or flash page buffer write, check if EEPROM page buffer active loading flag (EELOAD) is set. Do not write NVM DATA0 when EELOAD is set.

14. Pending full asynchronous pin change interrupts will not wake the device

Any full asynchronous pin-change Interrupt from pin 2, on any port, that is pending when the sleep instruction is executed, will be ignored until the device is woken from another source or the source triggers again. This applies when entering all sleep modes where the System Clock is stopped.

Problem fix/Workaround

None.

15. Pin configuration does not affect Analog Comparator output

The Output/Pull and inverted pin configuration does not affect the Analog Comparator output.

Problem fix/Workaround

None for Output/Pull configuration.

For inverted I/O, configure the Analog Comparator to give an inverted result (that is, connect positive input to the negative AC input and vice versa), or use and external inverter to change polarity of Analog Comparator output.

16. NMI Flag for Crystal Oscillator Failure automatically cleared

NMI flag for Crystal Oscillator Failure (XOSCFDIF) will be automatically cleared when executing the NMI interrupt handler.

Problem fix/Workaround

This device revision has only one NMI interrupt source, so checking the interrupt source in software is not required.

17. Writing EEPROM or Flash while reading any of them will not work

The EEPROM and Flash cannot be written while reading EEPROM or Flash, or while executing code in Active mode.

Problem fix/Workaround

Enter IDLE sleep mode within 2.5µs (five 2MHz clock cycles and 80 32MHz clock cycles) after starting an EEPROM or flash write operation. Wake-up source must either be EEPROM ready or NVM ready interrupt. Alternatively set up a Timer/Counter to give an overflow interrupt 7ms after the erase or write operation has started, or 13ms after atomic erase-and-write operation has started, and then enter IDLE sleep mode.

18. Crystal start-up time required after power-save even if crystal is source for RTC

Even if 32.768kHz crystal is used for RTC during sleep, the clock from the crystal will not be ready for the system before the specified start-up time. See "XOSCSEL[3:0]: Crystal Oscillator Selection" in XMEGA D Manual. If BOD is used in active mode, the BOD will be on during this period (0.5s).

Problem fix/Workaround

If faster start-up is required, go to sleep with internal oscillator as system clock.

19. RTC Counter value not correctly read after sleep

If the RTC is set to wake up the device on RTC Overflow and bit 0 of RTC CNT is identical to bit 0 of RTC PER as the device is entering sleep, the value in the RTC count register can not be read correctly within the first prescaled RTC clock cycle after wakeup. The value read will be the same as the value in the register when entering sleep.

The same applies if RTC Compare Match is used as wake-up source.

Problem fix/Workaround

Wait at least one prescaled RTC clock cycle before reading the RTC CNT value.

20. Pending asynchronous RTC-interrupts will not wake up device

Asynchronous Interrupts from the Real-Time-Counter that is pending when the sleep instruction is executed, will be ignored until the device is woken from another source or the source triggers again.

Problem fix/Workaround

None.

21. TWI Transmit collision flag not cleared on repeated start

The TWI transmit collision flag should be automatically cleared on start and repeated start, but is only cleared on start.

Problem fix/Workaround

Clear the flag in software after address interrupt.

22. Clearing TWI Stop Interrupt Flag may lock the bus

If software clears the STOP Interrupt Flag (APIF) on the same Peripheral Clock cycle as the hardware sets this flag due to a new address received, CLKHOLD is not cleared and the SCL line is not released. This will lock the bus.

Problem fix/Workaround

Check if the bus state is IDLE. If this is the case, it is safe to clear APIF. If the bus state is not IDLE, wait for the SCL pin to be low before clearing APIF.

Code:

```
/* Only clear the interrupt flag if within a "safe zone". */
while ( /* Bus not IDLE: */
       ((COMMS_TWI.MASTER.STATUS & TWI_MASTER_BUSSTATE_gm) !=
         TWI_MASTER_BUSSTATE_IDLE_gc)) &&
         /* SCL not held by slave: */
         !(COMMS_TWI.SLAVE.STATUS & TWI_SLAVE_CLKHOLD_bm)
      )
{
    /* Ensure that the SCL line is low */
    if ( !(COMMS_PORT.IN & PIN1_bm) )
        if ( !(COMMS_PORT.IN & PIN1_bm) )
            break;
}
/* Check for an pending address match interrupt */
if ( !(COMMS_TWI.SLAVE.STATUS & TWI_SLAVE_CLKHOLD_bm) )
{
    /* Safely clear interrupt flag */
    COMMS_TWI.SLAVE.STATUS |= (uint8_t)TWI_SLAVE_APIF_bm;
}
```

23. TWI START condition at bus timeout will cause transaction to be dropped

If Bus Timeout is enabled and a timeout occurs on the same Peripheral Clock cycle as a START is detected, the transaction will be dropped.

Problem fix/Workaround

None.

24. TWI Data Interrupt Flag erroneously read as set

When issuing the TWI slave response command CMD=0b11, it takes one Peripheral Clock cycle to clear the data interrupt flag (DIF). A read of DIF directly after issuing the command will show the DIF still set.

Problem fix/Workaround

Add one NOP instruction before checking DIF.

25. WDR instruction inside closed window will not issue reset

When a WDR instruction is execute within one ULP clock cycle after updating the window control register, the counter can be cleared without giving a system reset.

Problem fix/Workaround

Wait at least one ULP clock cycle before executing a WDR instruction.

26. Non available functions and options

The below function and options are not available. Writing to any registers or fuse to try and enable or configure these functions or options will have no effect, and will be as writing to a reserved address location.

- TWIE, the TWI module on PORTE
- TWI SDAHOLD option in the TWI CTRL register is one bit
- CRC generator module
- ADC 1/2× gain option, and this configuration option in the GAIN bits in the ADC Channel CTRL register
- ADC VCC/2 reference option and this configuration option in the REFSEL bits on the ADC REFCTRL register
- ADC option to use internal Gnd as negative input in differential measurements and this configuration option in the MUXNEG bits in the ADC Channel MUXCTRL register
- ADC channel scan and the ADC SCAN register
- ADC current limitation option, and the CURRLIMIT bits in the ADC CTRLB register
- ADC impedance mode selection for the gain stage, and the IMPMODE bit in the ADC CTRLB register
- Timer/Counter 2 and the SPLITMODE configuration option in the BYTEM bits in the Timer/Counter 0 CTRLE register
- Analog Comparator (AC) current output option, and the AC CURRCTRL and CURRCALIB registers
- PORT remap functions with alternate pin locations for Timer/Counter output compare channels, USART0 and SPI, and the PORT REMAP register
- PORT RTC clock output option and the RTCOUT bit in the PORT CLKEVOUT register
- PORT remap functions with alternate pin locations for the clock and event output, and the CLKEVPIN bit in the PORT CLKEVOUT register.
- TOSC alternate pin locations, and TOSCSEL bit in FUSEBYTE2
- Real Time Counter clock source options of external clock from TOSC1, and 32.768kHz from TOSC, and 32.768kHz from the 32.768kHz internal oscillator, and these configuration options in the RTCSRC bits in the Clock RTCTRL register
- PLL divide by two option, and the PLLDIV bit in the Clock PLLCTRL register

- PLL lock detection failure function and the PLLDIF and PLLFDEN bits in the Clock XOSCFAIL register
- The high drive option for external crystal and the XOSCPWR bit on the Oscillator XOSCCTRL register
- The option to enable sequential startup of the analog modules and the ANAINIT register in MCU Control memory

Problem fix/Workaround

None.

34.2.10 Rev. A

Not sampled.

34.3 Atmel ATxmega192D3

34.3.1 Rev. I

- AC system status flags are only valid if AC-system is enabled.

1. AC system status flags are only valid if AC-system is enabled

The status flags for the ac-output are updated even though the AC is not enabled which is invalid. Also, it is not possible to clear the AC interrupt flags without enabling either of the Analog comparators.

Problem fix/Workaround

Software should clear the AC system flags once, after enabling the AC system before using the AC system status flags.

34.3.2 Rev. H

Not sampled.

34.3.3 Rev. G

Not sampled.

34.3.4 Rev. F

Not sampled.

34.3.5 Rev. E

- Bandgap voltage input for the ACs can not be changed when used for both ACs simultaneously
- V_{CC} voltage scaler for AC is non-linear
- ADC gain stage cannot be used for single conversion
- ADC has increased INL error for some operating conditions
- ADC gain stage output range is limited to 2.4V
- ADC Event on compare match non-functional
- ADC propagation delay is not correct when 8× – 64× gain is used
- Bandgap measurement with the ADC is non-functional when V_{CC} is below 2.7V
- Accuracy lost on first three samples after switching input to ADC gain stage
- Configuration of PGM and CWCM not as described in XMEGA D Manual
- PWM is not restarted properly after a fault in cycle-by-cycle mode
- BOD will be enabled at any reset
- EEPROM page buffer always written when NVM DATA0 is written
- Pending full asynchronous pin change interrupts will not wake the device
- Pin configuration does not affect Analog Comparator Output
- NMI Flag for Crystal Oscillator Failure automatically cleared
- Crystal start-up time required after power-save even if crystal is source for RTC
- RTC Counter value not correctly read after sleep
- Pending asynchronous RTC-interrupts will not wake up device
- TWI Transmit collision flag not cleared on repeated start
- Clearing TWI Stop Interrupt Flag may lock the bus
- TWI START condition at bus timeout will cause transaction to be dropped
- TWI Data Interrupt Flag (DIF) erroneously read as set

- WDR instruction inside closed window will not issue reset
- Non available functions and options

1. Bandgap voltage input for the ACs cannot be changed when used for both ACs simultaneously

If the Bandgap voltage is selected as input for one Analog Comparator (AC) and then selected/deselected as input for another AC, the first comparator will be affected for up to 1µs and could potentially give a wrong comparison result.

Problem fix/Workaround

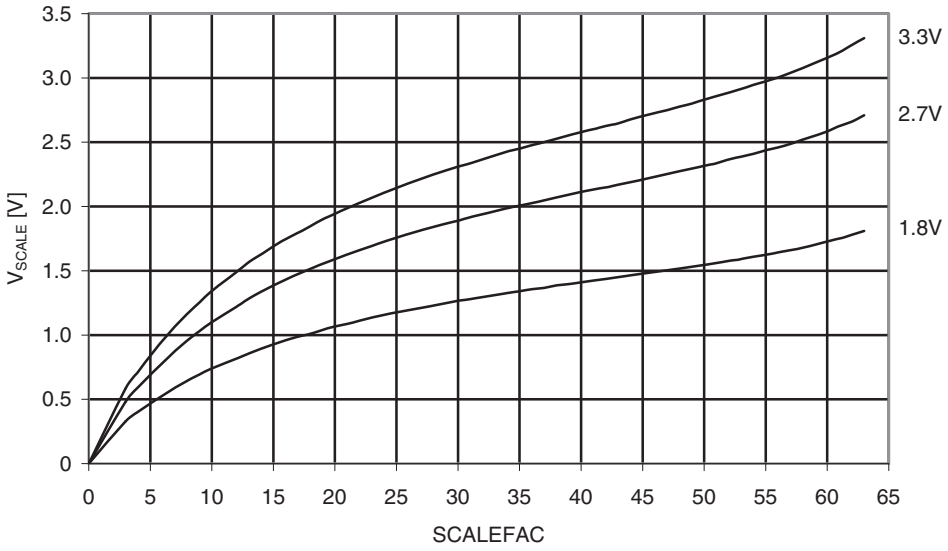
If the Bandgap is required for both ACs simultaneously, configure the input selection for both ACs before enabling any of them.

2. VCC voltage scaler for AC is non-linear

The 6-bit VCC voltage scaler in the Analog Comparators is non-linear.

Figure 34-5. Analog comparator voltage scaler vs. scalefac.

T = 25°C.



Problem fix/Workaround

Use external voltage input for the analog comparator if accurate voltage levels are needed

3. ADC gain stage cannot be used for single conversion

The ADC gain stage will not output correct result for single conversion that is triggered and started from software or event system.

Problem fix/Workaround

When the gain stage is used, the ADC must be set in free running mode for correct results.

4. ADC has increased INL error for some operating conditions

Some ADC configurations or operating condition will result in increased INL error.

In signed mode INL is increased to:

6LSB for sample rates above 130ksps, and up to 8LSB for 200ksps sample rate.

6LSB for reference voltage below 1.1V when V_{CC} is above 3.0V.

20LSB for ambient temperature below 0°C and reference voltage below 1.3V.

In unsigned mode, the INL error cannot be guaranteed, and this mode should not be used.

Problem fix/Workaround

None, avoid using the ADC in the above configurations in order to prevent increased INL error. Use the ADC in signed mode also for single ended measurements.

5. ADC gain stage output range is limited to 2.4V

The amplified output of the ADC gain stage will never go above 2.4V, hence the differential input will only give correct output when below 2.4V/gain. For the available gain settings, this gives a differential input range of:

—	1×	gain:	2.4	V
—	2×	gain:	1.2	V
—	4×	gain:	0.6	V
—	8×	gain:	300	mV
—	16×	gain:	150	mV
—	32×	gain:	75	mV
—	64×	gain:	38	mV

Problem fix/Workaround

Keep the amplified voltage output from the ADC gain stage below 2.4V in order to get a correct result, or keep ADC voltage reference below 2.4V.

6. ADC Event on compare match non-functional

ADC signalling event will be given at every conversion complete even if Interrupt mode (INTMODE) is set to BELOW or ABOVE.

Problem fix/Workaround

Enable and use interrupt on compare match when using the compare function.

7. ADC propagation delay is not correct when 8× – 64× gain is used

The propagation delay will increase by only one ADC clock cycle for all gain settings.

Problem fix/Workaround

None.

8. Bandgap measurement with the ADC is non-functional when V_{CC} is below 2.7V

The ADC can not be used to do bandgap measurements when V_{CC} is below 2.7V.

Problem fix/Workaround

None.

9. Accuracy lost on first three samples after switching input to ADC gain stage

Due to memory effect in the ADC gain stage, the first three samples after changing input channel must be disregarded to achieve 12-bit accuracy.

Problem fix/Workaround

Run three ADC conversions and discard these results after changing input channels to ADC gain stage.

10. Configuration of PGM and CWCM not as described in XMEGA D Manual

Enabling Common Waveform Channel Mode will enable Pattern generation mode (PGM), but not Common Waveform Channel Mode.

Enabling Pattern Generation Mode (PGM) and not Common Waveform Channel Mode (CWCM) will enable both Pattern Generation Mode and Common Waveform Channel Mode.

Problem fix/Workaround

Table 34-5. Configure PWM and CWCM according to this table:

PGM	CWCM	Description
0	0	PGM and CWCM disabled
0	1	PGM enabled
1	0	PGM and CWCM enabled
1	1	PGM enabled

11. PWM is not restarted properly after a fault in cycle-by-cycle mode

When the AWeX fault restore mode is set to cycle-by-cycle, the waveform output will not return to normal operation at first update after fault condition is no longer present.

Problem fix/Workaround

Do a write to any AWeX I/O register to re-enable the output.

12. BOD will be enabled after any reset

If any reset source goes active, the BOD will be enabled and keep the device in reset if the V_{CC} voltage is below the programmed BOD level. During Power-On Reset, reset will not be released until V_{CC} is above the programmed BOD level even if the BOD is disabled.

Problem fix/Workaround

Do not set the BOD level higher than V_{CC} even if the BOD is not used.

13. EEPROM page buffer always written when NVM DATA0 is written

If the EEPROM is memory mapped, writing to NVM DATA0 will corrupt data in the EEPROM page buffer.

Problem fix/Workaround

Before writing to NVM DATA0, for example when doing software CRC or flash page buffer write, check if EEPROM page buffer active loading flag (EELOAD) is set. Do not write NVM DATA0 when EELOAD is set.

14. Pending full asynchronous pin change interrupts will not wake the device

Any full asynchronous pin-change Interrupt from pin 2, on any port, that is pending when the sleep instruction is executed, will be ignored until the device is woken from another source or the source triggers again. This applies when entering all sleep modes where the System Clock is stopped.

Problem fix/Workaround

None.

15. Pin configuration does not affect Analog Comparator output

The Output/Pull and inverted pin configuration does not affect the Analog Comparator output.

Problem fix/Workaround

None for Output/Pull configuration.

For inverted I/O, configure the Analog Comparator to give an inverted result (that is, connect positive input to the negative AC input and vice versa), or use and external inverter to change polarity of Analog Comparator output.

16. NMI Flag for Crystal Oscillator Failure automatically cleared

NMI flag for Crystal Oscillator Failure (XOSCFDIF) will be automatically cleared when executing the NMI interrupt handler.

Problem fix/Workaround

This device revision has only one NMI interrupt source, so checking the interrupt source in software is not required.

17. Crystal start-up time required after power-save even if crystal is source for RTC

Even if 32.768kHz crystal is used for RTC during sleep, the clock from the crystal will not be ready for the system before the specified start-up time. See "XOSCSEL[3:0]: Crystal Oscillator Selection" in XMEGA D Manual. If BOD is used in active mode, the BOD will be on during this period (0.5s).

Problem fix/Workaround

If faster start-up is required, go to sleep with internal oscillator as system clock.

18. RTC Counter value not correctly read after sleep

If the RTC is set to wake up the device on RTC Overflow and bit 0 of RTC CNT is identical to bit 0 of RTC PER as the device is entering sleep, the value in the RTC count register can not be read correctly within the first prescaled RTC clock cycle after wakeup. The value read will be the same as the value in the register when entering sleep.

The same applies if RTC Compare Match is used as wake-up source.

Problem fix/Workaround

Wait at least one prescaled RTC clock cycle before reading the RTC CNT value.

19. Pending asynchronous RTC-interrupts will not wake up device

Asynchronous Interrupts from the Real-Time-Counter that is pending when the sleep instruction is executed, will be ignored until the device is woken from another source or the source triggers again.

Problem fix/Workaround

None.

20. TWI Transmit collision flag not cleared on repeated start

The TWI transmit collision flag should be automatically cleared on start and repeated start, but is only cleared on start.

Problem fix/Workaround

Clear the flag in software after address interrupt.

21. Clearing TWI Stop Interrupt Flag may lock the bus

If software clears the STOP Interrupt Flag (APIF) on the same Peripheral Clock cycle as the hardware sets this flag due to a new address received, CLKHOLD is not cleared and the SCL line is not released. This will lock the bus.

Problem fix/Workaround

Check if the bus state is IDLE. If this is the case, it is safe to clear APIF. If the bus state is not IDLE, wait for the SCL pin to be low before clearing APIF.

Code:

```
/* Only clear the interrupt flag if within a "safe zone". */
while ( /* Bus not IDLE: */
       ((COMMS_TWI.MASTER.STATUS & TWI_MASTER_BUSSTATE_gm) !=
         TWI_MASTER_BUSSTATE_IDLE_gc)) &&
         /* SCL not held by slave: */
         !(COMMS_TWI.SLAVE.STATUS & TWI_SLAVE_CLKHOLD_bm)
      )
{
    /* Ensure that the SCL line is low */
    if ( !(COMMS_PORT.IN & PIN1_bm) )
        if ( !(COMMS_PORT.IN & PIN1_bm) )
            break;
}
/* Check for an pending address match interrupt */
if ( !(COMMS_TWI.SLAVE.STATUS & TWI_SLAVE_CLKHOLD_bm) )
{
    /* Safely clear interrupt flag */
    COMMS_TWI.SLAVE.STATUS |= (uint8_t)TWI_SLAVE_APIF_bm;
}
```

22. TWI START condition at bus timeout will cause transaction to be dropped

If Bus Timeout is enabled and a timeout occurs on the same Peripheral Clock cycle as a START is detected, the transaction will be dropped.

Problem fix/Workaround

None.

23. TWI Data Interrupt Flag erroneously read as set

When issuing the TWI slave response command CMD=0b11, it takes one Peripheral Clock cycle to clear the data interrupt flag (DIF). A read of DIF directly after issuing the command will show the DIF still set.

Problem fix/Workaround

Add one NOP instruction before checking DIF.

24. WDR instruction inside closed window will not issue reset

When a WDR instruction is execute within one ULP clock cycle after updating the window control register, the counter can be cleared without giving a system reset.

Problem fix/Workaround

Wait at least one ULP clock cycle before executing a WDR instruction.

25. Non available functions and options

The below function and options are not available. Writing to any registers or fuse to try and enable or configure these functions or options will have no effect, and will be as writing to a reserved address location.

- TWIE, the TWI module on PORTE
- TWI SDAHOLD option in the TWI CTRL register is one bit
- CRC generator module
- ADC 1/2× gain option, and this configuration option in the GAIN bits in the ADC Channel CTRL register
- ADC VCC/2 reference option and this configuration option in the REFSEL bits on the ADC REFCTRL register
- ADC option to use internal Gnd as negative input in differential measurements and this configuration option in the MUXNEG bits in the ADC Channel MUXCTRL register
- ADC channel scan and the ADC SCAN register
- ADC current limitation option, and the CURRLIMIT bits in the ADC CTRLB register
- ADC impedance mode selection for the gain stage, and the IMPMODE bit in the ADC CTRLB register
- Timer/Counter 2 and the SPLITMODE configuration option in the BYTEM bits in the Timer/Counter 0 CTRLE register
- Analog Comparator (AC) current output option, and the AC CURRCTRL and CURRCALIB registers
- PORT remap functions with alternate pin locations for Timer/Counter output compare channels, USART0 and SPI, and the PORT REMAP register
- PORT RTC clock output option and the RTCOUT bit in the PORT CLKEVOUT register
- PORT remap functions with alternate pin locations for the clock and event output, and the CLKEVPIN bit in the PORT CLKEVOUT register
- TOSC alternate pin locations, and TOSCSEL bit in FUSEBYTE2
- Real Time Counter clock source options of external clock from TOSC1, and 32.768kHz from TOSC, and 32.768kHz from the 32.768kHz internal oscillator, and these configuration options in the RTCSRC bits in the Clock RTCTRL register
- PLL divide by two option, and the PLLDIV bit in the Clock PLLCTRL register
- PLL lock detection failure function and the PLLDIF and PLLFDEN bits in the Clock XOSCFAIL register
- The high drive option for external crystal and the XOSCPWR bit on the Oscillator XOSCCTRL register
- The option to enable sequential startup of the analog modules and the ANAINIT register in MCU Control memory

Problem fix/Workaround

None.

34.3.6 Rev. D

Not sampled.

34.3.7 Rev. C

Not sampled.

34.3.8 Rev. B

- Bandgap voltage input for the ACs can not be changed when used for both ACs simultaneously
- VCC voltage scaler for AC is non-linear
- ADC gain stage cannot be used for single conversion
- ADC has increased INL error for some operating conditions
- ADC gain stage output range is limited to 2.4V
- ADC Event on compare match non-functional
- ADC propagation delay is not correct when 8× – 64× gain is used
- Bandgap measurement with the ADC is non-functional when VCC is below 2.7V
- Accuracy lost on first three samples after switching input to ADC gain stage
- Configuration of PGM and CWCM not as described in XMEGA D Manual
- PWM is not restarted properly after a fault in cycle-by-cycle mode
- BOD will be enabled at any reset
- EEPROM page buffer always written when NVM DATA0 is written
- Pending full asynchronous pin change interrupts will not wake the device
- Pin configuration does not affect Analog Comparator Output
- NMI Flag for Crystal Oscillator Failure automatically cleared
- Writing EEPROM or Flash while reading any of them will not work
- Crystal start-up time required after power-save even if crystal is source for RTC
- RTC Counter value not correctly read after sleep
- Pending asynchronous RTC-interrupts will not wake up device
- TWI Transmit collision flag not cleared on repeated start
- Clearing TWI Stop Interrupt Flag may lock the bus
- TWI START condition at bus timeout will cause transaction to be dropped
- TWI Data Interrupt Flag (DIF) erroneously read as set
- WDR instruction inside closed window will not issue reset
- Non available functions and options

1. Bandgap voltage input for the ACs cannot be changed when used for both ACs simultaneously

If the Bandgap voltage is selected as input for one Analog Comparator (AC) and then selected/deselected as input for another AC, the first comparator will be affected for up to 1µs and could potentially give a wrong comparison result.

Problem fix/Workaround

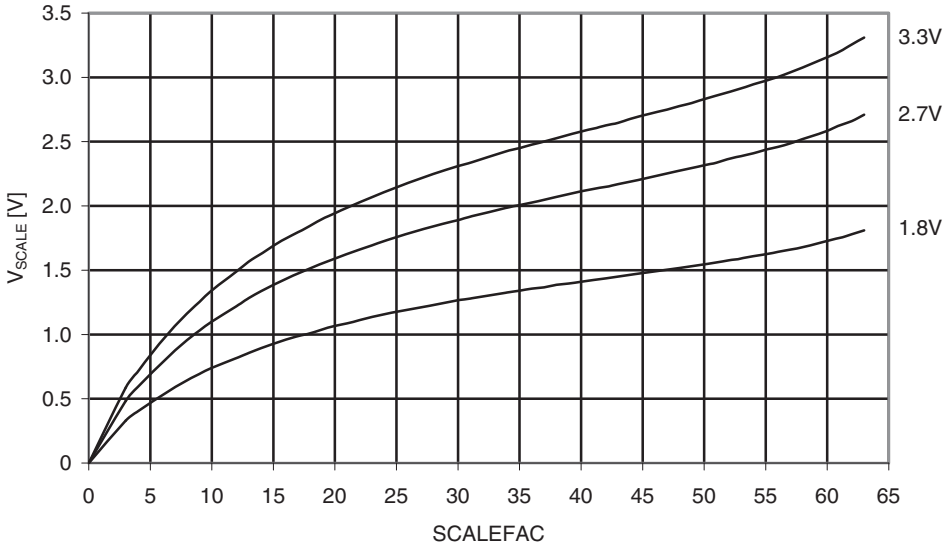
If the Bandgap is required for both ACs simultaneously, configure the input selection for both ACs before enabling any of them.

2. VCC voltage scaler for AC is non-linear

The 6-bit VCC voltage scaler in the Analog Comparators is non-linear.

Figure 34-6. Analog comparator voltage scaler vs. scalefac.

T = 25°C.



Problem fix/Workaround

Use external voltage input for the analog comparator if accurate voltage levels are needed

3. ADC gain stage cannot be used for single conversion

The ADC gain stage will not output correct result for single conversion that is triggered and started from software or event system.

Problem fix/Workaround

When the gain stage is used, the ADC must be set in free running mode for correct results.

4. ADC has increased INL error for some operating conditions

Some ADC configurations or operating condition will result in increased INL error.

In signed mode INL is increased to:

6LSB for sample rates above 130ksps, and up to 8LSB for 200ksps sample rate.

6LSB for reference voltage below 1.1V when V_{CC} is above 3.0V.

20LSB for ambient temperature below 0°C and reference voltage below 1.3V.

In unsigned mode, the INL error cannot be guaranteed, and this mode should not be used.

Problem fix/Workaround

None, avoid using the ADC in the above configurations in order to prevent increased INL error. Use the ADC in signed mode also for single ended measurements.

5. **ADC gain stage output range is limited to 2.4V**

   The amplified output of the ADC gain stage will never go above 2.4V, hence the differential input will only give correct output when below 2.4V/gain. For the available gain settings, this gives a differential input range of:

   - 1× gain: 2.4 V
   - 2× gain: 1.2 V
   - 4× gain: 0.6 V
   - 8× gain: 300 mV
   - 16× gain: 150 mV
   - 32× gain: 75 mV
   - 64× gain: 38 mV

   Problem fix/Workaround

   Keep the amplified voltage output from the ADC gain stage below 2.4V in order to get a correct result, or keep ADC voltage reference below 2.4V.

6. **ADC Event on compare match non-functional**

   ADC signalling event will be given at every conversion complete even if Interrupt mode (INTMODE) is set to BELOW or ABOVE.

   Problem fix/Workaround

   Enable and use interrupt on compare match when using the compare function.

7. **ADC propagation delay is not correct when 8× – 64× gain is used**

   The propagation delay will increase by only one ADC clock cycle for all gain settings.

   Problem fix/Workaround

   None.

8. **Bandgap measurement with the ADC is non-functional when V_{CC} is below 2.7V**

   The ADC can not be used to do bandgap measurements when V_{CC} is below 2.7V.

   Problem fix/Workaround

   None.

9. **Accuracy lost on first three samples after switching input to ADC gain stage**

   Due to memory effect in the ADC gain stage, the first three samples after changing input channel must be disregarded to achieve 12-bit accuracy.

   Problem fix/Workaround

   Run three ADC conversions and discard these results after changing input channels to ADC gain stage.

10. Configuration of PGM and CWCM not as described in XMEGA D Manual

Enabling Common Waveform Channel Mode will enable Pattern generation mode (PGM), but not Common Waveform Channel Mode.

Enabling Pattern Generation Mode (PGM) and not Common Waveform Channel Mode (CWCM) will enable both Pattern Generation Mode and Common Waveform Channel Mode.

Problem fix/Workaround

Table 34-6. Configure PWM and CWCM according to this table:

PGM	CWCM	Description
0	0	PGM and CWCM disabled
0	1	PGM enabled
1	0	PGM and CWCM enabled
1	1	PGM enabled

11. PWM is not restarted properly after a fault in cycle-by-cycle mode

When the AWeX fault restore mode is set to cycle-by-cycle, the waveform output will not return to normal operation at first update after fault condition is no longer present.

Problem fix/Workaround

Do a write to any AWeX I/O register to re-enable the output.

12. BOD will be enabled after any reset

If any reset source goes active, the BOD will be enabled and keep the device in reset if the V_{CC} voltage is below the programmed BOD level. During Power-On Reset, reset will not be released until V_{CC} is above the programmed BOD level even if the BOD is disabled.

Problem fix/Workaround

Do not set the BOD level higher than V_{CC} even if the BOD is not used.

13. EEPROM page buffer always written when NVM DATA0 is written

If the EEPROM is memory mapped, writing to NVM DATA0 will corrupt data in the EEPROM page buffer.

Problem fix/Workaround

Before writing to NVM DATA0, for example when doing software CRC or flash page buffer write, check if EEPROM page buffer active loading flag (EELOAD) is set. Do not write NVM DATA0 when EELOAD is set.

14. Pending full asynchronous pin change interrupts will not wake the device

Any full asynchronous pin-change Interrupt from pin 2, on any port, that is pending when the sleep instruction is executed, will be ignored until the device is woken from another source or the source triggers again. This applies when entering all sleep modes where the System Clock is stopped.

Problem fix/Workaround

None.

15. Pin configuration does not affect Analog Comparator output

The Output/Pull and inverted pin configuration does not affect the Analog Comparator output.

Problem fix/Workaround

None for Output/Pull configuration.

For inverted I/O, configure the Analog Comparator to give an inverted result (that is, connect positive input to the negative AC input and vice versa), or use and external inverter to change polarity of Analog Comparator output.

16. NMI Flag for Crystal Oscillator Failure automatically cleared

NMI flag for Crystal Oscillator Failure (XOSCFDIF) will be automatically cleared when executing the NMI interrupt handler.

Problem fix/Workaround

This device revision has only one NMI interrupt source, so checking the interrupt source in software is not required.

17. Writing EEPROM or Flash while reading any of them will not work

The EEPROM and Flash cannot be written while reading EEPROM or Flash, or while executing code in Active mode.

Problem fix/Workaround

Enter IDLE sleep mode within 2.5µs (five 2MHz clock cycles and 80 32MHz clock cycles) after starting an EEPROM or flash write operation. Wake-up source must either be EEPROM ready or NVM ready interrupt. Alternatively set up a Timer/Counter to give an overflow interrupt 7ms after the erase or write operation has started, or 13ms after atomic erase-and-write operation has started, and then enter IDLE sleep mode.

18. Crystal start-up time required after power-save even if crystal is source for RTC

Even if 32.768kHz crystal is used for RTC during sleep, the clock from the crystal will not be ready for the system before the specified start-up time. See "XOSCSEL[3:0]: Crystal Oscillator Selection" in XMEGA D Manual. If BOD is used in active mode, the BOD will be on during this period (0.5s).

Problem fix/Workaround

If faster start-up is required, go to sleep with internal oscillator as system clock.

19. RTC Counter value not correctly read after sleep

If the RTC is set to wake up the device on RTC Overflow and bit 0 of RTC CNT is identical to bit 0 of RTC PER as the device is entering sleep, the value in the RTC count register can not be read correctly within the first prescaled RTC clock cycle after wakeup. The value read will be the same as the value in the register when entering sleep.

The same applies if RTC Compare Match is used as wake-up source.

Problem fix/Workaround

Wait at least one prescaled RTC clock cycle before reading the RTC CNT value.

20. Pending asynchronous RTC-interrupts will not wake up device

Asynchronous Interrupts from the Real-Time-Counter that is pending when the sleep instruction is executed, will be ignored until the device is woken from another source or the source triggers again.

Problem fix/Workaround

None.

21. TWI Transmit collision flag not cleared on repeated start

The TWI transmit collision flag should be automatically cleared on start and repeated start, but is only cleared on start.

Problem fix/Workaround

Clear the flag in software after address interrupt.

22. Clearing TWI Stop Interrupt Flag may lock the bus

If software clears the STOP Interrupt Flag (APIF) on the same Peripheral Clock cycle as the hardware sets this flag due to a new address received, CLKHOLD is not cleared and the SCL line is not released. This will lock the bus.

Problem fix/Workaround

Check if the bus state is IDLE. If this is the case, it is safe to clear APIF. If the bus state is not IDLE, wait for the SCL pin to be low before clearing APIF.

Code:

```
/* Only clear the interrupt flag if within a "safe zone". */
while ( /* Bus not IDLE: */
       ((COMMS_TWI.MASTER.STATUS & TWI_MASTER_BUSSTATE_gm) !=
         TWI_MASTER_BUSSTATE_IDLE_gc)) &&
         /* SCL not held by slave: */
         !(COMMS_TWI.SLAVE.STATUS & TWI_SLAVE_CLKHOLD_bm)
      )
{
    /* Ensure that the SCL line is low */
    if ( !(COMMS_PORT.IN & PIN1_bm) )
        if ( !(COMMS_PORT.IN & PIN1_bm) )
            break;
}
/* Check for an pending address match interrupt */
if ( !(COMMS_TWI.SLAVE.STATUS & TWI_SLAVE_CLKHOLD_bm) )
{
    /* Safely clear interrupt flag */
    COMMS_TWI.SLAVE.STATUS |= (uint8_t)TWI_SLAVE_APIF_bm;
}
```

23. TWI START condition at bus timeout will cause transaction to be dropped

If Bus Timeout is enabled and a timeout occurs on the same Peripheral Clock cycle as a START is detected, the transaction will be dropped.

Problem fix/Workaround

None.

24. TWI Data Interrupt Flag erroneously read as set

When issuing the TWI slave response command CMD=0b11, it takes one Peripheral Clock cycle to clear the data interrupt flag (DIF). A read of DIF directly after issuing the command will show the DIF still set.

Problem fix/Workaround

Add one NOP instruction before checking DIF.

25. WDR instruction inside closed window will not issue reset

When a WDR instruction is execute within one ULP clock cycle after updating the window control register, the counter can be cleared without giving a system reset.

Problem fix/Workaround

Wait at least one ULP clock cycle before executing a WDR instruction.

26. Non available functions and options

The below function and options are not available. Writing to any registers or fuse to try and enable or configure these functions or options will have no effect, and will be as writing to a reserved address location.

- TWIE, the TWI module on PORTE
- TWI SDAHOLD option in the TWI CTRL register is one bit
- CRC generator module
- ADC 1/2× gain option, and this configuration option in the GAIN bits in the ADC Channel CTRL register
- ADC VCC/2 reference option and this configuration option in the REFSEL bits on the ADC REFCTRL register
- ADC option to use internal Gnd as negative input in differential measurements and this configuration option in the MUXNEG bits in the ADC Channel MUXCTRL register
- ADC channel scan and the ADC SCAN register
- ADC current limitation option, and the CURRLIMIT bits in the ADC CTRLB register
- ADC impedance mode selection for the gain stage, and the IMPMODE bit in the ADC CTRLB register
- Timer/Counter 2 and the SPLITMODE configuration option in the BYTEM bits in the Timer/Counter 0 CTRLE register
- Analog Comparator (AC) current output option, and the AC CURRCTRL and CURRCALIB registers
- PORT remap functions with alternate pin locations for Timer/Counter output compare channels, USART0 and SPI, and the PORT REMAP register
- PORT RTC clock output option and the RTCOUT bit in the PORT CLKEVOUT register
- PORT remap functions with alternate pin locations for the clock and event output, and the CLKEVPIN bit in the PORT CLKEVOUT register.
- TOSC alternate pin locations, and TOSCSEL bit in FUSEBYTE2
- Real Time Counter clock source options of external clock from TOSC1, and 32.768kHz from TOSC, and 32.768kHz from the 32.768kHz internal oscillator, and these configuration options in the RTCSRC bits in the Clock RTCTRL register
- PLL divide by two option, and the PLLDIV bit in the Clock PLLCTRL register
- PLL lock detection failure function and the PLLDIF and PLLFDEN bits in the Clock XOSCFAIL register
- The high drive option for external crystal and the XOSCPWR bit on the Oscillator XOSCCTRL register
- The option to enable sequential startup of the analog modules and the ANAINIT register in MCU Control memory

Problem fix/Workaround

None.

34.3.9 Rev. A

Not sampled.

34.4 Atmel ATxmega256D3

34.4.1 Rev. I

- AC system status flags are only valid if AC-system is enabled.

1. AC system status flags are only valid if AC-system is enabled

The status flags for the ac-output are updated even though the AC is not enabled which is invalid. Also, it is not possible to clear the AC interrupt flags without enabling either of the Analog comparators.

Problem fix/Workaround

Software should clear the AC system flags once, after enabling the AC system before using the AC system status flags.

34.4.2 Rev. H

Not sampled.

34.4.3 Rev. G

Not sampled.

34.4.4 Rev. F

Not sampled.

34.4.5 Rev. E

- Bandgap voltage input for the ACs can not be changed when used for both ACs simultaneously
- V_{CC} voltage scaler for AC is non-linear
- ADC gain stage cannot be used for single conversion
- ADC has increased INL error for some operating conditions
- ADC gain stage output range is limited to 2.4V
- ADC Event on compare match non-functional
- ADC propagation delay is not correct when 8× – 64× gain is used
- Bandgap measurement with the ADC is non-functional when V_{CC} is below 2.7V
- Accuracy lost on first three samples after switching input to ADC gain stage
- Configuration of PGM and CWCM not as described in XMEGA D Manual
- PWM is not restarted properly after a fault in cycle-by-cycle mode
- BOD will be enabled at any reset
- EEPROM page buffer always written when NVM DATA0 is written
- Pending full asynchronous pin change interrupts will not wake the device
- Pin configuration does not affect Analog Comparator Output
- NMI Flag for Crystal Oscillator Failure automatically cleared
- Crystal start-up time required after power-save even if crystal is source for RTC
- RTC Counter value not correctly read after sleep
- Pending asynchronous RTC-interrupts will not wake up device
- TWI Transmit collision flag not cleared on repeated start
- Clearing TWI Stop Interrupt Flag may lock the bus
- TWI START condition at bus timeout will cause transaction to be dropped
- TWI Data Interrupt Flag (DIF) erroneously read as set

- WDR instruction inside closed window will not issue reset
- Non available functions and options

1. Bandgap voltage input for the ACs cannot be changed when used for both ACs simultaneously

If the Bandgap voltage is selected as input for one Analog Comparator (AC) and then selected/deselected as input for another AC, the first comparator will be affected for up to 1µs and could potentially give a wrong comparison result.

Problem fix/Workaround

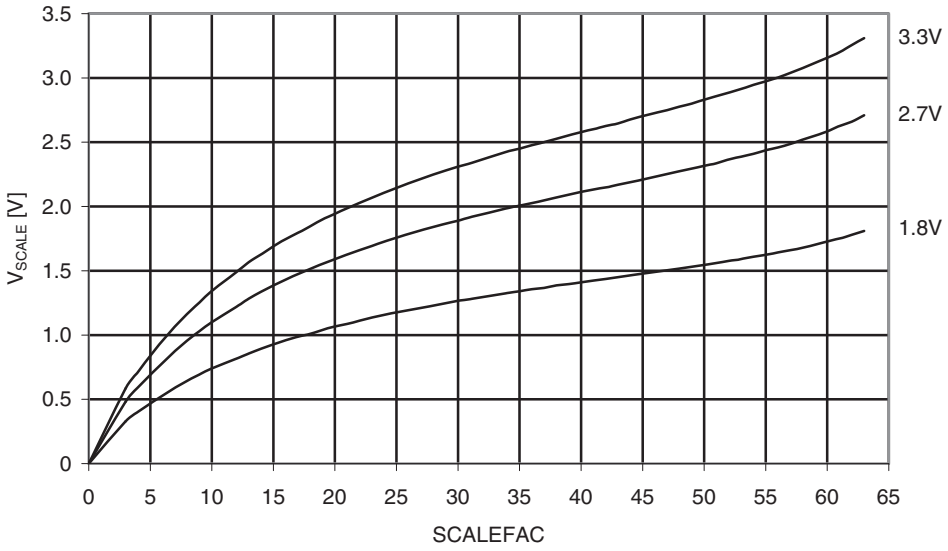
If the Bandgap is required for both ACs simultaneously, configure the input selection for both ACs before enabling any of them.

2. VCC voltage scaler for AC is non-linear

The 6-bit VCC voltage scaler in the Analog Comparators is non-linear.

Figure 34-7. Analog comparator voltage scaler vs. scalefac.

T = 25°C.



Problem fix/Workaround

Use external voltage input for the analog comparator if accurate voltage levels are needed

3. ADC gain stage cannot be used for single conversion

The ADC gain stage will not output correct result for single conversion that is triggered and started from software or event system.

Problem fix/Workaround

When the gain stage is used, the ADC must be set in free running mode for correct results.

4. ADC has increased INL error for some operating conditions

Some ADC configurations or operating condition will result in increased INL error.

In signed mode INL is increased to:

6LSB for sample rates above 130ksps, and up to 8LSB for 200ksps sample rate.

6LSB for reference voltage below 1.1V when V_{CC} is above 3.0V.

20LSB for ambient temperature below 0°C and reference voltage below 1.3V.

In unsigned mode, the INL error cannot be guaranteed, and this mode should not be used.

Problem fix/Workaround

None, avoid using the ADC in the above configurations in order to prevent increased INL error. Use the ADC in signed mode also for single ended measurements.

5. ADC gain stage output range is limited to 2.4V

The amplified output of the ADC gain stage will never go above 2.4V, hence the differential input will only give correct output when below 2.4V/gain. For the available gain settings, this gives a differential input range of:

—	1×	gain:	2.4	V
—	2×	gain:	1.2	V
—	4×	gain:	0.6	V
—	8×	gain:	300	mV
—	16×	gain:	150	mV
—	32×	gain:	75	mV
—	64×	gain:	38	mV

Problem fix/Workaround

Keep the amplified voltage output from the ADC gain stage below 2.4V in order to get a correct result, or keep ADC voltage reference below 2.4V.

6. ADC Event on compare match non-functional

ADC signalling event will be given at every conversion complete even if Interrupt mode (INTMODE) is set to BELOW or ABOVE.

Problem fix/Workaround

Enable and use interrupt on compare match when using the compare function.

7. ADC propagation delay is not correct when 8× – 64× gain is used

The propagation delay will increase by only one ADC clock cycle for all gain settings.

Problem fix/Workaround

None.

8. Bandgap measurement with the ADC is non-functional when V_{CC} is below 2.7V

The ADC can not be used to do bandgap measurements when V_{CC} is below 2.7V.

Problem fix/Workaround

None.

9. Accuracy lost on first three samples after switching input to ADC gain stage

Due to memory effect in the ADC gain stage, the first three samples after changing input channel must be disregarded to achieve 12-bit accuracy.

Problem fix/Workaround

Run three ADC conversions and discard these results after changing input channels to ADC gain stage.

10. Configuration of PGM and CWCM not as described in XMEGA D Manual

Enabling Common Waveform Channel Mode will enable Pattern generation mode (PGM), but not Common Waveform Channel Mode.

Enabling Pattern Generation Mode (PGM) and not Common Waveform Channel Mode (CWCM) will enable both Pattern Generation Mode and Common Waveform Channel Mode.

Problem fix/Workaround

Table 34-7. Configure PWM and CWCM according to this table:

PGM	CWCM	Description
0	0	PGM and CWCM disabled
0	1	PGM enabled
1	0	PGM and CWCM enabled
1	1	PGM enabled

11. PWM is not restarted properly after a fault in cycle-by-cycle mode

When the AWeX fault restore mode is set to cycle-by-cycle, the waveform output will not return to normal operation at first update after fault condition is no longer present.

Problem fix/Workaround

Do a write to any AWeX I/O register to re-enable the output.

12. BOD will be enabled after any reset

If any reset source goes active, the BOD will be enabled and keep the device in reset if the V_{CC} voltage is below the programmed BOD level. During Power-On Reset, reset will not be released until V_{CC} is above the programmed BOD level even if the BOD is disabled.

Problem fix/Workaround

Do not set the BOD level higher than V_{CC} even if the BOD is not used.

13. EEPROM page buffer always written when NVM DATA0 is written

If the EEPROM is memory mapped, writing to NVM DATA0 will corrupt data in the EEPROM page buffer.

Problem fix/Workaround

Before writing to NVM DATA0, for example when doing software CRC or flash page buffer write, check if EEPROM page buffer active loading flag (EELOAD) is set. Do not write NVM DATA0 when EELOAD is set.

14. Pending full asynchronous pin change interrupts will not wake the device

Any full asynchronous pin-change Interrupt from pin 2, on any port, that is pending when the sleep instruction is executed, will be ignored until the device is woken from another source or the source triggers again. This applies when entering all sleep modes where the System Clock is stopped.

Problem fix/Workaround

None.

15. Pin configuration does not affect Analog Comparator output

The Output/Pull and inverted pin configuration does not affect the Analog Comparator output.

Problem fix/Workaround

None for Output/Pull configuration.

For inverted I/O, configure the Analog Comparator to give an inverted result (that is, connect positive input to the negative AC input and vice versa), or use and external inverter to change polarity of Analog Comparator output.

16. NMI Flag for Crystal Oscillator Failure automatically cleared

NMI flag for Crystal Oscillator Failure (XOSCFDIF) will be automatically cleared when executing the NMI interrupt handler.

Problem fix/Workaround

This device revision has only one NMI interrupt source, so checking the interrupt source in software is not required.

17. Crystal start-up time required after power-save even if crystal is source for RTC

Even if 32.768kHz crystal is used for RTC during sleep, the clock from the crystal will not be ready for the system before the specified start-up time. See "XOSCSEL[3:0]: Crystal Oscillator Selection" in XMEGA D Manual. If BOD is used in active mode, the BOD will be on during this period (0.5s).

Problem fix/Workaround

If faster start-up is required, go to sleep with internal oscillator as system clock.

18. RTC Counter value not correctly read after sleep

If the RTC is set to wake up the device on RTC Overflow and bit 0 of RTC CNT is identical to bit 0 of RTC PER as the device is entering sleep, the value in the RTC count register can not be read correctly within the first prescaled RTC clock cycle after wake-up. The value read will be the same as the value in the register when entering sleep.

The same applies if RTC Compare Match is used as wake-up source.

Problem fix/Workaround

Wait at least one prescaled RTC clock cycle before reading the RTC CNT value.

19. Pending asynchronous RTC-interrupts will not wake up device

Asynchronous Interrupts from the Real-Time-Counter that is pending when the sleep instruction is executed, will be ignored until the device is woken from another source or the source triggers again.

Problem fix/Workaround

None.

20. TWI Transmit collision flag not cleared on repeated start

The TWI transmit collision flag should be automatically cleared on start and repeated start, but is only cleared on start.

Problem fix/Workaround

Clear the flag in software after address interrupt.

21. Clearing TWI Stop Interrupt Flag may lock the bus

If software clears the STOP Interrupt Flag (APIF) on the same Peripheral Clock cycle as the hardware sets this flag due to a new address received, CLKHOLD is not cleared and the SCL line is not released. This will lock the bus.

Problem fix/Workaround

Check if the bus state is IDLE. If this is the case, it is safe to clear APIF. If the bus state is not IDLE, wait for the SCL pin to be low before clearing APIF.

Code:

```
/* Only clear the interrupt flag if within a "safe zone". */
while ( /* Bus not IDLE: */
       ((COMMS_TWI.MASTER.STATUS & TWI_MASTER_BUSSTATE_gm) !=
         TWI_MASTER_BUSSTATE_IDLE_gc)) &&
         /* SCL not held by slave: */
         !(COMMS_TWI.SLAVE.STATUS & TWI_SLAVE_CLKHOLD_bm)
      )
{
    /* Ensure that the SCL line is low */
    if ( !(COMMS_PORT.IN & PIN1_bm) )
        if ( !(COMMS_PORT.IN & PIN1_bm) )
            break;
}
/* Check for an pending address match interrupt */
if ( !(COMMS_TWI.SLAVE.STATUS & TWI_SLAVE_CLKHOLD_bm) )
{
    /* Safely clear interrupt flag */
    COMMS_TWI.SLAVE.STATUS |= (uint8_t)TWI_SLAVE_APIF_bm;
}
```

22. TWI START condition at bus timeout will cause transaction to be dropped

If Bus Timeout is enabled and a timeout occurs on the same Peripheral Clock cycle as a START is detected, the transaction will be dropped.

Problem fix/Workaround

None.

23. TWI Data Interrupt Flag erroneously read as set

When issuing the TWI slave response command CMD=0b11, it takes one Peripheral Clock cycle to clear the data interrupt flag (DIF). A read of DIF directly after issuing the command will show the DIF still set.

Problem fix/Workaround

Add one NOP instruction before checking DIF.

24. WDR instruction inside closed window will not issue reset

When a WDR instruction is execute within one ULP clock cycle after updating the window control register, the counter can be cleared without giving a system reset.

Problem fix/Workaround

Wait at least one ULP clock cycle before executing a WDR instruction.

25. Non available functions and options

The below function and options are not available. Writing to any registers or fuse to try and enable or configure these functions or options will have no effect, and will be as writing to a reserved address location.

- TWIE, the TWI module on PORTE
- TWI SDAHOLD option in the TWI CTRL register is one bit
- CRC generator module
- ADC 1/2× gain option, and this configuration option in the GAIN bits in the ADC Channel CTRL register
- ADC VCC/2 reference option and this configuration option in the REFSEL bits on the ADC REFCTRL register
- ADC option to use internal Gnd as negative input in differential measurements and this configuration option in the MUXNEG bits in the ADC Channel MUXCTRL register
- ADC channel scan and the ADC SCAN register
- ADC current limitation option, and the CURRLIMIT bits in the ADC CTRLB register
- ADC impedance mode selection for the gain stage, and the IMPMODE bit in the ADC CTRLB register
- Timer/Counter 2 and the SPLITMODE configuration option in the BYTEM bits in the Timer/Counter 0 CTRLE register
- Analog Comparator (AC) current output option, and the AC CURRCTRL and CURRCALIB registers
- PORT remap functions with alternate pin locations for Timer/Counter output compare channels, USART0 and SPI, and the PORT REMAP register
- PORT RTC clock output option and the RTCOUT bit in the PORT CLKEVOUT register
- PORT remap functions with alternate pin locations for the clock and event output, and the CLKEVPIN bit in the PORT CLKEVOUT register
- TOSC alternate pin locations, and TOSCSEL bit in FUSEBYTE2
- Real Time Counter clock source options of external clock from TOSC1, and 32.768kHz from TOSC, and 32.768kHz from the 32.768kHz internal oscillator, and these configuration options in the RTCSRC bits in the Clock RTCTRL register
- PLL divide by two option, and the PLLDIV bit in the Clock PLLCTRL register
- PLL lock detection failure function and the PLLDIF and PLLFDEN bits in the Clock XOSCFAIL register
- The high drive option for external crystal and the XOSCPWR bit on the Oscillator XOSCCTRL register
- The option to enable sequential startup of the analog modules and the ANAINIT register in MCU Control memory

Problem fix/Workaround

None.

34.4.6 Rev. D

Not sampled.

34.4.7 Rev. C

Not sampled.

34.4.8 Rev. B

- Bandgap voltage input for the ACs can not be changed when used for both ACs simultaneously
- VCC voltage scaler for AC is non-linear
- ADC gain stage cannot be used for single conversion
- ADC has increased INL error for some operating conditions
- ADC gain stage output range is limited to 2.4V
- ADC Event on compare match non-functional
- ADC propagation delay is not correct when 8× – 64× gain is used
- Bandgap measurement with the ADC is non-functional when VCC is below 2.7V
- Accuracy lost on first three samples after switching input to ADC gain stage
- Configuration of PGM and CWCM not as described in the XMEGA D Manual
- PWM is not restarted properly after a fault in cycle-by-cycle mode
- BOD will be enabled at any reset
- EEPROM page buffer always written when NVM DATA0 is written
- Pending full asynchronous pin change interrupts will not wake the device
- Pin configuration does not affect Analog Comparator Output
- NMI Flag for Crystal Oscillator Failure automatically cleared
- Writing EEPROM or Flash while reading any of them will not work
- Crystal start-up time required after power-save even if crystal is source for RTC
- RTC Counter value not correctly read after sleep
- Pending asynchronous RTC-interrupts will not wake up device
- TWI Transmit collision flag not cleared on repeated start
- Clearing TWI Stop Interrupt Flag may lock the bus
- TWI START condition at bus timeout will cause transaction to be dropped
- TWI Data Interrupt Flag (DIF) erroneously read as set
- WDR instruction inside closed window will not issue reset
- Non available functions and options

1. Bandgap voltage input for the ACs cannot be changed when used for both ACs simultaneously

If the Bandgap voltage is selected as input for one Analog Comparator (AC) and then selected/deselected as input for another AC, the first comparator will be affected for up to 1µs and could potentially give a wrong comparison result.

Problem fix/Workaround

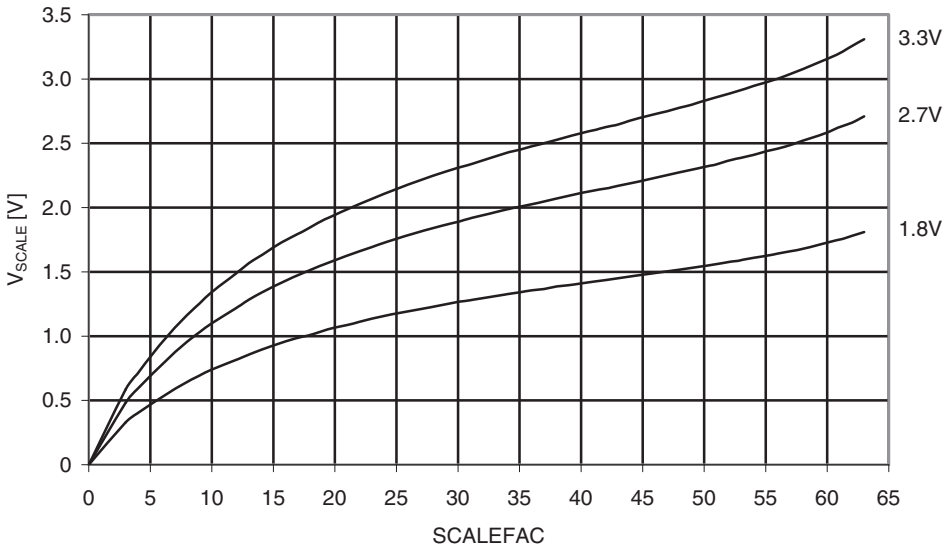
If the Bandgap is required for both ACs simultaneously, configure the input selection for both ACs before enabling any of them.

2. VCC voltage scaler for AC is non-linear

The 6-bit VCC voltage scaler in the Analog Comparators is non-linear.

Figure 34-8. Analog comparator voltage scaler vs. scalefac.

T = 25°C.



Problem fix/Workaround

Use external voltage input for the analog comparator if accurate voltage levels are needed

3. ADC gain stage cannot be used for single conversion

The ADC gain stage will not output correct result for single conversion that is triggered and started from software or event system.

Problem fix/Workaround

When the gain stage is used, the ADC must be set in free running mode for correct results.

4. ADC has increased INL error for some operating conditions

Some ADC configurations or operating condition will result in increased INL error.

In signed mode INL is increased to:

6LSB for sample rates above 130ksps, and up to 8LSB for 200ksps sample rate.

6LSB for reference voltage below 1.1V when V_{CC} is above 3.0V.

20LSB for ambient temperature below 0°C and reference voltage below 1.3V.

In unsigned mode, the INL error cannot be guaranteed, and this mode should not be used.

Problem fix/Workaround

None, avoid using the ADC in the above configurations in order to prevent increased INL error. Use the ADC in signed mode also for single ended measurements.

5. **ADC gain stage output range is limited to 2.4V**

   The amplified output of the ADC gain stage will never go above 2.4V, hence the differential input will only give correct output when below 2.4V/gain. For the available gain settings, this gives a differential input range of:

   - 1× gain: 2.4 V
   - 2× gain: 1.2 V
   - 4× gain: 0.6 V
   - 8× gain: 300 mV
   - 16× gain: 150 mV
   - 32× gain: 75 mV
   - 64× gain: 38 mV

   Problem fix/Workaround

   Keep the amplified voltage output from the ADC gain stage below 2.4V in order to get a correct result, or keep ADC voltage reference below 2.4V.

6. **ADC Event on compare match non-functional**

   ADC signalling event will be given at every conversion complete even if Interrupt mode (INTMODE) is set to BELOW or ABOVE.

   Problem fix/Workaround

   Enable and use interrupt on compare match when using the compare function.

7. **ADC propagation delay is not correct when 8× – 64× gain is used**

   The propagation delay will increase by only one ADC clock cycle for all gain settings.

   Problem fix/Workaround

   None.

8. **Bandgap measurement with the ADC is non-functional when V_{CC} is below 2.7V**

   The ADC can not be used to do bandgap measurements when V_{CC} is below 2.7V.

   Problem fix/Workaround

   None.

9. **Accuracy lost on first three samples after switching input to ADC gain stage**

   Due to memory effect in the ADC gain stage, the first three samples after changing input channel must be disregarded to achieve 12-bit accuracy.

   Problem fix/Workaround

   Run three ADC conversions and discard these results after changing input channels to ADC gain stage.

10. Configuration of PGM and CWCM not as described in XMEGA D Manual

Enabling Common Waveform Channel Mode will enable Pattern Generation Mode (PGM), but not Common Waveform Channel Mode.

Enabling Pattern Generation Mode (PGM) and not Common Waveform Channel Mode (CWCM) will enable both Pattern Generation Mode and Common Waveform Channel Mode.

Problem fix/Workaround

Table 34-8. Configure PWM and CWCM according to this table:

PGM	CWCM	Description
0	0	PGM and CWCM disabled
0	1	PGM enabled
1	0	PGM and CWCM enabled
1	1	PGM enabled

11. PWM is not restarted properly after a fault in cycle-by-cycle mode

When the AWeX fault restore mode is set to cycle-by-cycle, the waveform output will not return to normal operation at first update after fault condition is no longer present.

Problem fix/Workaround

Do a write to any AWeX I/O register to re-enable the output.

12. BOD will be enabled after any reset

If any reset source goes active, the BOD will be enabled and keep the device in reset if the V_{CC} voltage is below the programmed BOD level. During Power-On Reset, reset will not be released until V_{CC} is above the programmed BOD level even if the BOD is disabled.

Problem fix/Workaround

Do not set the BOD level higher than V_{CC} even if the BOD is not used.

13. EEPROM page buffer always written when NVM DATA0 is written

If the EEPROM is memory mapped, writing to NVM DATA0 will corrupt data in the EEPROM page buffer.

Problem fix/Workaround

Before writing to NVM DATA0, for example when doing software CRC or flash page buffer write, check if EEPROM page buffer active loading flag (EELOAD) is set. Do not write NVM DATA0 when EELOAD is set.

14. Pending full asynchronous pin change interrupts will not wake the device

Any full asynchronous pin-change Interrupt from pin 2, on any port, that is pending when the sleep instruction is executed, will be ignored until the device is woken from another source or the source triggers again. This applies when entering all sleep modes where the System Clock is stopped.

Problem fix/Workaround

None.

15. Pin configuration does not affect Analog Comparator output

The Output/Pull and inverted pin configuration does not affect the Analog Comparator output.

Problem fix/Workaround

None for Output/Pull configuration.

For inverted I/O, configure the Analog Comparator to give an inverted result (that is, connect positive input to the negative AC input and vice versa), or use and external inverter to change polarity of Analog Comparator output.

16. NMI Flag for Crystal Oscillator Failure automatically cleared

NMI flag for Crystal Oscillator Failure (XOSCFDIF) will be automatically cleared when executing the NMI interrupt handler.

Problem fix/Workaround

This device revision has only one NMI interrupt source, so checking the interrupt source in software is not required.

17. Writing EEPROM or Flash while reading any of them will not work

The EEPROM and Flash cannot be written while reading EEPROM or Flash, or while executing code in Active mode.

Problem fix/Workaround

Enter IDLE sleep mode within 2.5µs (five 2MHz clock cycles and 80 32MHz clock cycles) after starting an EEPROM or flash write operation. Wake-up source must either be EEPROM ready or NVM ready interrupt. Alternatively set up a Timer/Counter to give an overflow interrupt 7ms after the erase or write operation has started, or 13ms after atomic erase-and-write operation has started, and then enter IDLE sleep mode.

18. Crystal start-up time required after power-save even if crystal is source for RTC

Even if 32.768kHz crystal is used for RTC during sleep, the clock from the crystal will not be ready for the system before the specified start-up time. See "XOSCSEL[3:0]: Crystal Oscillator Selection" in XMEGA D Manual. If BOD is used in active mode, the BOD will be on during this period (0.5s).

Problem fix/Workaround

If faster start-up is required, go to sleep with internal oscillator as system clock.

19. RTC Counter value not correctly read after sleep

If the RTC is set to wake up the device on RTC Overflow and bit 0 of RTC CNT is identical to bit 0 of RTC PER as the device is entering sleep, the value in the RTC count register can not be read correctly within the first prescaled RTC clock cycle after wakeup. The value read will be the same as the value in the register when entering sleep.

The same applies if RTC Compare Match is used as wake-up source.

Problem fix/Workaround

Wait at least one prescaled RTC clock cycle before reading the RTC CNT value.

20. Pending asynchronous RTC-interrupts will not wake up device

Asynchronous Interrupts from the Real-Time-Counter that is pending when the sleep instruction is executed, will be ignored until the device is woken from another source or the source triggers again.

Problem fix/Workaround

None.

21. TWI Transmit collision flag not cleared on repeated start

The TWI transmit collision flag should be automatically cleared on start and repeated start, but is only cleared on start.

Problem fix/Workaround

Clear the flag in software after address interrupt.

22. Clearing TWI Stop Interrupt Flag may lock the bus

If software clears the STOP Interrupt Flag (APIF) on the same Peripheral Clock cycle as the hardware sets this flag due to a new address received, CLKHOLD is not cleared and the SCL line is not released. This will lock the bus.

Problem fix/Workaround

Check if the bus state is IDLE. If this is the case, it is safe to clear APIF. If the bus state is not IDLE, wait for the SCL pin to be low before clearing APIF.

Code:

```
/* Only clear the interrupt flag if within a "safe zone". */
while ( /* Bus not IDLE: */
       ((COMMS_TWI.MASTER.STATUS & TWI_MASTER_BUSSTATE_gm) !=
         TWI_MASTER_BUSSTATE_IDLE_gc)) &&
         /* SCL not held by slave: */
         !(COMMS_TWI.SLAVE.STATUS & TWI_SLAVE_CLKHOLD_bm)
      )
{
    /* Ensure that the SCL line is low */
    if ( !(COMMS_PORT.IN & PIN1_bm) )
        if ( !(COMMS_PORT.IN & PIN1_bm) )
            break;
}
/* Check for an pending address match interrupt */
if ( !(COMMS_TWI.SLAVE.STATUS & TWI_SLAVE_CLKHOLD_bm) )
{
    /* Safely clear interrupt flag */
    COMMS_TWI.SLAVE.STATUS |= (uint8_t)TWI_SLAVE_APIF_bm;
}
```

23. TWI START condition at bus timeout will cause transaction to be dropped

If Bus Timeout is enabled and a timeout occurs on the same Peripheral Clock cycle as a START is detected, the transaction will be dropped.

Problem fix/Workaround

None.

24. TWI Data Interrupt Flag erroneously read as set

When issuing the TWI slave response command CMD=0b11, it takes one Peripheral Clock cycle to clear the data interrupt flag (DIF). A read of DIF directly after issuing the command will show the DIF still set.

Problem fix/Workaround

Add one NOP instruction before checking DIF.

25. WDR instruction inside closed window will not issue reset

When a WDR instruction is execute within one ULP clock cycle after updating the window control register, the counter can be cleared without giving a system reset.

Problem fix/Workaround

Wait at least one ULP clock cycle before executing a WDR instruction.

26. Non available functions and options

The below function and options are not available. Writing to any registers or fuse to try and enable or configure these functions or options will have no effect, and will be as writing to a reserved address location.

- TWIE, the TWI module on PORTE
- TWI SDAHOLD option in the TWI CTRL register is one bit
- CRC generator module
- ADC 1/2× gain option, and this configuration option in the GAIN bits in the ADC Channel CTRL register
- ADC VCC/2 reference option and this configuration option in the REFSEL bits on the ADC REFCTRL register
- ADC option to use internal Gnd as negative input in differential measurements and this configuration option in the MUXNEG bits in the ADC Channel MUXCTRL register
- ADC channel scan and the ADC SCAN register
- ADC current limitation option, and the CURRLIMIT bits in the ADC CTRLB register
- ADC impedance mode selection for the gain stage, and the IMPMODE bit in the ADC CTRLB register
- Timer/Counter 2 and the SPLITMODE configuration option in the BYTEM bits in the Timer/Counter 0 CTRLE register
- Analog Comparator (AC) current output option, and the AC CURRCTRL and CURRCALIB registers
- PORT remap functions with alternate pin locations for Timer/Counter output compare channels, USART0 and SPI, and the PORT REMAP register
- PORT RTC clock output option and the RTCOUT bit in the PORT CLKEVOUT register
- PORT remap functions with alternate pin locations for the clock and event output, and the CLKEVPIN bit in the PORT CLKEVOUT register.
- TOSC alternate pin locations, and TOSCSEL bit in FUSEBYTE2
- Real Time Counter clock source options of external clock from TOSC1, and 32.768kHz from TOSC, and 32.768kHz from the 32.768kHz internal oscillator, and these configuration options in the RTCSRC bits in the Clock RTCTRL register
- PLL divide by two option, and the PLLDIV bit in the Clock PLLCTRL register
- PLL lock detection failure function and the PLLDIF and PLLFDEN bits in the Clock XOSCFAIL register
- The high drive option for external crystal and the XOSCPWR bit on the Oscillator XOSCCTRL register
- The option to enable sequential startup of the analog modules and the ANAINIT register in MCU Control memory

Problem fix/Workaround

None.

34.4.9 Rev. A

Not sampled.

34.5 Atmel ATxmega384D3

34.5.1 Rev. B

No known errata.

34.5.2 Rev. A

Not sampled.

35. Datasheet revision history

Please note that the referring page numbers in this section are referred to this document. The referring revision in this section are referring to the document revision.

35.1 8134K – 05/2013

1.	"Errata" is updated.

35.2 8134J – 03/2013

1.	Almost all figures in Chapter "Typical characteristics" are updated.
2.	Added new Errata "Rev. G" on page 117.
3.	Added new Errata "Rev. B" on page 125 and "Rev. E" on page 118. Non available functions and options.
4.	Editing updates.
5.	Added ATxmega32D3 and ATxmega384D3.
6.	New datasheet template is added.
7.	A lot of small corrections and a complete reorganization of "Electrical characteristics" and "Typical characteristics" .
8.	Bullet "Optional Slew Rate Control" in Chapter "I/O ports" on page 29 is removed
9.	The sentence "The port pins also have configurable slew rate limitation to reduce electromagnetic emission" in Chapter "I/O ports" on page 29 is removed.
10.	The sentence "The I/O pins complies with the JEDEC LVTTL and LVCMOS specification and the high- and low level input and output voltage limits reflect or exceed this specification" is added to Section 32.1.5 on page 68, Section 32.2.5 on page 87, Section 32.6.5 on page 161, Section 33.3.2 on page 224, Section 33.4.2 on page 258, Section 33.5.2 on page 292 and Section 33.6.2 on page 326.
11.	Figure 2-1 on page 4 is updated by changing VDD to VCC.
12.	Table 7-1 on page 14 is updated.
13.	Figure 7-2 on page 15 is updated.
14.	Figure 14-7 on page 32 is updated.
15.	Former Table 32-24, Table 32-52, Table 32-79, Table 32-107, Table 32-135, Table 32-163 (title: "External clock") have each been replaced by two new tables, named respectively "External clock used as system clock without prescaling" and "External clock with prescaler for system clock".
16.	In Table 32-29 on page 81, Table 32-57 on page 98, Table 32-86 on page 117, Table 32-115 on page 136, Table 32-144 on page 155, and Table 32-172 on page 172 the value for the parameter "Input voltage" has been corrected.
17.	In Table 32-18 on page 73, Table 32-47 on page 92, Table 32-75 on page 109, Table 32-104 on page 128, Table 32-133 on page 147, and Table 32-162 on page 166 the parameter "Application erase" has been added.
18.	Table 32-14 on page 72, Table 32-43 on page 91, Table 32-100 on page 127, Table 32-129 on page 146 and Table 32-158 on page 165 (Brownout detection characteristics) are updated.
19.	Table 32-20 on page 74 and Table 32-49 on page 93 (2MHz internal oscillator characteristics) are updated.

20.	Table 32-21 on page 74 and Table 32-50 on page 93 (32MHz internal oscillator characteristics) are updated.
21.	Accuracy added in Table 32-108 on page 129.
22.	Table 32-148 on page 158 has been corrected.
23	Table 32-166 on page 167; “Factory calibration accuracy” and “Accuracy” is added.
24.	Table 32-149 on page 159, Table 32-151 on page 161, Table 32-153 on page 162, Table 32-154 on page 163, Table 32-155 on page 164, and Table 32-156 on page 164 has been updated.
25.	Section 1. “Ordering information” on page 2 is updated
26.	Former Section 31.3 “64Z3” has been removed.
27.	Section 31.2 “64M” on page 62 has replaced the former Section 31.2 “64M2”.

35.3 8134I – 12/2010

1.	Datasheet status changed to complete: Preliminary removed from front page.
2.	Updated all tables in the The maximum CPU clock frequency depends on VCC. As shown in Figure 32-8 on page 83 the frequency vs. VCC curve is linear between 1.8V < VCC < 2.7V. on page 64
3.	Replaced Table 31-11 on page 67.
4.	Replaced Table 31-17 on page 68 and added the figure “TOSC input capacitance” on page 78.
5.	Added “Rev. E” on page 118.
6.	Updated ERRATA for ADC (ADC has increased INL error for some operating conditions).
7.	Updated ERRATA “Rev. B” on page 125 with twie (TWIE is not available).
8.	Updated the last page by Atmel new Brand Style Guide.

35.4 8134H – 09/2010

1.	Updated “Errata” on page 352.

35.5 8134G – 08/2010

1.	Updated the Footnote 3 of “Ordering information” on page 2.
2.	All references to CRC removed. Updated Figure 3-1 on page 5.
3.	Updated “Features” on page 29.
4.	Updated “DC Characteristics” on page 61 by adding Icc for Flash/EEPROM Programming.
5.	Added AV_{CC} in “ADC Characteristics” on page 68.
6.	Updated Start up time in “ADC Characteristics” on page 68.
7.	Updated and fixed typo in “Errata” on page 352.

35.6 8134F – 02/2010

1. Added “PDI Speed” on page 105.

35.7 8134E – 01/2010

1. Updated the device pin-out Figure 2-1 on page 4. PDI_CLK and PDI_DATA renamed only PDI.
2. Updated “ADC – 12-bit Analog to Digital Converter” on page 44.
3. Updated Figure 25-1 on page 45.
4. Updated “Alternate pin function description” on page 49.
5. Updated “Alternate pin functions” on page 50.
6. Updated “Timer/counter and AWEX functions” on page 49.
7. Added Table 31-17 on page 68.
8. Added Table 31-18 on page 69.
9. Changed internal oscillator speed to “Power-on reset current consumption vs. VCC. BOD level = 3.0V, enabled in continuous mode.” on page 108
10. Updated “Errata” on page 352.

35.8 8134D – 11/2009

1. Added Table 31-3 on page 64, Endurance and data retention
2. Updated Table 31-10 on page 67, Input hysteresis is in V and not in mV.
3. Added “Errata” on page 352
4. Editing updates.

35.9 8134C – 10/2009

1. Updated “Features” on page 1 with two-wire interfaces.
2. Updated “Pinout/block diagram” on page 4.
3. Updated “Overview” on page 5.
4. Updated “XMEGA D# block diagram” on page 5.
5. Updated Table 13-1 on page 28.
6. Updated “Overview” on page 38.
7. Updated Table 28-5 on page 53.
8. Updated “Peripheral module address map” on page 54.

35.10 8134B – 08/2009

1. Added The maximum CPU clock frequency depends on VCC. As shown in Figure 32-8 on page 83 the frequency vs. VCC curve is linear between 1.8V < VCC < 2.7V. on page 64.
2. Added “Typical characteristics” on page 174.

35.11 8134A – 03/2009

1. Initial revision.

Table of Contents

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