PGA450-Q1 EVM User's Guide

User's Guide



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PGA450-Q1 EVM User's Guide

1 Read This First

The PGA450-Q1 is an interface device for ultrasonic transducers used in automotive parking assistance and blind spot detection applications. The device functions as the driver and receiver for a wide range of transducers with frequency ranges from 40kHz to 70kHz. The PGA450-Q1 incorporates an analog front end (AFE) and a 8051W microprocessor core. The AFE includes voltage regulators, an amplifier, an ADC, an oscillator, and a temperature sensor. The PGA450-Q1 also implements LIN 2.1 physical layer for communication. For more details, see the device data sheet.

2 About This Manual

This user's guide describes the characteristics, operation, and use of the PGA450-Q1 EVM. An EVM description, GUI description, interface requirements, and complete schematic are included.

3 EVM Overview

The features of this EVM are as follows:

- Single power-supply input for basic operation
- Example push-pull transformer and 58-kHz transducer
- LIN master transceiver
- RS-232 transceiver for UART testing and debug
- PC control with a graphical user interface and USB communications board

4 CAUTION

- 1. The PGA450-Q1EVM can have either a through-hole or surface-mount transformer installed on it. When a through-hole transformer is installed, ensure that the case corners are not touching the surface mount pads.
- 2. The PGA450-Q1EVM can be used to drive either a single-ended or push-pull transformer. The selection of the drive method is achieved through jumper selection.
- 3. The USB communication board 5-V power supply must be enabled for LIN communication to work. The 5-V power supply provides power to the LIN master transceiver installed on the board.
- 4. In order to communicate with PGA450-Q1 using SPI, the 8051W inside the device must be put in the reset state.



5 **Power-Supply Requirements and Connections**

5.1 Power Supply

Only one main power supply is needed. Apply 7 VDC to 18 VDC to the PGA450-Q1EVM that supplies power to the entire board, except for the USB communications board and LIN which are powered by the USB communication PCB. Connect a power supply to the banana jacks, P1 "VPWR_IN" and P3 "GND" or use the screw terminal P2.

5.2 Controlling and Powering the PGA450-Q1 EVM via the USB Interface Board

The PGA450-Q1 EVM is shipped with a USB interface board that provides a link from the PC-controlled GUI (described later) to the EVM. Connect the USB interface board to the PGA450-Q1 by connecting the 30-pin female header on the interface board to P6, the male 30-pin header on the PGA450-Q1 EVM. The TI logo on the interface board should face up when it is plugged in. Figure 1 shows the interface board connected to the PGA450-Q1 EVM.



Figure 1. PGA450-Q1 EVM Set-Up

5.3 Connecting the Transducer

A Murata transducer is included with the EVM. Solder the transducer connector to the through-holes at P6. Alternatively, use the screw terminal to connect the transducer.



6 Jumper Settings

There are several jumpers and $0-\Omega$ resistors located on the board, which are used to configure the connections to the PGA450-Q1 and the rest of the EVM. The default settings and their effects are listed below.

6.1 Jumpers

Table 1 shows the function of each specific jumper setting on the EVM.

Reference	Jumper Setting	Function
	Closed	VP_OTP power supply input on the PGA450-Q1 is connected to the 8-V voltage supply on the EVM.
vi witteon	Open	VP_OTP power supply input on the PGA450-Q1 is not connected to the 8-V voltage supply on the EVM.
	Closed	VPWR is connected to V_LIN, which is the LIN bus voltage.
	Open	VPWR is not connected to V_LIN, which is the LIN bus voltage.
ID2	Closed	The secondary of the transformer on the EVM is connected to the PGA450-Q1 on the EVM.
JEQ	Open	The secondary of the transformer on the EVM is not connected to the PGA450-Q1 on the EVM.
JP4	Closed	The transformer primary top terminal is connected to the OUTA pin on PGA450-Q1, for push-pull configuration. ⁽¹⁾
	Open	The transformer primary top terminal is not connected to the OUTA pin on PGA450-Q1.
JP5	Closed	The transformer primary top terminal is connected to the VREG pin on PGA450-Q1, for single-ended configuration.
	Open	The transformer primary top terminal is not connected to the VREG pin on PGA450-Q1.

Table 1. Jumpers

⁽¹⁾ The transformer provided with the EVM is push-pull. When using the single-ended configuration, JP4 must be disconnected and JP5 must be closed

6.2 Default Jumper Settings

Reference	Jumper Position	Function
VPWR:VOTP	Open	VP_OTP power supply input on the PGA450-Q1 is not connected to the 8-V voltage supply on the EVM.
VPWR:VLIN	Closed	VPWR is connected to V_LIN, which is the LIN bus voltage.
JP3	Closed	The secondary of the transformer on the EVM is connected to PGA450-Q1 on the EVM.
JP4	Closed	The transformer primary terminal 1 is connected to the OUTA pin on the PGA450-Q1 for push-pull configuration.
JP5	Open	The transformer primary terminal 1 is not connected to the VREG pin on the PGA450-Q.

6.3 0-Ω Resistors

The 0- Ω resistor R2 is used to connect the programming voltage to the PGA450-Q1 that is soldered to the PCB. This resistor is not populated on the PCB. The soldered device has had the OTP programmed for DEVRAM usage.

Table 3. Default 0-Ω Resistor Setting

Reference	Install	Function
R2	DNP	The VP_OTP pin of the device does not have OTP programming voltage.

Although they are installed to default settings in the factory, it is recommended that the user verify that the jumpers and $0-\Omega$ resistors are installed to their default settings before powering on the EVM.



7 Socket for Programming OTP

The PGA450-Q1 EVM runs from the PGA450-Q1 device that is soldered to the board. In addition, the EVM provides a footprint for a socket to enable programming the OTP in devices that are for customerboard use. The socket is not populated by default on the EVM. The part number for the recommended socket is OTS-28-0.65-01.

The GUI then can be used to select the target PGA450-Q1 when programming OTP (the two options are the soldered device, or the device in the socket). More details of how to do this are described in the OTP section.

8 Transformer and Transducer

The PGA450-Q1 has a matched transformer-transducer pair. The transformer is a tunable Toko push-pull transformer, whereas the transducer is a Murata transducer with the Murata part number MA58MF14-0N (58 kHz).





9 PGA450-Q1 Communication Interfaces

The PGA450-Q1 has several communication options including: SPI, LIN, and UART. All of these communication interfaces and related circuitry are present on the PGA450-Q1 EVM.

9.1 SPI

SPI is the main communication method on the PGA450-Q1. The 8051W inside the device must be put in reset to communicate using SPI. The SPI signals can be monitored with the CS, SCLK, SDI, and SDO test points on the EVM.

9.2 LIN

8

The EVM includes a LIN transceiver, which is the master transceiver. The PGA450-Q1 is always a slave on the LIN bus and has the slave transceiver integrated inside the device.





Figure 3. LIN Master Transceiver

The 5-V supply in Figure 3 is provided by the USB communication board.

9.3 UART

An RS-232 transceiver (MAX3221) is present on the EVM that can be used as a debugging interface from the 8051 MCU to a host PC. The circuit connects the TXD and RXD pins on the PGA450-Q1 to the MAX3221. The RX and TX RS-232 signals are routed to a standard DB-9 connector on the EVM. The RS-232 circuit is shown in Figure 4.



10.0k,0603,1/10W,5%

Figure 4. RS232 Transceiver



10 Controlling the PGA450-Q1 Memory Spaces With the GUI

The PGA450-Q1 EVM is controlled by the user through a PC with the USB communication board and associated GUI. The PGA450-Q1 EVM GUI provides ways to manipulate all of the register spaces present inside the PGA450-Q1 (ESFR, EEPROM, RAM, OTP, DEVELOPMENT RAM). The following sections describe how to manipulate the register spaces.

10.1 Using the Register Grids to Manipulate the Register Spaces

Most of the register spaces have register grids associated with them that provide a simple way to read/write the registers in the grid. There are eight buttons that are associated with the grid operations: ZERO GRID, DESELECT GRID, SAVE GRID, RECALL GRID, READ SELECTED, WRITE SELECTED, READ ALL, and WRITE ALL. These buttons perform operations on whichever register grid is currently displayed. For example, when the GUI first loads, the ESFR register tab is displayed, if any of the previously listed buttons are pressed they perform operations on the ESFR register space. Each of the GRID functions is in one of the following sections.

10.1.1 ZERO GRID

The ZERO GRID button replaces the contents of the entire grid with 0.

10.1.2 DESELECT GRID

The DESELECT GRID button removes any selections that have been made in the grid without performing any operations on the registers that were selected.

10.1.3 SAVE GRID

The SAVE GRID button takes the contents of the register grid and saves them to a .TXT file. The data is saved in comma-separated-values format.

10.1.4 RECALL GRID

The RECALL GRID button opens a prompt that allows the user to select a .TXT file that was produced during the SAVE GRID operation and then loads the grid with the contents from the .TXT file.

10.1.5 READ SELECTED

The READ SELECTED button performs a read operation on any registers in the grid that have been selected by clicking the desired register number. Any selected registers are displayed blue.

10.1.6 WRITE SELECTED

The WRITE SELECTED button will perform a write operation on any registers in the grid that have been selected by clicking the register number or modifying the register contents. Any selected registers are displayed in blue and any modified registers are highlighted in yellow. Any blue or yellow registers are written to when the WRITE SELECTED button is pressed.

10.1.7 READ ALL

The READ ALL button performs a read operation on every register in the grid.

10.1.8 WRITE ALL

The WRITE ALL button performs a write operation on every register in the grid.



Controlling the PGA450-Q1 Memory Spaces With the GUI

10.2 ESFR Registers

The ESFR register displays all the function registers that are specific to PGA450-Q1 functionality. The user can set each register manually through SPI or define register values in 8051W firmware. An *Evaluation* tab on the right side helps to set the ESFR registers for quick evaluation. More details of the *Evaluation* tab are described in a later section.

10.3 EEPROM Registers

The EEPROM in the PGA450-Q1 comprises 32 bytes of EEPROM and an EEPROM cache. When the EEPROM grid is updated in the GUI, only the cache is updated.

10.3.1 Program EEPROM

The *Program EEPROM* button writes 0x01 to the EE_CTRL ESFR to program the EEPROM memory cells. The EEPROM memory cells are programmed with the values that are in the EEPROM cache inside the PGA450-Q1.

The contents in the GUI are first transferred to the cache and then the cache is programmed.

10.3.2 Reload EEPROM

The *Reload EEPROM* button reloads the EEPROM cache inside the PGA450-Q1 with the values in the EEPROM memory cells. It then performs a READ ALL to update the grid with the refreshed contents of the EEPROM bank.

The contents of the EEPROM cache can be updated on the GUI by clicking on the READ SELECTED or READ ALL button.

10.4 RAM

The RAM tab is set up only for individual register read/writes without the use of the grid. When this tab is displayed, the READ SELECTED / READ ALL and WRITE SELECTED / WRITE ALL buttons perform the same operations, respectively.

The PGA450-Q1 has 512 bytes of general-purpose RAM. This general-purpose RAM is memory-mapped into two different memory spaces inside the PGA450-Q1: internal memory space (0x00–0xFF) and external memory space (0x0300–0x03FF).

The user must select the appropriate memory space in the Combo Box before making the Read/Write request. Note the valid address range for the two RAM sections.

10.5 OTP

The OTP tab is set up only for individual register read/writes without the use of the grid. When this tab is displayed, the READ SELECTED / READ ALL and WRITE SELECTED / WRITE ALL buttons perform the same operations, respectively. The OTP tab also contains buttons used to load a .HEX 8051 program file into the 8051 MCU in the PGA450-Q1.

The PGA450-Q1 EVM could potentially have two devices: a device that is soldered on the EVM and a device that is in the socket. The GUI allows programming of either device. When the device choice is made, the GUI automatically resets the microprocessor for the respective device so that it is ready to load OTP through SPI

NOTE: The OTP program requires R2 to be populated and the VPWR:VOTP jumper to be installed. This connects the VPROG_OTP 8-V supply on the VP_OTP pin during programming. See the data sheet for more details.



10.5.1 Load .HEX File Into GUI

The Load .HEX File into GUI button is used to load the contents of a .HEX file into the GUI RAM for use with other operations. When the button is pressed, a second window opens that allows the user to locate and open the desired .HEX file on the PC. See Figure 5 for an example of this operation.



Figure 5. Loading a .HEX File Into the GUI

10.5.2 Program OTP Memory from .HEX File

If the *Program OTP Memory from .HEX File* check box was checked (default) when the .HEX file was loaded into the GUI, the OTP memory is programmed with the contents of the .HEX file.

10.5.3 Verify OTP Programming

If the *Verify OTP Programming* button was also checked (default), then after the OTP memory is finished programming, the GUI reads the contents of the OTP memory through SPI and verifies against the .HEX file. If the OTP memory matches the contents of the .HEX file, the GUI displays the message "OTP Memory Verification Successful," as seen in Figure 6.



	DISCONNECT	TIME: 1:04 PM BASE CONVERTER
ERROF	S RESET THIS APPLICATION	3//5V JMP 2//5 DVM1 Image: Constraint of the second seco
ESFR EEPROM RAM OTP DEVRAM FIFO/EC	O EVAL MONITOR	Evaluation LIN Test MUX
ADDRESS DATA Cx DATA	soldered (MAIN) de	EVICE Transducer Transmit and Receive Settings Transducer Freq KHz BPF Coefficient (HEX) B1 A2 Check OTP Status VREG Voltage UNA Gain VREG Voltage UNA Gain Clock Select Internal Clk Clk with Sync Et Crystal FIFO Mode 12 Bt 8 MId8 bit Transducer Drive and Receive Monitor Analog Echo Signal on TESTO_A
		Amplifier Output (unfiltered) OR Datapath Output (filtered)
ZERO GRID DESELECT GRID READ SELECT SAVE GRID RECALL GRID READ ALL STATUS: L	ED WRITE SELE WRITE A	TEXAS INSTRUMENTS

Figure 6. OTP Memory Successful Programming Verification

10.5.4 Check OTP Status

Press the "Check OTP Status" button to verify what is currently programmed into OTP. The three possible results are:

- Programmed to Jump to DEVRAM: The jump to DEVRAM statement has been programmed into the OTP. This means that programs loaded into the DEVRAM will execute.
- OTP Empty: Nothing has been programmed in the OTP.
- Programmed: The OTP has been programmed with something other than the jump to DEVRAM statement.

10.6 DEVRAM

The DEVRAM tab is set up only for individual register read/writes, without the use of the grid. When this tab is displayed, the READ SELECTED / READ ALL and WRITE SELECTED / WRITE ALL buttons perform the same operations, respectively. The DEVRAM tab also contains buttons used to load a .HEX 8051 program file into the 8051 MCU in the PGA450-Q1.

The process of loading the .HEX file into the DEVRAM is identical to that of OTP.

For a pristine IC that has never been programmed (OTP Status reads "OTP Empty"), in order to run software from DEVRAM, the OTP memory must be programmed with some specific instructions to redirect the 8051 μ P to DEVRAM. This must only be done once. To do this, check the "Program OTP Memory Also" button, and the GUI will program the OTP with this jump statement as well as program the DEVRAM with the selected HEX file.



ERRORS DISCONNECT USB HARDWARE RESET THIS APPLICATION ESFR EEPROM RAM OTP DEVRAM FIFO/ECHO EVAL MONITOR	Image: Second
ADDRESS DATA Ox DX Load .HEX File into GUI Verfy DEVRAM from .HEX File Verfy DEVRAM Programming	Transducer Transmit and Receive Settings Transducer Freq kHz BPF Coefficient (HEX) B1 A2 B1 A2 A2 A3 LP Coefficient (HEX) B1 A2 B1 B1 B2 B1 B1 B2 B2 B1 B1 B2 B2 B1 B1 B2 B2 B1 B2 B2
OTP Memory can also be programmed while programming the DEVRAM. OTP programming may be needed to program the interrupt vectors.	Downsample: 25 Barrier Output (unfiltered) Downsample: 25 Barrier Output (unfiltered) Downsample: 25 Barrier Output (infiltered) Downsample: 25 Barrier Output (infiltered) Barri
ZERO GRID DESELECT GRID READ SELECTED WRITE SELECTED SAVE GRID RECALL GRID READ ALL WRITE ALL STATUS: Loaded.	Texas Instruments

Note that OTP programming may be required if the interrupt vectors are not programmed

Figure 7. OTP Memory can be programmed while programming the Development RAM

10.7 FIFO/ECHO

10.7.1 FIFO

The PGA450-Q1 has a FIFO RAM that contains the output of the digital data path. The contents of the FIFO RAM can be displayed on the GUI and/or can be plotted in Excel.

The FIFO RAM is displayed in the form of a grid. The GUI grid contents can be updated either by clicking on the READ ALL button or by clicking on the READ SELECTED button.

The FIFO RAM contents can be displayed on the GUI and plotted in Excel by clicking the *Read and Save FIFO Data to File* button.

NOTE: Note: Microsoft Office version 2007 or above is required for this function to work properly.





Figure 8. Echo Data Stored in FIFO RAM Plotted in Excel

10.7.2 EVAL Monitor

This tab graphs the output of the digital data path directly in the GUI. The 8051W microcontroller must be in reset to use this tab.

10.7.2.1 No. of Loops

This option selects how many times the GUI will transmit a burst and plot the echo data.

10.7.2.2 Trigger

If "Auto" is displayed, the GUI will continue sending bursts and plotting the echo data until the "Loops Complete" count matches the "No. of Loops." If "USER" is displayed, the GUI will stop and wait for the user to press the green flashing "Trigger" button before continuing.

10.7.2.3 Resolution

This button has three options, "FULL", "1/2", and "1/4". The "FULL" setting plots all of the echo data points, but takes more time. The "1/2" and "1/4" options reduce the number of data points plotted which results in faster plotting.

10.7.2.4 Clear Plot

The "CLR" button clears all data from the graph. If the "Clear Plot" option is checked, echo data will be cleared from the plot every loop. If "Clear Plot" is not checked, every loop will plot the new echo data in a new color on top of the existing data on the graph.

10.7.2.5 Export Data to Excel

This option exports the echo data to Excel for each loop.

10.7.2.6 Start/Stop

Click on the "Start" button to start the first loop. Click on "Stop" at any time to stop the program immediately.

11 LIN Master

The PGA450-Q1 GUI communicates with the PGA450-Q1 using LIN. The USB Communication board UART is the LIN master, and the PGA450-Q1 is the LIN slave. The GUI can be used to configure the LIN frames that are transmitted to the PGA450-Q1.

		-	ERROF	۱S	D USE F AJ	ISCON B HARD RESET PPLICA	NECT DWAR			E: 1:16 PM UAL V/SV JMP VM1 VM2	⊇ ↓ ↓	BASE CONVERTER 255 FF 1111111111111111
ESFR EEPROM RAM OTP	DEVRAM	FI	FO/EC	но	EV/	AL MO	NITO	R		Evaluation LIN Test MUX		
ADDRESS	HEX	b7	b6 b	5 F	-4 b	3 b2	b1	ь0				
► 92 (BPE B1 MSB)	00 0		0 0	0	0	0	0 (0		TRANSMIT TO L		(PCA450)
93 (BPE_B1_LSB)	00 0		0 0	0	0	0	0 (D				(1 0/430)
94 (BPE A2 MSB)	00 0	,	0 0	0	0	0	0 (D		Soldered Davisor	1	Tx Checksum
95 (BPE A2 LSB)	00 0		0 0	0	0	0	0 (D	Ξ	Microcontroller State		ENHANCED -
96 (BPE A3 MSB)	00 0	,	0 0	0	0	0	0 (0		Data to be Txed 0x	~	
97 (BPE A3 LSB)	00 0	,	0 0	0	0	0	0 (D		ON (Misse Astron)		
A1 (LPE_B1_MSB)	00 0	,	0 0	0	0	0	0 (D		Note: 1 byte per row		
A2 (LPE B1 LSB)	00 0	,	0 0	0	0	0	0 (D	-	OFF		
A3 (LPE A2 MSB)	00 0	,	0 0	0	0	0	0 (0		(Micro Reset)		TRANSMIT
A4 (LPE A2 LSB)	00 0	,	0 0	0	0	0	0 (0		MICRO ACTIVE	Ŧ	
A5 (DOWNSAMPLE)	00 0)	0 0	0	0	0	0 (0				
A6 (BURST ONA MSB)	00 0)	0 0	0	0	0	0 (0				
A7 (BURST ONA LSB)	00 0)	0 0	0	0	0	0 (D				
A9 (BURST OFFA MSB)	00 0	,	0 0	0	0	0	0 (D		RECEIVE FROM	LIN SLAVE	= (PGA450)
AA (BURST OFFA LSB)	00 0)	0 0	0	0	0	0 (D		Number of data bytes)	Br Checksum
AB (BURST_ONB_MSB)	00 0)	0 0	0	0	0	0 (0		to be receiied		ENHANCED -
AC (BURST ONB LSB)	00 0)	0 0	0	0	0	0 (D		Rx Frame PID or 0	1	
AD (BURST OFFB MSB)	00 0)	0 0	0	0	0	0 (D		(Enter 6 bits Only)		
AE (BURST OFFB LSB)	00 0)	0 0	0	0	0	0 (0		Data received Ox		
AF (PULSE CNTA)	00 0)	0 0	0	0	0	0 (D				
B1 (PULSE_CNTB)	00 0)	0 0	0	0	0	0 (0				
B2 (DEADTIME)	00 0)	0 0	0	0	0	0 (0		Note: 1 byte per row		
B3 (BURST_MODE)	00 0)	0 0	0	0	0	0 (D				DECENT
	00 0		0 0	0	0	0	0 1	n	*		~	RECEIVE
ZERO GRID DESELECT GRID	REA	D S	ELECT	ED		WRIT	E SEL	.ECT	ED			
SAVE GRID RECALL GRID	F	REA	D ALL			W	RITE	ALL		🔰 👭 Texas Ins	TRUM	IENTS
		STA	TUS: L	.oad	led.							

Figure 9. LIN Master on GUI

In order to transmit data to PGA450-Q1 using a LIN frame, the user must do the following:

- 1. Enter the Frame PID in Edit Box corresponding to "Tx Frame PID". The PID must be entered in hex. Note that valid PID ranges from 0x00 to 0x3F. The GUI software calculates the parity bits using the LIN 2.1 method before the PID is transmitted to the slave.
- 2. Enter 0–8 bytes of data in the "Data to be Txed" box. Each data byte must be entered in Hex.
- 3. Select the CLASSIC or ENHANCED checksum, which must match the LIN checksum setting in the PGA450-Q1 ESFR LIN_CFG register.
- 4. Click on the TRANSMIT button

In order to receive data from PGA450-Q1 using a LIN frame, the user must do the following:

- 1. Enter the Frame PID in Edit Box corresponding to "Rx Frame PID". The PID must be entered in hex. Note that valid PID ranges from 0x00 to 0x3F. The GUI software calculates the parity bits using the LIN 2.1 method before the PID is transmitted.
- 2. Enter the number of data bytes the user expects back from the PGA450-Q1
- 3. Select the CLASSIC or ENHANCED checksum
- 4. Click on the RECEIVE button

The data received from the PGA450-Q1 is displayed in the Data Received box.

If the data communication is not working, try *Reset This Application*, which power-cycles the LIN master IC on the EVM.

12 Use Case

The purpose of this section is to provide step-by-step instructions on the setup and some basic evaluation procedures.

12.1 Evaluation Through SPI Communication

In order to provide a quick evaluation of the IC performance using the TI EVM and GUI without having to develop sophisticated 8051 µP software, the GUI provides an intuitive interface tab, *Evaluation Tab*, that collects all necessary information regarding the transducer drive and receive. For transducer drive, it includes: transducer frequency; transducer drive voltage, VREG; transformer configuration; and number of drive pulses. For transducer signal receive, it includes signal-processing parameters: LNA gain setting; BPF and LPF coefficient; clock selection; FIFO mode; and FIFO downsample size.

- 1. Make sure all jumpers are connected according to the default settings, see Section 6.2.
- 2. Connect the hardware and power supply, see Section 5. Make sure USB cable is connected to the computer and the interface board. It is recommended to monitor power supply current. Normal idle current is around 6 mA. Active current is around 15 mA.
- 3. Launch GUI software on computer.
- 4. Click the "OFF (Micro Reset)" button to put the Micro in reset, then click READ ALL to read the default register values. Some default values are loaded in the table grid. If all are 0 or FF values, this means that there is an error with communication to the device. Check the hardware setup or restart the GUI software.

Fill out the "Evaluation" tab with the values shown in Figure 10.

Use the "Eval Monitor" tab to send bursts and view the resulting echo data.



500	DISCONNECT USB HARDWARE	TIME: 1:18 PM MANUAL	III III III III III III III III I	BASE CONVERTER 255
ERR	RESET THIS APPLICATION	DVM1 DVM2	Ĵ 💽 🖁	FF 1111111111111111
ESFR EEPROM RAM OTP DEVRAM FIFO/E	ECHO EVAL MONITOR		Evaluation LIN Test MUX	
X Axis - FIFO Sample Number (DEC) Y Axis - Datapath Data (DEC)	START	Trigger AUTO Resolution FULL	Transducer Transmit and Receive Settings Transducer Freq 58 kHz BPF Coefficient (HEX) B1 32D A2 EC3D A3 F9A5 LP Coefficient (HEX) B1 2D68 A2 2530 VREG Voltage SV SV SV SV SV SV SV S4B S4 dB 40 dB # of Burst 18	XFMR Config (a) [Push-Pull Single-End Clock Select Clock Select Clock Select Clock Select Clock Select Ext Crystal FIFO Mode 12 Bit (a) 8 LSB (b) 8 MSB (b) Mid8 bit
No. of Loops: 0 (0 - Infinity)	START	Resolution FULL		
Loops Complete:			Transducer Drive and R	eceive
Export Data to Excel			Monitor Analog Echo Signal	on TESTO_A
			Amplifier Output (unfiltered)	atapath Output (filtered)
ZERO GRID DESELECT GRID READ SELECT	CTED WRITE SELECT	TED		
SAVE GRID RECALL GRID READ AL	L WRITE ALL		IEXAS INSTRU	MENTS
STATUS	: Loaded.	•		

Figure 10. Evaluation Tab Setting

After all information is entered, make sure the device is in the micro reset state, then hit the *Transducer Drive and Receive* button to start the burst and receive.

12.2 Monitoring the Signal Path

The PGA450-Q1 has two useful test modes that allow users to quickly observe the echo signal as an amplified analog signal or from a DAC output which converts a digitally filtered echo signal. In the *Evaluation* tab, quick-access buttons *Amplifier Output (unfiltered)* and *Datapath Output (filtered)* are available. The signal is viewable on the DACO pin. Only one mode can be selected at a time. See Figure 11 and Figure 12 for the captured waveforms.



Figure 11. Echo Analog Waveform Output (Channel1), Drive voltage (Channel 2)





Figure 12. DAC Output of Filtered Signal (Channel 2) and Drive Voltage (Channel 1)



13 PGA450-Q1 EVM Schematics and Layout Drawings











PGA450-Q1 EVM Schematics and Layout Drawings





Figure 16. Schematic, USB Controller



PGA450-Q1 EVM Schematics and Layout Drawings



Figure 17. Schematic, PGA450-Q1





Figure 18. PCB Layout, Bottom



Figure 19. PCB Layout, Top

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General Statement for EVMs including a radio

User Power/Frequency Use Obligations: This radio is intended for development/professional use only in legally allocated frequency and power limits. Any use of radio frequencies and/or power availability of this EVM and its development application(s) must comply with local laws governing radio spectrum allocation and power limits for this evaluation module. It is the user's sole responsibility to only operate this radio in legally acceptable frequency space and within legally mandated power limitations. Any exceptions to this are strictly prohibited and unauthorized by Texas Instruments unless user has obtained appropriate experimental/development licenses from local regulatory authorities, which is responsibility of user including its acceptable authorization.

For EVMs annotated as FCC – FEDERAL COMMUNICATIONS COMMISSION Part 15 Compliant

Caution

This device complies with part 15 of the FCC Rules. Operation is subject to the following two conditions: (1) This device may not cause harmful interference, and (2) this device must accept any interference received, including interference that may cause undesired operation.

Changes or modifications not expressly approved by the party responsible for compliance could void the user's authority to operate the equipment.

FCC Interference Statement for Class A EVM devices

This equipment has been tested and found to comply with the limits for a Class A digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference when the equipment is operated in a commercial environment. This equipment generates, uses, and can radiate radio frequency energy and, if not installed and used in accordance with the instruction manual, may cause harmful interference to radio communications. Operation of this equipment in a residential area is likely to cause harmful interference in which case the user will be required to correct the interference at his own expense.

FCC Interference Statement for Class B EVM devices

This equipment has been tested and found to comply with the limits for a Class B digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference in a residential installation. This equipment generates, uses and can radiate radio frequency energy and, if not installed and used in accordance with the instructions, may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one or more of the following measures:

- Reorient or relocate the receiving antenna.
- Increase the separation between the equipment and receiver.
- · Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.
- Consult the dealer or an experienced radio/TV technician for help.

For EVMs annotated as IC – INDUSTRY CANADA Compliant

This Class A or B digital apparatus complies with Canadian ICES-003.

Changes or modifications not expressly approved by the party responsible for compliance could void the user's authority to operate the equipment.

Concerning EVMs including radio transmitters

This device complies with Industry Canada licence-exempt RSS standard(s). Operation is subject to the following two conditions: (1) this device may not cause interference, and (2) this device must accept any interference, including interference that may cause undesired operation of the device.

Concerning EVMs including detachable antennas

Under Industry Canada regulations, this radio transmitter may only operate using an antenna of a type and maximum (or lesser) gain approved for the transmitter by Industry Canada. To reduce potential radio interference to other users, the antenna type and its gain should be so chosen that the equivalent isotropically radiated power (e.i.r.p.) is not more than that necessary for successful communication.

This radio transmitter has been approved by Industry Canada to operate with the antenna types listed in the user guide with the maximum permissible gain and required antenna impedance for each antenna type indicated. Antenna types not included in this list, having a gain greater than the maximum gain indicated for that type, are strictly prohibited for use with this device.

Cet appareil numérique de la classe A ou B est conforme à la norme NMB-003 du Canada.

Les changements ou les modifications pas expressément approuvés par la partie responsable de la conformité ont pu vider l'autorité de l'utilisateur pour actionner l'équipement.

Concernant les EVMs avec appareils radio

Le présent appareil est conforme aux CNR d'Industrie Canada applicables aux appareils radio exempts de licence. L'exploitation est autorisée aux deux conditions suivantes : (1) l'appareil ne doit pas produire de brouillage, et (2) l'utilisateur de l'appareil doit accepter tout brouillage radioélectrique subi, même si le brouillage est susceptible d'en compromettre le fonctionnement.

Concernant les EVMs avec antennes détachables

Conformément à la réglementation d'Industrie Canada, le présent émetteur radio peut fonctionner avec une antenne d'un type et d'un gain maximal (ou inférieur) approuvé pour l'émetteur par Industrie Canada. Dans le but de réduire les risques de brouillage radioélectrique à l'intention des autres utilisateurs, il faut choisir le type d'antenne et son gain de sorte que la puissance isotrope rayonnée équivalente (p.i.r.e.) ne dépasse pas l'intensité nécessaire à l'établissement d'une communication satisfaisante.

Le présent émetteur radio a été approuvé par Industrie Canada pour fonctionner avec les types d'antenne énumérés dans le manuel d'usage et ayant un gain admissible maximal et l'impédance requise pour chaque type d'antenne. Les types d'antenne non inclus dans cette liste, ou dont le gain est supérieur au gain maximal indiqué, sont strictement interdits pour l'exploitation de l'émetteur.

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This development kit is NOT certified as Confirming to Technical Regulations of Radio Law of Japan

If you use this product in Japan, you are required by Radio Law of Japan to follow the instructions below with respect to this product:

- Use this product in a shielded room or any other test facility as defined in the notification #173 issued by Ministry of Internal Affairs and Communications on March 28, 2006, based on Sub-section 1.1 of Article 6 of the Ministry's Rule for Enforcement of Radio Law of Japan,
- 2. Use this product only after you obtained the license of Test Radio Station as provided in Radio Law of Japan with respect to this product, or
- 3. Use of this product only after you obtained the Technical Regulations Conformity Certification as provided in Radio Law of Japan with respect to this product. Also, please do not transfer this product, unless you give the same notice above to the transferee. Please note that if you could not follow the instructions above, you will be subject to penalties of Radio Law of Japan.

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