TSW140x High Speed Data Capture/Pattern Generator Card

The Texas Instruments TSW1400 Evaluation Module (EVM) is a next generation of pattern generator and data capture card used to evaluate performances of a wide range of Texas Instruments (TI) high-speed analog-to-digital converters (ADC) and digital-to-analog converters (DAC). For an ADC, capturing the sampled data over an LVDS interface when using a high-quality, low-jitter clock, and a high-quality input frequency, the TSW1400 can be used to demonstrate data sheet performance specifications. Together with the accompanying LabVIEW™-based Graphic User Interface (GUI), it is a complete system that captures and evaluates data samples from ADC EVM's and generates and sends desired test patterns to DAC EVM's.

The TSW1405 is a low cost data capture card with limited capabilities as compared with the TSW1400. The TSW1405 supports pattern capture for most LVDS format TI ADC EVMs, but with a capture buffer limitation of 64K samples. The TSW1405 draws its power from the USB connection to the PC for easy setup and operation. The same TSW1400 Graphical User Interface supports the TSW1405 as well, making for a consistent feel across the different platforms.

The TSW1406 is a low cost pattern generator card with limited capabilities as compared with the TSW1400. The TSW1406 supports pattern generation for most LVDS format TI DAC EVMs, but with a pattern limitation of 64K samples. The TSW1406 draws its power from the USB connection to the PC for easy setup and operation. The same TSW1400 GUI supports the TSW1406 as well.

Table 1. TSW140x EVM Features

	I/O Interface					
	LVDS	**CMOS**	**JESD**	**16 Bit Memory Depth**	**Data Capture**	**Data Source**
TSW1400	Yes	Yes	No	512M	Yes	Yes
TSW1405	Yes	No	No	64K	Yes	No
TSW1406	Yes	No	No	64K	No	Yes

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1 Functionality

The TSW1400 has two direct interfaces to TI ADC EVM's. One option captures data through a LVDS interface and the other uses a CMOS interface. Sampled data from the ADC is de-serialized and formatted by an Altera Stratix IV FPGA, then stored into an external onboard 1GB DDR memory card. The onboard memory enables the TSW1400 to store up to 512M 16 bit data samples. To acquire data on a host PC, the FPGA reads the data from memory and transmits it on Serial Peripheral Interface (SPI). An onboard high speed USB to SPI converter bridges the FPGA SPI interface to the host PC and GUI.

The TSW1400 has two direct interfaces to TI DAC EVM's. In Pattern Generator Mode, the TSW1400 generates desired test patterns for DAC EVM's under test. These patterns are sent from the host PC over the USB interface to the TSW1400. The FPGA stores the data received into the board DDR memory module. The data from the memory is then read by the FPGA and transmitted to a DAC EVM either across a DAC LVDS interface connector or a CMOS interface connector.

A block diagram of the TSW1400 EVM is shown in Figure 1.

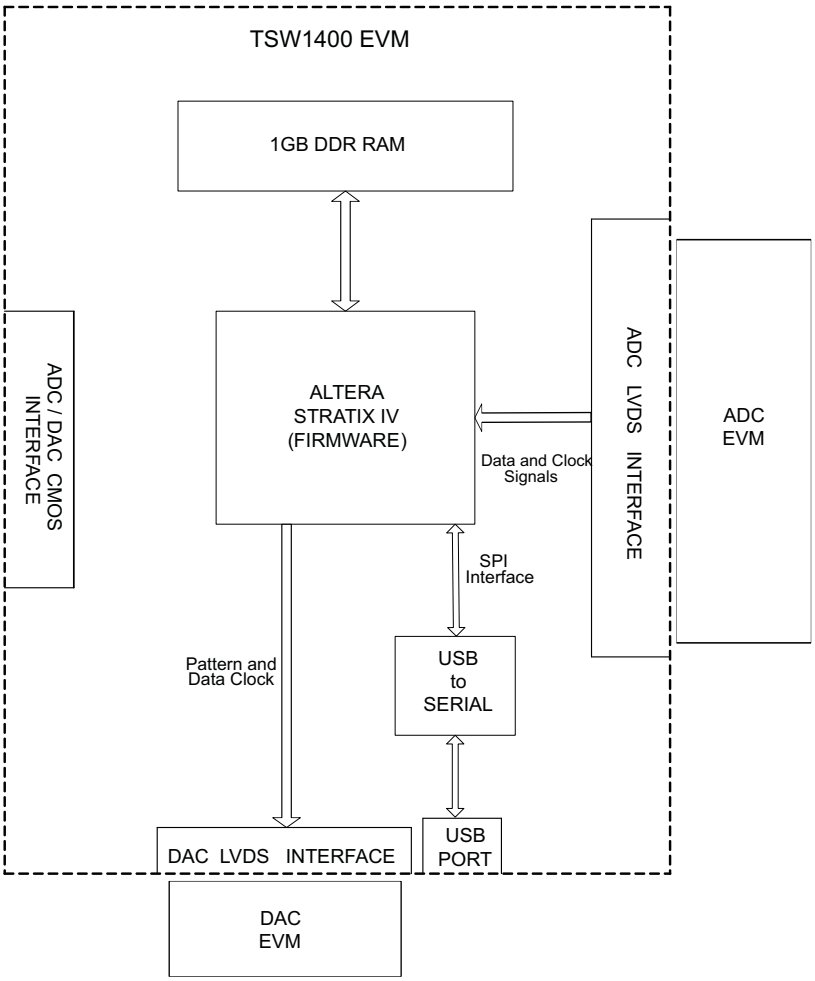

Figure 1. TSW1400EVM Block Diagram

1.1 ADC EVM Data Capture

Many TI high-speed ADCs have LVDS outputs for the digitized data. These ADCs are generally available on an EVM that connects directly to the TSW1400EVM. The common connector between the ADC EVM and the TSW1400EVM is a Samtec high-speed connector with differential pairs routed to adjacent pins and the pairs separated by a ground pin. A common pinout for the connector across a family of EVMs has been established. At present, the interface between the ADC EVM and the TSW1400EVM has defined connections for 35 pairs of LVDS data lines, two clock pairs, and eight general purpose CMOS I/O pins. The TSW1400 has a CMOS interface that provides 44 single ended connections to a two row, 88 pin, 100 mil center, female header style connector.

The data format for the LVDS data bus can be in one of many formats, all supported by the TSW1400. For single-channel, high-speed ADCs, the data format is commonly a parallel dual-data rate with one output clock . Dual-data rate means that both the rising and falling edges of the clock register data into the TSW1400. For multichannel ADCs, the data is commonly presented in a serialized format, where individual bits of the output data are presented on an LVDS pair one bit at a time, at a higher data rate than the sample rate of the ADC.

Several firmware files are used by the FPGA on the TSW1400 to accommodate both parallel DDR formats an serial LVDS formats, although not at the same time. The GUI will load the FPGA with the appropriate firmware based on the ADC EVM under test selected by the user.

The parallel DDR FPGA program supports several types of data formats. One common format presents odd-numbered data bits on the bus on one clock edge and even-numbered data bits on the bus on the other clock edge. This format is commonly used for ADCs with sampling rates up to 250 MHz. For this bit-wise DDR format, the parallel data bus uses half as many LVDS pairs as there are bits in the sample. For example, a 16-bit ADC uses eight LVDS pairs for data plus an LVDS clock pair for bit-wise DDR. For higher sample rates up to 1 GHz, a sample-wise DDR format is often used. For sample-wise DDR, the data bus width has as many LVDS pairs as the bit resolution of the ADC. On one clock edge, a data sample from the ADC is registered; on the next clock edge, the next data sample from the ADC is registered.

The serial FPGA program also supports several data formats. For one-wire serial formats, the data is serialized onto a single LVDS pair at a rate that is 12 times the sample rate for an ADC with a 12-bit resolution. A one-wire serialization format also is used for 14-bit and 16-bit data at data rates 14 or 16 times the sample rate, respectively. For serial data formats, a DDR LVDS bit clock is used to strobe the serial data bits and to de-serialize the data. An additional clock pair operating at the sample rate of the ADC identifies the sample-word boundaries in the serial data. For multichannel ADCs, a single-bit clock and a single sample-rate clock (frame clock) is used for all of the LVDS data channels. The other common serial data format is two-wire serialization. Two-wire serialization is similar to one-wire serialization except that a data channel uses two LVDS pairs to carry the serialized data at a rate that is half of what it is for one-wire serialization.

1.2 DAC EVM Pattern Generator

Some TI high-speed DAC's have LVDS inputs for the digitized data. These DACs are generally available on an EVM that connects directly to the TSW1400EVM. The common connector between the DAC EVM and the TSW1400EVM is a Samtec high-speed connector with differential pairs routed to adjacent pins and the pairs separated by a ground pin. A common pinout for the connector across a family of EVMs has been established. At present, the interface between these DAC EVM's and the TSW1400EVM has defined connections for 32 pairs of LVDS data lines, two data output clock pairs, four control pairs, two input clock pairs (sync, strobes, and so on), eight general purpose CMOS I/O pins (USB controlled) and 10 general purpose CMOS I/O pins (FPGA controlled). The TSW1400 CMOS interface provides up to 40 single-ended CMOS data outputs and two clock sources for CMOS DAC EVM formats. This interface has an option to be either 3V or 1.8V CMOS logic.

2 Hardware Configuration

In this section, the various portions of the TSW1400EVM hardware are described.

2.1 Power Connections

The TSW1400EVM hardware is designed to operate from a single-supply voltage of 5 Vdc. The power input is controlled by the ON/OFF switch SW7. Make sure this switch is in the “OFF” position before inserting the power plug. Connect the 5 V output of the provided AC-to-DC power supply to J12 of the EVM and the other power supply cable to 110-120 VAC source.

2.1.1 Output Power Regulators

The TSW1400 provides two output power sources with these default settings:

- 3.3 V at 3 A at J10 and the return at J9
- 1.8 V at 6 A at J8 and the return to J9.

Both power supplies are derived from on-board switching power supplies and controlled by switch SW7. See the TI TPS54620 (SLVS949) and TPS54325 data sheet (SLVS932) for more information regarding the performance of these devices before deciding to use them to power up external EVM’s.

2.2 Switches, Jumpers and Fuses

2.2.1 Switches and Pushbuttons

Switch SW7 is the main power ON/OFF switch.

Dipswitch SW1 has all switches routed to spare pins on the FPGA. Each switch trace has a pullup to 3.3V and shorts this to ground when the switch is closed. Currently none of the switches are used.

Five pushbutton switches are mounted on the TSW1400EVM. One pushbutton switch currently has a defined function; one of the other switches is reserved for future use.

The CPU_RESET (SW6) pushbutton causes the FPGA to reset the internal PLL logic.

The CONF/ SPI (SW2) will reload the FPGA from a configuration prom (for future board revision).

2.2.2 Jumpers

Jumpers JP5, JP6, and JP7 allow the option to break the connection on three GPIO signals that are routed between connector J3 and USB controller U3 through buffer U16. When the jumper shunts are removed and buffer U16 is disabled, the user can provided external signals to three signals going to an ADC EVM that is connected to J3 by using pin 1 of JP5, JP6, and JP7. Connecting pins 1 and 2 of Jumper SJP1 will disable U16. Connecting pins 1 and 2 of Jumper SJP2 will disable U17, which is the buffer providing the GPIO signals to the DAC EVM interface connector. See the TSW1400 EVM schematic for more details.

Jumpers JP3 and JP4 set the output voltage of buffers U16 and U17. These buffers provide GPIO signals between the TSW1400 and ADC and DAC EVM’s. When set to pins 1-2, the buffers will provide 1.8 V CMOS logic level signal interface to the ADC and DAC EVM connectors. When set to 2-3, the level will be 3 V. JP3 controls the ADC signals, and JP4 controls the DAC signals. See the TSW1400 EVM schematic for more details.

Jumper JP8 sets the signal output voltage of CMOS_PORT1[19:1] bus on connector J1. When set to pins 1-2, the FPGA will provide 1.8 V CMOS logic level signals. When set to 2-3, the level will be 3 V.

2.2.3 Fuses

Fuse F1 is in line with the EVM input power. This is used along with diode D14 to protect the board from surges and over voltage on the input power supply.

Fuse F2, when installed, will provide 6VDC to the DAC EVM interface connector J4.

CAUTION

When using this 6 VDC for a DAC EVM, make sure the DAC EVM power connection is removed.

2.3 LED's

Eleven LED's are on the TSW1400EVM to indicate the presence of power and the state of the FPGA.

The LED on the left edge of the board illuminates to indicate the presence of a 5-V power to the board after SW7 is placed in the "ON" position.

LED D1 illuminates to indicate that the FPGA programming has completed and is now operational.

USER_LED0 and LED1 indicate transmission of data samples over SPI interface.

USER_LED2 turns off when the FPGA is in reset mode.

USER_LED3 indicates the FPGA PLL1 is locked to the ADC input clock from port 0.

USER_LED4 indicates the FPGA PLL2 is locked to the ADC input clock from port 1 or locked to the FPGACLK from the DAC when in the DAC mode.

USER_LED5 indicates that the DDR memory initialization is complete and the interface is ready to use.

USER_LED6 and LED7 indicate that the two SPI FIFO's are empty.

LED D10 indicates the presence of 6-V power to the DAC EVM interface connector J4.

2.4 Connectors

The TSW1400 EVM has several connectors to allow for direct plug in of various TI CMOS and LVDS ADC and DAC EVM's.

2.4.1 Input LVDS ADC Interface Connector

The connection between the TSW1400EVM and the ADC EVM to be tested is through a 128-pin High speed Samtec connector. 35 LVDS data pairs plus two LVDS clock pairs have a defined position in the connector pinout that is common between the TSW1400EVM and many TI ADC EVMs. For the parallel LVDS DDR data format, the bit clock runs at the same rate as the sample clock to the ADC. For the serial LVDS data format, the bit clock runs at a higher multiple of the ADC sample clock and is used to strobe the serial data into the TSW1400EVM and then de-serialize the data. For the serial LVDS data format, a second clock is provided, called the frame clock or FCLK, that runs at the sample rate and is used to delineate the sample boundaries in the serial data stream. The frame clock line can be used as a second clock in the parallel LVDS DDR format that uses two data buses. The data direction for the LVDS data pairs is always defined as the ADC EVM driving the signal through the connector to the TSW1400EVM FPGA, with integrated 100 Ω termination in the FPGA.

For one-channel parallel DDR bit-wise data formats, eight of the LVDS data pairs are used to support up to 16-bit-resolution ADCs at up to 250-MHz sampling rates. For one-channel parallel DDR sample-wise data formats, 14 of the LVDS data pairs are used to support up to 14-bit-resolution ADCs at up to 500-MHz sampling rates. For two-channel parallel DDR bit-wise data formats, 14 of the LVDS data pairs are used to support two channels of 14-bit resolution at up to 250-MHz sampling rate.

For serial data formats, eight of the LVDS data pairs support up to eight channels of one-wire serial ADCs at up to 65-MHz sampling rate or four channels of two-wire serial ADCs at up to 125-MHz sampling rates.

Eight extra CMOS single-ended signals are defined in the Samtec connector that are sourced from the USB interface through the connector to the ADC EVM. These signals, in the future, will allow the GUI to control the SPI serial programming of the ADC for those ADC EVMs that support this feature.

The Samtec connectors snap together with no screws or other mechanism to hold the TSW1400EVM and the ADC EVM together. The TSW1400EVM comes with standoff posts for setting the TSW1400EVM flat on a bench or table. The ADC EVM has shorter standoff posts so that the TSW1400EVM and ADC EVM will lay flat on a bench or table and stay snapped together during use.

2.4.2 JTAG Connector

The TSW1400EVM includes an industry-standard JTAG connector that connects to the JTAG ports of the FPGA and the programming pins of the FPGA EEPROM. Jumpers on the TSW1400EVM allow for either the FPGA or the FPGA EEPROM to be programmed from the JTAG chain. The JTAG connector is to be used for trouble shooting only. The board default setup is with the FPGA JTAG pins connected to the USB interface. This allows the FPGA to be programmed by the GUI though the USB interface. The current design does not support the use of the FPGA EEPROM. Every time the TSW1400 EVM is powered down, the FPGA configuration is removed. The user must program the FPGA through the GUI after every time the board is powered up.

In future versions, once the FPGA is power-cycled or re-programmed by the CONF/SPI pushbutton, the current loaded FPGA bit file will be lost and the FPGA will revert to the bit file that is stored in the FPGA EEPROM.

2.4.3 Input CMOS ADC Interface Connector

The connection between the TSW1400EVM and a CMOS ADC EVM to be tested is through a two row, 88 pin, 100 mil center, Samtec female header style connector (J1). The 40 single-ended data lines and two clock lines have a defined position in the connector pinout that is common between the TSW1400EVM and several TI CMOS ADC EVMs. The Samtec connectors couple together with no screws or other mechanism to hold the TSW1400EVM and the ADC EVM together. The TSW1400EVM comes with standoff posts for setting the TSW1400EVM flat on a bench or table. The ADC EVM has shorter standoff posts so that the TSW1400EVM and ADC EVM will lay flat on a bench or table when connected together.

2.4.4 Output LVDS Connector

The connection between the TSW1400EVM and the DAC EVM to be tested is through a 192-pin High speed Samtec connector. 32 LVDS output data pairs plus two LVDS output clock pairs, four differential control pairs (sync, strobes, and so on), two input clock pairs, eight general purpose CMOS I/O pins (USB controlled) and 10 general purpose CMOS I/O pins (FPGA controlled). These signals have a defined position in the connector pinout that is common between the TSW1400EVM and many TI DAC EVM's.

2.4.5 Output CMOS DAC Interface Connector

The TSW1400EVM CMOS ADC Interface connector, J1, is also used to support several TI CMOS DAC EVM's. The 40 single-ended data lines and two clock lines have a defined position in the connector pinout that is common between the TSW1400EVM and several TI CMOS DAC EVMs. The Samtec connectors couple together with no screws or other mechanism to hold the TSW1400EVM and the DAC EVM together.

2.4.6 USB I/O Connection

Control of the TSW1400EVM is through a USB connection to a PC running Windows operating system. For the computer, the drivers needed to access the USB port are included on the TSW1400 installation software that can be downloaded from the web. The drivers are automatically installed during the installation process. On the TSW1400EVM, the USB port is used to identify the type and serial number of the EVM under test, load the desired FPGA configuration file, capture data from ADC EVM's, and send test pattern data to the DAC EVM's.

On first connection of the USB port to a computer, the Microsoft Found New Hardware Wizard appears. Follow the dialog box prompts as covered in the Software Installation section of this User's Guide.

3 Software Start up

3.1 Installation Instructions

- Download the latest version of the GUI software files and User's Guide manual to a local location on a host PC. These can be found on the TI website by entering "TSW1400EVM" in the search parameter window at www.ti.com.
- Unzipping the software package will generate a folder called "High Speed Data Converter Pro xpx",

where xpx is the version number. Under this folder will be a “setup.bat" file, a folder called “EVM GUI” and another folder called “FTDI”. The EVM GUI folder contains the GUI code and the other folder contains the drivers for the USB interface.

- If running the software for the first time, run the file called “setup.bat”. This loads the FTDI drivers followed by installing the High Speed Data Converter Pro GUI software.
- Follow the on-screen instructions during installation.
- Once installed, the GUI executable will reside in the following directory.
- C:\Program Files\Texas Instruments\High Speed Data Converter Pro.
- Connect one end of a mini-USB cable to J5 (top right corner) of the TSW1400 and the other end to a host PC USB port.

  NOTE: Launch and connect the TSW1400 GUI to the EVM before starting other TI ADC and DAC EVM GUI’s.
- If not already connected, connect the provided 5 VDC power supply to J12, located on the bottom left corner of the board and the end to 110-120 VAC source. Set SW7 to the “ON” position.
- To start the GUI, click on the file called “High Speed Data Converter Pro.exe", located under “C:\Program Files\Texas Instruments\High Speed Data Converter Pro”.

NOTE: If an older version of the GUI has already been installed, make sure to uninstall it before loading a newer version. If the GUI detects a new version of the GUI is available online (http://www.ti.com/tool/tsw1400evm), it will assist the user with downloading the latest version from the TI website. The GUI automatically interrogates the product website for latest version every seven days but the latest version check can also be manually invoked through use of the pull-down menu Help->Check for updates.

NOTE: When new TI HSDC evms become available that are not supported with the current GUI software release, the HSDCProv_xpxx_Patch_setup executable, available on the TI website (www.TI.com), will allow the user to add this to the GUI device list. Doing a search for TSW1400 will direct the user to this location. The user should download this patch . Start the application and follow the on screen instructions. The patch will display the files that will be either added or replaced and have tabs for viewing what files will be deleted and release notes. After running the patch, the user will then be able to start the High Speed Data Converter Pro GUI and notice new parts added to the ADC and DAC device drop down selection box.

The patch is always specific to a core GUI version so the patch application would not work for any GUI version that the patch was not explicitly created for.

3.2 USB Interface and Drivers

The TSW1400 GUI will first attempt to connect to the EVM USB interface. If the GUI identifies a valid board serial number, a pop-up will open displaying this value, as shown in Figure 2. The serial number also has an EVM type number attached to it. This indicates to the GUI which of the three TSW140x boards is being used. It is possible to connect several TSW1400 EVM’s to one host PC but the GUI can only connect to one at a time. If multiple boards are connected to the PC, the pop-up displays all of the serial numbers found. It is then up to the user to select which board the GUI will be associated.

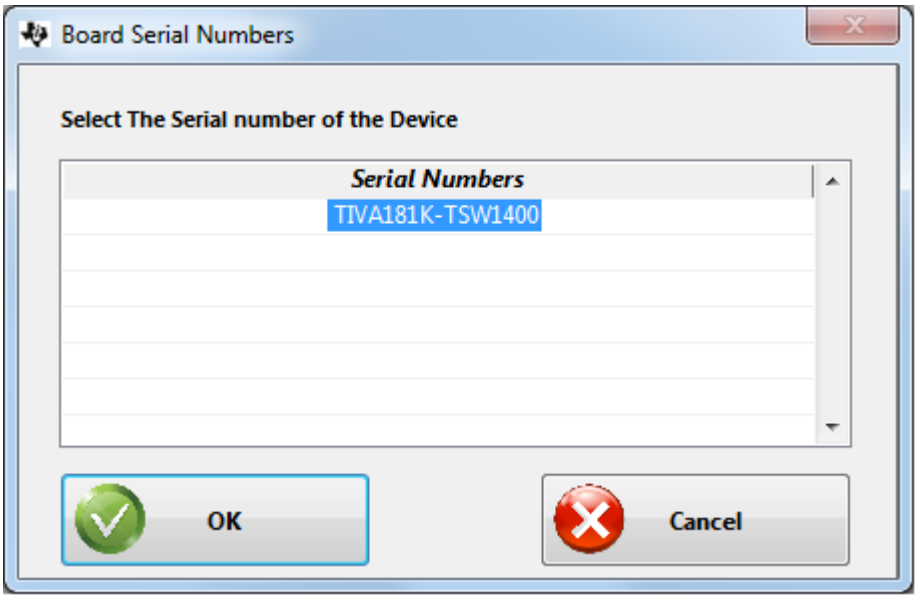

Figure 2. TSW1400EVM Serial Number

Click on “OK” to connect the GUI to the board. If the FPGA firmware version read by the GUI does not match the firmware to be used as determined by the device selected, the following message appears as shown in Figure 3. This message also appears after power up as the FPGA is not programmed.

Figure 3. Firmware Does Not Match the Device Selected

Click on “OK”. The Top level GUI now opens and appears as shown in Figure 4.

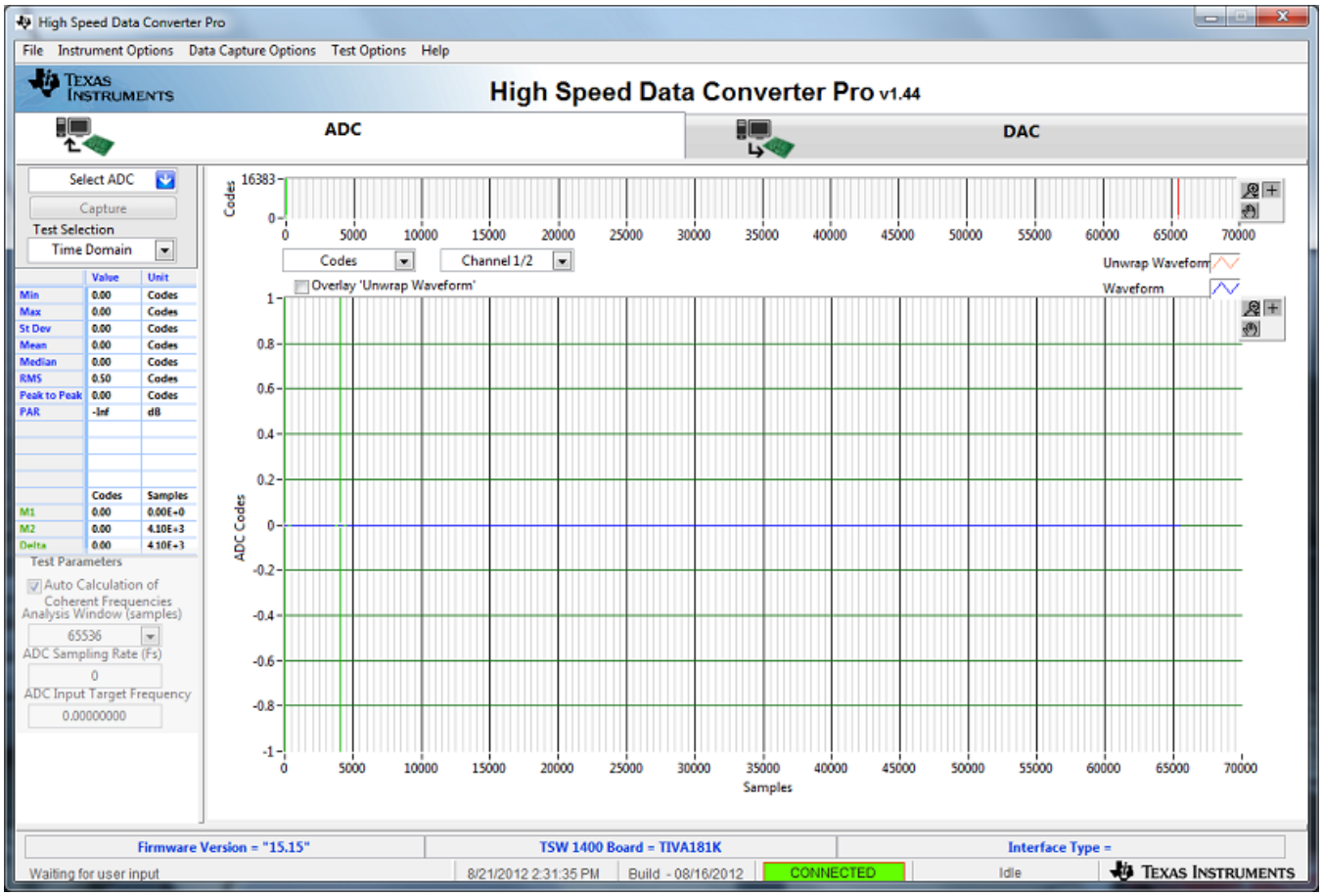

Figure 4. TSW1400EVM GUI Top Level

After the software has established a connection, if the message “Board not Connected” opens, double check the USB cable connections and that power switch SW7 is in the “ON” position. If the cable connections appear fine, try establishing a connection by clicking on the “Instrument Option” tab at the top left of the GUI and select “Connect to the Board” (see Figure 5). If this still does not correct this issue, check the status of the host USB port.

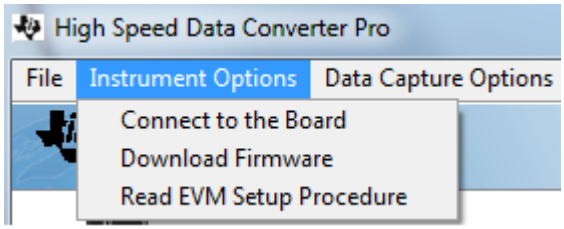

Figure 5. Connecting GUI to EVM

When the software has been installed and the USB cable has been connected to the TSW1400EVM and the PC, the TSW1400 USB serial converter should be located in the Hardware Device Manager under the Universal Serial Bus controllers as shown in Figure 6. This is a quad device which is why there is an A, B, C, and D USB Serial Converter shown. When the USB cable is removed, these four will no longer be visible in the Device Manager. If the drivers are present in the Device Manager window and the software still does not connect, cycle power to the board and repeat the steps above.

If the GUI starts up but freezes before it brings up the "Connected to Board" dialog, or takes unusually long time for other actions to occur, it is possible the USB being used from the host PC is operating at USB 1.0 speeds. A common indication of this is when the status bar on the bottom left of the screen keeps reading "Disable all Controls" upon loading the software without ever going to the "Connect Board Dialog". The GUI is designed to run at USB 2.0 speeds and some computers have USB 1.0 ports on the front panel and 2.0 on the back panel. Using the ports on the back of the PC if at all possible is recommended.

The setup.bat file installs the FTDI drivers during software installation. If after connecting the USB cable and Windows lists the board as an "unknown device", this could be caused by corrupted FTDI drivers being installed on the computer. This happens in cases where the same computer has been used to interface with previous products that used FTDI drivers. In this case, users are advised to download and install a utility from FTDI at http://www.ftdichip.com/Support/Utilities/CDMUninstaller_v1.4.zip.

The help file for using this utility can be found at:
http:/www.ftdichip.com/Support/Utilities/CDM_Uninst_GUI_Readme.html

Users will need to use the following hex values to uninstall previous versions of the ftdi drivers:

Vendor ID (VID): 0403

Product ID (PID): 6010

After removing the drivers for this PID and VID, users are advised to re-connect the TSW140x USB cable and check if the TSW140x ports get listed properly in Device Manager.

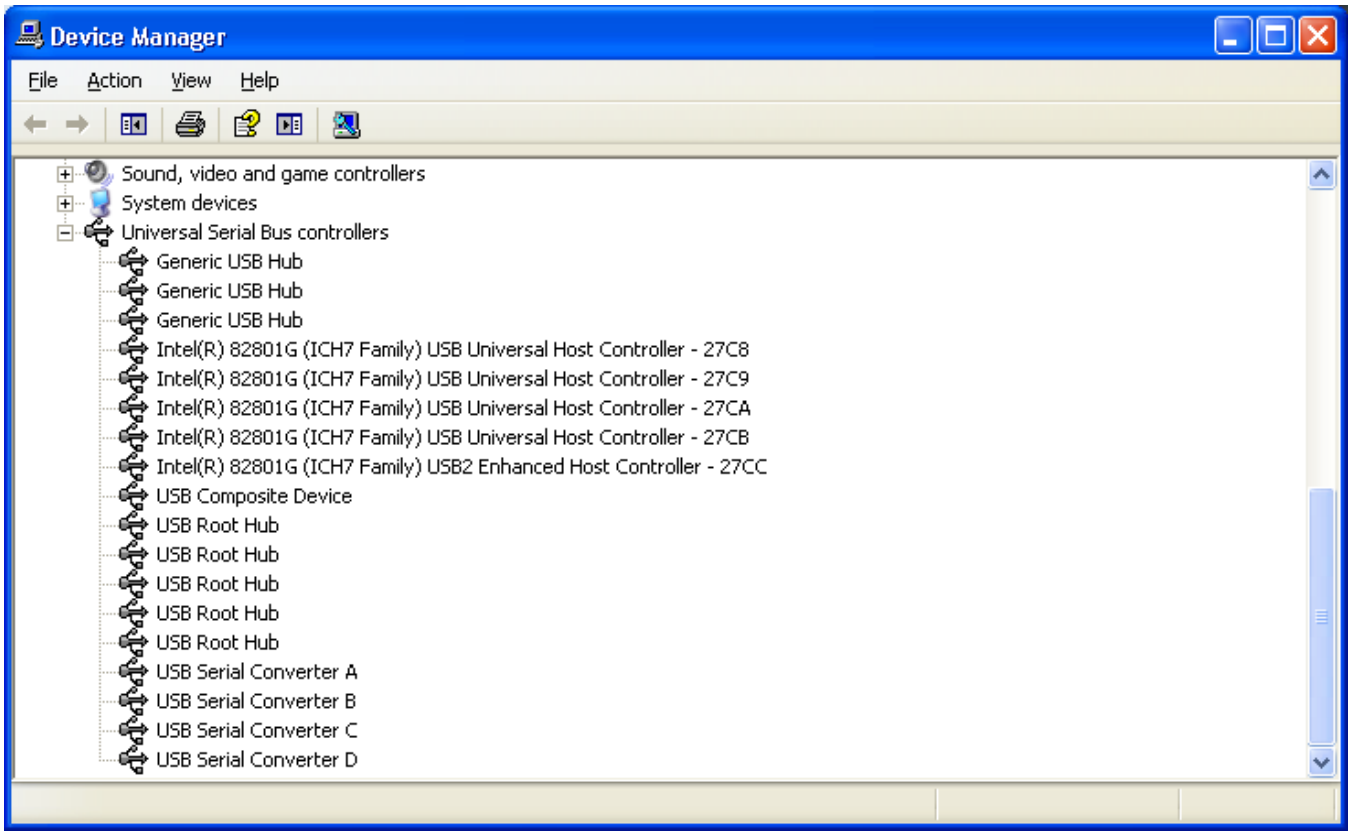

Figure 6. Hardware Device Manager

3.3 Device ini Files

Included in the installation for the TSW1400 GUI software is a subdirectory of ini files for each category of ADC and DAC that is supported by the TSW1400EVM. TI strongly recommends that these files are not edited except at the factory. These files contain necessary information for the GUI software to properly configure the TSW1400EVM FPGA registers for proper operation with the desired ADC or DAC EVM. Some of the entries within the ini file are obvious, such as defining the bit resolution for a device to be 11, 12, 14, or 16 bits. Other entries in the ini file define for the FPGA which LVDS pairs within the Samtec connector define the data bus, and correct operation may not be possible if these entries are edited. The use of ini files allows for new device types to be supported by the TSW1400EVM as they become available without having to modify, re-release, or re-install the TSW1400 GUI software. New device types may be supported at a later date simply by adding a new ini file to the proper subdirectory. This file can be found on the TI website under the TSW1400 product folder.

4 User Interface

When the TSW1400 GUI software is started, the initial setup screen of Figure 4 appears. The TSW1400EVM serial number is reported in the lower center of the GUI. After the FPGA is loaded with the selected firmware, the GUI would reports the firmware version in the bottom left and the interface type will be reported in the lower right. The connection status should read “Connected” and be highlighted in green (lower center of the GUI). The status panel, located in the lower right, will report “IDLE”. Many of the TSW1400 software controls are available from the main screen, such as “ADC or DAC” mode, “Select device”, “Capture and Test Selection” (ADC mode only), and “Load File to transfer to TSW1400” (DAC mode only).

4.1 Toolbar

The toolbar contains options and settings that are independent of the device selected for test or the test to be performed, such as configuration options and save/recall operations. The operations available under the toolbar are grouped in categories as follows: File, Instrument Option, Data Capture Option, Test Option and Help.

4.1.1 File Options

The file tab contains all of the options for saving or importing test results. Placing the mouse indicator over the File tab will open a window with the available options as shown in Figure 7.

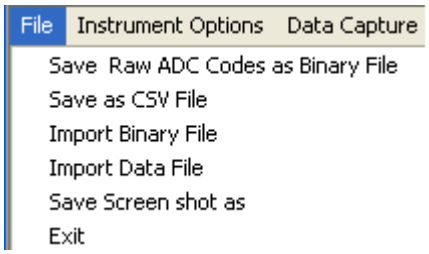

Figure 7. File Tab Options

There are options for saving the ADC captured data as CSV or Binary format in a directory specified by the user for export or archival purposes. The “Save as CSV File” and “Save as Binary File” will save the results that are displayed in the test window. If the Single Tone FFT test is active, then the FFT plot will be saved, along with the performance statistics and setup information. If the Time Domain test is active, then the Time Domain plot will be saved along with the time domain statistics. The “Save Screen shot as “ option, when selected, will open a window that will allow the user to save the current GUI screen shot as either a bmp, jpeg, or png file in the directory specified by the user.

The GUI provides an option to allow the user to replay files captured from an ADC by the GUI itself. To use this feature, import a test file by either selecting "Import Binary File" or "Import Data File" in the drop down. A new navigator window will open. Select the desired file to be loaded. If a binary file is to be used, after the file is selected (.bin file), a new window will open asking for number of channels. Provide this information then click "OK". This 16 bit binary format file must have values from -32768 to 32767, and will

be used by the GUI as input data for display and analysis. For two channel test cases, the test file must be 16 bit interleaved binary data, where channel 1 is the first sample and channel 2 is the second sample. For Data files, the user has an option to use several different types of files. After the file is selected, the GUI will ask for number of channels and number of bits. The user must know this information for proper data to be displayed. The data test file must be in text format having integer values from -32768 to 32767. For two channel test cases, channel 1 is the data in the first column and channel 2 is the data in the second column. The different file types that can be used include .gcin (space), .ssv (space), .csv (comma), .txt (tab), and .tsw. The GUI expects such files to be delimited by the delimiters shown in the parentheses. Adjacent columns are separated by the delimiter. The .tsw files are proprietary encoded files created by Texas Instruments.

4.1.2 Instrument Options

The Instrument Options menu tab contains four options: Reinitialize Instrument, Read EVM Setup Procedure, Download Firmware, and Connect to the Board as shown in Figure 8.

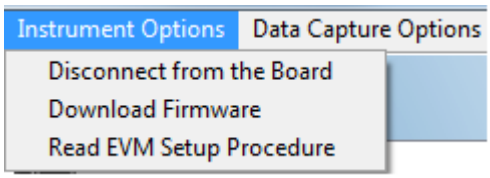

Figure 8. Instrument Options

The Read ADC EVM Setup Procedure command causes the TSW1400 software to read a comment string from the ini file for the device that is currently selected and then display that comment string in the status pane. This comment string generally contains necessary setup information pertaining to the EVM under test, such as possibly requiring a non-default data format or required jumper setting for the EVM to communicate properly with the TSW1400EVM.

The Download Firmware command allows the user to select a file that will be used to program the FPGA. These files need to be .rbf files for this to work. The files used by the GUI currently reside in the directory called ”Firmware”, under the TSW1400 directory. This option would be used if the GUI cannot identify the firmware file called out in the ini file, or if an advanced user has a new file they would like to try.

The Connect to the Board command will cause the GUI to read the serial number inside the USB controller on the TSW1400 and display the value found or report that no board is connected. This can be used when a user removes power from the TSW1400 board, then re-applies power while leaving the GUI active.

4.1.3 Data Capture Option

The Data Capture Option (ADC mode only) has two options: Capture Option or Trigger Option. Selecting Capture Option opens a new window as shown in Figure 9.

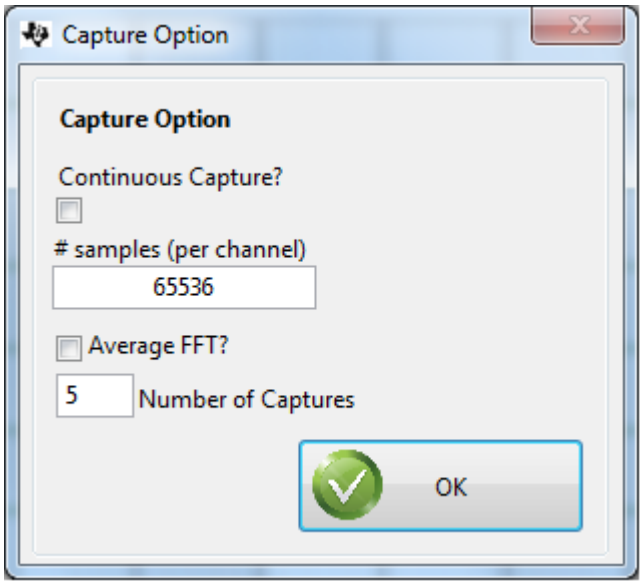

Figure 9. Capture Option

The user can adjust the number of samples to capture from 4096 to 524,288. The GUI will round down to the nearest multiple of 4096 and display this value. This captured data will be displayed in the codes graph of the main screen as another method of letting the user know how many samples of data has been collected. This number sets the maximum size that can be used for the Record Length value on the main window. When Continuous Capture option is selected, the GUI will keep performing data captures and displaying the results. Clicking on the "Average FFT" option will cause the GUI to display the average results over the number of captures specified by the user in the "Number of Captures" box.

4.1.3.1 Trigger Operation

Clicking on the Trigger Option will open a new panel as shown in Figure 10. The TSW1400 provides two options of capturing data using a trigger function. Selecting "Trigger mode enable" will arm the TSW1400 to accept an external trigger. Selecting both options will allow the TSW1400 to generate a trigger pulse in addition to accepting an external trigger. One of the options is a software generated trigger.

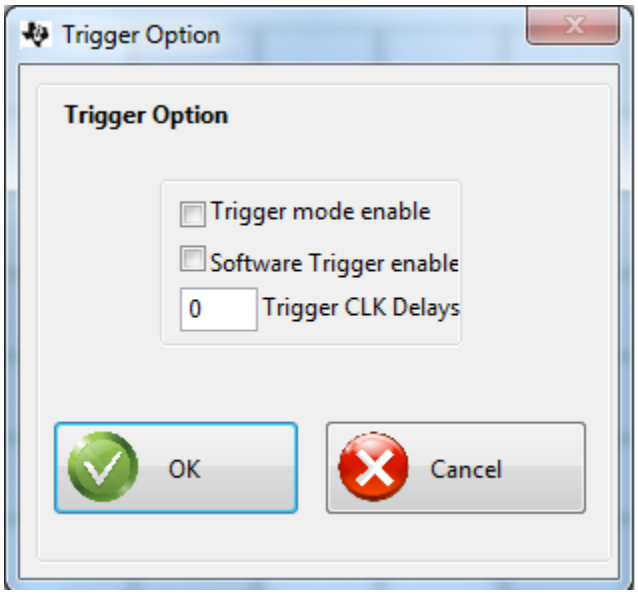

Figure 10. Trigger Option

With both enables selected, the capture button on the main panel of the GUI will now change from "Capture" to “Generate Trigger”. When the user clicks on this button, the GUI will send a CMOS logic high level (3VDC) to four SMA connectors labeled SYNC1, SYNC2, SYNC3, and SYNC4. This signal can be used to trigger other TSW1400 evm’s or the same TSW1400. To use this rising edge to trigger the same TSW1400, the user must connect a cable from the “EXT_TRG_INPUT” SMA (J11) to one of the SYNC SMA's. Without this connection, the GUI will never detect a trigger and will report “No trigger occurred” a short time after the user has clicked on the "Generate Trigger" button. Once a trigger is detected on J11, the output signal will be driven low and the GUI will do a data capture.

The other trigger option is to use an external trigger source. To use this mode, only select “Trigger mode enable”. When this mode is selected, the status button located at the bottom of the main GUI screen will display “TRIGGER ARMED”. The capture button displays “Read DDR Memory”. The software is now waiting for a CMOS logic low to high transition to occur on the “EXT_TRG_INPUT” SMA (J11). Once this occurs, a data capture will happen. The user will now click on the “Read DDR Memory” button to display the captured data. If the user clicks on this button before a trigger occurred, a “No trigger occurred” message appears. If the external trigger is a continuous event, the GUI will not do a new capture until the user does a "Read DDR Memory". This causes the software to display the results from the first trigger event and reload the memory with new data on the next rising edge of the external trigger input.

When using the trigger capture mode, the user has an option to capture data a fixed amount of samples after the capture has actually started. This is useful for devices that have a “High Resolution Burst mode”, where it takes several clock cycles to occur before valid samples are available. This delay is determined by the value entered in the “Trigger CLK Delays” box. The default value is “0”. The user can enter a value from 0-7 with the corresponding sample delay shown in Table 2. Note that the delay is also based on the number of channels captured. For example, if a user selects a Trigger Delay of “2” and is capturing data from 2 Channels, after a trigger is detected by the GUI (from a rising edge on EXT_TRIG_INPUT connector J11), the data capture starts. With this delay setting though, the first data sample used by the GUI will be the 81th sample from the ADC after the trigger occurred.

Table 2. Trigger Delay options

Trigger Delay	Number of Samples Skipped Per Channel			
	1 Channel	2 Channel	4 Channel	8 Channel
1	80	40	20	10
2	160	80	40	20
3	240	120	60	30
4	320	160	80	40
5	400	200	100	50
6	480	240	120	60
7	560	280	140	70

4.1.3.2 Using Multiple TSW1400 and ADC EVM's for Simultaneous Capture using Trigger Option

Multiple TSW1400 EVMs can connect to a single PC. To access up to four individual TSW1400 EVMs with the HSDC Pro software, use the disconnect and connect function of the HSDC Pro GUI.

- To disconnect: go to "Instrument Options > Disconnect from the Board"
- To connect: go to "Instrument Options > connect to the Board"

Before setting the trigger option, determine which evm is the master and which is the slave. In Figure 11, TIVHLO5 is the slave board and TIVHIWGZ is the master board.

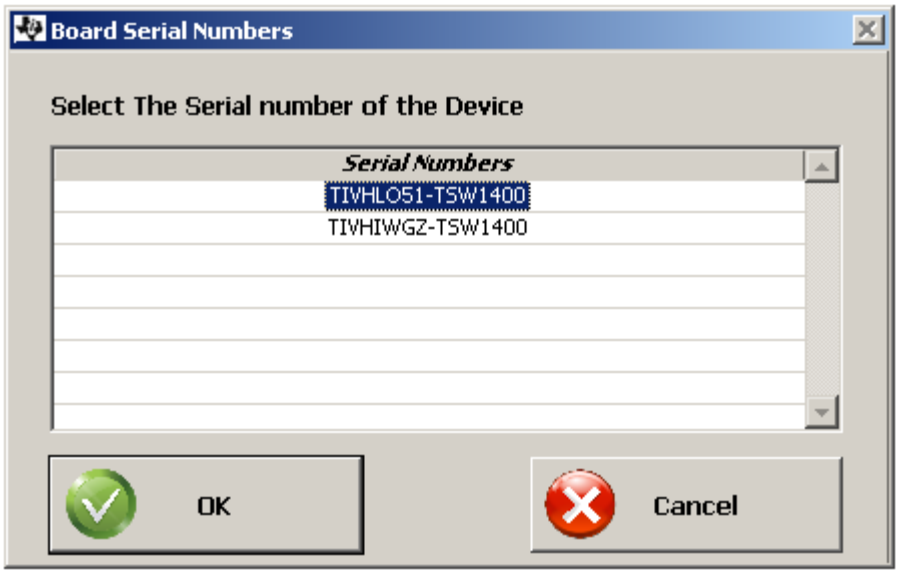

Figure 11. Two TSW1400 EVM's Connected to one PC

4.1.3.2.1 Hardware Setup

- Connect a cable from the Master TSW1400 SYNC2 (J15) to Master TSW1400 EXT_TRIG_INPUT (J11). This allows the Master TSW1400 to register its own trigger output.
- Connect a cable from the Master TSW1400 SYNC1 (J14) to the SLAVE TSW1400 EXT_TRIG_INPUT (J11). This allows the Salve TSW1400 to receive the trigger signal from the Master.

NOTE: All SYNC SMA's contain the same signal. The order does not matter. The cables of each trigger signal should have equal length to ensure the trigger signal arrives at the same time for all boards.

4.1.3.2.2 Setting up the Slave Board

With the HSDCPro GUI not connected to any of the TSW1400 boards, establish connection to the slave TSW1400. To set up the slave TSW1400 to accept a trigger signal, go to “data capture options > trigger option”.

Setup the trigger option as shown in Figure 12. This step arms the TSW1400 slave board to detect trigger signal.

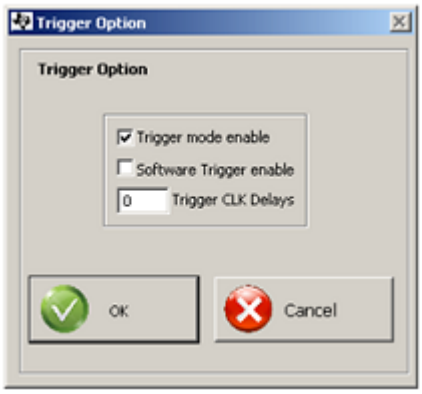

Figure 12. Slave Trigger Setup

Disconnect the TSW1400 slave board from the HSDC Pro GUI. To disconnect, go to “Instrument Options > Disconnect from the Board”.

4.1.3.2.3 Setting up the Master Board

Connect the GUI to the master TSW1400 board. To set up the master TSW1400 to generate a trigger signal, go to “data capture options > trigger option”.

Set up the trigger option as shown in Figure 13. The software trigger sends out a trigger signal upon a software GUI button press. This also arms the TSW1400 master board to register its own trigger signal. To capture data using the "Software Trigger enable" option, click on the "Generate Trigger" button on the main panel of the GUI. This will send out a pulse on the SYNC outputs. This signal, which is now connected to the EXT_TRG_INPUT of both boards, starts a capture once detected by the FPGA of each board.

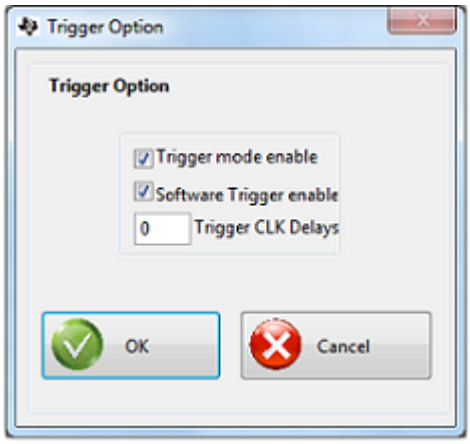

Figure 13. Master Trigger Setup

4.1.3.2.4 Read Captured Memory from the Slave Board

Disconnect the HSDC Pro from master board, and connect the software to slave. The user must select the device under test on the slave board again as the GUI does not keep track when using multiple boards.

Once the device is selected from the drag down menu, the message in Figure 14 will occur. Click OK to continue.

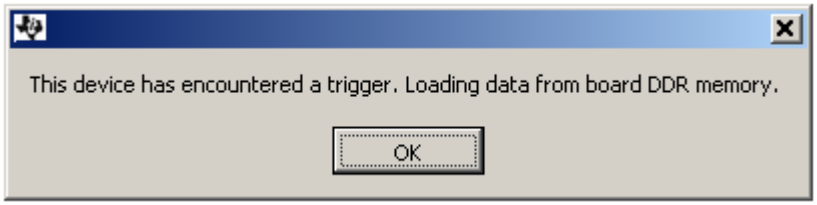

Figure 14. Trigger Confirmation Window

In the GUI main panel, be sure to enter sampling rate and target input frequency to ensure correct FFT processing. Once these values are entered, the captured data from the trigger event is displayed.

4.1.4 Test Option

The Test Option menu tab allows for setting the parameter options for the Single Tone FFT test, notch frequency bins, Cursor Locks, an option to display 2 channels, a dBFs/dBc display option and an option to turn on Bandwidth Integration Markers as shown in Figure 15.

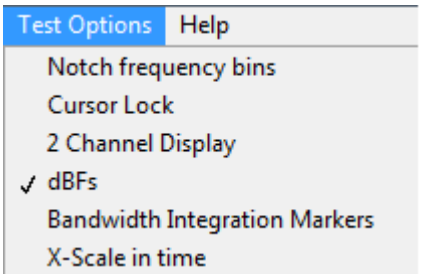

Figure 15. Test Options

4.1.4.1 dBFs

When selected, SNR, SFDR, and SINAD results are displayed in dBFs. When not selected, the results are displayed in dBc.

4.1.4.2 Notch Frequency Bins

The Notch Frequency Bins option allows the user to remove a number of bins from the SNR calculation of the input frequency around the fundamental, DC and a predetermined number of harmonics. The default values for these settings when the capture is using rectangular mode is 25, 25, 25, and 5, as shown in Figure 16. When the capture mode is set to windowing, the default values are 5, 5, 5, 5.

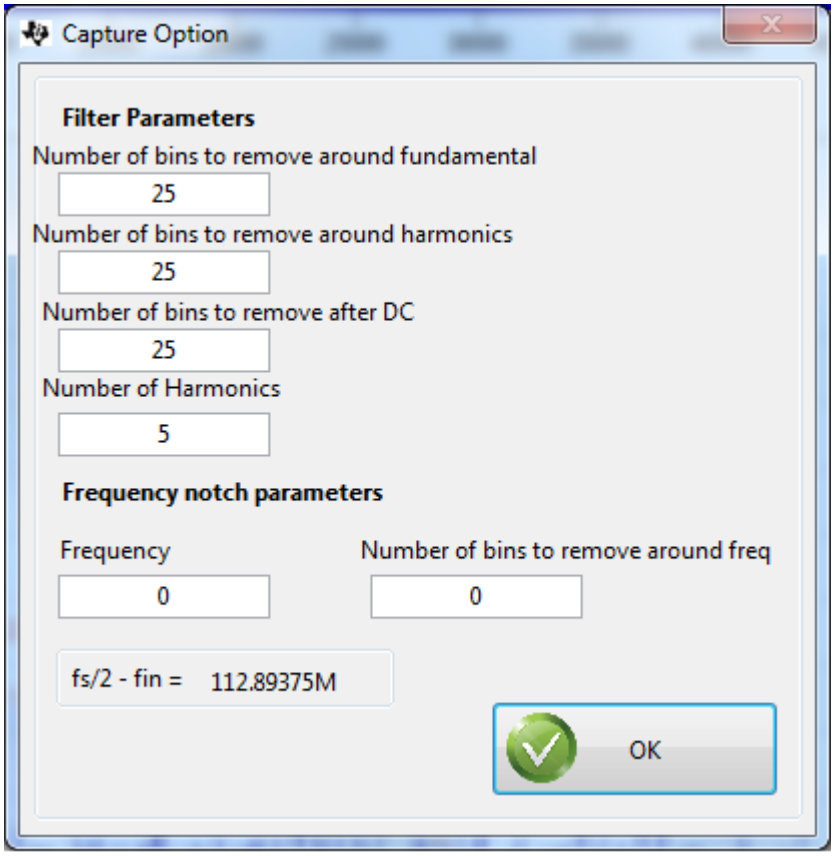

Figure 16. Notch Frequency Bin removal

By default, the noise calculations for SNR and SINAD are based on the FFT of the captured data with the Notch Filter parameters applied. The first FFT bin at DC is not used because the first bin contains DC offset and thus does not effect AC parameters or AC performance. The rest of the FFT bins out to the Nyquist frequency are included in the calculation of the total noise. There is also an option to notch out bins around a user defined frequency. The default frequency and number of bins is set to 0. If the clock input is mixing with the input signal, there may be a spur at fs/2 - fin, where fs is the ADC sample frequency and fin is the input frequency. This option could be used to notch this spur from the results if desired. If the user enters a "1" for number of bins to be removed, 1 bin will be removed at the frequency entered and one bin will be removed from each side of this frequency. If the user enters a "2", the bin at the frequency will be removed along with 2 bins on each side of the frequency, and so on. The GUI calculates this frequency for informational use only in the equation box. The default value is "0" since the default value of both fs/2 and fin is "0".

4.1.4.3 2 Channel Display and Cursor Lock

If the 2 channel display option is selected, a second data capture display window will open (Figure 17). The user can now use this window to display the same channel but a different parameter, or a different channel if a multi-channel ADC is under test. To remove the second channel display and go back to a single channel display, click on this option again to remove the selected check mark.

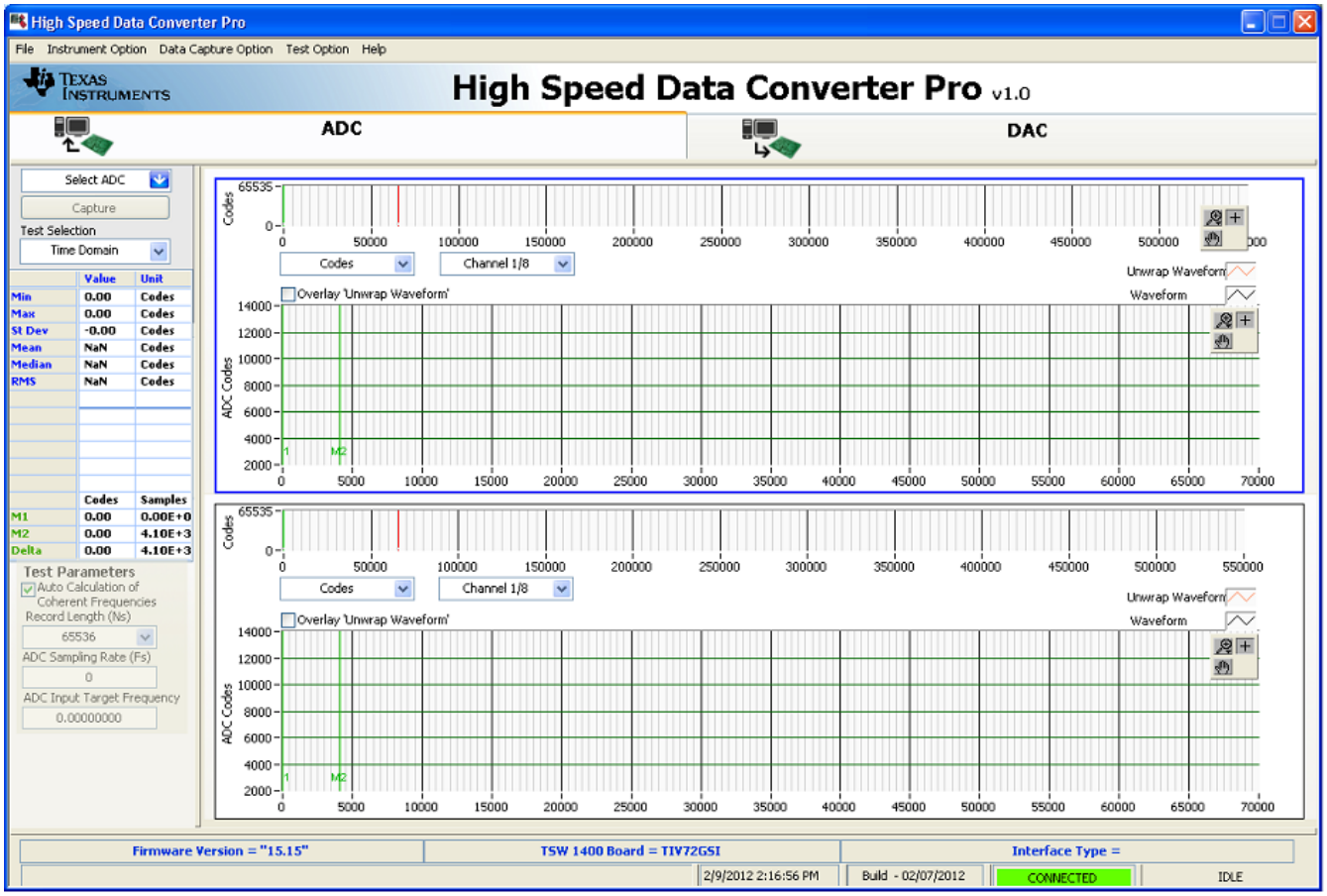

Figure 17. Two Channel Display

When 2 channels are displayed, if Cursor lock is enabled, the cursors in the lower display is locked to the ones in the upper display.

4.1.4.4 Bandwidth Integration Markers

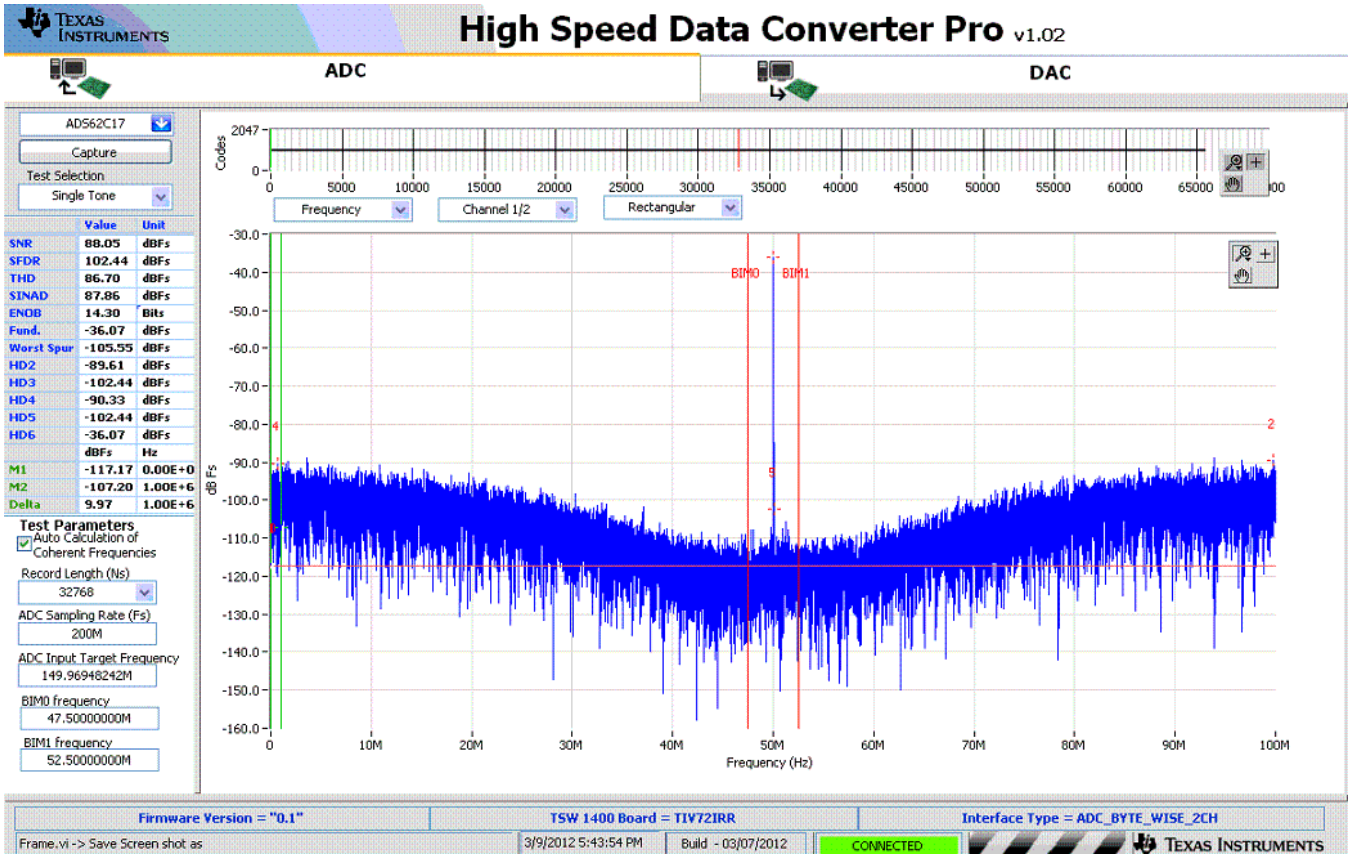

Figure 18. Bandwidth Integration Marker Example

When this option is selected, two new markers labeled BIM0 and BIM1 will appear on the FFT plot when using the GUI in Single Tone mode only. All of the calculated AC performance statistics in the left column will only use the captured values between these bandwidth markers for the calculations. The default location of marker BIM0 is at 0MHz and marker BIM1 is at ½ the ADC sample rate (Nyquist). The location of these markers can be set either by entering a frequency value (in Hertz) in the BIM0 and BIM1 location boxes located in the bottom left corner of the GUI or by clicking on the markers directly and dragging them with the computer mouse. The AC parameters update immediately after the markers have been moved. Figure 18 shows an example of the Bandwidth Integration Markers being used to display AC parameters inside a 5Mhz bandwidth window centered around a 150 MHz tone that is aliased back to the 50 MHz location in the FFT.

4.1.4.5 X-Scale in Time

When using the Time Domain option, the user can change the X-scale of the display from samples to time in µSeconds.

4.1.5 Help

Clicking on the help tab opens a window with four options. The first option, labeled "About", opens a status window displaying the current version of the GUI, the software DLL, the loaded firmware, and patch version.

The second option labeled "Debug Support", enables a debug email option. With this option enabled, if a GUI error occurs, the software prompts the user that it is emailing a debug log to a TI support team. For every subsequent error until the user disables this feature, the GUI will silently send the log file. The third option, labeled "Check for Updates", will verify if the user's GUI is the latest version available on the TI website.

The fourth option, labeled "EVM GUI Help", opens a window displaying the contents of the User's Guide, allowing the user to search for topics regarding the operation of the GUI.

4.2 Status Windows

The TSW1400 GUI reports system status such as downloading, capturing, warnings, errors, and informational output in several locations. In the lower right portion of the screen, when the GUI is loading the FPGA, loading data to memory, or performing a data capture, a rolling bar will appear in place of the IDLE message. A new window will also open in the middle of the screen describing what the GUI is currently doing. An example showing these status windows during a firmware load is shown in Figure 19.

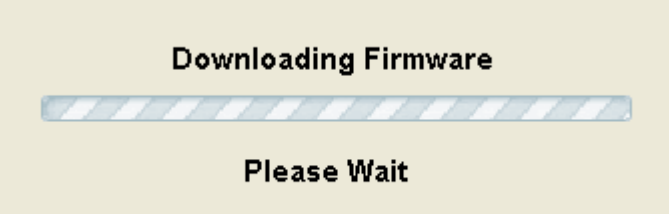

Figure 19. Status Window

During operation of the TSW1400 software, warnings may appear in the center status window if selections made from the drop-down menus of the interface are incompatible with the hardware selections or settings. For example, if a sample rate is entered that is faster than that supported by a particular ADC data sheet, a warning appears as shown in Figure 20.

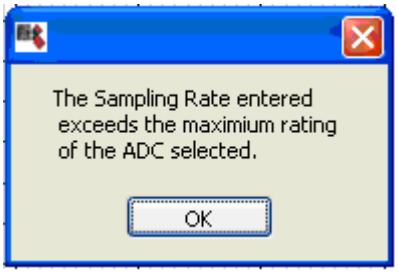

Figure 20. Center Status Window

4.3 Mode Selection

The first selection a user needs to make is to select the type of EVM that is to be tested with the TSW1400 EVM. The user will click on either the “ADC” or “DAC” button located at the top of the GUI as shown in Figure 21.

Figure 21. TSW1400 Modes

The mode selected will determine the main screen format. When ADC is selected, the GUI will be setup for displaying ADC data capture results. If DAC is selected, the GUI will setup controls to load a test pattern, create a test pattern, and display the graphical representation of the test pattern to be sent to a DAC EVM once the file has been read by the GUI.

4.4 Device Selection

After the board mode has been set, the user needs to select the device to be tested from the device selection drop-down menu. If the GUI is in ADC mode, clicking on the drop down arrow will display the ADC options available, as shown in Figure 22. If in DAC mode, the list will display available DAC's.

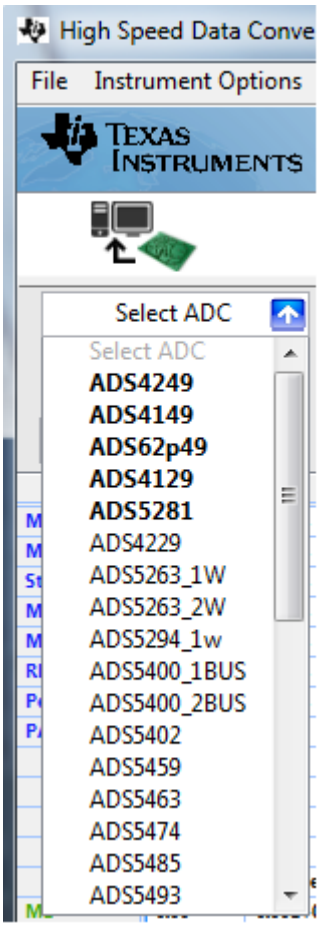

Figure 22. ADC Device Selection Window

Each device that has an ini file installed in the proper directory automatically has an entry in the device selection drop-down menu.

4.5 Capture Button (ADC Mode only)

The Capture button initiates a data capture once all other selections are made. The data capture can be a single capture and display, or a continuous repeating capture (Capture option under Data Capture Option tab in Tool Bar). When continuous capture is enabled, this button display will change from "Capture" to "Stop". Clicking on this button when in this mode will stop the continuous capture. After a captured has been issued, the GUI will store the setups currently used. If the GUI is closed and then re-opened, most of the settings will be restored if the original firmware is still present in the FPGA.

4.6 Test Selection (ADC Mode only)

The Test Selection drop-down has options for displaying data as a Time Domain, Single Tone, Two Tone, or Channel Power, as shown in Figure 23. The Single Tone FFT displays the power spectrum of the captured data with calculated AC performance statistics. Time Domain displays the raw captured data in the format of a logic analyzer display and output level over time. Two tone mode sets up cursors and displays results normally used with this type of testing. Channel Power will place cursors around the channels selected by the user (up to 5) and report the power of each.

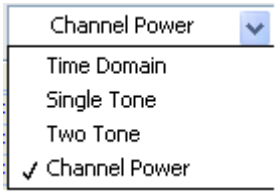

Figure 23. Test Selection Drop-Down Options

4.6.1 Single Tone FFT

The Single Tone FFT screen is shown in Figure 24. The larger central pane displays the FFT power spectrum, whereas the calculated statistics are grouped into categories on the left side of the screen. Settings and inputs relevant to the test are entered in drop-down menus or text input boxes on the bottom left portion of the window. .

The red horizontal line shown is the RMS line. This line indicates the RMS average of the noise floor of the FFT plot. The RMS average is computed over all of the FFT bins except the bin containing the input frequency. More precisely, the RMS line = SINAD + FFT Record Length Process Gain where FFT Record Process Gain = 10log(number of points/2).

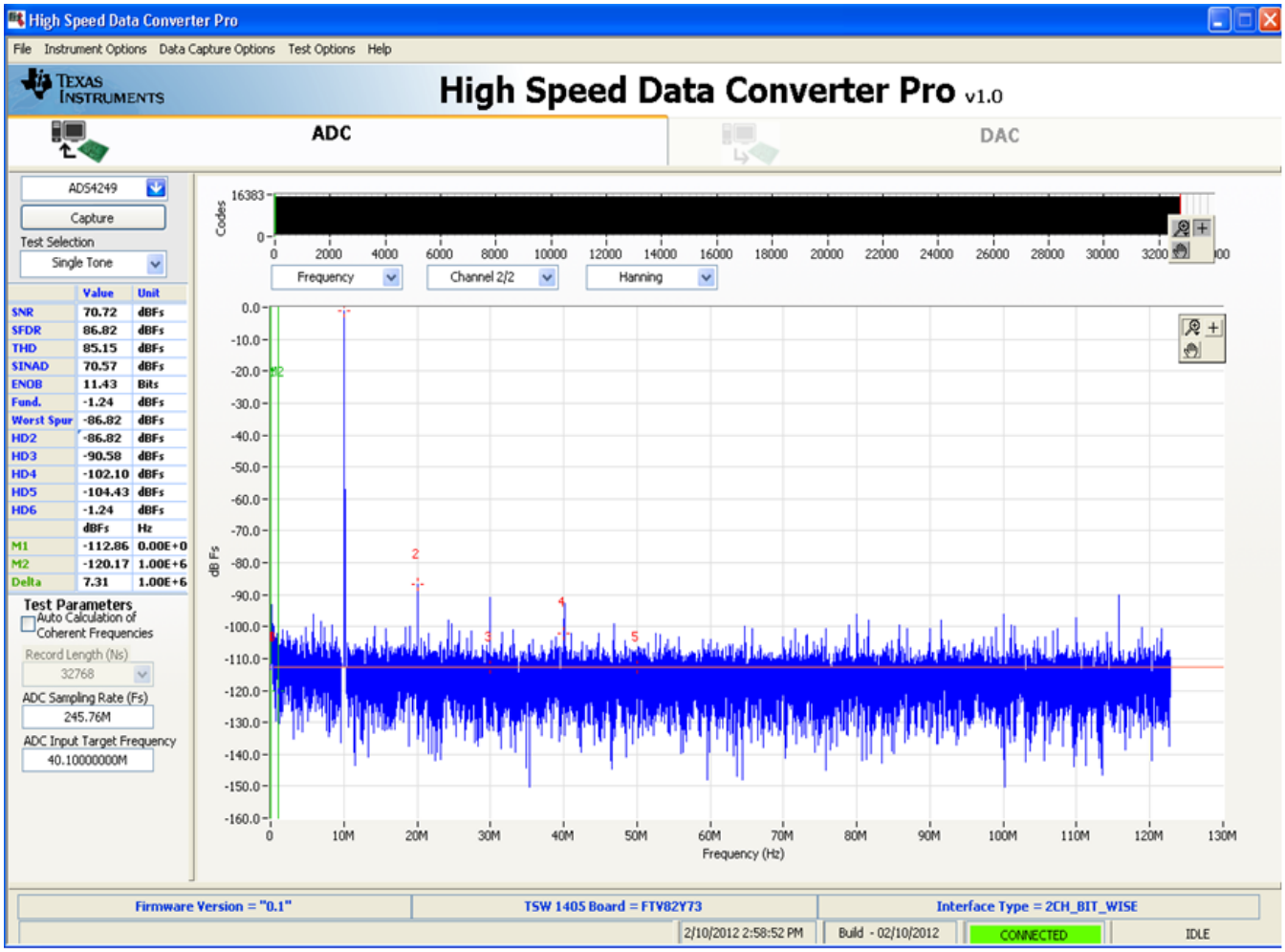

Figure 24. Single Tone FFT Display

4.6.1.1 Parameter Controls

The sampling rate is entered in the ADC Sampling Rate (Fs) text box. The number is entered in Hertz (Hz), although the letter M may be appended to represent the sampling rate in MHz. For example, 125M = 125 MHz or 125,000,000 Hz.

The expected input frequency is entered in the ADC Input Target Frequency text box. If the Auto Calculation of Coherent Input Frequency mode is enabled, then this input frequency is adjusted up or down slightly away from the input frequency automatically. If coherent input frequency is required, the signal generator used to source the input frequency must be set to this exact calculated coherent frequency. The coherent frequency calculation takes the ADC sampling rate, the input frequency as entered by the user in Hertz, and the FFT record length and adjusts the input frequency so that the captured data starts and ends on the same place of the sine wave of the input frequency. This avoids an artifact of the FFT calculation from presenting a smeared power spectrum due to the fact that the FFT presumes the sample of the input is part of a continuous input signal. If the input and sampling frequency is not coherent, and the sampled data is appended end to end to form a continuous input signal, then there is an apparent phase discontinuity at the beginning and the end of the sampled data. Making the sampling and input frequencies coherent avoids this apparent discontinuity. If the input frequency cannot be made coherent, then the windowing functions other than Rectangular can be used to process out this effect to some degree.

The FFT record length can be set in the Analysis Window (samples) text box. The TSW1400EVM supports FFT analysis lengths of as much as 524288 samples, or as little as 4096 samples. The red vertical line shown in the codes graph represents where the last sample is used from the captured data. The GUI will only allow record lengths that are the same size or smaller than the number of captured samples, which is set by the value in the capture option under the Data Capture Options tab. The default value is 65,536.

4.6.1.2 ADC Captured Data Display Pane

The ADC captured data is displayed in the major center portion of the GUI. The data display panel has three display control drop-downs. The data type drop-down allows the user to display the results as Frequency, Codes, or Bits as shown in Figure 25.

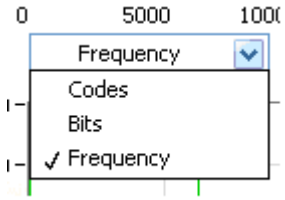

Figure 25. Data Display Options

The Codes option will display the data as actual digital codes. The Bit option will show the values of the individual ADC output bits and displayed as if it were captured by a logic analyzer.

The Channel drop-down selects which channel of a multi-channel ADC is to be displayed as shown in Figure 26.

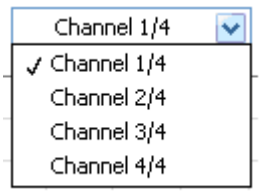

Figure 26. Channel Selection Window

When in the frequency domain mode, the GUI provides a windowing function to be applied to ADC captured data in the Window Display drop-down menu (Figure 27), Rectangular Window applies a unity gain to all data points of the captured data. A Hanning Window, Hamming Window, or Blackman-Harris Window function can be applied to the captured data for situations where the sample rate and the input frequency are not or cannot be set precisely to capture an integer number of cycles of the input frequency (sometimes called coherent frequency).

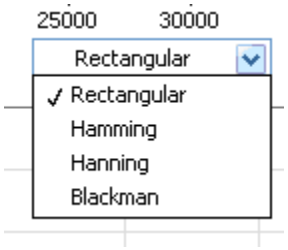

Figure 27. Data Windowing Options

4.6.1.3 FFT Power Spectrum

The FFT power spectrum of the captured data is displayed in the major center portion of the window. The TSW1400 software automatically scales the horizontal axis from DC through the Nyquist frequency, although the scale of the horizontal axis can be changed simply by highlighting the text and typing in a new value. For example, the display in Figure 24 can be used to zoom in on the input frequency by highlighting the 0 MHz at the end of the spectrum and typing 25M, and then highlighting a value at the other end and typing in 35M. This causes the portion of the power spectrum from 25 MHz through 35 MHz to fill the power spectrum display.

The vertical scale of the power spectrum is automatically scaled to display the noise floor of the FFT result up through 0 dBFS. The vertical scale can also be manually adjusted by highlighting the limits of the vertical scale and typing in new limits. By default, the first few harmonics of the input frequency are marked in the display, as well as 2 additional marker, M1 and M2, that can be placed by dragging the marker to any place in the power spectrum, such as a noise spur that is not already marked as a harmonic.

Display properties can be edited by using the mouse to right-click in the power spectrum display. Visible properties such as the graph palette or plot legend can be edited, and auto-scale of the vertical and horizontal axis's can be enabled or not. The data can also be exported to Excel or a clipboard for coping or processing.

4.6.1.4 Overlay Unwrap Waveform

When in the time domain mode, the Overlay Unwrap Waveform check box, located near the top left section of the captured display, allows a calculated normalized waveform to be overlaid (in red) over the sample data waveform (in blue). If the sample and input frequencies are coherent, the sampled data is normalized into a calculated representation of a single period of a sine wave. Errors in the sampled data for any reason become immediately apparent as spikes on the unwrapped waveform.

4.6.1.5 Single Tone FFT Statistics

For the Single FFT test, a number of calculated statistics and AC performance measurements are displayed to the left of the power spectrum display.

SNR - Signal-to-Noise Ratio is the ratio of the power of the fundamental (PS) or input frequency to the noise floor power (PN), excluding the power at DC and the first five harmonics. SNR is either given in units of dBc (dB to carrier) when the absolute power of the fundamental is used as the reference, or dBFS (dB to full scale) when the power of the fundamental is extrapolated to the converter's full-scale range.

$$SNR = 10Log10(Ps/Pn) \quad (1)$$

SFDR - Spurious-Free Dynamic Range is ratio of the power of the fundamental to the highest other spectral component (either spur or harmonic). SFDR is typically given in units of dBc (dB to carrier).

THD - Total Harmonic Distortion is the ratio of the power of the fundamental (PS) to the power in the first five harmonics (PD). THD is typically given in data sheets in units of dBc (dB to carrier).

SINAD - Signal-to-Noise and Distortion is the ratio of the power of the fundamental (PS) to the power of all the other spectral components including noise (PN) and distortion (PD), but excluding DC.

$$SINAD = 10Log10(Ps/(Pn+Pd)) \quad (2)$$

ENOB - Effective Number of Bits is a measure of a converter's performance as compared to the theoretical limit based on quantization noise.

$$ENOB = (SINAD-1.76)/6.02 \quad (3)$$

Fund. – This parameter displays the power level of the fundamental.

Worst Spur. - This parameter displays the power level of the worst spur.

HD2-6 – Display the power values of the second through sixth harmonics of the input frequency in dBc.

M1, M2, Delta – Displays the power level of the location of markers M1 and M2. These markers can be moved around on the spectrum with the mouse. The Delta parameter displays the power difference between M2 and M1.

4.6.2 Time Domain

The Time Domain option, when selected, will display the ADC captured data as digital codes in the time domain. The statistics of the codes reported on the left side of the GUI are minimum value (Min), maximum value (Max), Standard deviation (St. Dev), Mean, Median, RMS, Peak-to-Peak and PAR.

M1, M2, Delta – Displays the code value of the location of markers M1 and M2. These markers can be moved around on the display with the mouse. The Delta parameter displays the code value difference between M2 and M1.

4.6.3 Two Tone

The Two Tone option, when selected, will display a two tone ADC captured with markers placed at the locations specified by the user. The statistics of the captured data reported on the left side of the GUI are as follows:

F1 - This parameter displays the power level of the first fundamental.

F2 - This parameter displays the power level of the second fundamental.

2F1+F2 - This parameter displays the power level at the frequency that is equal to twice the first fundamental plus the second fundamental.

2F2+F1 - This parameter displays the power level at the frequency that is equal to twice the second fundamental plus the first fundamental. The other parameters follow this format.

A new window opens on the bottom left of the GUI for entering the second ADC input frequency, Figure 28.

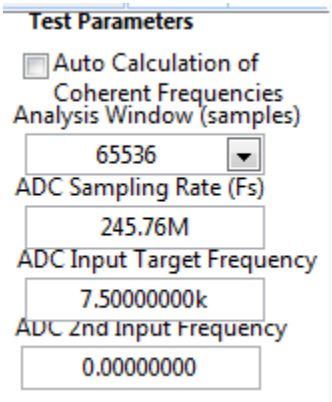

Figure 28. ADC 2nd Input Frequency Box

4.6.4 Channel Power

The Channel Power option, when selected, will display the calculated power of the channels selected in the parameter column on the left side of the GUI. This option will have three new setting windows displayed in the bottom left of the GUI for the user to select the number of channels (up to 5), the signal width, and channel separation of the captured data to be used for channel power measurements. Each channel that is selected for a power measurement will have two cursors, one labeled CxL and the other CxU. The "x" value will indicate the actual channel number. Figure 29 shows an example of a 3 channel power measurement while using the simulated ADC input function. The input test pattern is called "WCDMA_TM1_complexIF30MHZ_Fdata245.76MHZ_1000.tsw", which is located in the test files directory.

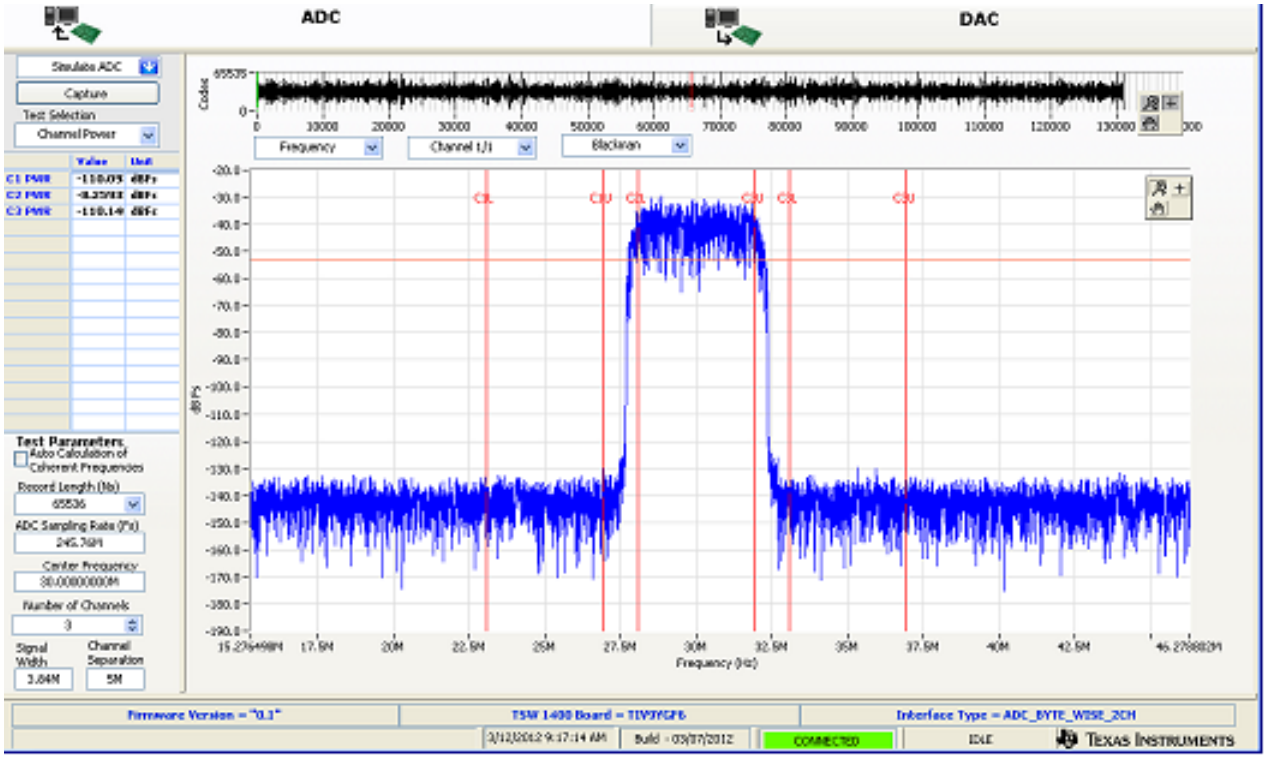

Figure 29. Three Channel Power Measurement Example

4.7 DAC Display Panel (DAC Mode only)

Selecting the “DAC” button at the top right of the GUI main panel will change the panel display mode for DAC operation as shown in Figure 30.

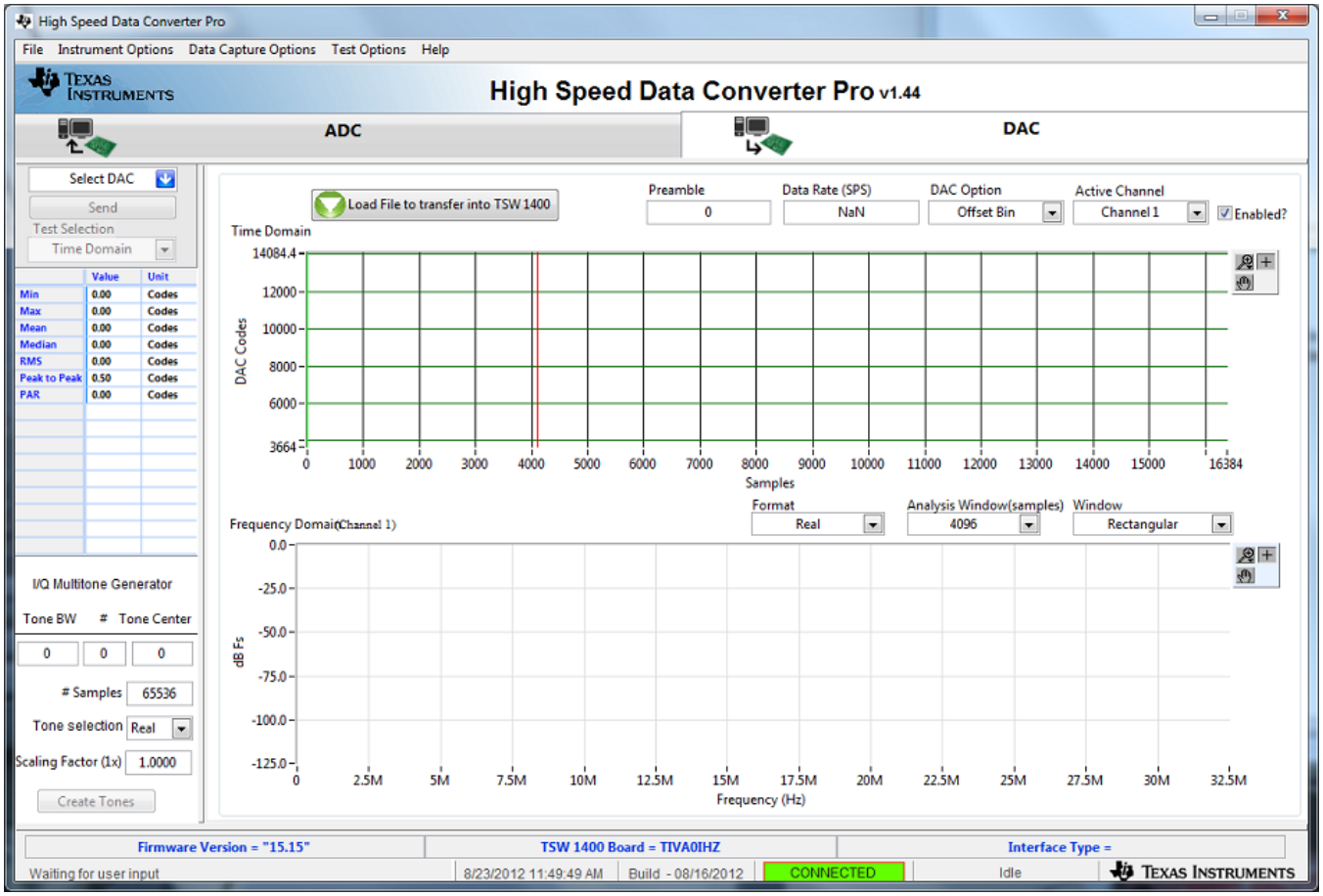

Figure 30. DAC Display Mode

4.7.1 Send Button (DAC Mode only)

This button, located in the upper left side of the GUI, causes the GUI to download data to the TSW1400 on-board memory, followed by the TSW1400 sending data from the memory module to the DAC EVM under test. This button is only active after valid data has been loaded into the PC memory by the GUI.

4.7.2 Load File to transfer into TSW1400 Button

The button labeled “Load File to transfer into TSW1400” is used to select the test pattern file to be loaded into the board memory. Clicking on this button opens a navigator which the user will use to select the desired test file. The format of the test file can be either .csv or .tsw. Once selected, the file will be loaded into the PC memory used by the GUI.

The imported file must be text format integer value from -32768 to 32767 in a single column format if testing a single DAC. For dual DAC’s, the file must be in 2 columns. For quad DAC’s, 4 columns. The length can be from 4096 to 512M (single column) in increments of 32. The GUI comes with several example test files that can be found under the following directory: C:\Program Files\Texas Instruments\High Speed Data Converter Pro\TSW1400 Details\Test files.

4.7.3 Parameter Controls

Four parameters are used with the data file to generate the Time and Frequency domain plots.

Preamble – The number of samples before the loop starting point (default is 0). This value must be in increments of 32.

Data Rate – Sample rate of I/Q samples of the test file. This is only used by the GUI FFT frequency display graph. The number is entered in Hertz (Hz), although the letter M may be appended to represent the sampling rate in MHz.

DAC Option – Determines if the test pattern file is either 2's Compliment or Offset Binary.

Active Channel – Selects the channel in the test pattern file that is displayed (1, 2, 3, or 4).

After a file has been loaded and the parameters updated, the GUI panel will present a graphical representation of the data. An example of an Offset Binary, 25.1 MHz tone with a data rate of 250 MHz is shown in Figure 31.

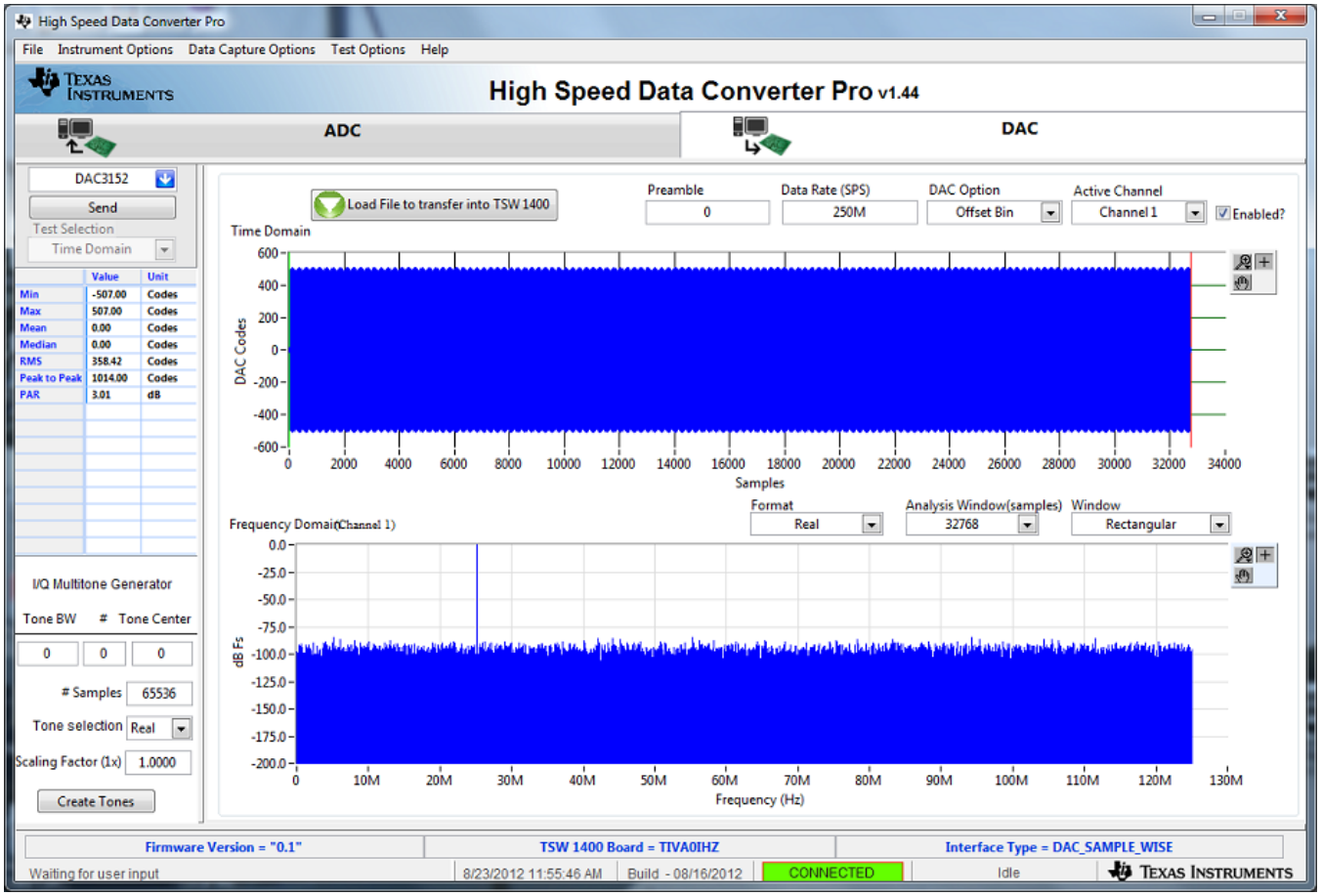

Figure 31. DAC Test Pattern Display

The “Send” button will now became active. Clicking on this button will start the transfer of data from the TSW1400 to a DAC EVM under test. This pattern is a looping test pattern that constantly runs until the send button is clicked on again.

Every time the pattern starts over, a sync pulse will be generated on the SMA labeled "SYNC4". This active high pulse width will be 8 sample clock cycles wide. The SMA labeled "SYNC3" will have a clock that is the sample rate divided by 16. These signals can be used to trigger external test equipment such as a spectrum analyzer.

4.8 I/Q Multi-tone Generator

Located in the lower left corner of the GUI is an I/Q Multi-tone Generator tool that allows the user to generate test patterns that can be used with the TSW1400 GUI. The following parameters are used with this tool:

Tone BW – Tone bandwidth in Hertz. For Megahertz, enter a "M" after the number.

- Number of tones. If set to 1, Tone BW will be ignored.

Tone Center – Center frequency of tones in Hertz.

# of Samples – Number of test samples. 4096 to 2M, in increments of 32.

Tone Selection – Real or I/Q.

Scaling Factor (1X) – From full scale output. 0.0000 to 1.0000.

To generate a pattern, enter the desired parameters then click on the button labeled “Create Tones”. Click on “Send” will send the data to the TSW1400 memory then to the DAC EVM under test. An option exist to allow the user to save this file as well.

5 ADC Data Capture Software Operation

5.1 Testing with an ADS5281 EVM

This section describes the operation when testing with an ADS5281 EVM that has a LVDS output interface.

- Power down the TSW1400 if an ADC evm is not installed.
- Connect J8 of the ADS5281 EVM to connector J3 of the TSW1400.
- Provide unpowered +5 VDC connections to J1 and return to J2 of the ADS5281 EVM.
- Provide a 1.5 V*PP* 40 MHz sine-wave clock to J26 of the ADS5281 EVM.
- Provide a filter 5.1 MHz analog input to CH1.
- Power up the TSW1400 followed by the ADC evm.
- Start up the TSW1400 GUI as described in the Software Start Up section.
- The TSW1400 EVM connected to an ADS5281 EVM is shown in Figure 32

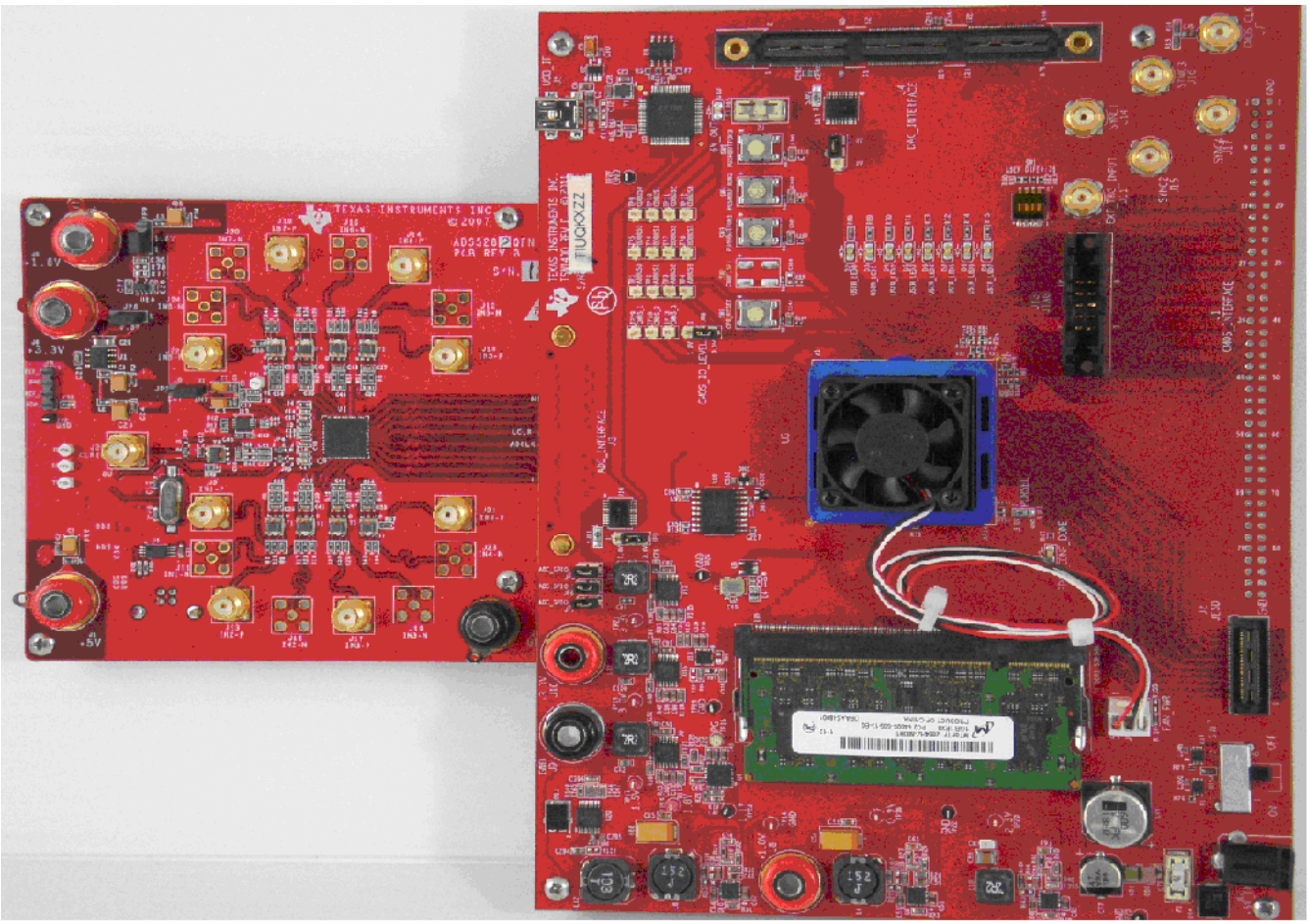

Figure 32. TSW1400EVM interfacing to an ADS5281 EVM

To setup the GUI to run in the data capture mode, click on the “ADC” tab in the top left side of the GUI. Navigate to the device selection button located in the upper left side of the GUI, click on the drop down arrow, then select “ADS5281”. After double clicking on this file, a pop-up will open asking “Do you want to update the Firmware for ADC”. Click on “Yes”. The firmware will now start loading and take ~ 20 seconds to complete. After the ADS5281 firmware load has completed, the FPGA_CONF_DONE LED will turn on after the FPGA configured. The LED’s labeled USER_LED (0-7) will also be on except for USER_LED4.

NOTE: If the TSW1400 is not receiving a valid clock from the ADC EVM, USER_LED3 will be off.

- Use the “Test Selection” button to change the capture display to Single Tone.
- Set the active channel setting to Channel 1/8.
- Use the default Record Length value of 65,536.
- Set the ADC Sampling Rate to 40 MHz.
- Click on the Auto Calculation of Coherent Frequency function and Rectangular capture mode if using a coherent input frequency. Otherwise, do not set this and use "Blackman" windowing mode.
- Set the input frequency source to the new value in ADC Input Target Frequency that is generated by the Auto Calculation of Coherent Frequency function.
- Make sure the display mode is set to “Frequency”.
- Click on the “Capture” button to perform a data capture. The results should like similar to those shown in Figure 33.

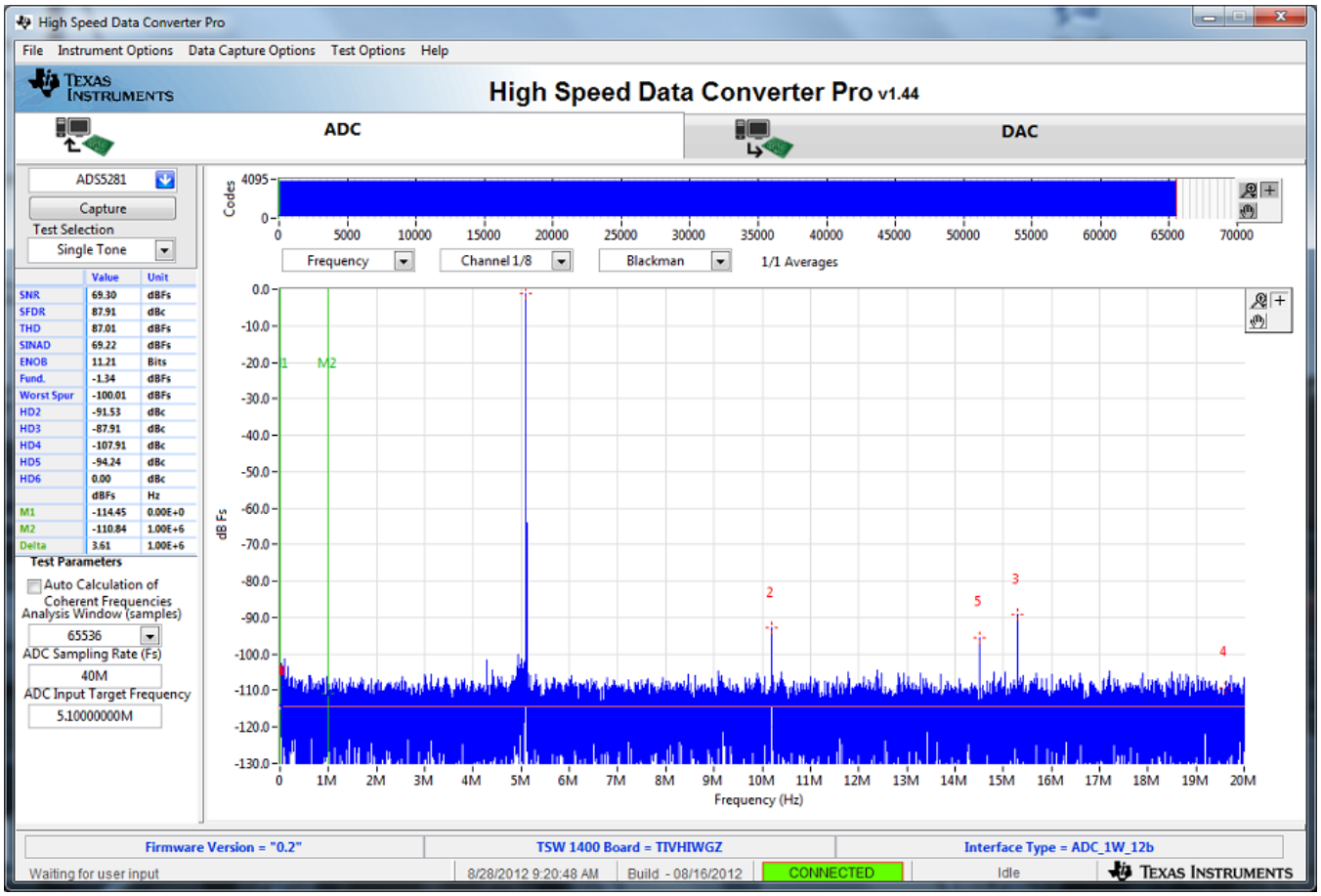

Figure 33. ADC5281 Single Tone FFT Capture Results

The user can now change other parameters and do another capture to observe the ADC outputs with different frequencies, amplitudes, and in other formats such as codes, or bits.

After the firmware is loaded, if the user clicks the drop down arrow in the device selection window, the GUI will indicate which ADC EVM's can be used with this firmware load by adding a black diamond in front of the device name, as shown in Figure 34. If the user does not power down the TSW1400, any one of the devices with a black diamond can be tested without doing another firmware load.

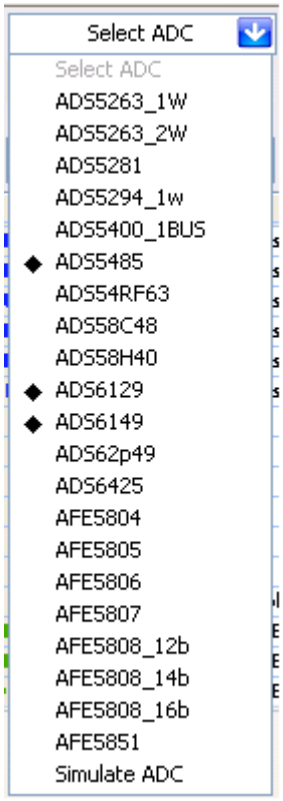

Figure 34. Devices Supported with Current GUI

WARNING

After testing is completed, always close the GUI before disconnecting the USB cable between the host PC and EVM. Failure to do this can cause a blue screen reboot to occur on the host PC.

5.2 Testing with an ADS62P49EVM CMOS Interface

This section describes the operation when testing with an ADS62P49EVM that is configured for CMOS output interface.

- Power down the TSW1400 if an ADC evm is not installed.
- Connect J1 and J2 of the ADS62P49EVM to connector J1 of the TSW1400EVM.

NOTE: Pin 1 of the TSW1400 connector plugs into pin 39 of J1 on the ADS62P49EVM.

- Provide unpowered +5 VDC connections to J10 and return to J12 of the ADS62P49EVM.
- Provide a 1.5 V_{PP} 150 MHz sine-wave clock to J19 of the ADS62P49EVM. Make sure this clock is within the frequency limits specified in the data sheet when operating in CMOS mode.
- Provide a filtered 5.1 MHz analog input to CH1 (J6).
- Power up the TSW1400 followed by the ADC EVM.
- Setup the ADS62P49EVM to operate in parallel mode, offset binary parallel CMOS output, and internal reference.
- Start up the TSW1400 GUI as described in the Software Start Up section.

- The TSW1400 EVM connected to the CMOS connectors of the ADS62P49EVM is shown in Figure 35

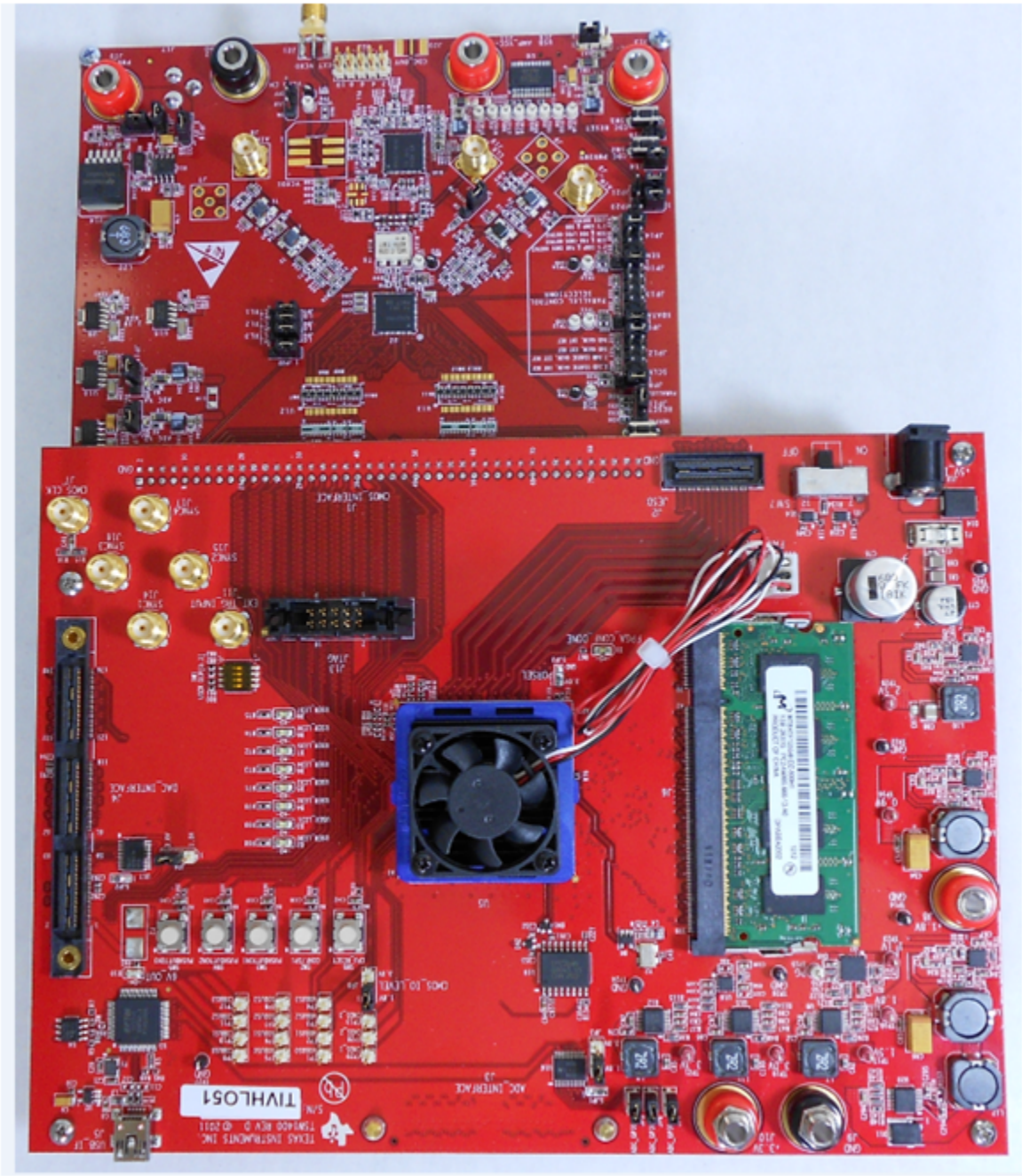

Figure 35. TSW1400EVM interfacing to the CMOS connectors of an ADS62P49EVM

To setup the GUI to run in the data capture mode, click on the “ADC” tab in the top left side of the GUI. Navigate to the device selection button located in the upper left side of the GUI, click on the drop down arrow, then select “ADS62p49_cmos”. After double clicking on this file, a pop-up will open asking “Do you want to update the Firmware for ADC”. Click on “Yes”. The firmware starts loading which takes approximately 20 seconds to complete. After the firmware load has completed, the FPGA_CONF_DONE LED turns on after the FPGA is configured. The LED’s labeled USER_LED (0-7) should now all be on.

NOTE: If the TSW1400 is not receiving a valid clock from the ADC EVM, USER_LED3 and USER_LED4 will be off.

- Use the “Test Selection” button to change the capture display to Single Tone.
- Set the active channel setting to Channel 1/2.
- Use the default Record Length value of 65,536.
- Set the ADC Sampling Rate to 150 MHz.
- Click on the Auto Calculation of Coherent Frequency function and Rectangular capture mode if using a coherent input frequency. Otherwise, do not set this and use "Blackman" windowing mode.
- Set the input frequency source to the new value in ADC Input Target Frequency that is generated by the Auto Calculation of Coherent Frequency function.
- Make sure the display mode is set to “Frequency”.
- Click on the “Capture” button to perform a data capture. The results should like similar to those shown in Figure 36

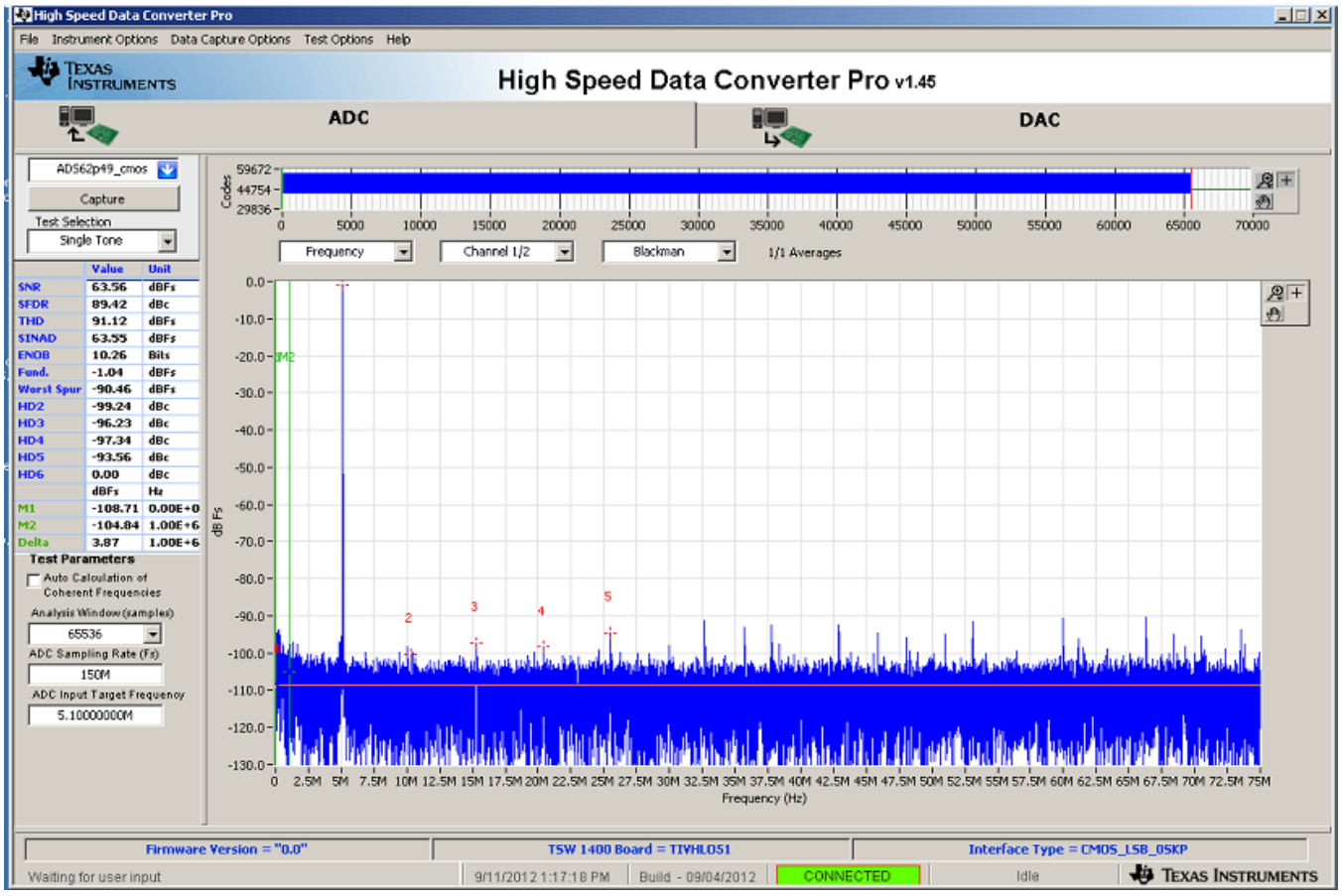

Figure 36. TSW1400EVM Captured Results from ADS62P49EVM

6 TSW1400 Pattern Generator Operation

6.1 Testing with DAC3152 EVM

This section describes the pattern generator operation when testing with a DAC3152 EVM that has a LVDS input interface.

- Power down the TSW1400.
- Connect J5 of the DAC3152 EVM to connector J4 of the TSW1400.
- Provide +5 VDC to J12 and return to J13 of the DAC3152 EVM.
- Provide a 0.5-Vrms 250 MHz clock to J9 of the DAC3152 EVM.
- Power up the TSW1400 EVM
- Start up the TSW1400 GUI as described in the Software Start Up.
- A TSW1400 EVM connected to a DAC3152 EVM is shown in Figure 37.

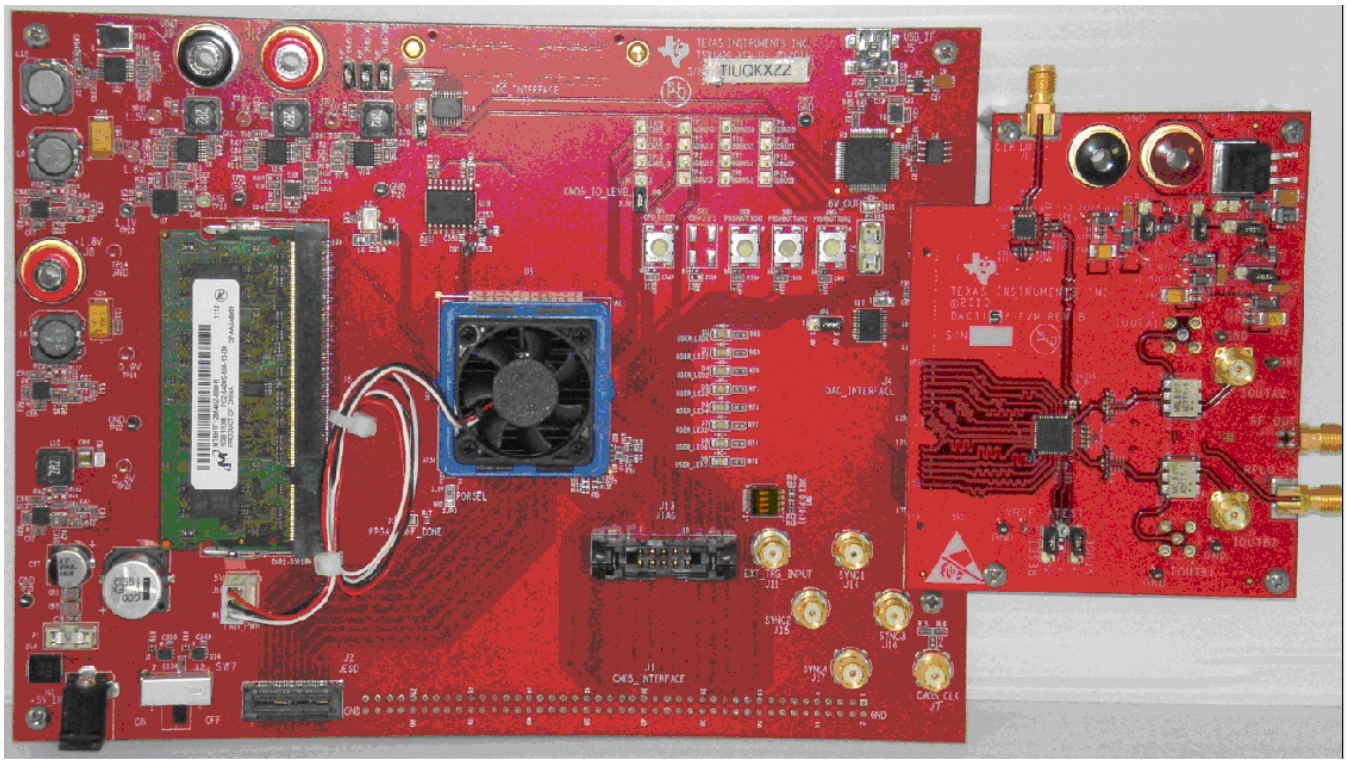

Figure 37. TSW1400 EVM Interfacing to a DAC EVM

NOTE: The FPGA clocks from DAC EVM's to the TSW1400 EVM have to be LVDS level. Exceeding LVDS levels may damage the TSW1400 FPGA.

6.2 Loading DAC Firmware

If opening the GUI for the first time, when setting up for pattern generator mode, make sure "DAC" in the top right side of the GUI is selected. After clicking on "DAC", the top level GUI shall look as shown in Figure 38.

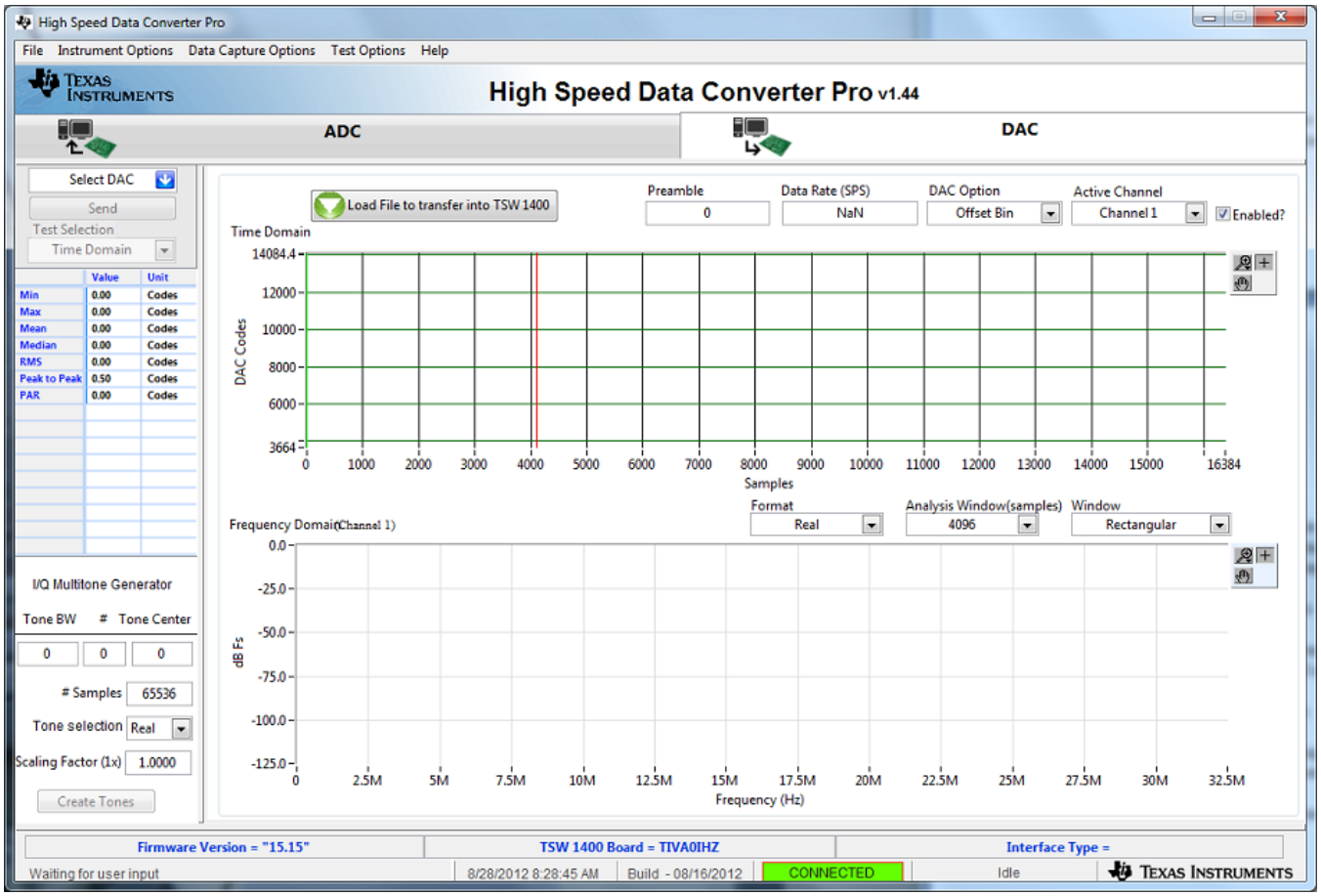

Figure 38. TSW1400EVM GUI DAC Mode Top Level

To run the GUI in DAC pattern generator mode, the FPGA must be loaded with the proper firmware, which is determined by the DAC type to be tested.

In the “Select DAC” button of the GUI, click on the drop down arrow and select the DAC3152 (Figure 39). This will be the targeted EVM for this test example.

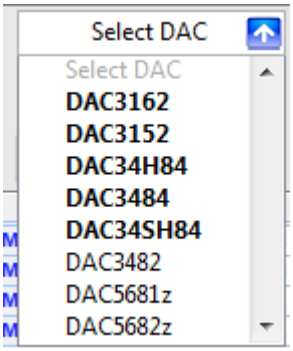

Figure 39. DAC Selection

Click on “Yes” when asked “Do you want to update the firmware for DAC”. The firmware for this setup will now be loaded during this process, which will take approximately 20 seconds. After the firmware load has completed, the LED’s labeled USER_LED (0-7) will now turn on except for USER_LED 3 and 5. USER_LED 3 is used to indicate the status of a second PLL, which is not used with this firmware build, and USER_LED 5 indicates if there is a FIFO overflow (error) of the transmit data.

NOTE: If the TSW1400 is not receiving a valid clock from the DAC evm, USER_LED3 and USER_LED4 will be off.

6.3 Configuring TSW1400 for Pattern Generation

For this test, at the top of the GUI, set the following parameters:

- Preamble to 0
- Data Rate – 250 MSPS
- DAC Option – Offset Binary
- Active Channel – Channel 1
- FFT Length – 32768
- Window - Rectangular

The pattern generation data file should match one of the Record Length's to us the Rectangular window mode. If it does not, switch the window mode to another setting such as "Hanning".

- Click on the button labeled "Load File to transfer into TSW1400".
- Select "single_tone_cmplx_32768_250MSPS_BW_25.1MHZ.csv".
- Click on "Send".

The display panel of the GUI will be updated, showing the test data that will be transmitted to the DAC EVM in both codes and frequency domain as shown in Figure 40.

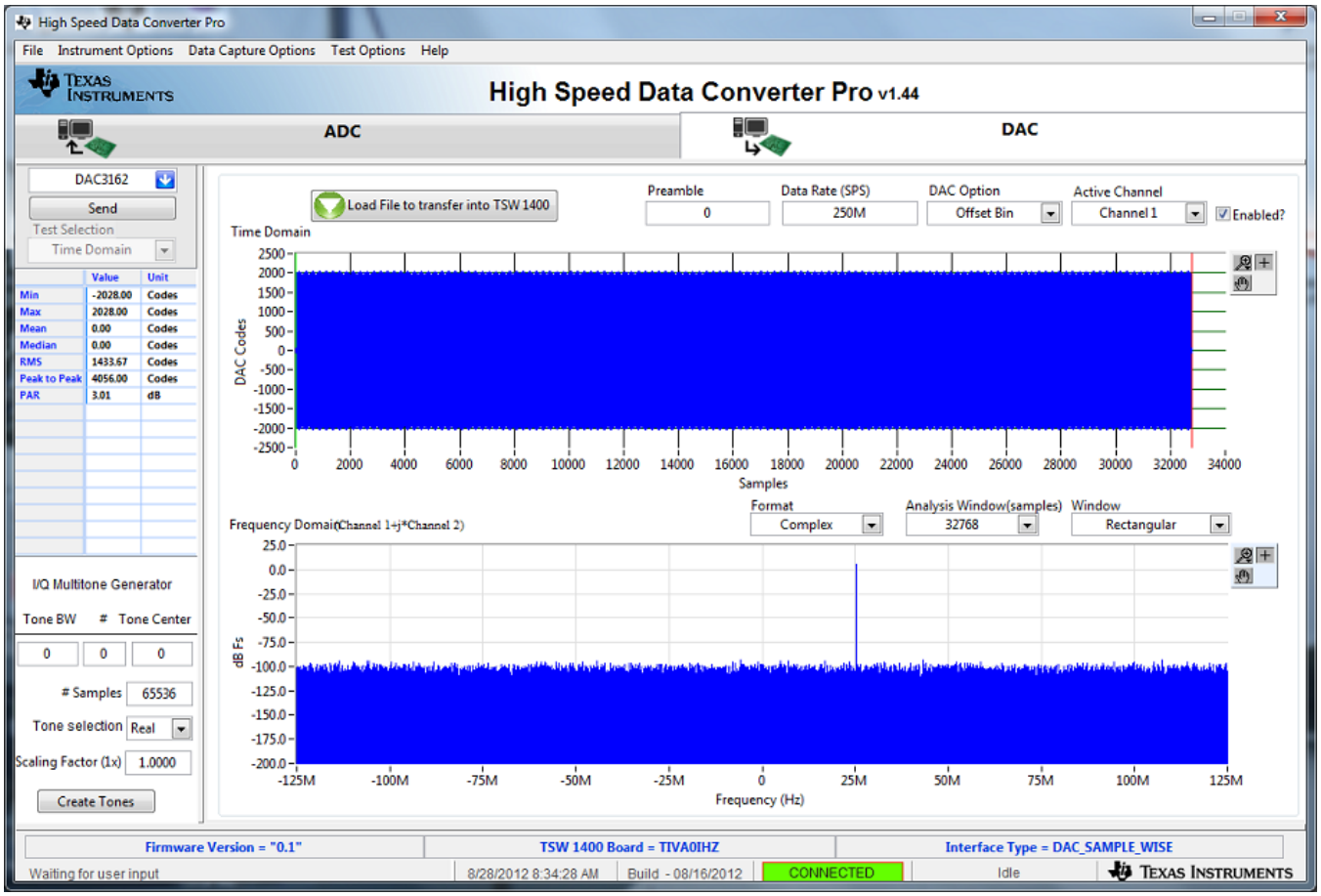

Figure 40. TSW1400 Output Data to DAC EVM

Using a spectrum analyzer, verify that there is now a 25.1 MHz tone present on both SMA J2 (IOUTA2) and J3 (IOUTB2) of the DAC3152 EVM.

To shut down the GUI, click on the “File” tab in the upper right corner of the GUI and select “Exit” in the pop up window that opens. This will specify that the USB ports are released by the software.

6.4 Testing with a DAC5688EVM CMOS Interface

This section describes the operation when testing with a DAC5688EVM that has a CMOS input interface.

- Power down the TSW1400 if the DAC5688EVM is not installed.

NOTE: J1 pin 1 of the TSW1400 connector plugs into J2 pin 1 on the DAC5688EVM

- Provide unpowered +3.3 VDC connections to J15 and return to J16 of the DAC5688EVM.
- Provide unpowered +1.8 VDC connections to J13 and return to J14 of the DAC5688EVM.
- Provide a USB cable between the DAC5688EVM and a host PC.
- Provide an external sinewave source at 491.52 MHz with a 1-Vrms, 0-V offset to SMA J20 (EXT_VCXO) of the DAC5688EVM.
- Connect a SMA cable from OUTCLK3 connector (J17) of the DAC5688EVM to CMOS_CLK (J7) of the TSW1400EVM.
- Power up the TSW1400 followed by the DAC evm.
- Load and start up the DAC5688EVM GUI as described in the DAC5688EVM User’s Guide. The software and User’s Guide can be found at http://www.ti.com/tool/dac5688evm.
- Start up the TSW1400 GUI as described in the Software Start Up section.
- The TSW1400EVM connected to the CMOS connectors of the DAC5688EVM is shown in Figure 41

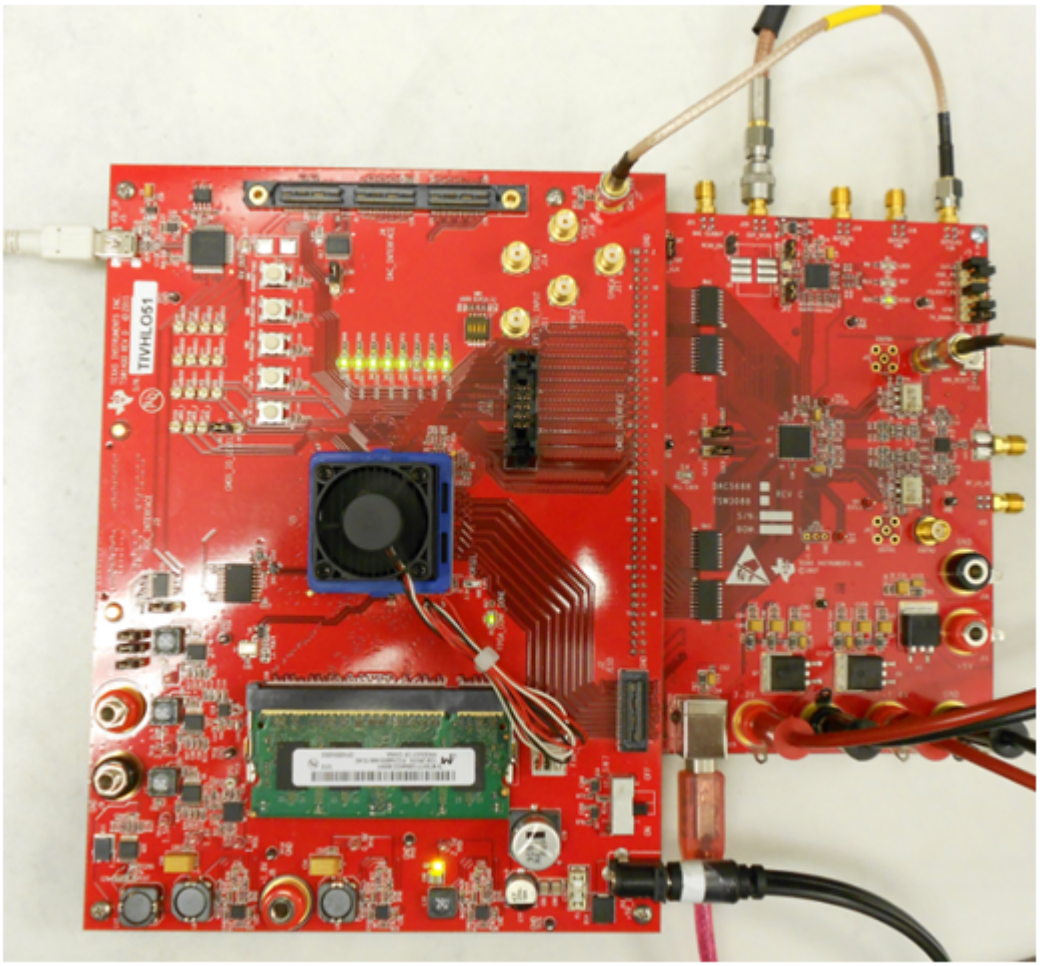

Figure 41. TSW1400EVM Interfacing to the CMOS Connectors of a DAC5688EVM

Using the DAC5688EVM GUI, load the EVM with the test file called “example”. This can be found at C:\Program Files\Texas Instruments\DAC5688\DAC5688 Configuration Files. This sets up the DAC5688 to receive a WCDMA test pattern from the TSW1400 with a data rate of 122.88MHz. CLK2 of DAC5688 operates at 491.52 MHz and the DAC interpolation is set to 4x, requiring the input data rate to be at 122.88MHz.

In the DAC5688 GUI, go to the CDCM7005 tab and set the Y3 Output (OUTCLK3) to divide by 4, LVCMOS, and inverting per Figure 42.

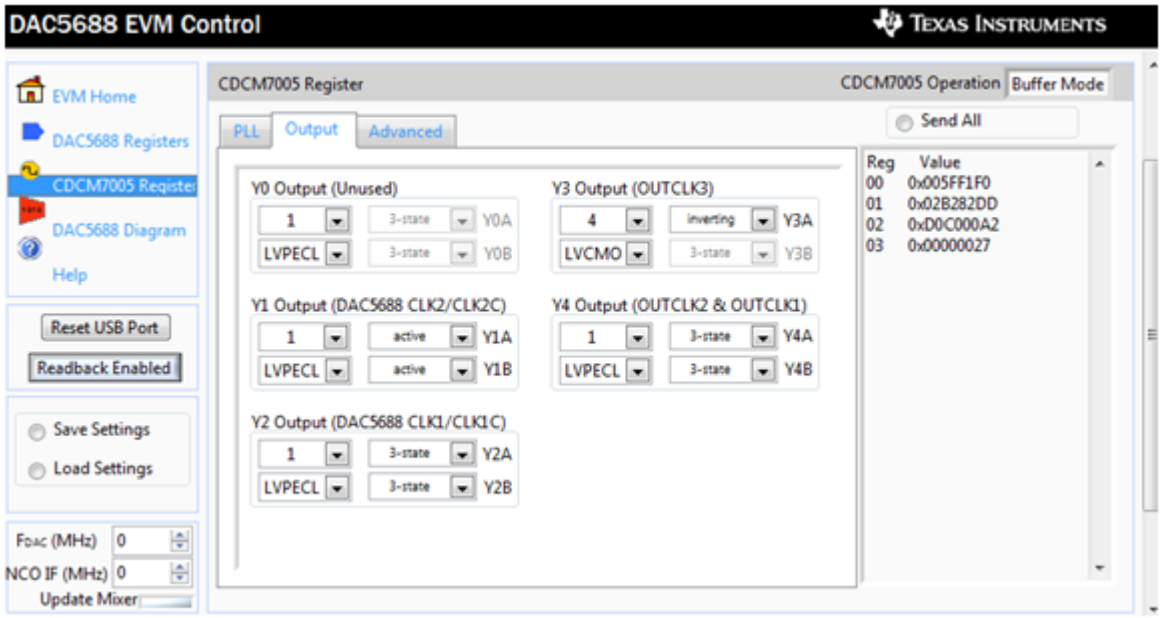

Figure 42. CDCM7005 tab on DAC5688 GUI

This generates an inverted 122.88MHz clock used by the TSW1400 to generate the CMOS test pattern.

NOTE: The CMOS data rate for the TSW1400EVM should never exceed 250 MHz. This rate is set by the CMOS_CLOCK input provide to J7. When operating at frequencies near this limit, the user may need to adjust the delay of this signal to meet the timing specs of the DAC under test.

On the DAC5688EVM, there is an option to use a spare output of the CDCM7005 clock generator as a clock source. In this example, the OUTCLK3 of the CDCM7005 is inverted for optimized setup and hold time. Another way to adjust the delay is to use different cable lengths for this clock source.

If opening the TSW1400 GUI for the first time, when setting up for pattern generator mode, make sure “DAC” in the top right side of the GUI is selected. This targets the EVM for this test example. In the “Select DAC” button of the GUI, click on the drop down arrow and select “cmos”. This firmware is used by most High Speed CMOS DAC EVM’s.

Click on “Yes” when asked “Do you want to update the firmware for DAC”. The firmware setup is loaded during this process, which takes approximately 20 seconds. After the firmware load has completed, the LED’s labeled USER_LED (0-7) will now turn on except for USER_LED 5. USER_LED 3 is used to indicate the status of a second PLL, and USER_LED 5 indicates if there is a FIFO overflow (error) of the transmit data.

NOTE: If the TSW1400 is not receiving a valid clock from the DAC EVM, USER_LED3 and USER_LED4 are off.

6.4.1 For this test, at the top of the GUI, set the following parameters:

- Preamble to 0
- Data Rate – 122.88M (MSPS)
- DAC Option – 2's Comp
- Active Channel – Channel 1
- Click on the button labeled "Load File to transfer into TSW1400".
- Select "WCDMA_TM1_complexIF30MHz_Fdata122.88MHz_1000.csv".
- Click on "Send".

The display panel of the GUI is updated, showing the test data that is transmitted to the DAC EVM in both codes and frequency domain as shown in Figure 43.

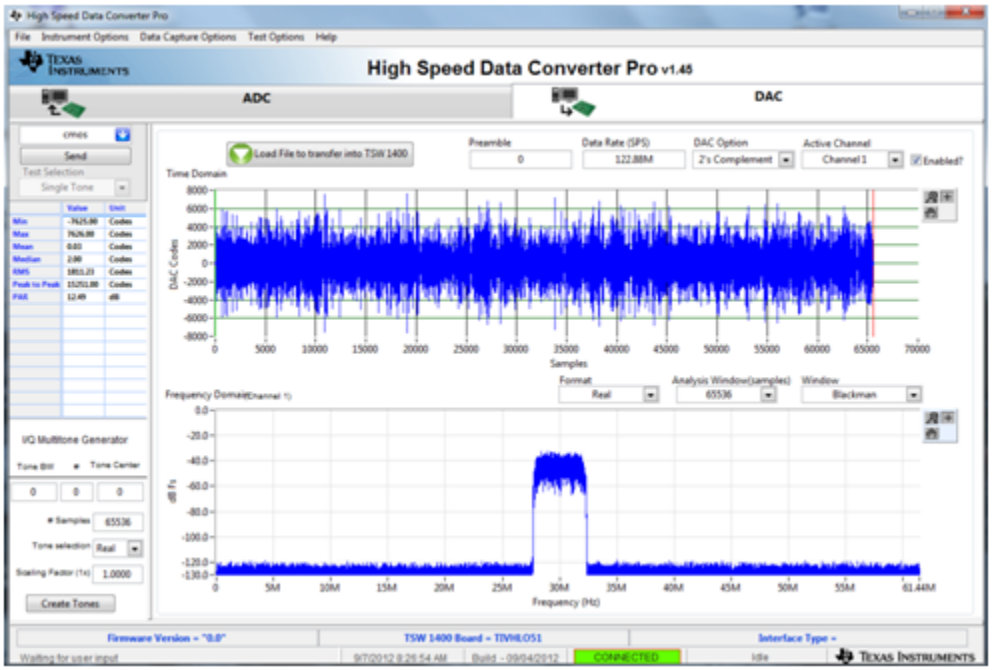

Figure 43. GUI After Test File Loaded

If the DAC5688EVM is configured for IF output, connect a spectrum analyzer to either SMA J4 (IOUTB2) or J9 (IOUTA2) of the EVM. The DAC example file has a NCO setting of 61.44 MHz and the test pattern IF is centered at 30 MHz. The signal should be a single carrier centered around 91.44 MHz, as shown in Figure 44.

NOTE: The DAC5688EVM has the default setup as RF output. The modulator output location will be at the LO frequency plus 91.44 MHz. For details about IF and RF output configuration settings, see section 4.7 of the DAC5688EVM User's Guide (SLAU241).

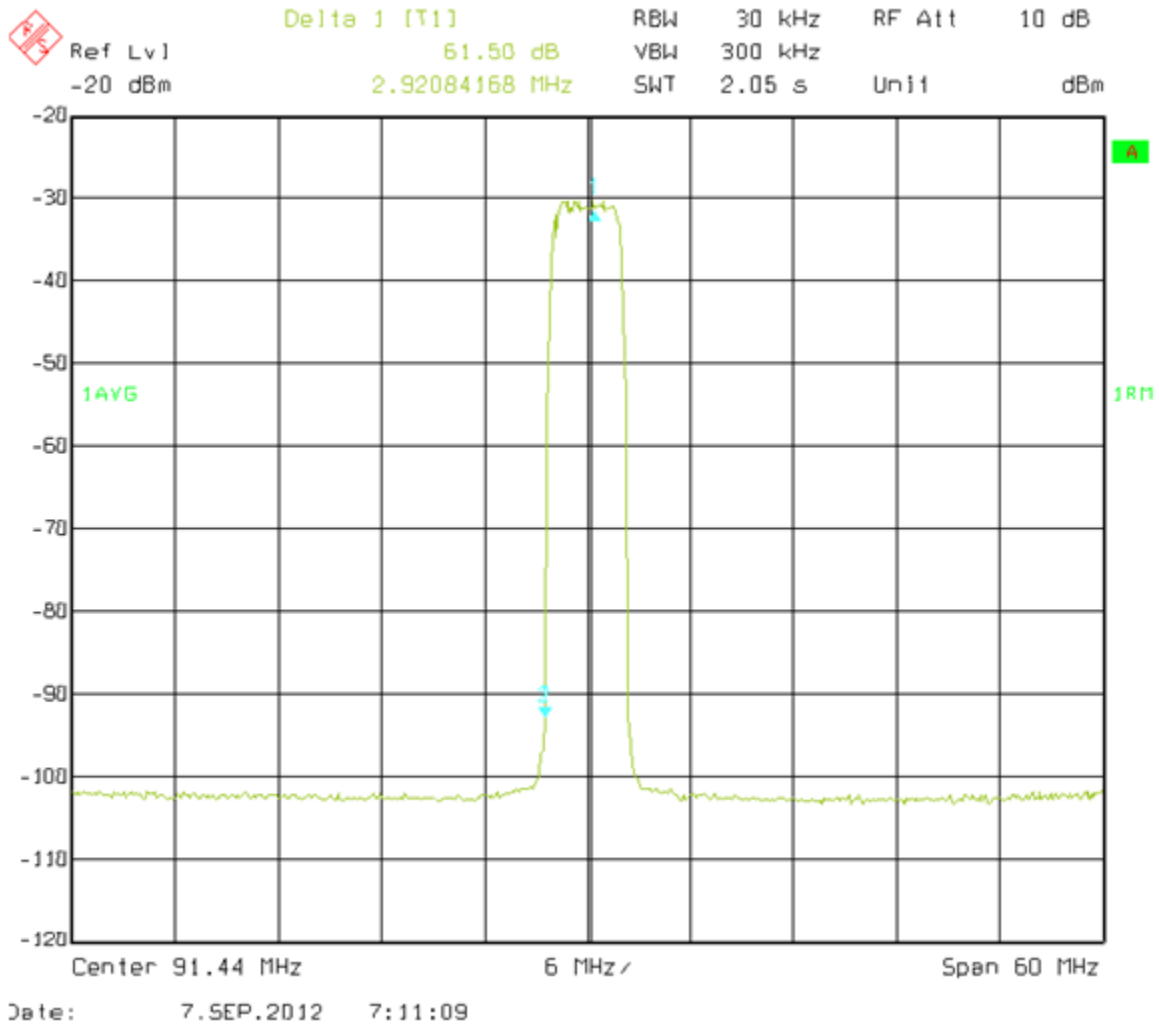

Figure 44. DAC5688 IF Output

7 TSW1405 Functional Description

The TSW1405 Capture Card is a lower cost capture card than the TSW1400, with reduced memory capacity for storing samples captured from TI High Speed ADC EVMs. The TSW1405 has a Samtec connector to directly connect to the LVDS data bus from the EVM. The TSW1400 does not have connections for CMOS ADC EVMs. The TSW1405 uses the same software GUI as the TSW1400.

The TSW1405 does not have an EEPROM resident on the board to hold an FPGA bit file, but rather will get the bit file downloaded from the software GUI running on a PC at runtime. In this manner the TSW1405 will not need to be reprogrammed when new ADC EVMs or additional capture features become available. The planned FPGA firmware upgrades consists of new files to be downloaded to the software GUI. The TSW1405 does have a footprint for a firmware EEPROM to be installed, if desired.

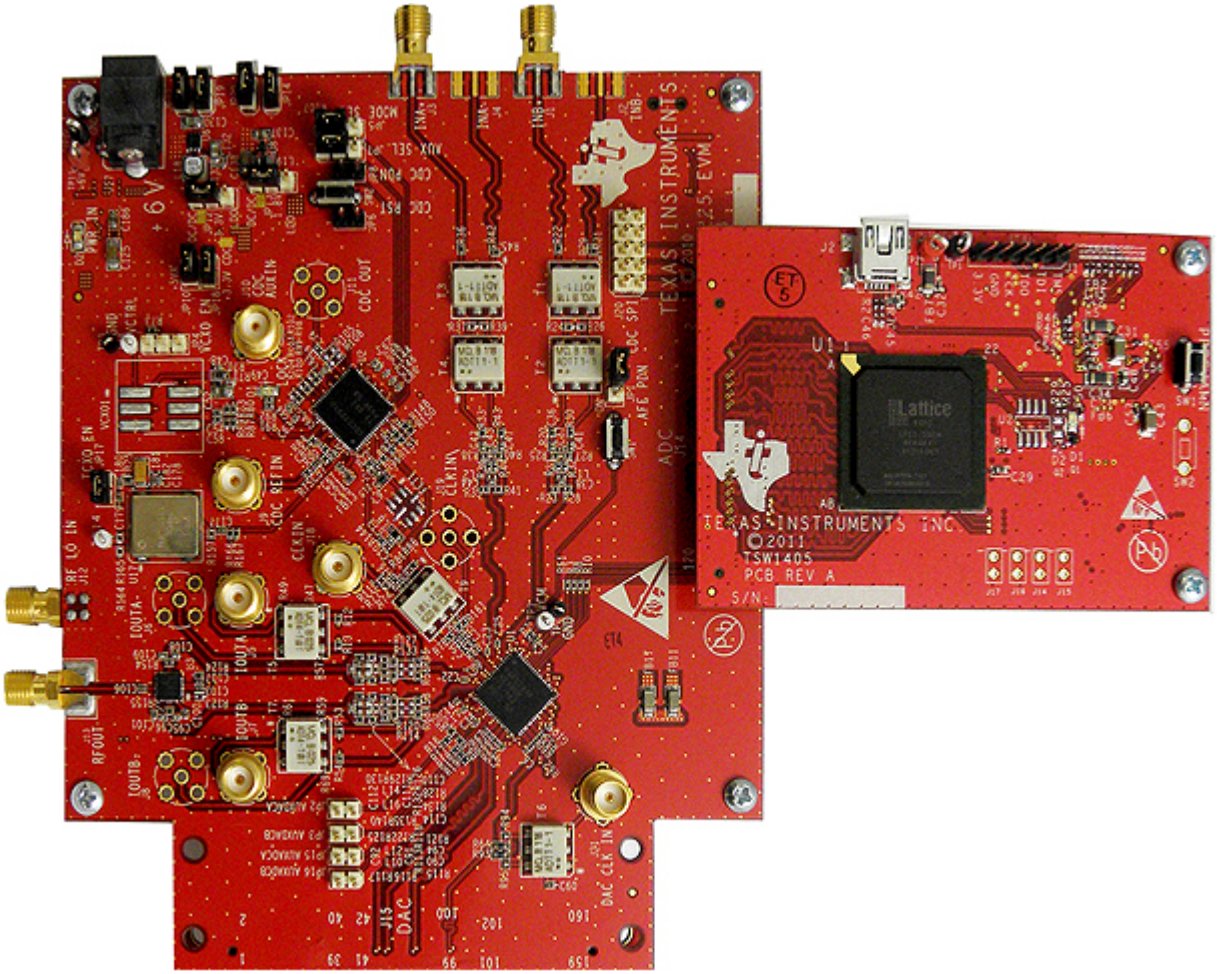

Figure 45. TSW1405EVM Connected to the ADC Output of the AFE7225EVM

7.1 Hardware Description

7.1.1 Power Connections

The TSW1405 draws its power supply from the 5 V source of the USB connection, so no additional external power supply is needed in most applications. For applications where the USB connection does not supply the 5 V, there is the option to connect an external 5 V supply to the test point loop labeled as TP2, 5 V. To use the 5V test point loop, it may be necessary to remove the surface mount zero-ohm resistor in location R42 to disconnect the board's 5 V supply from the USB connector.

7.1.2 Pushbuttons

The TSW1405 has provisions for two pushbutton switches which are normally not installed. SW1 causes the FPGA to load its bit file from the on-board SPI Flash EEPROM. Since the EEPROM is normally not installed, the pushbutton switch SW1 is normally not installed. Pushbutton switch SW2 is reserved for possible future use, so it is also not installed at present.

7.1.3 Jumpers

The TSW1405 has provisions for four jumpers which are normally not installed. Each jumper has one post connected to an FPGA input and a pull up resistor while the other post connects to ground. These jumpers are reserved for possible future use for setting options to the FPGA or for possible output connections from the FPGA.

The TSW1405 also has an optional 6-pin header for connection to the JTAG port of the FPGA, but the JTAG header may not be installed. The JTAG port would allow the use of an FPGA programming pod, but is not necessary since the FPGA firmware is downloaded from the PC at runtime.

7.1.4 LEDs

The TSW1405 has an LED labeled D1 Done that is lit when the FPGA is finished loading a bit file and is ready for use. An additional LED labeled D2 is normally not installed and is reserved for future use. For the initial release of the TSW1405, the LED D2 (if installed) will flash when an LVDS clock is present from the ADC EVM.

7.2 Software Operation

The TSW1405 uses the same software GUI as the TSW1400, providing for a consistent and familiar experience for the user of the TI Capture Cards. When the GUI is launched on the PC, the GUI will detect whether any TSW1400 or TSW1405 capture cards are connected to the PC USB ports, and allow the user to select which to connect to if there are more than one connected.

7.2.1 Channel Selection

Because the TSW1405 has limited memory for sample capture, the GUI makes provision for selecting the number of channels from which to capture samples. This is a feature in the GUI that is not needed for the TSW1400, so there is a GUI popup dialog box for the TSW1405 that is not used for the TSW1400, as shown in Figure 46.

If a device is selected in the GUI that has more than one channel available, the Channel Selection Dialog window will let the user select one or more channels to be used for capture. If two, four or eight channels are selected, then samples from those channels are captured into the capture memory simultaneously.

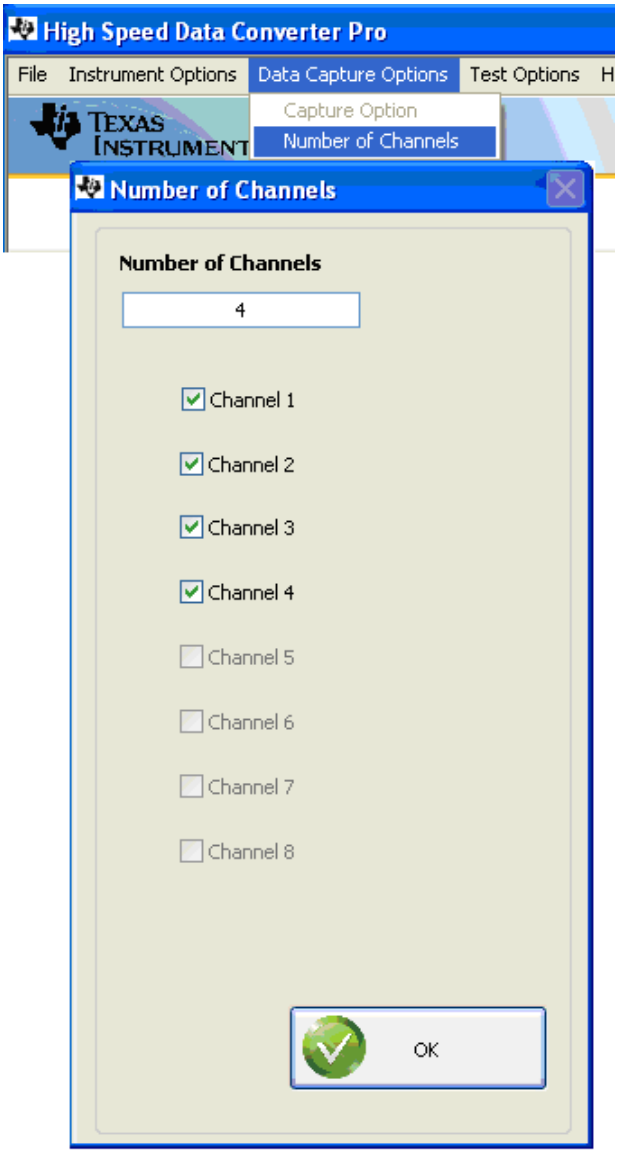

Figure 46. Number of Channels Selection

The TSW1405 has enough internal memory in the FPGA to capture as many as 65536 samples of 16bit data. The 65536 samples will be automatically allocated to one, two, four or eight channels depending on the channel selections set in the GUI. If one channel is selected for capture, then the record length for that channel will be 65536 samples. If two channels are selected for capture, then each channel will get a record length of 32768 samples. Four channels will cause a record length of 16384 samples to be captured for each channel, and eight channels will capture 8192 samples for each channel.

8 TSW1406 Functional Description

The TSW1406 Pattern Generator Card is a low cost pattern generator card with reduced memory capacity for providing test patterns to TI High Speed DAC EVMs. The TSW1406 has a High Speed Samtec connector that directly connects to the LVDS input data bus of DAC EVM. The TSW1406 does not have connections for CMOS DAC EVMs. The TSW1406 uses the same software GUI as the TSW1400.

The TSW1406 does not have an EEPROM resident on the board to hold an FPGA bit file, but rather will get the bit file downloaded from the software GUI running on a PC at runtime. In this manner the TSW1406 will not need to be reprogrammed when new DAC EVMs or additional capture features become available. The planned FPGA firmware upgrades consists of new files to be downloaded to the software GUI. The TSW1406 does have a footprint for a firmware EEPROM to be installed, if desired.

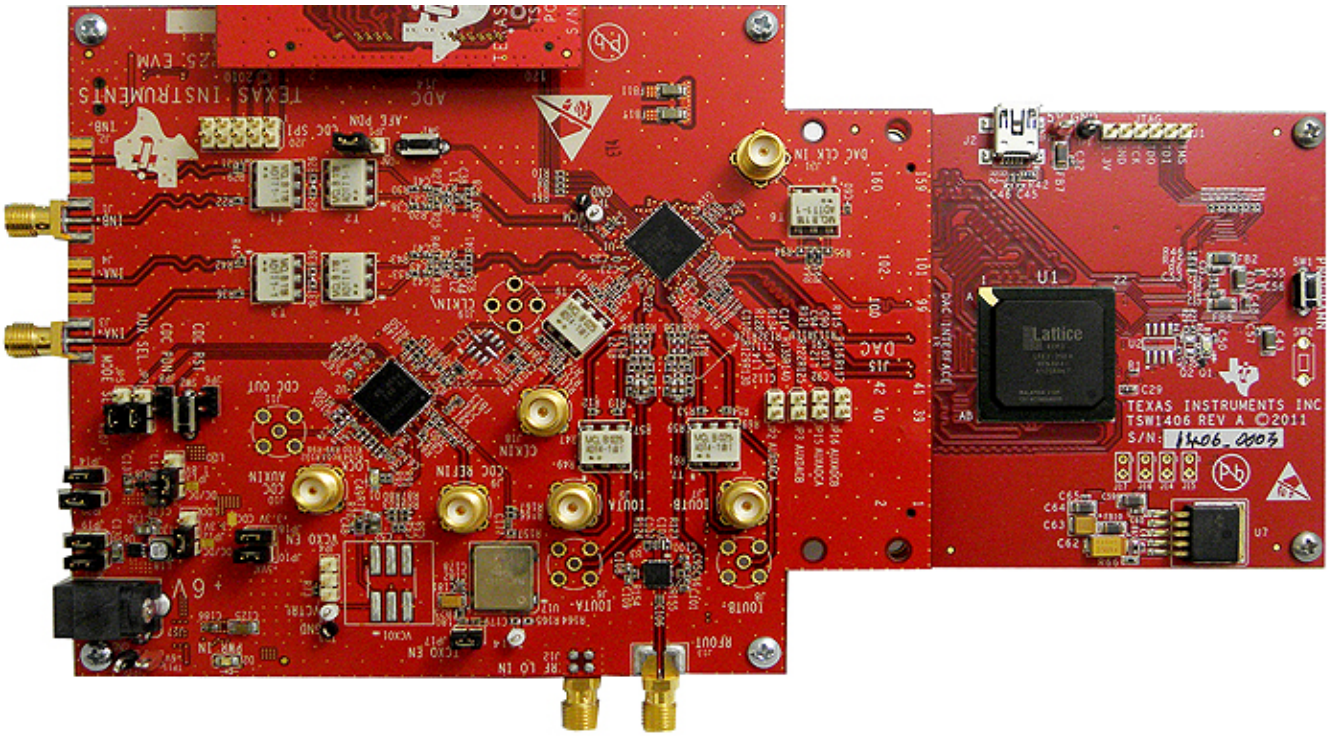

Figure 47. TSW1406EVM Connected to the DAC input of the AFE7225EVM

8.1 Hardware Description

8.1.1 Power Connections

The TSW1406 draws its power supply from the 5 V source of the USB connection, so no additional external power supply is needed in most applications. For applications where the USB connection does not supply the 5 V, there is the option to connect an external 5V supply to the test point loop labeled as TP2 and GND to TP1. To use the 5 V test point loop, make sure to remove R42 to disconnect the board's 5 V supply from the USB connector.

8.1.2 Pushbuttons

The TSW1406 has provisions for two pushbutton switches. SW1 causes the FPGA to load its bit file from the on-board SPI Flash EEPROM. This mode is currently not supported. Pushbutton switch SW2 is reserved for possible future use.

8.1.3 Jumpers

The TSW1406 has provisions for four jumpers which are normally not installed. Each jumper has one post connected to an FPGA input and a pull up resistor while the other post connects to ground. These jumpers are reserved for possible future use for setting options to the FPGA or for possible output connections from the FPGA. The TSW1406 also has an optional 6-pin header for connection to the JTAG port of the FPGA. The JTAG port would allow the use of an FPGA programming pod, but is not necessary since the FPGA firmware is downloaded from the PC at runtime.

8.1.4 LEDs

The TSW1406 LED labeled D1 is the “Done” indicator of the FPGA. This LED is lit when the FPGA is finished loading a bit file and is ready for use. An additional LED labeled D2 represents PLL lock status of the FPGA which should be on for normal operation.

8.2 Software Operation

The TSW1406 uses the same software GUI as the TSW1400, providing for a consistent and familiar experience for the user of the TI Pattern Generator Cards. When the GUI is launched on the PC, the GUI detects whether any TSW1400 or TSW1406 capture cards are connected to the PC USB ports, and allow the user to select which to connect to if there are more than one connected.

9 Revision History

Revision A (March 2012)
Changed and Added figures and text throughout the document
Added section 7 - TSW1405 Functional Description
Revision B (September 2012)
The GUI supports the TSW1406 Low Cost pattern Generation card in addition to the TSW1400 and TSW1405.
Master and slave triggering modes are available for the TSW1400. Under 'Data Capture Option' there is now a 'Trigger Option' menu with two sub-options. 'Trigger Mode Enable' allows externally triggering capture into DDR memory through SMA connector named 'EXT_TRG_IN' while 'Software Trigger' generates a trigger on the four SMA connectors labeled 'SYNC'
Added FFT Averaging feature (with or without continuous capture). This feature performs 'n' continuous captures (max = 10) and averages the FFT's on the fly to reduce noise
Complex FFT feature is now available for the DAC panel. The 'format' dropdown above the FFT plot controls whether the FFT is visualized in real or complex mode.
Includes ‘DAC channel enable’ feature that allows one to selectively send zeroes to selected DAC channels
Increased speed of Continuous Capture function.
The notch frequency bins menu option is disabled in all modes except single tone.
Revised defaults for notch filters (25:25:25) in windowed modes only. Rectangular window modes filter parameters unchanged.
Peak to Peak amplitude and PAR values are now displayed for time domain DAC and ADC.
FFT plot in DAC mode defaults to windowed (Blackman window) mode when creating tone or loading file with >64K samples.
The Time domain plot color is now dark blue (both on the context plot and main plots).
Test Options tab added option to display the X axis scale in "time" instead of "Samples".
The Bandwidth Integration Markers could earlier be swapped, causing problems. Now they cannot.
GUI auto-disconnects gracefully if the USB cable is unplugged and some user operation is attempted.
GUI includes a "Check for Updates" feature that checks (every 7 days) for latest version and prompts a download if a newer version is available for download at the TI product page. Feature is also accessible from menu.
Advanced "FFT x scale" feature in Device INI to adjust the FFT x scale for decimated sample rate devices.

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Changes or modifications not expressly approved by the party responsible for compliance could void the user's authority to operate the equipment.

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- Reorient or relocate the receiving antenna.
- Increase the separation between the equipment and receiver.
- Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.
- Consult the dealer or an experienced radio/TV technician for help.

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