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Specification

MCT057HA6W320240LSL

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1. Revision History

DATE	VERSION	REVISED PAGE NO.	Note
2012/06/20	1		First issue

2. General Specification

This product is composed of a TFT LCD panel, driver ICs, FPC, Control Board and a backlight unit. The following table described the features of MCT057HA6W320240LSL

- Dot Matrix: 320 x RGB x240
- Module dimension: 141.12x 101.55 x 6.3 (max.) mm
- View area: 117.9 x 89.1 mm
- Active area: 115.2 x 86.4 mm
- Dot pitch: 0.12 x 0.36 mm
- LCD type: TFT, Negative, Transmissive
- View direction: 6 o'clock
- Backlight Type: LED, Normally White
- Controller IC: HX8218-A+HZ8615A(or compatible)

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Midas Active Matrix Display Part Number System

MC	T	057	A	6	*	W	320240	L	M	L	*	*	*	*	*
1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16

1 = **MC:** Midas Components

2 = **T:** TFT **A:** Active Matrix OLED

3 = **Size**

4 = **Series**

5 = **Viewing Angle: 6:** 6 O'clock **12:** 12 O'clock

6 = **Blank:** No Touch **T:** Touchscreen

7 = **Operating Temp Range:** **S:** 0 to 50Deg C **B:** -20+60Deg C
W: -20+70Deg C **E:** -30+85Deg C

8 = **No of Pixels**

9 = **Orientation:** **P:** Portrait **L:** Landscape

10 = **Mode:** **R:** Reflective **M:** Transmissive **T:** Transflective
S: Sunlight Readable (transmissive)

11 = **Backlight:** **Blank:** None **L:** LED **C:** CCFL

12 = **Blank:** No Module/board **C:** Controller board module

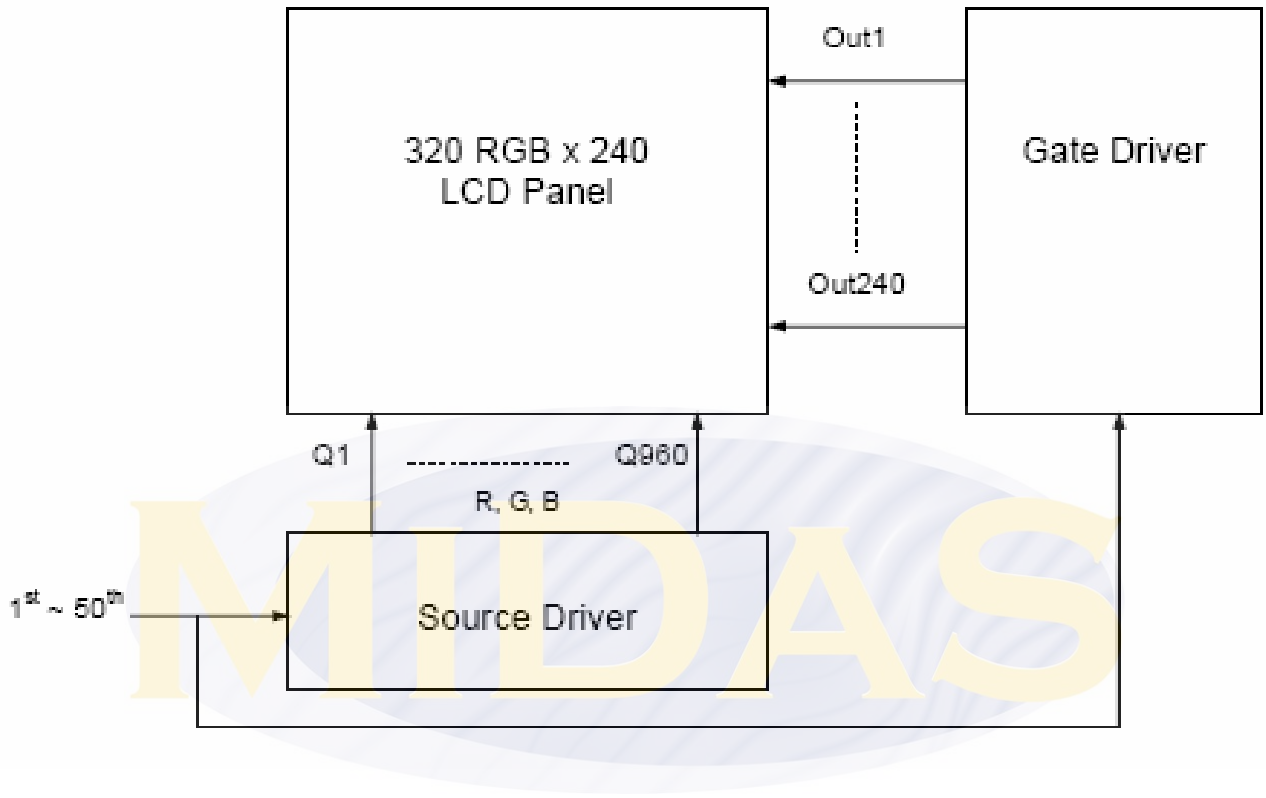
13 = **Blank:** None **V**: Video

14 = **Blank:** None **B**: Bracket

15 = **Blank:** None **H**: Host Cable

16 = **Blank:** None **K**: Keyboard

4.Block Diagram



5.Electrical Characteristics

Item	Symbol	Condition	Min	Typ	Max	Unit
Supply Voltage For Logic	V_{DD}	—	3.0	3.3	3.6	V
Input High Volt.	V_{IH}	—	0.7 V_{DD}	—	V_{DD}	V
Input Low Volt.	V_{IL}	—	0	—	0.3 V_{DD}	V
Power Supply Voltage	V_{GH}	Ta=25℃	10		30	V
	V_{GL}	Ta=25℃	-17		-5	V
Supply Current	I_{VDD}	V_{DD}=3.3V	—	5	8	mA

6.Absolute Maximum Ratings

Item	Symbol	Min	Typ	Max	Unit
Operating Temperature	T_{OP}	-20	—	+70	℃
Storage Temperature	T_{ST}	-30	—	+80	℃
Power Supply Voltage	V_{GH}	-0.3	—	32.0	V
	V_{GL}	-22	—	0.3	V
	V_{GH} - V_{GL}	-0.3	—	+45	V

7. Interface Pin Function

7-1 LCM PIN Definition

Pin No.	Symbol	I/O	Description	Remark
1	IF1	I	Input data format control (Note1)	Note1
2	IF2	I	Input data format control (Note1)	Note1
3	POL	O	Polarity Signal connect to VCOM driving circuit.	Note3
4	RESET	I	Hardware reset.	
5	SPENA	I	Chip select	Note2
6	SPCL	I	Serial Clock	Note2
7	SPDA	I/O	Serial Data	
8	B0	I	Blue Data bit (LSB)	
9	B1	I	Blue Data bit	
10	B2	I	Blue Data bit	
11	B3	I	Blue Data bit	
12	B4	I	Blue Data bit	
13	B5	I	Blue Data bit	
14	B6	I	Blue Data bit	
15	B7	I	Blue Data bit(MSB)	
16	G0	I	Green Data bit(LSB)	
17	G1	I	Green Data bit	
18	G2	I	Green Data bit	
19	G3	I	Green Data bit	
20	G4	I	Green Data bit	
21	G5	I	Green Data bit	
22	G6	I	Green Data bit	
23	G7	I	Green Data bit(MSB)	
24	R0	I	Red Data bit(LSB)	
25	R1	I	Red Data bit	
26	R2	I	Red Data bit	
27	R3	I	Red Data bit	
28	R4	I	Red Data bit	
29	R5	I	Red Data bit	
30	R6	I	Red Data bit	
31	R7	I	Red Data bit(MSB)	
32	Hsync	I	Horizontal synchronous signal	
33	Vsync	I	Vertical synchronous signal	
34	Data CLK	I	Dot data clock	
35	AVDD(analog)	I	Analog power: 4.5V~5.5V	
36	AVDD(analog)	I	Analog power: 4.5V~5.5V	
37	VDD(Digital)	I	Digital power: 3V~3.6V	
38	VDD(Digital)	I	Digital power: 3V~3.6V	
39	NPC	O	NTSC/PAL mode Auto detection result H:NTSC/L:PAL	
40	VGL	I	Gate off power	
41	VGL	I	Gate off power	

42	UD	I	Up/Down scan setting. H: Reverse scan / L: Normal scan	
43	VGH	I	Gate on power	
44	LRC	I	Shift direction of device internal shift register control.	
45	GND	I	GROUND	
46	VCOM	I	VCOM driving input	Note3
47	VCOM	I	VCOM driving input	
48	ENB	I	Data enable input. Normally pull low.	Note4
49	GND	I	GROUND	
50	GND	I	GROUND	

Note: 1.Control the input data format.

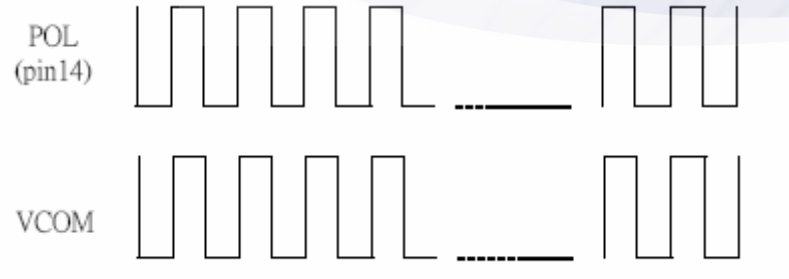
IF2,IF1	Input data format
L,L(default)	Serial RGB
L,H	Parallel RGB
H,L	CCIR601
H,H	CCIR656

2. Pin 5、Pin 6 usually pull high.

3. The polarity of VCOM (Pin 46,47) should be generated from POL (Pin 3).

4. For digital RGB input data format, both SYNC mode and DE+SYNC mode are supported. If ENB signal is fixed low, SYNC mode is used. Otherwise, DE+SYNC mode is used.

5. The phase of POL (pin 3):



7.2 Backlight PIN Definition

Pin No.	Symbol	I/O	Description
1	VLED+	I	Red, LED_ Anode
2	VLED-	I	Black, LED_ Cathode

Note: The backlight interface connector is a model **PHR-2** manufactured by JST or equivalent.

The matching connector part number is **S 2B-PH-K-S** manufactured by JST or equivalent.

8. AC Characteristics

8.1. CCIR601/656 Interface

8.1.1. Input signal characteristics

PARAMETER	Symbol	Min.	Typ.	Max.	Unit
CLK period	T_{OSC}	-	37	-	ns
Data setup time	T_{SU}	12	-	-	ns
Data hold time	T_{HD}	12	-	-	ns

8.1.2 Hardware reset timing

PARAMETER	Symbol	Min.	Typ.	Max.	Unit
RESET low pulse width	T_{RSB}	10	-	-	μs

8.1.3. Output signal characteristics

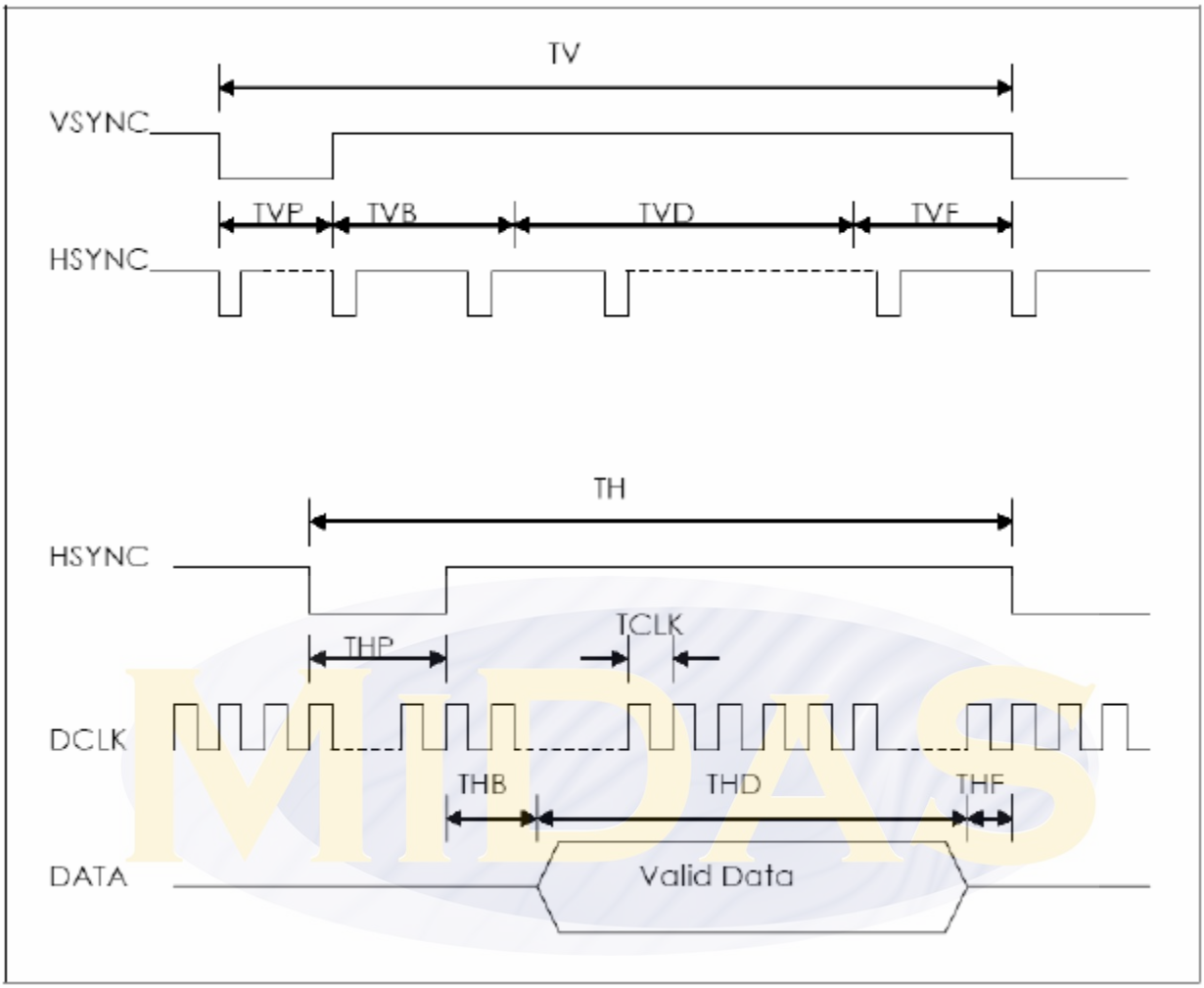
PARAMETER		Symbol	Min.	Typ.	Max.	Unit
Rising time		T_r	-	-	10	ns
Falling time		T_f	-	-	10	ns
Internal STH setup time		T_{SUS}	12	-	-	ns
Internal STH hold time		T_{HDS}	12	-	-	ns
Internal data setup time		T_{SUD}	60	-	-	ns
Internal data hold time		T_{HDD}	40	-	-	ns
OEH pulse width		T_{OEH}	-	1248	-	ns
OEV pulse width		T_{OEV}	-	4992	-	ns
CKV pulse width		T_{CKV}	-	3744	-	ns
Hsync – DEH time		T_1	-	4368	-	ns
Hsync – CKV time		T_2	-	2496	-	ns
Hsync – OEV time		T_3	-	624	-	ns
Vsync – setup time		T_{SUV}		1872	-	ns
Vsync – pulse time		T_{STV}		1	-	T_H
Vsync – STV time	NTSC	T_{VS1}	-	19	-	T_H
	PAL	T_{VS1}	-	27	-	T_H
OEH – STV time		T_{HE}	-	2	-	T_H
Output settling time		T_{OES}	-	12	20	μs

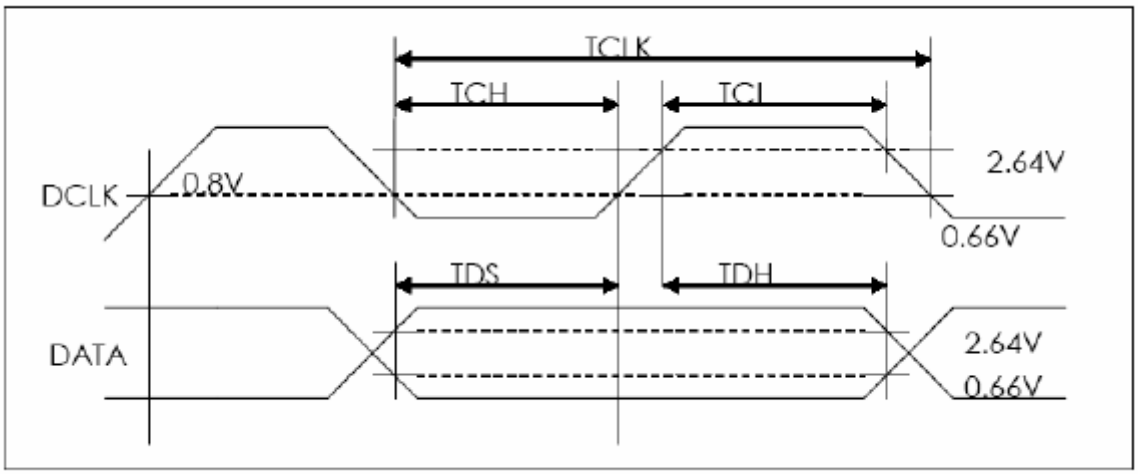
8.2. 24-bits parallel RGB Interface

8.2.1 AC Timing Characteristics

Signal	Item		Symbol	Min	Typ	Max	Unit
Dclk	Frequency		Dclk	-	6.4	-	MHZ
	High Time		Tch	-	78	-	ns
	Low Time		Tcl	-	78	-	ns
Data	Setup Time		Tds	12	-	-	ns
	Hold Time		Tdh	12	-	-	ns
Hsync	Period		TH	-	408	-	DCLK
	Pulse Width		Thp	-	30	-	DCLK
	Back-Porch		Thb	-	38	-	DCLK
	Display Period		Thd	-	320	-	DCLK
	Front-Porch		Thf	-	20	-	DCLK
Vsync	Period	NTSC	Tv	-	262.5	-	TH
		PAL			312.5		
	Pulse Width		Tvp	1	3	5	TH
	Back-Porch	NTSC	Tvb	-	15	-	TH
		PAL			23		
	Display Period		Tvd	-	240	-	TH
	Front-Porch	NTSC	Tvf	-	4.5	-	TH
		PAL			46.5		

8.2.2 AC Timing Diagrams

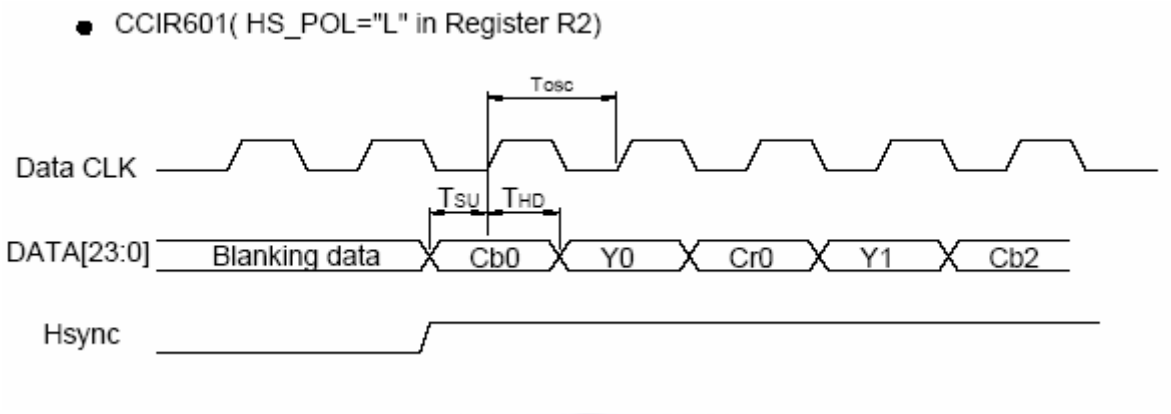


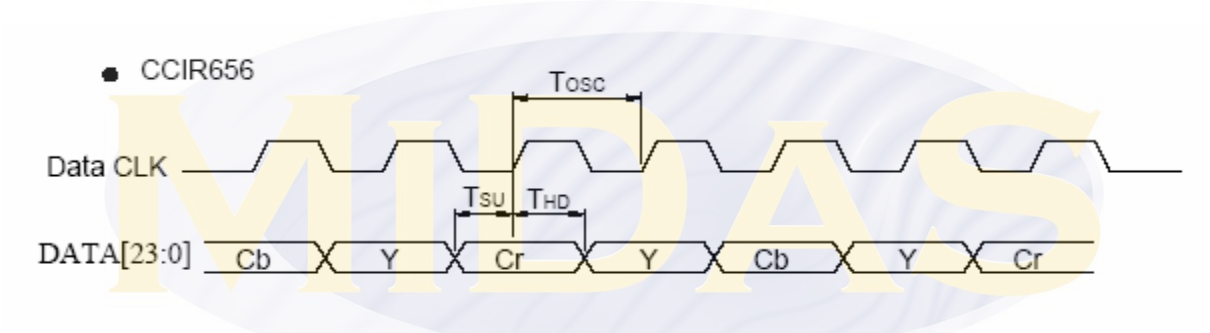


9. Waveform

9.1. Timing Controller Timing Chart

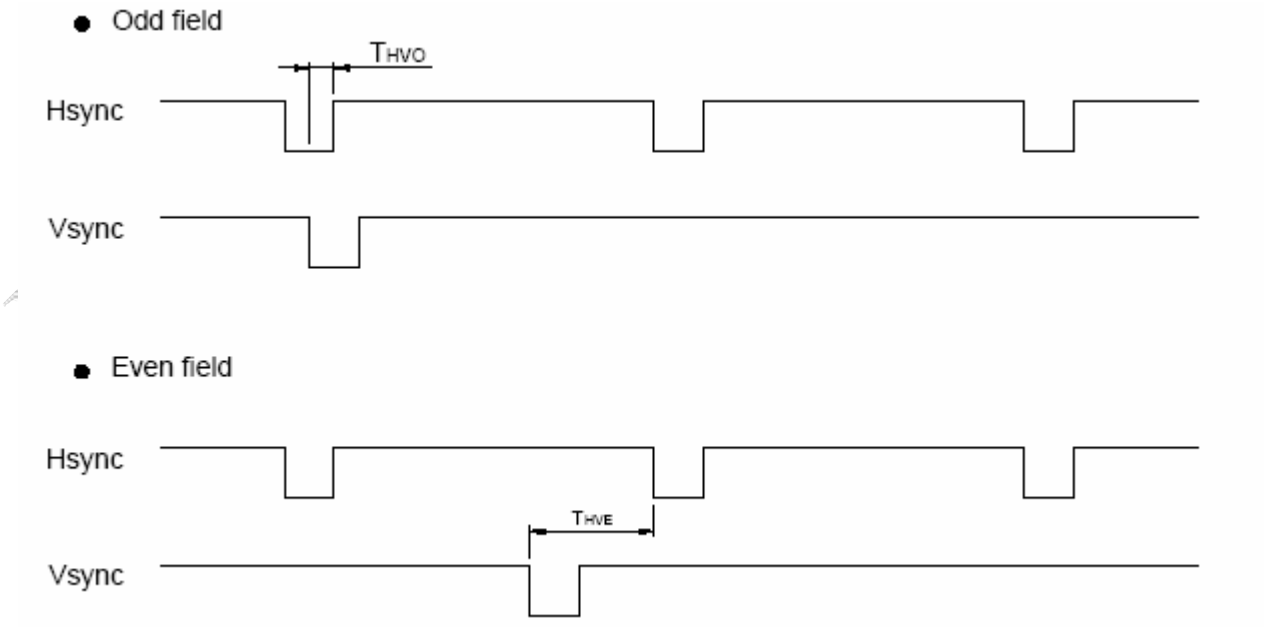
9.1.1. Clock and Data waveform



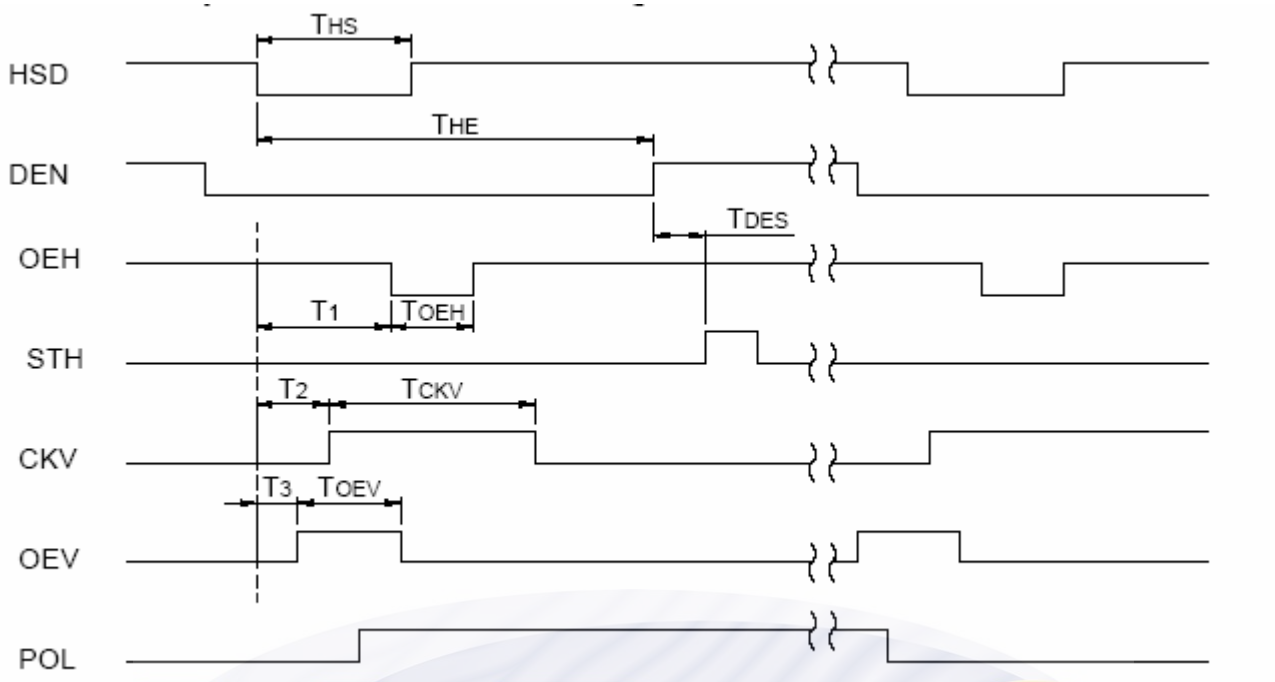


9.1.2 Digital / Analog RGB timing waveform

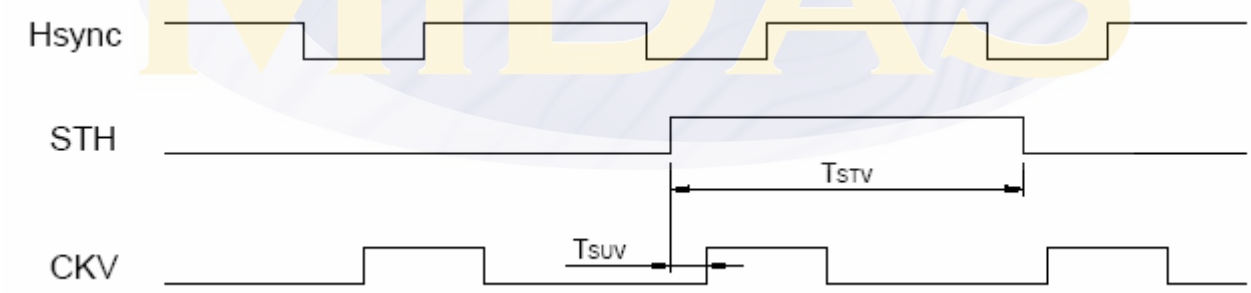
9.1.2.1 Hsync and Vsync timing



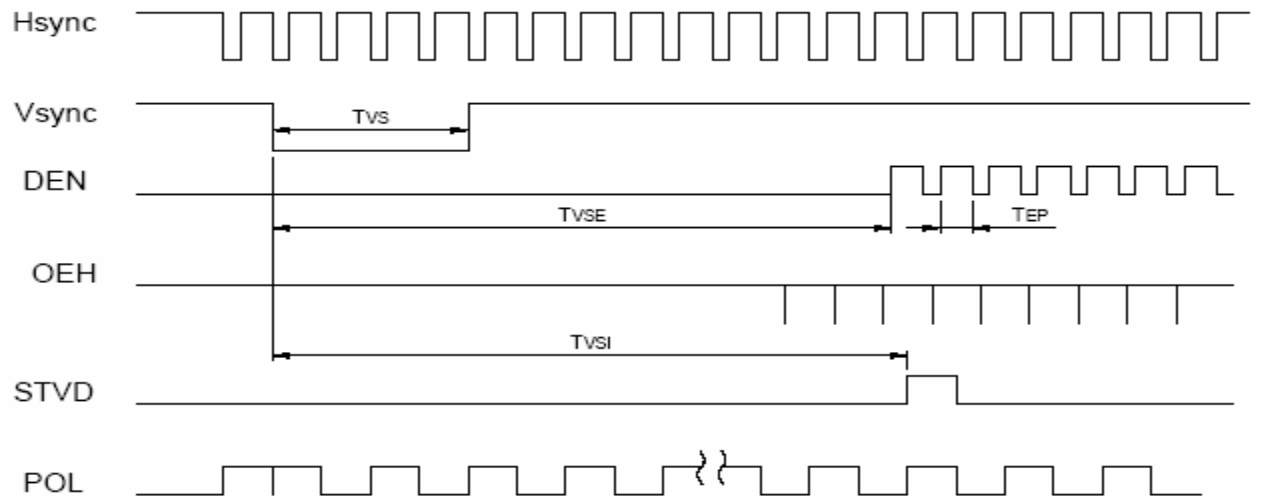
9.1.2.2 Hsync and horizontal control timing waveform



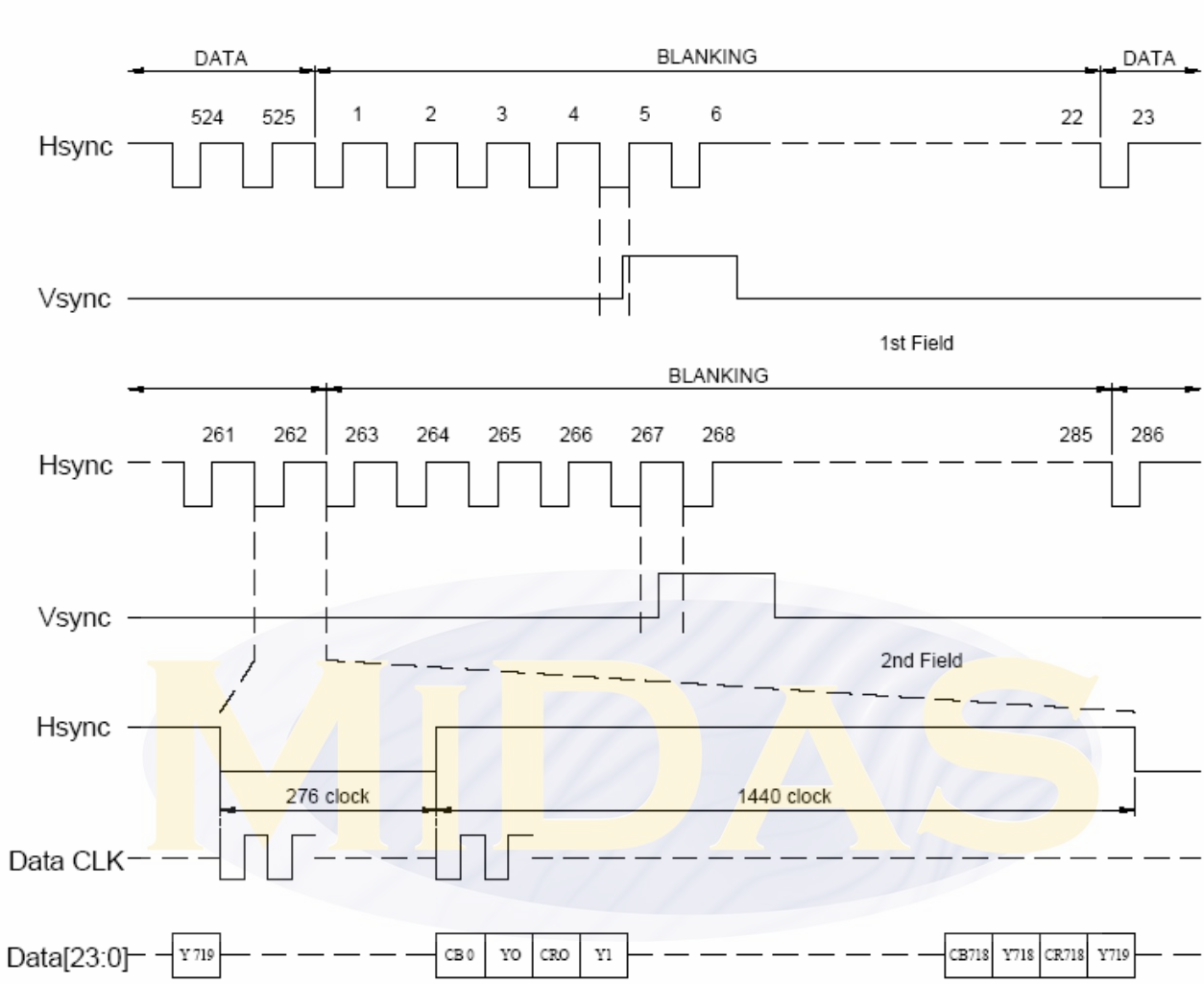
9.1.2.3 Hsync and vertical shift clock timing waveform



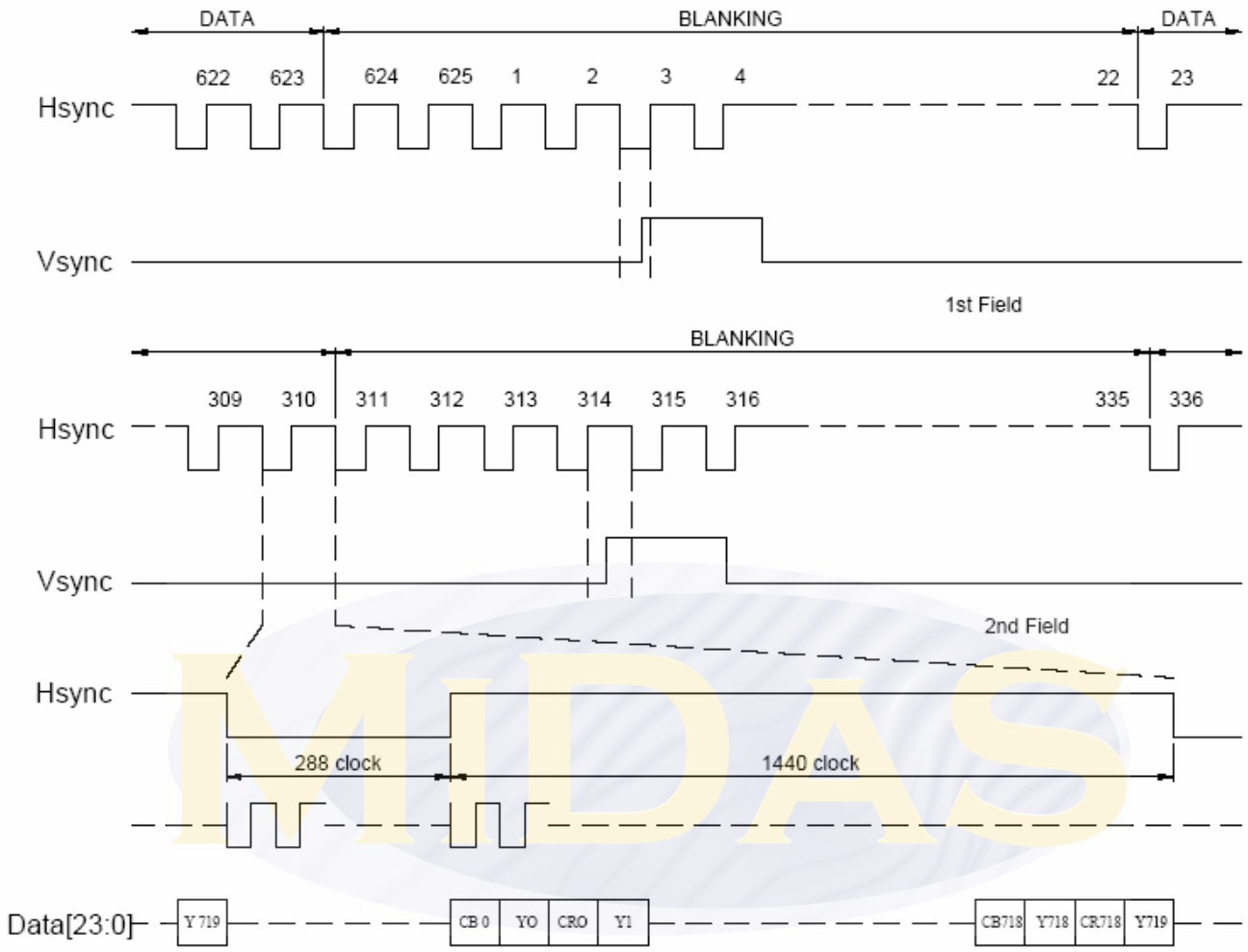
9.1.2.4 Hsync and vertical shift clock timing waveform



9.1.3 CCIR601 timing waveform (VS_POL="H" , HS_POL="L" in Register R2)



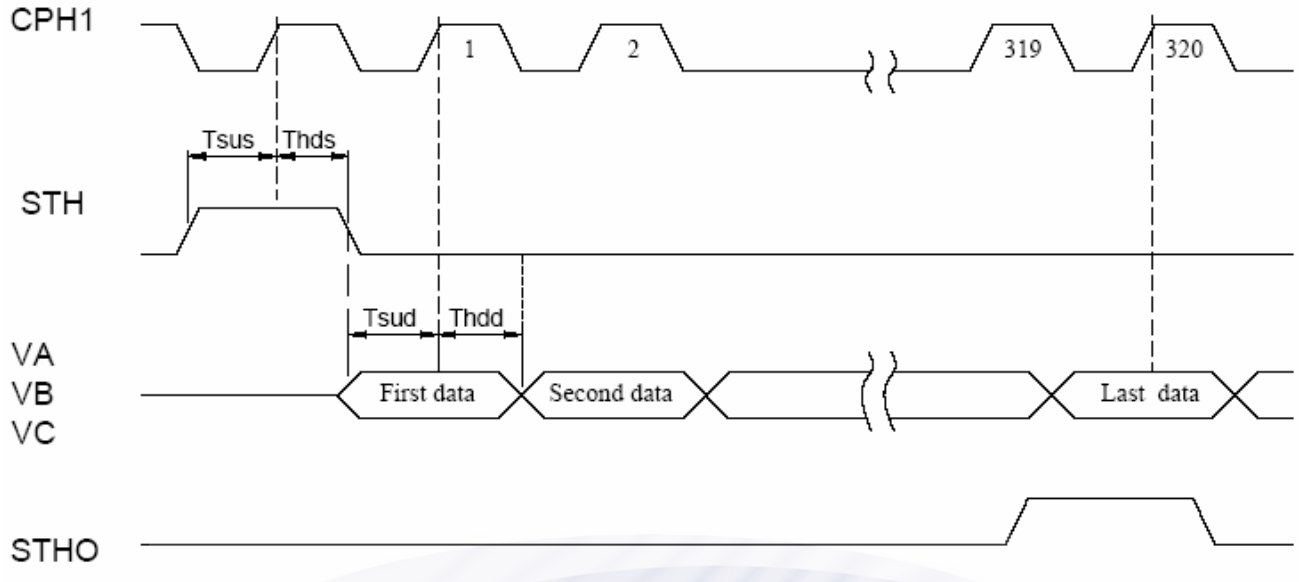
ITU-BT.601 NTSC Input Timing



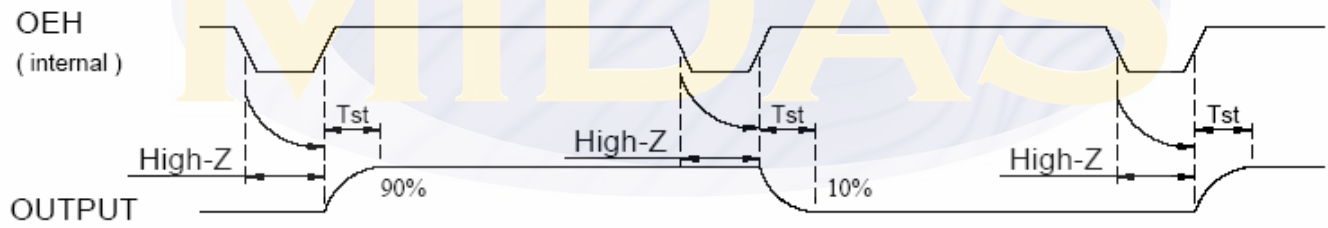
ITU-BT.601 PAL Input Timing

9.2 Source Driver Timing Chart

9.2.1 Clock and Start Pulse timing waveform



9.2.2 OEH and Data Output timing waveform



9.3 Analog video signal characteristics

PARAMETER	Symbol	Min.	Typ.	Max.	Unit
Video signal amplitude (VA, VB, VC)	V_{IAC}	-	3.81	-	V
	V_{IDC}	-	2.385	-	V

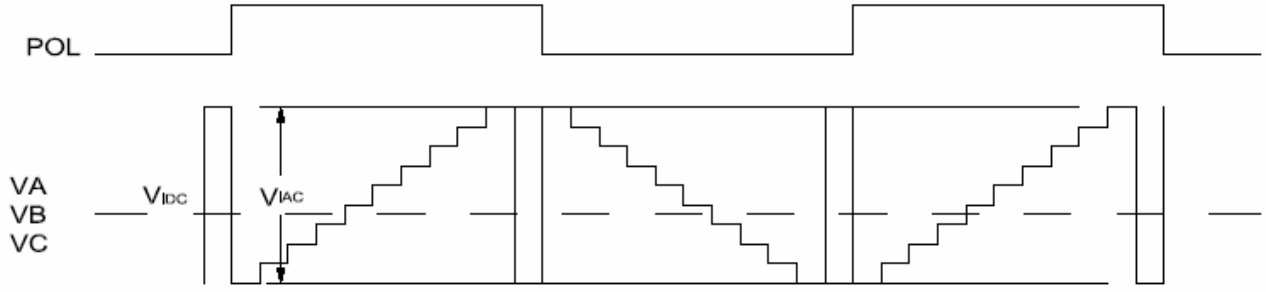
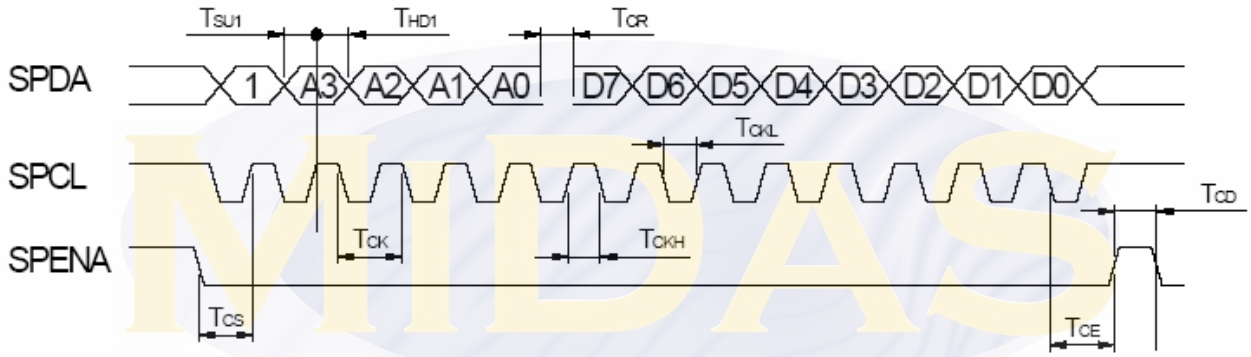


Fig. 4-(a) Horizontal timing

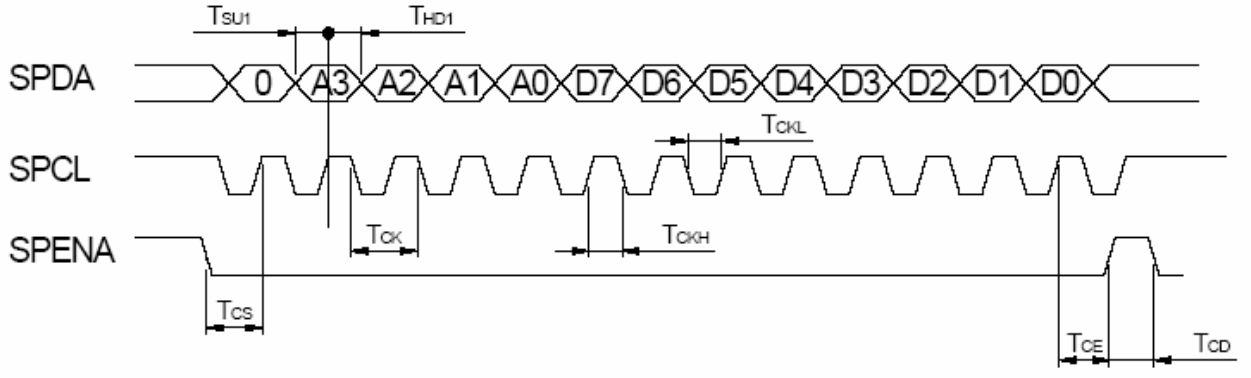
9.4 SPI timing characteristics

PARAMETER	Symbol	Min.	Typ.	Max.	Unit
SPCL period	T_{CK}	60	-	-	ns
SPCL high width	T_{CKH}	30	-	-	ns
SPCL low width	T_{CKL}	30	-	-	ns
Data setup time	T_{SU1}	12	-	-	ns
Data hold time	T_{HD1}	12	-	-	ns
SPENA to SPCK setup time	T_{CS}	20	-	-	ns
SPENA to SPDA hold time	T_{CE}	20	-	-	ns
SPENA high pulse width	T_{CD}	50	-	-	ns
SPDA output latency	T_{CR}		1/2	-	T_{CK}

- SPI "read" timing

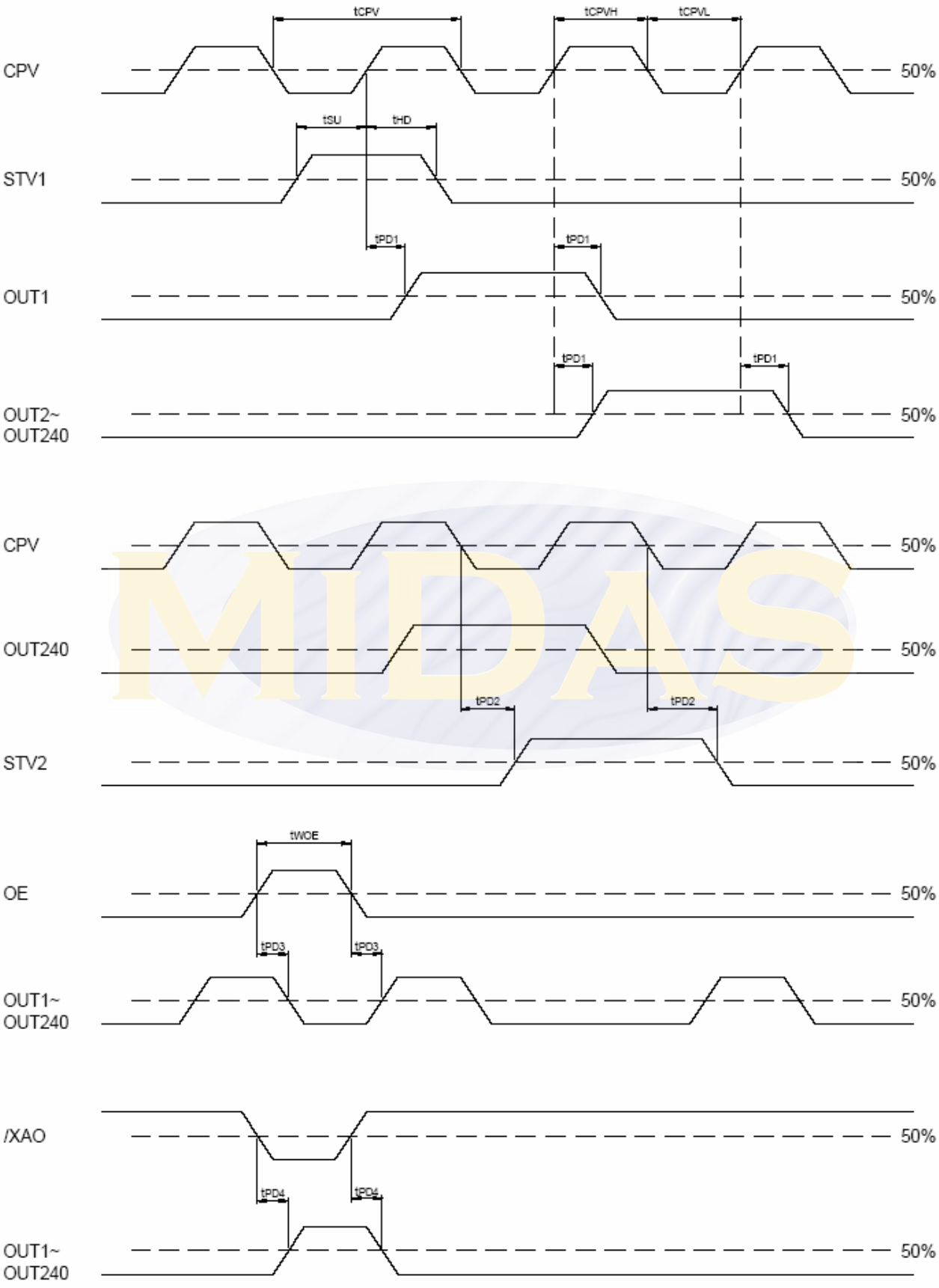


- SPI "write" timing



9.5 Gate Driver Timing Chart

Parameter	Symbol	Condition	Spec		Unit
			Min.	Max.	
Operation frequency	tCPV		5	-	μs
CPV pulse width	tCPVH,tCPVL	50%duty cycle	2.5	-	
OE pulse width	twOE		1	-	
Data setup time	tsu		0.4	-	us
Data hold time	thd		0.7	-	
Output delay time	tpd1	CL=300pF	-	1	
Output delay time	tpd2	CL=300pF	-	0.8	
Output delay time	tpd3	CL=300pF	-	0.8	
Output delay time	tpd4	CL=300pF	-	10	


tCPV
tCPVH
tCPVL
CPV
50%
tSU
tHD
STV1
50%
tPD1
tPD1
OUT1
50%
tPD1
tPD1
OUT2~
OUT240
50%
CPV
50%
OUT240
50%
tPD2
tPD2
STV2
50%
tWOE
OE
50%
tPD3
tPD3
OUT1~
OUT240
50%
/XAO
50%
tPD4
tPD4
OUT1~
OUT240
50%

10. Optical Characteristics

Item		Symbol	Condition	Min.	Typ.	Max.	Unit	Remark
Response time		Tr	θ=0°	—	15	30	ms	Note 3,5
		Tf		—	35	50	ms	
Contrast ratio		CR	At optimized viewing angle	350				Note 4,5
Color chromaticity	White	Wx	θ=0°	(0.25)	(0.30)	(0.35)		Note 2,6,7
		Wy		(0.27)	(0.32)	(0.37)		
Viewing angle	Hor.	θR	CR≧10	50	65	—	Deg.	Note 1
		θL		50	65	—		
	Ver.	θT		30	50	—		
		θB		50	55	—		
Uniformity		U	—	(70)	(75)	—	%	Note 8
Brightness		—	25°C	800	—	—	Cd/m^2	Center of display. Note 9

PS. The inaccuracy of average brightness is around 10% to 15% due to material differences.

Note 1: Definition of viewing angle range

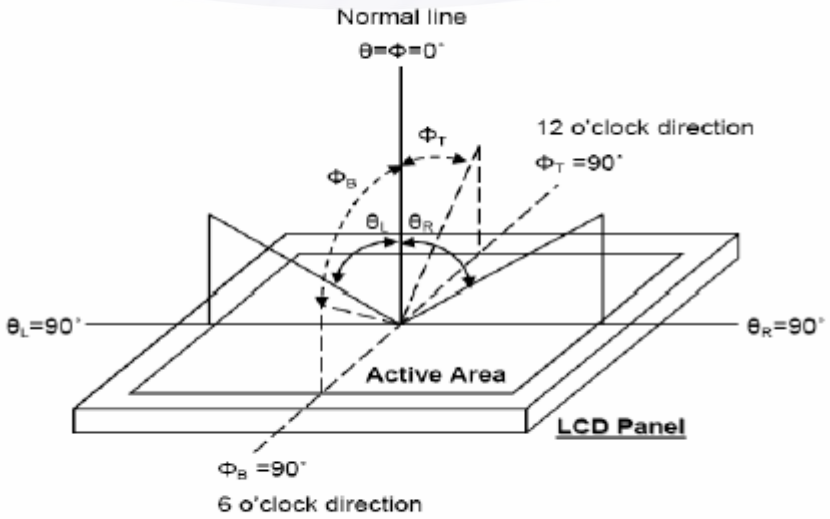


Fig. 8-1 Definition of viewing angle

Note 2: Test equipment setup:

After stabilizing and leaving the panel alone at a driven temperature for 5 minutes, the measurement should be executed. Measurement should be executed in a stable, windless, and dark room. Optical specifications are measured by Topcon BM-7 luminance meter 1.0° field of view at a distance of 50cm and normal direction.

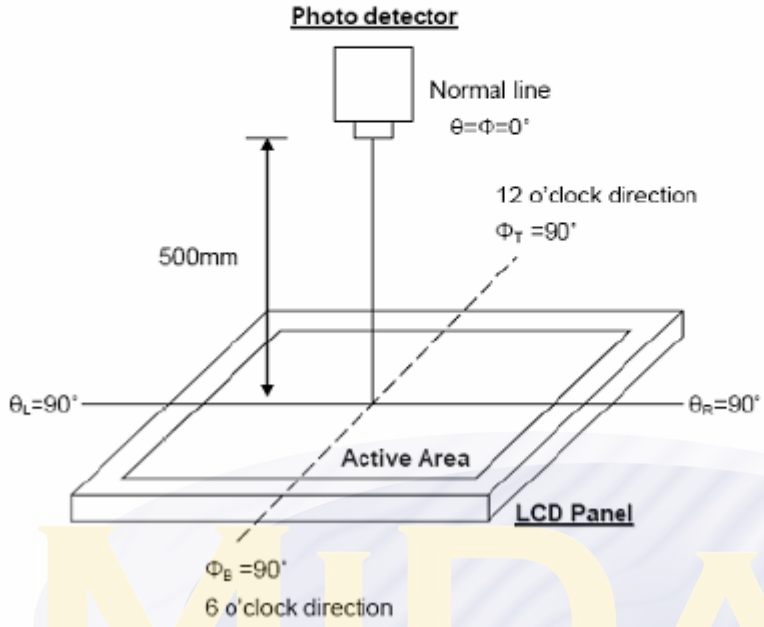


Fig. 8-2 Optical measurement system setup

Note 3: Definition of Response time:

The response time is defined as the LCD optical switching time interval between "White" state and "Black" state. Rise time, Tr, is the time between photo detector output intensity changed from 90% to 10% . And fall time, Tf, is the time between photo detector output intensity changed from 10% to 90% .

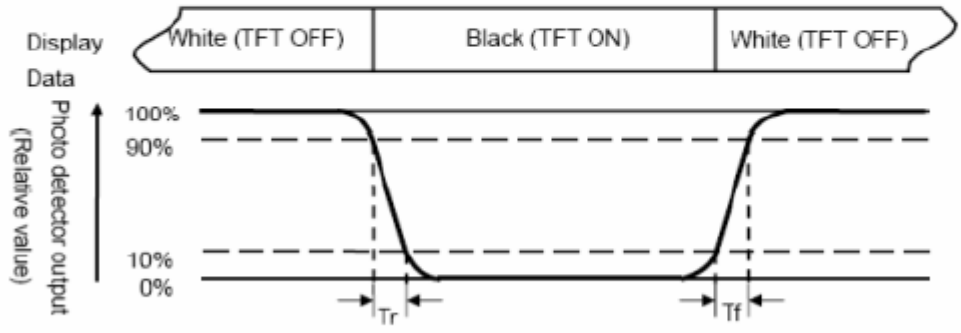


Fig. 3-3 Definition of response time

Note 4: Definition of contrast ratio:
The contrast ratio is defined as the following expression.

$$\text{Contrast ratio (CR)} = \frac{\text{Luminance measured when LCD on the "White" state}}{\text{Luminance measured when LCD on the "Black" state}}$$

Note 5: White Vi = $V_{i50} \pm 1.5V$
Black Vi = $V_{i50} \pm 2.0V$
"±" means that the analog input signal swings in phase with VCOM signal.
"±" means that the analog input signal swings out of phase with VCOM signal.
The 100% transmission is defined as the transmission of LCD panel when all the input terminals of module are electrically opened.

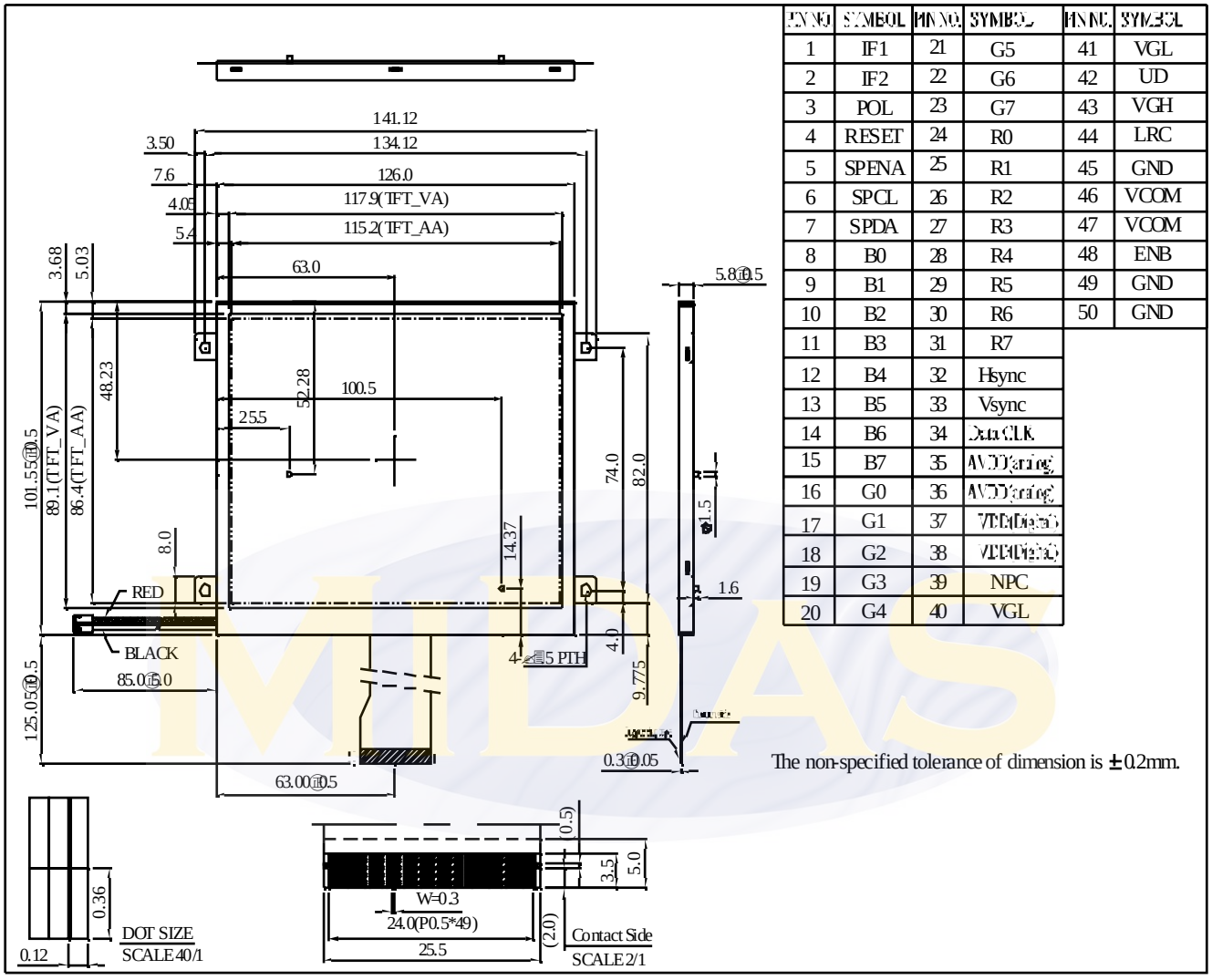
Note 6: Definition of color chromaticity (CIE 1931)
Color coordinates measured at the center point of LCD

Note 7: Measured at the center area of the panel when all the input terminals of LCD panel are electrically opened.

$$\text{Note 8 : Uniformity (U)} = \frac{\text{Brightness (min)}}{\text{Brightness (max)}} \times 100\%$$

Note 9: The brightness of center will decrease 10% to 15% due to rising temperatures in work environment.

11. Contour Drawing

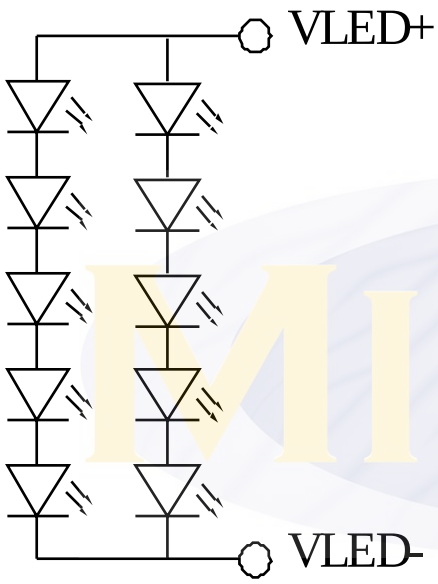


PIN NO	SYMBOL	PIN NO	SYMBOL	PIN NO	SYMBOL
1	IF1	21	G5	41	VGL
2	IF2	22	G6	42	UD
3	POL	23	G7	43	VGH
4	RESET	24	R0	44	LRC
5	SPENA	25	R1	45	GND
6	SPCL	26	R2	46	VCOM
7	SPDA	27	R3	47	VCOM
8	B0	28	R4	48	ENB
9	B1	29	R5	49	GND
10	B2	30	R6	50	GND
11	B3	31	R7		
12	B4	32	Hsync		
13	B5	33	Vsync		
14	B6	34	Data CLK		
15	B7	35	AVDD(analog)		
16	G0	36	AVDD(analog)		
17	G1	37	VDD(Digital)		
18	G2	38	VDD(Digital)		
19	G3	39	NPC		
20	G4	40	VGL		

The non-specified tolerance of dimension is ±0.2mm.

12. LED driving conditions

Parameter	Symbol	Min.	Typ.	Max.	Unit	Remark
LED Current	I_{LED}	120	----	130	mA	Note1
LED voltage	V_{LED}	13.5	----	16.0	V	
LED life Time	-	----	50K	----	-	Note 2,3.4



Note1 : There are 2Groups LED shown as below, V_{LED}=13.5 (min.)
Note2 : Ta=25℃
Note3 : Brightness to be decreased to 50% of the initial value
Note4:50K hours is only an estimate for reference.

13. Reliability Test

WIDE TEMPERATURE RELIABILITY TEST

NO	ITEM	CONDITION			STANDARD	NOTE
1	High Temp. Storage	80℃	240 Hrs		Appearance without defect	
2	Low Temp. Storage	-30℃	240 Hrs		Appearance without defect	
3	High Temp. & High Humi. Storage	60 ℃ 90%RH	240 Hrs		Appearance without defect	
4	High Temp. Operating Display	70℃	240 Hrs		Appearance without defect	
5	Low Temp. Operating Display	-20℃	240 Hrs		Appearance without defect	
6	Thermal Shock	-20 ℃, 30min. → 70℃, 30min. (1cycle)			Appearance without defect	10 cycles

Inspection Provision

1.Purpose

The Midas inspection provision provides outgoing inspection provision and its expected quality level based on our outgoing inspection of Midas LCD produces.

2.Applicable Scope

The Midas inspection provision is applicable to the arrangement in regard to outgoing inspection and quality assurance after outgoing.

3.Technical Terms

3-1 Midas Technical Terms

4.Outgoing Inspection

4-1 Inspection Method

MIL-STD-105E Level Ⅱ Regular inspection

4-2 Inspection Standard

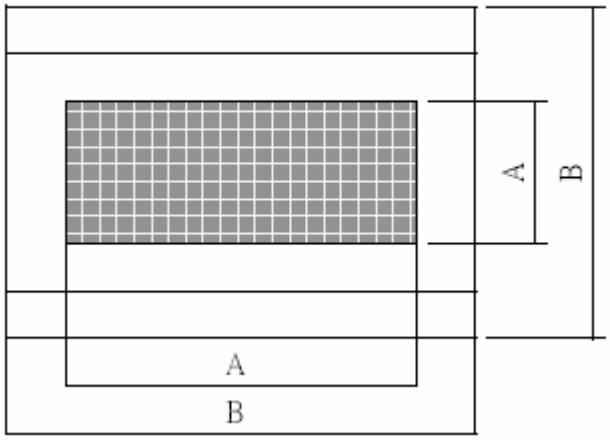
	Item		AQL(%)	Remarks
Major Defect	Dots	Opens Shorts Erroneous operation	0.4	Faults which substantially lower the practicality and the initial purpose difficult to achieve
	Solder appearance	Shorts Loose		
	Cracks	Display surface cracks		

	Dimensions	External from Dimensions	0.4	
Minor Defect	Inside the glass	Black spots	0.65	Faults which appear to pose almost no obstacle to the practicality, effective use, and operation
	Polarizing plate	Scratches, foreign Matter, air bubbles, and peeling		
	Dots	Pinhole, deformation		
	Color tone	Color unevenness		
	Solder appearance	Cold solder Solder projections		

4-3 Inspection Provisions

*Viewing Area Definition

Fig. 1



A : Zone Viewing Area

B : Zone Glass Plate Outline

*Inspection place to be 500 to 1000 lux illuminance uniformly without glaring.
The distance between luminous source(daylight fluorescent lamp and cool white fluorescent lamp)
and sample to be 30 cm to 50 cm.

*Test and measurement are performed under the following conditions, unless otherwise specified.

Temperature 20 ± 15℃
Humidity 65 ± 20%R.H.
Pressure 860~1060hPa(mmbar)

In case of doubtful judgment, it is performed under the following conditions.

Temperature 20 ± 2℃
Humidity 65 ±5%R.H.
Pressure 860~1060hPa(mmbar)

5.Specification for quality check

5-1-1 Electrical characteristics :

NO.	Item	Criterion
1	Non operational	Fail
2	Miss operating	Fail
3	Contrast irregular	Fail
4	Response time	Within Specified value

5-1-2 Components soldering :

Should be no defective soldering such as shorting, loose terminal cold solder, peeling of printed circuit board pattern, improper mounting position, etc.

5-2 Inspection Standard for TFT panel

5-2-1 The environmental condition of inspection :

The environmental condition and visual inspection shall be conducted as below.

(1) Ambient temperature : 25±5℃

(2) Humidity : 25~75% RH

(3) External appearance inspection shall be conducted by using a single 20W fluorescent lamp or equivalent illumination.

(4) Visual inspection on the operation condition for cosmetic shall be conducted at the distance 30cm or more between the LCD panels and eyes of inspector. The viewing angle shall be 90 degreeto the front surface of display panel.

(5) Ambient Illumination : 300~500 Lux for external appearance inspection.

(6) Ambient Illumination : 100~200 Lux for light on inspection.

5-2-2 Inspection Criteria

(1) Definition of dot defect induced from the panel inside

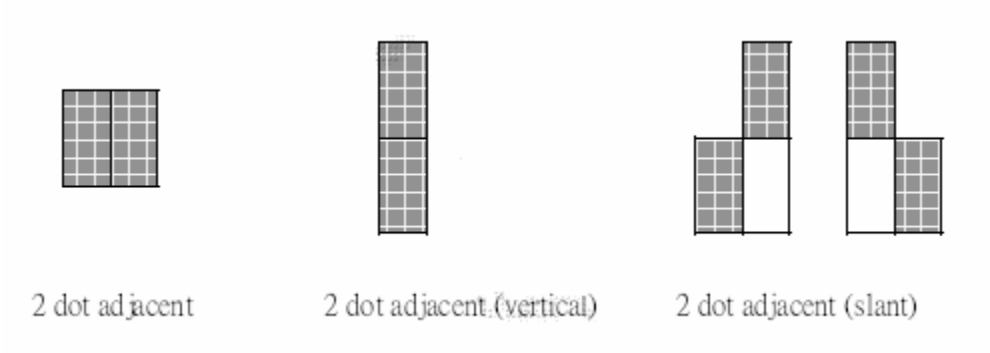
a) The definition of dot : The size of a defective dot over 1/2 of whole dot is regarded as one defective dot

b) Bright dot : Dots appear bright and unchanged in size in which LCD panel is displaying under black pattern.

c) Dark dot : Dots appear dark and unchanged in size in which LCD panel is displaying under pure red, green, blue pattern.

d) 2 dot adjacent = 1 pair = 2 dots

Picture :



(2) Display Inspection

NO.	Item			Acceptable Count
1	Dot defect	Bright Dot	Random	N ≦ 2
			2 dots adjacent	N ≦ 0
		Dark Dot	Random	N ≦ 3
			2 dots adjacent	N ≦ 1
		Total bright and dark dot		N ≦ 4
	Functional failure (V-line/ H-line/Cross line etc.)			Not allowable
	Mura	It's OK if mura is slight visible through 6% ND filter. (Judged by limit sample if it is necessary)		
2	Newton ring (touch panel)	Orbicular of interference fringes is not allowed in the optimum contrast within the active area under viewing angle.		

(3) Appearance inspection

NO.	Item	Standards
1	Panel Crack	Not allow. It is shown in Fig.1.
2	Broken CF Non -lead Side of TFT	The broken in the area of W > 2mm is ignored, L is ignored. It is shown in Fig.2.
3	Broken Lead Side of TFT	FPC lead, electrical line or alignment mark can't be damaged. It is shown in Fig.3.
4	Broken Corner of TFT at Lead Side	FPC lead. electrical line or alignment mark can't be damaged. It is shown in Fig.4.
5	Burr of TFT / CF Edge	The distance of burr from the edge of TFT / CF, W ≦ 0.3mm. It is shown in Fig.5.
6	Foreign Black / White/Bright Spot	(1) 0.15 < D ≦ 0.5 mm, N≦ 4 ; (2) D ≦ 0.15mm, Ignore. It is shown in Fig.6.
7	Foreign Black / White/Bright Line	(1) 0.05<W≦ 0.1 mm, 0.3<L≦2 mm, N≦ 4.
		(2) W ≦ 0.05mm and L≦ 0.3mm Ignore.
		It is shown in Fig.7.
8	Color irregular	Not remarkable color irregular.

Fig 1.

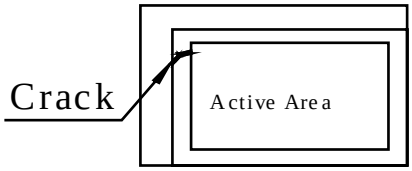


Fig 2.

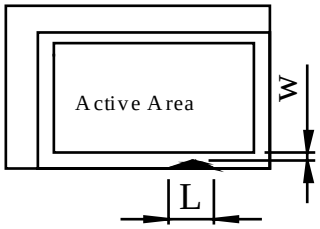


Fig 3.

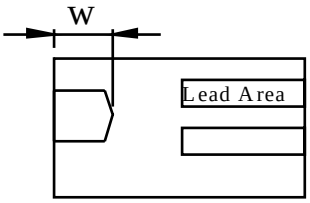


Fig 4.

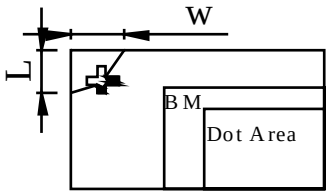


Fig 5.

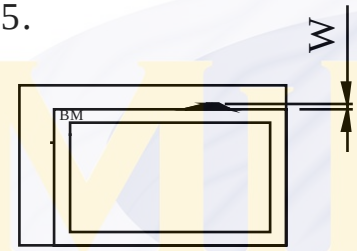
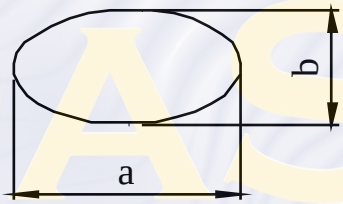


Fig 6.



D=(a+b)/2

Fig 7.

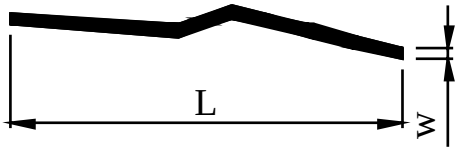
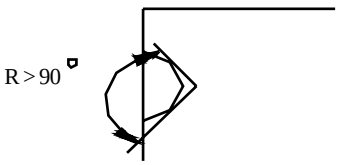


Fig8.



Notes
1.W:Widh
2.Lengh
3.D:Average Diameter
4.N:Count
5.All the anhle of the broken must be larger than 90～.It is shown in Fig.8.(R>90～)

NOTICE:

• SAFETY

1. If the LCD panel breaks, be careful not to get the liquid crystal to touch your skin.
2. If the liquid crystal touches your skin or clothes, please wash it off immediately by using soap and water.

• HANDLING

1. Avoid static electricity which can damage the CMOS LSI.
2. Do not remove the panel or frame from the module.
3. The polarizing plate of the display is very fragile. So, please handle it very carefully.
4. Do not wipe the polarizing plate with a dry cloth, as it may easily scratch the surface of plate.
5. Do not use ketonics solvent & Aromatic solvent. Use a soft cloth soaked with a cleaning naphtha solvent.

• STORAGE

1. Store the panel or module in a dark place where the temperature is 25±5℃ and the humidity is below 65% RH.
2. Do not place the module near organics solvents or corrosive gases.
3. Do not crush, shake, or jolt the module.

• TERMS OF WARRANT

1. Acceptance inspection period

The period is within one month after the arrival of contracted commodity at the buyer's factory site.

2. Applicable warrant period

The period is within twelve months since the date of shipping out under normal using and storage conditions.