

## 0.03- $\mu\text{V}/^\circ\text{C}$ Drift, Low-Noise, Rail-to-Rail Output, 36-V, Zero-Drift OPERATIONAL AMPLIFIERS

Check for Samples: [OPA4188](#)

### FEATURES

- **Low Offset Voltage:** 25  $\mu\text{V}$  (max)
- **Zero-Drift:** 0.03  $\mu\text{V}/^\circ\text{C}$
- **Low Noise:** 8.8  $\text{nV}/\sqrt{\text{Hz}}$   
0.1-Hz to 10-Hz Noise: 0.25  $\mu\text{V}_{\text{PP}}$
- **Excellent DC Precision:**  
PSRR: 142 dB  
CMRR: 146 dB  
Open-Loop Gain: 136 dB
- **Gain Bandwidth:** 2 MHz
- **Quiescent Current:** 475  $\mu\text{A}$  (max)
- **Wide Supply Range:**  $\pm 2\text{ V}$  to  $\pm 18\text{ V}$
- **Rail-to-Rail Output:**  
Input Includes Negative Rail
- **RFI Filtered Inputs**
- **MicroSIZE Packages**

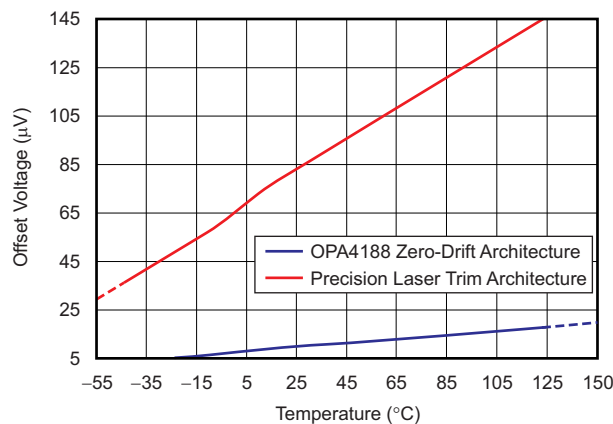
### APPLICATIONS

- **Bridge Amplifiers**
- **Strain Gauges**
- **Test Equipment**
- **Transducer Applications**
- **Temperature Measurement**
- **Electronic Scales**
- **Medical Instrumentation**
- **Resistance Temperature Detectors**
- **Precision Active Filters**

### DESCRIPTION

The OPA4188 operational amplifier uses TI proprietary auto-zeroing techniques to provide low offset voltage (25  $\mu\text{V}$ , max), and near zero-drift over time and temperature. These miniature, high-precision, low quiescent current amplifiers offer high input impedance and rail-to-rail output swing within 15 mV of the rails. The input common-mode range includes the negative rail. Either single or dual supplies can be used in the range of +4.0 V to +36 V ( $\pm 2\text{ V}$  to  $\pm 18\text{ V}$ ).

The quad version is available in SO-14 and TSSOP-14 packages. All versions are specified for operation from  $-40^\circ\text{C}$  to  $+125^\circ\text{C}$ .



### Zero-Drift Amplifier Portfolio

VERSION	PRODUCT	OFFSET VOLTAGE ( $\mu\text{V}$ )	OFFSET VOLTAGE DRIFT ( $\mu\text{V}/^\circ\text{C}$ )	BANDWIDTH (MHz)
Single	<a href="#">OPA188</a> (4 V to 36 V)	25	0.085	2
	<a href="#">OPA333</a> (5 V)	10	0.05	0.35
	<a href="#">OPA378</a> (5 V)	50	0.25	0.9
	<a href="#">OPA735</a> (12 V)	5	0.05	1.6
Dual	<a href="#">OPA2188</a> (4 V to 36 V)	25	0.085	2
	<a href="#">OPA2333</a> (5 V)	10	0.05	0.35
	<a href="#">OPA2378</a> (5 V)	50	0.25	0.9
	<a href="#">OPA2735</a> (12 V)	5	0.05	1.6
Quad	<a href="#">OPA4188</a> (4 V to 36 V)	25	0.085	2
	<a href="#">OPA4330</a> (5 V)	50	0.25	0.35



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This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

### PACKAGE INFORMATION<sup>(1)</sup>

PRODUCT	PACKAGE-LEAD	PACKAGE DESIGNATOR	SPECIFIED TEMPERATURE RANGE	PACKAGE MARKING	ORDERING NUMBER	TRANSPORT MEDIA, QUANTITY
OPA4188	SO-14	D	–40°C to +125°C	OPA4188	OPA4188AID	Rails, 50
					OPA4188AIDR	Tape and Reel, 2500
	TSSOP-14	PW	–40°C to +125°C	OPA4188	OPA4188AIPW	Rails, 90
					OPA4188AIPWR	Tape and Reel, 2000

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or visit the device product folder at [www.ti.com](http://www.ti.com).

### ABSOLUTE MAXIMUM RATINGS<sup>(1)</sup>

		VALUE	UNIT
Supply voltage		±20, 40 (single supply)	V
Signal input terminals <sup>(2)</sup>	Voltage	(V–) – 0.5 to (V+) + 0.5	V
	Current	±10	mA
Output short-circuit <sup>(3)</sup>		Continuous	
Temperature range	Operating, T <sub>A</sub>	–55 to +150	°C
	Storage, T <sub>stg</sub>	–65 to +150	°C
	Junction, T <sub>J</sub>	+150	°C
Electrostatic discharge (ESD) ratings	Human body model (HBM)	2	kV
	Charged device model (CDM)	1	kV

- (1) Stresses above these ratings may cause permanent damage. Exposure to absolute maximum conditions for extended periods may degrade device reliability. These are stress ratings only and functional operation of the device at these or any other conditions beyond those specified is not implied.
- (2) Input terminals are diode-clamped to the power-supply rails. Input signals that can swing more than 0.5 V beyond the supply rails should be current-limited to 10 mA or less.
- (3) Short-circuit to ground, one amplifier per package.

**ELECTRICAL CHARACTERISTICS:  
High-Voltage Operation,  $V_S = \pm 4\text{ V}$  to  $\pm 18\text{ V}$  ( $V_S = +8\text{ V}$  to  $+36\text{ V}$ )**

At  $T_A = +25^\circ\text{C}$ ,  $R_L = 10\text{ k}\Omega$  connected to  $V_S / 2$ , and  $V_{\text{COM}} = V_{\text{OUT}} = V_S / 2$ , unless otherwise noted.

PARAMETER		CONDITIONS	OPA4188			UNIT
			MIN	TYP	MAX	
<b>OFFSET VOLTAGE</b>						
$V_{\text{OS}}$	Input offset voltage			6	25	$\mu\text{V}$
$dV_{\text{OS}}/dT$		$T_A = -40^\circ\text{C}$ to $+125^\circ\text{C}$		0.03	0.085	$\mu\text{V}/^\circ\text{C}$
PSRR	Power-supply rejection ratio	$V_S = 4\text{ V}$ to $36\text{ V}$ , $V_{\text{CM}} = V_S / 2$		0.075	0.3	$\mu\text{V}/\text{V}$
		$V_S = 4\text{ V}$ to $36\text{ V}$ , $V_{\text{CM}} = V_S / 2$ , $T_A = -40^\circ\text{C}$ to $+125^\circ\text{C}$			0.3	$\mu\text{V}/\text{V}$
	Long-term stability			4 <sup>(1)</sup>		$\mu\text{V}$
	Channel separation, dc			1		$\mu\text{V}/\text{V}$
<b>INPUT BIAS CURRENT</b>						
$I_B$	Input bias current	$V_{\text{CM}} = V_S / 2$		$\pm 160$	$\pm 1400$	$\text{pA}$
		$T_A = -40^\circ\text{C}$ to $+125^\circ\text{C}$			$\pm 8$	$\text{nA}$
$I_{\text{OS}}$	Input offset current			$\pm 320$	$\pm 2800$	$\text{pA}$
		$T_A = -40^\circ\text{C}$ to $+125^\circ\text{C}$			$\pm 6$	$\text{nA}$
<b>NOISE</b>						
$e_n$	Input voltage noise	$f = 0.1\text{ Hz}$ to $10\text{ Hz}$		0.25		$\mu\text{V}_{\text{PP}}$
$e_n$	Input voltage noise density	$f = 1\text{ kHz}$		8.8		$\text{nV}/\sqrt{\text{Hz}}$
$i_n$	Input current noise density	$f = 1\text{ kHz}$		7		$\text{fA}/\sqrt{\text{Hz}}$
<b>INPUT VOLTAGE RANGE</b>						
$V_{\text{CM}}$	Common-mode voltage range	$T_A = -40^\circ\text{C}$ to $+125^\circ\text{C}$	$V^-$		$(V^+) - 1.5$	$\text{V}$
CMRR	Common-mode rejection ratio	$(V^-) < V_{\text{CM}} < (V^+) - 1.5\text{ V}$	120	134		$\text{dB}$
		$(V^-) + 0.5\text{ V} < V_{\text{CM}} < (V^+) - 1.5\text{ V}$ , $V_S = \pm 18\text{ V}$	130	146		$\text{dB}$
		$(V^-) + 0.5\text{ V} < V_{\text{CM}} < (V^+) - 1.5\text{ V}$ , $V_S = \pm 18\text{ V}$ , $T_A = -40^\circ\text{C}$ to $+125^\circ\text{C}$	120	126		$\text{dB}$
<b>INPUT IMPEDANCE</b>						
	Input impedance	Differential		100    6		$\text{M}\Omega \parallel \text{pF}$
		Common-mode		6    9.5		$10^{12}\ \Omega \parallel \text{pF}$
<b>OPEN-LOOP GAIN</b>						
$A_{\text{OL}}$	Open-loop voltage gain	$(V^-) + 500\text{ mV} < V_{\text{O}} < (V^+) - 500\text{ mV}$ , $R_L = 10\text{ k}\Omega$	130	136		$\text{dB}$
		$(V^-) + 500\text{ mV} < V_{\text{O}} < (V^+) - 500\text{ mV}$ , $R_L = 10\text{ k}\Omega$ , $T_A = -40^\circ\text{C}$ to $+125^\circ\text{C}$	118	126		$\text{dB}$
<b>FREQUENCY RESPONSE</b>						
GBW	Gain-bandwidth product			2		$\text{MHz}$
SR	Slew rate	$G = +1$		0.8		$\text{V}/\mu\text{s}$
$t_s$	Settling time	0.1%	$V_S = \pm 18\text{ V}$ , $G = 1$ , 10-V step	20		$\mu\text{s}$
		0.01%	$V_S = \pm 18\text{ V}$ , $G = 1$ , 10-V step	27		$\mu\text{s}$
	Overload recovery time	$V_{\text{IN}} \times G = V_S$		1		$\mu\text{s}$
THD+N	Total harmonic distortion + noise	1 kHz, $G = 1$ , $V_{\text{OUT}} = 1\text{ V}_{\text{RMS}}$		0.0001		%

(1) 1000-hour life test at  $+125^\circ\text{C}$  demonstrated randomly distributed variation in the range of measurement limits—approximately  $4\ \mu\text{V}$ .

**ELECTRICAL CHARACTERISTICS:**  
**High-Voltage Operation,  $V_S = \pm 4\text{ V}$  to  $\pm 18\text{ V}$  ( $V_S = +8\text{ V}$  to  $+36\text{ V}$ ) (continued)**

 At  $T_A = +25^\circ\text{C}$ ,  $R_L = 10\text{ k}\Omega$  connected to  $V_S / 2$ , and  $V_{\text{COM}} = V_{\text{OUT}} = V_S / 2$ , unless otherwise noted.

PARAMETER		CONDITIONS	OPA4188			UNIT
			MIN	TYP	MAX	
<b>OUTPUT</b>						
Voltage output swing from rail		No load		6	15	mV
		$R_L = 10\text{ k}\Omega$		220	250	mV
		$R_L = 10\text{ k}\Omega$ , $T_A = -40^\circ\text{C}$ to $+125^\circ\text{C}$		310	350	mV
$I_{\text{SC}}$	Short-circuit current			$\pm 18$		mA
$R_O$	Open-loop output resistance	$f = 1\text{ MHz}$ , $I_O = 0$		120		$\Omega$
$C_{\text{LOAD}}$	Capacitive load drive			1		nF
<b>POWER SUPPLY</b>						
$V_S$	Operating voltage range			4 to 36 ( $\pm 2$ to $\pm 18$ )		V
$I_Q$	Quiescent current (per amplifier)	$V_S = \pm 4\text{ V}$ to $V_S = \pm 18\text{ V}$		415	475	$\mu\text{A}$
		$I_O = 0\text{ mA}$ , $T_A = -40^\circ\text{C}$ to $+125^\circ\text{C}$			525	$\mu\text{A}$
<b>TEMPERATURE RANGE</b>						
Temperature range	Specified			-40	+125	$^\circ\text{C}$
	Operating			-55	+150	$^\circ\text{C}$
	Storage			-65	+150	$^\circ\text{C}$

**ELECTRICAL CHARACTERISTICS:  
Low-Voltage Operation,  $V_S = \pm 2\text{ V}$  to  $< \pm 4\text{ V}$  ( $V_S = +4\text{ V}$  to  $< +8\text{ V}$ )**

 At  $T_A = +25^\circ\text{C}$ ,  $R_L = 10\text{ k}\Omega$  connected to  $V_S / 2$ , and  $V_{\text{COM}} = V_{\text{OUT}} = V_S / 2$ , unless otherwise noted.

PARAMETER		CONDITIONS	OPA4188			UNIT
			MIN	TYP	MAX	
<b>OFFSET VOLTAGE</b>						
$V_{\text{OS}}$	Input offset voltage			6	25	$\mu\text{V}$
$dV_{\text{OS}}/dT$		$T_A = -40^\circ\text{C}$ to $+125^\circ\text{C}$		0.03	0.085	$\mu\text{V}/^\circ\text{C}$
PSRR	Power-supply rejection ratio	$V_S = 4\text{ V}$ to $36\text{ V}$ , $V_{\text{CM}} = V_S / 2$		0.075	0.3	$\mu\text{V}/\text{V}$
		$V_S = 4\text{ V}$ to $36\text{ V}$ , $V_{\text{CM}} = V_S / 2$ , $T_A = -40^\circ\text{C}$ to $+125^\circ\text{C}$			0.3	$\mu\text{V}/\text{V}$
	Long-term stability			4 <sup>(1)</sup>		$\mu\text{V}$
	Channel separation, dc			1		$\mu\text{V}/\text{V}$
<b>INPUT BIAS CURRENT</b>						
$I_B$	Input bias current	$V_{\text{CM}} = V_S / 2$		$\pm 160$	$\pm 1400$	$\text{pA}$
		$T_A = -40^\circ\text{C}$ to $+125^\circ\text{C}$			$\pm 8$	$\text{nA}$
$I_{\text{OS}}$	Input offset current			$\pm 320$	$\pm 2800$	$\text{pA}$
		$T_A = -40^\circ\text{C}$ to $+125^\circ\text{C}$			$\pm 6$	$\text{nA}$
<b>NOISE</b>						
$e_n$	Input voltage noise	$f = 0.1\text{ Hz}$ to $10\text{ Hz}$		0.25		$\mu\text{V}_{\text{PP}}$
$e_n$	Input voltage noise density	$f = 1\text{ kHz}$		8.8		$\text{nV}/\sqrt{\text{Hz}}$
$i_n$	Input current noise density	$f = 1\text{ kHz}$		7		$\text{fA}/\sqrt{\text{Hz}}$
<b>INPUT VOLTAGE RANGE</b>						
$V_{\text{CM}}$	Common-mode voltage range		$V^-$		$(V^+) - 1.5$	$\text{V}$
CMRR	Common-mode rejection ratio	$(V^-) < V_{\text{CM}} < (V^+) - 1.5\text{ V}$	106	114		$\text{dB}$
		$(V^-) + 0.5\text{ V} < V_{\text{CM}} < (V^+) - 1.5\text{ V}$ , $V_S = \pm 2\text{ V}$	114	120		$\text{dB}$
		$(V^-) + 0.5\text{ V} < V_{\text{CM}} < (V^+) - 1.5\text{ V}$ , $V_S = \pm 2\text{ V}$ , $T_A = -40^\circ\text{C}$ to $+125^\circ\text{C}$	108	120		$\text{dB}$
<b>INPUT IMPEDANCE</b>						
	Input impedance	Differential		$100 \parallel 6$		$\text{M}\Omega \parallel \text{pF}$
		Common-mode		$6 \parallel 9.5$		$10^{12}\ \Omega \parallel \text{pF}$
<b>OPEN-LOOP GAIN</b>						
$A_{\text{OL}}$	Open-loop voltage gain	$(V^-) + 500\text{ mV} < V_{\text{O}} < (V^+) - 500\text{ mV}$ , $R_L = 10\text{ k}\Omega$	120	130		$\text{dB}$
		$(V^-) + 500\text{ mV} < V_{\text{O}} < (V^+) - 500\text{ mV}$ , $R_L = 10\text{ k}\Omega$ , $T_A = -40^\circ\text{C}$ to $+125^\circ\text{C}$	110	120		$\text{dB}$
<b>FREQUENCY RESPONSE</b>						
GBW	Gain-bandwidth product			2		$\text{MHz}$
SR	Slew rate	$G = +1$		0.8		$\text{V}/\mu\text{s}$
	Overload recovery time	$V_{\text{IN}} \times G = V_S$		1		$\mu\text{s}$
THD+N	Total harmonic distortion + noise	1 kHz, $G = 1$ , $V_{\text{OUT}} = 1\text{ V}_{\text{RMS}}$		0.0001		%

 (1) 1000-hour life test at  $+125^\circ\text{C}$  demonstrated randomly distributed variation in the range of measurement limits—approximately  $4\ \mu\text{V}$ .

**ELECTRICAL CHARACTERISTICS:**  
**Low-Voltage Operation,  $V_S = \pm 2\text{ V}$  to  $< \pm 4\text{ V}$  ( $V_S = +4\text{ V}$  to  $< +8\text{ V}$ ) (continued)**

At  $T_A = +25^\circ\text{C}$ ,  $R_L = 10\text{ k}\Omega$  connected to  $V_S / 2$ , and  $V_{COM} = V_{OUT} = V_S / 2$ , unless otherwise noted.

PARAMETER		CONDITIONS	OPA4188			UNIT
			MIN	TYP	MAX	
<b>OUTPUT</b>						
Voltage output swing from rail	No load			6	15	mV
	$R_L = 10\text{ k}\Omega$			220	250	mV
	$R_L = 10\text{ k}\Omega$ , $T_A = -40^\circ\text{C}$ to $+125^\circ\text{C}$			310	350	mV
$I_{SC}$	Short-circuit current		$\pm 18$			mA
$R_O$	Open-loop output resistance	$f = 1\text{ MHz}$ , $I_O = 0$		120		$\Omega$
$C_{LOAD}$	Capacitive load drive			1		nF
<b>POWER SUPPLY</b>						
$V_S$	Operating voltage range		4 to 36 ( $\pm 2$ to $\pm 18$ )			V
$I_Q$	Quiescent current (per amplifier)	$V_S = \pm 2\text{ V}$ to $V_S = \pm 4\text{ V}$		385	440	$\mu\text{A}$
		$I_O = 0\text{ mA}$ , $T_A = -40^\circ\text{C}$ to $+125^\circ\text{C}$			525	$\mu\text{A}$
<b>TEMPERATURE RANGE</b>						
Temperature range	Specified		-40		+125	$^\circ\text{C}$
	Operating		-40		+125	$^\circ\text{C}$
	Storage		-65		+150	$^\circ\text{C}$

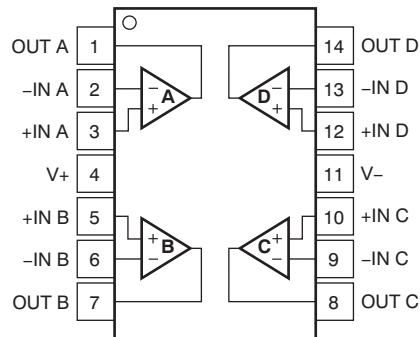
**THERMAL INFORMATION**

THERMAL METRIC <sup>(1)</sup>		OPA4188		UNITS
		D (SO)	PW (TSSOP)	
		14 PINS	14 PINS	
$\theta_{JA}$	Junction-to-ambient thermal resistance	93.2	106.9	$^\circ\text{C}/\text{W}$
$\theta_{JCTop}$	Junction-to-case (top) thermal resistance	51.8	24.4	
$\theta_{JB}$	Junction-to-board thermal resistance	49.4	59.3	
$\psi_{JT}$	Junction-to-top characterization parameter	13.5	0.6	
$\psi_{JB}$	Junction-to-board characterization parameter	42.2	54.3	
$\theta_{JCbott}$	Junction-to-case (bottom) thermal resistance	N/A	N/A	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, [SPRA953](#).

**PIN CONFIGURATION**

**D, PW PACKAGES**  
**SO-14, TSSOP-14**  
**(TOP VIEW)**



## TYPICAL CHARACTERISTICS

**Table 1. Characteristic Performance Measurements**

DESCRIPTION	FIGURE
Offset Voltage Production Distribution	<a href="#">Figure 1</a>
Offset Voltage Drift Distribution	<a href="#">Figure 2</a>
Offset Voltage vs Temperature	<a href="#">Figure 3</a>
Offset Voltage vs Common-Mode Voltage	<a href="#">Figure 4, Figure 5</a>
Offset Voltage vs Power Supply	<a href="#">Figure 6</a>
$I_B$ and $I_{OS}$ vs Common-Mode Voltage	<a href="#">Figure 7</a>
Input Bias Current vs Temperature	<a href="#">Figure 8</a>
Output Voltage Swing vs Output Current (Maximum Supply)	<a href="#">Figure 9</a>
CMRR and PSRR vs Frequency (Referred-to-Input)	<a href="#">Figure 10</a>
CMRR vs Temperature	<a href="#">Figure 11, Figure 12</a>
PSRR vs Temperature	<a href="#">Figure 13</a>
0.1-Hz to 10-Hz Noise	<a href="#">Figure 14</a>
Input Voltage Noise Spectral Density vs Frequency	<a href="#">Figure 15</a>
THD+N Ratio vs Frequency	<a href="#">Figure 16</a>
THD+N vs Output Amplitude	<a href="#">Figure 17</a>
Quiescent Current vs Supply Voltage	<a href="#">Figure 18</a>
Quiescent Current vs Temperature	<a href="#">Figure 19</a>
Open-Loop Gain and Phase vs Frequency	<a href="#">Figure 20</a>
Closed-Loop Gain vs Frequency	<a href="#">Figure 21</a>
Open-Loop Gain vs Temperature	<a href="#">Figure 22</a>
Open-Loop Output Impedance vs Frequency	<a href="#">Figure 23</a>
Small-Signal Overshoot vs Capacitive Load (100-mV Output Step)	<a href="#">Figure 24, Figure 25</a>
No Phase Reversal	<a href="#">Figure 26</a>
Positive Overload Recovery	<a href="#">Figure 27</a>
Negative Overload Recovery	<a href="#">Figure 28</a>
Small-Signal Step Response (100 mV)	<a href="#">Figure 29, Figure 30</a>
Large-Signal Step Response	<a href="#">Figure 31, Figure 32</a>
Large-Signal Settling Time (10-V Positive Step)	<a href="#">Figure 33</a>
Large-Signal Settling Time (10-V Negative Step)	<a href="#">Figure 34</a>
Short-Circuit Current vs Temperature	<a href="#">Figure 35</a>
Maximum Output Voltage vs Frequency	<a href="#">Figure 36</a>
Channel Separation vs Frequency	<a href="#">Figure 37</a>
EMIRR IN+ vs Frequency	<a href="#">Figure 38</a>

### TYPICAL CHARACTERISTICS

$V_S = \pm 18\text{ V}$ ,  $V_{CM} = V_S / 2$ ,  $R_{LOAD} = 10\text{ k}\Omega$  connected to  $V_S / 2$ , and  $C_L = 100\text{ pF}$ , unless otherwise noted.

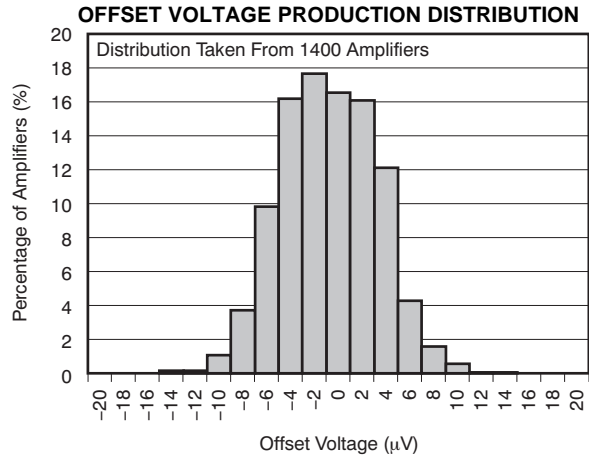


Figure 1.

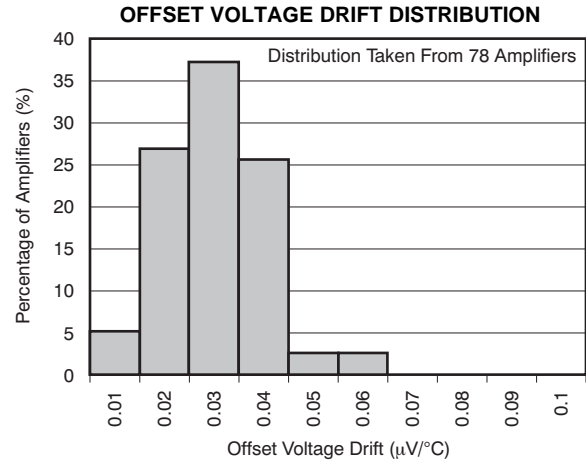


Figure 2.

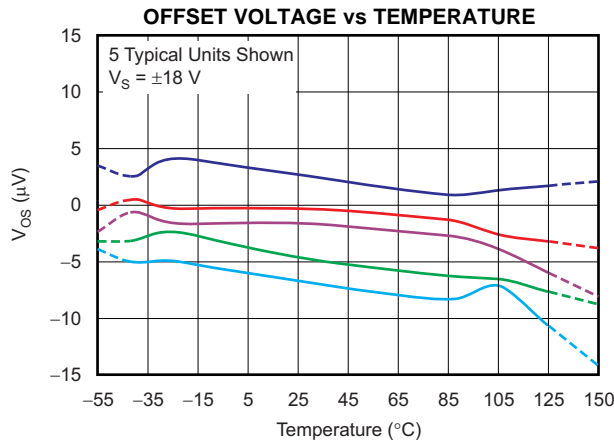


Figure 3.

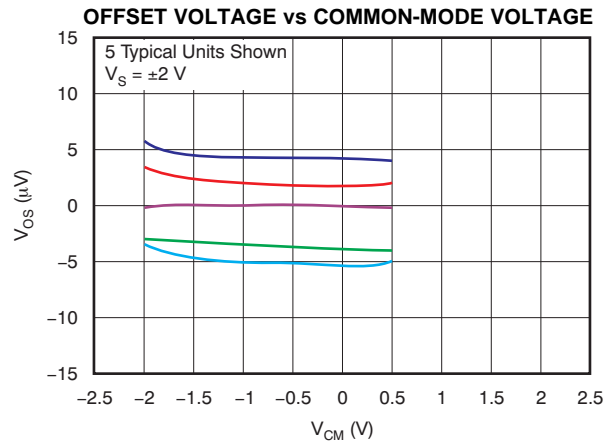


Figure 4.

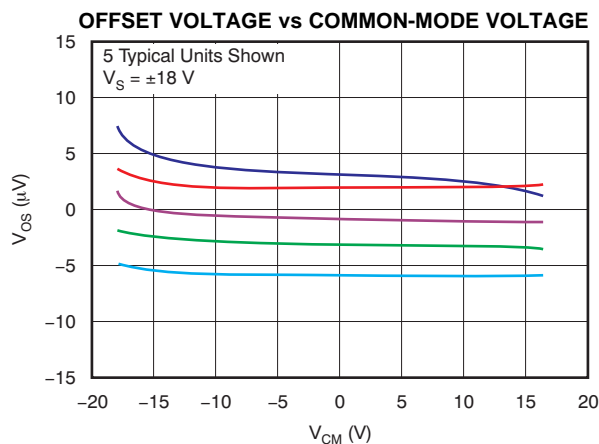


Figure 5.

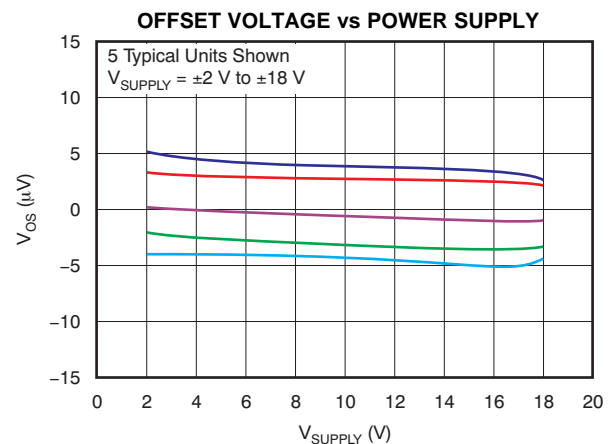


Figure 6.



**TYPICAL CHARACTERISTICS (continued)**

$V_S = \pm 18\text{ V}$ ,  $V_{CM} = V_S / 2$ ,  $R_{LOAD} = 10\text{ k}\Omega$  connected to  $V_S / 2$ , and  $C_L = 100\text{ pF}$ , unless otherwise noted.

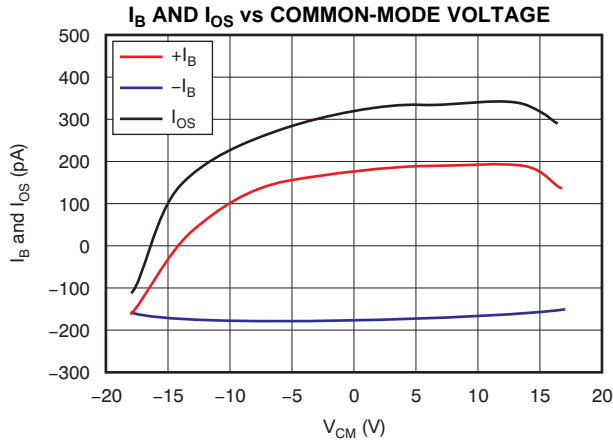


Figure 7.

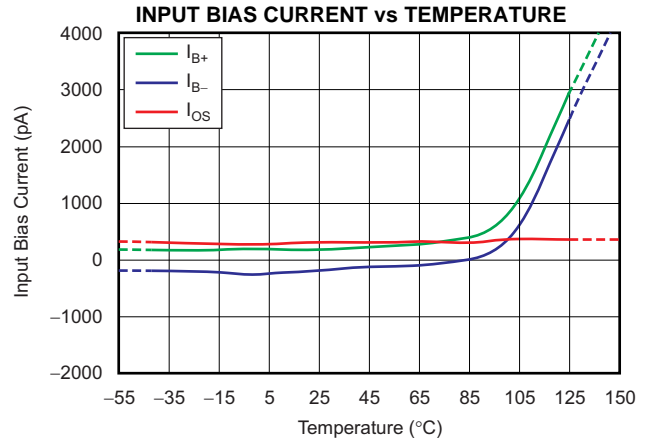


Figure 8.

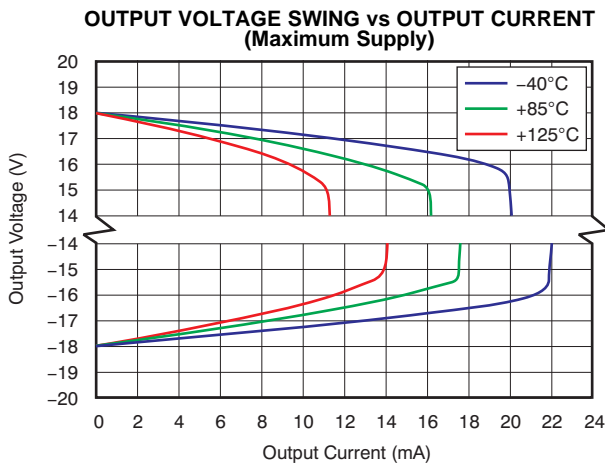


Figure 9.

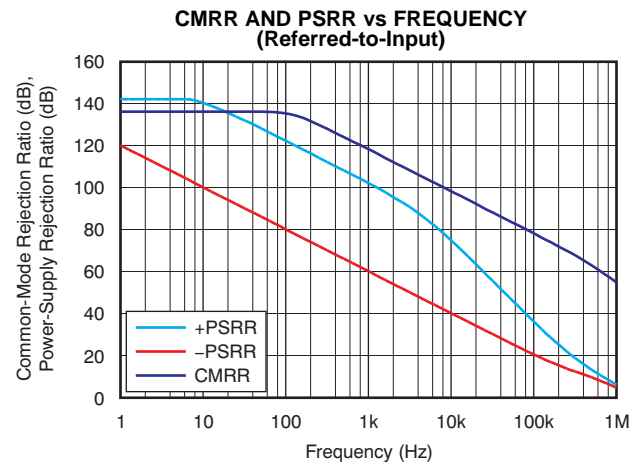


Figure 10.

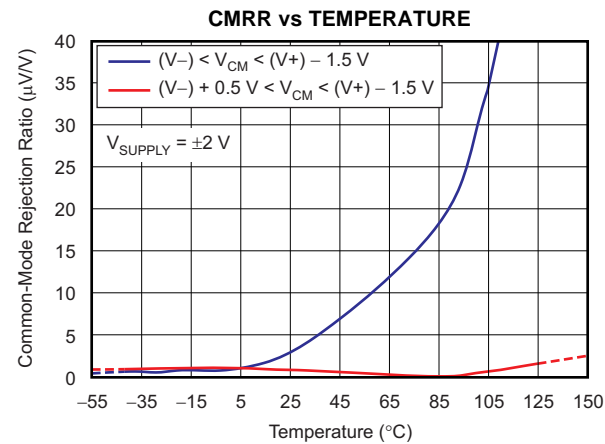


Figure 11.

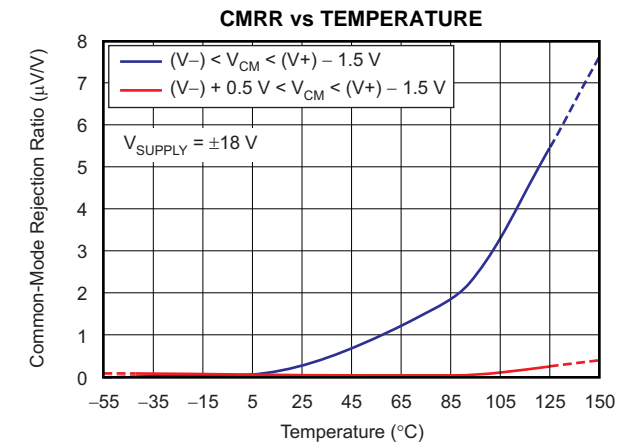


Figure 12.

**TYPICAL CHARACTERISTICS (continued)**

$V_S = \pm 18\text{ V}$ ,  $V_{CM} = V_S / 2$ ,  $R_{LOAD} = 10\text{ k}\Omega$  connected to  $V_S / 2$ , and  $C_L = 100\text{ pF}$ , unless otherwise noted.

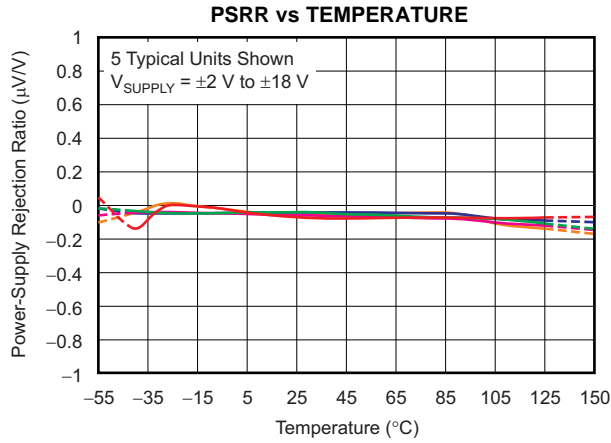


Figure 13.

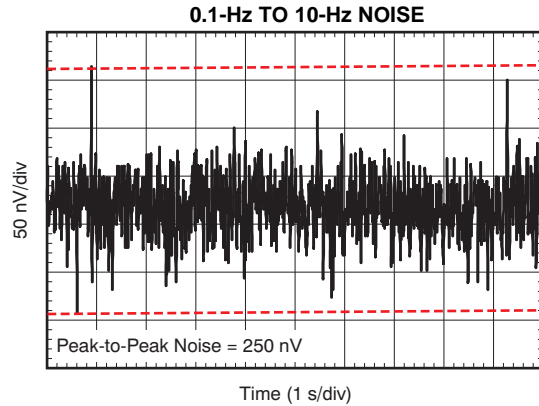


Figure 14.

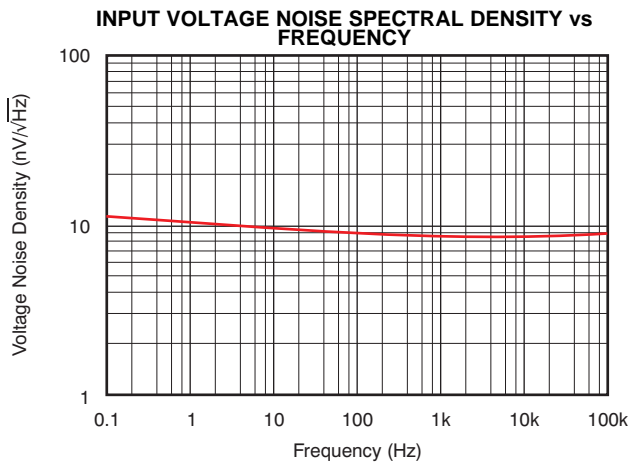


Figure 15.

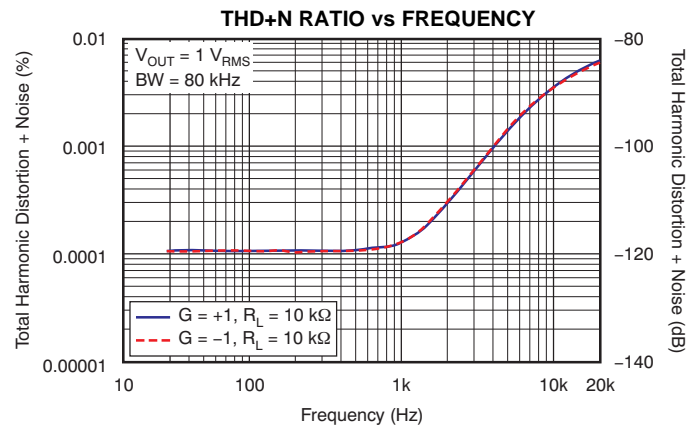


Figure 16.

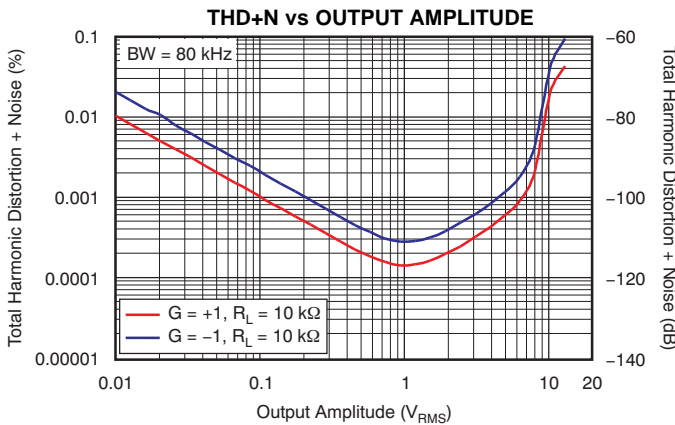


Figure 17.

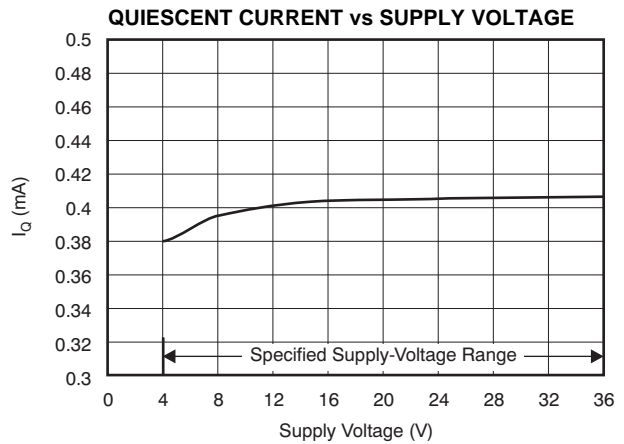


Figure 18.

**TYPICAL CHARACTERISTICS (continued)**

$V_S = \pm 18\text{ V}$ ,  $V_{CM} = V_S / 2$ ,  $R_{LOAD} = 10\text{ k}\Omega$  connected to  $V_S / 2$ , and  $C_L = 100\text{ pF}$ , unless otherwise noted.

**QUIESCENT CURRENT vs TEMPERATURE**

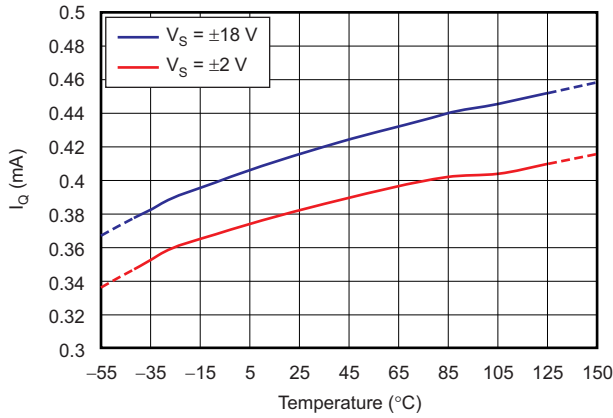


Figure 19.

**OPEN-LOOP GAIN AND PHASE vs FREQUENCY**

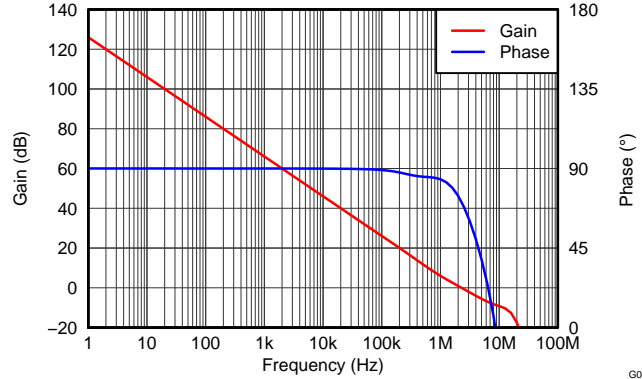


Figure 20.

**CLOSED-LOOP GAIN vs FREQUENCY**

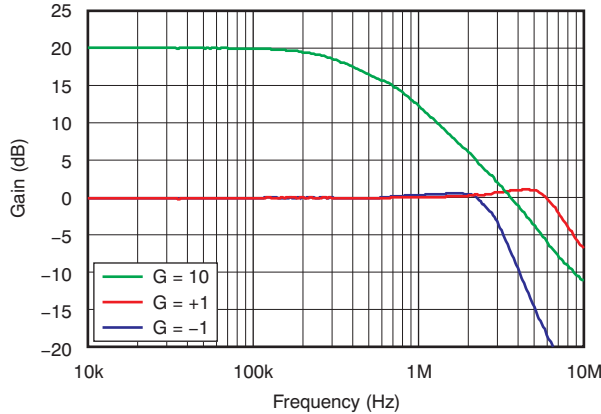


Figure 21.

**OPEN-LOOP GAIN vs TEMPERATURE**

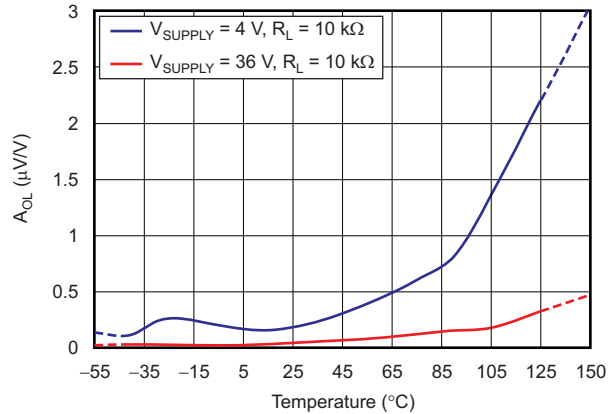


Figure 22.

**OPEN-LOOP OUTPUT IMPEDANCE vs FREQUENCY**

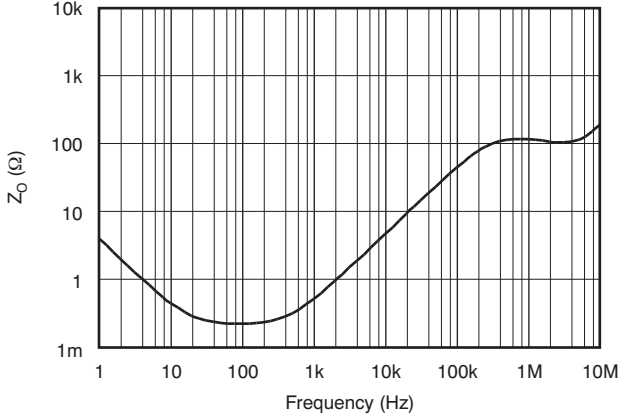


Figure 23.

**SMALL-SIGNAL OVERSHOOT vs CAPACITIVE LOAD (100-mV Output Step)**

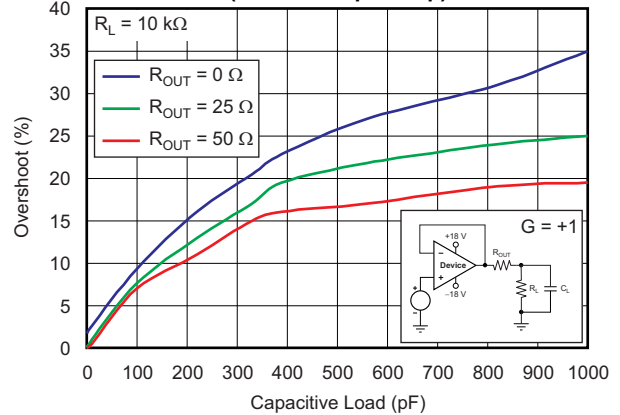


Figure 24.

**TYPICAL CHARACTERISTICS (continued)**

$V_S = \pm 18\text{ V}$ ,  $V_{CM} = V_S / 2$ ,  $R_{LOAD} = 10\text{ k}\Omega$  connected to  $V_S / 2$ , and  $C_L = 100\text{ pF}$ , unless otherwise noted.

**SMALL-SIGNAL OVERSHOOT vs CAPACITIVE LOAD  
(100-mV Output Step)**

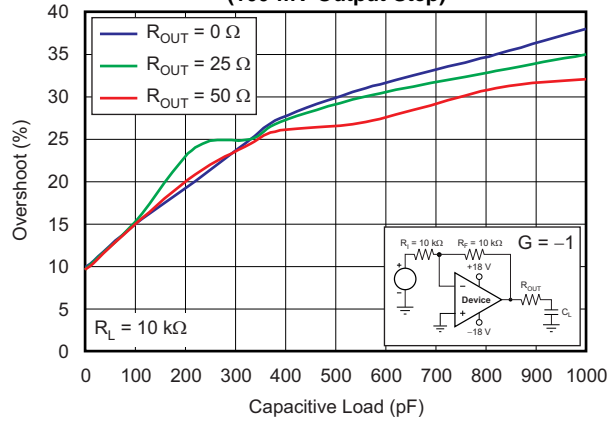


Figure 25.

**NO PHASE REVERSAL**

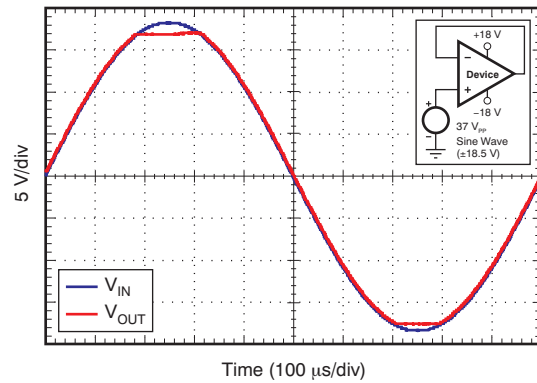


Figure 26.

**POSITIVE OVERLOAD RECOVERY**

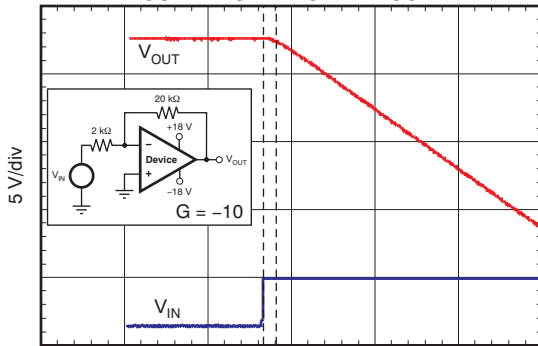


Figure 27.

**NEGATIVE OVERLOAD RECOVERY**

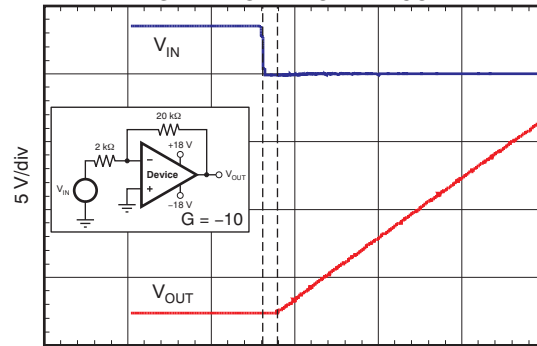


Figure 28.

**SMALL-SIGNAL STEP RESPONSE  
(100 mV)**

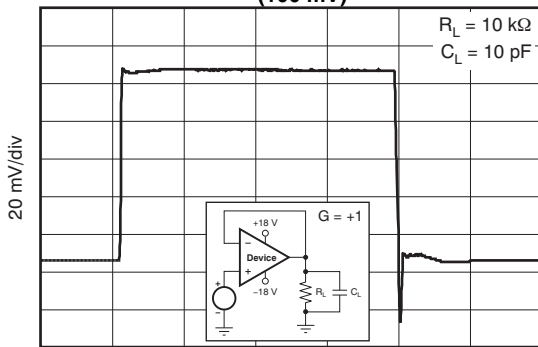


Figure 29.

**SMALL-SIGNAL STEP RESPONSE  
(100 mV)**

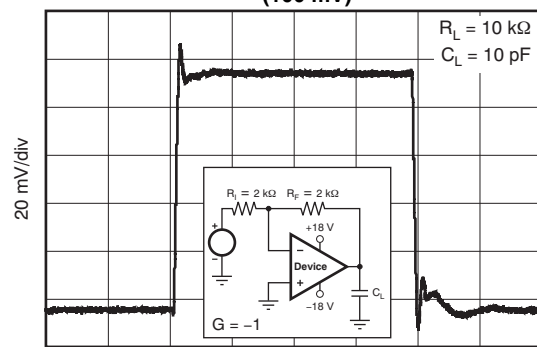
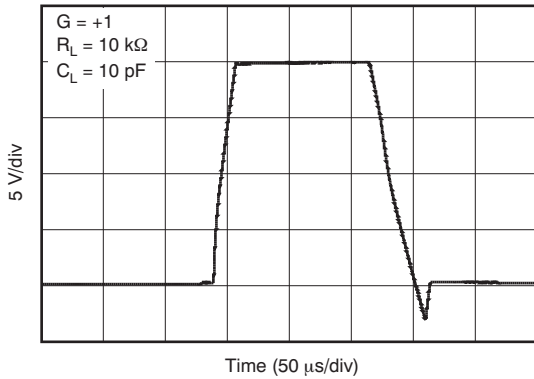


Figure 30.

**TYPICAL CHARACTERISTICS (continued)**

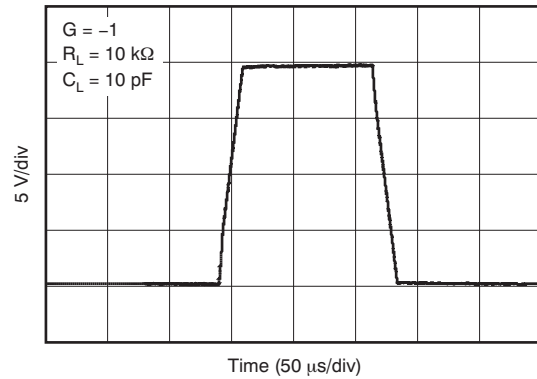
$V_S = \pm 18\text{ V}$ ,  $V_{CM} = V_S / 2$ ,  $R_{LOAD} = 10\text{ k}\Omega$  connected to  $V_S / 2$ , and  $C_L = 100\text{ pF}$ , unless otherwise noted.

**LARGE-SIGNAL STEP RESPONSE**



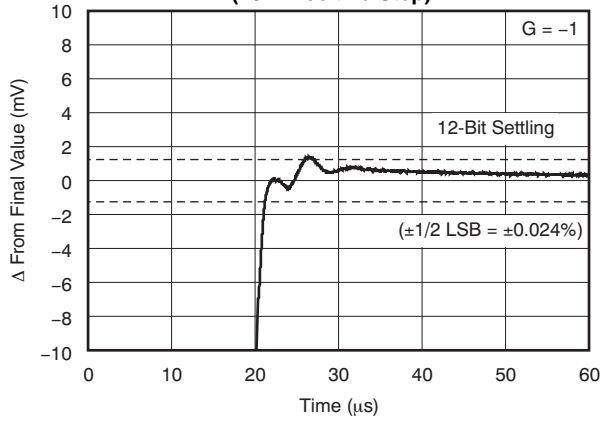
**Figure 31.**

**LARGE-SIGNAL STEP RESPONSE**



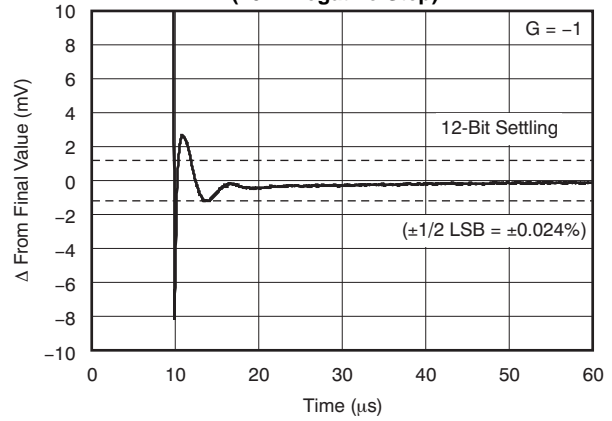
**Figure 32.**

**LARGE-SIGNAL SETTLING TIME (10-V Positive Step)**



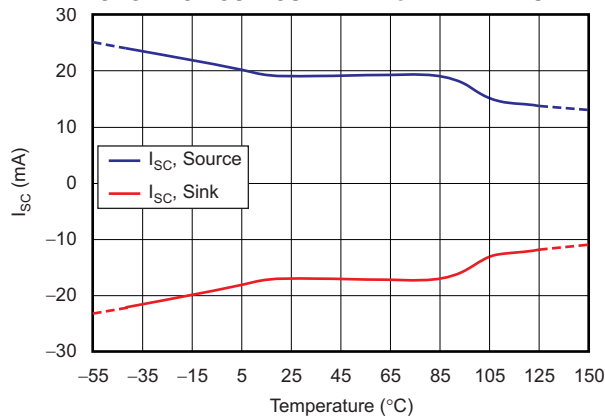
**Figure 33.**

**LARGE-SIGNAL SETTLING TIME (10-V Negative Step)**



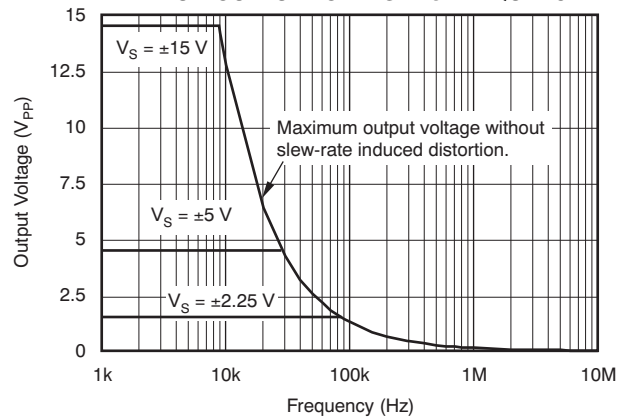
**Figure 34.**

**SHORT-CIRCUIT CURRENT vs TEMPERATURE**



**Figure 35.**

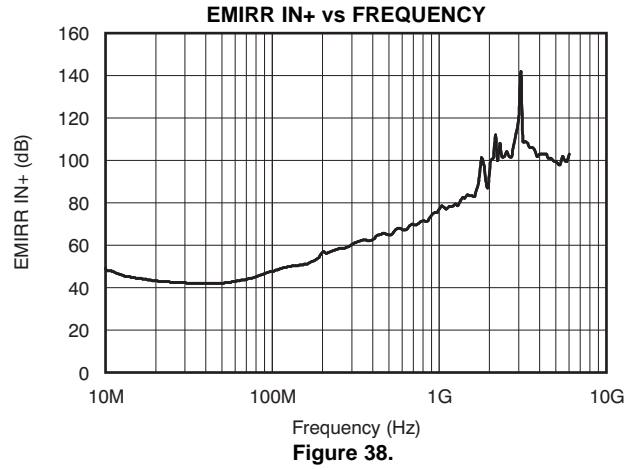
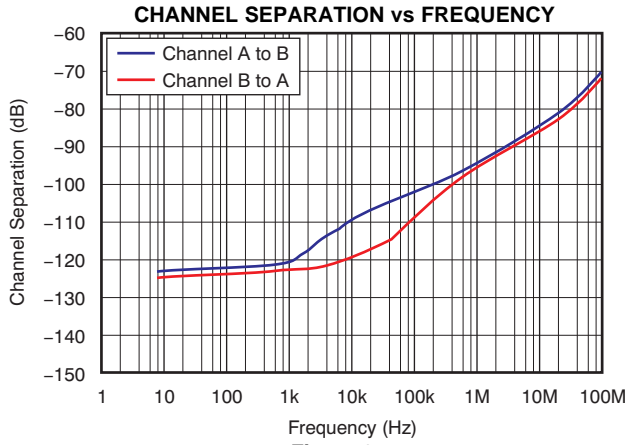
**MAXIMUM OUTPUT VOLTAGE vs FREQUENCY**



**Figure 36.**

**TYPICAL CHARACTERISTICS (continued)**

$V_S = \pm 18\text{ V}$ ,  $V_{CM} = V_S / 2$ ,  $R_{LOAD} = 10\text{ k}\Omega$  connected to  $V_S / 2$ , and  $C_L = 100\text{ pF}$ , unless otherwise noted.



## APPLICATION INFORMATION

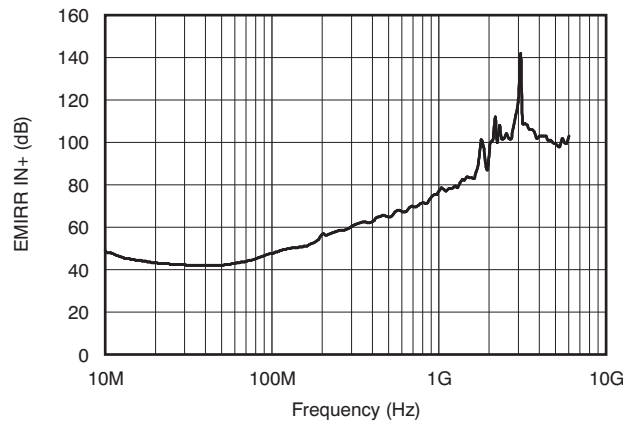
The OPA4188 operational amplifier combines precision offset and drift with excellent overall performance, making it ideal for many precision applications. The precision offset drift of only 0.085  $\mu\text{V}$  per degree Celsius provides stability over the entire temperature range. In addition, the device offers excellent overall performance with high CMRR, PSRR, and  $A_{OL}$ . As with all amplifiers, applications with noisy or high-impedance power supplies require decoupling capacitors close to the device pins. In most cases, 0.1- $\mu\text{F}$  capacitors are adequate.

### OPERATING CHARACTERISTICS

The OPA4188 is specified for operation from 4 V to 36 V ( $\pm 2$  V to  $\pm 18$  V). Many of the specifications apply from  $-40^\circ\text{C}$  to  $+125^\circ\text{C}$ . Parameters that can exhibit significant variance with regard to operating voltage or temperature are presented in the [Typical Characteristics](#).

### EMI REJECTION

The OPA4188 uses integrated electromagnetic interference (EMI) filtering to reduce the effects of EMI interference from sources such as wireless communications and densely-populated boards with a mix of analog signal chain and digital components. EMI immunity can be improved with circuit design techniques; the OPA4188 benefits from these design improvements. Texas Instruments has developed the ability to accurately measure and quantify the immunity of an operational amplifier over a broad frequency spectrum extending from 10 MHz to 6 GHz. [Figure 39](#) shows the results of this testing on the OPA4188. Detailed information can also be found in the [Application Report EMI Rejection Ratio of Operational Amplifiers \(SBOA128\)](#), available for download from [www.ti.com](http://www.ti.com).



**Figure 39. EMIRR Testing**

### GENERAL LAYOUT GUIDELINES

For best operational device performance, good printed circuit board (PCB) layout practices are recommended. Low-loss, 0.1- $\mu\text{F}$  bypass capacitors should be connected between each supply pin and ground, placed as close to the device as possible. A single bypass capacitor from V+ to ground is applicable to single-supply applications.

### PHASE-REVERSAL PROTECTION

The OPA4188 has an internal phase-reversal protection. Many op amps exhibit a phase reversal when the input is driven beyond its linear common-mode range. This condition is most often encountered in noninverting circuits when the input is driven beyond the specified common-mode voltage range, causing the output to reverse into the opposite rail. The OPA4188 input prevents phase reversal with excessive common-mode voltage. Instead, the output limits into the appropriate rail. This performance is shown in Figure 40.

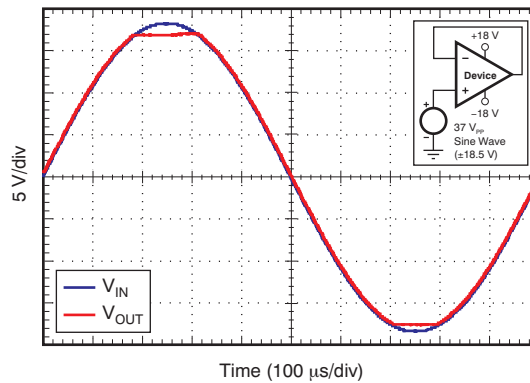


Figure 40. No Phase Reversal

### CAPACITIVE LOAD AND STABILITY

The OPA4188 dynamic characteristics have been optimized for a range of common operating conditions. The combination of low closed-loop gain and high capacitive loads decreases the amplifier phase margin and can lead to gain peaking or oscillations. As a result, heavier capacitive loads must be isolated from the output. The simplest way to achieve this isolation is to add a small resistor (for example,  $R_{OUT}$  equal to 50  $\Omega$ ) in series with the output. Figure 41 and Figure 42 illustrate graphs of small-signal overshoot versus capacitive load for several values of  $R_{OUT}$ . Also, refer to the Applications Report, *Feedback Plots Define Op Amp AC Performance (SBOA015)*, available for download from [www.ti.com](http://www.ti.com), for details of analysis techniques and application circuits.

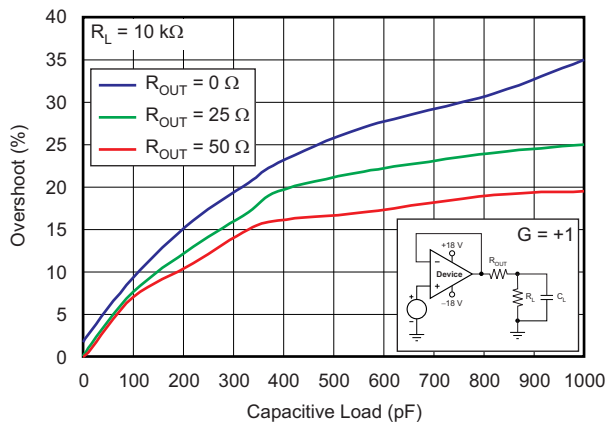


Figure 41. Small-Signal Overshoot versus Capacitive Load (100-mV Output Step)

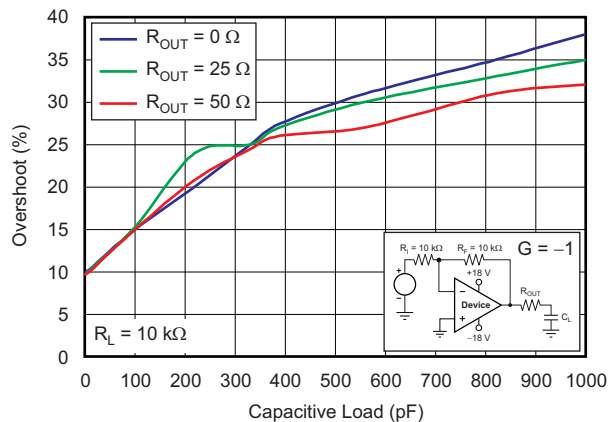


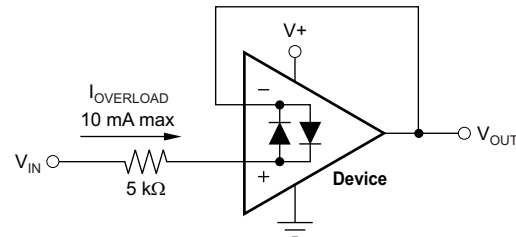
Figure 42. Small-Signal Overshoot versus Capacitive Load (100-mV Output Step)



## ELECTRICAL OVERSTRESS

Designers often ask questions about the capability of an operational amplifier to withstand electrical overstress. These questions tend to focus on the device inputs, but may involve the supply voltage pins or even the output pin. Each of these different pin functions have electrical stress limits determined by the voltage breakdown characteristics of the particular semiconductor fabrication process and specific circuits connected to the pin. Additionally, internal electrostatic discharge (ESD) protection is built into these circuits to protect them from accidental ESD events both before and during product assembly.

These ESD protection diodes also provide in-circuit, input overdrive protection, as long as the current is limited to 10 mA as stated in the [Absolute Maximum Ratings](#). [Figure 43](#) shows how a series input resistor may be added to the driven input to limit the input current. The added resistor contributes thermal noise at the amplifier input and its value should be kept to a minimum in noise-sensitive applications.



**Figure 43. Input Current Protection**

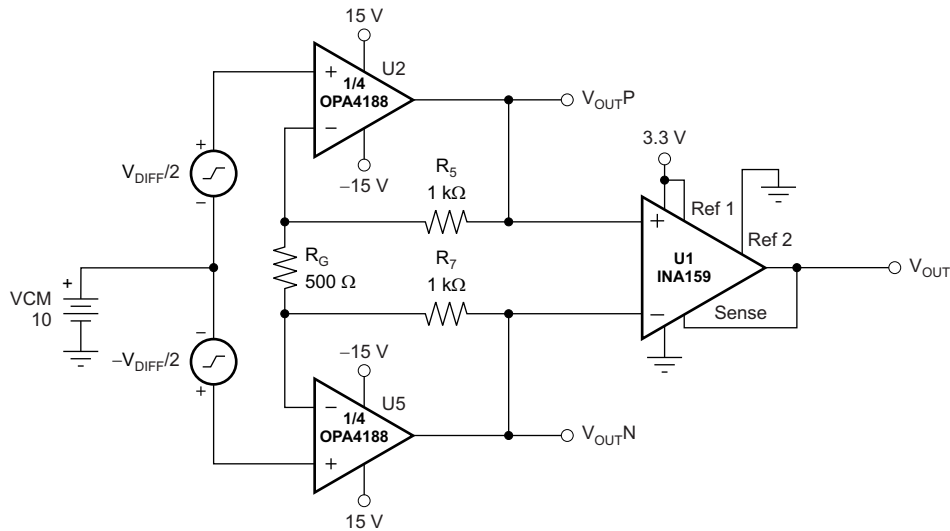
An ESD event produces a short-duration, high-voltage pulse that is transformed into a short-duration, high-current pulse as it discharges through a semiconductor device. The ESD protection circuits are designed to provide a current path around the operational amplifier core to prevent it from being damaged. The energy absorbed by the protection circuitry is then dissipated as heat.

When the operational amplifier connects into a circuit, the ESD protection components are intended to remain inactive and not become involved in the application circuit operation. However, circumstances may arise where an applied voltage exceeds the operating voltage range of a given pin. Should this condition occur, there is a risk that some of the internal ESD protection circuits may be biased on, and conduct current. Any such current flow occurs through ESD cells and rarely involves the absorption device.

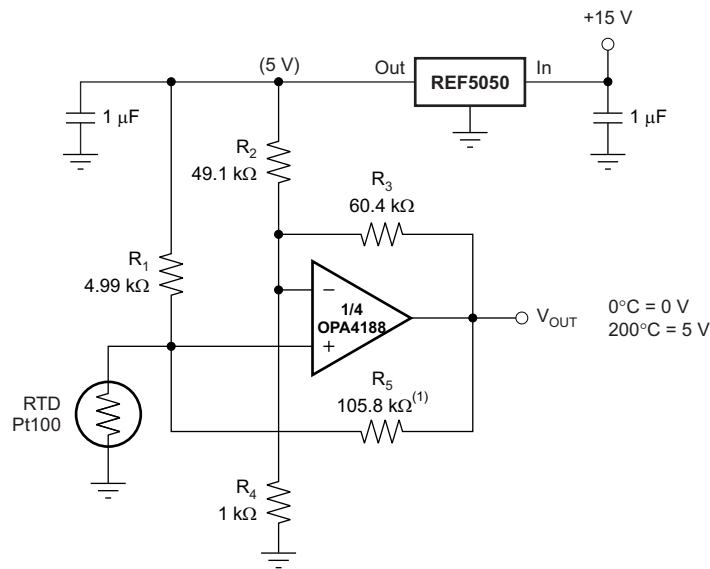
If there is an uncertainty about the ability of the supply to absorb this current, external zener diodes may be added to the supply pins. The zener voltage must be selected such that the diode does not turn on during normal operation. However, its zener voltage should be low enough so that the zener diode conducts if the supply pin begins to rise above the safe operating supply voltage level.

**APPLICATION EXAMPLES**

The application examples of [Figure 44](#) and [Figure 45](#) highlight only a few of the circuits where the OPA4188 can be used.



**Figure 44. Discrete INA + Attenuation for ADC with a 3.3-V Supply**



(1) R<sub>5</sub> provides positive-varying excitation to linearize output.

**Figure 45. RTD Amplifier with Linearization**

## REVISION HISTORY

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

<b>Changes from Revision A (September 2012) to Revision B</b>	<b>Page</b>
<ul style="list-style-type: none"> <li>• Changed maximum specification of second Input Bias Current, <math>I_B</math> parameter row in High-Voltage Electrical Characteristics table ..... 3</li> <li>• Changed maximum specification of second Input Bias Current, <math>I_B</math> parameter row in Low-Voltage Electrical Characteristics table ..... 5</li> <li>• Changed Input Impedance, <i>Input impedance</i> (Common-mode) parameter typical specification in Low-Voltage Electrical Characteristics table ..... 5</li> </ul>	
<b>Changes from Original (June2012) to Revision A</b>	<b>Page</b>
<ul style="list-style-type: none"> <li>• Changed second to last Applications bullet ..... 1</li> </ul>	

**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
OPA4188AID	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	OPA4188	<a href="#">Samples</a>
OPA4188AIDR	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	OPA4188	<a href="#">Samples</a>
OPA4188AIPW	ACTIVE	TSSOP	PW	14	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	OPA4188	<a href="#">Samples</a>
OPA4188AIPWR	ACTIVE	TSSOP	PW	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	OPA4188	<a href="#">Samples</a>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSELETE:** TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

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## TAPE AND REEL INFORMATION



### QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
OPA4188AIPWR	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
OPA4188AIPWR	TSSOP	PW	14	2000	367.0	367.0	35.0

D (R-PDSO-G14)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
  - Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
  - E. Reference JEDEC MS-012 variation AB.



D (R-PDSO-G14)

PLASTIC SMALL OUTLINE



- NOTES:
- All linear dimensions are in millimeters.
  - This drawing is subject to change without notice.
  - Publication IPC-7351 is recommended for alternate designs.
  - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
  - Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

PW (R-PDSO-G14)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
  - B. This drawing is subject to change without notice.
  -  Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
  -  Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
  - E. Falls within JEDEC MO-153

PW (R-PDSO-G14)

PLASTIC SMALL OUTLINE



- NOTES:
- All linear dimensions are in millimeters.
  - This drawing is subject to change without notice.
  - Publication IPC-7351 is recommended for alternate designs.
  - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
  - Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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