

April 2013

FQA62N25C

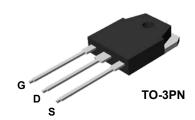
N-Channel QFET® MOSFET 250 V, 62 A, 35 mΩ

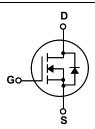
General Description

This N-Channel enhancement mode power MOSFET is produced using Fairchild Semiconductor®'s proprietary planar stripe and DMOS technology. This advanced MOSFET technology has been especially tailored to reduce on-state resistance, and to provide superior switching performance and high avalanche energy strength. These devices are suitable for switched mode power supplies, active power factor correction (PFC), and electronic lamp ballasts.

Features

- 62 A, 250 V, $R_{DS(on)}$ = 35 m Ω (Max.)@V_{GS} = 10 V, I_D = 31 A
- Low GateCharge (Typ. 100 nC)
- Low Crss (Typ. 63.5 pF)
- · 100% Avalanche Tested





Absolute Maximum Ratings T_C = 25°C unless otherwise noted

Symbol	Parameter		FQA62N25C	Unit	
V _{DSS}	Drain-Source Voltage		250	V	
I _D	Drain Current - Continuous (T _C = 25°	°C)	62	Α	
	- Continuous (T _C = 100°C)		39	Α	
I _{DM}	Drain Current - Pulsed	(Note 1)	248	Α	
V _{GSS}	Gate-Source Voltage		± 30	V	
E _{AS}	Single Pulsed Avalanche Energy	(Note 2)	2300	mJ	
I _{AR}	Avalanche Current	(Note 1)	62	А	
E _{AR}	Repetitive Avalanche Energy	(Note 1)	29.8	mJ	
dv/dt	Peak Diode Recovery dv/dt	(Note 3)	5.5	V/ns	
P_D	Power Dissipation (T _C = 25°C)		298	W	
	- Derate above 25°C		2.38	W/°C	
T _J , T _{STG}	Operating and Storage Temperature Range		-55 to +150	°C	
Tı	Maximum lead temperature for soldering purposes, 1/8" from case for 5 seconds		300	°C	
'L			300		

Thermal Characteristics

Symbol	Parameter	FQA62N25C	Unit
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case, Max.	0.42	°C/W
$R_{\theta CS}$	Thermal Resistance, Case-to-Sink, Typ.	0.24	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient, Max.	40	°C/W

Symbol	Parameter	Test Conditions		Min	Тур	Max	Unit
Off Cha	racteristics						
BV _{DSS}	Drain-Source Breakdown Voltage	V _{GS} = 0 V, I _D = 250 μA		250			V
ΔBV _{DSS} / ΔT _J	Breakdown Voltage Temperature Coefficient	I _D = 250 μA, Referenced t	o 25°C		0.28		V/°C
I _{DSS}	Zero Gate Voltage Drain Current	V _{DS} = 250 V, V _{GS} = 0 V				10	μА
		V _{DS} = 200 V, T _C = 125°C				100	μА
I _{GSSF}	Gate-Body Leakage Current, Forward	V _{GS} = 30 V, V _{DS} = 0 V				100	nA
I _{GSSR}	Gate-Body Leakage Current, Reverse	V _{GS} = -30 V, V _{DS} = 0 V				-100	nA
On Cha	racteristics						
V _{GS(th)}	Gate Threshold Voltage	$V_{DS} = V_{GS}, I_{D} = 250 \mu A$		2.0		4.0	V
R _{DS(on)}	Static Drain-Source On-Resistance	V _{GS} = 10 V, I _D = 31 A			0.029	0.035	Ω
g _{FS}	Forward Transconductance	V _{DS} = 40 V, I _D = 31 A	(Note 4)		55		S
C _{iss}	Input Capacitance	V _{DS} = 25 V, V _{GS} = 0 V, f = 1.0 MHz			4830	6280	pF
C _{oss}	Output Capacitance				945	1230	pF
C _{rss}	Reverse Transfer Capacitance				63.5	83	pF
Switchi	ng Characteristics						
t _{d(on)}	Turn-On Delay Time	\/ - 425 \/ L - 62 A			75	160	ns
t _r	Turn-On Rise Time	$V_{DD} = 125 \text{ V}, I_{D} = 62 \text{ A},$ $R_{G} = 25 \Omega$			395	800	ns
t _{d(off)}	Turn-Off Delay Time				245	500	ns
t _f	Turn-Off Fall Time		(Note 4)		335	680	ns
Qg	Total Gate Charge	V _{DS} = 200 V, I _D = 62 A,			100	130	nC
Q _{gs}	Gate-Source Charge	$V_{GS} = 10 \text{ V}$ (Note 4)			25.5		nC
Q _{gd}	Gate-Drain Charge				39		nC
	ource Diode Characteristics a	nd Maximum Ratings					
I _S	Maximum Continuous Drain-Source Diode Forward Current				62	Α	
I _{SM}	Maximum Pulsed Drain-Source Diode F					248	Α
V_{SD}	Drain-Source Diode Forward Voltage	$V_{GS} = 0 \text{ V}, I_{S} = 62 \text{ A}$				1.5	V
t _{rr}	Reverse Recovery Time	$V_{GS} = 0 \text{ V, I}_{S} = 62 \text{ A,}$			340		ns
Q _{rr}	Reverse Recovery Charge	dI _F / dt = 100 A/μs	(Note 4)		4.77		μС

- **Notes:**1. Repetitive Rating : Pulse width limited by maximum junction temperature 2. L = 0.96mH, I_{AS} = 62A, V_{DD} = 50V, R_G = 25 Ω , Starting T_J = 25°C 3. I_{SD} \leq 62A, di/dt \leq 300A/µs, V_{DD} \leq BV_{DSS}, Starting T_J = 25°C 4. Pulse Test : Pulse width \leq 300µs, Duty cycle \leq 2% 5. Essentially independent of operating temperature

Typical Characteristics

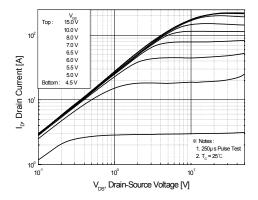


Figure 1. On-Region Characteristics

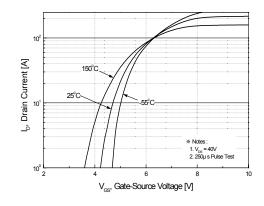


Figure 2. Transfer Characteristics

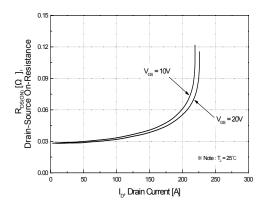


Figure 3. On-Resistance Variation vs Drain Current and Gate Voltage

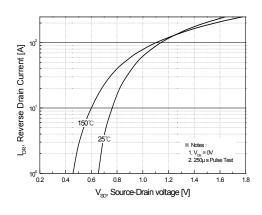


Figure 4. Body Diode Forward Voltage Variation with Source Current and Temperature

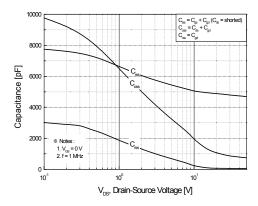


Figure 5. Capacitance Characteristics

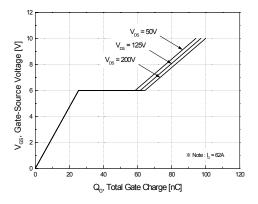


Figure 6. Gate Charge Characteristics

Typical Characteristics (Continued) 12 (Description of the property of the pr

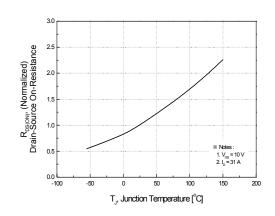
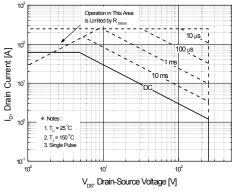


Figure 8. On-Resistance Variation vs Temperature



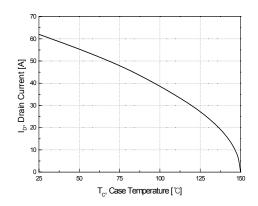


Figure 9. Maximum Safe Operating Area

Figure 10. Maximum Drain Current vs Case Temperature

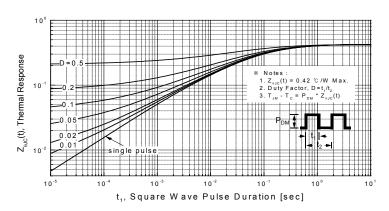
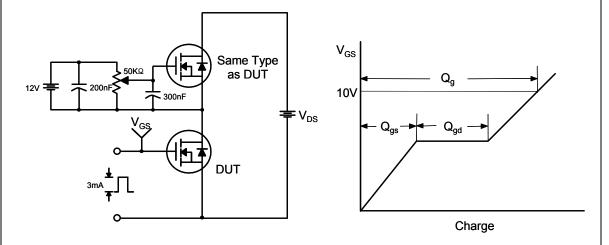
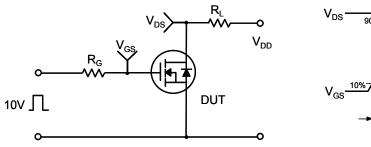


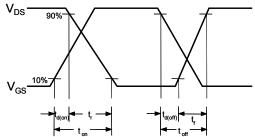
Figure 11. Transient Thermal Response Curve

Gate Charge Test Circuit & Waveform

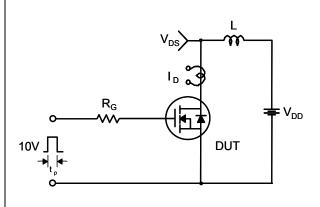


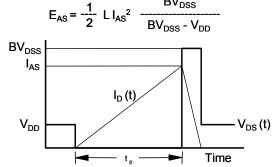
Resistive Switching Test Circuit & Waveforms



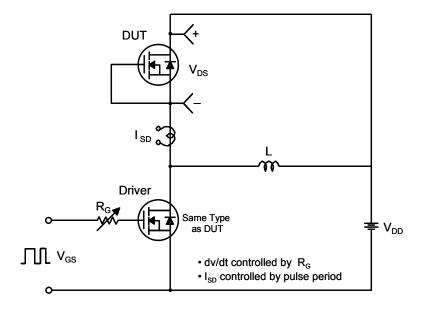


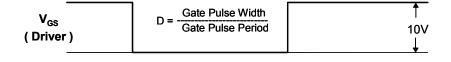
Unclamped Inductive Switching Test Circuit & Waveforms

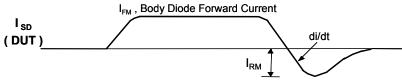




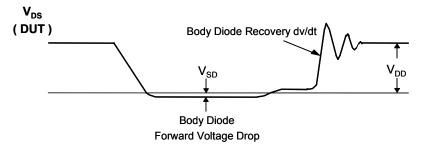
Peak Diode Recovery dv/dt Test Circuit & Waveforms





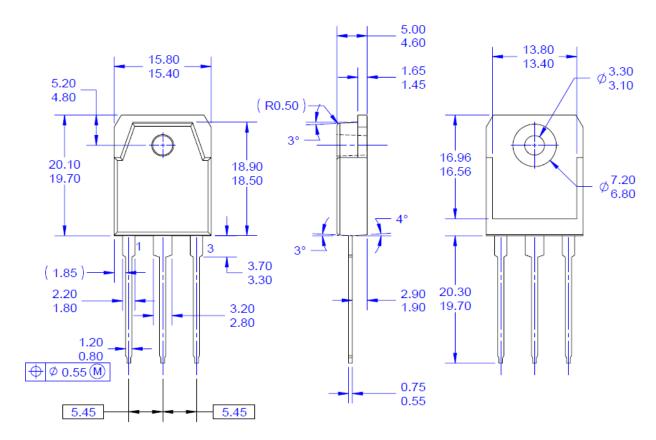


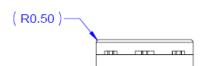
Body Diode Reverse Current



Mechanical Dimensions

TO-3PN





NOTES: UNLESS OTHERWISE SPECIFIED

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