POWER DRIVER FOR STEPPER MOTORS

INTEGRATED CIRCUITS

TMC262 DATASHEET

Universal, cost-effective stepper driver for two-phase bipolar motors with state-of-the-art features. External MOSFETs fit different motor sizes. With Step/Dir Interface and SPI.

APPLICATIONS

- Textile, Sewing Machines
- Factory Automation
- Lab Automation
- Liquid Handling
- Medical
- Office Automation
- Printer and Scanner
- CCTV, Security
- ATM, Cash recycler
- POS
- Pumps and Valves
- Heliostat Controller
- CNC Machines

FEATURES AND BENEFITS

High Current up to 8A Motor current using external (N&P) MOSFETs.

Highest Voltage up to 60V DC operating voltage

Highest Resolution up to 256 microsteps per full step

Smallest Size 5x5mm QFN32 package

Low Power Dissipation synchronous rectification

EMI-optimized slope & current controlled gate drivers

Protection & Diagnostics overcurrent, short to GND, overtemperature & undervoltage

stallGuard2™ high precision sensorless motor load detection

coolStep™ load dependent current control for energy savings up to 75%

microPlyer™ microstep interpolation for increased smoothness with coarse step inputs.

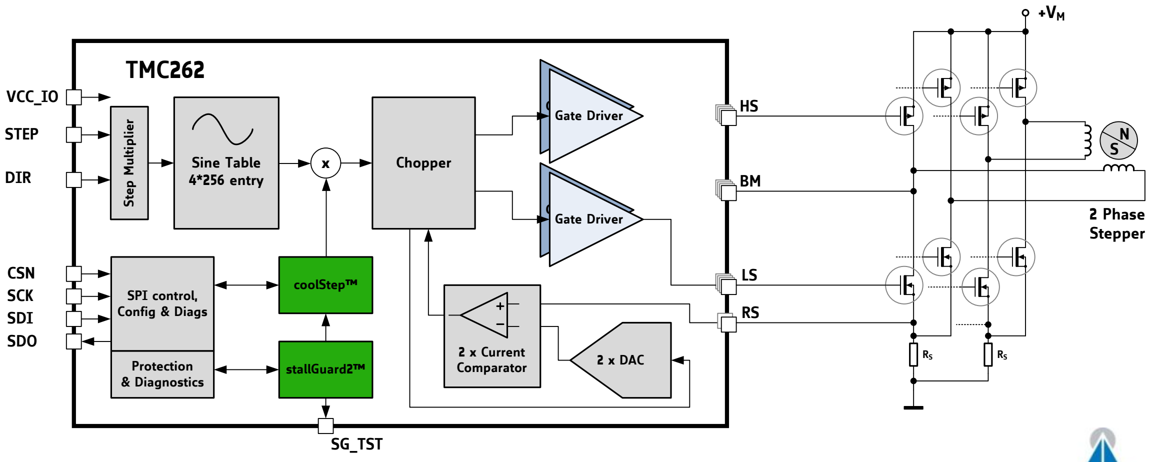
spreadCycle™ high-precision chopper for best current sine wave form and zero crossing

DESCRIPTION

The TMC262 driver for two-phase stepper motors offers an industry-leading feature set, including high-resolution microstepping, sensorless mechanical load measurement, load-adaptive power optimization, and low-resonance chopper operation. Standard SPI™ and STEP/DIR interfaces simplify communication. The TMC262 drives four external N- and P-channel dual MOSFETs for motor currents up to 8A and up to 60V. Integrated protection and diagnostic features support robust and reliable operation.

High integration, high energy efficiency and small form factor enable miniaturized designs with low external component count for cost-effective and highly competitive solutions.

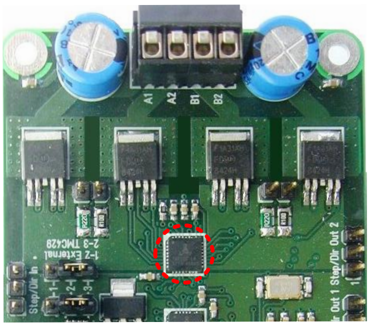
BLOCK DIAGRAM



TRINAMIC Motion Control GmbH & Co. KG
Hamburg, Germany

APPLICATION EXAMPLES: HIGH POWER – SMALL SIZE

The TMC262 scores with its high power density and a versatility that covers a wide spectrum of applications and motor sizes, all while keeping costs down. Extensive support at the chip, board, and software levels enables rapid design cycles and fast time-to-market with competitive products. High energy efficiency from TRINAMIC's coolStep technology delivers further cost savings in related systems such as power supplies and cooling.

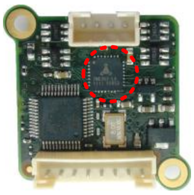


Layout with 6A MOSFETs

STEPROCKER™

The driver stage shown uses 6A-capable dual MOSFETs. All cooling requirements are satisfied by passive convection cooling. The stepRocker is supported by the motioncontrol-community, with forum, applications, schematics, open source projects, demos etc.:

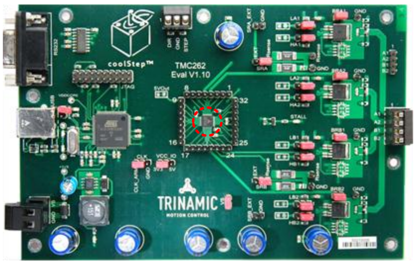
motioncontrol-community.org



Miniaturized Layout

TMCM-MODULE FOR NEMA 11 STEPPER MOTORS

This miniaturized power stage drives up to 1.2A RMS and mounts directly on a 28mm-size motor. Tiny TSOP6 dual MOSFETs enable an ultra-compact and flexible PCB layout.



Layout for Evaluation

TMC262-EVAL DEVELOPMENT PLATFORM

This evaluation board is a development platform for applications based on the TMC262.

The board features USB and RS232 interfaces for communication with control software running on a PC. External power MOSFETs support drive currents up to 6A at 40 V.

The control software provides a user-friendly GUI for setting control parameters and visualizing the dynamic response of the motor.

Motor movement can be controlled through the Step and Dir interface using inputs from an external source or signals generated by the onboard microcontroller acting as a step generator.

ORDER CODES

Order code	Description	Size
TMC262-LA	coolStep™ driver for external MOSFETs, QFN32	5 x 5 mm^2
TMC262-EVAL	Evaluation board for TMC262 (RS232, USB)	10 x 16 cm^2
TMC429+26x-EVAL	Chipset evaluation board for TMC429, TMC260, TMC261, TMC262, and TMC424.	10 x 16 cm^2

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1 Principles of Operation

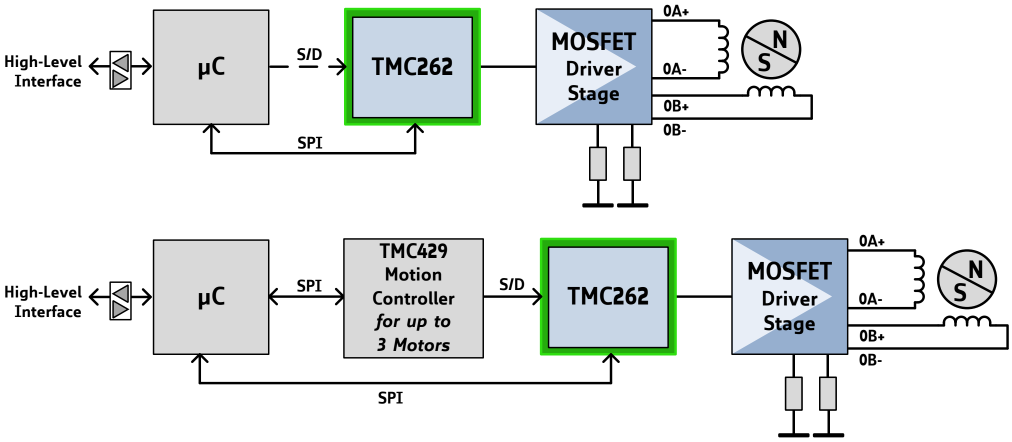


Figure 1.1 Applications block diagrams

The TMC262 motor driver is the intelligence between a motion controller and the power MOSFETs for driving a two-phase stepper motor, as shown in Figure 1.1 Following power-up, an embedded microcontroller initializes the driver by sending commands over an SPI bus to write control parameters and mode bits in the TMC262. The microcontroller may implement the motion-control function as shown in the upper part of the figure, or it may send commands to a dedicated motion controller chip such as TRINAMIC's TMC429 as shown in the lower part.

The motion controller can control the motor position by sending pulses on the STEP signal while indicating the direction on the DIR signal. The TMC262 has a microstep counter and sine table to convert these signals into the coil currents which control the position of the motor. If the microcontroller implements the motion-control function, it can write values for the coil currents directly to the TMC262 over the SPI interface, in which case the STEP/DIR interface may be disabled. This mode of operation requires software to track the motor position and reference a sine table to calculate the coil currents.

To optimize power consumption and heat dissipation, software may also adjust coolStep and stallGuard2 parameters in real-time, for example to implement different tradeoffs between speed and power consumption in different modes of operation.

The motion control function is a hard real-time task which may be a burden to implement reliably alongside other tasks on the embedded microcontroller. By offloading the motion-control function to the TMC429, up to three motors can be operated reliably with very little demand for service from the microcontroller. Software only needs to send target positions, and the TMC429 generates precisely timed step pulses. Software retains full control over both the TMC262 and TMC429 through the SPI bus.

1.1 Key Concepts

The TMC262 motor driver implements several advanced patented features which are exclusive to TRINAMIC products. These features contribute toward greater precision, greater energy efficiency, higher reliability, smoother motion, and cooler operation in many stepper motor applications.

stallGuard2™	High-precision load measurement using the back EMF on the coils
coolStep™	Load-adaptive current control which reduces energy consumption by as much as 75%
spreadCycle™	High-precision chopper algorithm available as an alternative to the traditional constant off-time algorithm
microPlyer™	Microstep interpolator for obtaining increased smoothness of microstepping over a STEP/DIR interface

In addition to these performance enhancements, TRINAMIC motor drivers also offer safeguards to detect and protect against shorted outputs, open-circuit output, overtemperature, and undervoltage conditions for enhancing safety and recovery from equipment malfunctions.

1.2 Control Interfaces

There are two control interfaces from the motion controller to the motor driver: the SPI serial interface and the STEP/DIR interface. The SPI interface is used to write control information to the chip and read back status information. This interface must be used to initialize parameters and modes necessary to enable driving the motor. This interface may also be used for directly setting the currents flowing through the motor coils, as an alternative to stepping the motor using the STEP and DIR signals, so the motor can be controlled through the SPI interface alone.

The STEP/DIR interface is a traditional motor control interface available for adapting existing designs to use TRINAMIC motor drivers. Using only the SPI interface requires slightly more CPU overhead to look up the sine tables and send out new current values for the coils.

1.2.1 SPI Interface

The SPI interface is a bit-serial interface synchronous to a bus clock. For every bit sent from the bus master to the bus slave, another bit is sent simultaneously from the slave to the master. Communication between an SPI master and the TMC262 slave always consists of sending one 20-bit command word and receiving one 20-bit status word.

The SPI command rate typically corresponds to the microstep rate at low velocities. At high velocities, the rate may be limited by CPU bandwidth to 10-100 thousand commands per second, so the application may need to change to fullstep resolution.

1.2.2 STEP/DIR Interface

The STEP/DIR interface is enabled by default. Active edges on the STEP input can be rising edges or both rising and falling edges, as controlled by another mode bit (DEDGE). Using both edges cuts the toggle rate of the STEP signal in half, which is useful for communication over slow interfaces such as optically isolated interfaces.

On each active edge, the state sampled from the DIR input determines whether to step forward or back. Each step can be a fullstep or a microstep, in which there are 2, 4, 8, 16, 32, 64, 128, or 256 microsteps per fullstep. During microstepping, a low state on DIR increases the microstep counter and a high decreases the counter by an amount controlled by the microstep resolution. An internal table translates the counter value into the sine and cosine values which control the motor current for microstepping.

1.3 Mechanical Load Sensing

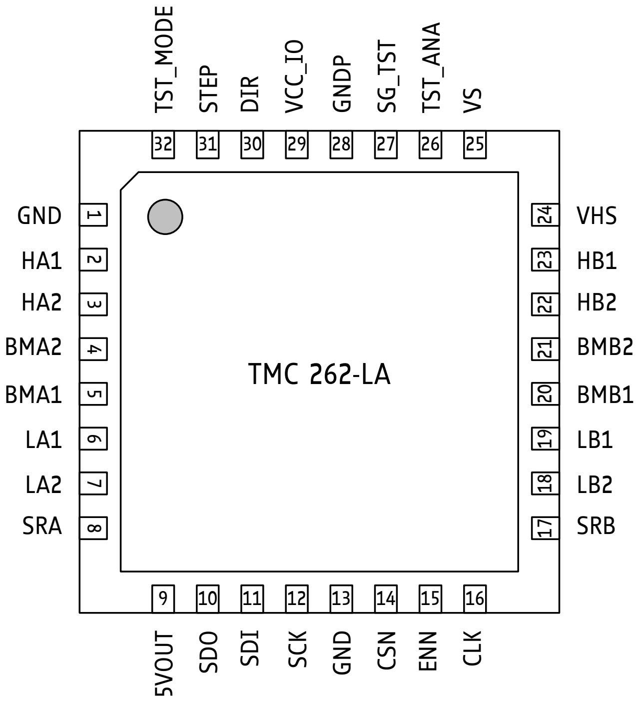
The TMC262 provides stallGuard2 high-resolution load measurement for determining the mechanical load on the motor by measuring the back EMF. In addition to detecting when a motor stalls, this feature can be used for homing to a mechanical stop without a limit switch or proximity detector. The coolStep power-saving mechanism uses stallGuard2 to reduce the motor current to the minimum motor current required to meet the actual load placed on the motor.

1.4 Current Control

Current into the motor coils is controlled using a cycle-by-cycle chopper mode. Two chopper modes are available: a traditional constant off-time mode and the new spreadCycle mode. spreadCycle mode offers smoother operation and greater power efficiency over a wide range of speed and load.

2 Pin Assignments

2.1 Package Outline



Top view

Figure 2.1 TMC262 pin assignments

2.2 Signal Descriptions

Pin	Number	Type	Function
GND	1 13		Digital and analog low power GND
HA1	2	O (VS)	High side P-channel driver output. Becomes driven to VHS to switch on MOSFET.
HA2	3		
HB1	23		
HB2	22		
BMA1	5	I (VS)	Sensing input for bridge outputs. Used for short to GND protection. May be tied to VS if unused.
BMA2	4		
BMB1	20		
BMB2	21		
LA1	6	O 5V	Low side MOSFET driver output. Becomes driven to 5VOUT to switch on MOSFET.
LA2	7		
LB1	19		
LB2	18		
SRA	8	AI	Sense resistor input of chopper driver.
SRB	17		
5VOUT	9		Output of internal 5V linear regulator. This voltage is used to supply the low side drivers and internal analog circuitry. An external capacitor to GND close to the pin is required. Place the capacitor near to pin 9 and pin 13. 470nF ceramic are sufficient for most applications, an additional tantalum capacitor (10µF or more) improves performance with high gate charge MOSFETs.

Pin	**Number**	**Type**	**Function**
SDO	10	DO VIO	Data output of SPI interface (Tristate)
SDI	11	DI VIO	Data input of SPI interface (Scan test input in test mode)
SCK	12	DI VIO	Serial clock input of SPI interface (Scan test shift enable input in test mode)
CSN	14	DI VIO	Chip select input of SPI interface
ENN	15	DI VIO	Enable not input for drivers. Switches off all MOSFETs.
CLK	16	DI VIO	Clock input for all internal operations. Tie low to use internal oscillator. A high signal disables the internal oscillator until power down.
VHS	24		High side supply voltage (motor supply voltage - 10V)
VS	25		Motor supply voltage
TST_ANA	26	AO VIO	Analog mode test output. Leave open for normal operation.
SG_TST	27	DO VIO	stallGuard2™ output. Signals motor stall (high active).
GNDP	28		Power GND for MOSFET drivers. Connect directly to GND
VCC_IO	29		Input / output supply voltage VIO for all digital pins. Tie to digital logic supply voltage. Allows operation in 3.3V and 5V systems.
DIR	30	DI VIO	Direction input. Is sampled upon detection of a step to determine stepping direction. An internal glitch filter for 60ns is provided.
STEP	31	DI VIO	Step input. An internal glitch filter for 60ns is provided.
TST_MODE	32	DI VIO	Test mode input. Puts IC into test mode. Tie to GND for normal operation.

3 Internal Architecture

Figure 3.1 shows the internal architecture of the TMC262.

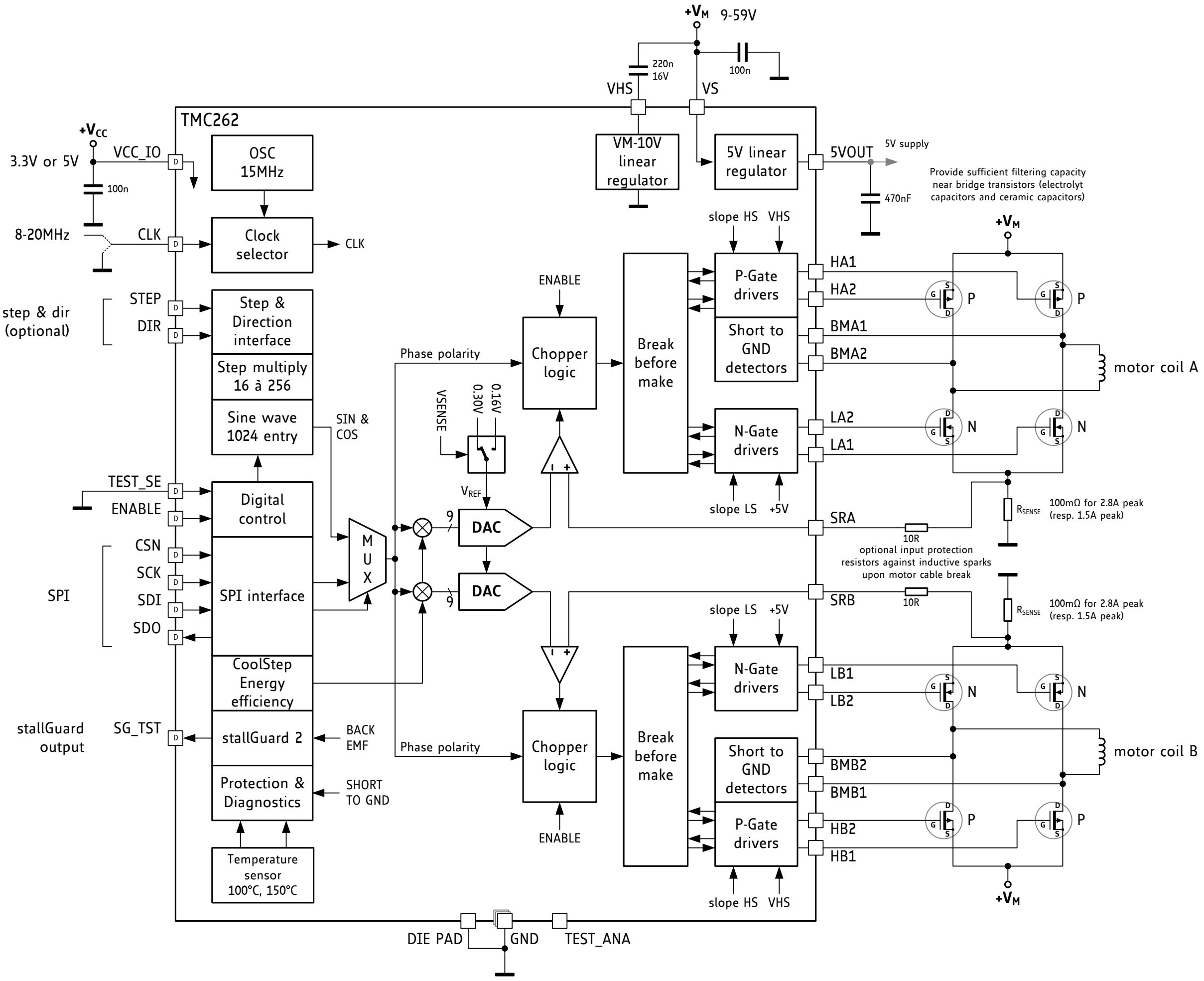


Figure 3.1 TMC262 block diagram

Prominent features include:

Oscillator and clock selector	provides the system clock from the on-chip oscillator or an external source.
Step and direction interface	uses a microstep counter and sine table to generate target currents for the coils.
SPI interface	receives commands that directly set the coil current values.
Multiplexer	selects either the output of the sine table or the SPI interface for controlling the current into the motor coils.
Multipliers	scales down the currents to both coils when the currents are greater than those required by the load on the motor or as set by the CS current scale parameter.
DACs and comparators	converts the digital current values to analog signals that are compared with the voltages on the sense resistors. Comparator outputs terminate chopper drive phases when target currents are reached.
Break-before-make and gate drivers	ensure non-overlapping pulses, boost pulse voltage, and control pulse slope to the gates of the power MOSFETs.
On-chip voltage regulators	provide high-side voltage for P-channel MOSFET gate drivers and supply voltage for on-chip analog and digital circuits.

4 stallGuard2 Load Measurement

stallGuard2 provides an accurate measurement of the load on the motor. It can be used for stall detection as well as other uses at loads below those which stall the motor, such as coolStep load-adaptive current reduction. (stallGuard2 is a more precise evolution of the earlier stallGuard technology.)

The stallGuard2 measurement value changes linearly over a wide range of load, velocity, and current settings, as shown in Figure 4.1. At maximum motor load, the value goes to zero or near to zero. This corresponds to a load angle of 90° between the magnetic field of the coils and magnets in the rotor. This also is the most energy-efficient point of operation for the motor.

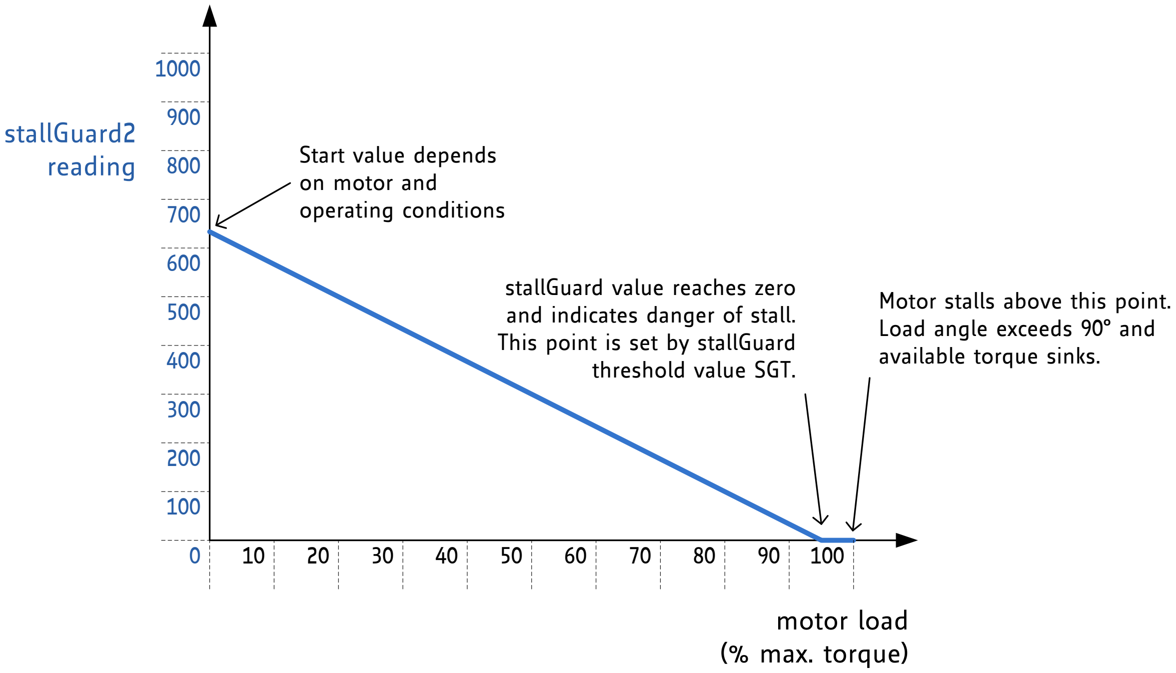


Figure 4.1 stallGuard2 load measurement SG as a function of load

Two parameters control stallGuard2 and one status value is returned.

Parameter	Description	Setting	Comment
SGT	7-bit signed integer that sets the stallGuard2 threshold level for asserting the SG_TST output and sets the optimum measurement range for readout. Negative values increase sensitivity, and positive values reduce sensitivity so more torque is required to indicate a stall. Zero is a good starting value. Operating at values below -10 is not recommended.	0	indifferent value
		+1… +63	less sensitivity
		-1… -64	higher sensitivity
SFILT	Mode bit which enables the stallGuard2 filter for more precision. If set, reduces the measurement frequency to one measurement per four fullsteps. If cleared, no filtering is performed. Filtering compensates for mechanical asymmetries in the construction of the motor, but at the expense of response time. Unfiltered operation is recommended for rapid stall detection. Filtered operation is recommended for more precise load measurement.	0	standard mode
		1	filtered mode

Status word	Description	Range	Comment
SG	10-bit unsigned integer stallGuard2 measurement value. A higher value indicates lower mechanical load. A lower value indicates a higher load and therefore a higher load angle. For stall detection, adjust SGT to return an SG value of 0 or slightly higher upon maximum motor load before stall.	0… 1023	0: highest load low value: high load high value: less load

4.1 Tuning the stallGuard2 Threshold

Due to the dependency of the stallGuard2 value SG from motor-specific characteristics and application-specific demands on load and velocity the easiest way to tune the stallGuard2 threshold *SGT* for a specific motor type and operating conditions is interactive tuning in the actual application.

The procedure is:

1. Operate the motor at a reasonable velocity for your application and monitor SG.
2. Apply slowly increasing mechanical load to the motor. If the motor stalls before SG reaches zero, decrease SGT. If SG reaches zero before the motor stalls, increase SGT. A good SGT starting value is zero. SGT is signed, so it can have negative or positive values.
3. The optimum setting is reached when SG is between 0 and 400 at increasing load shortly before the motor stalls, and SG increases by 100 or more without load. SGT in most cases can be tuned together with the motion velocity in a way that SG goes to zero when the motor stalls and the stall output SG_TST is asserted. This indicates that a step has been lost.

The system clock frequency affects SG. An external crystal-stabilized clock should be used for applications that demand the highest performance. The power supply voltage also affects SG, so tighter regulation results in more accurate values. SG measurement has a high resolution, and there are a few ways to enhance its accuracy, as described in the following sections.

4.1.1 Variable Velocity Operation

Across a range of velocities, on-the-fly adjustment of the stallGuard2 threshold SGT improves the accuracy of the load measurement SG. This also improves the power reduction provided by coolStep, which is driven by SG. Linear interpolation between two SGT values optimized at different velocities is a simple algorithm for obtaining most of the benefits of on-the-fly SGT adjustment, as shown in Figure 4.2. This figure shows an optimal SGT curve in black and a two-point interpolated SGT curve in red.

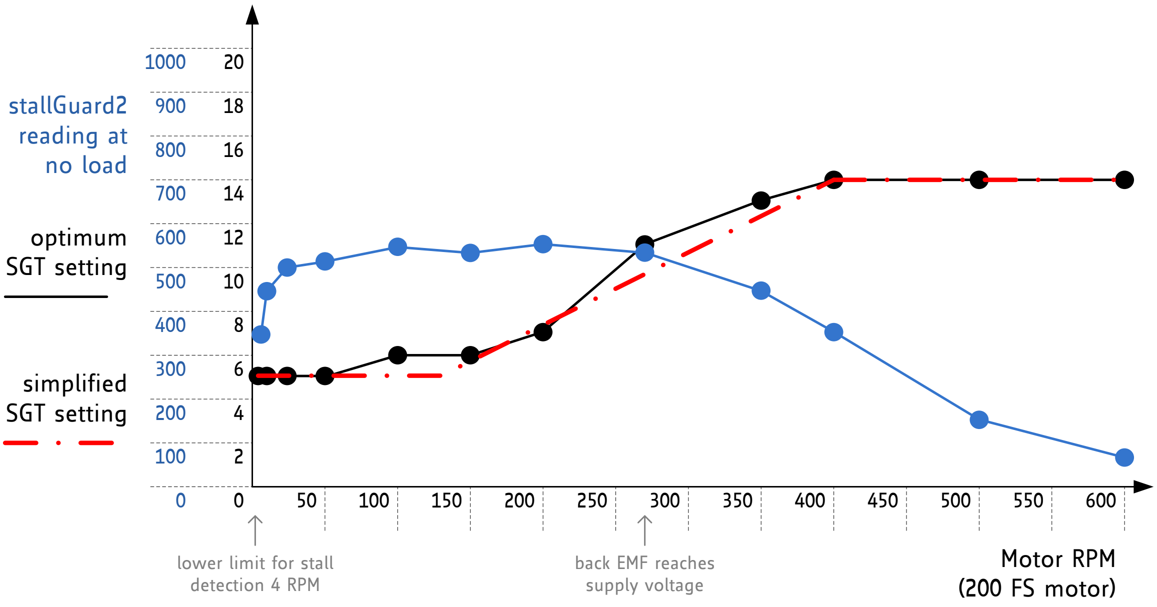


Figure 4.2 Linear interpolation for optimizing SGT with changes in velocity

4.1.2 Small Motors with High Torque Ripple and Resonance

Motors with a high detent torque show an increased variation of the stallGuard2 measurement value SG with varying motor currents, especially at low currents. For these motors, the current dependency might need correction in a similar manner to velocity correction for obtaining the highest accuracy.

4.1.3 Temperature Dependence of Motor Coil Resistance

Motors working over a wide temperature range may require temperature correction, because motor coil resistance increases with rising temperature. This can be corrected as a linear reduction of SG at increasing temperature, as motor efficiency is reduced.

4.1.4 Accuracy and Reproducibility of stallGuard2 Measurement

In a production environment, it may be desirable to use a fixed SGT value within an application for one motor type. Most of the unit-to-unit variation in stallGuard2 measurements results from manufacturing tolerances in motor construction. The measurement error of stallGuard2 – provided that all other parameters remain stable – can be as low as:

$$stallGuard\ measurement\ error = \pm max(1, |SGT|)$$

4.2 stallGuard2 Measurement Frequency and Filtering

The stallGuard2 measurement value SG is updated with each full step of the motor. This is enough to safely detect a stall, because a stall always means the loss of four full steps. In a practical application, especially when using coolStep, a more precise measurement might be more important than an update for each fullstep because the mechanical load never changes instantaneously from one step to the next. For these applications, the SFILT bit enables a filtering function over four load measurements. The filter should always be enabled when high-precision measurement is required. It compensates for variations in motor construction, for example due to misalignment of the phase A to phase B magnets. The filter should only be disabled when rapid response to increasing load is required, such as for stall detection at high velocity.

4.3 Detecting a Motor Stall

To safely detect a motor stall, a stall threshold must be determined using a specific SGT setting. Therefore, you need to determine the maximum load the motor can drive without stalling and to monitor the SG value at this load, for example some value within the range 0 to 400. The stall threshold should be a value safely within the operating limits, to allow for parameter stray. So, your microcontroller software should set a stall threshold which is slightly higher than the minimum value seen before an actual motor stall occurs. The response at an SGT setting at or near 0 gives some idea on the quality of the signal: Check the SG value without load and with maximum load. These values should show a difference of at least 100 or a few 100, which shall be large compared to the offset. If you set the SGT value so that a reading of 0 occurs at maximum motor load, an active high stall output signal will be available at SG_TST output.

4.4 Limits of stallGuard2 Operation

stallGuard2 does not operate reliably at extreme motor velocities: Very low motor velocities (for many motors, less than one revolution per second) generate a low back EMF and make the measurement unstable and dependent on environment conditions (temperature, etc.). Other conditions will also lead to extreme settings of SGT and poor response of the measurement value SG to the motor load.

Very high motor velocities, in which the full sinusoidal current is not driven into the motor coils also lead to poor response. These velocities are typically characterized by the motor back EMF reaching the supply voltage.

5 coolStep Load-Adaptive Current Control

coolStep allows substantial energy savings, especially for motors which see varying loads or operate at a high duty cycle. Because a stepper motor application needs to work with a torque reserve of 30% to 50%, even a constant-load application allows significant energy savings because coolStep automatically enables torque reserve when required. Reducing power consumption keeps the system cooler, increases motor life, and allows reducing cost in the power supply and cooling components.

Reducing motor current by half results in reducing power by a factor of four.

Energy efficiency	-	power consumption decreased up to 75%.
Motor generates less heat	-	improved mechanical precision.
Less cooling infrastructure	-	for motor and driver.
Cheaper motor	-	does the job.

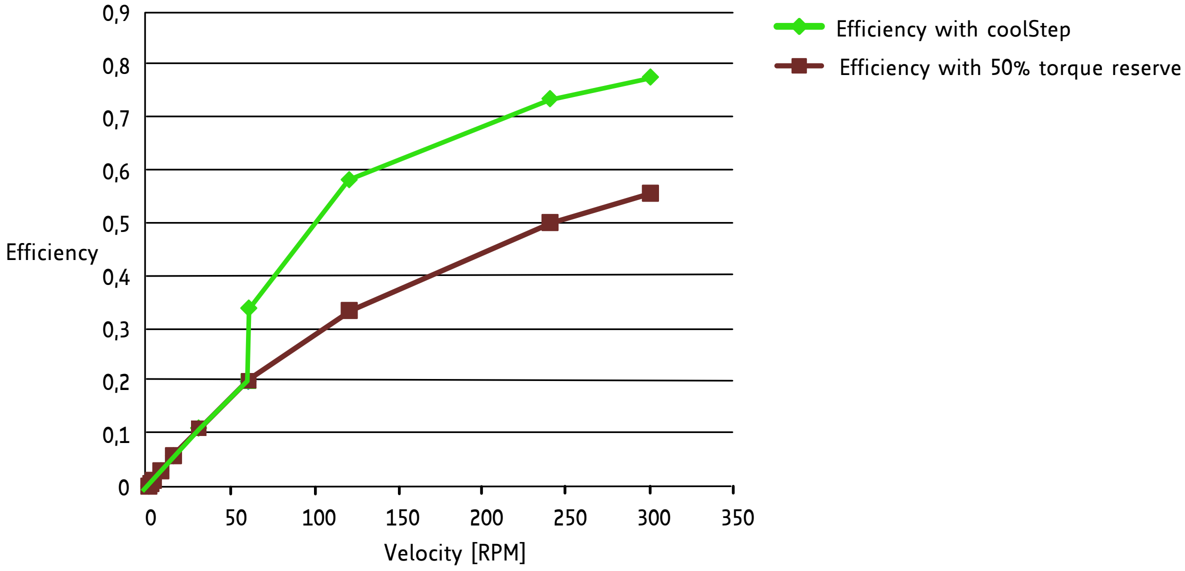


Figure 5.1 Energy efficiency example with coolStep

Figure 5.1 shows the efficiency gain of a 42mm stepper motor when using coolStep compared to standard operation with 50% of torque reserve. coolStep is enabled above 60rpm in the example.

coolStep is controlled by several parameters, but two are critical for understanding how it works:

Parameter	Description	Range	Comment
SEMIN	4-bit unsigned integer that sets a lower threshold. If SG goes below this threshold, coolStep increases the current to both coils. The 4-bit SEMIN value is scaled by 32 to cover the lower half of the range of the 10-bit SG value. (The name of this parameter is derived from smartEnergy, which is an earlier name for coolStep.)	0… 15	lower stallGuard threshold: SEMINx32
SEMAX	4-bit unsigned integer that controls an upper threshold. If SG is sampled equal to or above this threshold enough times, coolStep decreases the current to both coils. The upper threshold is (SEMIN + SEMAX + 1) x 32.	0… 15	upper stallGuard threshold: (SEMIN+SEMAX+1)x32

Figure 5.2 shows the operating regions of coolStep. The black line represents the SG measurement value, the blue line represents the mechanical load applied to the motor, and the red line represents the current into the motor coils. When the load increases, SG falls below SEMIN, and coolStep

increases the current. When the load decreases and SG rises above (SEMIN + SEMAX + 1) x 32 the current becomes reduced.

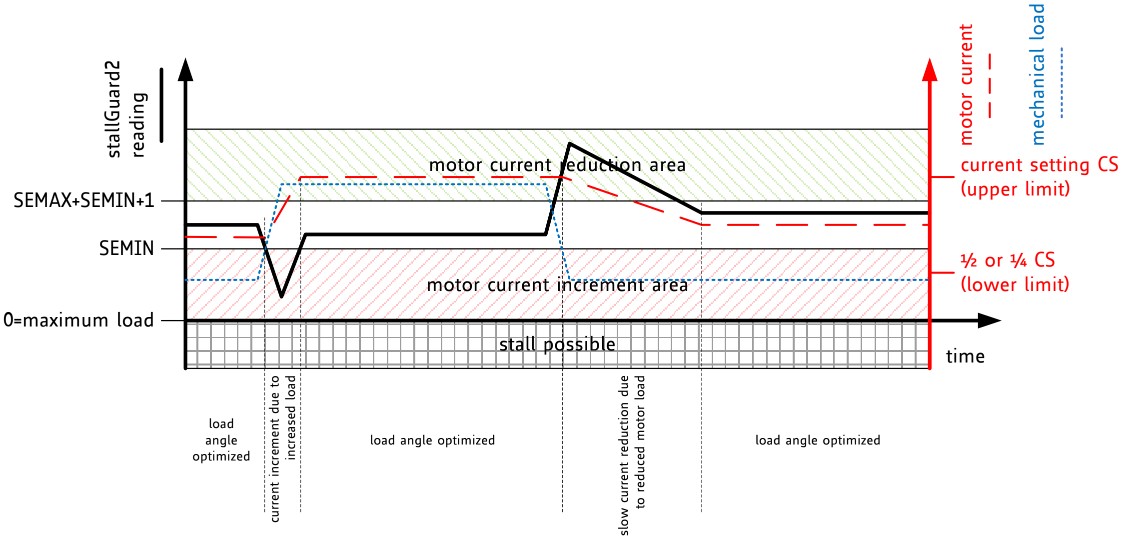


Figure 5.2 coolStep adapts motor current to the load

Four more parameters control coolStep and one status value is returned:

Parameter	**Description**	**Range**	**Comment**
CS	*Current scale.* Scales both coil current values as taken from the internal sine wave table or from the SPI interface. For high precision motor operation, work with a current scaling factor in the range 16 to 31, because scaling down the current values reduces the effective microstep resolution by making microsteps coarser. This setting also controls the maximum current value set by coolStep™.	0… 31	scaling factor: 1/32, 2/32, … 32/32
SEUP	Number of increments of the coil current for each occurrence of an SG measurement below the lower threshold.	0… 3	step width is: 1, 2, 4, 8
SEDN	Number of occurrences of SG measurements above the upper threshold before the coil current is decremented.	0… 3	number of stallGuard measurements per decrement: 32, 8, 2, 1
SEIMIN	Mode bit that controls the lower limit for scaling the coil current. If the bit is set, the limit is ¼ CS. If the bit is clear, the limit is ½ CS.	0	Minimum motor current: 1/2 of CS
		1	1/4 of CS
Status word	**Description**	**Range**	**Comment**
SE	5-bit unsigned integer reporting the actual current scaling value determined by coolStep. This value is biased by 1 and divided by 32, so the range is 1/32 to 32/32. The value will not be greater than the value of CS or lower than either ¼ CS or ½ CS depending on the setting of SEIMIN.	0… 31	Actual motor current scaling factor set by coolStep: 1/32, 2/32, … 32/32

5.1 Tuning coolStep

Before tuning coolStep, first tune the stallGuard2 threshold level SGT, which affects the range of the load measurement value SG. coolStep uses SG to operate the motor near the optimum load angle of +90°.

The current increment speed is specified in SEUP, and the current decrement speed is specified in SEDN. They can be tuned separately because they are triggered by different events that may need different responses. The encodings for these parameters allow the coil currents to be increased much more quickly than decreased, because crossing the lower threshold is a more serious event that may require a faster response. If the response is too slow, the motor may stall. In contrast, a slow response to crossing the upper threshold does not risk anything more serious than missing an opportunity to save power.

coolStep operates between limits controlled by the current scale parameter CS and the SEIMIN bit.

5.1.1 Response Time

For fast response to increasing motor load, use a high current increment step SEUP. If the motor load changes slowly, a lower current increment step can be used to avoid motor current oscillations. If the filter controlled by SFILT is enabled, the measurement rate and regulation speed are cut by a factor of four.

5.1.2 Low Velocity and Standby Operation

Because stallGuard2 is not able to measure the motor load in standstill and at very low RPM, the current at low velocities should be set to an application-specific default value and combined with standstill current reduction settings programmed through the SPI interface.

6 SPI Interface

The TMC262 requires setting configuration parameters and mode bits through the SPI interface before the motor can be driven. The SPI interface also allows reading back status values and bits.

6.1 Bus Signals

The SPI bus on the TMC262 has four signals:

SCK	bus clock input
SDI	serial data input
SDO	serial data output
CSN	chip select input (active low)

The slave is enabled for an SPI transaction by a low on the chip select input CSN. Bit transfer is synchronous to the bus clock SCK, with the slave latching the data from SDI on the rising edge of SCK and driving data to SDO following the falling edge. The most significant bit is sent first. A minimum of 20 SCK clock cycles is required for a bus transaction with the TMC262.

If more than 20 clocks are driven, the additional bits shifted into SDI are shifted out on SDO after a 20-clock delay through an internal shift register. This can be used for daisy chaining multiple chips.

CSN must be low during the whole bus transaction. When CSN goes high, the contents of the internal shift register are latched into the internal control register and recognized as a command from the master to the slave. If more than 20 bits are sent, only the last 20 bits received before the rising edge of CSN are recognized as the command.

6.2 Bus Timing

SPI interface is synchronized to the internal system clock, which limits the SPI bus clock SCK to half of the system clock frequency. If the system clock is based on the on-chip oscillator, an additional 10% safety margin must be used to ensure reliable data transmission. All SPI inputs as well as the ENN input are internally filtered to avoid triggering on pulses shorter than 20ns. Figure 6.1 shows the timing parameters of an SPI bus transaction, and the table below specifies their values.

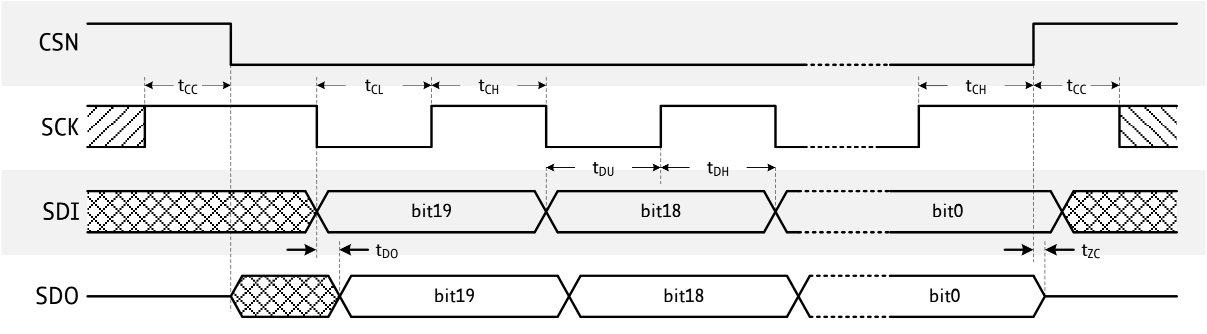


Figure 6.1 SPI Timing

SPI Interface Timing	**AC-Characteristics** clock period is t_{CLK}					
Parameter	**Symbol**	**Conditions**	**Min**	**Typ**	**Max**	**Unit**
SCK valid before or after change of CSN	t_{CC}		10			ns
CSN high time	t_{CSH}	*)Min time is for synchronous CLK with SCK high one t_{CH} before CSN high only	t_{CLK}	$>2t_{CLK}+10$		ns
SCK low time	t_{CL}	*)Min time is for synchronous CLK only	t_{CLK}	$>t_{CLK}+10$		ns
SCK high time	t_{CH}	*)Min time is for synchronous CLK only	t_{CLK}	$>t_{CLK}+10$		ns
SCK frequency using internal clock	f_{SCK}	Assumes minimum OSC frequency			4	MHz
SCK frequency using external 16MHz clock	f_{SCK}	Assumes synchronous CLK			8	MHz
SDI setup time before rising edge of SCK	t_{DU}		10			ns
SDI hold time after rising edge of SCK	t_{DH}		10			ns
Data out valid time after falling SCK clock edge	t_{DO}	No capacitive load on SDO			$t_{FILT}+5$	ns
SDI, SCK, and CSN filter delay time	t_{FILT}	Rising and falling edge	12	20	30	ns

6.3 Bus Architecture

SPI slaves can be chained and used with a single chip select line. If slaves are chained, they behave like a long shift register. For example, a chain of two motor drivers requires 40 bits to be sent. The last bits shifted to each register in the chain are loaded into an internal register on the rising edge of the CSN input. For example, 24 or 32 bits can be sent to a single motor driver, but it latches just the last 20 bits received before CSN goes high.

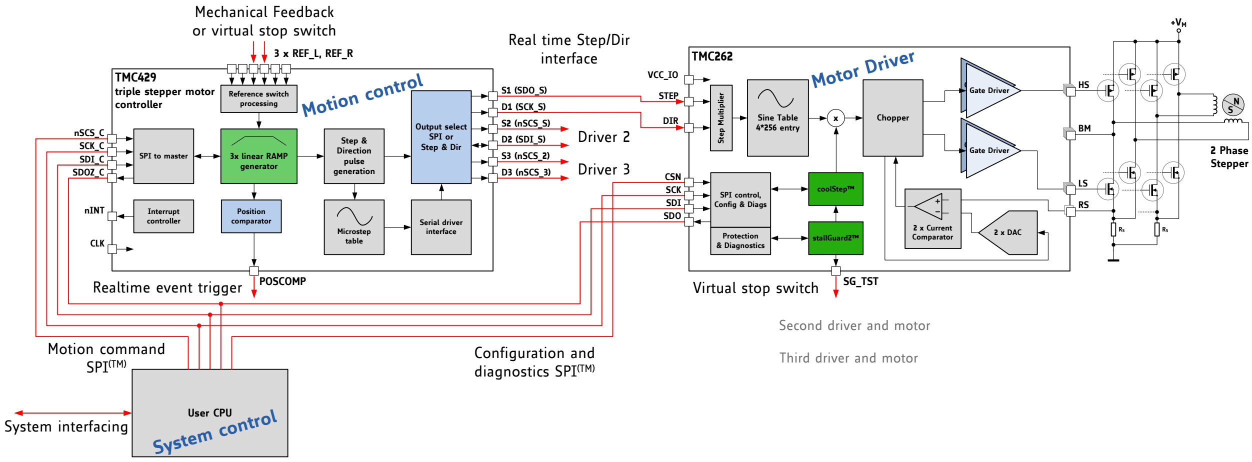


Figure 6.2 Interfaces to a TMC429 motion controller chip and a TMC262 motor driver

Figure 6.2 shows the interfaces in a typical application. The SPI bus is used by an embedded MCU to initialize the control registers of both a motion controller and one or more motor drivers. STEP/DIR interfaces are used between the motion controller and the motor drivers.

6.4 Register Write Commands

An SPI bus transaction to the TMC262 is a write command to one of the five write-only registers that hold configuration parameters and mode bits:

Register	**Description**
Driver Control Register (DRVCTRL)	The DRVCTRL register has different formats for controlling the interface to the motion controller depending on whether or not the STEP/DIR interface is enabled.
Chopper Configuration Register (CHOPCONF)	The CHOPCONF register holds chopper parameters and mode bits.
coolStep Configuration Register (SMARTEN)	The SMARTEN register holds coolStep parameters and a mode bit. (smartEnergy is an earlier name for coolStep.)
stallGuard2 Configuration Register (SGCSCONF)	The SGCSCONF register holds stallGuard2 parameters and a mode bit.
Driver Configuration Register (DRVCONF)	The DRVCONF register holds parameters and mode bits used to control the power MOSFETs and the protection circuitry. It also holds the SDOFF bit which controls the STEP/DIR interface and the RDSEL parameter which controls the contents of the response returned in an SPI transaction

In the following sections, multibit binary values are prefixed with a % sign, for example %0111.

6.4.1 Write Command Overview

The table below shows the formats for the five register write commands. Bits 19, 18, and sometimes 17 select the register being written, as shown in bold. The DRVCTRL register has two formats, as selected by the SDOFF bit. Bits shown as 0 must always be written as 0, and bits shown as 1 must always be written with 1. Detailed descriptions of each parameter and mode bit are given in the following sections.

Register/ Bit	**DRVCTRL (*SDOFF*=1)**	**DRVCTRL (*SDOFF*=0)**	**CHOPCONF**	**SMARTEN**	**SGCSCONF**	**DRVCONF**
19	**0**	**0**	**1**	**1**	**1**	**1**
18	**0**	**0**	**0**	**0**	**1**	**1**
17	PHA	0	**0**	**1**	**0**	**1**
16	CA7	0	TBL1	0	SFILT	TST
15	CA6	0	TBL0	SEIMIN	0	SLPH1
14	CA5	0	CHM	SEDN1	SGT6	SLPH0
13	CA4	0	RNDTF	SEDN0	SGT5	SLPL1
12	CA3	0	HDEC1	0	SGT4	SLPL0
11	CA2	0	HDEC0	SEMAX3	SGT3	0
10	CA1	0	HEND3	SEMAX2	SGT2	DISS2G
9	CA0	INTPOL	HEND2	SEMAX1	SGT1	TS2G1
8	PHB	DEDGE	HEND1	SEMAX0	SGT0	TS2G0
7	CB7	0	HEND0	0	0	*SDOFF*
6	CB6	0	HSTRT2	SEUP1	0	VSENSE
5	CB5	0	HSTRT1	SEUP0	0	*RDSEL1*
4	CB4	0	HSTRT0	0	CS4	*RDSEL0*
3	CB3	MRES3	TOFF3	SEMIN3	CS3	0
2	CB2	MRES2	TOFF2	SEMIN2	CS2	0
1	CB1	MRES1	TOFF1	SEMIN1	CS1	0
0	CB0	MRES0	TOFF0	SEMIN0	CS0	0

6.4.2 Read Response Overview

The table below shows the formats for the read response. The RDSEL parameter in the DRVCONF register selects the format of the read response.

Bit	***RDSEL*=%00**	***RDSEL*=%01**	***RDSEL*=%10**
19	MSTEP9	SG9	SG9
18	MSTEP8	SG8	SG8
17	MSTEP7	SG7	SG7
16	MSTEP6	SG6	SG6
15	MSTEP5	SG5	SG5
14	MSTEP4	SG4	SE4
13	MSTEP3	SG3	SE3
12	MSTEP2	SG2	SE2
11	MSTEP1	SG1	SE1
10	MSTEP0	SG0	SE0
9	-	-	-
8	-	-	-
7	STST		
6	OLB		
5	OLA		
4	S2GB		
3	S2GA		
2	OTPW		
1	OT		
0	SG		

6.5 Driver Control Register (DRVCTRL)

The format of the DRVCTRL register depends on the state of the SDOFF mode bit.

SPI Mode	SDOFF bit is set, the STEP/DIR interface is disabled, and DRVCTRL is the interface for specifying the currents through each coil.
STEP/DIR Mode	SDOFF bit is clear, the STEP/DIR interface is enabled, and DRVCTRL is a configuration register for the STEP/DIR interface.

6.5.1 DRVCTRL Register in SPI Mode

DRVCTRL		**Driver Control in SPI Mode (SDOFF=1)**	
Bit	**Name**	**Function**	**Comment**
19	0	Register address bit	
18	0	Register address bit	
17	PHA	Polarity A	Sign of current flow through coil A: 0: Current flows from OA1 pins to OA2 pins. 1: Current flows from OA2 pins to OA1 pins.
16	CA7	Current A MSB	Magnitude of current flow through coil A. The range is 0 to 248, if hysteresis or offset are used up to their full extent. The resulting value after applying hysteresis or offset must not exceed 255.
15	CA6		
14	CA5		
13	CA4		
12	CA3		
11	CA2		
10	CA1		
9	CA0	Current A LSB	

DRVCTRL		**Driver Control in SPI Mode (SDOFF=1)**	
Bit	**Name**	**Function**	**Comment**
8	PHB	Polarity B	Sign of current flow through coil B: 0: Current flows from OB1 pins to OB2 pins. 1: Current flows from OB2 pins to OB1 pins.
7	CB7	Current B MSB	Magnitude of current flow through coil B. The range is 0 to 248, if hysteresis or offset are used up to their full extent. The resulting value after applying hysteresis or offset must not exceed 255.
6	CB6		
5	CB5		
4	CB4		
3	CB3		
2	CB2		
1	CB1		
0	CB0	Current B LSB	

6.5.2 DRVCTRL Register in STEP/DIR Mode

DRVCTRL		**Driver Control in STEP/DIR Mode (SDOFF=0)**	
Bit	**Name**	**Function**	**Comment**
19	0	Register address bit	
18	0	Register address bit	
17	0	Reserved	
16	0	Reserved	
15	0	Reserved	
14	0	Reserved	
13	0	Reserved	
12	0	Reserved	
11	0	Reserved	
10	0	Reserved	
9	INTPOL	Enable STEP interpolation	0: Disable STEP pulse interpolation. 1: Enable STEP pulse multiplication by 16.
8	DEDGE	Enable double edge STEP pulses	0: Rising STEP pulse edge is active, falling edge is inactive. 1: Both rising and falling STEP pulse edges are active.
7	0	Reserved	
6	0	Reserved	
5	0	Reserved	
4	0	Reserved	
3	MRES3	Microstep resolution for STEP/DIR mode	Microsteps per 90°: %0000: 256 %0001: 128 %0010: 64 %0011: 32 %0100: 16 %0101: 8 %0110: 4 %0111: 2 (halfstep) %1000: 1 (fullstep)
2	MRES2		
1	MRES1		
0	MRES0		

6.6 Chopper Control Register (CHOPCONF)

CHOPCONF		**Chopper Configuration**		
Bit	**Name**	**Function**	**Comment**	
19	1	Register address bit		
18	0	Register address bit		
17	0	Register address bit		
16	TBL1	Blanking time	Blanking time interval, in system clock periods: %00: 16 %01: 24 %10: 36 %11: 54	
15	TBL0			
14	CHM	Chopper mode	This mode bit affects the interpretation of the HDEC, HEND, and HSTRT parameters shown below.	
			0	Standard mode (spreadCycle)
			1	Constant t_{OFF} with fast decay time. Fast decay time is also terminated when the negative nominal current is reached. Fast decay is after on time.
13	RNDTF	Random TOFF time	Enable randomizing the slow decay phase duration: 0: Chopper off time is fixed as set by bits t_{OFF} 1: Random mode, t_{OFF} is random modulated by dN_{CLK}= -12 … +3 clocks.	
12	HDEC1	Hysteresis decrement interval or Fast decay mode	CHM=0	Hysteresis decrement period setting, in system clock periods: %00: 16 %01: 32 %10: 48 %11: 64
11	HDEC0		CHM=1	HDEC1=0: current comparator can terminate the fast decay phase before timer expires. HDEC1=1: only the timer terminates the fast decay phase. HDEC0: MSB of fast decay time setting.
10	HEND3	Hysteresis end (low) value or Sine wave offset	CHM=0	%0000 … %1111: Hysteresis is -3, -2, -1, 0, 1, …, 12 (1/512 of this setting adds to current setting) This is the hysteresis value which becomes used for the hysteresis chopper.
9	HEND2			
8	HEND1		CHM=1	%0000 … %1111: Offset is -3, -2, -1, 0, 1, …, 12 This is the sine wave offset and 1/512 of the value becomes added to the absolute value of each sine wave entry.
7	HEND0			
6	HSTRT2	Hysteresis start value or Fast decay time setting	CHM=0	Hysteresis start offset from HEND: %000: 1 %100: 5 %001: 2 %101: 6 %010: 3 %110: 7 %011: 4 %111: 8 *Effective: HEND+HSTRT must be ≤ 15*
5	HSTRT1			
4	HSTRT0		CHM=1	Three least-significant bits of the duration of the fast decay phase. The MSB is HDEC0. Fast decay time is a multiple of system clock periods: N_{CLK}= 32 x (*HDEC0+HSTRT*)

CHOPCONF		**Chopper Configuration**	
Bit	**Name**	**Function**	**Comment**
3	TOFF3	Off time/MOSFET disable	Duration of slow decay phase. If TOFF is 0, the MOSFETs are shut off. If TOFF is nonzero, slow decay time is a multiple of system clock periods: N_{CLK}= 12 + (32 x TOFF) (Minimum time is 64clocks.) %0000: Driver disable, all bridges off %0001: 1 (use with TBL of minimum 24 clocks) %0010 … %1111: 2 … 15
2	TOFF2		
1	TOFF1		
0	TOFF0		

6.7 coolStep Control Register (SMARTEN)

SMARTEN		**coolStep Configuration**	
Bit	**Name**	**Function**	**Comment**
19	1	Register address bit	
18	0	Register address bit	
17	1	Register address bit	
16	0	Reserved	
15	SEIMIN	Minimum coolStep current	0: ½ CS current setting 1: ¼ CS current setting
14	SEDN1	Current decrement speed	Number of times that the stallGuard2 value must be sampled equal to or above the upper threshold for each decrement of the coil current: %00: 32 %01: 8 %10: 2 %11: 1
13	SEDN0		
12	0	Reserved	
11	SEMAX3	Upper coolStep threshold as an offset from the lower threshold	If the stallGuard2 measurement value SG is sampled equal to or above (SEMIN+SEMAX+1) x 32 enough times, then the coil current scaling factor is decremented.
10	SEMAX2		
9	SEMAX1		
8	SEMAX0		
7	0	Reserved	
6	SEUP1	Current increment size	Number of current increment steps for each time that the stallGuard2 value SG is sampled below the lower threshold: %00: 1 %01: 2 %10: 4 %11: 8
5	SEUP0		
4	0	Reserved	
3	SEMIN3	Lower coolStep threshold/coolStep disable	If SEMIN is 0, coolStep is disabled. If SEMIN is nonzero and the stallGuard2 value SG falls below SEMIN x 32, the coolStep current scaling factor is increased.
2	SEMIN2		
1	SEMIN1		
0	SEMIN0		

6.8 stallGuard2 Control Register (SGCSCONF)

SGCSCONF		**stallGuard2™ and Current Setting**	
Bit	**Name**	**Function**	**Comment**
19	1	Register address bit	
18	1	Register address bit	
17	0	Register address bit	
16	SFILT	stallGuard2 filter enable	0: Standard mode, fastest response time. 1: Filtered mode, updated once for each four fullsteps to compensate for variation in motor construction, highest accuracy.
15	0	Reserved	
14	SGT6	stallGuard2 threshold value	The stallGuard2 threshold value controls the optimum measurement range for readout and stall indicator output (SG_TST). A lower value results in a higher sensitivity and less torque is required to indicate a stall. The value is a two's complement signed integer. Values below -10 are not recommended. Range: -64 to +63
13	SGT5		
12	SGT4		
11	SGT3		
10	SGT2		
9	SGT1		
8	SGT0		
7	0	Reserved	
6	0	Reserved	
5	0	Reserved	
4	CS4	Current scale (scales digital currents A and B)	Current scaling for SPI and STEP/DIR operation. %00000 … %11111: 1/32, 2/32, 3/32, … 32/32 This value is biased by 1 and divided by 32, so the range is 1/32 to 32/32. Example: CS=20 is 21/32 current.
3	CS3		
2	CS2		
1	CS1		
0	CS0		

6.9 Driver Control Register (DRVCONF)

DRVCONF		**Driver Configuration**	
Bit	**Name**	**Function**	**Comment**
19	1	Register address bit	
18	1	Register address bit	
17	1	Register address bit	
16	TST	Reserved TEST mode	Must be cleared for normal operation. When set, the SG_TST output exposes digital test values, and the TEST_ANA output exposes analog test values. Test value selection is controlled by SGT1 and SGT0: TEST_ANA: %00: anatest_2vth, %01: anatest_dac_out, %10: anatest_vdd_half. SG_TST: %00: comp_A, %01: comp_B, %10: CLK, %11: on_state_xy
15	SLPH1	Slope control, high side	%00: Minimum %01: Minimum temperature compensation mode. %10: Medium temperature compensation mode. %11: Maximum In temperature compensated mode (tc), the MOSFET gate driver strength is increased if the overtemperature warning temperature is reached. This compensates for temperature dependency of high-side slope control.
14	SLPH0		
13	SLPL1	Slope control, low side	%00: Minimum. %01: Minimum. %10: Medium. %11: Maximum.
12	SLPL0		
11	0	Reserved	
10	DISS2G	Short to GND protection disable	0: Short to GND protection is enabled. 1: Short to GND protection is disabled.
9	TS2G1	Short to GND detection timer	%00: 3.2μs. %01: 1.6μs. %10: 1.2μs. %11: 0.8μs.
8	TS2G0		
7	SDOFF	STEP/DIR interface disable	0: Enable STEP/DIR operation. 1: Disable STEP/DIR operation. SPI interface is used to move motor.
6	VSENSE	Sense resistor voltage-based current scaling	0: Full-scale sense resistor voltage is 305mV. 1: Full-scale sense resistor voltage is 165mV. (Full-scale refers to a current setting of 31 and a DAC value of 255.)
5	RDSEL1	Select value for read out (RD bits)	%00 Microstep position read back %01 stallGuard2 level read back %10 stallGuard2 and coolStep current level read back %11 Reserved, do not use
4	RDSEL0		
3	0	Reserved	
2	0	Reserved	
1	0	Reserved	
0	0	Reserved	

6.10 Read Response

For every write command sent to the motor driver, a 20-bit response is returned to the motion controller. The response has one of three formats, as selected by the RDSEL parameter in the DRVCONF register. The table below shows these formats. Software must not depend on the value of any bit shown as reserved.

DRVSTATUS				**Read Response**	
Bit	**Name**			**Function**	**Comment**
	RDSEL=%00	**%01**	**%10**		
19	MSTEP9	SG9	SG9	Microstep counter for coil A *or* stallGuard2 value SG9:0 *or* stallGuard2 value SG9:5 *and* coolStep value SE4:0	Microstep position in sine table for coil A in STEP/DIR mode. MSTEP9 is the Polarity bit: 0: Current flows from OA1 pins to OA2 pins. 1: Current flows from OA2 pins to OA1 pins.
18	MSTEP8	SG8	SG8		
17	MSTEP7	SG7	SG7		
16	MSTEP6	SG6	SG6		
15	MSTEP5	SG5	SG5		stallGuard2 value SG9:0.
14	MSTEP4	SG4	SE4		
13	MSTEP3	SG3	SE3		
12	MSTEP2	SG2	SE2		stallGuard2 value SG9:5 and the actual coolStep scaling value SE4:0.
11	MSTEP1	SG1	SE1		
10	MSTEP0	SG0	SE0		
9	Reserved				
8	Reserved				
7	STST			Standstill indicator	0: No standstill condition detected. 1: No active edge occurred on the STEP input during the last 2^{20} system clock cycles.
6	OLB			Open load indicator	0: No open load condition detected. 1: No chopper event has happened during the last period with constant coil polarity. Only a current above 1/16 of the maximum setting can clear this bit! *Hint:* This bit is only a status indicator. The chip takes no other action when this bit is set. False indications may occur during fast motion and at standstill. Check this bit only during slow motion.
5	OLA				
4	S2GB			Short to GND detection bits on high-side transistors	0: No short to ground shutdown condition. 1: Short to ground shutdown condition. The short counter is incremented by each short circuit and the chopper cycle is suspended. The counter is decremented for each phase polarity change. The MOSFETs are shut off when the counter reaches 3 and remain shut off until the shutdown condition is cleared by disabling and re-enabling the driver. The shutdown condition becomes reset by deasserting the ENN input or clearing the TOFF parameter.
3	S2GA				
2	OTPW			Overtemperature warning	0: No overtemperature warning condition. 1: Warning threshold is active.
1	OT			Overtemperature shutdown	0: No overtemperature shutdown condition. 1: Overtemperature shutdown has occurred.
0	SG			stallGuard2 status	0: No motor stall detected. 1: stallGuard2 threshold has been reached, and the SG_TST output is driven high.

6.11 Device Initialization

The following sequence of SPI commands is an example of enabling the driver and initializing the chopper:

SPI = $901B4; // Hysteresis mode

or

SPI = $94557; // Constant t_{off} mode

SPI = $D001F; // Current setting: $d001F (max. current)

SPI = $EF010; // high gate driver strength, stallGuard read, SDOFF=0

SPI = $00000; // 256 microstep setting

First test of coolStep current control:

SPI = $A8202; // Enable coolStep with minimum current ¼ CS

The configuration parameters should be tuned to the motor and application for optimum performance.

7 STEP/DIR Interface

The STEP and DIR inputs provide a simple, standard interface compatible with many existing motion controllers. The microPlyer STEP pulse interpolator brings the smooth motor operation of high-resolution microstepping to applications originally designed for coarser stepping and reduces pulse bandwidth.

7.1 Timing

Figure 7.1 shows the timing parameters for the STEP and DIR signals, and the table below gives their specifications. When the DEDGE mode bit in the DRVCTRL register is set, both edges of STEP are active. If DEDGE is cleared, only rising edges are active. STEP and DIR are sampled and synchronized to the system clock. An internal analog filter removes glitches on the signals, such as those caused by long PCB traces. If the signal source is far from the chip, and especially if the signals are carried on cables, the signals should be filtered or differentially transmitted.

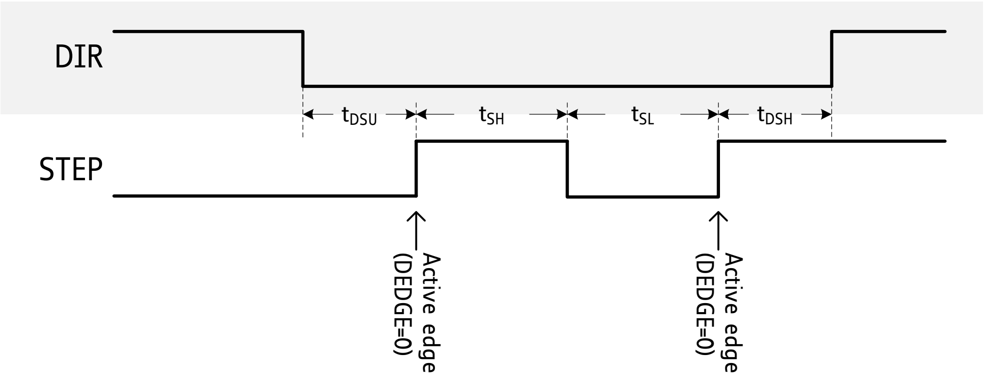


Figure 7.1 STEP/DIR timing

STEP and DIR Interface Timing	**AC-Characteristics** clock period is t_{CLK}					
Parameter	**Symbol**	**Conditions**	**Min**	**Typ**	**Max**	**Unit**
Step frequency (at maximum microstep resolution)	f_{STEP}	DEDGE=0			½ f_{CLK}	
		DEDGE=1			¼ f_{CLK}	
Fullstep frequency	f_{FS}				$f_{CLK}/512$	
STEP input low time	t_{SL}		max(t_{FILTSD}, t_{CLK}+20)			ns
STEP input high time	t_{SH}		max(t_{FILTSD}, t_{CLK}+20)			ns
DIR to STEP setup time	t_{DSU}		20			ns
DIR after STEP hold time	t_{DSH}		20			ns
STEP and DIR spike filtering time	t_{FILTSD}	Rising and falling edge	36	60	85	ns
STEP and DIR sampling relative to rising CLK input	$t_{SDCLKHI}$	Before rising edge of CLK		t_{FILTSD}		ns

7.2 Microstep Table

The internal microstep table maps the sine function from 0° to 90°, and symmetries allow mapping the sine and cosine functions from 0° to 360° with this table. The angle is encoded as a 10-bit unsigned integer MSTEP provided by the microstep counter. The size of the increment applied to the counter while microstepping through this table is controlled by the microstep resolution setting MRES in the DRVCTRL register. Depending on the DIR input, the microstep counter is increased (DIR=0) or decreased (DIR=1) by the step size with each STEP active edge. Despite many entries in the last quarter of the table being equal, the electrical angle continuously changes, because either the sine wave or cosine wave is in an area, where the current vector changes monotonically from position to position. Figure 7.2 shows the table. The largest values are 248, which leaves headroom used for adding an offset.

Entry	0-31	32-63	64-95	96-127	128-159	160-191	192-223	224-255
0	1	49	96	138	176	207	229	243
1	2	51	97	140	177	207	230	244
2	4	52	98	141	178	208	231	244
3	5	54	100	142	179	209	231	244
4	7	55	101	143	180	210	232	244
5	8	57	103	145	181	211	232	245
6	10	58	104	146	182	212	233	245
7	11	60	105	147	183	212	233	245
8	13	61	107	148	184	213	234	245
9	14	62	108	150	185	214	234	246
10	16	64	109	151	186	215	235	246
11	17	65	111	152	187	215	235	246
12	19	67	112	153	188	216	236	246
13	21	68	114	154	189	217	236	246
14	22	70	115	156	190	218	237	247
15	24	71	116	157	191	218	237	247
16	25	73	118	158	192	219	238	247
17	27	74	119	159	193	220	238	247
18	28	76	120	160	194	220	238	247
19	30	77	122	161	195	221	239	247
20	31	79	123	163	196	222	239	247
21	33	80	124	164	197	223	240	247
22	34	81	126	165	198	223	240	248
23	36	83	127	166	199	224	240	248
24	37	84	128	167	200	225	241	248
25	39	86	129	168	201	225	241	248
26	40	87	131	169	201	226	241	248
27	42	89	132	170	202	226	242	248
28	43	90	133	172	203	227	242	248
29	45	91	135	173	204	228	242	248
30	46	93	136	174	205	228	243	248
31	48	94	137	175	206	229	243	248

Figure 7.2 Internal microstep table showing the first quarter of the sine wave

7.3 Changing Resolution

The application may need to change the microstepping resolution to get the best performance from the motor. For example, high-resolution microstepping may be used for precision operations on a workpiece, and then fullstepping may be used for maximum torque at maximum velocity to advance to the next workpiece. When changing to coarse resolutions like fullstepping or halfstepping, switching should occur at or near positions that correspond to steps in the lower resolution, as shown in the table below.

Step Position	MSTEP Value	Coil A Current	Coil B Current
Half step 0	0	0%	100%
Full step 0	128	70.7%	70.7%
Half step 1	256	100%	0%
Full step 1	384	70.7%	-70.7%
Half step 2	512	0%	-100%
Full step 2	640	-70.7%	-70.7%
Half step 3	768	-100%	0%
Full step 3	896	-70.7%	70.7%

7.4 microPlyer Step Interpolator

For each active edge on STEP, microPlyer produces 16 microsteps at 256x resolution, as shown in Figure 7.3. microPlyer is enabled by setting the INTPOL bit in the DRVCTRL register. It supports input at 16x resolution, which it transforms into 256x resolution. The step rate for each 16 microsteps is determined by measuring the time interval of the previous step period and dividing it into 16 equal parts. The maximum time between two active edges on the STEP input corresponds to 2^{20} (roughly one million) system clock cycles, for an even distribution of 1/256 microsteps. At 16MHz system clock frequency, this results in a minimum step input frequency of 16Hz for microPlyer operation (one fullstep per second). A lower step rate causes the STST bit to be set, which indicates a standstill event. At that frequency, microsteps occur at a rate of $\frac{system\ clock\ frequency}{2^{16}} = 244Hz$.

microPlyer only works well with a stable STEP frequency. Do not use the DEDGE option if the STEP signal does not have a 50% duty cycle.

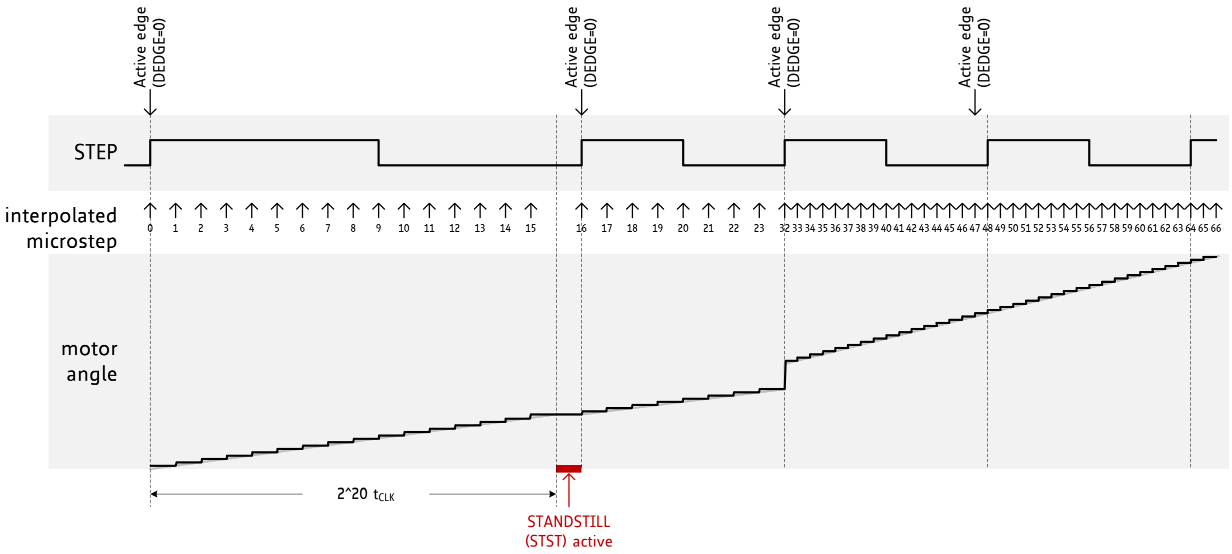


Figure 7.3 microPlyer microstep interpolation with rising STEP frequency

In Figure 7.3, the first STEP cycle is long enough to set the STST bit. This bit is cleared on the next STEP active edge. Then, the STEP frequency increases and after one cycle at the higher rate microPlyer increases the interpolated microstep rate. During the last cycle at the slower rate, microPlyer did not generate all 16 microsteps, so there is a small jump in motor angle between the first and second cycles at the higher rate.

7.5 Standstill current reduction

When a standstill event is detected, the motor current should be reduced to save energy and reduce heat dissipation in the power MOSFET stage. This is especially true at halfstep positions, which are a worst-case condition for the driver and motor because the full energy is consumed in one bridge and one motor coil.

8 Current Setting

The internal 5V supply voltage available at the pin 5VOUT is used as a reference for the coil current regulation based on the sense resistor voltage measurement. The desired maximum motor current is set by selecting an appropriate value for the sense resistor. The sense resistor voltage range can be selected by the VSENSE bit in the DRVCONF register. The low sensitivity (high sense resistor voltage, VSENSE=0) brings best and most robust current regulation, while high sensitivity (low sense resistor voltage, VSENSE=1) reduces power dissipation in the sense resistor. This setting reduces the power dissipation in the sense resistor by nearly half.

After choosing the VSENSE setting and selecting the sense resistor, the currents to both coils are scaled by the 5-bit current scale parameter CS in the SGCSCONF register. The sense resistor value is chosen so that the maximum desired current (or slightly more) flows at the maximum current setting (CS = %11111).

Using the internal sine wave table, which has amplitude of 248, the RMS motor current can be calculated by:

$$I_{RMS} = \frac{CS+1}{32} * \frac{V_{FS}}{R_{SENSE}} * \frac{1}{\sqrt{2}}$$

The momentary motor current is calculated as:

$$I_{MOT} = \frac{CURRENT_{A/B}}{248} * \frac{CS+1}{32} * \frac{V_{FS}}{R_{SENSE}}$$

where:

CS is the effective current scale setting as set by the CS bits and modified by coolStep. The effective value ranges from 0 to 31.

V_{FS} is the sense resistor voltage at full scale, as selected by the VSENSE control bit (refer to the electrical characteristics).

$CURRENT_{A/B}$ is the value set by the current setting in SPI mode or the internal sine table in STEP/DIR mode.

Parameter	Description	Setting	Comment
CS	*Current scale*. Scales both coil current values as taken from the internal sine wave table or from the SPI interface. For high precision motor operation, work with a current scaling factor in the range 16 to 31, because scaling down the current values reduces the effective microstep resolution by making microsteps coarser. This setting also controls the maximum current value set by coolStep™.	0 … 31	Scaling factor: 1/32, 2/32, … 32/32
VSENSE	Allows control of the sense resistor *voltage range* or adaptation of one electronic module to different maximum motor currents.	0	310mV
		1	165mV

8.1 Sense Resistors

Sense resistors should be carefully selected. The full motor current flows through the sense resistors. They also see the switching spikes from the MOSFET bridges. A low-inductance type such as film or composition resistors is required to prevent spikes causing ringing on the sense voltage inputs leading to unstable measurement results. A low-inductance, low-resistance PCB layout is essential. Any common GND path for the two sense resistors must be avoided, because this would lead to coupling between the two current sense signals. A massive ground plane is best. When using high currents or long motor cables, spike damping with parallel capacitors to ground may be needed, as shown in Figure 8.1. Because the sense resistor inputs are susceptible to damage from negative overvoltages, an additional input protection resistor helps protect against a motor cable break or ringing on long motor cables.

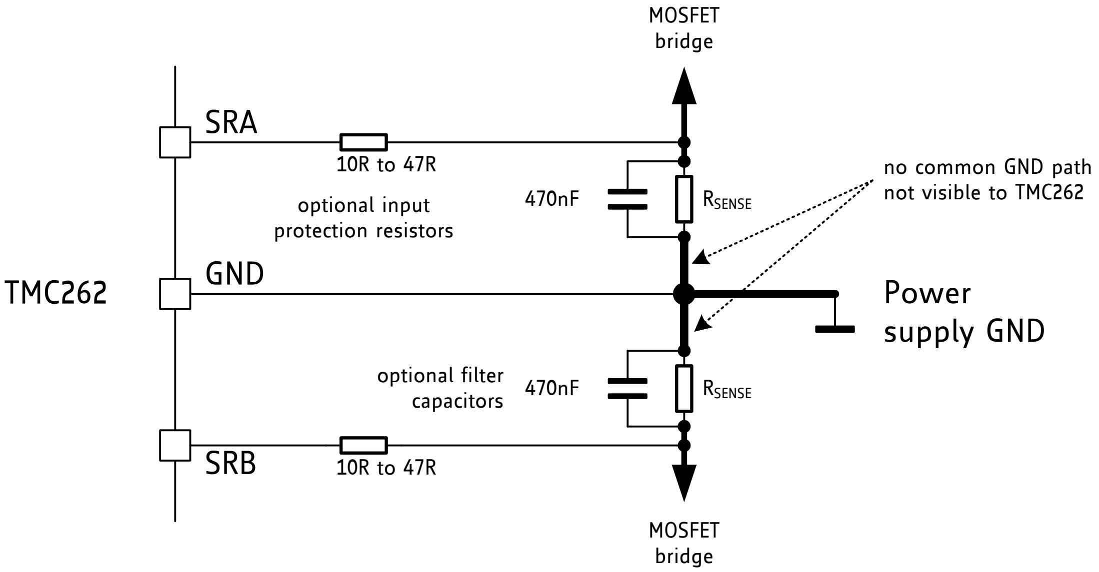


Figure 8.1 Sense resistor grounding and protection components

The sense resistor needs to be able to conduct the peak motor coil current in motor standstill conditions, unless standby power is reduced. Under normal conditions, the sense resistor sees a bit less than the coil RMS current, because no current flows through the sense resistor during the slow decay phases.

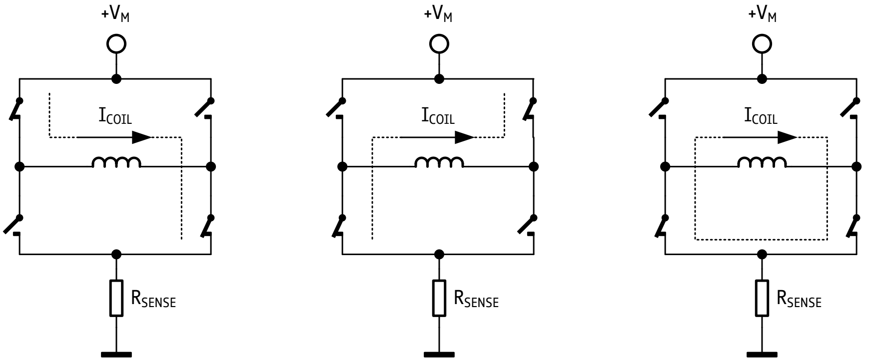
The peak sense resistor power dissipation is:

$$P_{RSMAX} = \frac{\left(V_{SENSE} * \frac{CS+1}{32}\right)^2}{R_{SENSE}}$$

For high-current applications, power dissipation is halved by using the lower sense resistor voltage setting and the corresponding lower resistance value. In this case, any voltage drop in the PCB traces has a larger influence on the result. A compact power stage layout with massive ground plane is best to avoid parasitic resistance effects.

9 Chopper Operation

The currents through both motor coils are controlled using choppers. The choppers work independently of each other. Figure 9.1 shows the three chopper phases:



On Phase:
current flows in
direction of target
current

Fast Decay Phase:
current flows in
opposite direction
of target current

Slow Decay Phase:
current re-circulation

Figure 9.1 Chopper phases

Although the current could be regulated using only on phases and fast decay phases, insertion of the slow decay phase is important to reduce electrical losses and current ripple in the motor. The duration of the slow decay phase is specified in a control parameter and sets an upper limit on the chopper frequency. The current comparator can measure coil current during phases when the current flows through the sense resistor, but not during the slow decay phase, so the slow decay phase is terminated by a timer. The on phase is terminated by the comparator when the current through the coil reaches the target current. The fast decay phase may be terminated by either the comparator or another timer.

When the coil current is switched, spikes at the sense resistors occur due to charging and discharging parasitic capacitances. During this time, typically one or two microseconds, the current cannot be measured. Blanking is the time when the input to the comparator is masked to block these spikes.

There are two chopper modes available: a new high-performance chopper algorithm called spreadCycle and a proven constant off-time chopper mode. The constant off-time mode cycles through three phases: on, fast decay, and slow decay. The spreadCycle mode cycles through four phases: on, slow decay, fast decay, and a second slow decay.

Three parameters are used for controlling both chopper modes:

Parameter	Description	Setting	Comment
TOFF	Off time. This setting controls the duration of the slow decay time and limits the maximum chopper frequency. For most applications an off time within the range of 5µs to 20µs will fit. If the value is 0, the MOSFETs are all shut off and the motor can freewheel. A value of 1 to 15 sets the number of system clock cycles in the slow decay phase to: $N_{CLK} = (TOFF \cdot 32) + 12$ The SD-Time is $t = \frac{1}{f_{CLK}} \cdot N_{CLK}$	0	Chopper off.
		1… 15	Off time setting. (1 will work with minimum blank time of 24 clocks.)

Parameter	Description	Setting	Comment
TBL	Blanking time. This time needs to cover the switching event and the duration of the ringing on the sense resistor. For most low-current applications, a setting of 16 or 24 is good. For high-current applications, a setting of 36 or 54 may be required.	0	16 system clock cycles
		1	24 system clock cycles
		2	36 system clock cycles
		3	54 system clock cycles
CHM	Chopper mode bit	0	spreadCycle mode
		1	Constant off time mode

9.1 spreadCycle Mode

The spreadCycle chopper algorithm (pat.fil.) is a precise and simple to use chopper mode which automatically determines the optimum length for the fast-decay phase. Several parameters are available to optimize the chopper to the application.

Each chopper cycle is comprised of an on phase, a slow decay phase, a fast decay phase and a second slow decay phase (see Figure 9.2). The slow decay phases limit the maximum chopper frequency and are important for low motor and driver power dissipation. The hysteresis start setting limits the chopper frequency by forcing the driver to introduce a minimum amount of current ripple into the motor coils. The motor inductance limits the ability of the chopper to follow a changing motor current. The duration of the on phase and the fast decay phase must be longer than the blanking time, because the current comparator is disabled during blanking. This requirement is satisfied by choosing a positive value for the hysteresis as can be estimated by the following calculation:

$$dI_{COILBLANK} = V_M * \frac{t_{BLANK}}{L_{COIL}}$$

$$dI_{COILSD} = R_{COIL} * I_{COIL} * \frac{2 * t_{SD}}{L_{COIL}}$$

where:

$dI_{COILBLANK}$ is the coil current change during the blanking time.

dI_{COILSD} is the coil current change during the slow decay time.

t_{SD} is the slow decay time.

t_{BLANK} is the blanking time (as set by TBL).

V_M is the motor supply voltage.

I_{COIL} is the peak motor coil current at the maximum motor current setting CS.

R_{COIL} and L_{COIL} are motor coil inductance and motor coil resistance.

With this, a lower limit for the start hysteresis setting can be determined:

$$Hysteresis\ Start \geq (dI_{COILBLANK} + dI_{COILSD}) * \frac{2 * 248}{I_{COIL}} * \frac{CS + 1}{32}$$

Example:

For a 42mm stepper motor with 7.5mH, 4.5Ω phase, and 1A RMS current at CS=31, i.e. 1.41A peak current, at 24V with a blank time of 1.5µs:

$$dI_{COILBLANK} = 24V * \frac{2\mu s}{7.5mH} = 6.4mA$$

$$dI_{COILSD} = 4.5\Omega * 1.41A * \frac{2 * 5\mu s}{7.5mH} = 8.5mA$$

With this, the minimum hysteresis start setting is 5.2. A value in the range 6 to 10 can be used.

An Excel spreadsheet is provided for performing these calculations.

As experiments show, the setting is quite independent of the motor, because higher current motors typically also have a lower coil resistance. Choosing a medium default value for the hysteresis (for example, effective HSTRT+HEND=10) normally fits most applications. The setting can be optimized by experimenting with the motor: A too low setting will result in reduced microstep accuracy, while a too high setting will lead to more chopper noise and motor power dissipation. When measuring the sense resistor voltage in motor standstill at a medium coil current with an oscilloscope, a too low setting shows a fast decay phase not longer than the blanking time. When the fast decay time becomes slightly longer than the blanking time, the setting is optimum. You can reduce the off-time setting, if this is hard to reach.

The hysteresis principle could in some cases lead to the chopper frequency becoming too low, for example when the coil resistance is high compared to the supply voltage. This is avoided by splitting the hysteresis setting into a start setting (HSTRT+HEND) and an end setting (HEND). An automatic hysteresis decrementer (HDEC) interpolates between these settings, by decrementing the hysteresis value stepwise each 16, 32, 48, or 64 system clock cycles. At the beginning of each chopper cycle, the hysteresis begins with a value which is the sum of the start and the end values (HSTRT+HEND), and decrements during the cycle, until either the chopper cycle ends or the hysteresis end value (HEND) is reached. This way, the chopper frequency is stabilized at high amplitudes and low supply voltage situations, if the frequency gets too low. This avoids the frequency reaching the audible range.

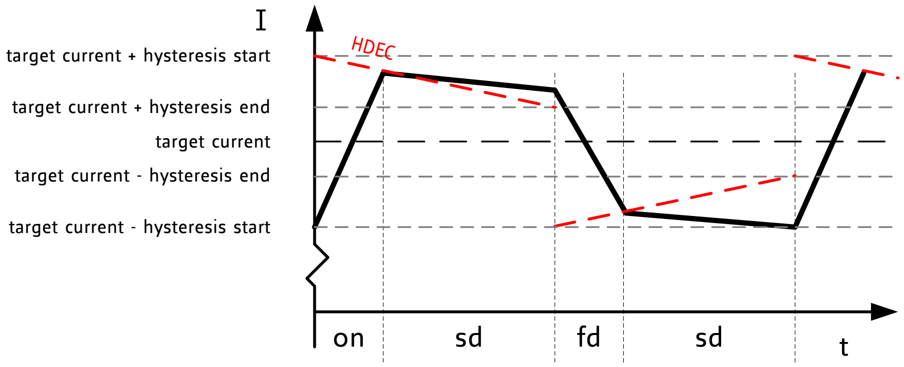


Figure 9.2 spreadCycle chopper mode showing the coil current during a chopper cycle

Three parameters control spreadCycle mode:

Parameter	Description	Setting	Comment
HSTRT	*Hysteresis start* setting. Please remark, that this value is an offset to the hysteresis end value HEND.	0… 7	This setting adds to HEND. %000: 1 %100: 5 %001: 2 %101: 6 %010: 3 %110: 7 %011: 4 %111: 8
HEND	*Hysteresis end* setting. Sets the hysteresis end value after a number of decrements. Decrement interval time is controlled by HDEC. The sum HSTRT+HEND must be <16. At a current setting CS of max. 30 (amplitude reduced to 240), the sum is not limited.	0… 2	Negative HEND: -3… -1 %0000: -3 %0001: -2 %0010: -1
		3	Zero HEND: 0 %0011: 0
		4… 15	Positive HEND: 1… 12 %0100: 1 %1010: 7 %0101: 2 %1011: 8 %0110: 3 %1100: 9 %0111: 4 %1101: 10 %1000: 5 %1110: 11 %1001: 6 %1111: 12

Parameter	Description	Setting	Comment
HDEC	*Hysteresis decrement* setting. This setting determines the slope of the hysteresis during on time and during fast decay time. It sets the number of system clocks for each decrement.	0… 3	0: fast decrement 3: very slow decrement %00: 16 %01: 32 %10: 48 %11: 64

Example:

In the example above, a hysteresis start of 7 has been chosen. The hysteresis end is set to about half of this value, 3. The resulting configuration register values are:

HEND=6	(sets an effective end value of 3)
HSTRT=3	(sets an effective start value of hysteresis end +4)
HDEC=0	(Hysteresis decrement becomes used)

9.2 Constant Off-Time Mode

The classic constant off-time chopper uses a fixed-time fast decay following each on phase. While the duration of the on phase is determined by the chopper comparator, the fast decay time needs to be fast enough for the driver to follow the falling slope of the sine wave, but it should not be so long that it causes excess motor current ripple and power dissipation. This can be tuned using an oscilloscope or evaluating motor smoothness at different velocities. A good starting value is a fast decay time setting similar to the slow decay time setting.

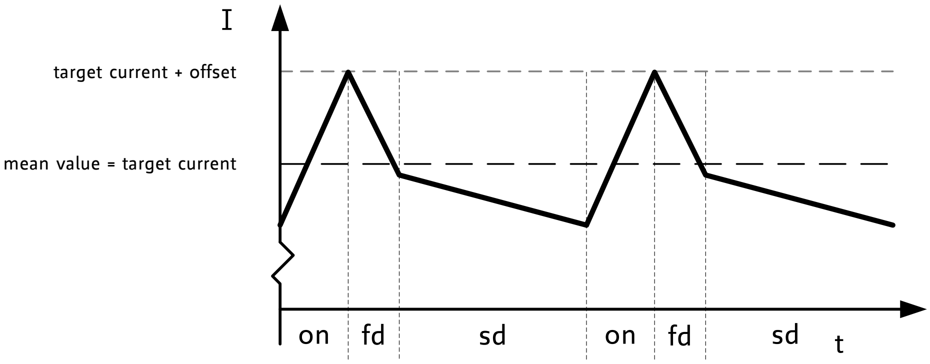


Figure 9.3 Constant off-time chopper with offset showing the coil current during two cycles

After tuning the fast decay time, the offset should be tuned for a smooth zero crossing. This is necessary because the fast decay phase makes the absolute value of the motor current lower than the target current (see Figure 9.4). If the zero offset is too low, the motor stands still for a short moment during current zero crossing. If it is set too high, it makes a larger microstep. Typically, a positive offset setting is required for smoothest operation.

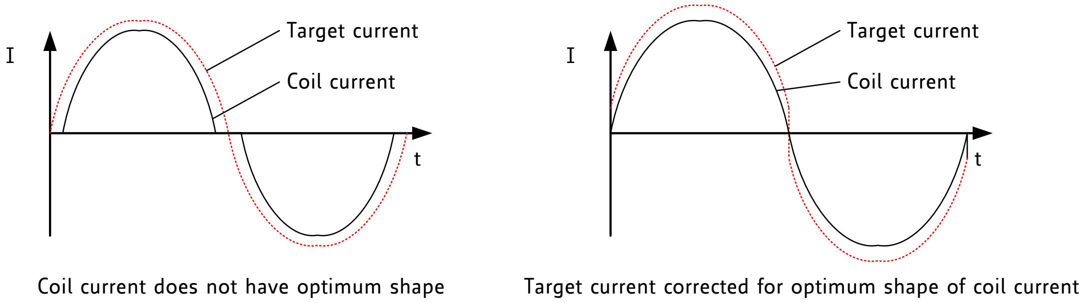


Figure 9.4 Zero crossing with correction using sine wave offset

Three parameters control constant off-time mode:

Parameter	**Description**	**Setting**	**Comment**
TFD (HSTART & HDEC0)	*Fast decay time* setting. With CHM=1, these bits control the portion of fast decay for each chopper cycle.	0	Slow decay only.
		1… 15	Duration of fast decay phase.
OFFSET (HEND)	*Sine wave offset*. With CHM=1, these bits control the sine wave offset. A positive offset corrects for zero crossing error.	0…2	Negative offset: -3… -1
		3	No offset: 0
		4… 15	Positive offset: 1… 12
NCCFD (HDEC1)	Selects usage of the *current comparator* for termination of the *fast decay* cycle. If current comparator is enabled, it terminates the fast decay cycle in case the current reaches a higher negative value than the actual positive value.	0	Enable comparator termination of fast decay cycle.
		1	End by time only.

9.2.1 Random Off Time

In the constant off-time chopper mode, both coil choppers run freely without synchronization. The frequency of each chopper mainly depends on the coil current and the motor coil inductance. The inductance varies with the microstep position. With some motors, a slightly audible beat can occur between the chopper frequencies when they are close together. This typically occurs at a few microstep positions within each quarter wave. This effect is usually not audible when compared to mechanical noise generated by ball bearings, etc. Another factor which can cause a similar effect is a poor layout of the sense resistor GND connections.

A common cause of motor noise is a bad PCB layout causing coupling of both sense resistor voltages.

To minimize the effect of a beat between both chopper frequencies, an internal random generator is provided. It modulates the slow decay time setting when switched on by the RNDTF bit. The RNDTF feature further spreads the chopper spectrum, reducing electromagnetic emission on single frequencies.

Parameter	**Description**	**Setting**	**Comment**
RNDTF	Enables a random off-time generator, which slightly modulates the off time t_{OFF} using a random polynomial.	0	Disable.
		1	Random modulation enable.

10 Power MOSFET Stage

The TMC262 provides gate drivers for two full-bridges using N- and P-channel power MOSFETs. The gate current for the MOSFETs can be adapted to influence the slew rate at the coil outputs. The main features of the stage are:

- 5V gate drive voltage for low-side N-MOS transistors, 8V for high-side P-MOS transistors.
- The gate drivers protect the bridges actively against cross-conduction using an internal Q_{GD} protection that holds the MOSFETs safely off.
- Automatic break-before-make logic minimizes dead time and diode-conduction time.
- Integrated short to ground protection detects a short of the motor wires and protects the MOSFETs.

The low-side gate driver is supplied by the 5VOUT pin. The low-side driver supplies 0V to the MOSFET gate to close the MOSFET, and 5VOUT to open it. The high-side gate driver voltage is supplied by the VS and the VHS pin. VHS is more negative than VS and allows opening the VS referenced high-side MOSFET. The high-side driver supplies VS to the P channel MOSFET gate to close the MOSFET and VHS to open it. The effective low-side gate voltage is roughly 5V; the effective high-side gate voltage is roughly 8V.

Parameter	Description	Setting	Comment
SLPL	Low-side slope control. Controls the MOSFET gate driver current. Set to a value appropriate for the external MOSFET gate charge and the desired slope.	0… 3	%00: Minimum. %01: Minimum. %10: Medium. %11: Maximum.
SLPH	High-side slope control. Controls the MOSFET gate driver current. Set to a value appropriate for the external MOSFET gate charge and the desired slope.	0… 3	%00: Minimum. %01: Minimum+TC. %10: Medium+TC. %11: Maximum.

10.1 Break-Before-Make Logic

Each half-bridge has to be protected against cross-conduction during switching events. When switching off the low-side MOSFET, its gate first needs to be discharged before the high-side MOSFET is allowed to switch on. The same goes when switching off the high-side MOSFET and switching on the low-side MOSFET. The time for charging and discharging of the MOSFET gates depends on the MOSFET gate charge and the gate driver current set by SLPL and SLPH. The BBM (break-before-make) logic measures the gate voltage and automatically delays turning on the opposite bridge transistor until its counterpart is discharged. This way, the bridge will always switch with optimized timing independent of the slope setting.

10.2 ENN Input

The MOSFETs can be completely disabled in hardware by pulling the ENN input high. This allows the motor to free-wheel. An equivalent function can be performed in software by setting the parameter TOFF to zero. The hardware disable is available for allowing the motor to be hot plugged. If a hardware disable function is not needed, tie ENN low.

10.3 Slope Control

The TMC262 provides constant-current gate drivers for slope control. This allows adapting the driver strength to the drive requirements of the power MOSFETs and adjusting the output slope of the controlled gate charge and discharge. A slower slope reduces electromagnetic emissions, but it increases power dissipation in the MOSFETs.

The duration of the complete switching event depends on the total gate charge of the MOSFETs. In Figure 10.1, the voltage transition of the gate-charge output (dotted line) takes place during the so-called Miller plateau. The Miller plateau results from the gate-to-drain capacitance of the MOSFET charging or discharging during switching. The datasheet for the MOSFETs typically will show a Miller plateau that only covers a part (for example, one quarter) of the complete charging/discharging event. The gate voltage level at which the Miller plateau starts depends on the threshold voltage of the MOSFET and on the actual load current.

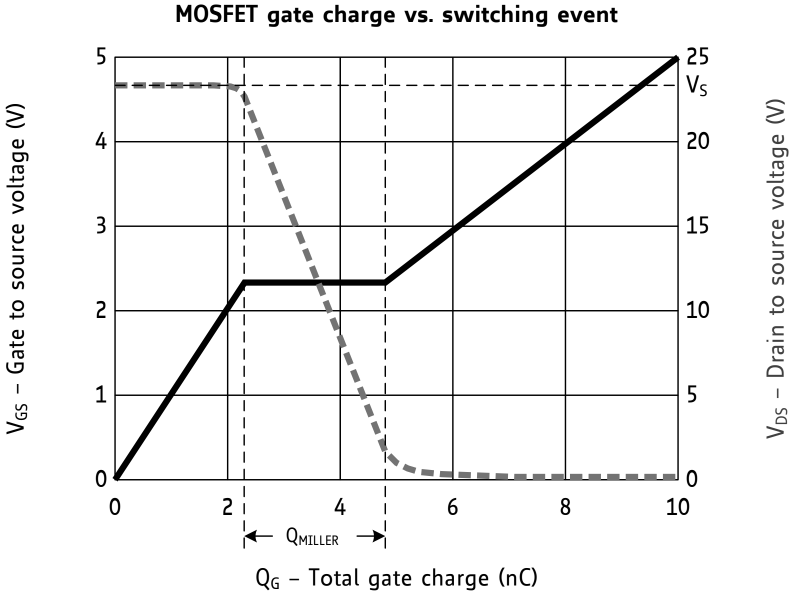


Figure 10.1 MOSFET gate charge vs. V_{DS} for a typical MOSFET during a switching event

The slope time t_{SLOPE} can be calculated as:

$$t_{SLOPE} = \frac{Q_{MILLER}}{I_{GATE}}$$

Where:
Q_{MILLER} is the charge the MOSFET needs for the switching event.
I_{GATE} is the driver current setting.

The chopper frequency is typically slightly above the audible range, around 18 kHz to 40 kHz. The lower limit for the slope is dictated by the reverse recovery time of the MOSFET internal diodes, unless additional Schottky diodes are used in parallel to the MOSFETs source-drain diode. For most applications a switching time between 100ns and 750ns is chosen.

Example:

> A circuit using the transistor in Figure 10.1 is operated with a gate current setting of 15mA. The Miller charge of the transistor is about 2.5nC.

$$t_{SLOPE} = \frac{2.5nC}{15mA} = 166ns$$

11 Diagnostics and Protection

11.1 Short to GND Detection

The short to ground detection prevents the high-side power MOSFETs from being damaged by accidentally shorting the motor outputs to ground. It disables the MOSFETs only if a short condition persists. A temporary event like an ESD event could look like a short, but these events are filtered out by requiring the event to persist.

When a short is detected, the bridge is switched off immediately, the chopper cycle on the affected coil is terminated, and the short counter is incremented. The counter is decremented for each phase polarity change. The MOSFETs are shut off when the counter reaches 3 and remain shut off until the short condition is cleared by disabling the driver and re-enabling it.

The short to ground detection status is indicated by two bits:

Status	Description	Range	Comment
S2GA	These bits identify a short to GND condition on coil A and coil B persisting for multiple chopper cycles. The bits are cleared when the MOSFETs are disabled.	0 / 1	0: No short condition detected. 1: Short condition detected.
S2GB			

An overload condition on the high-side MOSFET ("short to GND") is detected by monitoring the coil voltage during the high-side on phase. Under normal conditions, the high-side power MOSFET reaches the bridge supply voltage minus a small voltage drop during the on phase. If the bridge is overloaded, the voltage cannot rise to the detection level within the time defined by the internal detection delay setting. When an overload is detected, the bridge is switched off. The short to GND detection delay needs to be adjusted for the slope time, because it must be longer than slope, but should not be unnecessarily long.

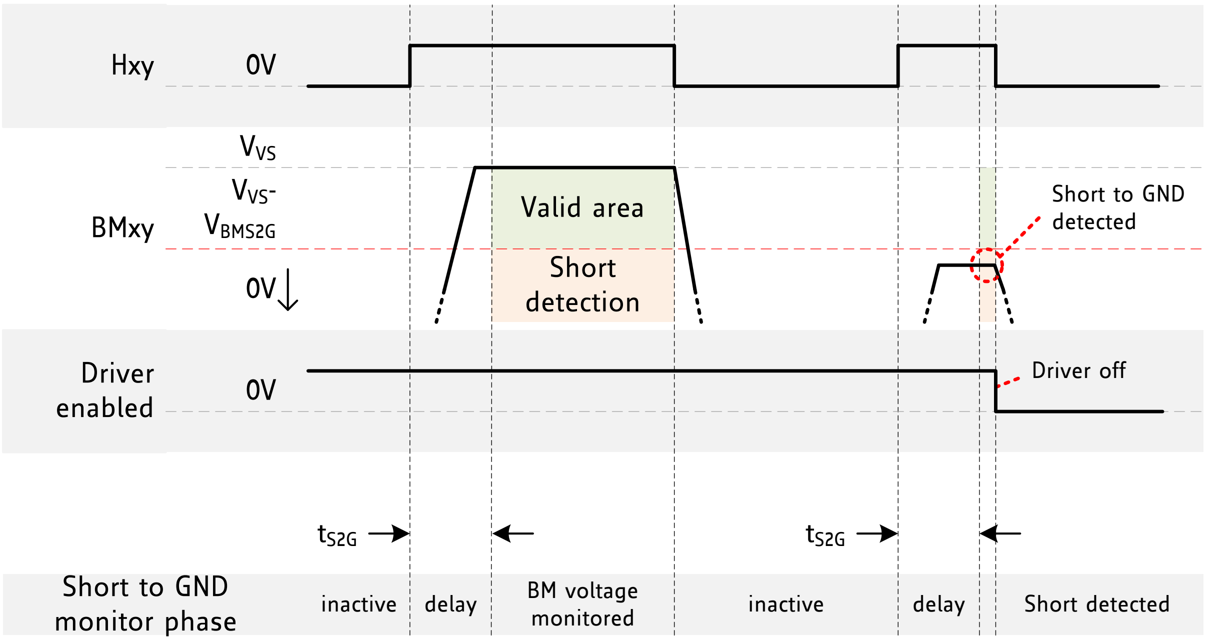


Figure 11.1 Short to GND detection timing

The short to ground detector is controlled by a mode bit and a parameter:

Mode bit / Parameter	Description	Setting	Comment
DISS2G	Short to ground detection disable bit.	0/1	0: Short to ground detection enabled. 1: Short to ground detection disabled.
TS2G	This setting controls the short to GND detection delay time. It needs to cover the switching slope time. A higher setting reduces sensitivity to capacitive loads.	0… 3	%00: 3.2µs. %01: 1.6µs. %10: 1.2µs. %11: 0.8µs.

11.2 Open-Load Detection

The open-load detection determines whether a motor coil has an open condition, for example due to a loose contact. When driving in fullstep mode, the open-load detection will also signal when the motor current cannot be reached within each step, for example due to a too-high motor velocity in which the back EMF voltage exceeds the supply voltage. The detection bit is only for information, and no other action is performed by the chip. Assertion of an open-load condition does not always indicate that the motor is not working properly. The bit is updated during normal operation whenever the polarity of the respective coil toggles.

The open-load detection status is indicated by two bits:

Status flag	Description	Range	Comment
OLA	These bits indicate an open-load condition on coil A and coil B. The flags become set, if no chopper event has happened during the last period with constant coil polarity. The flag is not updated with too low actual coil current below 1/16 of maximum setting.	0 / 1	0: No open-load detected 1: Open-load detected
OLB			

11.3 Overtemperature Detection

The TMC262 integrates a two-level temperature sensor (100°C warning and 150°C shutdown) for diagnostics and for protection of the power MOSFETs. The temperature detector can be triggered by heat accumulation on the board, for example due to missing convection cooling. Most critical situations, in which the MOSFETs could be overheated, are avoided when using the short to ground protection. For most applications, the overtemperature warning indicates an abnormal operation situation and can be used to trigger an alarm or power-reduction measures. If continuous operation in hot environments is necessary, a more precise mechanism based on temperature measurement should be used. The thermal shutdown is strictly an emergency measure and temperature rising to the shutdown level should be prevented by design. The shutdown temperature is above the specified operating temperature range of the chip.

The high-side P-channel gate drivers have a temperature dependency which can be compensated to some extent by increasing the gate driver current when the warning temperature threshold is reached. The chip automatically corrects for the temperature dependency above the warning temperature when the temperature-compensated modes of SLPH is used. In these modes, the gate driver current is increased by one step when the temperature warning threshold is reached.

Status	Description	Range	Comment
OTPW	Overtemperature warning. This bit indicates whether the warning threshold is reached. Software can react to this setting by reducing current.	0 / 1	1: temperature prewarning level reached
OT	Overtemperature shutdown. This bit indicates whether the shutdown threshold has been reached and the driver has been disabled.	0 / 1	1: driver shut down due to over-temperature

11.4 Undervoltage Detection

The undervoltage detector monitors both the internal logic supply voltage and the supply voltage. It prevents operation of the chip when the MOSFETs cannot be guaranteed to operate properly because the gate drive voltage is too low. It also initializes the chip at power up.

In undervoltage conditions, the logic control block becomes reset and the driver is disabled. All MOSFETs are switched off. All internal registers are reset to zero. Software also should monitor the supply voltage to detect an undervoltage condition. If software cannot measure the supply voltage, an undervoltage condition can be detected when the response to an SPI command returns only zero bits in the response and no bits are shifted through the internal shift register from SDI to SDO. After a reset due to undervoltage occurs, the CS parameter is cleared, which is reflected in an SE status of 0 in the read response.

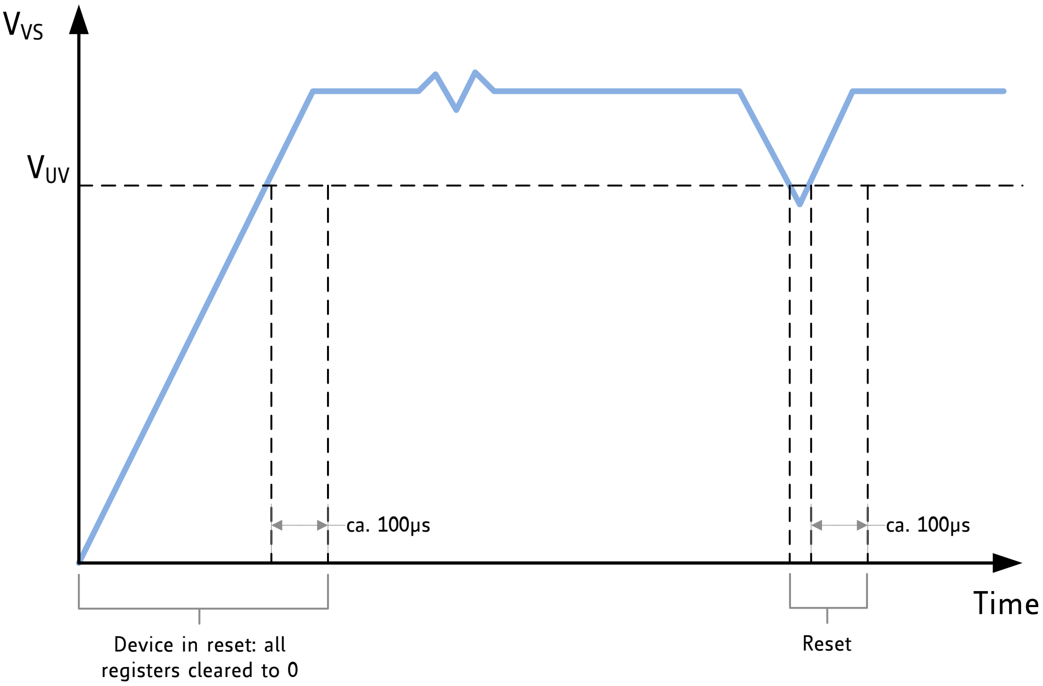


Figure 11.2 Undervoltage reset timing

Note: Be sure to operate the IC significantly above the undervoltage threshold to ensure reliable operation! Check for SE reading back as zero to detect an undervoltage event.

12 Power Supply Sequencing

The TMC262 generates its own 5V supply for all internal operations. The internal reset of the chip is derived from the supply voltage regulator in order to ensure a clean start-up of the device after power up. During start up, the SPI unit is in reset and cannot be addressed. All registers become cleared.

VCC_IO limits the voltage allowable on the inputs and outputs and is used for driving the outputs, but input levels thresholds are not depending on the actual level of VCC_IO. Therefore, the startup sequence of the VCC_IO power supply with respect to VS is not important.

13 System Clock

The internal system clock frequency for all operations is nominally 15MHz. An external clock of 10MHz to 20MHz (16MHz recommended for optimum performance) can be supplied for more exact timing, especially when using coolStep and stallGuard2. Alternatively, the on-chip oscillator clock frequency can be determined by measuring the delay time between the last step and assertion of the STST status bit, which is 2^{20} clocks. There is some delay in reading the STST bit through the SPI interface, but it is possible to measure the oscillator frequency within 1%. Chopper timing parameters can then be corrected using this measurement, because the oscillator is relatively stable over a wide range of environmental temperatures.

An external clock frequency of up to 20MHz can be supplied. The external clock is enabled and the on-chip oscillator is disabled with the first logic high driven on the CLK input. To use the on-chip oscillator, tie CLK to GND near the chip. If the external clock is suspended or disabled after the oscillator has been disabled, the chip will not operate. Be careful to switch off the power MOSFETs (by driving the ENN input high or setting the TOFF parameter to 0) before switching off the clock, because otherwise the chopper would stop and the motor current level could rise uncontrolled. If the short to GND detection is enabled, it stays active even without clock.

13.1 Frequency Selection

A higher frequency allows faster step rates, faster SPI operation, and higher chopper frequencies. On the other hand, it may cause more electromagnetic emission and more power dissipation in the digital logic. Generally, a system clock frequency of 8MHz to 16MHz should be sufficient for most applications, unless the motor is to operate at the highest velocities. If the application can tolerate reduced motor velocity and increased chopper noise, a clock frequency of 4MHz to 8MHz should be considered.

14 MOSFET Examples

There are a number of N- and P-channel paired MOSFETs available suitable for the TMC262, as well as single N- and P-devices. The important considerations are the electrical data (voltage, current, RDSon), package, and configuration (single vs. dual). The following table shows a few examples of SMD MOSFET pairs for different motor voltages and currents. These MOSFETs are recent types with a low total gate charge.

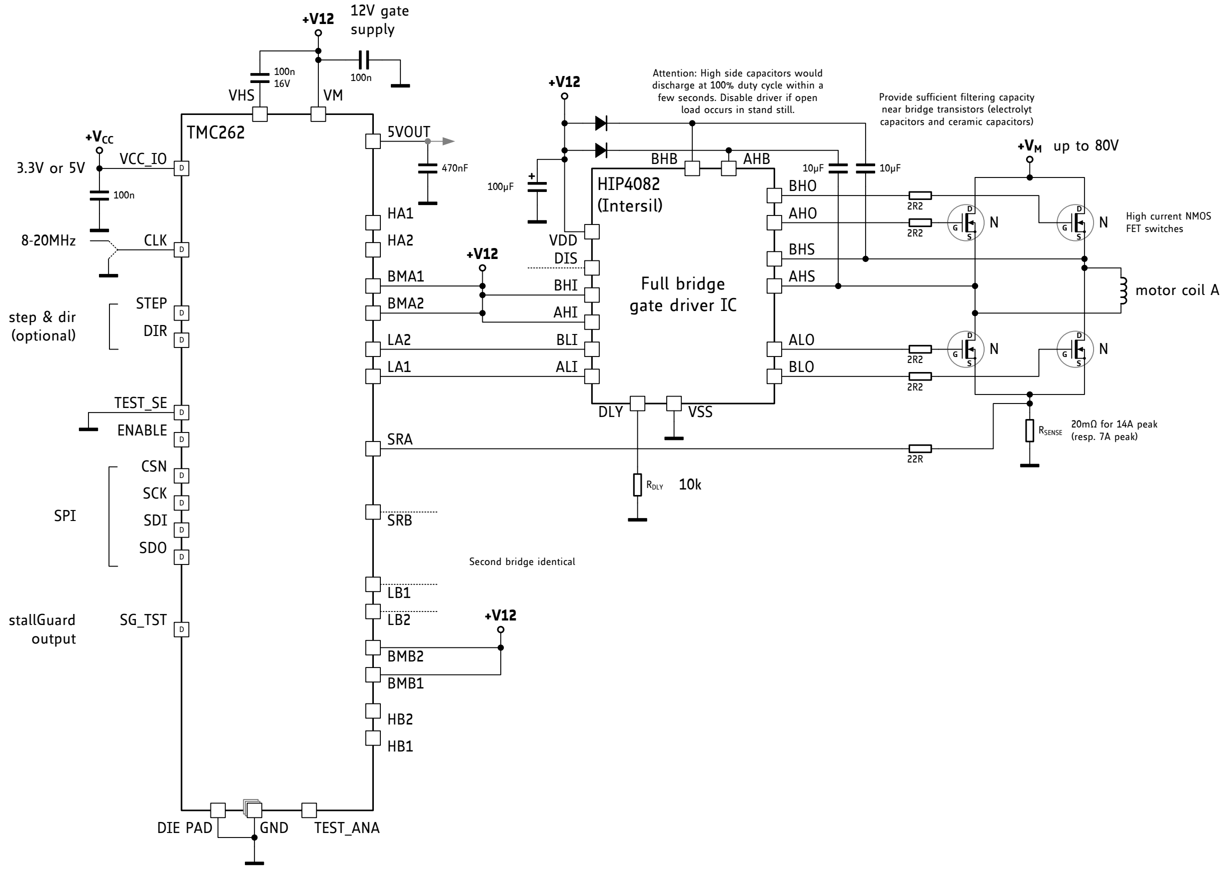
For the actual application, you should calculate static and dynamic power dissipation for a given MOSFET pair. A gate charge below 20nC (at 5V) is best for reaching reasonable slopes.

Transistor Type	**Manu-facturer**	**Voltage V_{DS}**	**Max. RMS Current (*)**	**Package**	**R_{DSon} N (5V)**	**R_{DSon} P (8V)**	**Q_G N**	**Q_G P**
Unit		**V**	**A**		**mΩ**	**mΩ**	**nC**	**nC**
SUD23N06 SUD19P06	Vishay	60	6	DPAK	35	50	8	22
SI7414 SI7415	Vishay	60	3	PPAK1212	28	60	9	12
SI7530	Vishay	60	3	PPAK-SO8	70	55	6	22
SI4559ADY	Vishay	60	2.2	SO8	55	110	7	12
IRF7343	Vishay	55	1.8	SO8	55	125	13	22
FDD8647L FDD4243	Fairchild	40	6	DPAK	13	40	12	18
FDD8424H	Fairchild	40	4.2	DPAK-4L	25	45	9	14
SI4565DY	Vishay	40	3	SO8	35	45	9	13
SI4567DY	Vishay	40	2.5	SO8	60	80	6	10
SI3529DV	Vishay	40	1.5	TSOP-6	110	190	2.5	4
FDS8960C	Fairchild	35	3.3	SO8	20	45	6	9
BSZ050N03 BSZ180P03	Infineon	30	8	S3O8	7	18	13	15
FDS8958A	Fairchild	30	3.2	SO8	25	45	6	9
TMC34NP	TRINAMIC	30	3	PPAK1212	35	50	5	11
SI4544DY	Vishay	30	3	SO8	40	40	9	15
SI4539ADY	Vishay	30	2.8	SO8	45	50	6	12
SI4532ADY	Vishay	30	2.7	SO8	50	70	4	8
IRF9952	Vishay	30	2	SO8	80	220	4	5.5

**** The maximum motor current applicable in a given design depends upon PCB size and layout, because all of these transistors are mainly cooled through the PCB. The data given implies adequate cooling measures in the design, especially for higher current designs. The maximum RMS current rating takes into account package power dissipation, on resistances, and gate charges.***

15 External Power Stage

The TMC262 uses a completely complementary driving scheme for the power MOSFETs. This allows using the low-side gate driver outputs to control external gate drivers for the power MOSFETs. In this case, the external gate driver must provide the break-before-make function. You can directly connect gate driver chips like the TMC603 as gate drivers for high-current NMOS transistor bridges. The TMC603 also supplies a gate-drive voltage regulator and allows 100% duty cycle. See the TMC603 datasheet for more information. The examples below show standard low-side and high-side drivers for boosting the TMC262. The higher gate-driving capability allows designs that exceed 20A and voltages above 60V. Two example schematics are shown for different gate-driver configurations.



Attention: High side capacitors would discharge at 100% duty cycle within a few seconds. Disable driver if open load occurs in stand still.

Provide sufficient filtering capacity near bridge transistors (electrolyt capacitors and ceramic capacitors)

Figure 15.1 High-current, high-voltage power stage using external gate drivers (minimum part count)

The short to GND protection of the TMC262 cannot be used in the configuration shown in Figure 15.1. The driver cannot be fully disabled, because the external gate driver just switches on either the high-side MOSFET or the low-side MOSFET. In this configuration, the external driver adds break-before-make capability. A configuration that takes advantage of the TMC262 short to GND protection is shown in Figure 15.2. The control style shown in this example can also be applied to the gate driver shown in Figure 15.1.

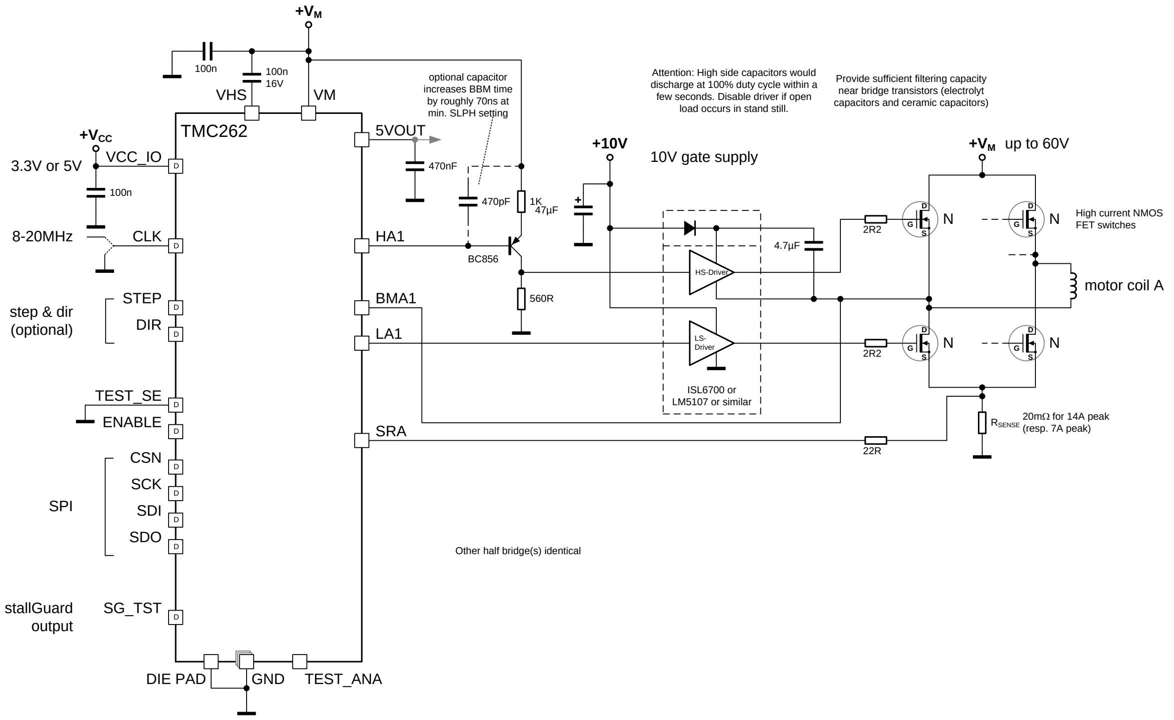


Figure 15.2 High-current power stage using external gate drivers with short to GND protection

When using high-current gate drivers, pay special attention to manufacturers' recommendations and application notes, especially concerning placement and layout of the circuit and additional parts not shown in the example figures, such as capacitors for supply voltage decoupling, protection diodes required in combination with some MOSFETs, etc.

16 Layout Considerations

The PCB layout is critical to good performance, because the environment includes both high-sensitivity analog signals and high-current motor drive signals.

16.1 Sense Resistors

The sense resistors are susceptible to ground differences and ground ripple voltage, as the microstep current steps result in voltages down to 0.5mV. No current other than the sense resistor currents should flow through their connections to ground. Place the sense resistors close to the power MOSFETs with one or more vias to the ground plane for each sense resistor.

The sense resistor layout is also sensitive to coupling between the axes. The two sense resistors should not share a common ground connection trace or vias, because PCB traces have some resistance.

16.2 Exposed Die Pad

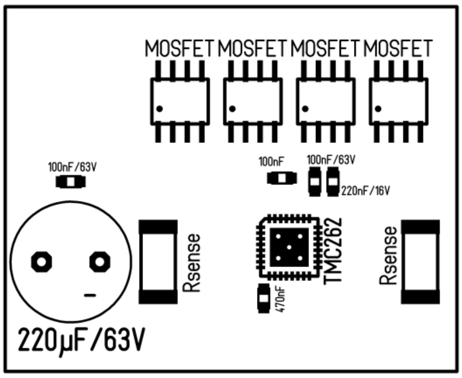
The exposed die pad and all GND pins must be connected to a solid ground plane spreading heat into the board and providing for a stable GND reference. All signals of the TMC262 are referenced to GND. Directly connect all GND pins to a common ground area.

16.3 Power Filtering

The 470nF ceramic filtering capacitor on 5VOUT should be placed as close as possible to the 5VOUT pin, with its GND return going directly to the nearest GND pin. Use as short and as thick connections as possible. A 100nF filtering capacitor should be placed as close as possible from the VS pin to the ground plane. The motor supply pins, VSA and VSB, should be decoupled with an electrolytic (>47 µF is recommended) capacitor and a ceramic capacitor, placed close to the device.

Take into account that the switching motor coil outputs have a high dV/dt, and thus capacitive stray into high resistive signals can occur, if the motor traces are near other traces over longer distances.

16.4 Layout Example



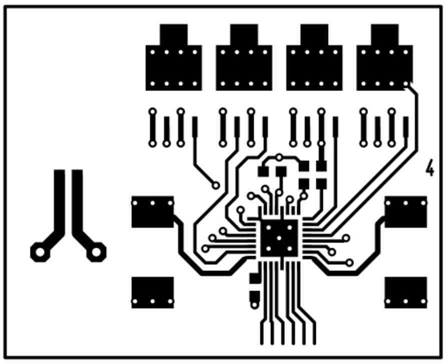
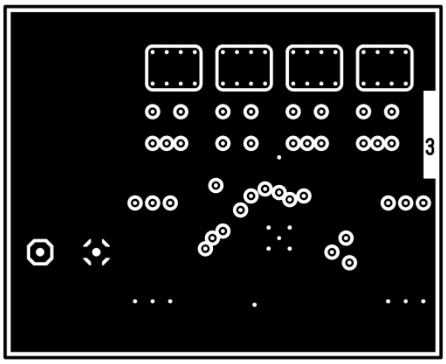
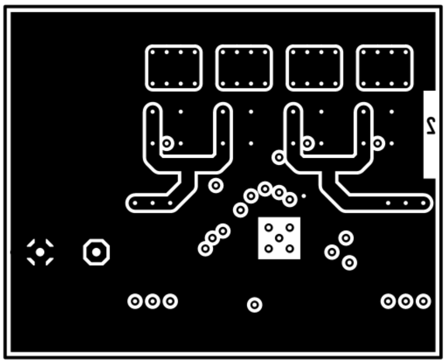
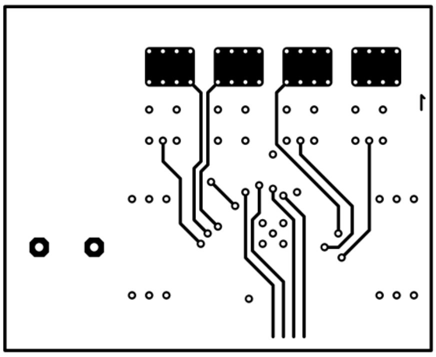
top layer (assembly side)	**inner layer**
 4	 3
inner layer	**bottom layer (solder side)**
 2	 1

Figure 16.1 Layout example

17 Absolute Maximum Ratings

The maximum ratings may not be exceeded under any circumstances. Operating the circuit at or near more than one maximum rating at a time for extended periods shall be avoided by application design.

Parameter	**Symbol**	**Min**	**Max**	**Unit**
Supply voltage	V_{VS}	-0.5	60	V
Supply and bridge voltage max. 20000s			65	V
Logic supply voltage	V_{VCC}	-0.5	6.0	V
I/O supply voltage	V_{VIO}	-0.5	6.0	V
Logic input voltage	V_I	-0.5	V_{VIO}+0.5	V
Analog input voltage	V_{IA}	-0.5	V_{CC}+0.5	V
Voltages on low-side gate driver outputs (LSx)	V_{OLS}	-0.7	V_{CC}+0.7	V
Voltages on high-side gate driver outputs (HSx)	V_{OHS}	V_{HS} -0.7	V_{VM}+0.7	V
Voltages on BM pins (BMx)	V_{IBM}	-5	V_{VM}+5	V
Relative high-side gate driver voltage (V_{VM} – V_{HS})	V_{HSVM}	-0.5	15	V
Maximum current to/from digital pins and analog low voltage I/Os	I_{IO}		+/-10	mA
Non-destructive short time peak current into input/output pins	I_{IO}		500	mA
5V regulator output current	I_{5VOUT}		50	mA
5V regulator peak power dissipation (V_{VM}-5V) * I_{5VOUT}	P_{5VOUT}		1	W
Junction temperature	T_J	-50	150	°C
Storage temperature	T_{STG}	-55	150	°C
ESD-Protection (Human body model, HBM), in application	V_{ESDAP}		1	kV
ESD-Protection (Human body model, HBM), device handling	V_{ESDDH}		300	V

18 Electrical Characteristics

18.1 Operational Range

Parameter	**Symbol**	**Min**	**Max**	**Unit**
Junction temperature	T_J	-40	125	°C
Supply voltage TMC261	V_{VS}	9	59	V
I/O supply voltage	V_{VIO}	3.00	5.25	V

18.2 DC and AC Specifications

DC characteristics contain the spread of values guaranteed within the specified supply voltage range unless otherwise specified. Typical values represent the average value of all parts measured at +25°C. Temperature variation also causes some values to stray. A device with typical values will not leave Min/Max range within the full temperature range.

Power Supply Current	**DC Characteristics** V_{VS} = 24.0V					
Parameter	**Symbol**	**Conditions**	**Min**	**Typ**	**Max**	**Unit**
Supply current, operating	I_{VS}	f_{CLK}=16MHz, 40kHz chopper, Q_G=10nC		12		mA
Supply current, MOSFETs off	I_{VS}	f_{CLK}=16MHz		10		mA
Supply current, MOSFETs off, dependency on CLK frequency	I_{VS}	f_{CLK} variable *additional to* I_{VS0}		0.32		mA/ MHz
Static supply current	I_{VS0}	f_{CLK}=0Hz, digital inputs at +5V or GND		3.2	4	mA
Part of supply current NOT consumed from 5V supply	I_{VSHV}	MOSFETs off		1.2		mA
IO supply current	I_{VIO}	No load on outputs, inputs at V_{IO} or GND		0.3		µA

NMOS Low-Side Driver	**DC Characteristics** V_{LSX} = 2.5V, slope setting controlled by SLPL					
Parameter	**Symbol**	**Conditions**	**Min**	**Typ**	**Max**	**Unit**
Gate drive current LSx low-side switch ON [a)]	I_{LSON}	SLPL=%00/%01		12		mA
Gate drive current LSx low-side switch ON [a)]	I_{LSON}	SLPL=%10		21		mA
Gate drive current LSx low-side switch ON [a)]	I_{LSON}	SLPL=%11	20	31	50	mA
Gate drive current LSx low-side switch OFF [a)]	I_{LSOFF}	SLPL=%00/%01		-13		mA
Gate drive current LSx low-side switch OFF [a)]	I_{LSOFF}	SLPL=%10		-25		mA
Gate drive current LSx low-side switch OFF [a)]	I_{LSOFF}	SLPL=%11	-25	-37	-60	mA
Gate off detector threshold	V_{GOD}	V_{LSX} falling		1		V
Q_{GD} protection resistance after detection of gate off	$R_{LSOFFQGD}$	SLPL=%11 V_{LSX} = 1V		26	50	Ω
Driver active output voltage	V_{LSON}			V_{VCC}		V

Notes:

a) Low-side drivers behave similar to a constant-current source between 0V and 2.5V (switching on) and between 2.5V and 5V (switching off), because switching MOSFETs go into saturation. At 2.5V, the output current is about 85% of peak value. This is the value specified.

PMOS High-Side Driver	**DC Characteristics** V_{VS} = 24.0V, V_{VS} - V_{HSX} = 2.5V, slope setting controlled by SLPH					
Parameter	**Symbol**	**Conditions**	**Min**	**Typ**	**Max**	**Unit**
Gate drive current HSx high-side switch ON [b)]	I_{HSON}	SLPH=%00/%01		-15		mA
Gate drive current HSx high-side switch ON [b)]	I_{HSON}	SLPH=%10		-29		mA
Gate drive current HSx high-side switch ON [b)]	I_{HSON}	SLPH=%11	-25	-42	-70	mA
Gate drive current HSx high-side switch OFF [c)]	I_{HSOFF}	SLPH=%00/%01		15		mA
Gate drive current HSx high-side switch OFF [c)]	I_{HSOFF}	SLPH=%10		29		mA
Gate drive current HSx high-side switch OFF [c)]	I_{HSOFF}	SLPH=%11	28	43	70	mA
Gate off detector threshold	V_{GOD}	V_{HSX} rising		V_{VS}-1		V
Q_{GD} protection resistance after detection of gate off	$R_{HSOFFQGD}$	SLPH=%11 V_{HSX} = V_{VS} - 1V		32	60	Ω
Driver active output voltage	V_{HSON}	I_{OUT} = 0mA	V_{VHS}+2.8	V_{VHS}+2.3	V_{VHS}+1.8	V

Notes:

b) High-side switch on drivers behave similar to a constant-current source between V_{VS} and V_{VS}–2.5V. At V_{VS}-2.5V, the output current is about 90% of peak value. This is the value specified.

c) High-side switch off drivers behave similar to a constant current source between V_{VS}-8V and V_{VS}-2.5V. At V_{VS}-2.5V, the output current is about 65% of peak value. This is the value specified.

High-Side Voltage Regulator	**DC-Characteristics** V_{VS} = 24.0V					
Parameter	**Symbol**	**Conditions**	**Min**	**Typ**	**Max**	**Unit**
Output voltage (V_{VM} – V_{HS})	V_{HSVM}	I_{OUT} = 0mA T_J = 25°C	9.3	10.0	10.8	V
Output resistance	R_{VHS}	Static load		50		Ω
Deviation of output voltage over the full temperature range	$V_{VHS(DEV)}$	T_J = full range		60	200	mV
DC Output current	I_{VHS}	(from VM to VHS)			4	mA
Current limit	I_{VHSMAX}	(from VM to VHS)		15		mA
Series regulator transistor output resistance (determines voltage drop at low supply voltages)	R_{VHSLV}			400	1000	Ω

Linear Regulator	**DC Characteristics**					
Parameter	**Symbol**	**Conditions**	**Min**	**Typ**	**Max**	**Unit**
Output voltage	V_{5VOUT}	I_{5VOUT} = 10mA T_J = 25°C	4.75	5.0	5.25	V
Output resistance	R_{5VOUT}	Static load		3		Ω
Deviation of output voltage over the full temperature range	$V_{5VOUT(DEV)}$	I_{5VOUT} = 10mA T_J = full range		30	60	mV
Output current capability (attention, do not exceed maximum ratings with DC current)	I_{5VOUT}	V_{VS} = 12V	100			mA
		V_{VS} = 8V	60			mA
		V_{VS} = 6.5V	20			mA

Clock Oscillator and CLK Input	**Timing Characteristics**					
Parameter	**Symbol**	**Conditions**	**Min**	**Typ**	**Max**	**Unit**
Clock oscillator frequency	f_{CLKOSC}	t_J=-50°C	10.0	14.3		MHz
Clock oscillator frequency	f_{CLKOSC}	t_J=50°C	10.8	15.2	20.0	MHz
Clock oscillator frequency	f_{CLKOSC}	t_J=150°C		15.4	20.3	MHz
External clock frequency (operating)	f_{CLK}		4		20	MHz
External clock high / low level time	t_{CLK}		12			ns

Detector Levels	**DC Characteristics**					
Parameter	**Symbol**	**Conditions**	**Min**	**Typ**	**Max**	**Unit**
V_{VS} undervoltage threshold	V_{UV}		6.5	8	8.5	V
Short to GND detector threshold (V_{VS} - V_{BMx})	V_{BMS2G}		1.0	1.5	2.3	V
Short to GND detector delay (low-side gate off detected to short detection)	t_{S2G}	TS2G=00	2.0	3.2	4.5	µs
		TS2G=10		1.6		µs
		TS2G=01		1.2		µs
		TS2G=11		0.8		µs
Overtemperature warning	t_{OTPW}		80	100	120	°C
Overtemperature shutdown	t_{OT}	Temperature rising	135	150	170	°C

Sense Resistor Voltage Levels	**DC Characteristics**					
Parameter	**Symbol**	**Conditions**	**Min**	**Typ**	**Max**	**Unit**
Sense input peak threshold voltage (low sensitivity)	$V_{SRTRIPL}$	VSENSE=0 Cx=248; Hyst.=0	290	310	330	mV
Sense input peak threshold voltage (high sensitivity)	$V_{SRTRIPH}$	VSENSE=1 Cx=248; Hyst.=0	153	165	180	mV

Digital Logic Levels	**DC Characteristics**					
Parameter	**Symbol**	**Conditions**	**Min**	**Typ**	**Max**	**Unit**
Input voltage low level [d)]	V_{INLO}		-0.3		0.8	V
Input voltage high level [d)]	V_{INHI}		2.4		V_{VIO}+0.3	V
Output voltage low level	V_{OUTLO}	I_{OUTLO} = 1mA			0.4	V
Output voltage high level	V_{OUTHI}	I_{OUTHI} = -1mA	0.8V_{VIO}			V
Input leakage current	I_{ILEAK}		-10		10	µA

Notes:

d) Digital inputs left within or near the transition region substantially increase power supply current by drawing power from the internal 5V regulator. Make sure that digital inputs become driven near to 0V and up to the V_{IO} I/O voltage. There are no on-chip pull-up or pull-down resistors on inputs.

19 Package Mechanical Data

19.1 Dimensional Drawings

Attention: Drawings not to scale.

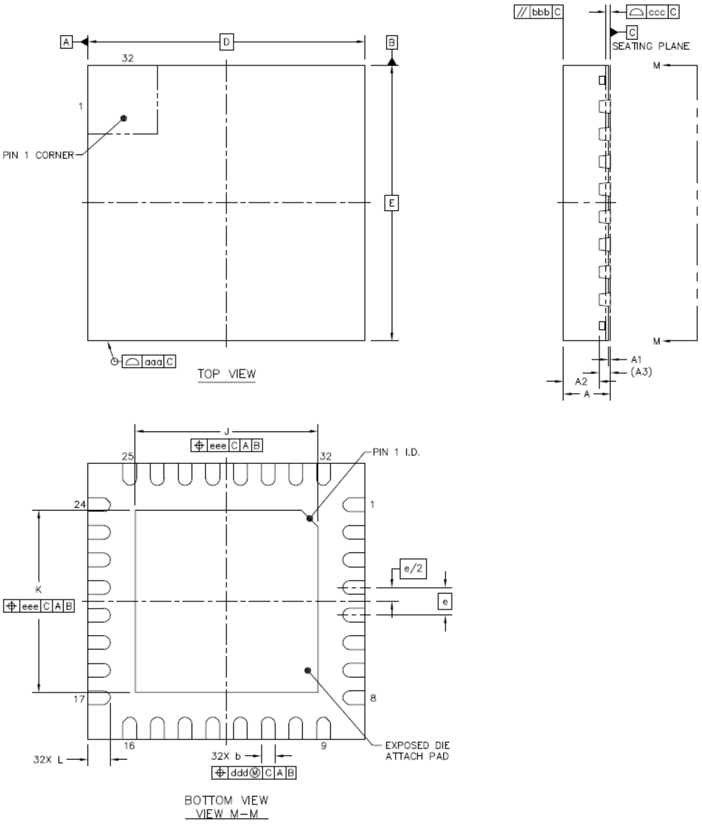


Figure 19.1 Dimensional drawings

Parameter	Ref	Min	Nom	Max
Total thickness	A	0.80	0.85	0.90
Standoff	A1	0.00	0.035	0.05
Mold thickness	A2	-	0.65	0.67
Lead frame thickness	A3		0.203	
Lead width	b	0.2	0.25	0.3
Body size X	D		5.0	
Body size Y	E		5.0	
Lead pitch	e		0.5	
Exposed die pad size X	J	3.2	3.3	3.4
Exposed die pad size Y	K	3.2	3.3	3.4
Lead length	L	0.35	0.4	0.45
Package edge tolerance	aaa			0.1
Mold flatness	bbb			0.1
Coplanarity	ccc			0.08
Lead offset	ddd			0.1
Exposed pad offset	eee			0.1

19.2 Package Code

Device	Package	Temperature range	Code/ Marking
TMC262	QFN32 (RoHS)	-40° to +125°C	TMC262-LA

20 Disclaimer

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21 ESD Sensitive Device

The TMC262 is an ESD-sensitive CMOS device and sensitive to electrostatic discharge. Take special care to use adequate grounding of personnel and machines in manual handling. After soldering the devices to the board, ESD requirements are more relaxed. Failure to do so can result in defects or decreased reliability.

Note: In a modern SMD manufacturing process, ESD voltages well below 100V are standard. A major source for ESD is hot-plugging the motor during operation. As the power MOSFETs are discrete devices, the device in fact is very rugged concerning any ESD event on the motor outputs. All other connections are typically protected due to external circuitry on the PCB.

22 Table of Figures

23 Revision History

Version	**Date**	**Author** BD = Bernhard Dwersteg SD – Sonja Dwersteg	**Description**
0.94	2010-APR-22	BD	New headline, photo, details
1.00	2010-AUG-09	BD	V2 silicon results, increased chopper thresholds (identical ratio of VCC power supply as in V1 and V1.2 silicon) VSENSE bit description corrected based on actual values
1.07	2010-NOV-22	BD	Changed optimum SG value range to 0 to 400 at max. load, lower SGT limit for best results: -10, Chapter on stall detect.
1.08	2010-DEC-01	BD	Added disclaimer, added SPI info
1.10	2011-MAR-09	BD	Corrected undervoltage threshold, chopper thresholds
1.11	2011-APR-12	BD	Slightly modified LS driver characteristics
1.12	2011-JUL-26	BD	Updated MOSFET list, typ. f_{CLKOSC} is 15MHz (old: 13MHz)
1.13	2011-OKT-05	BD	Corrected chopper illustration, new ext. driver application
1.15	2011-DEC-14	BD	Minor corrections, added layout considerations
2.00	2012-FEB-03	SD	- Amended datasheet version for TMC262 (design and wording). - Figure 5.1 new. - Application examples on second front page new.
2.01	2012-FEB-20	SD	Microstep resolution corrected (6.5.2).
2.02	2012-MAR-29	SD	- Description for CS parameter corrected (5) - New table design for signal descriptions (2.2)
2.03	2012-JUN-07	SD	- Information about power supply sequencing added (12).
2.04	2012-AUG-01	SD	- Chapter 6.4.2: table layout corrected. - Information about power supply sequencing updated.
2.05	2012-AUG-13	SD	- Figure 11.2 (undervoltage reset timing) new
2.06	2012-NOV-05	SD	Chapter 8 corrected: The low sensitivity (high sense resistor voltage, VSENSE=0) brings best and most robust current regulation, while high sensitivity (low sense resistor voltage; VSENSE=1) reduces power dissipation in the sense resistor.
2.07	2013-FEB-14	BD	- Figure 15.2 (high current power stage) corrected - Corrected electrical specs of PMOS high side driver

24 References

[TMC260]	TMC260/261 Datasheet
[TMC261]	TMC260/261 Datasheet
[TMC262-EVAL]	TMC262-EVAL Manual
[TMC32NP-PSO]	TMC32NP-PSO MOSFET Datasheet
[TMC34NP-PSO]	TMC34NP-PSO MOSFET Datasheet

Please refer to our web page http://www.trinamic.com.