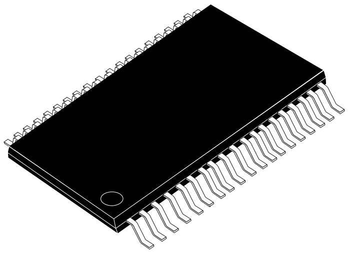
SCLT3-8BT8

Protected digital input termination with serialized state transfer

Datasheet - production data



HTSSOP-38 package

Features

- 8-input circuit in common ground low side topology
- Wide range input DC voltage V_I: -30 V to 35 V
  – On state threshold: < 11 V with R_I = 2.2 kΩ
  – Off state threshold: I_{in} > 1.5 mA or V_i > 5 V
  – Protected against -30 V reverse polarity
- 2.35 mA active current limiter with 10% tolerance
  – Drastic dissipation reduction: 78 mW max. per input
- Input digital filter with adjustable delay: 20 µs to 3 ms
- Energy-less LED visual status driver
- Input logic state transfer through a 2 MHz SPI
  – Programmable 8 / 16-bit register length
  – Multi SCLT connection in daisy chain
  – Chip temperature OTA and under voltage UVA alarms
  – Multi parity bits and power loss detection with stop bits
  – Drastic reduction of isolated coupler count and I/O of the field bus ASIC
- Power supply and input protection, R_I = 2.2 kΩ:
  – IEC 61000-4-4 transient burst: ± 4 kV minimum
  – IEC 61000-4-5 voltage surge: ± 1 kV minimum
  – IEC 61000-4-2 ESD: ± 8 kV in contact: ± 15 kV in air minimum
- Wide range power supply voltage V_C:
  – + 9 V to + 35 V with 10 mA output current
  – Protected against -30 V reverse polarity

Applications

- Digital inputs for programmable logic controller and decentralized I/O modules
- Digital input with serialized state transfer
- Enabling digital inputs to meet type 1 and 3 characteristics of IEC 61131-2
- EN60947-5-2 2-wire proximity sensor compatibility

Description

The SCLT3-8BT8 provides an 8-line protected digital input termination with serialized state transfer. This device enhances the I/O module density by cutting the dissipation (78 mW per input) and reducing the count of opto-transistors. An adjustable digital filter and an LED driver are embedded in each type 3 input section. Its 2 MHz SPI peripheral output serializes the input state transfer to the I/O module controller.

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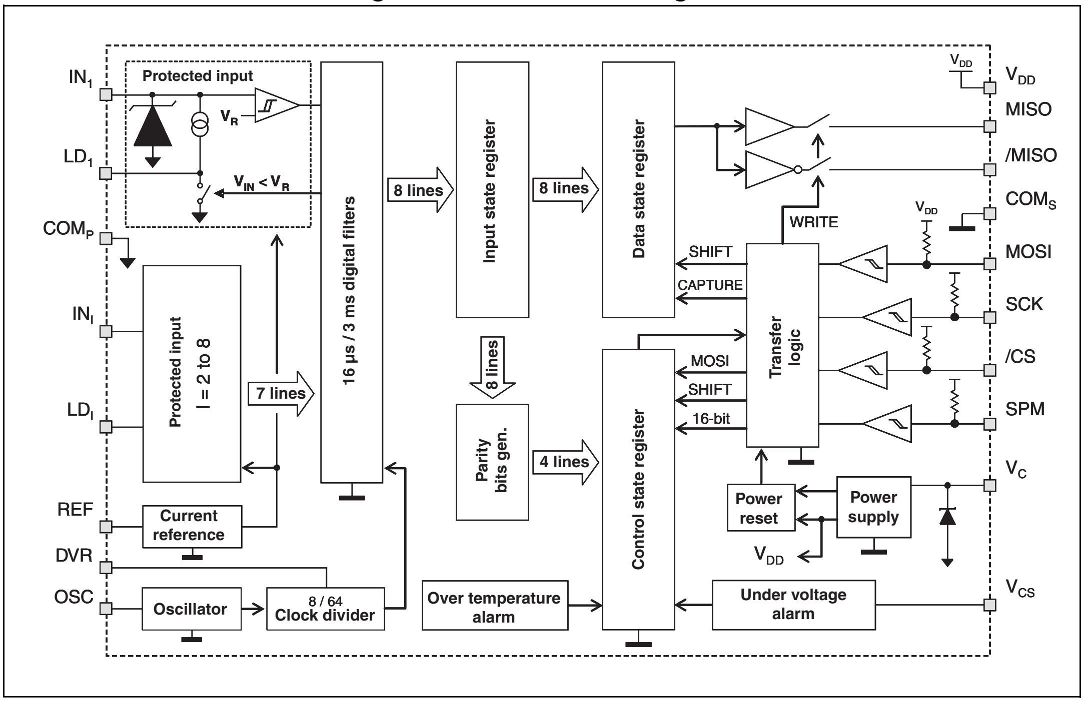
Contents

1 Circuit block diagram

Figure 1. Circuit block diagram



1.1 I/O pin descriptions

Table 1. I/O pin descriptions

Name	Type	Description	Pin #
IN_I	Power input	Logic input with a current regulation behavior, I = 1 to 8	8 to 11, 13 to 16
LD_I	Power output	LED output driver with a current regulation behavior, I = 1 to 8	20 to 27
V_C	Power input	24 V sensor power supply	5
V_{CS}	Signal input	24 V sensor power supply sensing input	6
COM_P	Ground	Power ground of power sensor supply	4, 7, 12, 17
V_{DD}	Power output	5 V logic power supply	38
COM_S	Ground	Signal ground of logic / output section	30
REF	Signal input	Input current limiter reference setting	29
DVR	Logic input	Divider ratio selector of the digital input filters (8 or 64 steps)	1
OSC	Signal input	Delay setting of the digital input filters	2
SPM	Signal input	SPI shift register length selector (8 or 16 bits)	3
/CS	Logic input	SPI chip Select signal	35
SCK	Logic input	SPI serial clock signal	34
MOSI	Logic output	SPI serial data input signal	33
/MISO	Logic output	Inverting SPI serial data output signal	32
MISO	Logic input	SPI serial data input signal	31
SUB	Substrate	Exposed pad: connected to die substrate, to connect to $COMP_P$	Exposed pad
NC		Not connected (or to be connected to COM_P)	18, 19, 28, 36, 37

Figure 2. Pinout description of the HTSSOP-38 version (top view)

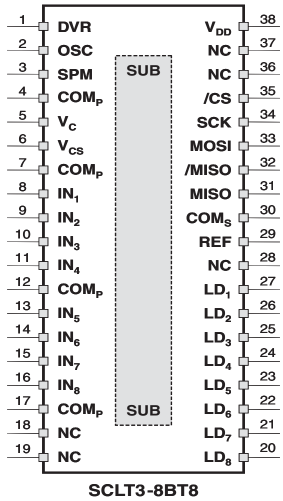


Figure 3. Basic application diagram

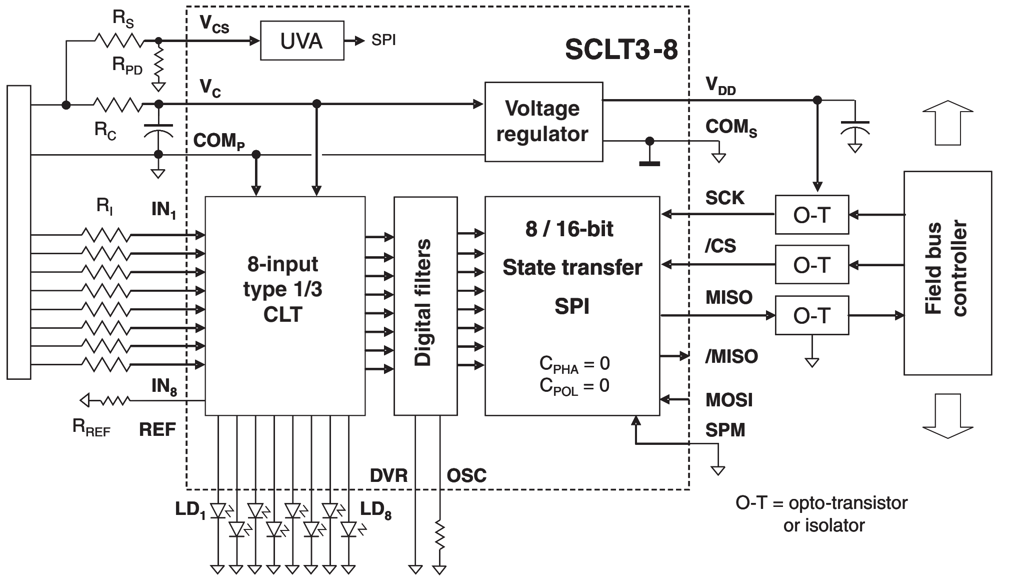
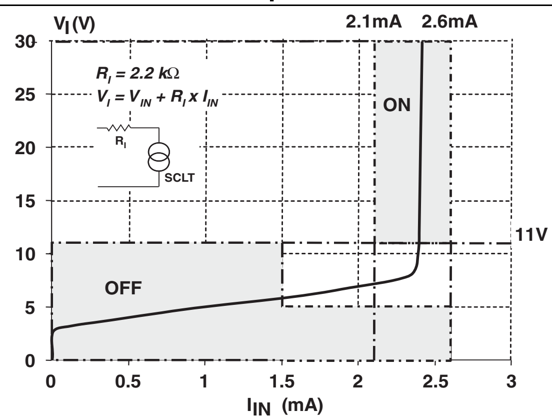


Figure 4. Basic module input characteristics in type 3



2 Functional description

2.1 Input power section

The SCLT3-8 is an 8-line input termination device designed for 24 V DC automation applications. It provides the front-end circuitry of a digital input module (I/O) in industrial automation.

Available in an eight-channel configuration, it offers a high-density termination by minimizing the conducting dissipation and the external component count.

Made of an input voltage protection, a serial current limiting circuit and an output interface, each channel circuit terminates the connection between the logic input and its associated high side sensor or switch.

The SCLT3-8 is an 8-line current limiting input array compatible with type 1 and 3 (>2 mA) characteristics of the IEC 61131-2 standard.

Each input voltage clamping block protects the module input against electromagnetic interferences such as those described in the IEC 61131-2 standard and IEC 61000-4-2 (ESD), 4-4 (transient burst), 4-5 (voltage surge) and 4-6 (conducted radio frequency interferences) standards. The supply input is also designed with such a protection structure.

The current limiting circuit connected between the IN_I and LD_I pins is set externally by a resistor R_{REF} and is compensated over the full temperature range. Thanks to its 10% tolerance, the current limitation allows drastic reduction of the input dissipation, 78 mW per channel in type 3, compared with a resistive input.

Furthermore, the SCLT3-8 is housed in a very low R_{TH} exposed pad HTSSOP surface mount package that allows the PCB cooling pad to be reduced. The overall module and printed board size become smaller and the hot spot effect is reduced.

In accordance with IEC 61131-2 standard when the input current is less than 1.5 mA, the output circuit maintains the associated output data and the visual LED in the OFF state.

When the module input voltage V_I, including the 2.2 kΩ input resistor, is higher than 11 V corresponding to a SCLT input voltage V_{IN} higher than 5 V, the output circuit puts its associated output data in ON state.

2.2 Visual input LED driver

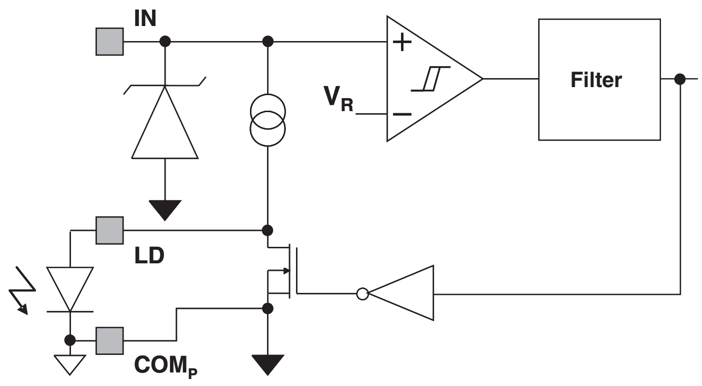
Since the inputs are indicated with an LED, as described in the IEC 61131-2 standard, an LED driver is implemented on each input power section.

This driver has two major benefits for the application. First, it takes its electrical energy directly from the input current. This energy is free being, in any case, dissipated in the SCLT. Second, it eliminates the need for extra pins on the I/O controller to manage the LED drive.

The LED will be powered when the input voltage V_I is higher than 11 V, and it is turned off when the input current is less than 1.5 mA.

The LED diodes will be driven in a low side configuration, all cathodes connected to ground. This topology naturally protects the LEDs and simplifies their wiring (8 wires plus the ground wire). When the LEDs are not used, the pins LD_I are grounded to COM_P to maintain the path of the input current.

Figure 5. Low side front-end input topology including the ESD surge protection and the LED driver



2.3 The input digital filter

A digital filter is implemented between the input state comparator and the input state register. It consists of a 2-step sampling circuit that is controlled by an oscillator as shown on *Figure 6*.

The filtering time t_{FT} is set by the external oscillator resistor and is a function of the oscillator period t_{CKF}:

$2 \times t_{CKF} < t_{FT} < 3 \times t_{CKF}$

t_{CKF} = Divider ratio x t_{OSC} (R_{OSC})

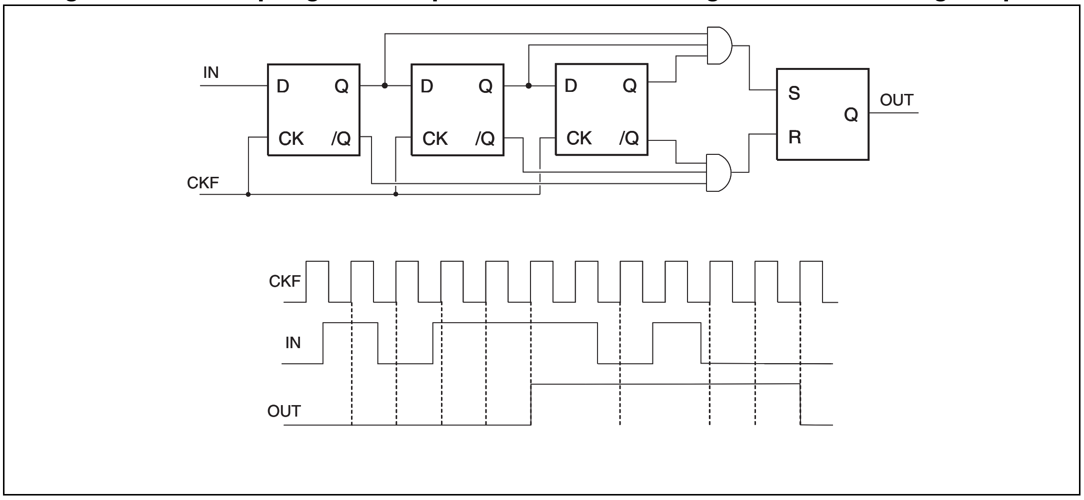
This period can be adjusted between 20 µs and 3000 µs and is compatible with the IEC 61131-2 standard as shown on *Table 2*.

Table 2. Typical setting of the digital filter timings

Input speed	Fast		Medium	Slow
Input frequency	60 kHz	20 kHz	5 kHz	300 Hz
Min. filter time t_{FT}	20 µs	50 µs	230 µs	3.0 ms
OSC resistance	51 kΩ	150 kΩ	82 kΩ	1.3 MΩ
CKF period t_{CKF}	10 µs	25 µs	115 µs	1500 µs
DVR connection	COM_S	COM_S	V_{DD}	V_{DD}
Divider ratio	8	8	64	64

Being placed in the front end of the module, this filter increases the transient immunity of the SCLT and its SPI logic circuitry. It also simplifies the input management software task of the ASIC controller.

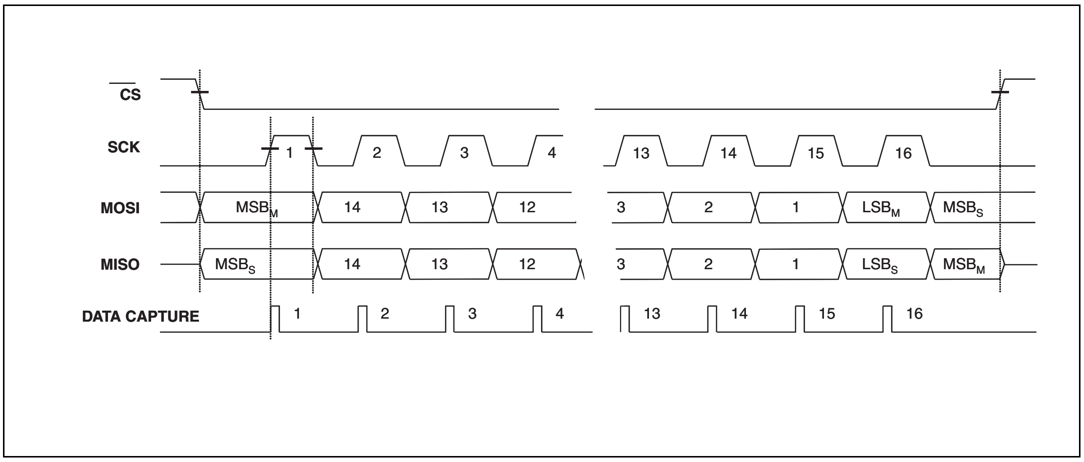
Figure 6. Two-step digital filter placed after the analog section of the logic input



2.4 Operation of the SCLT with the SPI bus

The SPI bus master controller manages the data transfer with the chip select signal /CS and controls the data shift in the register with the clock SCK signal. This data transfer operation is defined by the phase C_{PHA} and the polarity C_{POL} of the clock. The SCLT runs with an SPI master protocol mode: $C_{PHA} = 0$ and $C_{POL} = 0$.

Figure 7. Serial data format frame with a master running in $C_{PHA} = 0$ and $C_{POL} = 0$ mode



The transfer of the SCLT input state in the SPI register starts when the chip select signal /CS falls and ends when this chip select signal rises back.

The transfer of data out of the SCLT slave MISO output starts immediately when the chip select signal /CS goes low. The input MOSI is captured and presented to the shift register on each rising edge of the clock SCK. The data are shifted in this register on each falling edge of the serial clock SCK, the data bits are written on the output MISO with the most significant bit first.

During all operations, V_{DD} is held stable within the specified operating range.

2.5 SPI bus signal description

2.5.1 Chip select /CS

When the chip select signal /CS is high, the data transfer is disabled (SCK and MOSI signals are ignored) and the data output MISO is in high impedance tri-state Z.

Driving this input low enables the communication process. At each falling edge of the /CS, the 8 input logic states, and the 8 control bits are loaded into the SPI shift register.

The chip select /CS must toggle only when the serial clock signal SCK is in low state.

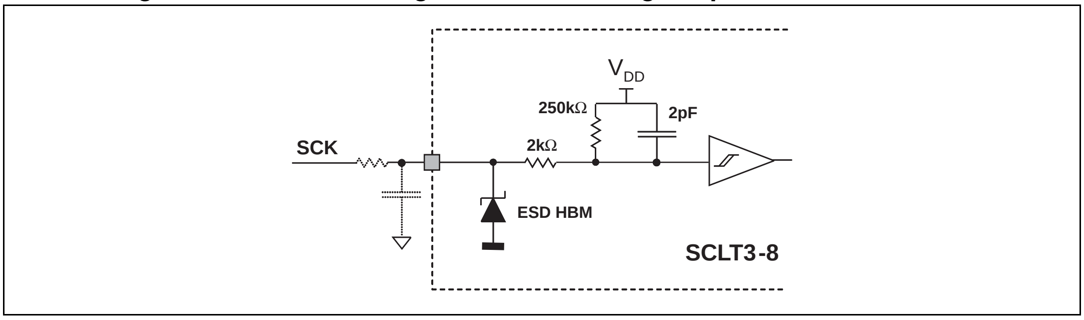
2.5.2 Serial clock SCK

This clock signal defines the speed and sequence of the SPI communication and is controlled by the master unit. Its transient edges define the serial protocol operation:

- The falling edge generates the shift of the data in the register and the last bit writing on the output MISO.
- The rising edge generates the capture of the data on the input MOSI.

The SCLT internal circuitry secures the SPI operation in mode C_{POL} = 0, C_{PHA} = 0. When the chip select /CS falls low, the first edge of the clock SCK to be active is always the rising edge.

Figure 8. Functional diagram of the SPI logic inputs SCK, MOSI, /CS



2.5.3 Serial data input MOSI

This input signal MOSI is used to shift external data bits into the SCLT register from the most significant (MSB) bit to the least significant one (LSB). The data bits are captured by the SCLT on the rising edge of the serial clock signal SCK.

Like the clock SCK, and the chip select /CS, the MOSI input circuit is filtered as shown in *Figure 8*, in order to match maximum speed operation and improve the EFT burst immunity of the SPI circuit.

2.5.4 Serial data output MISO

This output signal is used to transfer data out of the SCLT slave circuit from the most significant bit (MSB) to the least significant bit (LSB). The first data bit is written out when the chip select /CS goes low. Then the other data bits are written out on the falling edge of the clock signal SCK.

The output MISO goes to high impedance tri-state shown on *Table 5* when the /CS signal goes in high state.

2.5.5 SPI shift register operation selector SPM

The input SPM allows the operation of the SPI shift register to be configured for an 8-bit or 16-bit operation.

When SPM is set low (COM_P) the shift register runs in a 16-bit mode and transfers both the input state bits and the control bits. When SPM is set high (V_{DD}) the shift register runs in an 8-bit mode and transfers the eight input state bits in a faster transfer process.

This SPM input can be changed, and the SPI operation modified, only when the chip select /CS is high (no communication).

2.6 SPI data transfer operation

2.6.1 SPI data frame

The selected structure of the SPI is a 16-bit word in order to be able to implement the input state data and some control bits, such as the UVA alarm, the 4 parity bits and the two low and high state stop bits.

2.6.2 SPI data transfer

The SCLT transfers its 16 data bits through the SPI within one chip select Hi-Lo-Hi sequence. So, this length defines the minimum length that the shift register of the SPI master controller is able to capture 16 bits.

Table 3 shows the 16-bit mode in which the data are transferred starting from the data bits, the control bits and ending with a stop bit.

Table 3. SPI data transfer organization versus SCLT input states with SPM = 0

Bit #	LSB	Bit 1	Bit 2	Bit 3	Bit 4	Bit 5	Bit 6	Bit 7
Control	High	Low	PC4	PC3	PC2	PC1	/OTA	/UVA
	Last out							
Bit #	**Bit 8**	**Bit 9**	**Bit 10**	**Bit 11**	**Bit 12**	**Bit 13**	**Bit 14**	**MSB**
Data	IN 1	IN 2	IN 3	IN 4	IN 5	IN 6	IN 7	IN 8
								First out

Table 4. SPI data transfer organization versus CLT input states with SPM = 1

Bit #	Bit 8	Bit 9	Bit 10	Bit 11	Bit 12	Bit 13	Bit 14	MSB
Data	IN 1	IN 2	IN 3	IN 4	IN 5	IN 6	IN 7	IN 8
	Last out							First out

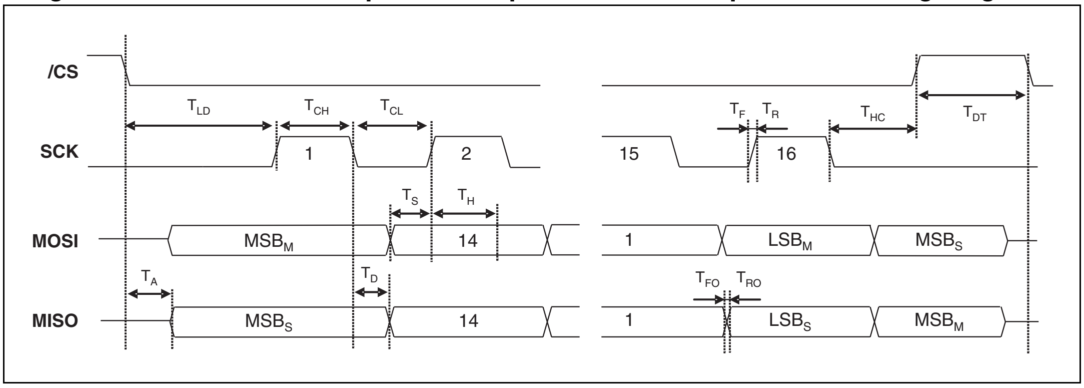
2.6.3 SPI transfer speed

The speed of the SPI is defined by the clock frequency and the data frame transfer time. In the SCLT application the transfer time correspond to the input scanning time programmed by the I/O controller.

In a 16-bit mode this scanning time should be less than 500 µs for a 64-input module (128 bits to transfer) where it should be about 160 µs for a 16-input module (32 bits to transfer).

To obtain such scanning with the data frame structure, the clock frequency is set respectively at 256 kHz and 200 kHz.

Figure 9. SCLT slave unit operation, input MOSI and output MISO timing diagrams



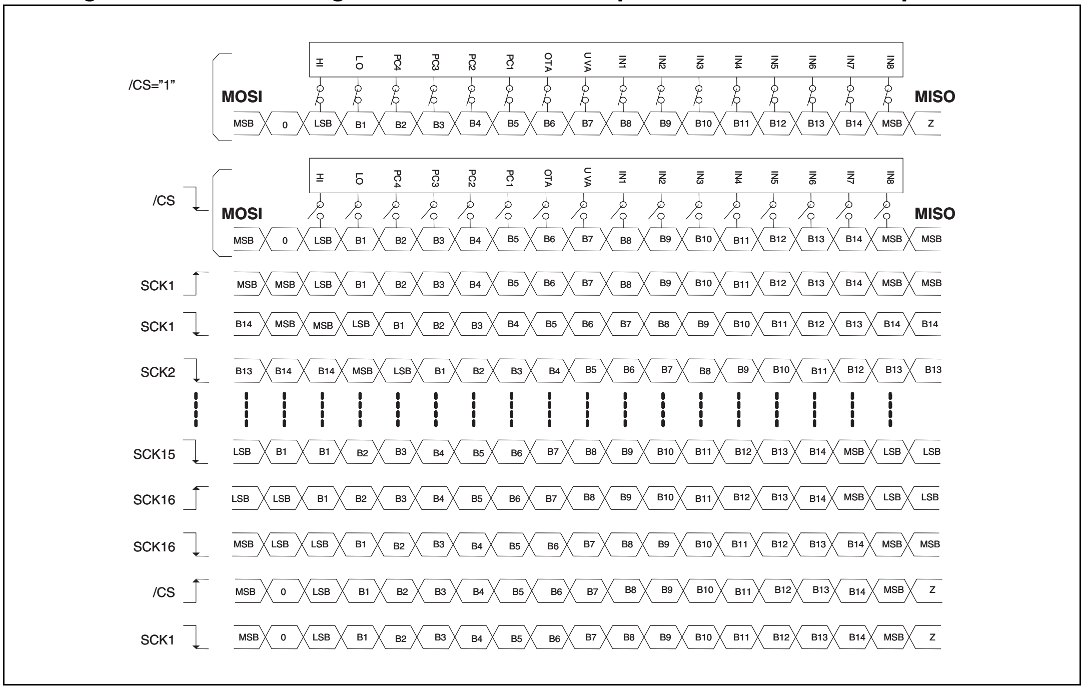
The clock frequency is limited by the application requirements to secure the immunity of the SPI section against fast transient disturbances and keep the isolator consumption low enough.

The SCLT maximum SPI clock frequency is 2 MHz.

- The minimum SPI clock period is also defined by the capability of the SCLT to capture data on MOSI and to write out data on MISO as shown in *Table 9*.
  - Capture rule: $t_{CH} > t_H$
  - Write out rule: $t_D + t_S < t_{CL} = t_C - t_{CH}$
- At the start of the transfer sequence the first rising edge of the clock SCK should occur after the data writing on the SPI output MISO corresponding with the propagation time t_A, avoiding missing the first data: $t_{LD} > t_A + t_S$

In between two transfer sequences the output driver of the SPI circuit should go in high impedance before any new transfer operation so falling edge of the chip select /CS: $t_{DIS} < t_{DT}$.

Figure 10. SPI shift register data transfer sequence versus SCLT input states



2.7 Control bit signals of the SPI transferred data frame

2.7.1 Power bus voltage monitoring

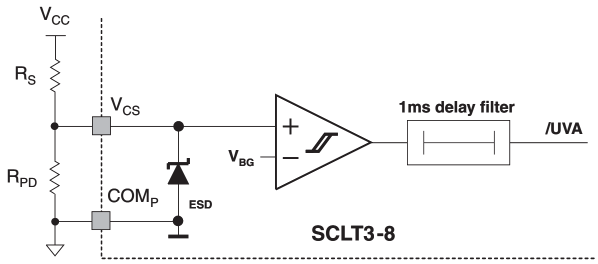
The UVA circuit generates the alarm /UVA that is active low when the power bus voltage is lower than the activation threshold V_{CON}, 17 V typical, and it is disabled high when the power bus voltage rises above the threshold V_{COFF}, 18 V typical as shown in *Figure 12*.

The UVA circuit is robust enough to resist ESD and EFT effects, and a filter is added to avoid drop out effects. The analog level can be adjusted externally with a pull down resistor.

The power bus voltage is sensed from a separate sensing pin V_{CS}. The overall accuracy is about 15% and the alarm circuit should be insensitive to drop out of less than 1 ms.

The under voltage detection does not lead to the SCLT internal shutdown but generates an alarm /UVA that is transmitted through the SPI on control bit #7.

Figure 11. UVA circuit block diagram



The power supply diagnostics help to determine if the input state is really low or if some power bus failure is damaging the quality of this state signal.

2.7.2 Over temperature alarm

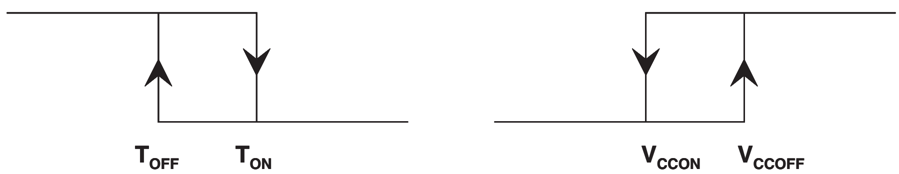
A temperature sensor, equivalent to a diode drop voltage, is placed on the power section of the SCLT in order to sense its operating junction temperature.

This protection allows abnormal temperature cases to be detected. The input reverse polarity generates higher current in the inputs, more than twice that shown in the application section, and a maintenance action allows the overall system and functional reliability to be improved.

The alarm signal /OTA is enabled, low state active, when the junction temperature is higher than the activation threshold T_{ON}, 150 °C typical, and it is disabled when the junction temperature falls below the threshold $T_{OFF,}$ 135 °C typical as shown in *Figure 12*.

The over temperature detection does not lead to the SCLT internal shutdown but generates an alarm OTA that is transmitted through the SPI on control bit #6. So, it is up to the I/O controller to launch the appropriate action on the system to reduce the constraint in the I/O module.

Figure 12. Logic behavior of the OTA and UVA alarm control bits



2.7.3 Parity checksum bits calculation and transfer

The aim of the parity checksum bit is to detect one error in the transferred SPI word. Several parity checksum bits are generated and transmitted through the SPI on the control bit #2 to #5.

Transmission errors can occur because of the ESD / surge effects or the indirect effects of EFT burst tests beyond the required levels.

It is supposed such disturbances affect one bit at a time during the SPI frame transfer. EFT burst repetition rate is about 200 µs (5 kHz) and the SPI 16-bit frame should last less than 160 µs.

A parity bit on the full byte should be obtained by applying an “exclusive NOR” Boolean operation to the eight logic input states (PC_1): it goes high when the parity of the 8 inputs is even.

The other parity bits PC2 and PC3 are obtained with an “exclusive NOR” Boolean operation respectively on the MSB half data byte (IN_5 to IN_8) and the LSB half data byte (IN1 to IN_4), and PC_4 on the middle half data byte (IN_3 to IN_6): they go high when the parity of the 4 considered inputs is even.

These parity bits allow one error to be detected at a time in the SPI data transfer, and this error can be corrected thanks to a second SPI data scan because the corrupted data bit should be statistically different between the two scan sequences.

A method is proposed to correct one corrupted input data bit. If full data byte parity bit PC_1 is wrong, the first scanned word is stored, and the SCLT input data are scanned immediately twice. Then the first full byte parity bit is checked with its half byte parity bits to confirm the error. The second scanned SPI word is stored and its full byte parity bit is also checked.

By using the parity bits on half data byte (the 4 MSB, the 4 LSB, the 4 medium bits), the corrupted input data bit couple of the two scanned SPI words can be detected and the input data byte can be re-synthesized by isolating and replacing these failing bit couples.

2.7.4 SPI hardware interface

All the logic level output signals deliver 80% of V_{DD} for high state and 20% V_{DD} for low state.

This SPI circuit is designed to drive CMOS circuit or isolated opto-transistors. Since the clock frequency is always higher than 100 kHz, high speed opto-transistors are selected requiring higher driving input and output currents.

The biasing resistors of their output transistors are kept external to allow the speed and the device sourcing to be set for each application, providing thus more flexibility in the choice of these isolators.

In *Section 3: Application considerations*, several cases are proposed for the major applications.

2.7.5 Loss of V_{CC} power supply

The operation of the SCLT is extended beyond the levels required in the IEC 61131-2 standard to allow the implementation of the under voltage alarm UVA as described in *Section 2.7.1*.

If there is no more power feeding on the V_{CC} input, the SCLT chip goes to sleep mode, and the MISO output is forced in low state during SPI transfer attempt. The last SPI control data bit is a stop bit placed normally in high state. The loss of power supply is detected by checking its state. If low, the output is disabled by the internal power reset POR.

This POR signal is active in low state when V_C is less than 9 V or the internal power supply V_{DD} is less than 3.25 V.

Table 5. Logic state of the SPI output versus the power loss signal POR and the SPI chip select /CS

POR	/CS	MISO	/MISO	SPI status
1	1	Z	Z	Normal with no communication
1	0	1	0	Normal with communication
1	0	0	1	Normal with communication
0	1	Z	Z	Power loss with no communication
0	0	0	1	Power loss with communication attempt

Figure 13. Logic status of the SCLT power supply

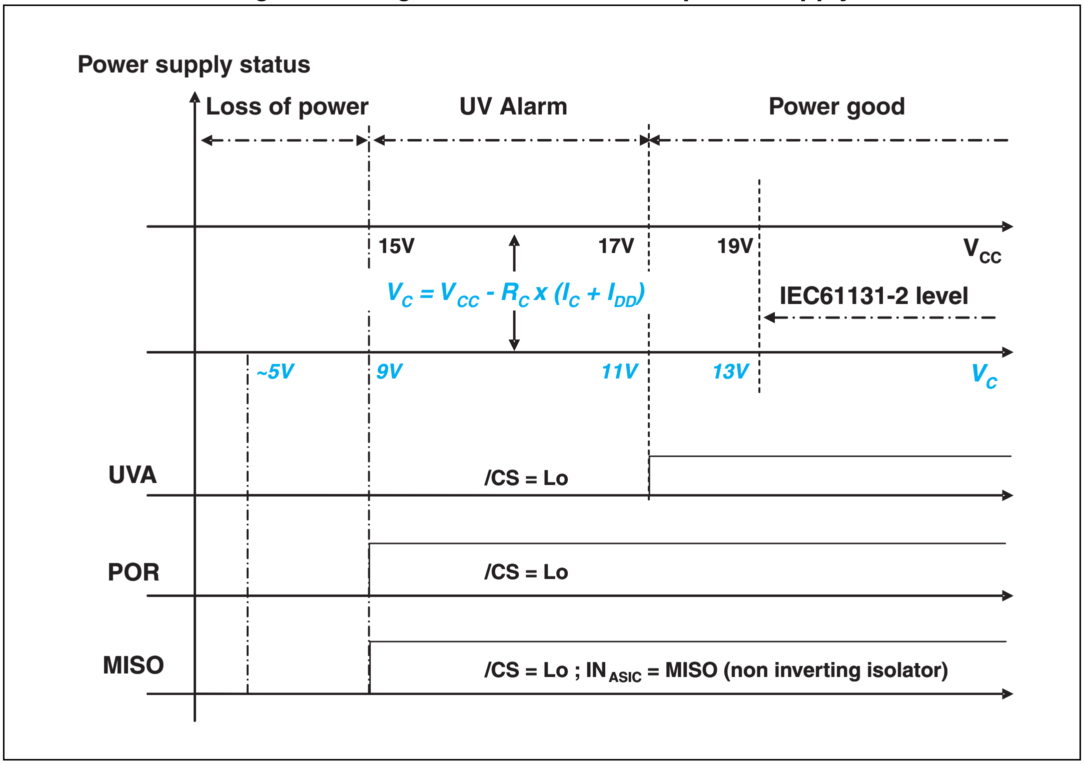


Table 6. Absolute ratings

Symbol	Pin	Parameter name and conditions	Value	Unit
V_{CC}	V_C	Bus power supply DC voltage, 500 Ω < R_C < 2.2 kΩ	- 0.3 to 35	V
V_C	V_C	SCLT power supply voltage, R_C = 0 kΩ	- 0.3 to 30	V
I_{CC}	V_C	Maximum bus power supply current	15	mA
V_{CS}	V_{CS}	Sensing bus power supply voltage	- 0.3 to 6	V
V_{DD}	V_{DD}	Internal logic power supply voltage	-0.3 to 6	V
I_{DD}	V_{DD}	Maximum logic power supply current	12	mA
V_{IN}	IN_I	Input steady state voltage, R_I = 0 Ω, I = 1 to 8	- 0.3 to 30	V
I_{IN}	IN_I	Input forward and reverse current range, R_I = 2.2 kΩ	-20 to +10	mA
LV_O	MISO /MISO	Logic output voltage	-0.3 to 6	V
LV_I	SCK /CS MOSI	Logic input voltage	-0.3 to 6	V
V_{LD}	LD_I	Maximum LED output voltage, I = 1 to 8	3	V
I_{REF}	REF	Maximum sourced reference current	300	µA
I_{OSC}	OSC	Maximum sourced oscillator current	120	µA
P_{DIS}	All	Maximum dissipation at T_{AMB}= 85 °C	850	mW
T_J	All	Storage junction temperature	- 40 to 150	°C

Table 7. Thermal resistance

Symbol	Parameter name and conditions	Value	Unit
$R_{TH(j-a)}$	Thermal resistance junction to ambient Copper thickness= 35 µm, printed board copper surface S = 1 cm^2	80	°C/W

Table 8. Operating conditions

Symbol	Pin	Parameter name and conditions	Value	Unit
V_{CC}	V_C	Bus power supply steady state voltage, $R_C > 500\ \Omega$	15 to 35	V
V_C	V_C	SCLT power supply voltage range	9 to 30	V
V_{CS}	V_{CS}	Sensing bus power supply voltage, $R_S = 1.5\ M\Omega$	0 to 5	V
V_{DD}	V_{DD}	Internal logic power supply voltage	5	V
I_{DD}	V_{DD}	Maximum logic power supply current, $R_C = 500\ \Omega$	10	mA
V_I	IN_I	Input repetitive steady state voltage, $R_I > 1.8\ k\Omega$(1)	- 30 to 35	V
R_{REF}	REF	Current limiter reference resistance range	4.7 to 18	kΩ
R_{osc}	OSC	Filter oscillator resistance range	15 k to 1.5 M	Ω
$F_{IN\ MAX}$		Maximum single input frequency	20	kHz
F_{SCK}	SCK	SPI clock frequency range	0.1 to 2	MHz
t_C	SCK	Clock period range	0.5 to 10	µs
t_{CH}	SCK	Minimum clock active width	0.25	ns
DC_{CH}	SCK	Clock duty cycle	50	%
t_R, t_F	SCK, /CS, MOSI	Minimum logic inputs rise and fall times	50	ns
LV_I		Logic input voltage	0 to 5.5	V
V_{LD}	LD_I	Maximum LED output voltage, I = 1 to 8	2.7	V
T_{AMB}	ALL	Operating ambient temperature range	- 40 to 85	°C
T_j		Operating junction temperature range	- 40 to 150	°C

1. $V_I = V_{IN} + R_I \times I_{IN}$, I = 1 to 8

Table 9. DC electrical characteristics(1)

Symbol	Pin	Name	Conditions	Min.	Typ.	Max.	Unit
Input current limitation							
I_{LIM}	IN	Input limiting current	V_{IN} = 5.5 to 26 V V_{CC} = 19 V to 30 V T_{AMB} = -40 to + 85 °C	2.1	2.35	2.6	mA
V_{LOW}	IN	Low current input voltage	I_{IN} = 100 µA, R_I = 0 Ω	-	2.6	3	V
$V_{LIM\ TH}$	IN	Current limiter activation voltage	I_{IN} = 95% x I_{LIM_TYP}(2)	-	8.5	-	V
Input and supply protection							
V_{CL}	IN, V_C	Clamping voltage	I_{IN}= 7 mA, t_P=1 ms, R_{REF} open	32.0	38.8	46.0	V
Input state operation							
V_{ON}	IN	On state input voltage	T_{AMB} = -40 to + 85 °C(3) I_{in} = I_{off} = 1.5 A	5	-	-	V
V_{TH_ON}	IN	Input on state threshold	R_I = 2.2 kΩ, OFF to ON	4.5	4.75	5	V
V_{TH_OFF}	IN	Input off state threshold	R_I = 2.2 kΩ, ON to OFF	3.5	3.75	4	V
V_{OFF}	IN	Maximum Off state voltage	T_{AMB} = -40 to + 85 °C(4)	2.9	3	3.4	V
I_{ON}	LD_I	On state LED current	V_I = 11 V	2.0	2.25	2.6	mA
Input digital filter							
t_{OSC}	OSC	Oscillator period	R_{OSC} = 51 kΩ	1.17	1.25	1.33	µs
			R_{OSC} = 1200 kΩ	22	25	27	µs
R_{OSC}	OSC	Oscillator resistance		51		1200	kΩ
t_{CKF}	-	CKF period	DVR = V_{DD}	64 x t_{OSC}			
			DVR = COM_S	8 x t_{OSC}			
t_{FT}	IN	Filtering time		2xt_{CKF}		3xt_{CKF}	
Power supply circuit							
V_{RSON}	V_C	Power on supply voltage	T_{AMB} = - 40 to + 85 °C	8	8.5	9	V
V_{RSOFF}	V_C	Power off supply voltage	T_{AMB} = - 40 to + 85 °C	7.5	8.1	8.5	V
I_C	V_C	Supply current	V_{CC} = 30 V, V_{DD}, MISO, /MISO open	1.2	1.6	2.3	mA
V_{DD}	V_{DD}	Internal supply voltage	I_{DD}= 10 mA, C_{DD} = 33 nF, R_C = 500 Ω, T_{AMB} = - 40 to + 85 °C	4.5	5	5.5	V
		Internal supply voltage	I_{DD}= 4 mA, C_{DD} = 33 nF T_{AMB} = - 40 to + 85 °C	4.75	5	5.25	V

Table 9. DC electrical characteristics(1) (continued)

Symbol	Pin	Name	Conditions	Min.	Typ.	Max.	Unit
Over temperature alarm							
T_{ON}	IN	Thermal alarm activation		-	148	-	°C
T_{OFF}	IN	Thermal alarm release		-	135	-	°C
Under voltage alarm							
V_{CON}	V_{CC}	Power voltage alarm	R_S =1.5 MΩ, R_{PD} =120 kΩ	16	17	18	V
$\Delta V_{OFF\text{-}ON}$	V_{CC}	Voltage release hysteresis		-	1	-	V
V_{BG}	V_{CS}	Input activation voltage		1.25	1.27	1.30	V
V_{HY}	V_{CS}	Input hysteresis voltage		-	0.1	-	V
t_{D_ON}	V_{CS}	Drop out filtering time		1	1.7	-	ms

1. T_J = 25 °C, V_{CC} = 24 V, R_{REF} = 15 kΩ, R_I = 2.2 kΩ, R_C = 2.2 kΩ with reference to COM_P = COM_S voltage, unless otherwise specified.
2. $V_{LIM} = V_{IN}$ + 95% x I_{LIM} x R_I
3. Corresponding to V_I = 11 V with R_I = 2.2 kΩ.
4. Corresponding to V_I = 5 V or I_{IN} = 1.5 mA.

Table 10. SPI serial bus link electrical characteristics(1)

Symbol	Pin	Name	Conditions	Min.	Typ.	Max.	Unit
t_{LD}	SCK	Enable lead time	/CS falling to SCK rising	-	-	50	ns
t_{HC}	SCK	Clock hold time	SCK falling to /CS rising	-	-	250	ns
t_{DT}	/CS	Transfer delay time	/CS rising to /CS falling	-	500	-	ns
C_{IN}	SCK, /CS, MOSI	Input capacitance		-	10	-	pF
t_{RC}	SCK, /CS, MOSI	Input filter time constant	Referred to V_{DD}	-	4	-	ns
I_{IN}	SCK, /CS, MOSI	Input pull up current	LV_I = 0 V	15	22	30	µA
t_S	MOSI	Data setup time	MOSI toggling to SCK rising	-	-	25	ns
t_H	MOSI	Data hold time	SCK rising to MOSI toggling	-	-	25	ns
LV_{IH}	MOSI	Logic input high voltage	Share of V_{DD}	-	-	70	%
LV_{IL}	SCK, /CS	Logic input low voltage	Share of V_{DD}	30	-	-	%
LV_{OH}	/MISO MISO	Logic output high voltage	I_{OH} = 3 mA	4	4.5	-	V
LV_{OL}	/MISO MISO	Logic output low voltage	I_{OH} = 3 mA	-	0.45	1	V
t_D	/MISO MISO	Write out propagation time	SCK falling to MISO toggling, C_O = 15 pF	-	35	50	ns
t_{RO}, t_{FO}	/MISO MISO	MISO signal fall/rise time	I_{MISO} = 3 mA	-	20	50	ns
			C_O = 15 pF	-	20	50	ns
t_A	MISO	Output access time	/CS falling to MISO toggling	-	55	80	ns

1. T_J = 25 °C, V_{CC} = 24 V, V_{DD} = 5 V with respect to COM_S ground pin, unless otherwise specified.

Table 11. Electromagnetic compatibility ratings(1)

Symbol	Node	Parameter name and conditions	Value	Unit
V_{PPB}	V_I	Burst Peak Pulse Voltage: IEC 61000-4-4 class 3 C_C = 33 nF, C_I = 22 nF, F= 5 kHz, test criteria A ((2) and (3))	± 2.5	kV
		Burst Peak Pulse Voltage: IEC 61000-4-4 class 4 C_C = 33 nF, C_I = 22 nF, F= 5 kHz, test criteria A(2)	±4	
V_{PP}	V_I	Surge Peak Pulse Voltage: IEC 61000-4-5 class 3 R = 42 Ω, test criteria B(2)	±1	kV
V_{PP}	V_{CC}	Surge Peak Pulse Voltage: IEC 61000-4-5 class 3, R = 2 Ω, R_C = 2.2 kΩ(2)	± 2.5	kV
		Surge Peak Pulse Voltage: IEC 61000-4-5 class 3, R = 2 Ω, R_C = 500 Ω(2)	±1	
V_{ESD}	IN	ESD protection, IEC 61000-4-2 class 4, in air Per input to ground, test criteria B	±15	kV
		ESD protection, IEC 61000-4-2 class 4, in contact Per input to ground COM_P, test criteria B	± 8	
V_{ESD}	V_{CC}	ESD protection, IEC 61000-4-2 class 4, in air Test criteria B, C_C = 33 nF, R_C = 500 Ω	±15	kV
		ESD protection, IEC 61000-4-2 class 4, in contact Test criteria B, C_C = 33 nF, R_C = 500 Ω	± 8	

1. T_J = 25 °C, R_I = 2.2 kΩ unless otherwise specified.
2. Respect to ground COM_P. Test according to standard with schematic described in application section.
3. Fully functional without any SPI data correction.

Figure 14. Typical limiting current I_{LIM} versus reference resistance R_{REF}

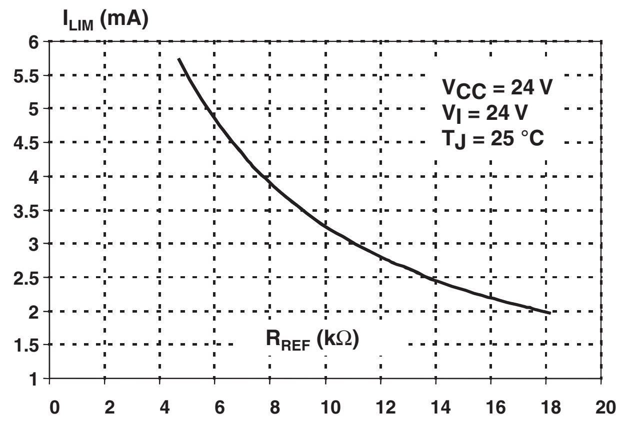


Figure 15. Typical limiting current I_{LIM} versus junction temperature T_J

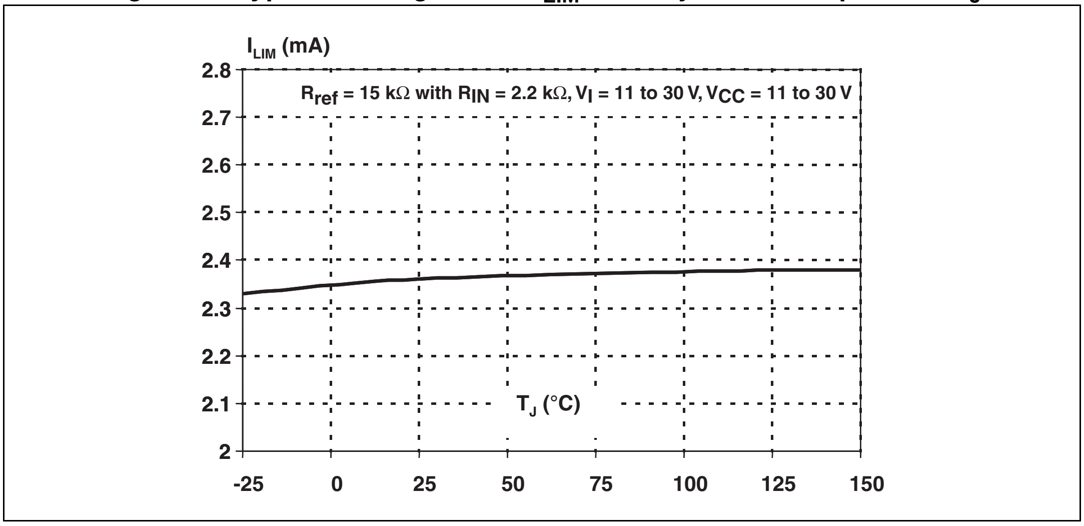
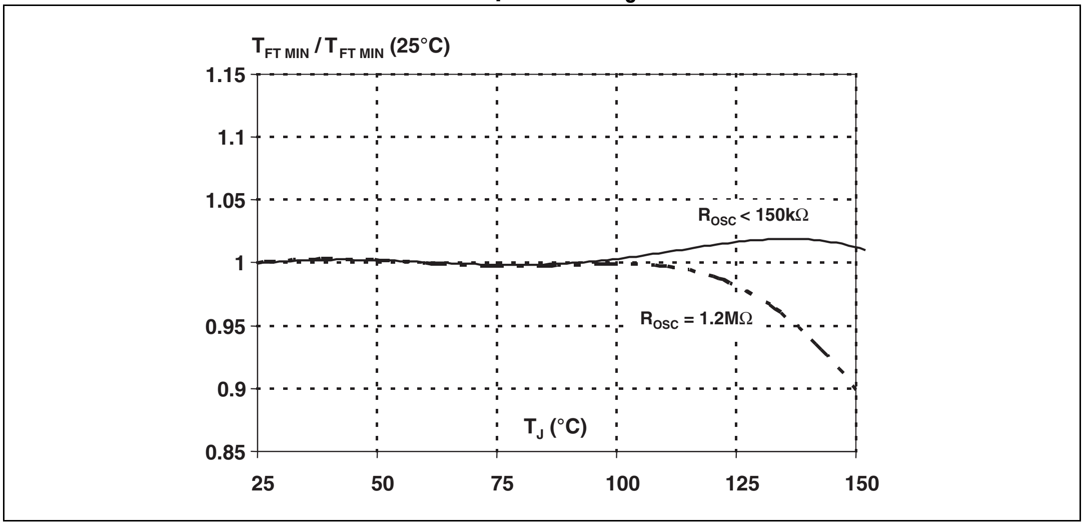


Figure 16. Relative variation of minimum filter time $T_{FT\ MIN}$ versus junction temperature T_J



3 Application considerations

3.1 SCLT serial link configurations

As long as /CS is low, a slave is able to transmit data bits whatever the length of the data frames. This feature allows several SCLT circuits to be connected in a daisy chain configuration.

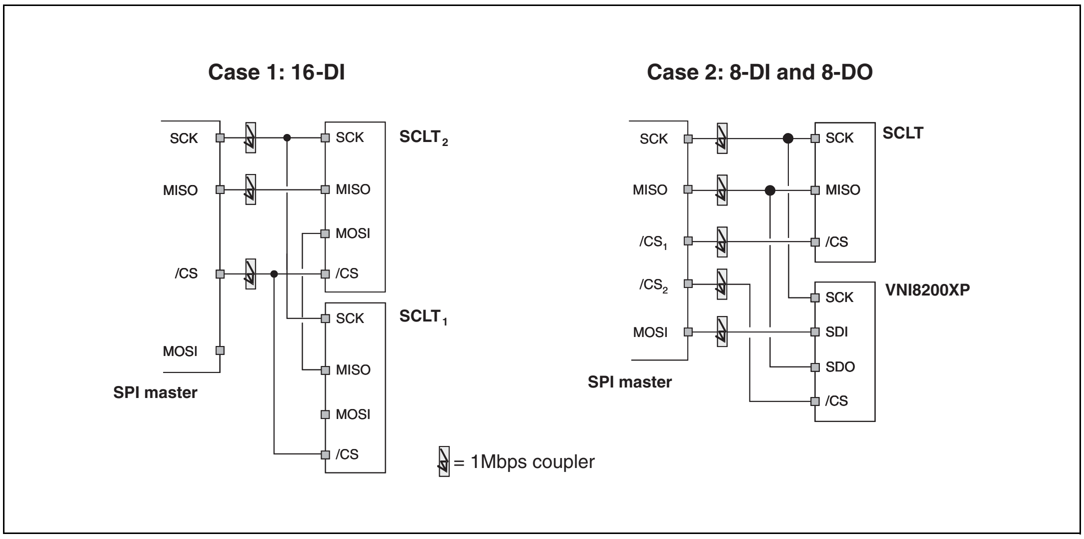
In the daisy chain configuration with several SCLT circuits (N) all the circuits are addressed by the same chip select and receive the clock signals from the same clock. They all work synchronously.

The SPI output MISO of the previous $SCLT_{P-1}$ device is connected to the SPI input MOSI of the next $SCLT_P$ device and the output MISO of the last $SCLT_N$ is connected to the MISO input of the master. The MOSI of the first $SCLT_1$ can be kept open or grounded.

So, the SPI master reads the whole chain of N 16-bit words starting with the word of the last $SCLT_N$ and ending with the word of the first $SCLT_1$.

Detailed considerations on SPI operation and daisy chain configurations are also described in ST application notes AN2846 and AN3031.

Figure 17. SCLT connection to opto-couplers, bus controller SPI master, and output driver

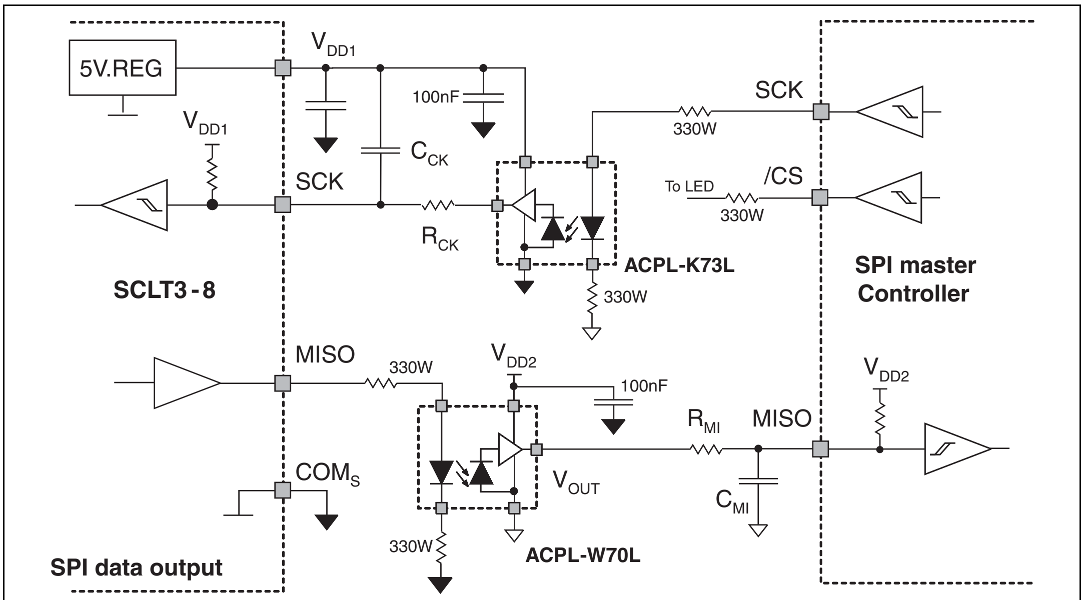


The configuration of the SCLT slave bus circuit allows the master bus controller to operate with other slave circuits in a different phase and polarity mode as long as it runs communication with SCLT in $C_{PHA} = 0$ and $C_{POL} = 0$.

The requirement to transfer data in a daisy chain configuration is to use an SPI control master circuit that is able to send and receive a bit stream from 8 minimum up to 128 within one chip select sequence depending on the number of SCLTs and SPI mode (8- or 16-bit).

3.1.1 Interfacing SPI section to I/O controller through opto-transistors

Figure 18. Opto-couplers connection between dual SCLT circuit and their master bus controller

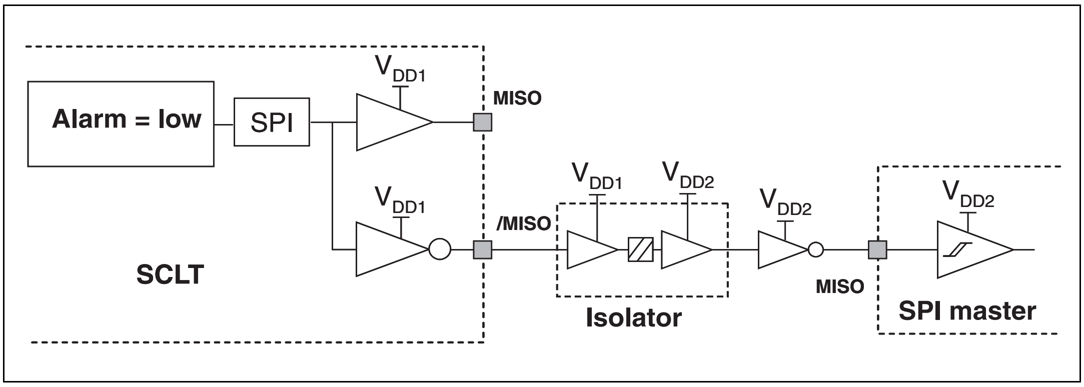


LED	V_{OUT}
ON	HIGH
OFF	LOW

F_{CK}	R_{CK}, R_{CS} , R_{MI}	C_{CK}, C_{CS}, C_{MI}
< 1MHz	220Ω	470pF

3.2 High speed operation with magnetic isolators

Figure 19. Connection of SCLT with a magnetic or capacitive coupler for alarm active in low level



Magnetic isolators are suitable for higher frequency operation, above 1 MHz, because of their lower current consumption.

But their primary power supply loss leads to a high state output that is not compatible with an alarm strategy active in low state as with SCLT. To overcome this issue, two inverting logic buffers can be implemented in the SPI hardware chain. The ASIC will also detect a primary supply loss with a low state. The SCLT is designed providing both MISO and /MISO in order to simplify this hardware environment as shown on *Figure 19*.

3.3 Reverse polarity robustness

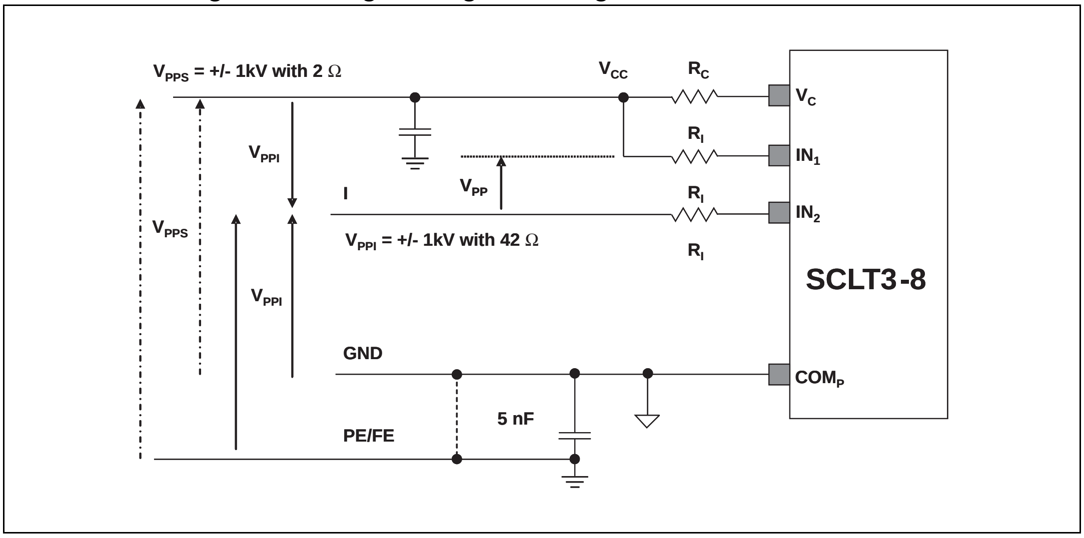
Any reverse polarity of an input IN_I generates some negative current in the circuit that does not disturb the operation of the other input channels as long as the power supply is working properly (V_{CC} >19 V).

Such a case is not dissipative for the SCLT, < 15 mW per input, but consideration should be given to the input resistors. A resistance of R_{IN} = 2.2 kΩ should produce a dissipation of 0.38 W at V_I = 30 V. The dissipation rating of the input resistor is set according to the duration of this situation.

The power supply V_C withstands also this kind of stress, the whole circuit being disabled.

3.4 Surge voltage immunity

Figure 20. Surge voltage test diagram of the SCLT circuit



The input and supply pins are designed to withstand electromagnetic interferences. They are protected by a clamping function that is connected to the ground pin COM_P. Combined with the serial input resistance R_I, this clamping protection is effective against the fast transient bursts (±4 kV, IEC 61000-4-4) and the voltage surges (±1 kV, IEC 61000-4-5).

This topology allows the surge voltage to be applied from each input to other inputs, the ground and the supply contacts in differential or common modes as shown in *Figure 20*.

Thanks to its high resistance R_C = 500 Ω, the supply pin V_C withstands ±1 kV surge voltage according to IEC 61000-4-5 using same diagram as *Figure 20*. With R_C = 2.2 kΩ, this power supply pin withstands more than ±2.5 kV.

3.5 Fast transient burst immunity

3.5.1 Considerations on the power section

The EFT protection is achieved with the same strategy as ESD and surge protection. An input capacitor C_I can be added to meet mainly the IEC 61000-4-6 conducted RFI immunity. These capacitors play a key role in suppressing front-end electrical stresses. Their capacitance can be about 22 nF (to validate by test for both EFT and RFI tests).

Detailed considerations for EMC performances, board design precautions and component selections are also described in ST application notes AN2846 and AN3031.

3.5.2 Considerations on the logic section

The SPI section is not submitted directly to the transient burst disturbance because this disturbance is applied to the logic input wires and the power supply wires.

Since the power section is protected with the clamping diodes, their serial impedance and the digital filters, the logic section and the serial interface is protected against the effects of transients.

Nevertheless, the SPI section may be submitted to indirect effects of the EFT transients. So, the design of the power supplies (V_{CC} and V_{DD}), the opto-transistors, and the printed circuit board are done with care to minimize the layout influences.

As shown on the suggested opto-transistor schematic on *Figure 13*, some R_C network and power supply decoupling capacitors should be added to meet the reinforced immunity level up to 2 MHz operation.

3.6 Under voltage alarm setting for IEC and device-net applications

The power supply voltage V_{CC} is monitored by the UVA block through the input resistances R_S and R_{PD}.

$V_{CON} = V_{BG} \times (1 + R_S/R_{PD})$

$V_{COFF} = (V_{BG} + V_{HY}) \times (1 + R_S/R_{PD})$

With V_{BG} = 1.26 V and V_{HY} = 0.1 V

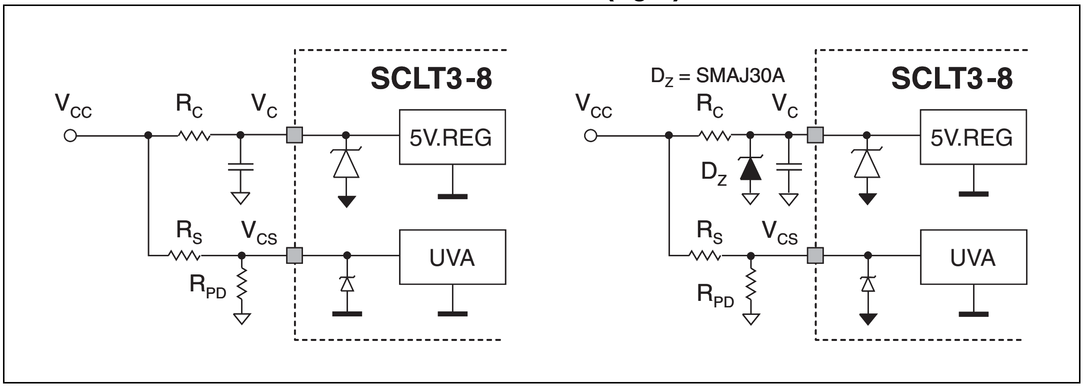
For IEC 6131 PLC applications, the alarm /UVA is activated when the power bus voltage is lower than the activation threshold V_{CON}, 17 V typical, and is released when the power bus voltage rises above the threshold V_{COFF}, 18 V typical.

In this application, the resistances are set to R_S = 1.5 MΩ and R_{PD} = 120 kΩ.

For device-net applications, the sensor power supply voltage can vary from 11 V to 25 V. The UVA alarm is set between the lower value and the SCLT minimum operation that is set at 9 V.

The power supply resistor R_C is reduced to match the minimum voltage V_{CC} with the device current consumption. The V_C pin robustness could be increased with an additional clamping diode D_Z to fit the 1 kV surge requirement. In this case an R_C resistance of 150 Ω and an SMAJ30A Transil™ diode are indicated.

Figure 21. Power supply connection versus IEC 61131-2 norm levels (left) and device-net norm levels (right)



3.7 Input operation for the device-net applications

If the sensor connected to the SCLT input has a drop voltage less than 1 V, this input runs with an on-state threshold equal to 10 V. Reducing the input resistance R_{IN} = 1.8 kΩ, the SCLT input meets such an operation.

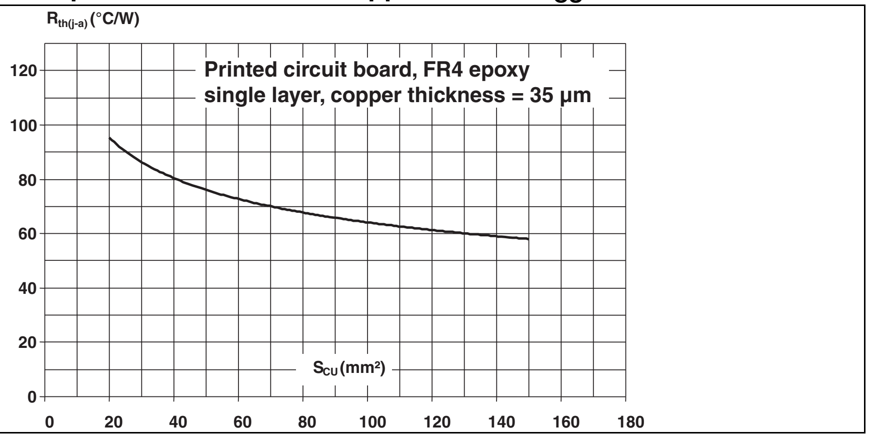
3.8 Dissipation calculation in the SCLT3-8 circuit

Table 12. Evaluation of dissipation in the SCLT3-8[(1)] with R_C = 500 Ω and I_{DD} = 7 mA

Circuit	Count	Drop voltage (V)	Current (mA)	Losses (mW)
V Regulator	1	30 - 500 x 0.007 - 5 = 21.5	7	150
Current limiter	8	30 - 2200 x 0.0026 = 24.3	< 2.6	505
Quiescent current	1	30 - 500 x 0.0018 = 29.1	1.8	53
			Total	708

1. Thermal resistance is less than: 90 °C/W corresponding to ΔT = 150 - 85 = 65 °C, P_D = 708 mW.

Figure 22. Relative variation of junction-to-ambient thermal resistance R_{TH_JA} versus printed circuit board copper surface S_{CU}



4 Package information

- Epoxy meets UL94, V0
- Lead-free packages

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: *www.st.com*. ECOPACK® is an ST trademark.

The exposed pad of the HTSSOP-38 improves heat transfer from the input dissipation to the printed circuit board. Increasing the copper surface helps to reduce any hot point on the board.

Figure 23. HTSSOP-38 dimension definitions

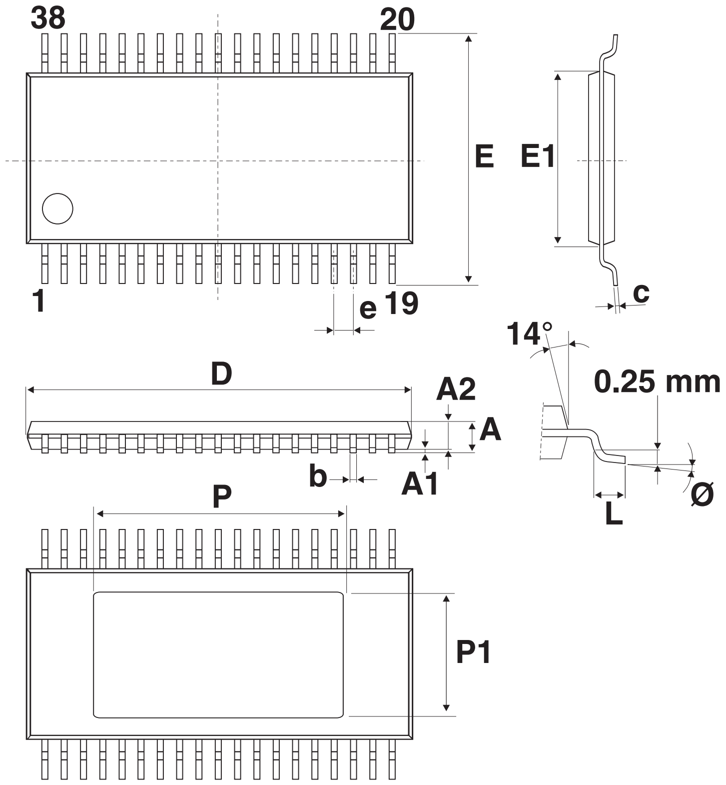
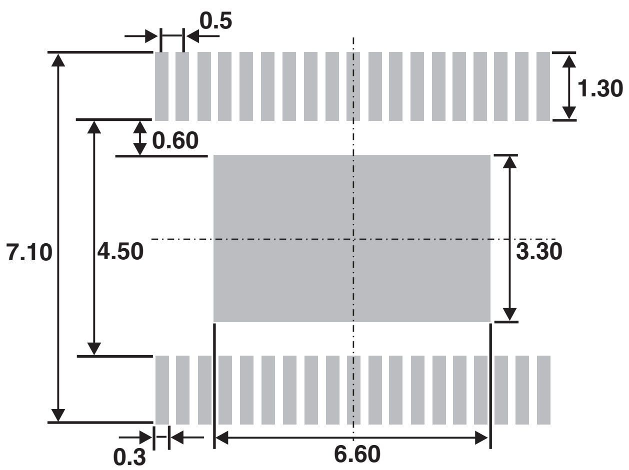


Table 13. HTSSOP-38 dimension values

Ref.	Dimensions					
	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	-	-	1.1	-	-	0.043
A1	0.05	-	0.15	0.002	-	0.006
A2	0.85	0.9	0.95	0.033	0.035	0.037
b	0.17	-	0.27	0.007	-	0.011
c	0.09	-	0.20	0.003	-	0.008
D	9.60	9.70	9.80	0.378	0.382	0.386
E1	4.30	4.40	4.50	0.169	0.173	0.177
e	-	0.50	-	-	0.020	-
E	-	6.40	-	-	0.252	-
L	0.50	0.60	0.70	0.020	0.024	0.027
P	6.40	6.50	6.60	0.252	0.256	0.260
P1	3.10	3.20	3.30	0.122	0.126	0.130
Ø	0°	-	8°	0°	-	8°

Figure 24. Footprint (dimensions in mm)



5 Ordering Information

Figure 25. Ordering information scheme

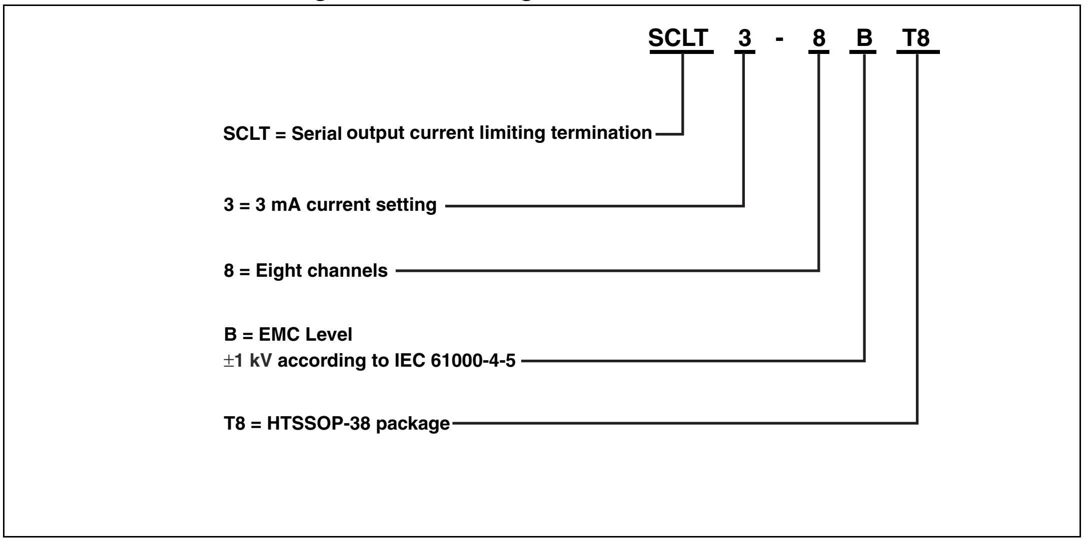


Table 14. Ordering information

Order code	Marking	Package	Weight	Base qty	Delivery mode
SCLT3-8BT8-TR	SCLT3-8BT8	HTSSOP-38	114 mg	2500	Tape and reel
SCLT3-8BT8	SCLT3-8BT8	HTSSOP-38	114 mg	50	Tube

6 Revision history

Table 15. Document revision history

Date	Revision	Changes
17-Nov-2008	1	Initial release.
04-May-2009	2	Updated mechanical data for package HTSSOP-38.
02-Nov-2009	3	Updated parameters in *Table 9* and *Table 10*. Added *Figure 14*, *Figure 15*, *Figure 16*, and *Figure 22*.
08-Sep-2011	4	Updated application note from AN2853 to AN3031.
04-Jul-2013	5	Updated *Figure 8* and *Figure 9*.

Please Read Carefully: