Precision Monolithic Quad SPST CMOS Analog Switches

DESCRIPTION

The DG1411 series of monolithic quad analog switches was designed to provide high speed, low error switching of precision analog signals. Combining low power (0.033 µW) with high speed (t_{ON}: 100 ns), the DG1411 family is ideally suited for portable and battery powered industrial and military applications.

To achieve high-voltage ratings and superior switching performance, the DG1411 series was built on Vishay Siliconix's newest high voltage silicon gate process. An epitaxial layer prevents latchup.

Each switch conducts equally well in both directions when on, and blocks input voltages up to the supply levels when off.

The DG1411, DG1412 respond to opposite control logic as shown in the Truth Table. The DG1413 has two normally open and two normally closed switches.

FEATURES

- 35 V supply max. rating
- ± 15 V analog signal range
- On-resistance - $R_{DS(on)}$: 1.5 Ω
- Fast switching - t_{ON}: 100 ns
- Ultra low power - P_D: 0.033 µW
- TTL, CMOS compatible
- Single supply capability
- Material categorization: For definitions of compliance please see www.vishay.com/doc?99912

Pb-free

RoHS COMPLIANT

HALOGEN FREE

BENEFITS

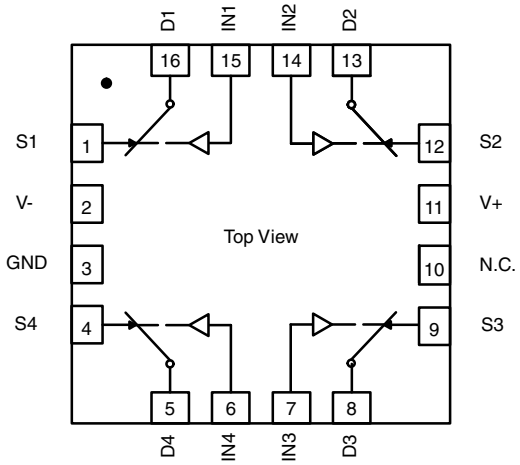
- Widest dynamic range
- Low signal errors and distortion
- Break-before-make switching action
- Simple interfacing

APPLICATIONS

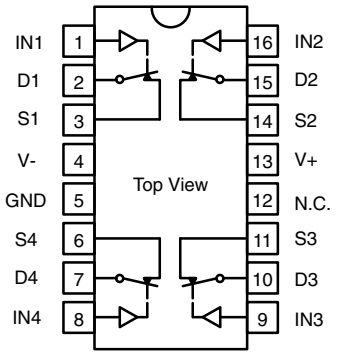
- Medical and Healthcare equipment
- Precision data acquisition
- Communication systems
- Battery powered systems
- Computer peripherals

FUNCTIONAL BLOCK DIAGRAM AND PIN CONFIGURATION - DG1411

DG1411EN
QFN-16 (4 x 4)



DG1411EQ
TSSOP



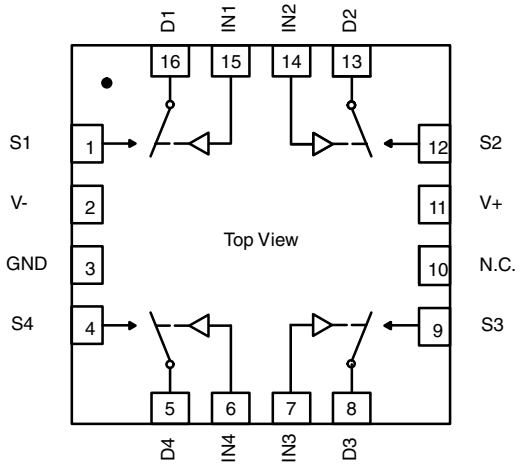
TRUTH TABLE - DG1411	
LOGIC	**SWITCH**
0	On
1	Off

Note

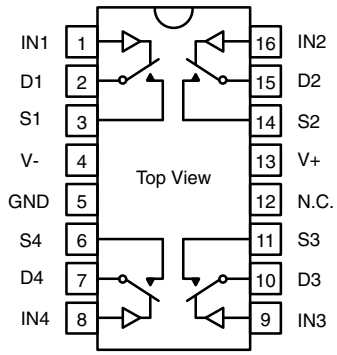
- Switches Shown for Logic "0" Input

FUNCTIONAL BLOCK DIAGRAM AND PIN CONFIGURATION - DG1412

DG1412EN
QFN-16 (4 x 4)



DG1412EQ
TSSOP



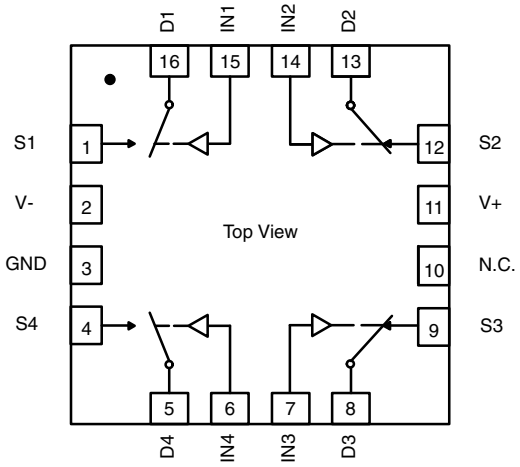
TRUTH TABLE - DG1412	
LOGIC	**SWITCH**
0	Off
1	On

Note

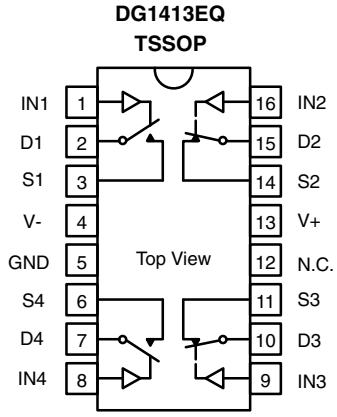
- Switches Shown for Logic “0” Input

FUNCTIONAL BLOCK DIAGRAM AND PIN CONFIGURATION - DG1413

DG1413EN
QFN-16 (4 x 4)



DG1413EQ
TSSOP



TRUTH TABLE - DG1413		
LOGIC	**SWITCHES 1, 4**	**SWITCHES 2, 3**
0	Off	On
1	On	Off

Note

- Switches Shown for Logic “0” Input

DEVICE OPTIONS				
PART NUMBER	**CONFIGURATION**	**SWITCH FUNCTION**	**TEMPERATURE RANGE**	**PACKAGE**
DG1411EN-T1-GE4	Quad SPST	NC	- 40 °C to + 125 °C	QFN(4x4) 16L (Variation 2)
DG1412EN-T1-GE4	Quad SPST	NO	- 40 °C to + 125 °C	QFN(4x4) 16L (Variation 2)
DG1413EN-T1-GE4	Quad SPST	NC/NO	- 40 °C to + 125 °C	QFN(4x4) 16L (Variation 2)
DG1411EQ-T1-GE3	Quad SPST	NC	- 40 °C to + 125 °C	TSSOP-16
DG1412EQ-T1-GE3	Quad SPST	NO	- 40 °C to + 125 °C	TSSOP-16
DG1413EQ-T1-GE3	Quad SPST	NC/NO	- 40 °C to + 125 °C	TSSOP-16

ABSOLUTE MAXIMUM RATINGS			
ELECTRICAL PARAMETER	**CONDITIONS**	**LIMITS**	**UNIT**
V+	Reference to GND	- 0.3 V to + 25 V	V
V-	Reference to GND	+ 0.3 V to - 25 V	
V+ to V-		+ 35	
Analog Inputs (S or D)		V- (- 0.3 V) to V+ (+ 0.3 V)	
Digital Inputs		GND (- 0.3 V) to V+ (+ 0.3 V)	
Maximum Continuous Switch Current	TSSOP-16, T_A = 25 °C	190	mA
	QFN(4x4) 16L, T_A = 25 °C	250	
	TSSOP-16, T_A = 125 °C	90	
	QFN(4x4) 16L, T_A = 125 °C	100	
Maximum Pulse Switch Current	Pulse at 1 mS, 1 % duty cycle	500	
Thermal Resistance	TSSOP-16	130	°C/W
	QFN(4x4) 16L	32	
Temperature			
Operating Temperature		- 40 to 125	°C
Max. Operating Junction Temperature		150	
Operating Junction Temperature		125	
Storage Temperature		- 65 to 150	

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING RANGE			
ELECTRICAL	**MINIMUM**	**MAXIMUM**	**UNIT**
IN	± 4.5	± 16.5	V

ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITIONS UNLESS OTHERWISE SPECIFIED V+ = 15 V, V- = - 15 V V_{INH} = 2 V, V_{INL} = 0.8 V	+ 25 °C	- 40 °C to + 85 °C	- 40 °C to + 125 °C	TYP/MAX.	UNIT
Analog Switch							
Analog Signal Range	V_{ANALOG}		V- to V+			-	V
Drain-Source On-Resistance	$R_{DS(on)}$	V_S = ± 10 V, I_S = - 10 mA; see fig. 23 V+ = + 13.5 V, V- = - 13.5 V	1.5	-	-	Typ.	Ω
			1.8	2.3	2.6	Max.	
ON-Resistance Flatness	$R_{flat(on)}$	V_S = ± 10 V, I_S = - 10 mA	0.3	-	-	-	Ω
			0.36	0.45	0.48	Max.	
ON-Resistance Matching	$\Delta R_{DS(on)}$		0.18	0.19	0.21	Max.	
Switch Off Leakage Current	$I_S/I_{d(off)}$	V+ = + 16.5 V, V- = - 16.5 V V_S = ± 10 V, V_D = ± 10 V; see fig. 24	± 0.03	-	-	Typ.	nA
			± 0.55	± 2	± 12.5	Max.	
Channel On Leakage Current	$I_{d(on)}$	V_S = V_D = ± 10 V; see fig. 25	± 0.15	-	-	Typ.	
			± 2	± 4	± 35	Max.	
Digital Control							
Input, High Voltage	V_{INH}		-	-	2	$V_{min.}$	V
Input, Low Voltage	V_{INL}		-	-	0.8	$V_{max.}$	
Input Leakage	I_{IN}	V_{IN} = V_{GND} or V+	0.005	-	-	Typ,	µA
			-	-	± 0.1	Max.	
Digital Input Capacitance	C_{IN}		3.5	-	-	Typ.	pF
Dynamic Characteristics							
Break-Before-Make Time	t_{OPEN}	V_{S1}= V_{S2} = 10 V, see fig. 31; R_L= 300 Ω, C_L = 35 pF	25	-	-	Typ.	ns
				-	10	Min.	
Turn-On Time	t_{ON}	V_S = 10 V, see fig. 30 R_L = 300 Ω, C_L = 35 pF	100	-	-	Typ,	
			150	170	190	Max.	
Turn-Off Time	t_{OFF}		90	-	-	Typ,	
			120	140	160	Max.	
Charge Injection	Q_{INj}	C_L = 1 nF, R_{GEN} = 0 Ω, V_S = 0 V see fig. 32	- 20	-	-	Typ.	pC
Off Isolation	OIRR	C_L = 5 pF, R_L = 50 Ω, 100 kHz	- 80	-	-	Typ.	dB
Cross Talk	X_{TALK}	C_L = 5 pF, R_L = 50 Ω, 1 MHz	- 100	-	-	Typ.	
Insertion Loss		f = 1 MHz, R_L = 50 Ω, C_L = 5 pF	- 0.35	-		Typ.	
Total Harmonic Distortion	THD	R_L = 110 Ω, 15 V_{p-p}, f = 20 Hz to 20 kHz	0.014	-	-	Typ.	%
Bandwidth, -3dB	BW	C_L = 5 pF, R_L = 50 Ω	170	-	-	Typ.	MHz
Source Off Capacitance	$C_{S(off)}$	f = 1 MHz, V_S = 0 V	11	-	-	Typ.	pF
Drain Off Capacitance	$C_{D(off)}$		24	-	-	Typ.	
Drain On Capacitance	$C_{D(on)}$		87	-	-	Typ.	
Power Requirements							
Power Supply Range		GND = 0 V	± 4.5/± 16.5 min./max.				V
Power Supply Current	I+	Digital Input 0 or V+ V+ = + 16.5 V, V- = - 16.5 V	0.001	-	-	Typ.	µA
				-	1	Max.	
		Digital Input = 5 V	220	-	-	Typ.	
				-	380	Max.	
	I-	Digital Input 0 or V+	0.001	-	-	Typ.	
				-	1	Max.	

ELECTRICAL CHARACTERISTICS - SINGLE 12 V SUPPLY							
PARAMETER	**SYMBOL**	**TEST CONDITIONS UNLESS OTHERWISE SPECIFIED V+ = 12 V, V- = 0 V V_{INH} = 2 V, V_{INL} = 0.8 V**	**+ 25 °C**	**- 40 °C to + 85 °C**	**- 40 °C to + 125 °C**	**TYP/MAX.**	**UNIT**
Analog Switch							
Analog Signal Range	V_{ANALOG}		0 V to V+				V
Drain-Source On-Resistance	$R_{DS(on)}$	V_S = 0 V to 10 V, I_S = - 10 mA; see fig. 23, V+ = 10.8 V, V- = 0 V	2.8	-	-	Typ.	Ω
			3.5	4.3	4.8	Max.	
ON-Resistance Flatness	$R_{flat(on)}$	V_S = 0 V to 10 V, I_S = - 10 mA	0.6	-	-	Typ.	Ω
			1.1	1.2	1.3	Max.	
ON-Resistance Matching	ΔR_{on}		0.13	-	-	Typ.	
			0.21	0.23	0.25	Max.	
Switch Off Leakage Current	$I_S/I_{d(off)}$	V+ = 10.8 V, V- = 0 V V_S = 1 V/10 V, V_D = 10 V/0 V see fig. 24	± 0.02	-	-	Typ.	nA
			± 0.55	± 2	± 12.5	Max.	
Channel On Leakage Current	$I_{d(on)}$	V_S = V_D = 1 V/10 V; see fig. 25	± 0.15	-	-	Typ.	
			± 1.5	± 4	± 30	Max.	
Digital Control							
Input, High Voltage	V_{INH}		-	-	2	Min.	V
Input, Low Voltage	V_{INL}		-	-	0.8	Max.	
Input Leakage	I_{IN}	V_{IN} = V_{GND} or V+	0.001	-	-	Typ.	µA
			-	-	± 0.1	Max.	
Digital Input Capacitance	C_{IN}		3.5	-	-	Typ.	pF
Dynamic Characteristics							
Break-Before-Make Time	t_{OPEN}	V_{S1} = V_{S2} = 8 V; see fig. 31, R_L = 300 Ω, C_L = 35 pF	100	-	-	Typ.	ns
			-	-	40	Min.	
Turn-On Time	t_{ON}	V_S = 8 V; see fig. 30, R_L = 300 Ω, C_L = 35 pF	210	-	-	Typ.	
			250	320	360	Max.	
Turn-Off Time	t_{OFF}		100	-	-	Typ.	
			135	165	190	Max.	
Charge Injection	Q_{INj}	C_L = 1 nF, R_{GEN} = 0 Ω, V_S = 6 V see fig. 32	30	-	-	Typ.	pC
Off Isolation	OIRR	R_L = 50 Ω, C_L = 5 pF, 100 kHz	- 80	-	-	Typ.	dB
Cross Talk	X_{TALK}	R_L = 50 Ω, C_L = 5 pF, 1 MHz	- 100	-	-	Typ.	
Insertion Loss		f = 1 MHz, R_L = 50 Ω, C_L = 5 pF	- 0.5	-	-	Typ.	
Bandwidth, -3dB	BW	R_L = 50 Ω, C_L = 5 pF	130	-	-	Typ.	MHz
Source Off Capacitance	$C_{S(off)}$	f = 1 MHz, V_S = 6 V	17	-	-	Typ.	pF
Drain Off Capacitance	$C_{D(off)}$		30	-	-	Typ.	
Drain On Capacitance	$C_{D(on)}$		94	-	-	Typ.	
Power Requirements							
Power Supply Range		GND = 0 V, V- = 0 V	± 5/± 16.5 min./max.				V
Power Supply Current	I+	Digital Input 0 or V+ V+ = 13.2 V	-	0.001	-	Typ.	µA
			-	-	1	Max.	
		Digital Input = 5 V	-	220	-	Typ.	
			-	-	380	Max.	

ELECTRICAL CHARACTERISTICS - DUAL ± 5 V SUPPLIES							
PARAMETER	**SYMBOL**	**TEST CONDITIONS UNLESS OTHERWISE SPECIFIED V+ = 5 V, V- = - 5 V V_{INH} = 2 V, V_{INL} = 0.8 V**	**+ 25 °C**	**- 40 °C to + 85 °C**	**- 40 °C to + 125 °C**	**TYP/MAX.**	**UNIT**
Analog Switch							
Analog Signal Range	V_{ANALOG}		0 to V+				V
Drain-Source On-Resistance	$R_{DS(on)}$	V_S = ± 4.5 V, I_S = - 10 mA; see fig. 23, V+ = + 4.5 V, V- = - 4.5 V	3.3	-	-	Typ.	Ω
			4	4.9	5.4	Max.	
ON-Resistance Flatness	$R_{flat(on)}$	V_S = ± 4.5 V, I_S = - 10 mA	0.9	-	-	Typ.	
			1.1	1.24	1.31	Max.	
ON-Resistance Matching	ΔR_{on}		0.13	-	-	Typ.	
			0.22	0.23	0.25	Max.	
Switch Off Leakage Current	$I_S/I_{d(off)}$	V+ = + 5.5 V, V- = - 5.5 V, V_S = +/- 4.5 V, V_D = -/+ 4.5 V; see fig. 24	± 0.03	-	-	Typ.	nA
			± 0.55	± 2	± 12.5	Max.	
Channel On Leakage Current	$I_{d(on)}$	VS = VD = ± 4.5 V; see fig. 25	± 0.05	-	-	Typ.	
			± 1	± 4	± 30	Max.	
Digital Control							
Input, High Voltage	V_{INH}		-	-	2	Min.	V
Input, Low Voltage	V_{INL}		-	-	0.8	Max.	
Input Leakage	I_{IN}	V_{IN} = V_{GND} or V+	0.001	-	-	Typ.	µA
			-	-	± 0.1	Max.	
Digital Input Capacitance	C_{IN}		3.5	-	-	Typ.	pF
Dynamic Characteristics							
Break-Before-Make Time	t_{OPEN}	V_{S1} = V_{S2} = 3 V; see fig. 31, R_L = 300 Ω, C_L = 35 pF	100	-	-	Typ.	ns
			-	-	50	Min.	
Turn-On Time	t_{ON}	V_S = 3 V; see fig. 30, R_L = 300 Ω, C_L = 35 pF	275	-	-	Typ.	
			400	465	510	Max.	
Turn-Off Time	t_{OFF}		175	-	-	Typ.	
			290	320	380	Max.	
Charge Injection	Q_{INj}	C_L = 1 nF, R_{GEN} = 0 Ω, V_S = 0 V; see fig. 32	30	-	-	Typ.	pC
Off Isolation	OIRR	R_L = 50 Ω, C_L = 5 pF, 100 KHz	- 80	-	-	Typ.	dB
Cross Talk	X_{TALK}	R_L = 50 Ω, C_L = 5 pF, 1 MHz	- 100	-	-	Typ.	
Insertion Loss		f = 1 MHz, R_L = 50 Ω, C_L = 5 pF	- 0.5	-	-	Typ.	
Bandwidth, -3dB	BW	R_L = 50 Ω, C_L = 5 pF	130	-	-	Typ.	MHz
Source Off Capacitance	$C_{S(off)}$	f = 1 MHz, V_S = 0 V	18	-	-	Typ.	pF
Drain Off Capacitance	$C_{D(off)}$		31	-	-	Typ.	
Drain On Capacitance	$C_{D(on)}$		95	-	-	Typ.	
Power Requirements							
Power Supply Range		GND = 0 V	± 4.5 V/± 16.5 min./max.				V
Power Supply Current	I+	Digital Input 0 V or V+ V+ = + 5.5 V, V- = - 5.5 V	0.001	-	-	Typ.	µA
			-	-	1	Max.	
	I-	Digital Input = 0 V or V+	0.001	-	-	Typ.	
			-	-	1	Max.	

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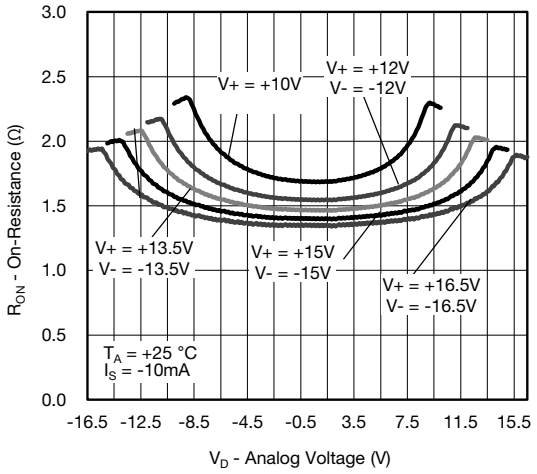
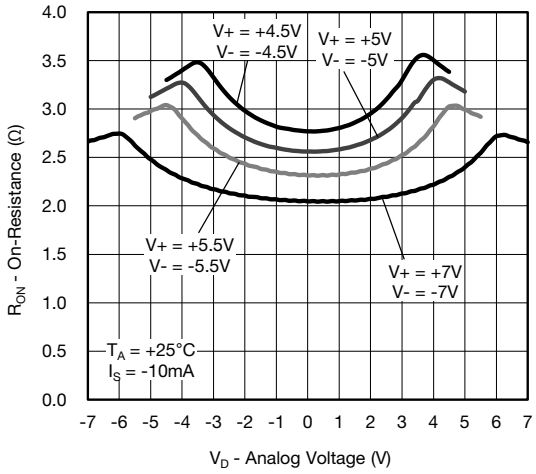
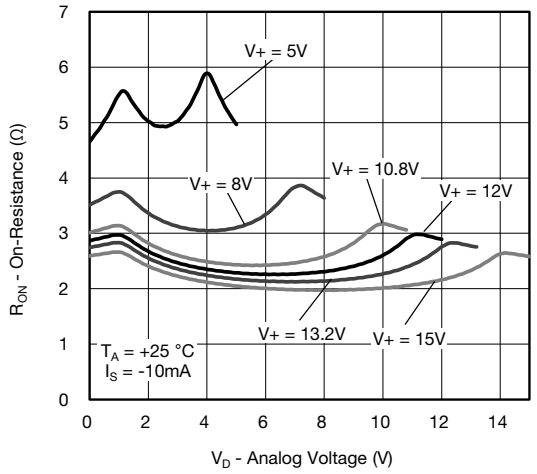
TYPICAL CHARACTERISTICS (T_A = 25 °C, unless otherwise noted)



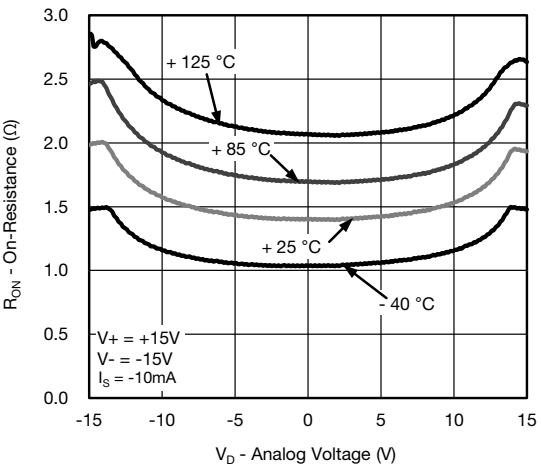
On-Resistance vs. Analog Voltage (DS1)



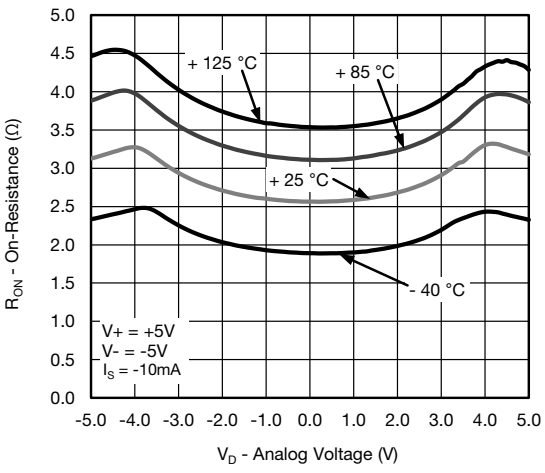
On-Resistance vs. Analog Voltage (DS2)



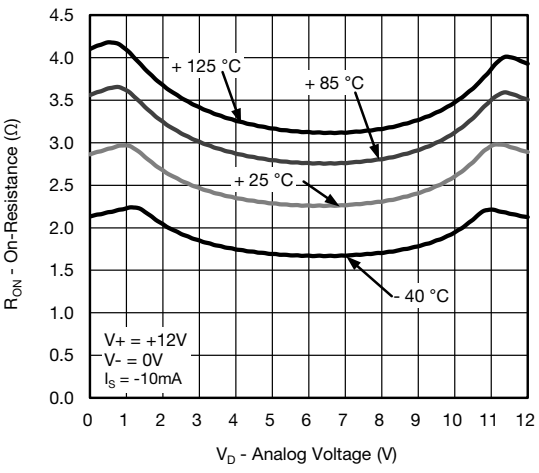
On-Resistance vs. Analog Voltage (DSS)



On-Resistance vs. Temperature (± 15 V)

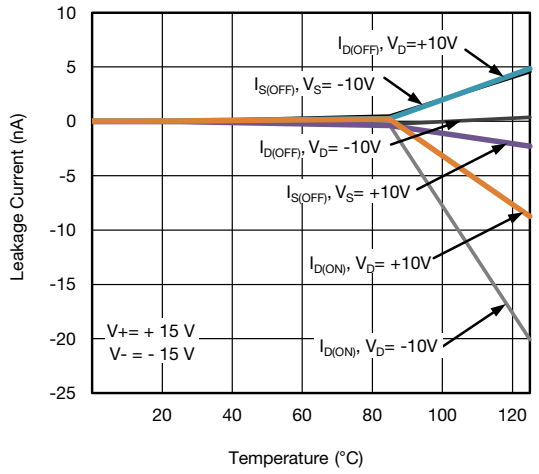


On-Resistance vs. Temperature (± 5 V)

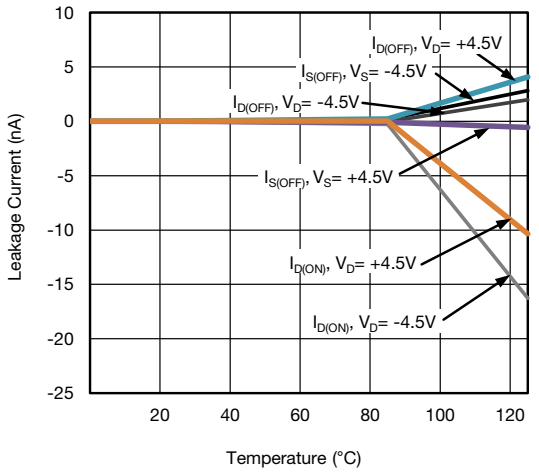


On-Resistance vs. Temperature (+ 12 V)

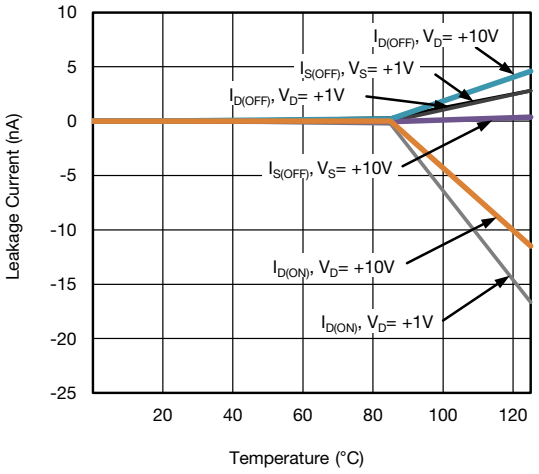
TYPICAL CHARACTERISTICS (T_A = 25 °C, unless otherwise noted)



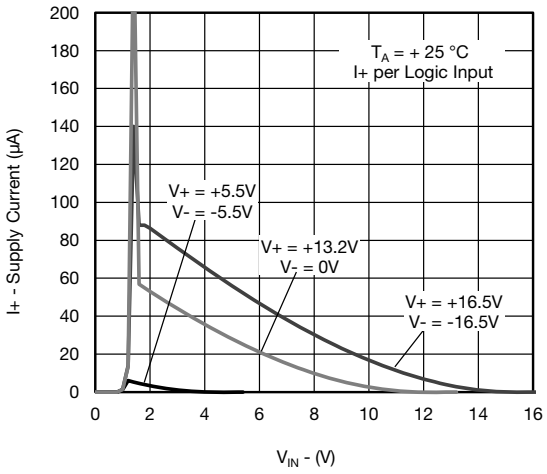
Leakage Current vs. Temperature (± 15 V)



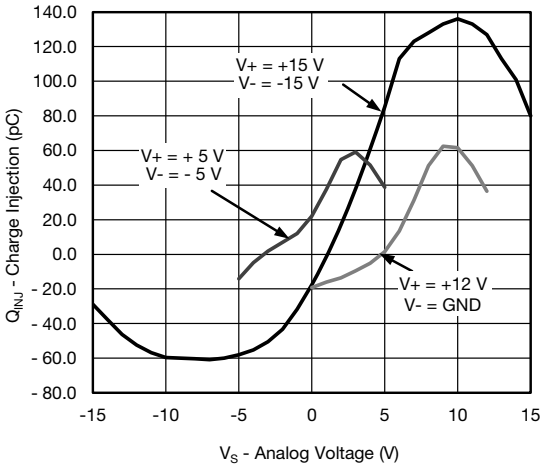
Leakage Current vs. Temperature (± 5 V)



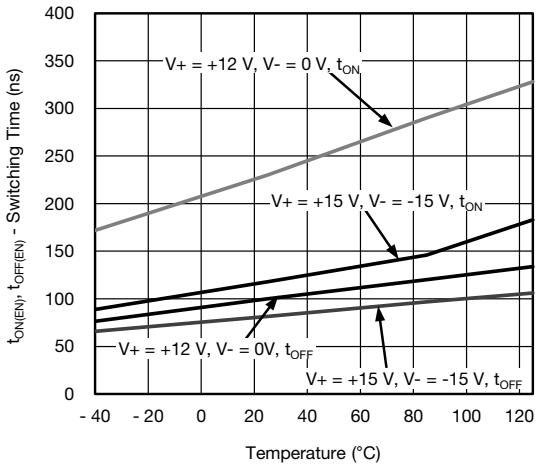
Leakage Current vs. Temperature (+ 12 V)



Supply Current vs. Logic Level

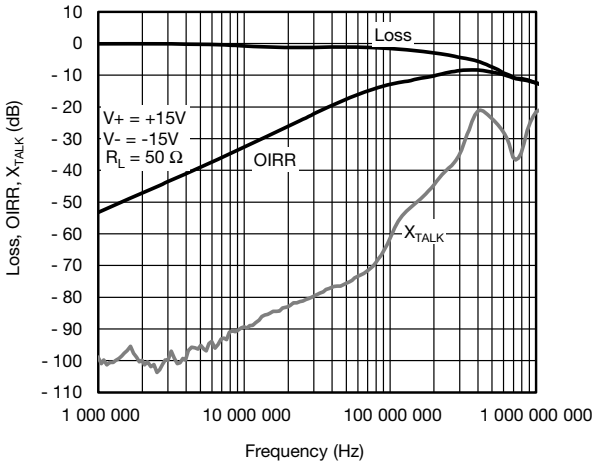


Charge Injection vs. Analog Voltage

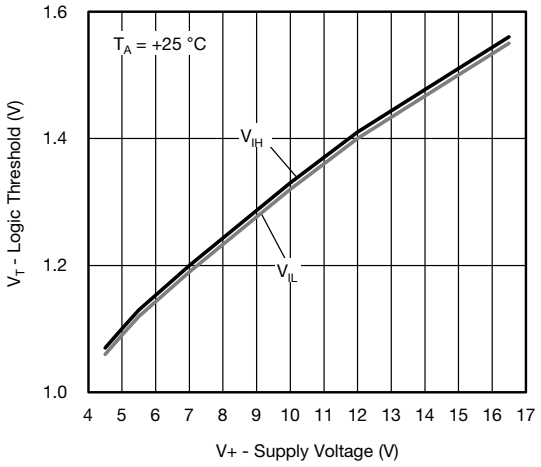


Switching Time vs. Temperature

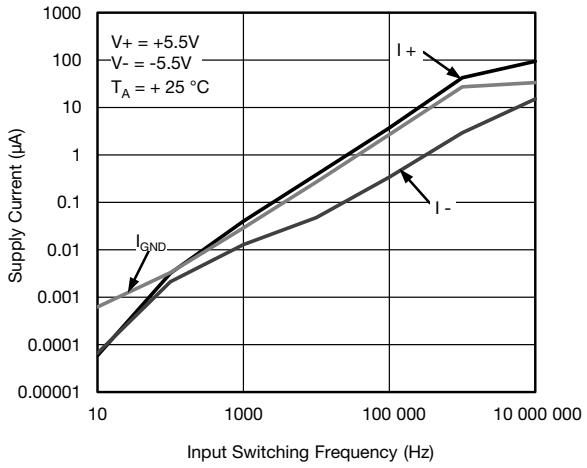
TYPICAL CHARACTERISTICS (T_A = 25 °C, unless otherwise noted)



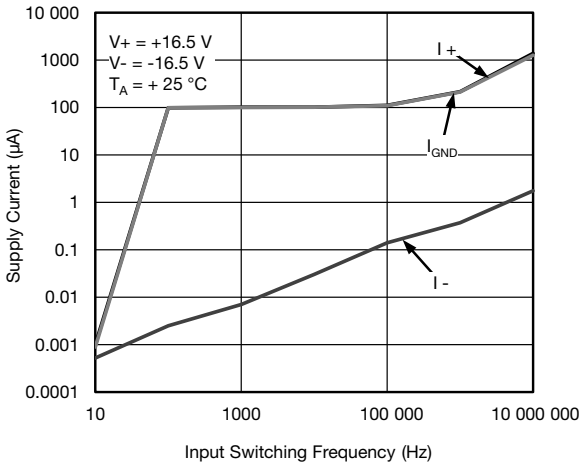
BW, OIRR, X_{TALK} vs. Frequency



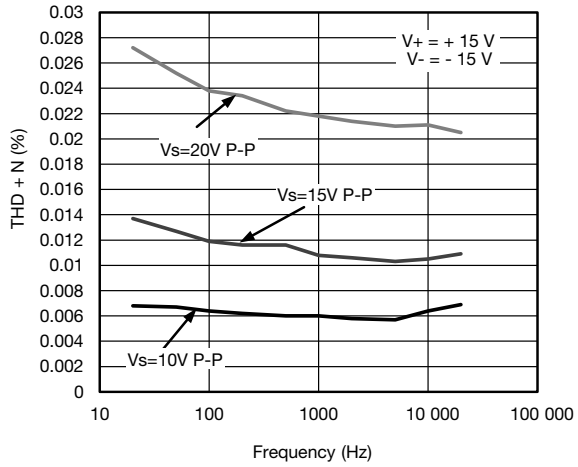
Logic Threshold vs. Supply Voltage



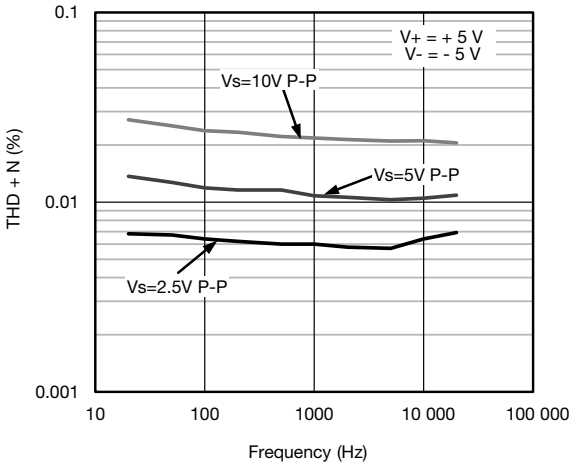
Supply Current vs. Switching Frequency (± 5.5 V)



Supply Current vs. Switching Frequency (± 16.5 V)

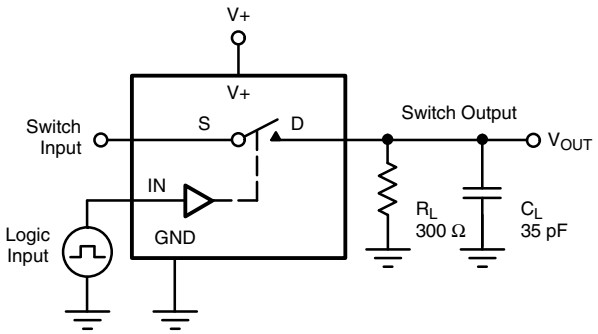


THD vs. Frequency (± 15 V)



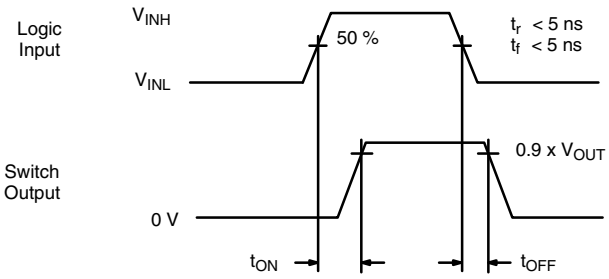
THD vs. Frequency (± 5 V)

TEST CIRCUITS



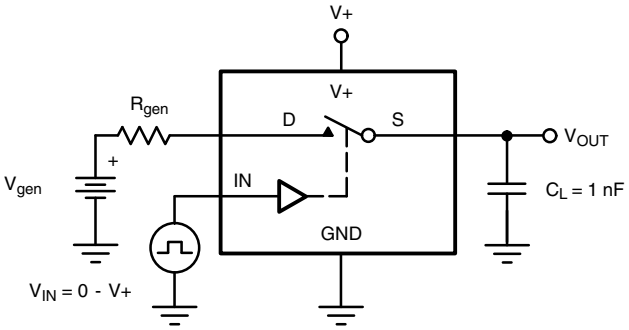
C_L (includes fixture and stray capacitance)

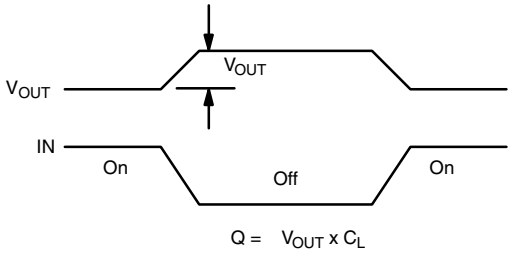
$$V_{OUT} = V_D \left(\frac{R_L}{R_L + R_{ON}} \right)$$



Logic "1" = Switch On
Logic input waveforms inverted for switches that have the opposite logic sense.

Fig. 1 - Switching Time





IN depends on switch configuration: input polarity determined by sense of switch.

Fig. 2 - Charge Injection

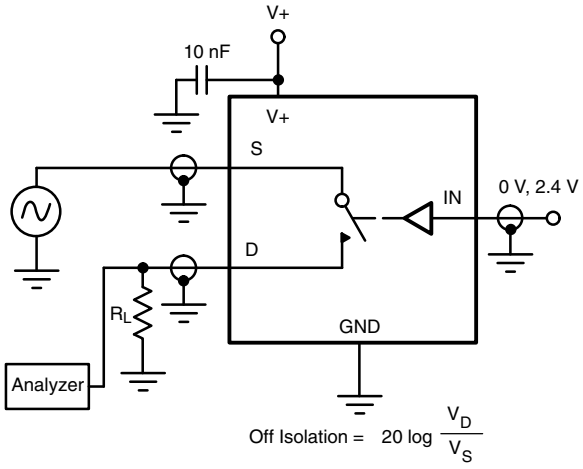


Fig. 3 - Off-Isolation

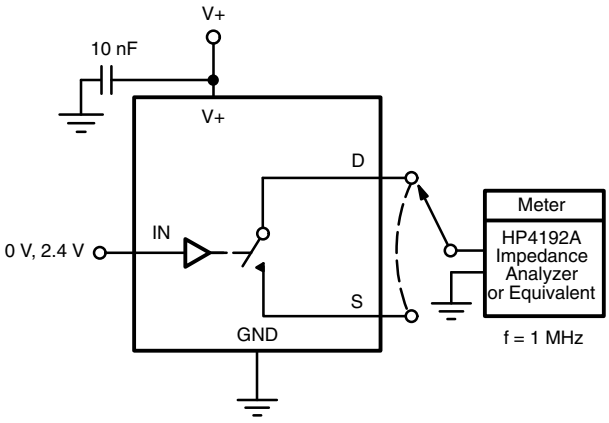
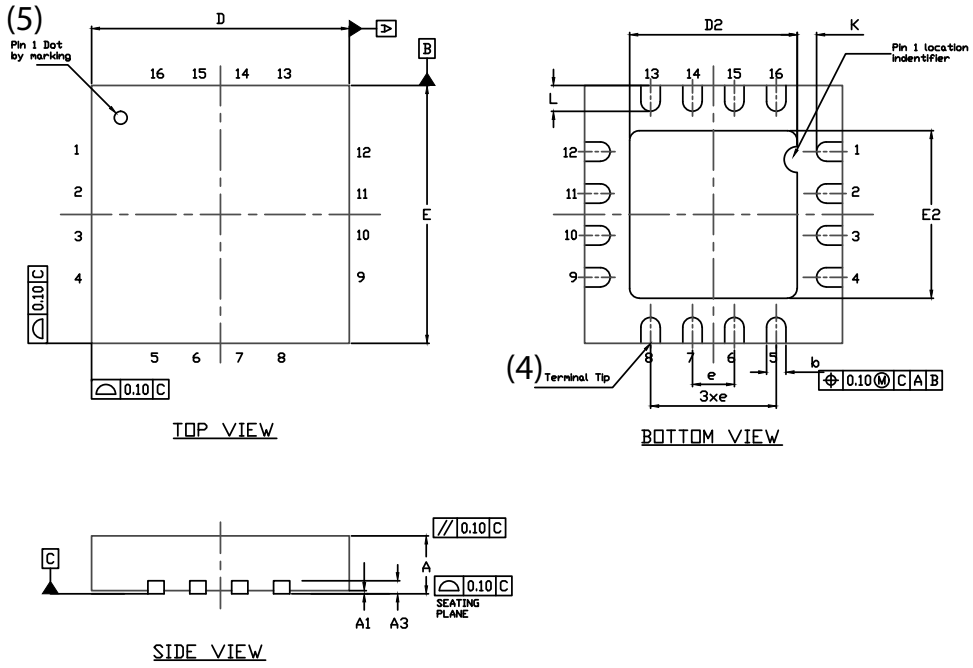


Fig. 4 - Channel Off/On Capacitance

QFN 4x4-16L Case Outline



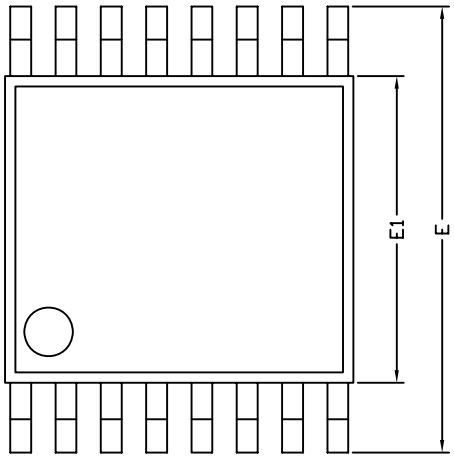
DIM	VARIATION 1						VARIATION 2					
	MILLIMETERS[1]			INCHES			MILLIMETERS[1]			INCHES		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.75	0.85	0.95	0.029	0.033	0.037	0.75	0.85	0.95	0.029	0.033	0.037
A1	0	-	0.05	0	-	0.002	0	-	0.05	0	-	0.002
A3	0.20 ref.			0.008 ref.			0.20 ref.			0.008 ref.		
b	0.25	0.30	0.35	0.010	0.012	0.014	0.25	0.30	0.35	0.010	0.012	0.014
D	4.00 BSC			0.157 BSC			4.00 BSC			0.157 BSC		
D2	2.0	2.1	2.2	0.079	0.083	0.087	2.5	2.6	2.7	0.098	0.102	0.106
e	0.65 BSC			0.026 BSC			0.65 BSC			0.026 BSC		
E	4.00 BSC			0.157 BSC			4.00 BSC			0.157 BSC		
E2	2.0	2.1	2.2	0.079	0.083	0.087	2.5	2.6	2.7	0.098	0.102	0.106
K	0.20 min.			0.008 min.			0.20 min.			0.008 min.		
L	0.5	0.6	0.7	0.020	0.024	0.028	0.3	0.4	0.5	0.012	0.016	0.020
N[3]	16			16			16			16		
Nd[3]	4			4			4			4		
Ne[3]	4			4			4			4		

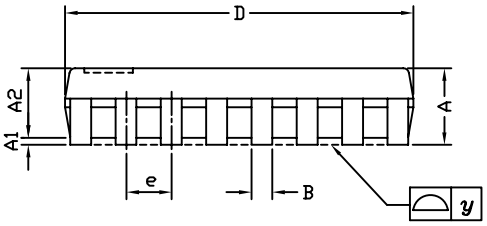
Notes

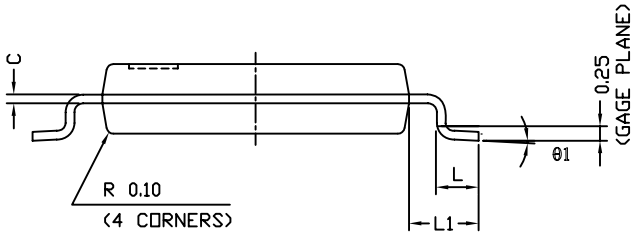
(1) Use millimeters as the primary measurement.
(2) Dimensioning and tolerances conform to ASME Y14.5M. - 1994.
(3) N is the number of terminals. Nd and Ne is the number of terminals in each D and E site respectively.
(4) Dimensions b applies to plated terminal and is measured between 0.15 mm and 0.30 mm from terminal tip.
(5) The pin 1 identifier must be existed on the top surface of the package by using identification mark or other feature of package body.
(6) Package warpage max. 0.05 mm.

ECN: S13-0893-Rev. B, 22-Apr-13
DWG: 5890

TSSOP: 16-LEAD

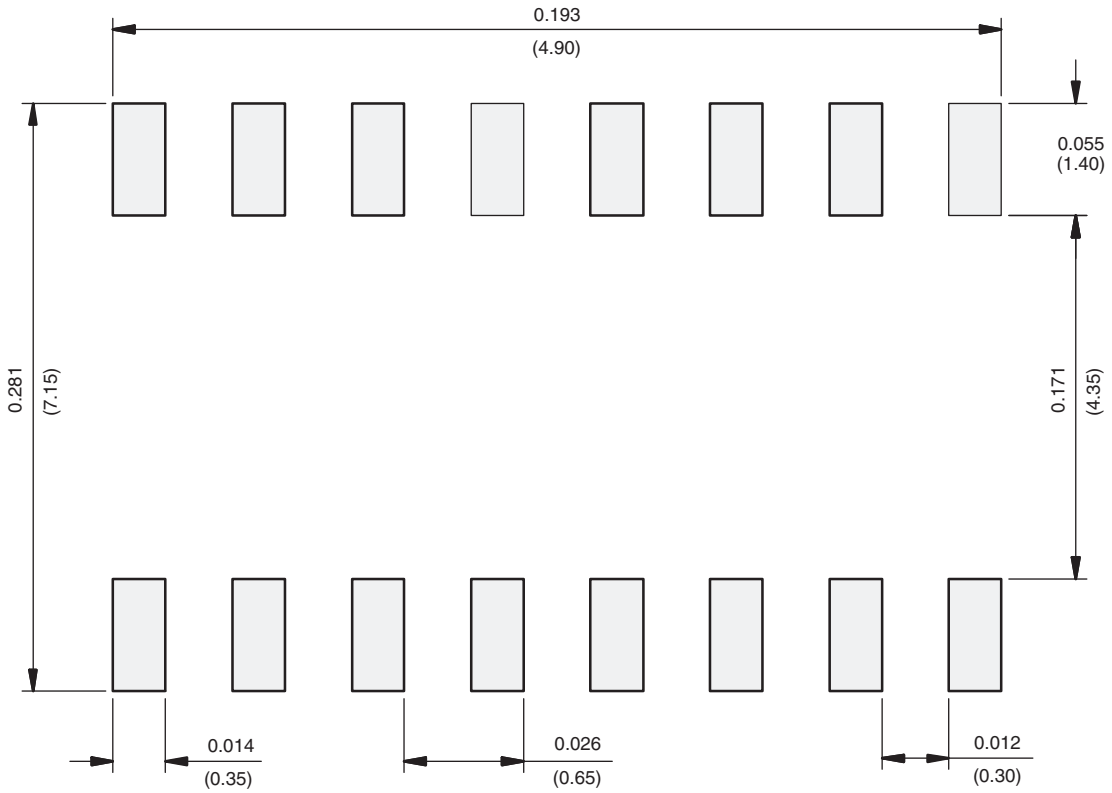






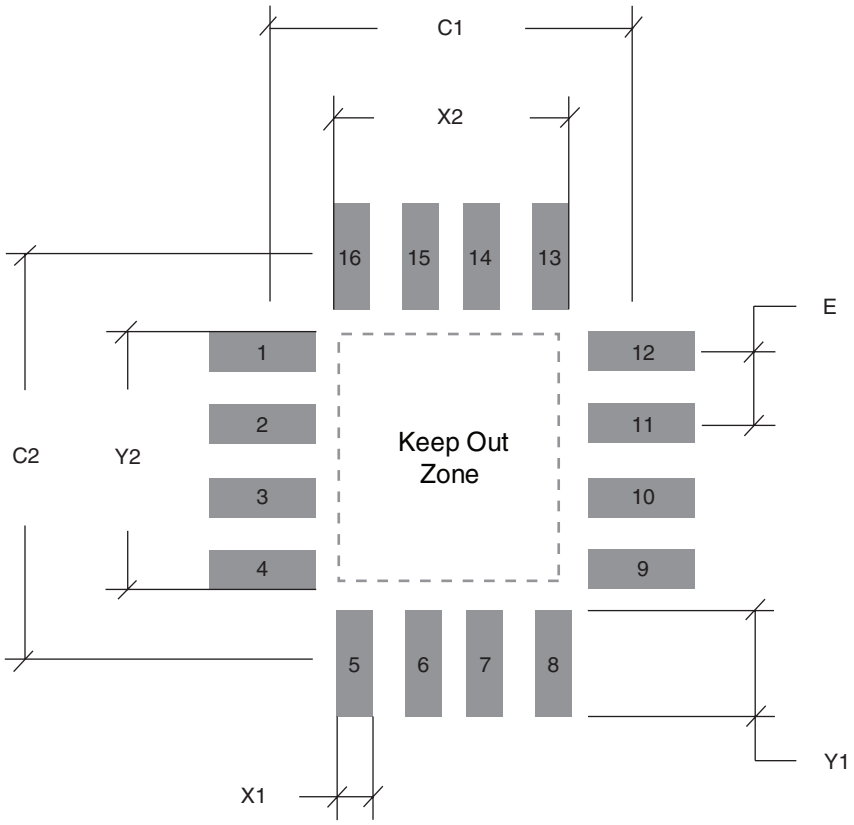
Symbols	DIMENSIONS IN MILLIMETERS		
	Min	Nom	Max
A	-	1.10	1.20
A1	0.05	0.10	0.15
A2	-	1.00	1.05
B	0.22	0.28	0.38
C	-	0.127	-
D	4.90	5.00	5.10
E	6.10	6.40	6.70
E1	4.30	4.40	4.50
e	-	0.65	-
L	0.50	0.60	0.70
L1	0.90	1.00	1.10
y	-	-	0.10
θ1	0°	3°	6°
ECN: S-61920-Rev. D, 23-Oct-06 DWG: 5624			

RECOMMENDED MINIMUM PAD FOR TSSOP-16



Recommended Minimum Pads
Dimensions in inches (mm)

RECOMMENDED MINIMUM PADS FOR QFN-16 (4 x 4 MM BODY)



	Inches	Millimeters
C1	0.142	3.60
C2	0.142	3.60
E	0.026	0.65
X1	0.014	0.35
X2	0.089	2.25
Y1	0.037	0.95
Y2	0.089	2.25

Note:
QFN-16 (4 x 4) has an exposed center pad that must not come into contact with any metalized structure on the PCB. This area is considered a Keep Out Zone.

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