Panasonic

AN32155A

http://www.semicon.panasonic.co.jp/en/

# 4×3 Matrix LED Driver LSI with Step-up Charge Pump Control Circuit

## FEATURES

- 4 x 3 LED Matrix Driver
  (Total LED that can be driven = 12)
- LED maximum current selectable
- Step-up charge pump DC/DC converter : 200 mA
- I²C interface (Slave address selectable)
- 24 pin Wafer Level Chip Size Package (WLCSP)

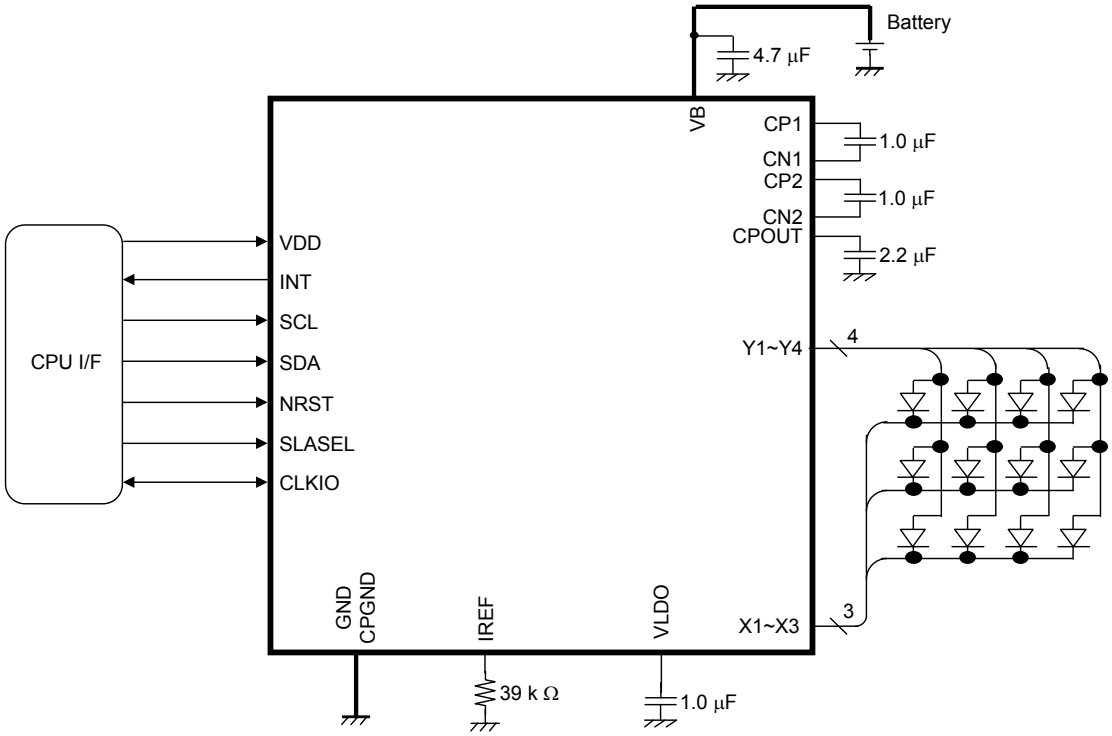
## DESCRIPTION

AN32155A is a 4 x 3 LED driver equipped with a step-up charge pump circuit.

## APPLICATIONS

- Mobile Phone
- Smart Phone
- PCs
- Game Consoles
- Home Appliances etc.

## TYPICAL APPLICATION




Note)
The application circuit is an example. The operation of the mass production set is not guaranteed. Sufficient evaluation and verification is required in the design of the mass production set. The Customer is fully responsible for the incorporation of the above illustrated application circuit in the design of the equipment.



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## ABSOLUTE MAXIMUM RATINGS

| Parameter | Symbol | Rating | Unit | Note |
|---|---|---|---|---|
| Supply voltage | $VB_{MAX}$ | 6.5 | V | *1 |
| | $CPOUT_{MAX}$ | 6.5 | V | *1 |
| | $VDD_{MAX}$ | 6.5 | V | *1 |
| Operating ambience temperature | $T_{opr}$ | – 30 to + 85 | °C | *2 |
| Operating junction temperature | $T_j$ | – 30 to + 125 | °C | *2 |
| Storage temperature | $T_{stg}$ | – 55 to + 125 | °C | *2 |
| Input Voltage Range | SLASEL, SCL, SDA, CLKIO, NRST | – 0.3 to 6.5 | V | — |
| Output Voltage Range | CLKIO, VLDO, INT, Y1, Y2, Y3, Y4, X1, X2, X3 | – 0.3 to 6.5 | V | — |
| ESD | HBM | 2.0 | kV | — |

Note) This product may sustain permanent damage if subjected to conditions higher than the above stated absolute maximum rating. This rating is the maximum rating and device operating at this range is not guaranteeable as it is higher than our stated recommended operating range.
When subjected under the absolute maximum rating for a long time, the reliability of the product may be affected.
*1: $VB_{MAX}$ = VB, $VDD_{MAX}$ = VDD , $CPOUT_{MAX}$ = CPOUT
The values under the condition not exceeding the above absolute maximum ratings and the power dissipation.
*2: Except for the power dissipation, operating ambient temperature, and storage temperature, all ratings are for $T_a$ = 25°C.

## POWER DISSIPATION RATING

| PACKAGE | $\theta_{JA}$ | $P_D$ (Ta=25 °C) | $P_D$ (Ta=85 °C) |
|---|---|---|---|
| 24 pin Wafer Level Chip Size Package (WLCSP) | 197.29 °C /W | 0.507 W | 0.2028 W |

Note) For the actual usage, please refer to the $P_D$-Ta characteristics diagram in the package specification, follow the power supply voltage, load and ambient temperature conditions to ensure that there is enough margin and the thermal design does not exceed the allowable value.

**CAUTION**

Although this LSI has built-in ESD protection circuit, it may still sustain permanent damage if not handled properly. Therefore, proper ESD precautions are recommended to avoid electrostatic damage to the MOS gates



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## RECOMMENDED OPERATING CONDITIONS

| Parameter | Symbol | Min. | Typ. | Max. | Unit | Note |
|---|---|---|---|---|---|---|
| Supply voltage range | VB (CPOUT) | 3.1 | 3.6 | 6.0 | V | *1 |
| | VDD | 1.7 | 1.85 | 6.0 | V | *1, 2 |
| Input Voltage Range | SLASEL, SCL, SDA, CLKIO | – 0.3 | — | VDD + 0.3 | V | *3 |
| | NRST | – 0.3 | — | VB + 0.3 | V | *3 |
| Output Voltage Range | CLKIO | – 0.3 | — | VDD + 0.3 | V | *3 |
| | VLDO, INT, Y1, Y2, Y3, Y4, X1, X2, X3 | – 0.3 | — | VB + 0.3 | V | *3 |

Note) *1: The values under the condition not exceeding the above absolute maximum ratings and the power dissipation.
Do not apply external currents and voltages to any pin not specifically mentioned.
Voltage values, unless otherwise specified, are with respect to GND. GND is voltage for GND and CPGND.
VDD is voltage for VDD. VB is voltage for VB and VBCP. VLED is voltage for VLED.
*2: VDD voltage must be applied in the range which does not exceed VB voltage.
*3: (VDD + 0.3 ) V must not exceed 6.5 V. (VB + 0.3 ) V must not exceed 6.5 V.



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## ELECTRICAL CHARACTERISTICS

VB = 3.6 V, VDD = 1.85 V

Note) $T_a$ = 25 °C ± 2 °C unless otherwise specified.

| Parameter | Symbol | Condition | Limits | | | Unit | Note |
|---|---|---|---|---|---|---|---|
| | | | Min | Typ | Max | | |
| **Current consumption** | | | | | | | |
| Current consumption (1) at OFF mode | ICC1 | VB = 3.6 V<br>NRST = 0V | — | 0 | 1 | μA | — |
| Current consumption (2) at OFF mode | ICC2 | VB = 3.6 V<br>NRST = High | — | 35 | 60 | μA | — |
| Current consumption (3) at VB through mode | ICC3 | VB = 4.6 V<br>NRST = High<br>VB through mode<br>$I_{CPOUT}$ = 0 mA<br>LED = current 0 mA setting | — | 0.26 | 0.52 | mA | — |
| Current consumption (4) at charge pump 1.5× (600 kHz operation) | ICC4 | VB = 3.1 V<br>NRST = High<br>Charge Pump ON,<br>1.5×, 600 kHz operation mode<br>LED = current 0 mA setting | — | 1.3 | 2.6 | mA | — |
| Current consumption (5) at charge pump 1.5× (1.2 MHz operation) | ICC5 | VB = 3.1 V<br>NRST = High<br>Charge Pump ON,<br>1.5×, 1.2 MHz operation mode<br>LED = current 0 mA setting | — | 2.3 | 4.6 | mA | — |
| **Internal oscillator** | | | | | | | |
| Oscillation frequency | FDC1 | VB = 3.1 V to 4.6 V | 1.92 | 2.40 | 2.88 | MHz | — |
| **VB through switch** | | | | | | | |
| Resistance at switch ON | RVBS | VB = 4.5 V<br>$I_{CPOUT}$ = – 30 mA<br>RVBS = ($V_{VB}$ – $V_{CPOUT}$) / 30 mA | — | 1.0 | 2.0 | Ω | — |
| **SCAN switch** | | | | | | | |
| Resistance at switch ON | RSCAN | CPOUT = 4.5 V<br>$I_{Y1}$ to $I_{Y4}$ = 20 mA | — | 1.6 | 3.0 | Ω | — |



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## ELECTRICAL CHARACTERISTICS (continued)

VB = 3.6 V, VDD = 1.85 V

Note) $T_a$ = 25 °C ± 2 °C unless otherwise specified.

| Parameter | Symbol | Condition | Limits | | | Unit | Note |
|---|---|---|---|---|---|---|---|
| | | | Min | Typ | Max | | |
| **Current regulator (matrix)** | | | | | | | |
| Output current (1) | IMX1 | At 25.50 mA setting<br>$V_{X1}$ to $V_{X3}$ = 1 V<br>IMX1 = $I_{X1}$ to $I_{X3}$ | 24.22 | 25.50 | 26.78 | mA | *1 |
| Output current (2) | IMX2 | At 1 mA setting<br>$V_{X1}$ to $V_{X3}$ = 1 V<br>IMX2 = $I_{X1}$ to $I_{X3}$ | 0.95 | 1.00 | 1.05 | mA | *1 |
| Current step | IMXSTEP | IMAX[2:0] = 011 setting | 0 | 100 | 200 | µA | — |
| Off leak current | IMXOFF | OFF setting<br>$V_{X1}$ to $V_{X3}$ = 4.5 V<br>IMXOFF = $I_{X1}$ to $I_{X3}$ | — | — | 1 | µA | — |
| Error between channels | IMXCH | At 12.8 mA setting<br>Current error between each channel and the median of X1 to 3 | – 5 | — | 5 | % | — |
| **Overvoltage detection** | | | | | | | |
| Overvoltage detection voltage | VOV | Charge pump DC/DC overvoltage detection | 5.3 | 5.5 | 5.7 | V | — |
| **Step-up mode switch of charge pump** | | | | | | | |
| Step-up mode switch voltage of charge pump | VLD1 | X1 to 3 pin voltage at the time when the step-up mode switch of charge pump changes | — | 0.35 | 0.40 | V | — |
| **Minimum voltage at which LED driver can keep constant current value** | | | | | | | |
| Minimum voltage at which LED driver can keep constant current value | VLD2 | IMAX[2:0] = 011,<br>95% LED current value at the time when X1 to 3 pin voltage is set to 1V.<br>Minimum value of X1 to 3 pin voltage | — | 0.20 | 0.35 | V | — |

Note)*1 : The specified values are the values in case that a recommended component (ERJ2RHD393X) is connected to IREF pin.



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## ELECTRICAL CHARACTERISTICS (continued)

VB = 3.6 V, VDD = 1.85 V

Note) $T_a$ = 25 °C ± 2 °C unless otherwise specified.

| Parameter | Symbol | Condition | Limits | | | Unit | Note |
|---|---|---|---|---|---|---|---|
| | | | Min | Typ | Max | | |
| **SLASEL** | | | | | | | |
| High-level input voltage range | VIH1 | High-level recognition voltage | 0.7 × VDD | — | VDD + 0.3 | V | — |
| Low-level input voltage range | VIL1 | Low-level recognition voltage | –0.3 | — | 0.3 × VDD | V | — |
| High-level input current | IIH1 | $V_{SLASEL}$ = 3.6 V | — | 0 | 1 | µA | — |
| Low-level input current | IIL1 | $V_{SLASEL}$ = 0 V | — | 0 | 1 | µA | — |
| **CLKIO** | | | | | | | |
| High-level input voltage range | VIH2 | High-level recognition voltage (at external clock input mode) | 0.7 × VDD | — | VDD + 0.3 | V | — |
| Low-level input voltage range | VIL2 | Low-level recognition voltage (at external clock input mode) | –0.3 | — | 0.3 × VDD | V | — |
| Pin pull-down resistance | RPD2 | — | 0.4 | 0.8 | 1.6 | MΩ | — |
| High-level input voltage | VOH2 | $I_{CLKIO}$ = –1mA (at external clock output mode) | 0.8 × VDD | — | VDD + 0.3 | V | — |
| Low-level input voltage | VOL2 | $I_{CLKIO}$ = 1mA (at external clock output mode) | –0.3 | — | 0.2 × VDD | V | — |
| **NRST** | | | | | | | |
| High-level input voltage range | VIH3 | High-level recognition voltage | 1.5 | — | VB + 0.3 | V | — |
| Low-level input voltage range | VIL3 | Low-level recognition voltage | –0.3 | — | 0.6 | V | — |
| High-level input current | IIH3 | $V_{NRST}$ = 3.6 V | — | 0 | 1 | µA | — |
| Low-level input current | IIL3 | $V_{NRST}$ = 0 V | — | 0 | 1 | µA | — |
| **INT** | | | | | | | |
| ON resistance | RINTON | $I_{INT}$ = 5 mA | — | — | 50 | Ω | — |



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## ELECTRICAL CHARACTERISTICS (continued)

VB = 3.6 V, VDD = 1.85 V

Note) $T_a$ = 25 °C ± 2 °C unless otherwise specified.

| Parameter | Symbol | Condition | Limits | | | Unit | Note |
|---|---|---|---|---|---|---|---|
| | | | Min | Typ | Max | | |
| **I²C bus (Internal I/O stage characteristics)** | | | | | | | |
| Low-level input voltage | VIH4 | Voltage which recognized that SDA and SCL are Low-level | 0.7 × VDD | — | VDD + 0.5, 6.0 | V | *2,3 |
| High-level input voltage | VIL4 | Voltage which recognized that SDA and SCL are High-level | — | — | 0.3 × VDD | V | *3 |
| Low-level output voltage 1 | VOL41 | VDD > 2 V<br>$I_{SDA}$ = 3 mA | 0 | — | 0.4 | V | — |
| Low-level output voltage 2 | VOL42 | VDD < 2 V<br>$I_{SDA}$ = 3 mA | 0 | — | 0.2 × VDD | V | — |
| Input current each I/O pin | Ii | $V_{SCL}$,$V_{SDA}$ = 0.17 V ~ 2.88 V | –10 | 0 | 10 | µA | — |
| SCL clock frequency | $f_{SCL}$ | — | — | — | 400 | kHz | — |
| **I²C bus (Internal I/O stage characteristics)** | | | | | | | |
| Hysteresis of Schmitt trigger input 1 | Vhys1 | Hysteresis of SDA, SCL<br>VDD > 2 V | 0.05 × VDD | — | — | V | *4<br>*5 |
| Hysteresis of Schmitt trigger input 2 | Vhys2 | Hysteresis of SDA, SCL<br>VDD < 2 V | 0.1 × VDD | — | — | V | *4<br>*5 |
| Output fall time from $V_{IHmin}$ to $V_{ILmax}$ | Tof | Bus capacitance : 10 pF to 400pF<br>$I_P \leq 6$ mA ($V_{OLmax}$ = 0.6 V)<br>$I_P$ : Max. sink current | 20 + 0.1×$C_b$ | — | 250 | ns | *4<br>*5 |
| Pulse width of spikes which must be suppressed by the input filter | Tsp | — | 0 | — | 50 | ns | *4<br>*5 |
| Capacitance for each I/O pin | Ci | — | — | — | 10 | pF | *4<br>*5 |

Note) *2 : The maximum value of High-level input voltage range is the voltage which is the lower of (VDD + 0.5 V) or 6.0 V.

*3 : The input threshold voltage of I²C bus (Vth) is linked to VDD (I²C bus I/O stage supply voltage).
In case the pull-up voltage is not VDD, the threshold voltage (Vth) is fixed to ((VDD / 2) ± (Schmitt width) / 2 ) and High-level, Low-level of input voltage are not specified. In this case, pay attention to Low-level (max.) value ($V_{ILMAX}$). It is recommended that the pull-up voltage of I²C bus is set to the I²C bus I/O stage supply voltage (VDD).

*4 : The timing of Fast-mode Plus devices in I2C-bus is specified in Page.19. All values referred to $V_{IHMIN}$ and $V_{ILMAX}$ level.

*5 : These are values checked by design but not production tested.



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## ELECTRICAL CHARACTERISTICS (continued)

VB = 3.6 V, VDD = 1.85 V

Note) $T_a$ = 25 °C ± 2 °C unless otherwise specified.

| Parameter | Symbol | Condition | Limits | | | Unit | Note |
|---|---|---|---|---|---|---|---|
| | | | Min | Typ | Max | | |
| **I²C bus (Bus line specifications)** | | | | | | | |
| Hold time (repeated) START condition | $t_{HD:STA}$ | The first clock pulse is generated after $t_{HD:STA.}$ | 0.6 | — | — | µs | *4 *5 |
| Low period of the SCL clock | $t_{LOW}$ | — | 1.3 | — | — | µs | *4 *5 |
| High period of the SCL clock | $t_{HIGH}$ | — | 0.6 | — | — | µs | *4 *5 |
| Set-up time for a repeat START condition | $t_{SU:STA}$ | — | 0.6 | — | — | µs | *4 *5 |
| Data hold time | $t_{HD:DAT}$ | — | 0 | — | — | µs | *4 *5 |
| Data set-up time | $t_{SU:DAT}$ | — | 100 | — | — | ns | *4 *5 |
| Rise time of both SDA and SCL signals | tr | — | 20 + 0.1×$C_b$ | — | 300 | ns | *4 *5 |
| Fall time of both SDA and SCL signals | $t_f$ | — | 20 + 0.1×$C_b$ | — | 300 | ns | *4 *5 |
| Set-up time of STOP condition | $t_{SU:STO}$ | — | 0.6 | — | — | µs | *4 *5 |
| Bus free time between STOP and START condition | $t_{BUF}$ | — | 1.3 | — | — | µs | *4 *5 |
| Capacitive load for each bus line | $C_b$ | — | — | — | 400 | pF | *4 *5 |
| Data valid time | $t_{VD:DAT}$ | — | — | — | 0.9 | µs | *4 *5 |
| Data valid acknowledge | $t_{VD:ACK}$ | — | — | — | 0.9 | µs | *4 *5 |
| Noise margin at the Low-level for each connected device | $V_{aL}$ | — | 0.1 × VDD | — | — | V | *4 *5 |
| Noise margin at the High-level for each connected device | $V_{aH}$ | — | 0.2 × VDD | — | — | V | *4 *5 |

Note) *4 : The timing of Fast-mode Plus devices in I²C-bus is specified in Page.19. All values referred to $V_{IHMIN}$ and $V_{ILMAX}$ level.
*5 : These are values checked by design but not production tested.



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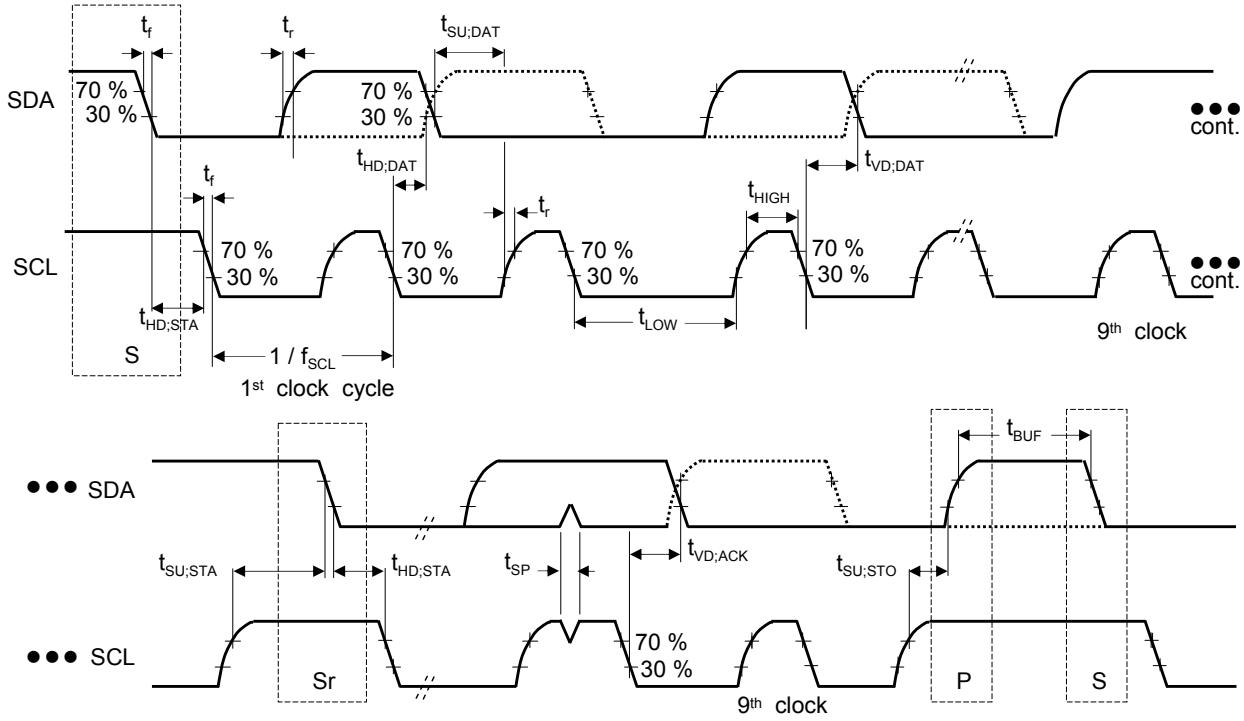
## ELECTRICAL CHARACTERISTICS (continued)

VB = 3.6 V, VDD = 1.85 V

Note) $T_a$ = 25 °C ± 2 °C unless otherwise specified.




$V_{ILMAX}$ = 0.3 $V_{DD}$

$V_{IHMIN}$ = 0.7 $V_{DD}$

S : START condition

Sr : Repeat START condition

P : STOP condition



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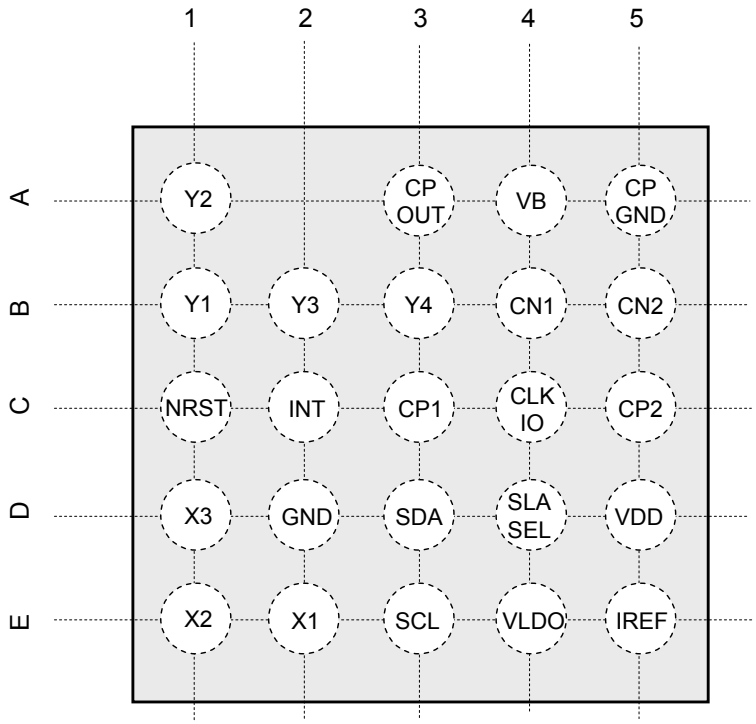
## PIN CONFIGURATION

Top View



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## PIN FUNCTIONS

| Pin No. | Pin name | Type | Description | Pin processing at unused |
|---|---|---|---|---|
| E3(1) | SCL | Input | I²C interface clock input pin | (Must be connected) *1 |
| D3(2) | SDA | Input/Output | I²C interface data input / output pin | (Must be connected) *1 |
| D4(3) | SLASEL | Input | I²C interface slave address selection pin | (Must be connected) *1 |
| D5(4) | VDD | Input | Power supply pin for interface | (Must be connected) *1 |
| C1(5) | NRST | Input | Reset input pin | (Must be connected) *1 |
| C2(6) | INT | Output | Interrupt output pin | Open |
| C4(7) | CLKIO | Input/Output | Clock input/output and LED lighting external synchronous input pin | Open |
| D2(8)<br>A5(22) | GND<br>CPGND | Ground | Ground pin | (Must be connected) *1 |
| E2(9) | X1 | Output | Constant current circuit, PWM control output pin<br>Connected to 1st row of matrix LED | Open |
| E1(10) | X2 | Output | Constant current circuit, PWM control output pin<br>Connected to 2nd row of matrix LED | Open |
| D1(11) | X3 | Output | Constant current circuit, PWM control output pin<br>Connected to 3rd row of matrix LED | Open |
| B1(12) | Y1 | Output | Control switch pin for matrix driver<br>Connected to A column of matrix LED | Open |
| A1(13) | Y2 | Output | Control switch pin for matrix driver<br>Connected to B column of matrix LED | Open |
| B2(14) | Y3 | Output | Control switch pin for matrix driver<br>Connected to C column of matrix LED | Open |
| B3(15) | Y4 | Output | Control switch pin for matrix driver<br>Connected to D column of matrix LED | Open |
| A3(16) | CPOUT | Output | Charge pump output pin / Power supply pin for matrix driver | (Must be connected) *1 |
| A4(17) | VB | Power supply | Power supply pin | (Must be connected) *1 |
| C3(18) | CP1 | Output | Capacitor connection pin for charge pump | Open |
| B4(19) | CN1 | Output | Capacitor connection pin for charge pump | Open |
| C5(20) | CP2 | Output | Capacitor connection pin for charge pump | Open |
| B5(21) | CN2 | Output | Capacitor connection pin for charge pump | Open |
| E5(23) | IREF | Output | Resistor connection pin for constant current setup | (Must be connected) *1 |
| E4(24) | VLDO | Output | Power supply pin for internal circuits | (Must be connected) *1 |

Note) *1 : This terminal is required pin when using this LSI. This terminal must be connected.



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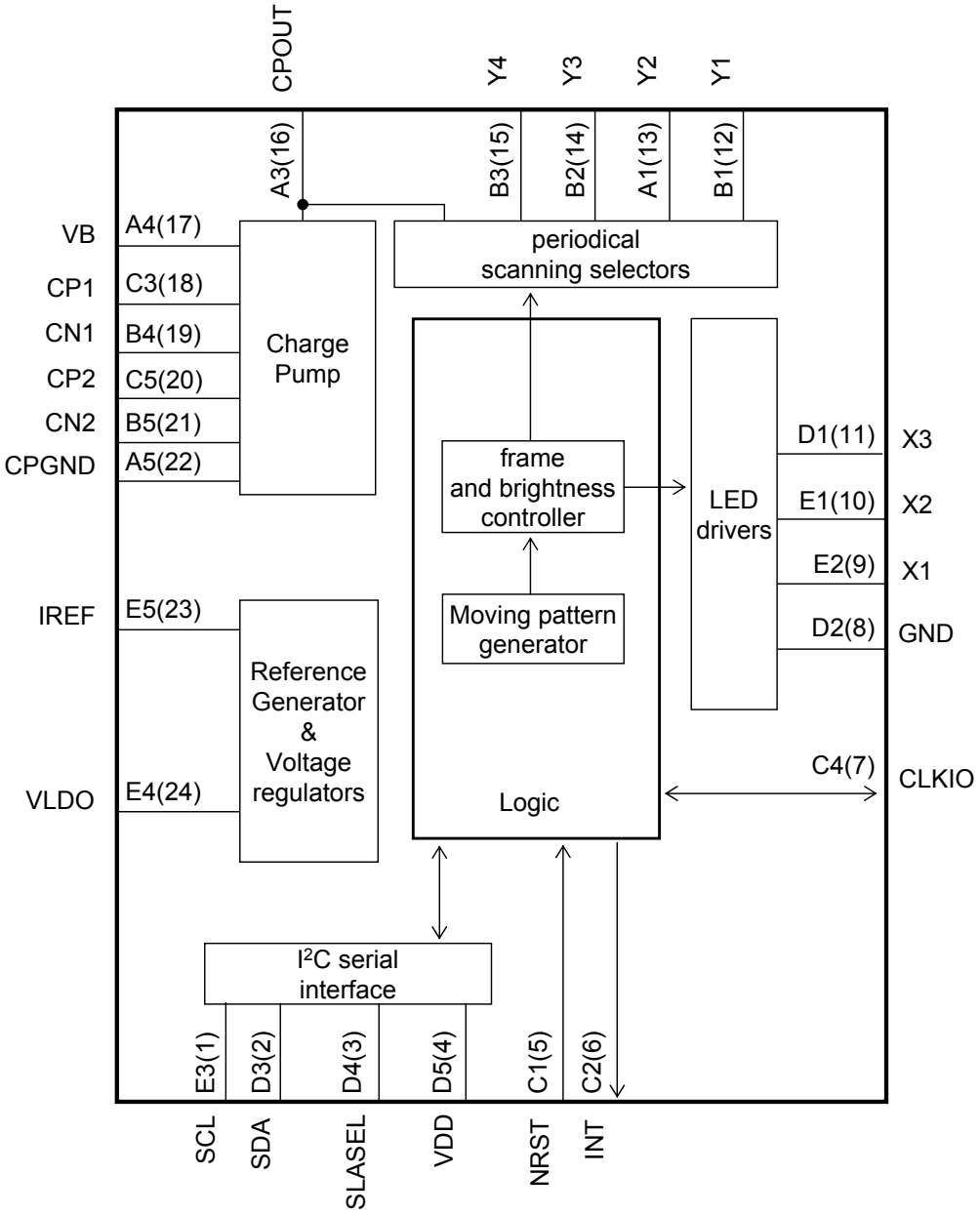
## FUNCTIONAL BLOCK DIAGRAM




Note) This block diagram is for explaining functions.
Part of the block diagram may be omitted, or it may be simplified.



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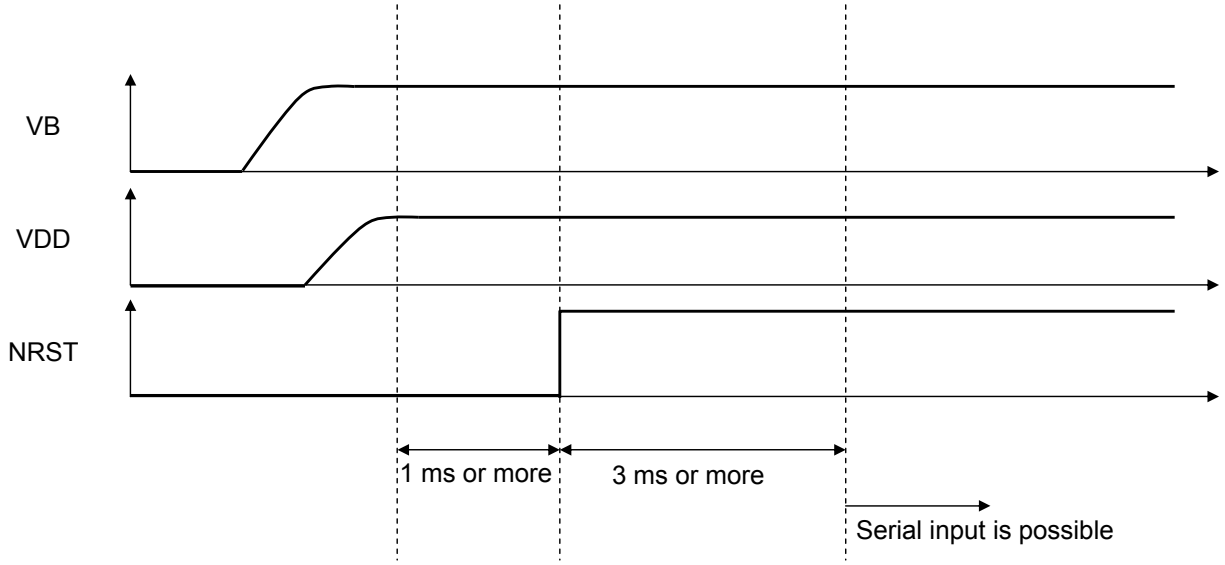
## OPERATION

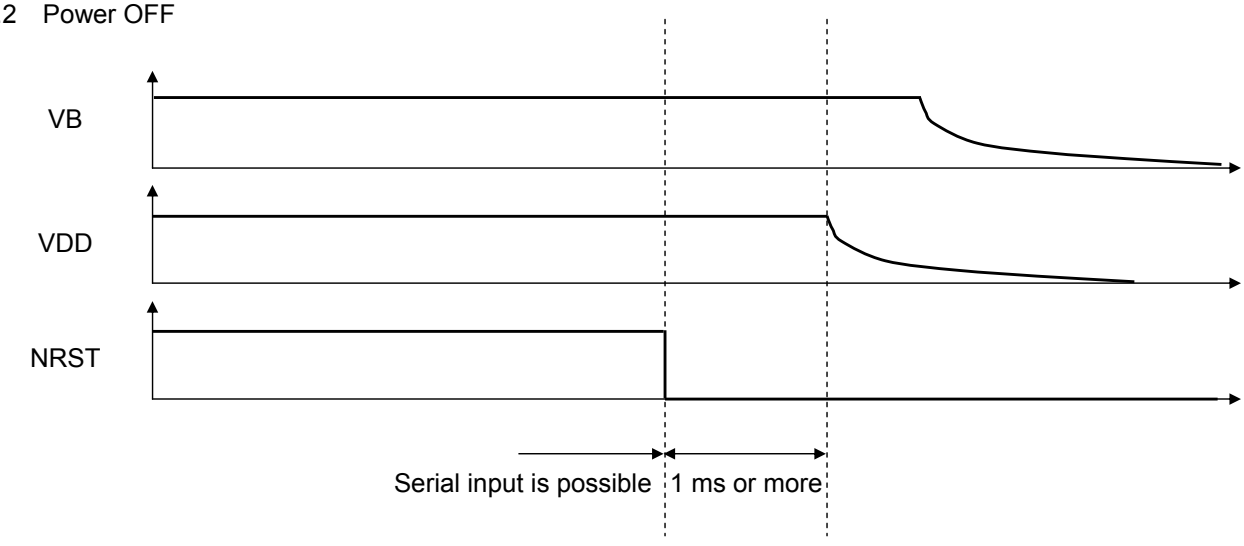
### 1. Power-on / Power-off sequence control

1.1 Power ON




Note) Even if the power-on timing of VDD is the same as the rising timing of VB, there is no problem unless VDD voltage exceeds VB voltage.

1.2 Power OFF




Note) Even if the power-off timing of VDD is the same as the falling timing of VB, there is no problem unless VDD voltage exceeds VB voltage.



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## OPERATION (continued)

### 2. Register map

| Sub Address | R/W | Register Name | Default | Data | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| 00h | W | SRESET | 00h | — | — | — | — | — | — | — | SRESET |
| 01h | R/W | POWERCNT | 00h | — | — | — | CPRET MODE | CPCLK SEL20 | CPCLK SEL15 | OSCEN | CPSW |
| 02h | W | LEDMODE | 00h | INFON | INFTIME[2:0] | | | SEQON | — | SEQNUM[1:0] | |
| 03h | R | STATE CHANGE | 01h | — | — | — | CPERR | CP20 | CP15 | VB | CPOFF |
| 04h | R/W | STATE FORCE | 00h | RETURN VB | ERRMSK | ERRCLR | ERRSTOP | FCP20 | FCP15 | FVB | FCPOFF |
| 05h | R/W | VDETLED CNT | 00h | — | — | — | — | VDETX3 EN | VDETX2 EN | VDETX1 EN | VDETMTX |
| 06h | R/W | MTXON | 60h | IMAX[2:0] | | | MTX DETTM | MTX CPMD | MTXTIME[1:0] | | MTXON |
| 07h | W | IOCNT | 00h | — | CTLGAIN[2:0] | | | — | IOEN | CLKDIR | EXTPWM |
| 08h | W | CONST | 00h | Y4CONST | Y3CONST | Y2CONST | Y1CONST | — | X3CONST | X2CONST | X1CONST |
| 09h | W | INTSEL | 00h | — | RSTCNT | — | — | — | — | — | INTSEL |
| 0Ah | R | INT1 | 00h | SLPINTC2 | SLPINTC1 | SLPINTB3 | SLPINTB2 | SLPINTB1 | SLPINTA3 | SLPINTA2 | SLPINTA1 |
| 0Bh | R | INT2 | 00h | SDET | VBDET | FUNCINT | CNTINT | SLPINTD3 | SLPINTD2 | SLPINTD1 | SLPINTC3 |
| 0Ch | W | INTCLR1 | 00h | SLPINTC2 CLR | SLPINTC1 CLR | SLPINTB3 CLR | SLPINTB2 CLR | SLPINTB1 CLR | SLPINTA3 CLR | SLPINTA2 CLR | SLPINTA1 CLR |
| 0Dh | W | INTCLR2 | 00h | — | VBDET CLR | FUNCINT CLR | CNTINT CLR | SLPINTD3 CLR | SLPINTD2 CLR | SLPINTD1 CLR | SLPINTC3 CLR |
| 0Eh | W | INTMSK1 | 00h | SLPINTC2 MSK | SLPINTC1 MSK | SLPINTB3 MSK | SLPINTB2 MSK | SLPINTB1 MSK | SLPINTA3 MSK | SLPINTA2 MSK | SLPINTA1 MSK |
| 0Fh | R/W | INTMSK2 | 00h | SDET MSK | VBDET MSK | FUNCINT MSK | CNTINT MSK | SLPINTD3 MSK | SLPINTD2 MSK | SLPINTD1 MSK | SLPINTC3 MSK |

Note) Read value of "—"(the blanks) is [0] in the register map.



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## OPERATION (continued)

### 2. Register map (continued)

| Sub Address | R/W | Register Name | Default | Data | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| 10h | R/W | LEDON1 | 00h | — | B3ON | B2ON | B1ON | — | A3ON | A2ON | A1ON |
| 11h | R/W | LEDON2 | 00h | — | D3ON | D2ON | D1ON | — | C3ON | C2ON | C1ON |
| 12h | R/W | FADE1 | 00h | — | FADEB3 | FADEB2 | FADEB1 | — | FADEA3 | FADEA2 | FADEA1 |
| 13h | R/W | FADE2 | 00h | — | FADED3 | FADED2 | FADED1 | — | FADEC3 | FADEC2 | FADEC1 |
| 14h | R/W | FF1 | 00h | — | FFB3 | FFB2 | FFB1 | — | FFA3 | FFA2 | FFA1 |
| 15h | R/W | FF2 | 00h | — | FFD3 | FFD2 | FFD1 | — | FFC3 | FFC2 | FFC1 |
| 16h | R/W | ACT1 | 00h | ACTINV | ACTB3 | ACTB2 | ACTB1 | — | ACTA3 | ACTA2 | ACTA1 |
| 17h | R/W | ACT2 | 00h | ACTON | ACTD3 | ACTD2 | ACTD1 | — | ACTC3 | ACTC2 | ACTC1 |
| 18h | R/W | COUNT1 | 00h | COUNTB1[1:0] | | COUNTA3[1:0] | | COUNTA2[1:0] | | COUNTA1[1:0] | |
| 19h | R/W | COUNT2 | 00h | COUNTC2[1:0] | | COUNTC1[1:0] | | COUNTB3[1:0] | | COUNTB2[1:0] | |
| 1Ah | R/W | COUNT3 | 00h | COUNTD3[1:0] | | COUNTD2[1:0] | | COUNTD1[1:0] | | COUNTC3[1:0] | |
| 1Bh | R | LSIVER | 01h | — | — | — | — | — | LSIVER[2:0] | | |

Note) Read value of "—"(the blanks) is [0] in the register map.



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## OPERATION (continued)

### 2. Register map (continued)

| Sub Address | R/W | Register Name | Default | Data | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| 20h | R/W | SEQA1 | 00h | — | — | — | — | SEQA14 | SEQA13 | SEQA12 | SEQA11 |
| 21h | R/W | SEQA2 | 00h | — | — | — | — | SEQA24 | SEQA23 | SEQA22 | SEQA21 |
| 22h | R/W | SEQA3 | 00h | — | — | — | — | SEQA34 | SEQA33 | SEQA32 | SEQA31 |
| 23h | R/W | SEQB1 | 00h | — | — | — | — | SEQB14 | SEQB13 | SEQB12 | SEQB11 |
| 24h | R/W | SEQB2 | 00h | — | — | — | — | SEQB24 | SEQB23 | SEQB22 | SEQB21 |
| 25h | R/W | SEQB3 | 00h | — | — | — | — | SEQB34 | SEQB33 | SEQB32 | SEQB31 |
| 26h | R/W | SEQC1 | 00h | — | — | — | — | SEQC14 | SEQC13 | SEQC12 | SEQC11 |
| 27h | R/W | SEQC2 | 00h | — | — | — | — | SEQC24 | SEQC23 | SEQC22 | SEQC21 |
| 28h | R/W | SEQC3 | 00h | — | — | — | — | SEQC34 | SEQC33 | SEQC32 | SEQC31 |
| 29h | R/W | SEQD1 | 00h | — | — | — | — | SEQD14 | SEQD13 | SEQD12 | SEQD11 |
| 2Ah | R/W | SEQD2 | 00h | — | — | — | — | SEQD24 | SEQD23 | SEQD22 | SEQD21 |
| 2Bh | R/W | SEQD3 | 00h | — | — | — | — | SEQD34 | SEQD33 | SEQD32 | SEQD31 |

Note) Read value of "—"(the blanks) is [0] in the register map.



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## OPERATION (continued)

### 2. Register map (continued)

| Sub Address | R/W | Register Name | Default | Data | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| 30h | R/W | A1SET1 | 00h | BLA1[7:0] | | | | | | | |
| 31h | R/W | A1SET2 | 00h | TSA1[7:0] | | | | | | | |
| 32h | R/W | A1SET3 | 00h | DLLCA1 | — | — | DLA1[4:0] | | | | |
| 33h | R/W | A2SET1 | 00h | BLA2[7:0] | | | | | | | |
| 34h | R/W | A2SET2 | 00h | TSA2[7:0] | | | | | | | |
| 35h | R/W | A2SET3 | 00h | DLLCA2 | — | — | DLA2[4:0] | | | | |
| 36h | R/W | A3SET1 | 00h | BLA3[7:0] | | | | | | | |
| 37h | R/W | A3SET2 | 00h | TSA3[7:0] | | | | | | | |
| 38h | R/W | A3SET3 | 00h | DLLCA3 | — | — | DLA3[4:0] | | | | |
| 39h | R/W | B1SET1 | 00h | BLB1[7:0] | | | | | | | |
| 3Ah | R/W | B1SET2 | 00h | TSB1[7:0] | | | | | | | |
| 3Bh | R/W | B1SET3 | 00h | DLLCB1 | — | — | DLB1[4:0] | | | | |
| 3Ch | R/W | B2SET1 | 00h | BLB2[7:0] | | | | | | | |
| 3Dh | R/W | B2SET2 | 00h | TSB2[7:0] | | | | | | | |
| 3Eh | R/W | B2SET3 | 00h | DLLCB2 | — | — | DLB2[4:0] | | | | |
| 3Fh | R/W | B3SET1 | 00h | BLB3[7:0] | | | | | | | |
| 40h | R/W | B3SET2 | 00h | TSB3[7:0] | | | | | | | |
| 41h | R/W | B3SET3 | 00h | DLLCB3 | — | — | DLB3[4:0] | | | | |

Note) Read value of "—"(the blanks) is [0] in the register map.



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## OPERATION (continued)

### 2. Register map (continued)

| Sub Address | R/W | Register Name | Default | Data | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| 42h | R/W | C1SET1 | 00h | BLC1[7:0] | | | | | | | |
| 43h | R/W | C1SET2 | 00h | TSC1[7:0] | | | | | | | |
| 44h | R/W | C1SET3 | 00h | DLLCC1 | — | — | DLC1[4:0] | | | | |
| 45h | R/W | C2SET1 | 00h | BLC2[7:0] | | | | | | | |
| 46h | R/W | C2SET2 | 00h | TSC2[7:0] | | | | | | | |
| 47h | R/W | C2SET3 | 00h | DLLCC2 | — | — | DLC2[4:0] | | | | |
| 48h | R/W | C3SET1 | 00h | BLC3[7:0] | | | | | | | |
| 49h | R/W | C3SET2 | 00h | TSC3[7:0] | | | | | | | |
| 4Ah | R/W | C3SET3 | 00h | DLLCC3 | — | — | DLC3[4:0] | | | | |
| 4Bh | R/W | D1SET1 | 00h | BLD1[7:0] | | | | | | | |
| 4Ch | R/W | D1SET2 | 00h | TSD1[7:0] | | | | | | | |
| 4Dh | R/W | D1SET3 | 00h | DLLCD1 | — | — | DLD1[4:0] | | | | |
| 4Eh | R/W | D2SET1 | 00h | BLD2[7:0] | | | | | | | |
| 4Fh | R/W | D2SET2 | 00h | TSD2[7:0] | | | | | | | |
| 50h | R/W | D2SET3 | 00h | DLLCD2 | — | — | DLD2[4:0] | | | | |
| 51h | R/W | D3SET1 | 00h | BLD3[7:0] | | | | | | | |
| 52h | R/W | D3SET2 | 00h | TSD3[7:0] | | | | | | | |
| 53h | R/W | D3SET3 | 00h | DLLCD3 | — | — | DLD3[4:0] | | | | |

Note) Read value of "—"(the blanks) is [0] in the register map.



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## OPERATION (continued)

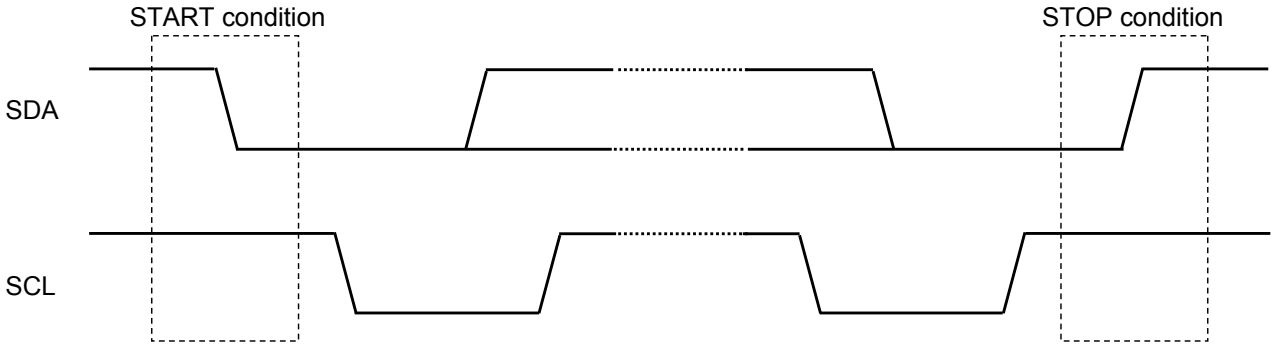
### 3. I²C-bus interface

3.1 Basic Rules

- This LSI, I²C-bus, is designed to correspond to the Standard-mode (100 kbps) and Fast-mode(400 kbps) devices in the version 03 of NXP's specification. However, it does not correspond to the $H_S$-mode (to 3.4 Mbps).
- This LSI will operate as a slave device in the I²C-bus system. This LSI will not operate as a master device.
- The program operation check of this LSI has not been conducted on the multi-master bus system and the mix-speed bus system, yet. The connected confirmation of this LSI to the CBUS receiver also has not been checked. Please confirm with our company if it will be used in these mode systems.
- The I²C is the brand of NXP.

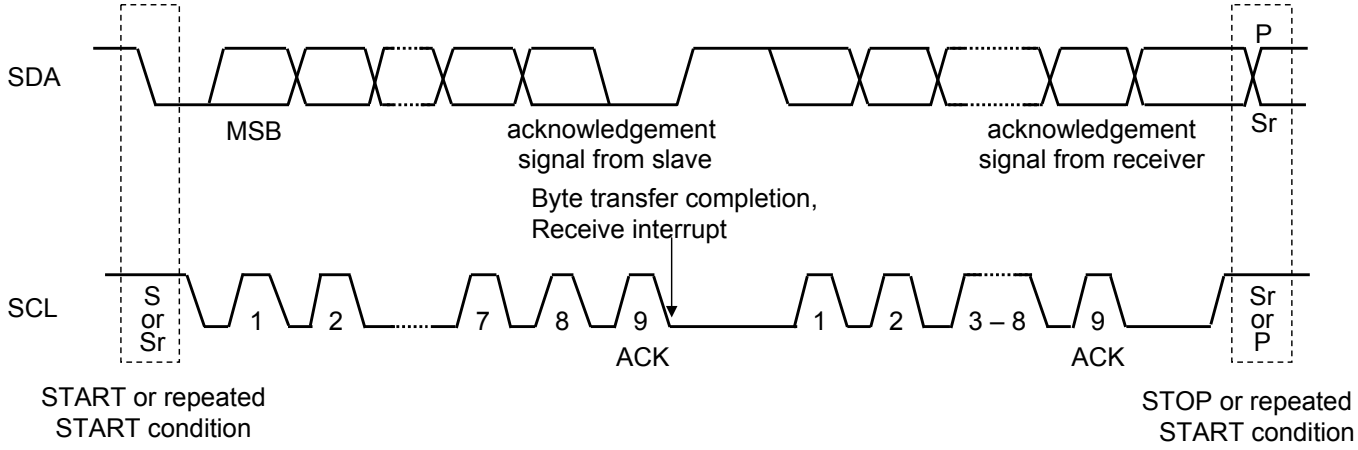
3.2. START and STOP conditions

A High to Low transition on the SDA line while SCL is High is one such unique case. This situation indicates START condition. A Low to High transition on the SDA line while SCL is High defines STOP condition. START and STOP conditions are always generated by the master. After START condition occur, the bus will be busy.
The bus is considered to be free again a certain time after the STOP condition.




3.3. Transferring Data

Every byte put on the SDA line must be 8-bits long. The number of bytes that can be transmitted per transfer is unrestricted. Each byte has to be followed by an acknowledge bit. Data is transferred with the most significant bit (MSB) first.



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## OPERATION (continued)

### 3. I²C-bus interface (continued)

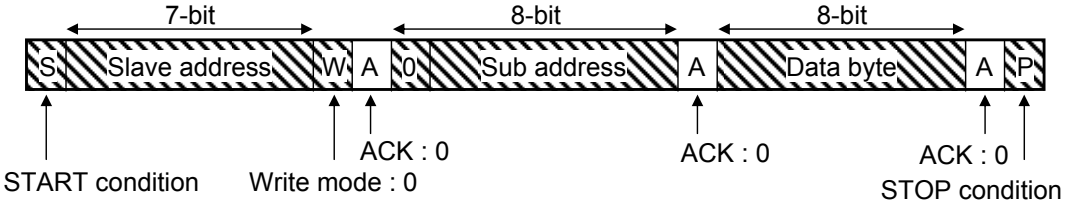
3.4 Data format

It is possible to select slave address by switching SLASEL pin from Low-level to High-level.
The slave address of this LSI is as follows.

| SLASEL | Slave address |
|---|---|
| Low | 0110100X |
| High | 0110101X |

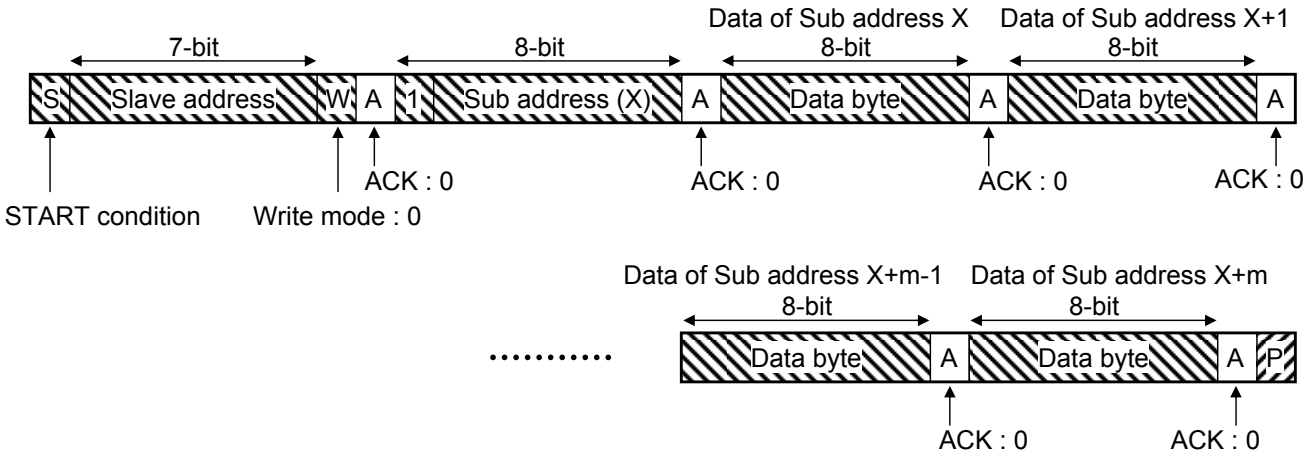
Write mode

When MSB of sub address (8-bit) is "0", the sub address is not incremented automatically.
By transmitting data bytes continuously, the next data bytes are written into the same sub address. by transmitting data byte continuously




Write mode (Auto increment mode)

When MSB of sub address (8-bit) is "1", auto increment mode is defined.
By transmitting data bytes continuously, the data bytes are written into continuous sub address.
The sub address is incremented automatically.




: Data transmission from Master

: Data transmission from Slave



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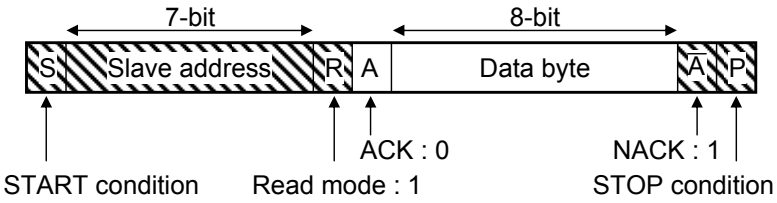
## OPERATION (continued)

### 3. I²C-bus interface (continued)

3.4 Data format (continued)

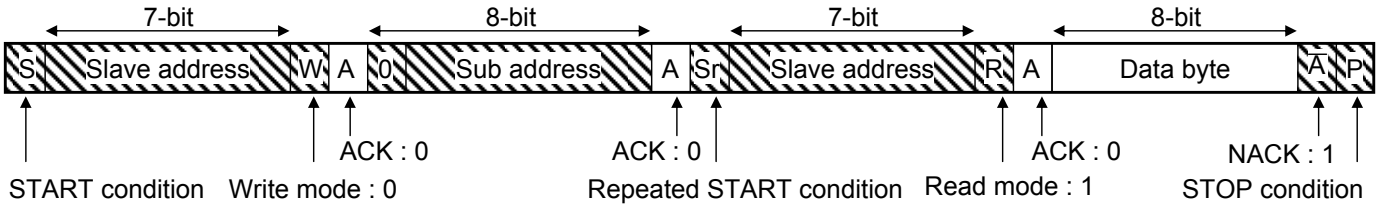
Read mode (In case sub address is not specified)

When the data is read without specifying sub address 8-bit, it is possible to read the value of sub address specified at adjacent write mode.



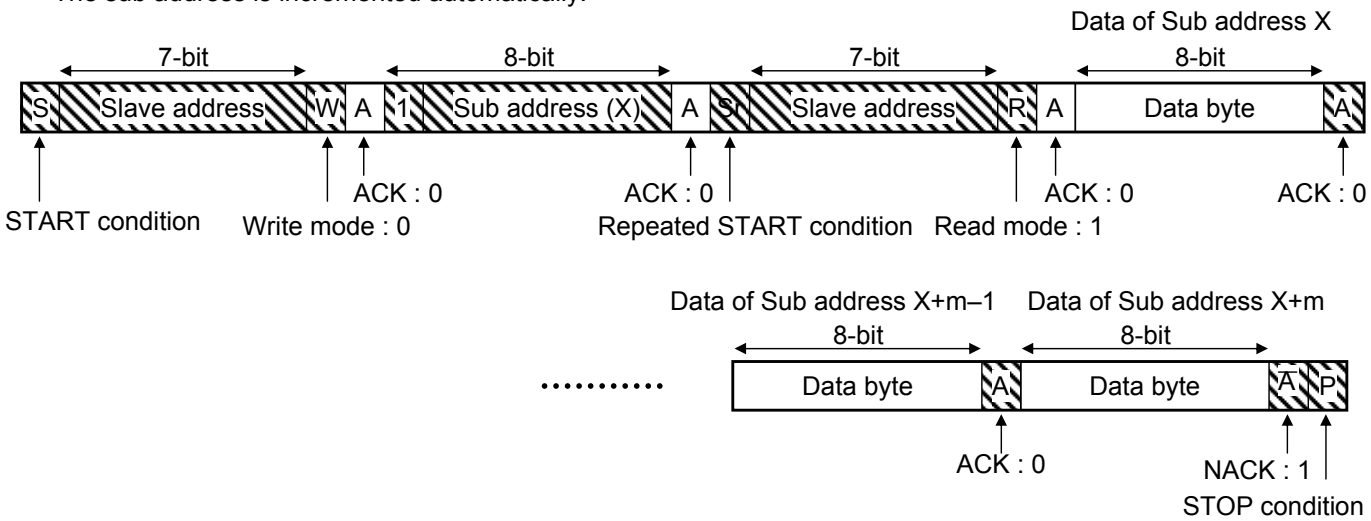

Read mode (In case sub address is specified)

When MSB of sub address (8-bit) is "0", sub address is incremented automatically.
Data byte of specified sub address is read repeatedly continuously until STOP condition is received.




Read mode (Auto increment mode in case sub address is specified)

When MSB of sub address (8-bit) is "1", auto increment mode is specified.
Until STOP condition is received, data byte of sub address incremented automatically by specified sub address can be read continuously
The sub address is incremented automatically.




: Data transmission from Master

: Data transmission from Slave



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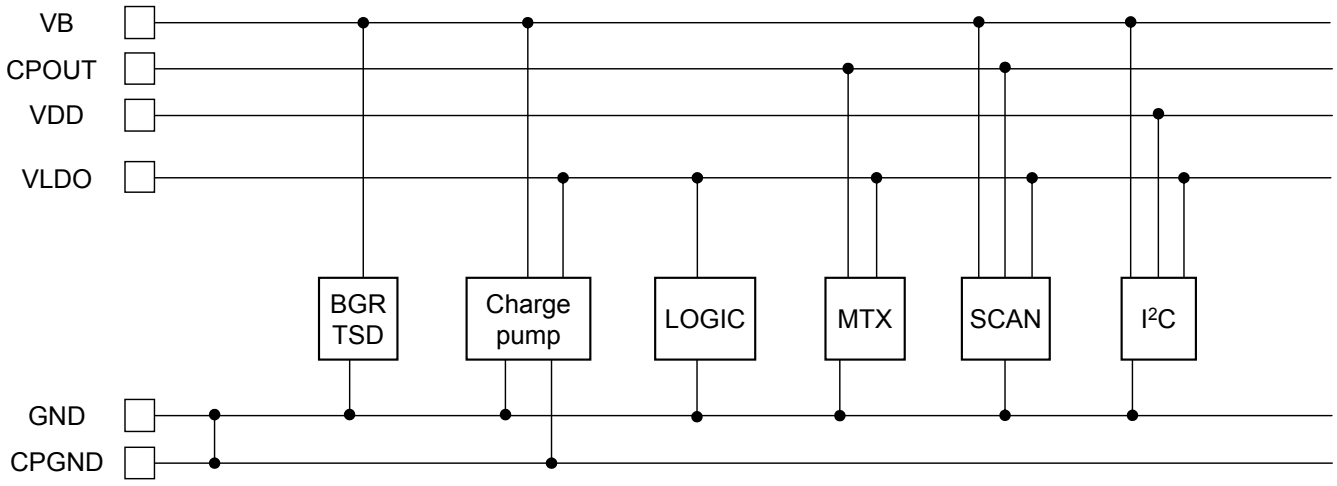
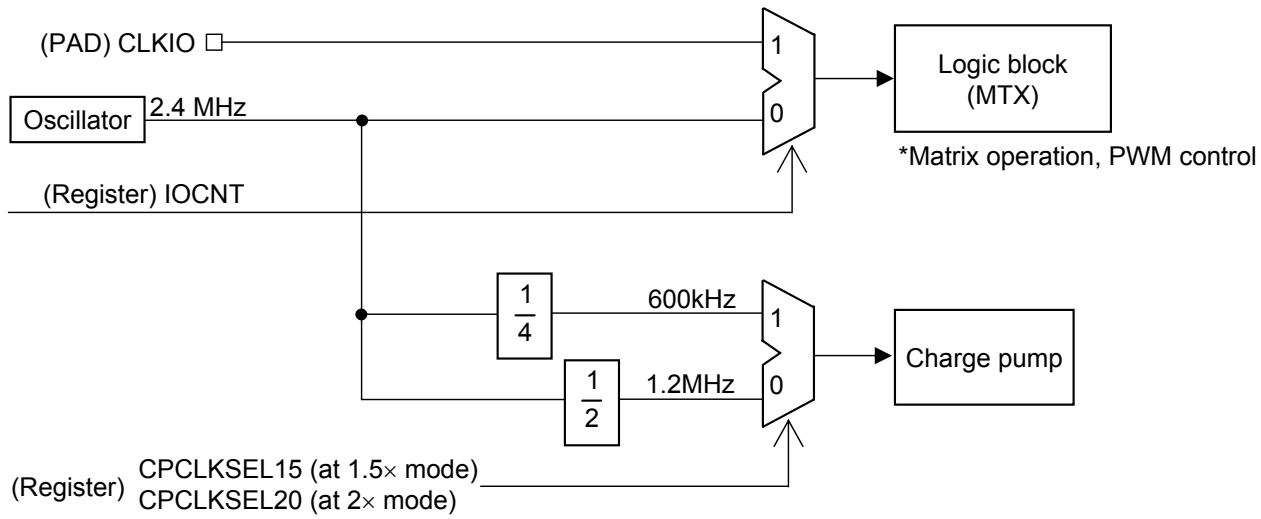
## OPERATION (continued)

### 4. Signal distribution diagram

Distribution diagram of power supply system




Distribution diagram of control / clock system



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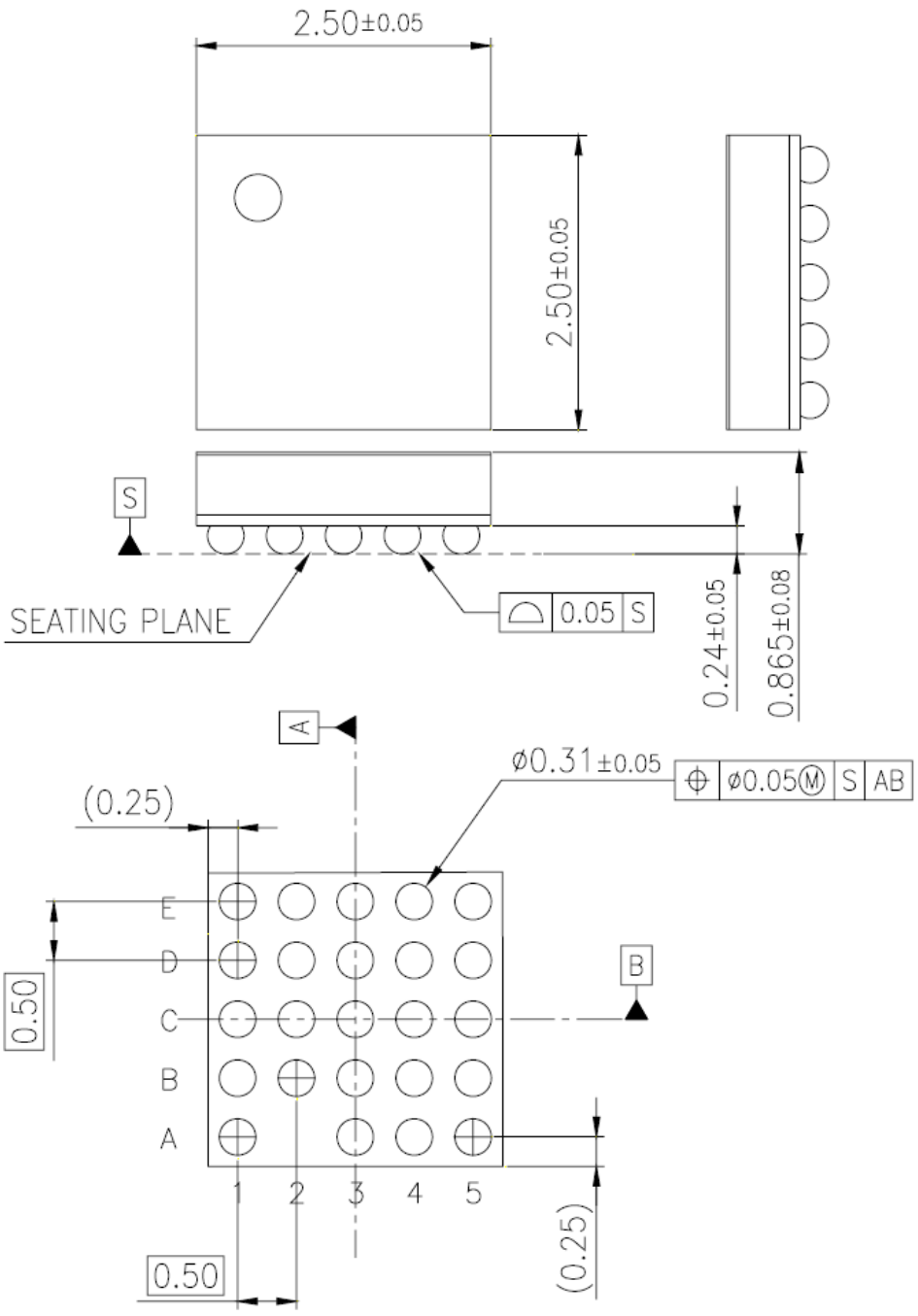
## PACKAGE INFORMATION ( Reference Data )

Package Code : UBGA024-W-2525AEL

Unit:mm




| | | |
|---|---|---|
| Body Material | : | Br / Sb Free Epoxy Resin |
| Reroute Material | : | Cu |
| Bump | : | SnAgCu |



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## IMPORTANT NOTICE

1. When using the LSI for new models, verify the safety including the long-term reliability for each product.
2. When the application system is designed by using this LSI, please confirm the notes in this book.
   Please read the notes to descriptions and the usage notes in the book.
3. This LSI is intended to be used for general electronic equipment.
   Consult our sales staff in advance for information on the following applications: Special applications in which exceptional quality and reliability are required, or if the failure or malfunction of this LSI may directly jeopardize life or harm the human body.
   Any applications other than the standard applications intended.
   (1) Space appliance (such as artificial satellite, and rocket)
   (2) Traffic control equipment (such as for automobile, airplane, train, and ship)
   (3) Medical equipment for life support
   (4) Submarine transponder
   (5) Control equipment for power plant
   (6) Disaster prevention and security device
   (7) Weapon
   (8) Others : Applications of which reliability equivalent to (1) to (7) is required
   Our company shall not be held responsible for any damage incurred as a result of or in connection with the LSI being used for any special application, unless our company agrees to the use of such special application.
4. This LSI is neither designed nor intended for use in automotive applications or environments unless the specific product is designated by our company as compliant with the ISO/TS 16949 requirements.
   Our company shall not be held responsible for any damage incurred by customers or any third party as a result of or in connection with the LSI being used in automotive application, unless our company agrees to such application in this book.
5. Please use this product in compliance with all applicable laws and regulations that regulate the inclusion or use of controlled substances, including without limitation, the EU RoHS Directive. Our company shall not be held responsible for any damage incurred as a result of our LSI being used by our customers, not complying with the applicable laws and regulations.
6. Pay attention to the direction of LSI. When mounting it in the wrong direction onto the PCB (printed-circuit-board), it might emit smoke or ignite.
7. Pay attention in the PCB (printed-circuit-board) pattern layout in order to prevent damage due to short circuit between pins. In addition, refer to the Pin Description for the pin configuration.
8. Perform visual inspection on the PCB before applying power, otherwise damage might happen due to problems such as solder-bridge between the pins of the semiconductor device. Also, perform full technical verification on the assembly quality, because the same damage possibly can happen due to conductive substances, such as solder ball, that adhere to the LSI during transportation.
9. Take notice in the use of this product that it might be damaged or occasionally emit smoke when an abnormal state occurs such as output pin-VCC short (Power supply fault), output pin-GND short (Ground fault), or output-to-output-pin short (load short). Safety measures such as installation of fuses are recommended because the extent of the above-mentioned damage and smoke emission will depend on the current capability of the power supply..
10. The protection circuit is for maintaining safety against abnormal operation. Therefore, the protection circuit should not work during normal operation.
    Especially for the thermal protection circuit, if the area of safe operation or the absolute maximum rating is momentarily exceeded due to output pin to VCC short (Power supply fault), or output pin to GND short (Ground fault), the LSI might be damaged before the thermal protection circuit could operate.
11. Unless specified in the product specifications, make sure that negative voltage or excessive voltage are not applied to the pins because the device might be damaged, which could happen due to negative voltage or excessive voltage generated during the ON and OFF timing when the inductive load of a motor coil or actuator coils of optical pick-up is being driven.
12. Verify the risks which might be caused by the malfunctions of external components.
13. Due to the unshielded structure of this LSI, functions and characteristics of the product cannot be guaranteed under the exposure of light. During normal operation or even under testing condition, please ensure that the LSI is not exposed to light.
14. Please ensure that your design does not have metal shield parts touching the chip surface as the surface potential is GND voltage.



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## Request for your special attention and precautions in using the technical information and semiconductors described in this book

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(3) The products described in this book are intended to be used for general applications (such as office equipment, communications equipment, measuring instruments and household appliances), or for specific applications as expressly stated in this book.
Consult our sales staff in advance for information on the following applications:
- Special applications (such as for airplanes, aerospace, automotive equipment, traffic signaling equipment, combustion equipment, life support systems and safety devices) in which exceptional quality and reliability are required, or if the failure or malfunction of the products may directly jeopardize life or harm the human body.

It is to be understood that our company shall not be held responsible for any damage incurred as a result of or in connection with your using the products described in this book for any special application, unless our company agrees to your using the products in this book for any special application.

(4) The products and product specifications described in this book are subject to change without notice for modification and/or improvement. At the final stage of your design, purchasing, or use of the products, therefore, ask for the most up-to-date Product Standards in advance to make sure that the latest specifications satisfy your requirements.

(5) When designing your equipment, comply with the range of absolute maximum rating and the guaranteed operating conditions (operating power supply voltage and operating environment etc.). Especially, please be careful not to exceed the range of absolute maximum rating on the transient state, such as power-on, power-off and mode-switching. Otherwise, we will not be liable for any defect which may arise later in your equipment.
Even when the products are used within the guaranteed values, take into the consideration of incidence of break down and failure mode, possible to occur to semiconductor products. Measures on the systems such as redundant design, arresting the spread of fire or preventing glitch are recommended in order to prevent physical injury, fire, social damages, for example, by using the products.

(6) Comply with the instructions for use in order to prevent breakdown and characteristics change due to external factors (ESD, EOS, thermal stress and mechanical stress) at the time of handling, mounting or at customer's process. When using products for which damp-proof packing is required, satisfy the conditions, such as shelf life and the elapsed time since first opening the packages.



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