Description:
The NTE4584B is a Hex Schmitt Trigger in a 14–Lead DIP type package constructed with MOS P–Channel and N–Channel enhancement mode devices in a single monolithic structure. This device finds primary use where low power dissipation and/or high noise immunity is desired. The NTE4584B may be used in place of the NTE4069 hex inverter for enhanced noise immunity to “square up” slowly changing waveforms.

Features:
- Supply Voltage Range = 3Vdc to 18Vdc
- Capable of Driving Two Low–Power TTL Loads or One Low–Power Schottky TTL Load Over the Rated Temperature Range
- Double Diode Protection on All Inputs
- Can Be Used to Replace NTE4069

Absolute Maximum Ratings: (Voltages Referenced to VSS, Note 1)
- DC Supply Voltage Range, VDD ............................................ –0.5 to +18.0V
- Input Voltage (DC or Transient), Vin ..................................... –0.5 to VDD to +0.5V
- Output Voltage (DC or Transient), Vout .................................. –0.5 to VDD to +0.5V
- Input Current (DC or Transient, Per Pin), Iin ................................ ±10mA
- Output Current (DC or Transient, Per Pin), Iout ................................ ±10mA
- Power Dissipation (Per Package), PD ...................................... 500mW
- Temperature Derating (from +65° to +125°C) ................. –7.0mW/°C
- Ambient Temperature Range, TA .................................... –55° to +125°C
- Storage Temperature Range, Tstg .................................. –65° to +150°C
- Lead Temperature (During Soldering, 8sec max), TL .................. +260°C

Note 1. Stresses exceeding Absolute Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommend Operating Conditions may affect device reliability.

This device contain circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation, V_in and V_out should be constrained to the range VSS ≤ (V_in or V_out) ≤ VDD.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either VSS or VDD). Unused outputs must be left open.
**Electrical Characteristics:** (Voltages referenced to VSS, Note 2)

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Symbol</th>
<th>VDD Vdc</th>
<th>-55°C</th>
<th>+25°C</th>
<th>+125°C</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Output Voltage</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>“0” Level</td>
<td>VOL</td>
<td>5.0 − 0.05 − 0</td>
<td>0 0.05 − 0 0.05</td>
<td>− 0.05</td>
<td>Vdc</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>10 − 0.05 − 0</td>
<td>0 0.05 − 0 0.05</td>
<td>− 0.05</td>
<td>Vdc</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>15 − 0.05 − 0</td>
<td>0 0.05 − 0 0.05</td>
<td>− 0.05</td>
<td>Vdc</td>
<td></td>
</tr>
<tr>
<td>“1” Level</td>
<td>VOH</td>
<td>5.0 4.95 4.95</td>
<td>5.0 − 4.95</td>
<td>4.95</td>
<td>− 0.05</td>
<td>Vdc</td>
</tr>
<tr>
<td></td>
<td></td>
<td>10 9.95 9.95</td>
<td>10 − 9.95</td>
<td>9.95</td>
<td>− 0.05</td>
<td>Vdc</td>
</tr>
<tr>
<td></td>
<td></td>
<td>15 14.95 14.95</td>
<td>15 − 14.95</td>
<td>14.95</td>
<td>− 0.05</td>
<td>Vdc</td>
</tr>
<tr>
<td><strong>Output Drive Current</strong></td>
<td>Source</td>
<td>IOH</td>
<td>5.0 − 3.0 − 2.4</td>
<td>− 4.2 − 1.7</td>
<td>− 2.4</td>
<td>mAdc</td>
</tr>
<tr>
<td></td>
<td></td>
<td>5.0 − 0.64 − 0.51</td>
<td>− 0.88 − 0.36</td>
<td>− 2.4</td>
<td>mAdc</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>10 − 1.6 − 1.3</td>
<td>− 2.25 − 0.9</td>
<td>− 2.4</td>
<td>mAdc</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>15 − 4.2 − 3.4</td>
<td>− 8.8 − 2.4</td>
<td>− 2.4</td>
<td>mAdc</td>
<td></td>
</tr>
<tr>
<td></td>
<td>Sink</td>
<td>IOL</td>
<td>5.0 0.64 0.51</td>
<td>0.88 − 0.36</td>
<td>− 3.4</td>
<td>mAdc</td>
</tr>
<tr>
<td></td>
<td></td>
<td>10 1.6 1.3</td>
<td>2.25 − 0.9</td>
<td>− 3.4</td>
<td>mAdc</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>15 4.2 3.4</td>
<td>8.8 − 2.4</td>
<td>− 3.4</td>
<td>mAdc</td>
<td></td>
</tr>
<tr>
<td><strong>Input Current</strong></td>
<td></td>
<td>IIN</td>
<td>15 − 0.1</td>
<td>± 0.00001 − ± 0.1</td>
<td>± 0.1</td>
<td>μAdc</td>
</tr>
<tr>
<td><strong>Input Capacitance (VIN = 0)</strong></td>
<td></td>
<td>Cin</td>
<td>− − −</td>
<td>− 5.0</td>
<td>7.5</td>
<td>− −</td>
</tr>
<tr>
<td><strong>Quiescent Current</strong></td>
<td>(Per Package)</td>
<td>IDD</td>
<td>5.0 − 0.25 − 0</td>
<td>0.005 0.25</td>
<td>7.5</td>
<td>μAdc</td>
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<tr>
<td></td>
<td></td>
<td>10 − 0.5 − 0</td>
<td>0.0010 0.5</td>
<td>− 15</td>
<td>μAdc</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>15 − 1.0 − 0</td>
<td>0.0015 1.0</td>
<td>− 30</td>
<td>μAdc</td>
<td></td>
</tr>
<tr>
<td><strong>Total Supply Current</strong></td>
<td>(Dynamic plus Quiescent, Per Package, CL = 50pF, on All Outputs, All Buffers Switching (Note 3, Note 4))</td>
<td>IT</td>
<td>5.0</td>
<td>1.8μA/kHz f + IDD</td>
<td>μAdc</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>10</td>
<td>3.6μA/kHz f + IDD</td>
<td>μAdc</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>15</td>
<td>5.4μA/kHz f + IDD</td>
<td>μAdc</td>
<td></td>
<td></td>
</tr>
<tr>
<td><strong>Hysteresis Voltage</strong></td>
<td>(Note 5)</td>
<td>VH</td>
<td>5.0 0.27 1.0</td>
<td>0.25 1.0 0.21</td>
<td>1.0</td>
<td>Vdc</td>
</tr>
<tr>
<td></td>
<td></td>
<td>10 0.36 1.3</td>
<td>0.3 1.2 0.25</td>
<td>1.2</td>
<td>Vdc</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>15 0.77 1.7</td>
<td>0.6 1.5 0.50</td>
<td>1.4</td>
<td>Vdc</td>
<td></td>
</tr>
<tr>
<td><strong>Threshold Voltage</strong></td>
<td>Positive Going</td>
<td>V+</td>
<td>5.0 1.9 3.5</td>
<td>1.8 2.7 3.4</td>
<td>3.4</td>
<td>Vdc</td>
</tr>
<tr>
<td></td>
<td></td>
<td>10 3.4 7.0</td>
<td>3.3 5.3 6.9</td>
<td>6.9</td>
<td>Vdc</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>15 5.2 10.6</td>
<td>5.2 8.0 10.5</td>
<td>10.5</td>
<td>Vdc</td>
<td></td>
</tr>
<tr>
<td><strong>Negative Going</strong></td>
<td></td>
<td>V−</td>
<td>5.0 1.6 3.3</td>
<td>1.6 2.1 3.2</td>
<td>3.2</td>
<td>Vdc</td>
</tr>
<tr>
<td></td>
<td></td>
<td>10 3.0 6.7</td>
<td>3.0 4.6 6.7</td>
<td>6.7</td>
<td>Vdc</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>15 4.5 9.7</td>
<td>4.6 6.9 9.8</td>
<td>9.9</td>
<td>Vdc</td>
<td></td>
</tr>
</tbody>
</table>

**Note 2.** Data labeled “Typ” is not to be used for design purposes but is intended as an indication of the device’s potential performance.

**Note 3.** The formulas given are for the typical characteristics only at +25°C.

**Note 4.** To calculate total supply current at loads other than 50pF:

\[ I_T(C_L) = I_T(50pF) + (C_L - 50) \times k \ V_f k \]

where: \( I_T \) is in μA (per package), \( C_L \) in pF, \( V = (V_{DD} - V_{SS}) \) in volts, \( f \) in kHz is input frequency, and \( k = 0.001 \).

**Note 5.** \( V_H = V_{T+} - V_{T−} \) (But maximum variation of \( V_H \) is specified as less than \( V_{T+\max} - V_{T−\min} \)).
**Switching Characteristics:** \( (C_L = 50\,\text{pF}, \, T_A = +25^\circ\text{C}, \, \text{Note 2}) \)

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Symbol</th>
<th>( \text{V_{DD}} \text{ Vdc} )</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>Output Rise and Fall Times</td>
<td>( t_{\text{TLH}}, t_{\text{THL}} )</td>
<td>5.0</td>
<td>–</td>
<td>100</td>
<td>200</td>
<td>ns</td>
</tr>
<tr>
<td></td>
<td></td>
<td>10</td>
<td>–</td>
<td>50</td>
<td>100</td>
<td>ns</td>
</tr>
<tr>
<td></td>
<td></td>
<td>15</td>
<td>–</td>
<td>40</td>
<td>80</td>
<td>ns</td>
</tr>
<tr>
<td>Propagation Delay Time</td>
<td>( t_{\text{PLH}}, t_{\text{PHL}} )</td>
<td>5.0</td>
<td>–</td>
<td>125</td>
<td>250</td>
<td>ns</td>
</tr>
<tr>
<td></td>
<td></td>
<td>10</td>
<td>–</td>
<td>50</td>
<td>100</td>
<td>ns</td>
</tr>
<tr>
<td></td>
<td></td>
<td>15</td>
<td>–</td>
<td>40</td>
<td>80</td>
<td>ns</td>
</tr>
</tbody>
</table>

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Note 3. The formulas given are for the typical characteristics only at +25°C.

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**Logic Diagram**

```
1 2
3 4
5 6
9 8
11 10
13 12
```

\( \text{V_{DD}} = \text{Pin 14} \)
\( \text{V_{SS}} = \text{Pin 7} \)

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**Pin Connection Diagram**

```
A 1
G = A 2
B 3
H = B 4
C 5
I = C 6
V_{SS} 7
14 \text{V_{DD}}
13 F
12 L = F
11 E
10 K = E
9 D
8 J = \overline{D}
```