

AN10800

Using the BLF578 in the 88 MHz to 108 MHz FM band

Rev. 01 — 13 October 2009

Application note

Document information

Info	Content
Keywords	BLF578, performance, high-efficiency tuning set-up, high voltage LDMOS, amplifier implementation, Class-C CW, FM band, pulsed power
Abstract	This application note describes the design and the performance of the BLF578 for Class-C CW and FM type applications in the 88 MHz to 108 MHz frequency range. The major aim has been to illustrate tuning set-up performance which targets very high-efficiency operation at reduced output power

Revision history

Rev	Date	Description
01	20091013	Initial version

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1. Introduction

The BLF578 is a new, 50 V, push-pull transistor using NXP Semiconductors' 6th generation of high voltage LDMOS technology. The two push-pull sections of the device are completely independent of each other inside the package. The gates of the device are internally protected by the integrated ElectroStatic Discharge (ESD) diode.

The device is unmatched and is designed for use in applications below 600 MHz where very high power and efficiency are required. Typical applications are FM/VHF broadcast, laser or Industrial Scientific and Medical (ISM) applications.

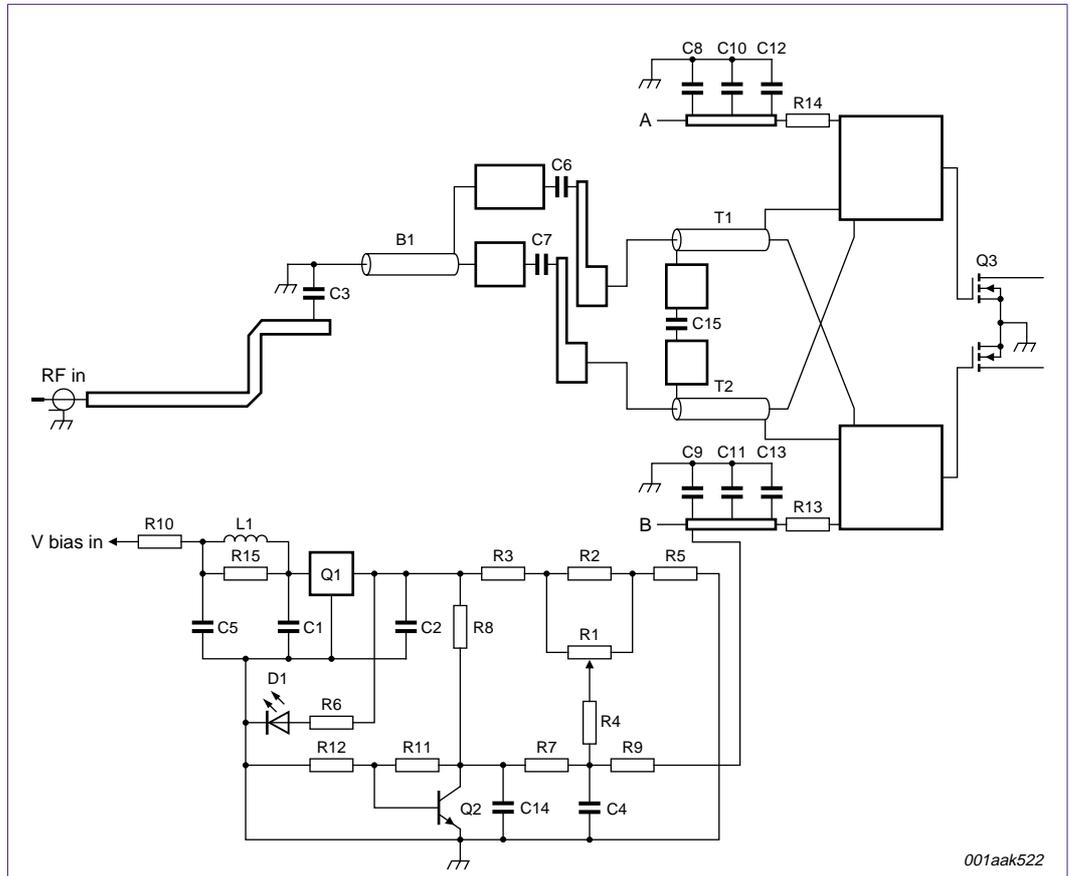
Great care has been taken during the design of the high voltage process to ensure that the device achieves high ruggedness. This is a critical parameter for successful broadcast operations. The device can withstand greater than a 10:1 VSWR for all phase angles at full operating power.

Another design goal was to minimize the size of the application circuit. This is important in that it allows amplifier designers to maximize the power in a given amplifier size. The design highlighted in this application note achieves over 1 kW in the 88 MHz to 108 MHz band in a space smaller than 50.8 mm × 101.6 mm (2 " × 4 "). The circuit only needs to be as wide as the transistor itself, enabling transistor mounting in the final amplifier to be as close as physically possible while still providing adequate room for the circuit implementation.

This application note describes the design and the performance of the BLF578 for Class-C CW and FM type applications in the 88 MHz to 108 MHz frequency band. It must be noted that the device is very powerful and more than 1200 W of pulsed power has been generated at 225 MHz. This application note describes tuning set-up performance which targets very high-efficiency operation at somewhat reduced output powers.

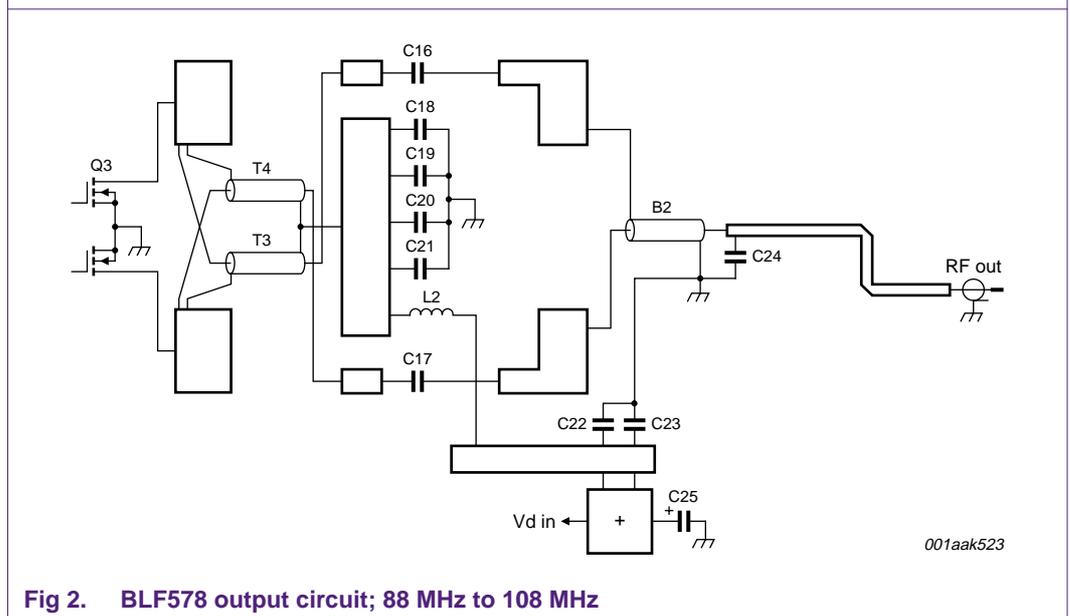
2. Circuit diagrams and PCB layout

2.1 Circuit diagrams



001aak522

Fig 1. BLF578 input circuit; 88 MHz to 108 MHz



001aak523

Fig 2. BLF578 output circuit; 88 MHz to 108 MHz

2.2 Bill Of Materials

Table 1. Bill of materials for BLF578 input and output circuits

PCB material: Taconic RF35; $\epsilon_r = 3.5$; thickness 0.76 mm (30 mil). [Figure 4](#) shows the BLF578 PCB layout.

Designator	Description	Part number	Manufacturer
A/B	connect jumper wire between points A and B	-	-
B1	7.7 " 086-50 semirigid through ferrite ^[1]	BN-61-202	Amidon
B2	6 " 141-50 flexible coax cable	-	-
C1, C2, C14	100 nF ceramic chip capacitor	S0805W104K1HRN-P4	Multicomp
C3	43 pF ceramic chip capacitor	ATC100B430JT500X	American Technical Ceramics
C4, C5, C10, C11	1 μ F ceramic chip capacitor	GRM31MR71H105K88L	MuRata
C6, C7	4700 pF ceramic chip capacitor	ATC700B472JT50X	American Technical Ceramics
C8, C9	10 μ F ceramic chip capacitor	GRM32ER7YA106K88L	MuRata
C12, C13	100 nF ceramic chip capacitor	GRM21BR72A104K	MuRata
C15	620 pF ceramic chip capacitor	ATC100B621JT500X	American Technical Ceramics
C16, C17	390 pF ceramic chip capacitor	ATC100B391JT500X	American Technical Ceramics
C18, C19, C22	100 nF ceramic chip capacitor	GRM32DR72E104KW01L	MuRata
C20, C21, C23	2.2 μ F ceramic chip capacitor	GRM32ER72A22KA35LX	MuRata
C24	18 pF ceramic chip capacitor	ATC100B180JT500X	American Technical Ceramics
C25	1000 μ F, 100 V electrolytic capacitor	EEV-TG1V102M	American Technical Ceramics
D1	0805 Green SMT LED	APT2012CGCK	KingBright
L1	ferroxcube bead	2743019447	Fair Rite
L2	3 turns 14 gauge wire, ID = 0.310 "	-	-
Microstrip	all microstrip sections	[2]	Vishay Dale
Q1	7808 voltage regulator	NJM#78L08UA-ND	NJR
Q2	SMT NPN transistor	PMBT2222	NXP Semiconductors
Q3	BLF578	BLF578	NXP Semiconductors
R1	200 Ω potentiometer	3214W-1-201E	Panasonic
R2, R3	432 Ω resistor	CRCW0805432RFKEA	Bourns
R4	2 k Ω resistor	CRCW08052K00FKTA	Vishay Dale
R5	75 Ω resistor	CRCW080575R0FKTA	Vishay Dale
R6, R8	1.1 k Ω resistor	CRCW08051K10FKEA	Vishay Dale
R7	11 k Ω resistor	CRCW080511K0FKEA	Vishay Dale
R9	5.1 Ω resistor	CRCW08055R1FKEA	Vishay Dale
R10	499 Ω , 1/4 W resistor	CRCW2010499RFKEF	Vishay Dale
R11	5.1 k Ω resistor	CRCW08055K10FKTA	Vishay Dale
R12	910 Ω resistor	CRCW0805909RFKTA	Vishay Dale
R13, R14, R15	9.1 Ω resistor	CRCW08059R09FKEA	Vishay Dale
T1, T2	2.5 " 062-18 semirigid through ferrite ^[1]	BN-61-202	Amidon
T3, T4	4 " 120-22 flexible coax cable	-	-

[1] The semirigid cable length is defined in [Figure 3](#).

[2] Contact your local NXP Semiconductors' salesperson for copies of the PCB layout files.

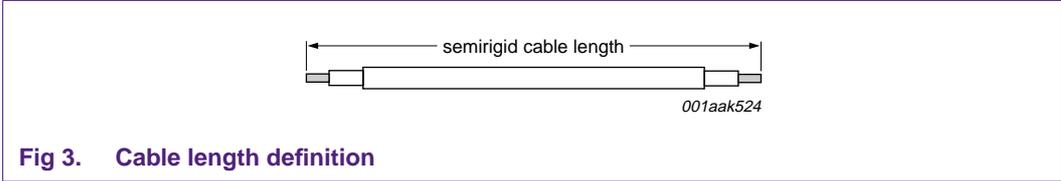


Fig 3. Cable length definition

2.3 BLF578 PCB layout

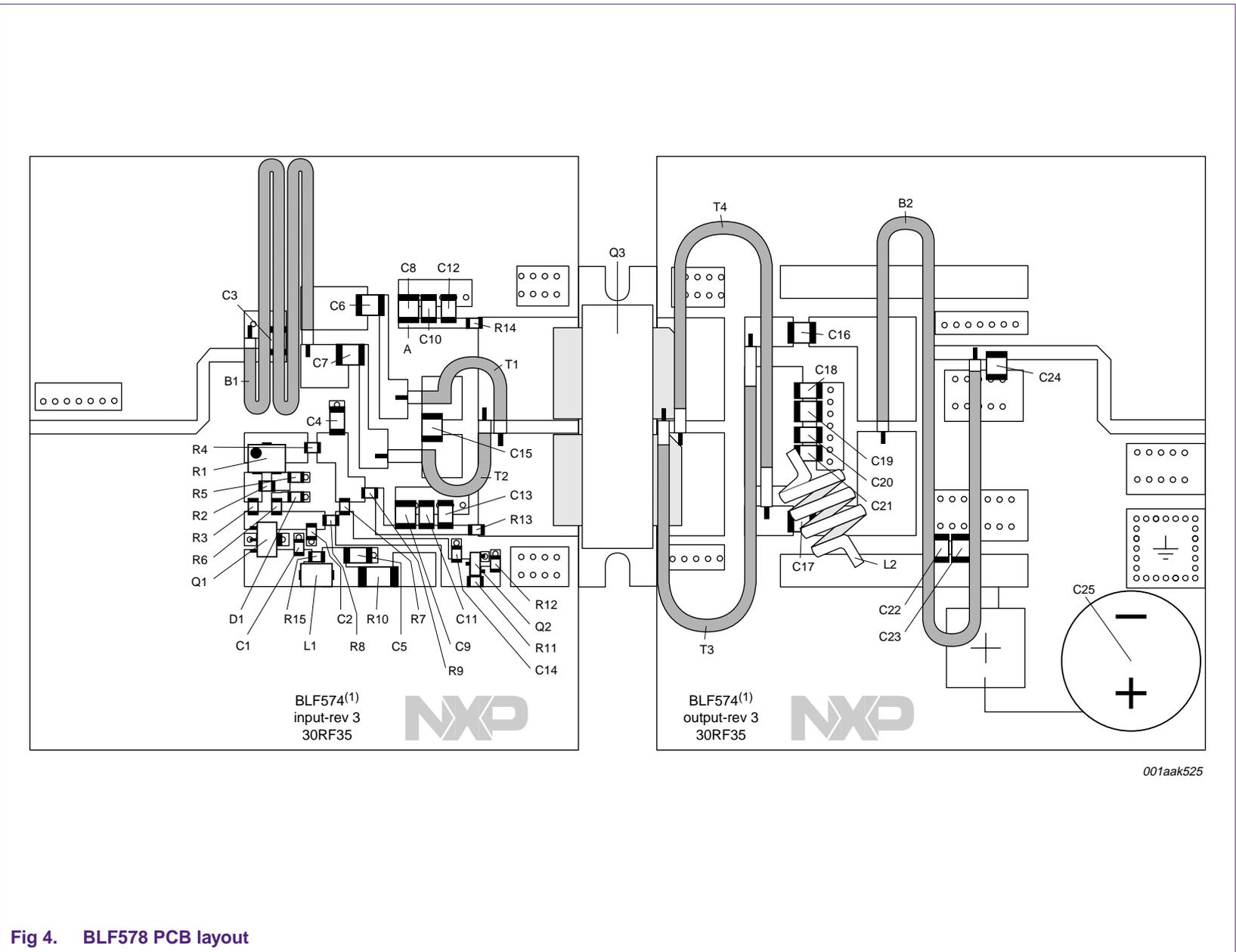


Fig 4. BLF578 PCB layout

2.4 PCB form factor

Care has been taken to minimize board space for the design. [Figure 5](#) shows how 1000 W can be generated in a space only as wide as the transistor itself.



Fig 5. Photograph of the BLF578 circuit board

3. Amplifier design

3.1 Mounting considerations

To ensure good thermal contact, a heatsink compound (such as Dow Corning 340) should be used when mounting the BLF578 in the SOT539A package to the heatsink. Improved thermal contact is obtainable when the devices are soldered on to the heatsink. This lowers the junction temperature at high operating power and results in slightly better performance.

When greasing the part down, care must be taken to ensure that the amount of grease is kept to an absolute minimum. The NXP Semiconductors' website can be consulted for application notes on the recommended mounting procedure for this type of device.

3.2 Bias circuit

A temperature compensated bias circuit is used and comprises the following:

An 8 V voltage regulator (Q1) supplies the bias circuit. The temperature sensor (Q2) must be mounted in good thermal contact with the device under test (Q3). The quiescent current is set using a potentiometer (R1). The gate voltage correction is approximately $-4.8 \text{ mV}/^\circ\text{C}$ to $-5.0 \text{ mV}/^\circ\text{C}$. The V_{GS} range is also reduced using a resistor (R2).

The $-2.2 \text{ mV}/^\circ\text{C}$ at its base is generated by Q2. This is then multiplied up by the R11 : R12 ratio for a temperature slope (i.e. approximately $-15 \text{ mV}/^\circ\text{C}$). The multiplication function provided by the transistor is the reason it is used rather than a diode. A portion of the $-15 \text{ mV}/^\circ\text{C}$ is summed into the potentiometer (R1).

The amount of temperature compensation is set by resistor R4. The ideal value proved to be 2 k Ω . The values of R9, R13 and R14 are not important for temperature compensation. However, they are used for baseband stability and to improve IMD asymmetry at lower power levels.

3.3 Amplifier alignment

There are several points in the circuit that allow performance parameters to be readily traded off against one another. In general, the following areas of the circuit have the most impact on the circuit performance.

Effect of changing the output capacitors (C16 and C17):

- This is a key tuning point in the circuit. This point has the strongest influence on the trade-off between efficiency and output power at 1 dB gain compression ($P_{L(1dB)}$).

Changing the frequency band:

- A demonstration was done with the BLF578, but the frequency of operation was higher, at 128 MHz. [Table 2](#) shows how the capacitors and baluns were modified to raise the frequency. This table can be used as a guide if the desired frequency band were to be lower as well, by making equivalent changes in the opposite direction.

Table 2. Increasing the operating frequency

Component	88 MHz to 108 MHz	128 MHz
Capacitors connected to the FET drains	0 pF	18 pF
C16, C17	390 pF	180 pF with 100 pF
Capacitors connected to output balun, C24	18 pF	20 pF
Output balun, B2	152.4 mm (6 ") 50 Ω	101.6 mm (4 ") 50 Ω

The high efficiency tuning set-up can be traded off against the $P_{L(1dB)}$ tuning set-up as indicated in [Table 3](#).

Table 3. High-efficiency tuning set-up and $P_{L(1dB)}$ tuning set-up trade-off

Component	High-efficiency tuning set-up	High $P_{L(1dB)}$ tuning set-up
Capacitors connected to the FET drains	24 pF	not placed
C24	24 pF	18 pF

Table 4. Tuned efficiency and power performance

Parameter	Frequency (MHz)	43 V ^[1]		50 V ^[2]	
		High-efficiency tuning set-up	High P _{L(1dB)} tuning set-up	High-efficiency tuning set-up	High P _{L(1dB)} tuning set-up
Compression at 800 W	88	3.3 dB	2.6 dB	-	-
	98	2.5 dB	1.8 dB	-	-
	108	2.0 dB	1.5 dB	-	-
Efficiency at 800 W	88	80 %	78 %	-	-
	98	80 %	77 %	-	-
	108	81 %	78 %	-	-
Compression at 1 kW	88	-	-	2.6 dB	1.0 dB
	98	-	-	1.2 dB	0.5 dB
	108	-	-	0.8 dB	0.3 dB
Efficiency at 1 kW	88	-	-	75 %	77 %
	98	-	-	77 %	75 %
	108	-	-	78 %	76 %

[1] In the 43 V case, the high-efficiency tuning set-up gets an extra 3 % efficiency at the expense of between 0.5 dB and 0.7 dB in compression performance.

[2] In the 50 V case, trading in 2 % efficiency lessens the compression by more than 0.5 dB at 1 kW.

4. RF performance characteristics

4.1 Continuous wave

This application explores two possible tuning compromises:

- high-efficiency 43 V, 800 W
- high P_{L(1dB)}, 50 V 1 kW

A summary of the results for these tuning set-ups is shown in [Table 5](#) and [Table 6](#).

Table 5. High-efficiency tuning set-up: 43 V, 800 W

This table summarizes the performance of the high-efficiency tuning set-up at I_{DQ} = 200 mA and T_h = 25 °C.

Frequency (MHz)	P _L (W)	G (dB)	η (%)
88	800	24.1	81
98	800	24.8	80
108	800	25.5	81

Table 6. $P_{L(1dB)}$ tuning set-up: 50 V, 1 kW

This table summarizes the performance of the high $P_{L(1dB)}$ tuning set-up at $I_{Dq} = 50 \text{ mA}$ and $T_h = 25^\circ\text{C}$.

Frequency (MHz)	P_L (W)	G (dB)	η (%)
88	1000	26.5	77
98	1000	26.8	75
108	1000	26.3	75.5

4.2 Continuous wave graphics

Figure 6 to Figure 11 illustrate the behavior and performance of the different tuning set-ups at the various supply voltages. The boards are tuned over a range of output powers and the relevant performance measurements are shown over the power range at low, middle and high frequencies.

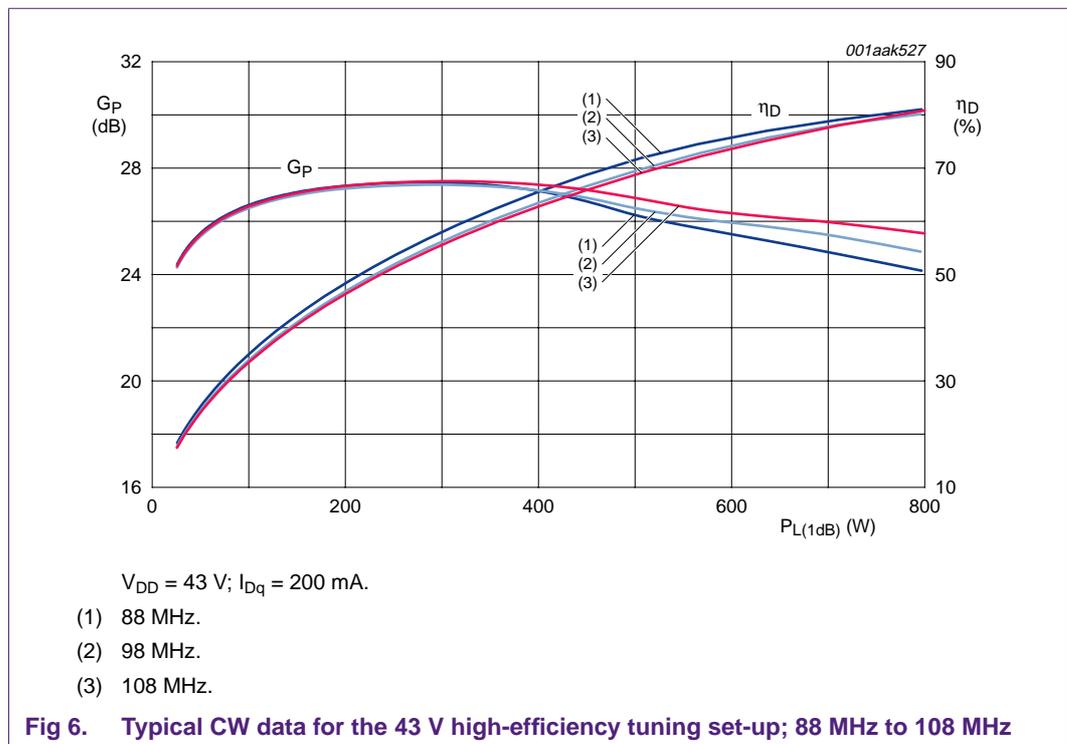


Figure 7 and Figure 8 show the gain and drain efficiency performance differences between the high-efficiency and high $P_{L(1dB)}$ tuning set-ups for the $V_{DD} = 43 \text{ V}$ (bias condition).

The difference in gain and drain efficiency between the two types of tuning set-up for a 50 V supply ($V_{DD} = 50 \text{ V}$) is shown in Figure 9 and Figure 10.

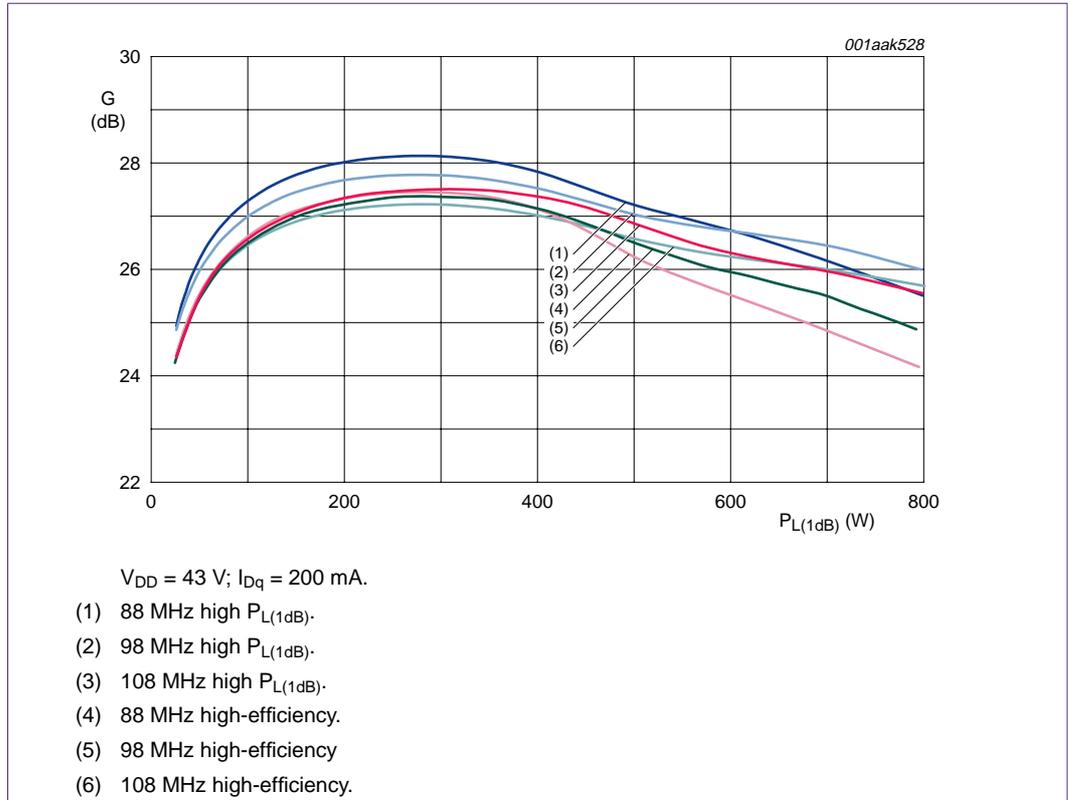


Fig 7. Gain comparison: 43 V, high-efficiency to high $P_{L(1dB)}$ tuning set-up

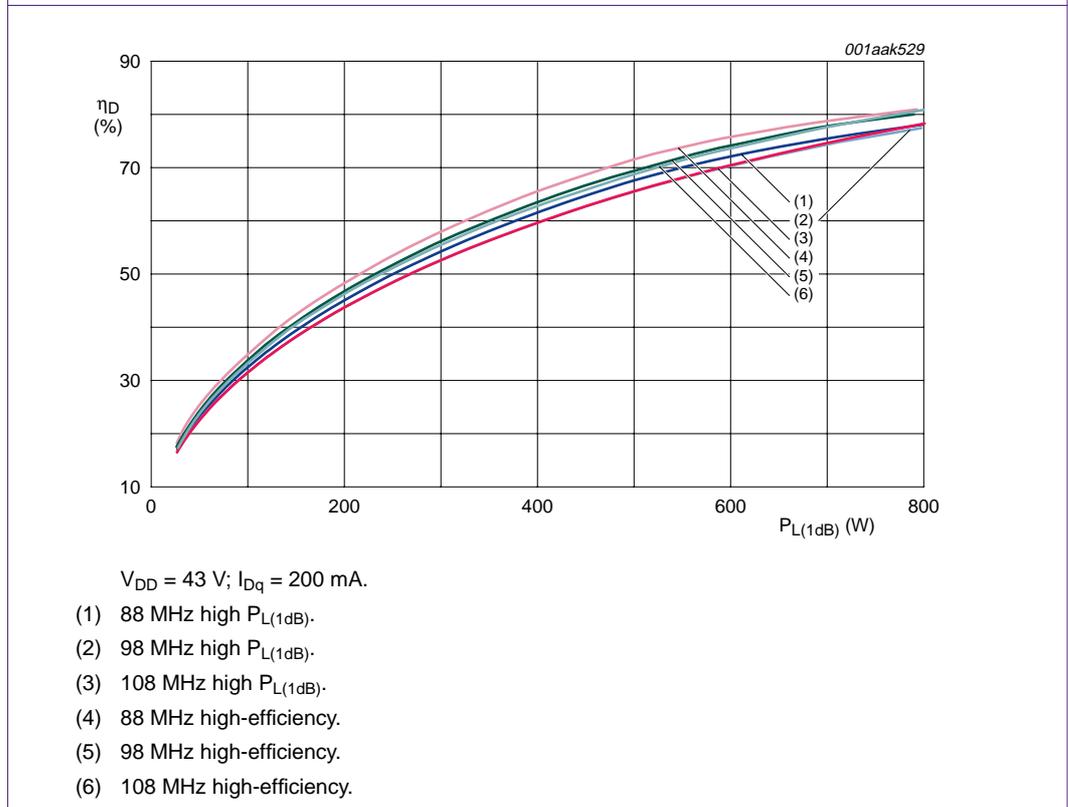


Fig 8. Efficiency comparison: 43 V, high-efficiency to high $P_{L(1dB)}$ tuning set-ups

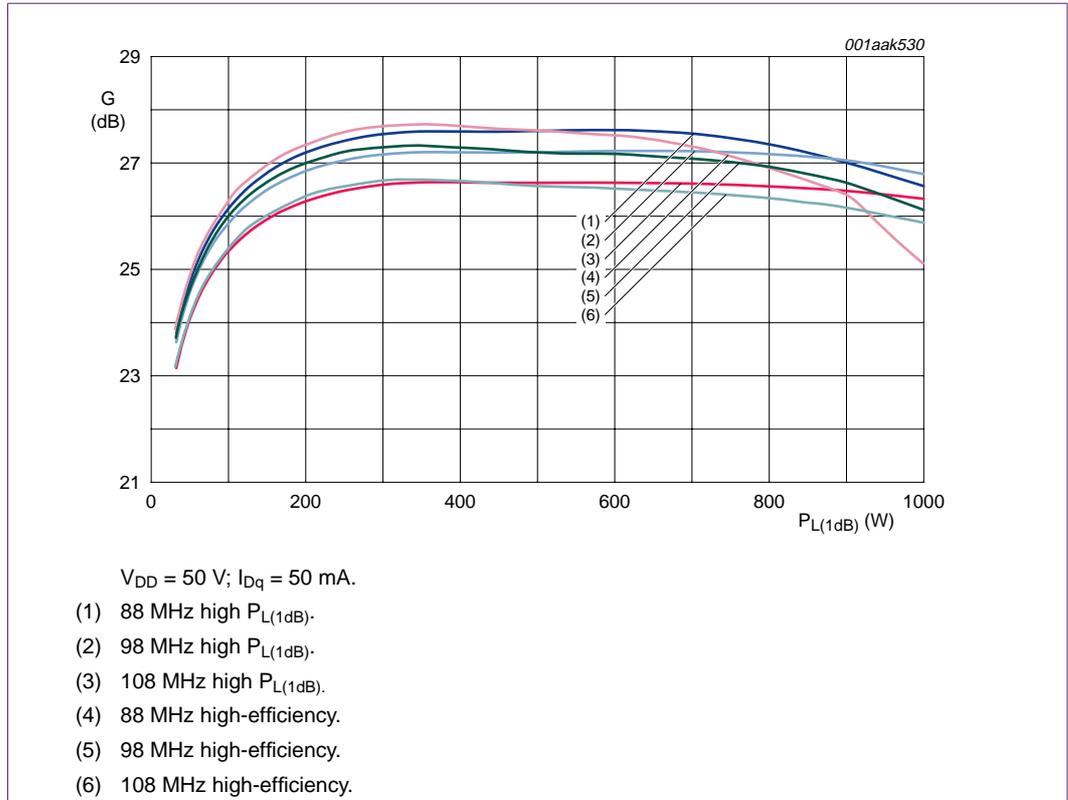


Fig 9. Gain comparison: 50 V, high-efficiency to high $P_{L(1dB)}$ tuning set-ups

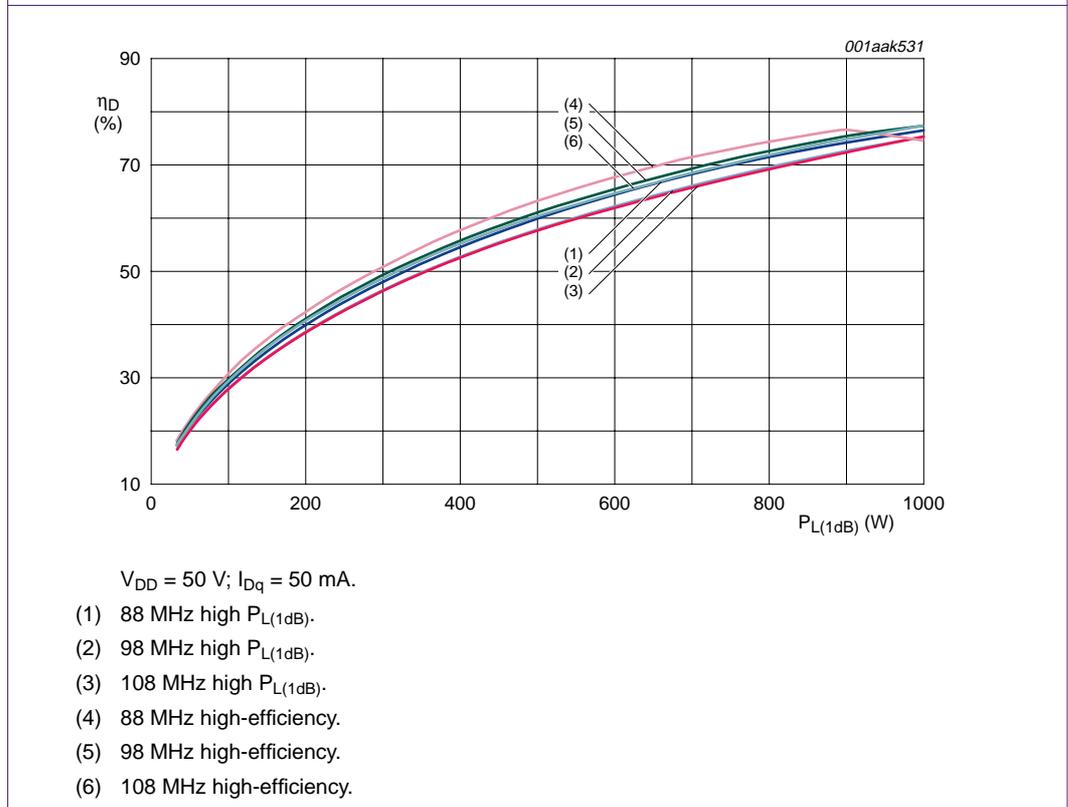


Fig 10. Efficiency comparison: 50 V, high-efficiency to high $P_{L(1dB)}$ tuning set-ups

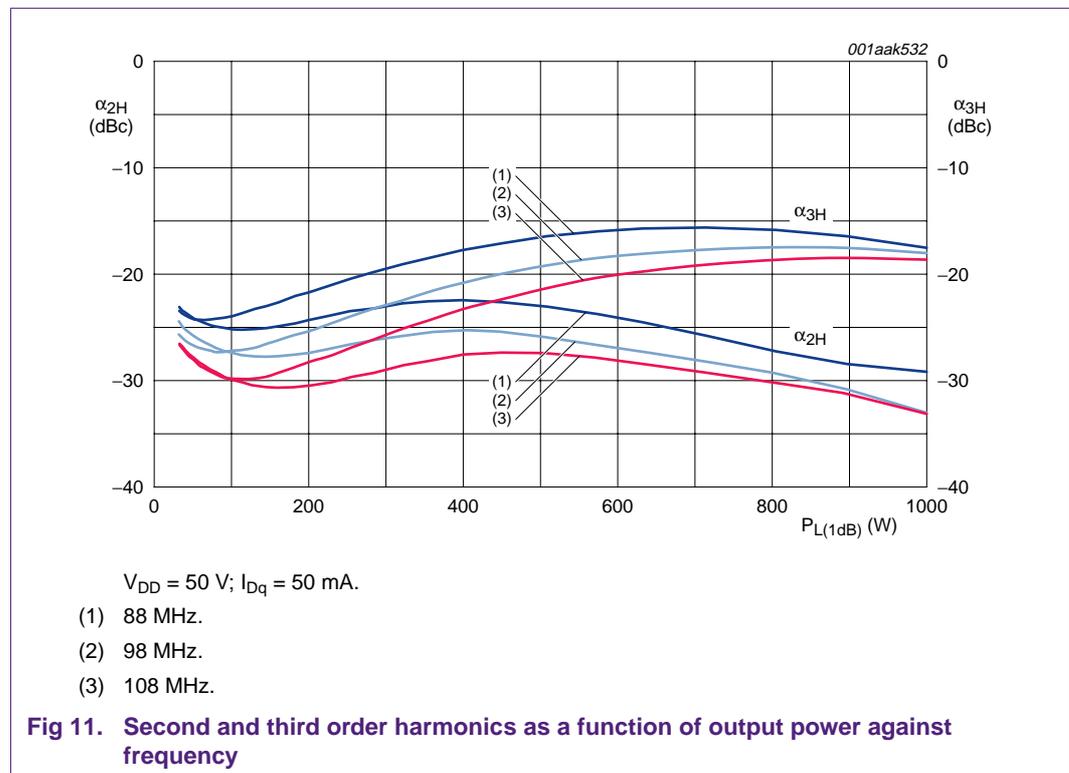
Table 7 shows the Input Return Loss (IRL) over the three frequencies for the high $P_{L(1dB)}$ tuning set-ups at 50 V.

Table 7. Input return loss for the high $P_{L(1dB)}$ tuning set-up

This table summarizes the input return loss of the high $P_{L(1dB)}$ tuning set-up at $I_{Dq} = 50\text{ mA}$ and $T_h = 25\text{ }^\circ\text{C}$.

Frequency (MHz)	Output power (W)	Input return loss (dB)
88	1000	-11
98	1000	-17
108	1000	-14

Figure 11 shows the 2nd and 3rd harmonic levels of the circuit. It can be seen from examining the 2nd harmonics that the push-pull action provides good cancellation. In addition, negligible power is present in the 2nd and 3rd harmonics, so that the power out of the circuit can be considered to be in the fundamental.



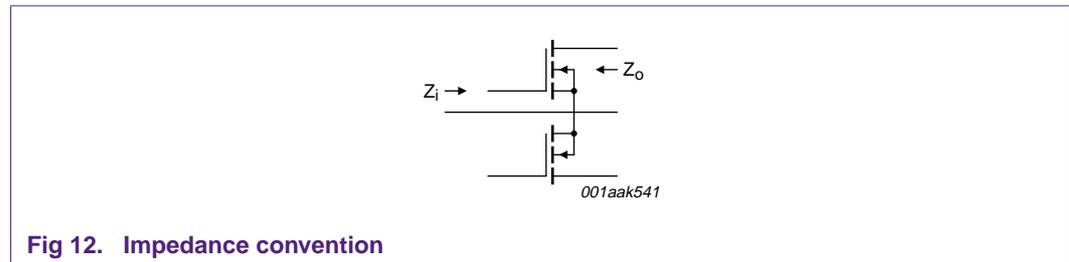
5. Input and output impedance

The BLF578 input and output impedances are given in [Table 8](#). These are generated from a first order equivalent circuit of the device and can be used to get the first-pass matching circuits.

Table 8. Input and output impedance per section

Frequency (MHz)	Input		Output	
	Z_i		Z_o	
25	1.176	-j13.262	1.697	-j0.060
50	1.176	-j6.617	1.688	-j0.120
75	1.176	-j4.395	1.674	-j0.178
100	1.176	-j3.280	1.654	-j0.234
125	1.176	-j2.607	1.630	-j0.288
150	1.176	-j2.155	1.600	-j0.338
175	1.177	-j1.830	1.567	-j0.385
200	1.177	-j1.583	1.531	-j0.427
225	1.177	-j1.390	1.491	-j0.466
250	1.178	-j1.233	1.449	-j0.500
275	1.178	-j1.103	1.406	-j0.531
300	1.178	-j0.993	1.361	-j0.556
325	1.179	-j0.898	1.316	-j0.578
350	1.179	-j0.816	1.270	-j0.596
375	1.180	-j0.743	1.225	-j0.610
400	1.180	-j0.678	1.179	-j0.620
425	1.181	-j0.620	1.135	-j0.627
450	1.181	-j0.567	1.091	-j0.631
475	1.182	-j0.519	1.048	-j0.632
500	1.183	-j0.474	1.007	-j0.631

The convention for these impedances is shown in [Figure 12](#). They indicate the impedances looking into half the device.



6. Base plate drawings

6.1 Input base plate

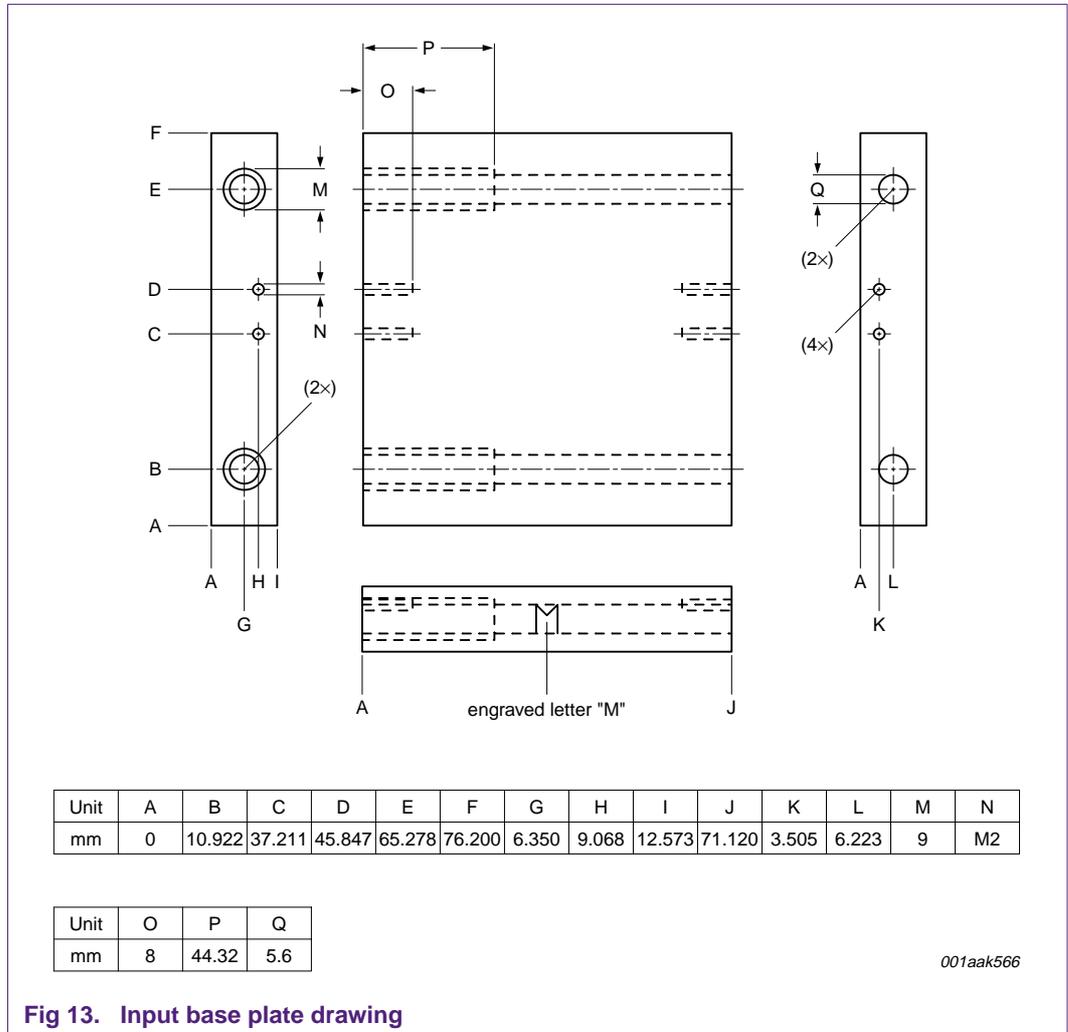
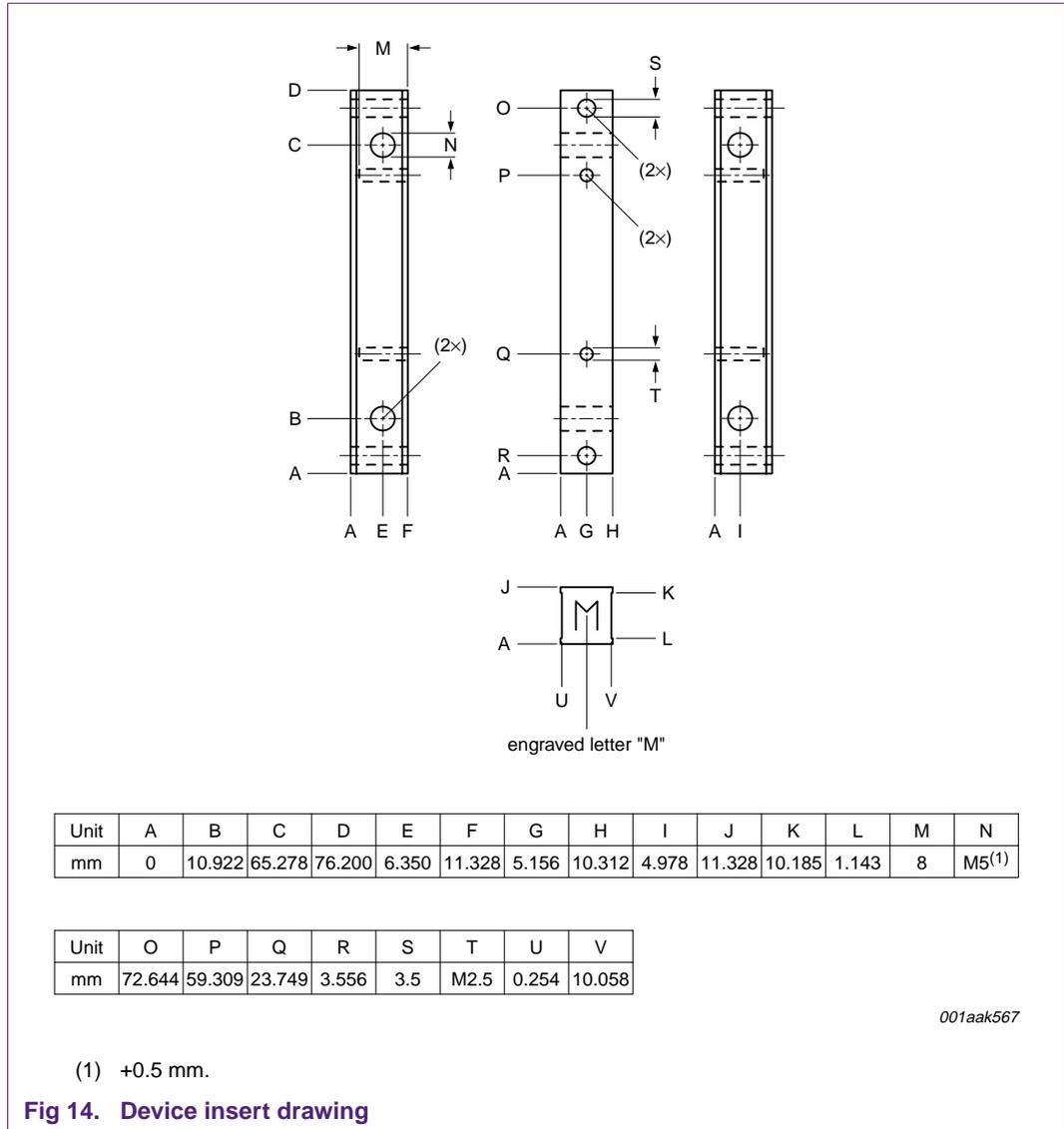


Fig 13. Input base plate drawing

6.2 Device insert



6.3 Output base plate

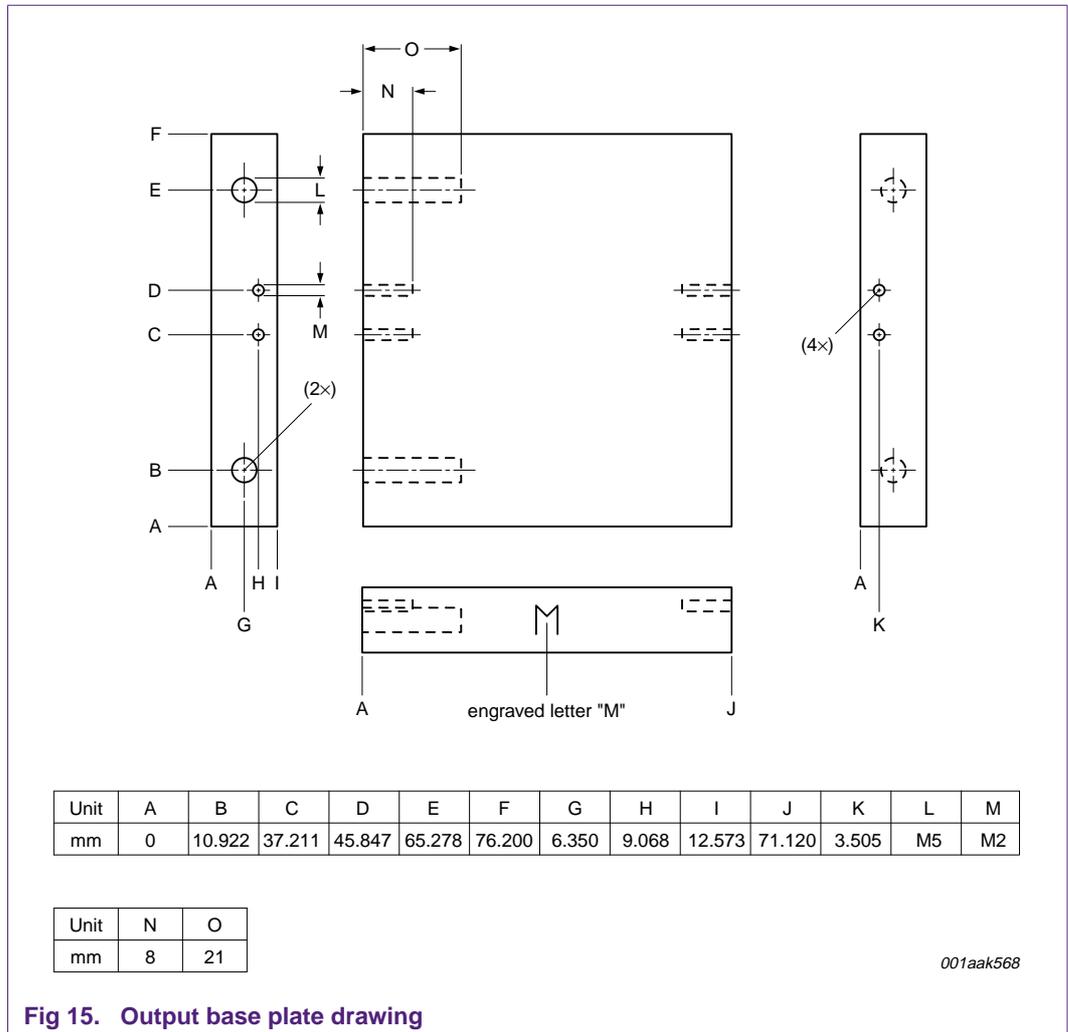


Fig 15. Output base plate drawing

7. Reliability

At first glance, it would seem that great strains would be put on a single device running at 800 W or even 1 kW of output power. Careful consideration to the die layout has helped minimize these stresses, resulting in very reliable performance.

Time-to-Failure (TTF) is defined as the expected time elapsed until 0.1 % of the devices of a sample size fail. This is different from Mean-Time-to-Failure (MTBF), where half the devices would have failed and its orders of magnitude are shorter. The predominant failure mode for LDMOS devices is electromigration. The TTF for this mode is primarily dependant on junction temperature (T_j). Once the device junction temperature is measured and an in-depth knowledge is obtained for the average operating current for the application, the TTF can be calculated using [Figure 16](#) and the related procedure.

7.1 Calculating TTF

The first step is use the thermal resistance (R_{th}) of the device to calculate the junction temperature. The R_{th} from the junction to the device flange for the BLF578 is 0.145 K/W. If the device is soldered down to the heatsink, this same value can be used to determine T_j . If the device is greased down to the heatsink, the $R_{th(j-h)}$ value becomes 0.3 K/W, as the thermal resistivity for the grease layer from the flange to the heatsink is approximately 0.15 K/W.

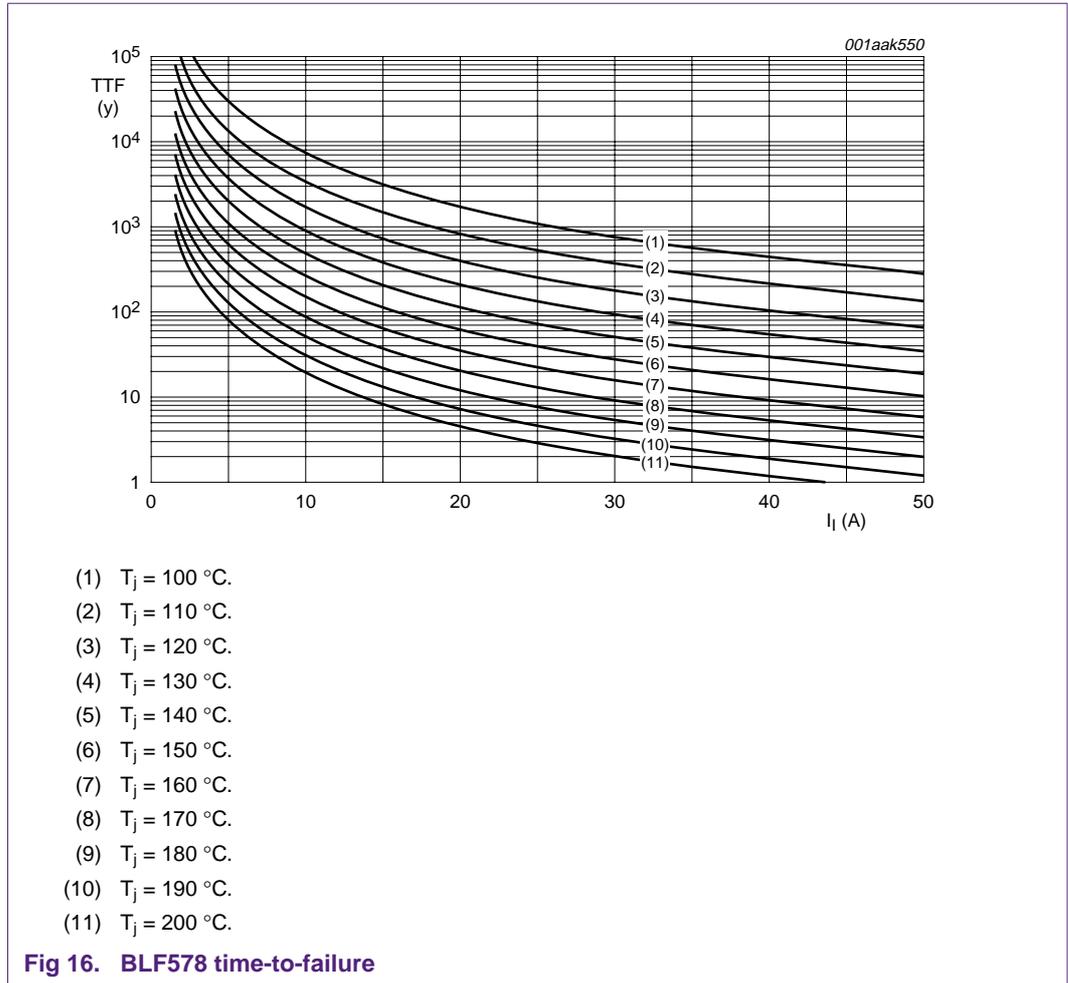
Example: Assuming the device is running at 1 kW with the RF output power at 75 % efficiency on a heatsink (e.g. 40 °C). T_j can be determined based on the operating efficiency for the given heatsink temperature:

- Dissipated power (P_d) = 333 W
- Temperature rise (T_r) = $P_d \times R_{th} = 333 \text{ W} \times (0.3 \text{ °C/W}) = 100 \text{ °C}$
- Junction temperature (T_j) = $T_h + T_r = 40 \text{ °C} + 100 \text{ °C} = 140 \text{ °C}$

Based on this, the TTF can be estimated using a device greased-down heatsink as follows:

- The operating current is just above 26.5 A
- $T_j = 140 \text{ °C}$

The curve in [Figure 16](#) intersects the x-axis at 27 A. At this point, it can be estimated that it would take 80 years for 0.1 % of the devices to fail.



8. Test configuration block diagram

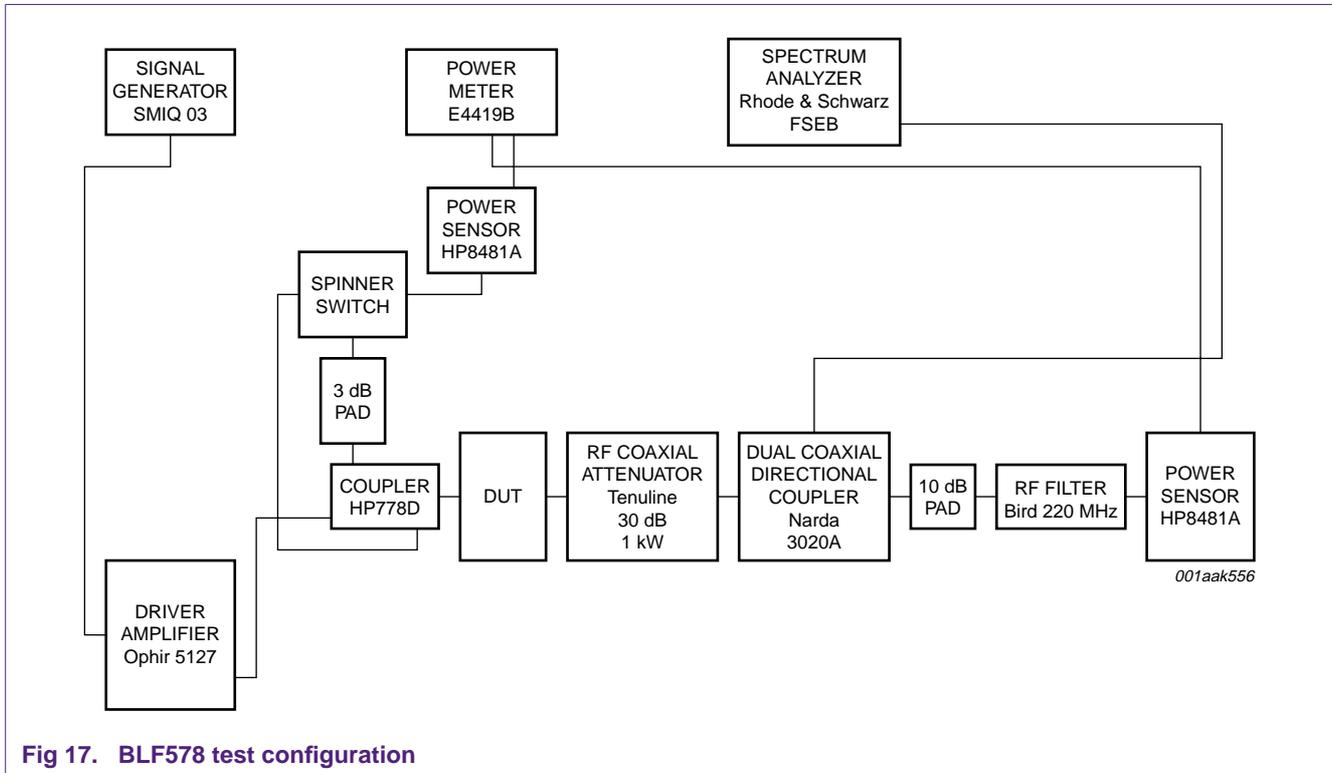


Fig 17. BLF578 test configuration

9. PCB layout diagrams

Please contact your local NXP Semiconductors' salesperson for copies of the PCB layout files.

10. Abbreviations

Table 9. Abbreviations

Acronym	Description
CW	Continuous Wave
ESD	ElectroStatic Discharge
FM	Frequency Modulation
IMD	InterModulation Distortion
IRL	Input Return Loss
LDMOST	Laterally Diffused Metal-Oxide Semiconductor Transistor
PAR	Peak-to-Average power Ratio
PCB	Printed-Circuit Board
SMT	Surface Mount Technology
VHF	Very High Frequency
VSWR	Voltage Standing Wave Ratio

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12. Figures

Fig 1.	BLF578 input circuit; 88 MHz to 108 MHz	4			
Fig 2.	BLF578 output circuit; 88 MHz to 108 MHz	4			
Fig 3.	Cable length definition	6			
Fig 4.	BLF578 PCB layout	7			
Fig 5.	Photograph of the BLF578 circuit board	8			
Fig 6.	Typical CW data for the 43 V high-efficiency tuning set-up; 88 MHz to 108 MHz	11			
Fig 7.	Gain comparison: 43 V, high-efficiency to high $P_{L(1dB)}$ tuning set-up	12			
Fig 8.	Efficiency comparison: 43 V, high-efficiency to high $P_{L(1dB)}$ tuning set-ups	12			
Fig 9.	Gain comparison: 50 V, high-efficiency to high $P_{L(1dB)}$ tuning set-ups	13			
Fig 10.	Efficiency comparison: 50 V, high-efficiency to high $P_{L(1dB)}$ tuning set-ups	13			
Fig 11.	Second and third order harmonics as a function of output power against frequency	14			
Fig 12.	Impedance convention	15			
Fig 13.	Input base plate drawing	16			
Fig 14.	Device insert drawing	17			
Fig 15.	Output base plate drawing	18			
Fig 16.	BLF578 time-to-failure	20			
Fig 17.	BLF578 test configuration	21			

13. Contents

1	Introduction	3
2	Circuit diagrams and PCB layout	4
2.1	Circuit diagrams	4
2.2	Bill Of Materials	5
2.3	BLF578 PCB layout	7
2.4	PCB form factor	8
3	Amplifier design	8
3.1	Mounting considerations	8
3.2	Bias circuit	8
3.3	Amplifier alignment	9
4	RF performance characteristics	10
4.1	Continuous wave	10
4.2	Continuous wave graphics	11
5	Input and output impedance	15
6	Base plate drawings	16
6.1	Input base plate	16
6.2	Device insert	17
6.3	Output base plate	18
7	Reliability	18
7.1	Calculating TTF	19
8	Test configuration block diagram	21
9	PCB layout diagrams	21
10	Abbreviations	21
11	Legal information	22
11.1	Definitions	22
11.2	Disclaimers	22
11.3	Trademarks	22
12	Figures	23
13	Contents	23

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Date of release: 13 October 2009
 Document identifier: AN10800_1