

# AN11176

## Automotive qualified ESD protection for LVDS interfaces

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Application note

### Document information

Info	Content
<b>Keywords</b>	Low-Voltage Differential Signaling (LVDS), ElectroStatic Discharge (ESD)
<b>Abstract</b>	This application note gives an overview of the importance of ESD protection for automotive LVDS interfaces. Eye diagrams demonstrate the high performance of NXP Semiconductors first automotive-qualified ESD protection product for an LVDS interface. This document demonstrates, that NXP Semiconductors' fully integrated solutions enable easy routing and relaxed board design.



## Revision history

Rev	Date	Description
1	20120423	Initial version

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## 1. Introduction

This report is structured as follows.

[Section 2](#) gives an overview and a short description of relevant ESD protection standards. [Section 3](#) presents a special rail-to-rail-based diode concept. NXP Semiconductors uses this concept to achieve ultra low line capacitance for high-speed data interface. Some basic information about Printed-Circuit Board (PCB) design is documented in [Section 4](#). [Section 6](#) ends this application note with a brief summary.

## 2. ESD protection standards

### 2.1 IEC 61000-4-2

Interfaces of consumer electronic equipment are widely specified according to the International Electrotechnical Commission (IEC) standard IEC 61000-4-2. This standard is not targeted towards particular devices but towards general equipment, systems and subsystems that may be involved in electrostatic discharge. The model [Figure 1](#) consists of a 150 pF capacitor and a 330 Ω series resistor representing the counterpart to the Device Under Test (DUT).

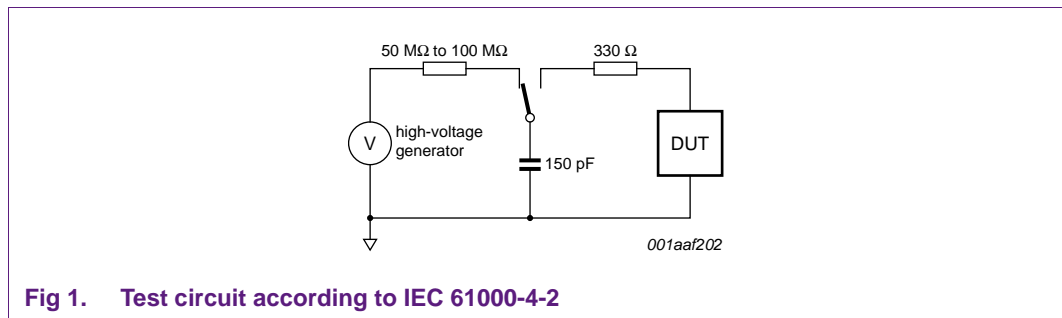


Fig 1. Test circuit according to IEC 61000-4-2

According to IEC 61000-4-2, an ESD surge can be applied by contact as well as by air discharge and is classified by the charge voltage of the capacitor ([Table 1](#)).

To achieve a reasonable relation between cost and prevention of field returns due to ESD failures, class 4 is considered as the most appropriate level for consumer products.

Table 1. IEC 61000-4-2 ESD surge classification<sup>[1]</sup>

Contact discharge			Air discharge	
Class	Test voltage (kV)	Maximum current (A)	Class	Test voltage (kV)
1	2	7.5	1	2
2	4	15	2	4
3	6	22.5	3	8
4	8	30	4	15
X	special	special	X	special

[1] X is an open level that must be specified in the dedicated device specification. If higher voltages than level 4 are specified, special test equipment may be needed.

[Figure 2](#) shows a typical ESD current pulse form generated by an ESD surge according to IEC 61000-4-2.

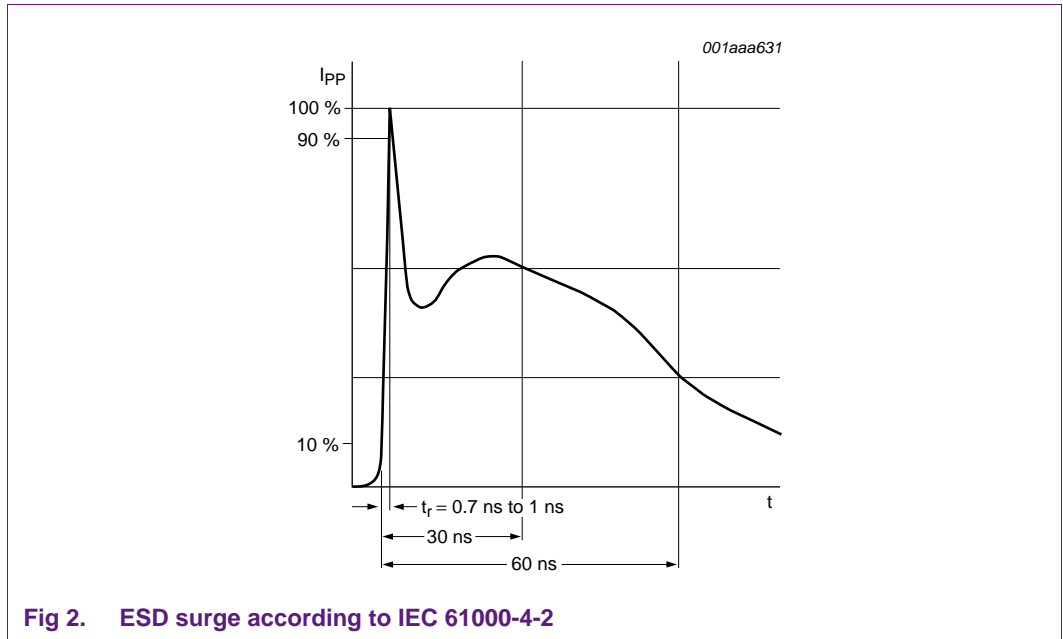


Fig 2. ESD surge according to IEC 61000-4-2

A characteristic of IEC 61000-4-2 ESD pulses is the very short rising edge. The maximum peak current is reached within 0.7 ns to 1 ns. To avoid severe voltage overshoots at the protected device, the ESD protection circuit needs a very short reaction time. Therefore, it is important to put special attention to the selection of the correct protection device. Ultra low line capacitance devices are recommended, especially for high-speed interfaces such as High-Definition Multimedia Interface (HDMI), because they react very fast (in the nanosecond range).

Another issue besides the voltage clamping is the maximum current injected into a device during an ESD discharge. To withstand a maximum current of 30 A as specified in IEC 61000-4-2, level 4, careful dimensioning of all conductors and components affected by an ESD surge is mandatory. Using appropriate structural dimensions helps to obtain very short reaction times of the ESD protection circuits. It avoids permanent damage caused by for example, electromigration of aluminum tracks.

**2.2 Human Body Model (HBM), MIL-883E method 3015.7**

The HBM standard simulates an ESD surge generated by human contact to electronic components.

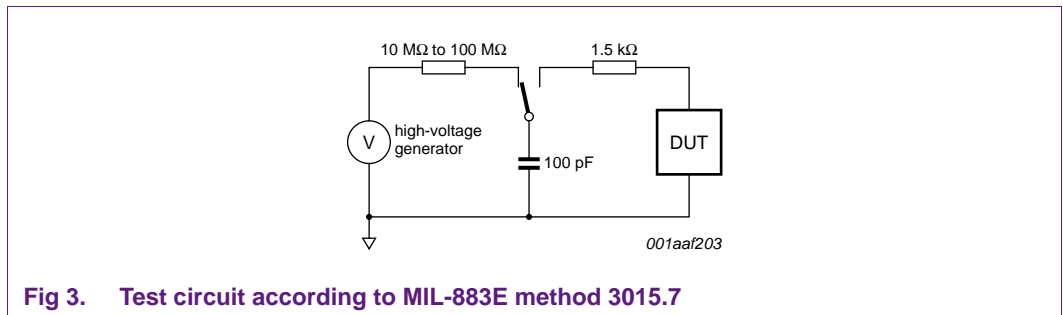


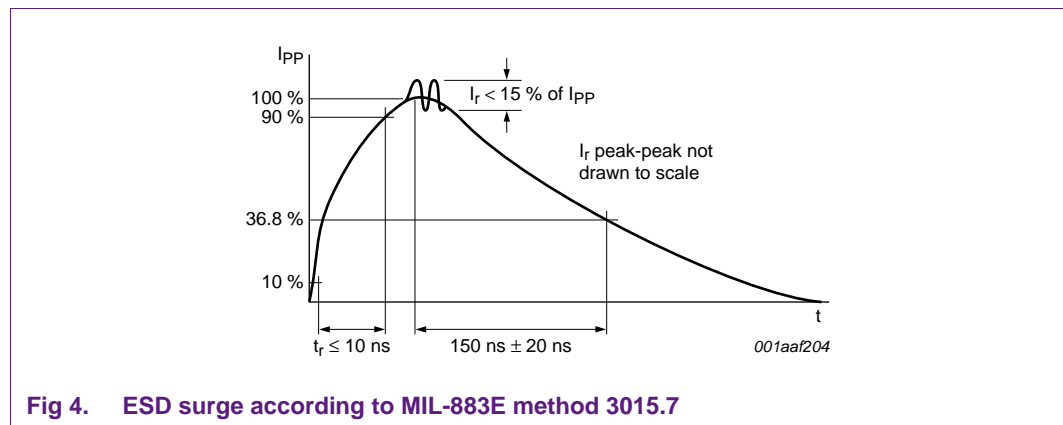
Fig 3. Test circuit according to MIL-883E method 3015.7

As shown in [Figure 3](#), the model consists of a 100 pF capacitor and a 1.5 kΩ serial resistor to simulate a human body. According to the standard, the ESD surge is applied by contact and the test is applied in both the positive and negative direction. [Table 2](#) shows three different classes differentiated by the charge voltage of the capacitor.

**Table 2. MIL-883E method 3015.7 ESD surge classification, contact discharge**

Class	Threshold voltage (V)	Maximum current (A)
0	< 250	-
1A	250 to 499	1.33
1B	500 to 999	
1C	1000 to 1999	
2	2000 to 3999	2.67
3A	4000 to 7999	> 2.67
3B	> 8000	

[Figure 4](#) shows a typical ESD current pulse form generated by an ESD surge according to MIL-883E method 3015.7.



**Fig 4. ESD surge according to MIL-883E method 3015.7**

The shape of the ESD surge looks similar to an RC-charge/discharge curve. As the maximum current applied is about a few amperes and the rise time about a few nanoseconds, the reaction time of an ESD protection circuit is relatively uncritical.

### 2.3 Comparison of IEC 61000-4-2 to MIL-883E method 3015.7

Direct comparison of both ESD models is difficult due to the differences in the discharge waveforms. Generally, the maximum injected current and the total load of IEC 61000-4-2 standard is much higher than those specified in the HBM according to the MIL-883E method 3015.7.

The rise time of the current waveform is different because the series resistor is 1.5 k $\Omega$  in the HBM instead of 330  $\Omega$  in the IEC 61000-4-2 model.

While the specified rise time for the IEC 61000-4-2-compliant current waveform is from 0.7 ns to 1 ns, the HBM waveform has a specified rise time below 10 ns only.

Assuming that the maximum current rating is more stressful to an ESD protection diode and other affected components than the duration of the current flow, the IEC 61000-4-2 standard is the most stringent of the two tests.

As the surge current is determined by the gradient of charge over time  $I = \frac{\partial Q}{\partial t}$ , the voltage drop across the protection diode can be described as  $V \approx R_{intrinsic} \times \frac{\partial Q}{\partial t}$ , where  $R_{intrinsic}$  is the inner resistance of the diode.

Overshoots occur mostly because of short ESD-surge rise times. Shorter rise times lead to higher voltage overshoots. This is due to the reaction time of the protection devices. Even if the test voltage of both methods/standards is similar, IEC 61000-4-2 remains the most stringent test for a protection circuit because the maximum internal voltage reaches a higher level during a discharge.

For a high resistor value in the HBM, the maximum current is in the order of a few amperes. In comparison, the maximum current of an ESD surge according to IEC 61000-4-2 can reach 30 A.

Integrated components such as resistors and integrated planar aluminum metal wires have a limited maximum current density. To avoid degradation effects such as electromigration, it is important to maintain certain design rules. High current densities might also result in a too high thermal stress in resistors and lead to a permanent shift of resistance value.

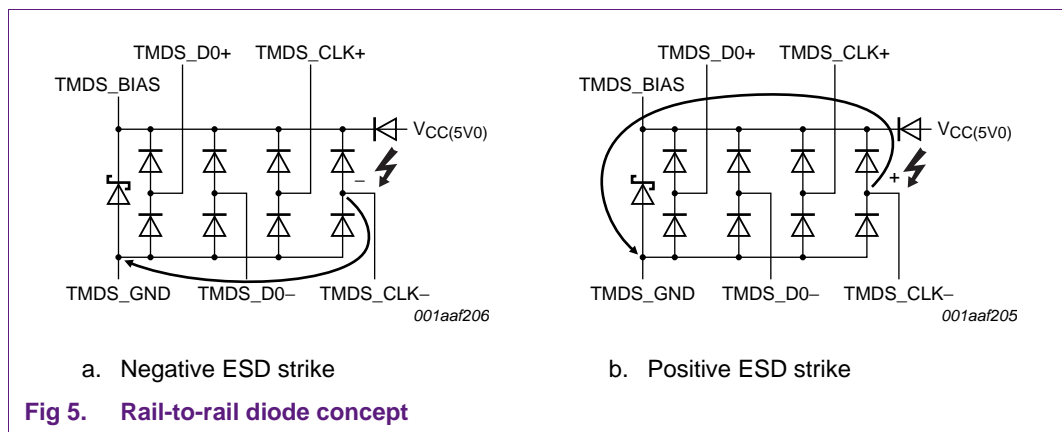
To avoid failure during a nearly unlimited number of ESD surges below the specified maximum voltage limit, NXP Semiconductors takes electromigration and thermal stress into account during standard design procedure.

### 3. Rail-to-rail concept

In the rail-to-rail concept, a negative ESD strike on the I/O pin causes one of the rail-to-rail diodes (the lower diode at the flash-sign in [Figure 5](#), left side) to become forward biased and transfer the ESD strike through the lower diode to ground.

A positive discharge strike causes the other rail-to-rail diode (the upper diode at the flash-sign in [Figure 5](#), right side) to become forward biased transferring the discharge to the  $V_{CC}$  pin of the device. To prevent charging of the supply, an additional Zener diode between ground and  $V_{CC}$  clamps voltages exceeding the Zener clamping voltage caused by the ESD strike to ground.

With this concept, ultra low line capacitances can be achieved.



### 4. PCB design

Following ten high-speed and ESD layout considerations are applicable to all high-speed designs, like for example HDMI, DisplayPort, Serial Advanced Technology Attachment (SATA).

1. Minimize the differential microstrip or stripline trace lengths: minimize Physical Layer (PHY) distance to connector and always place the ESD clamp as close as possible to the connector.
2. Minimize the inductive return parasitic of the ESD ground to the connector / chassis. Consider the current spreading that occurs when ESD energy is shunted into the GND planes / traces and must travel back to the chassis ground. This current can induce spurious voltages nearby unrelated circuitry such as memory or clock lines, which can cause upset to other system blocks.
3. Some PHY manufacturers recommend ultra low loss PCB dielectric material. This material is preferred for GHz signaling, but is impractical for very low-cost consumer or automotive devices. Shorter traces help to offset the shortcomings of cheaper dielectric PCB material.
4. Keep differential microstrip traces on the same layer and avoid vias. If vias and layer changes must be used, reserve them for low-speed signals and power traces.

5. Avoid right angles (90°), take two 45° angles instead. It reduces Time-Domain Reflectometer (TDR) discontinuities and lessens reflections (contributes to ElectroMagnetic Interference (EMI) and deterministic jitter).
6. Keep traces lengths within intra-pair skew specifications from the PHY manufacturer.
7. Avoid routing signal lines over any ground discontinuities. It can exacerbate EMI and inhibit ESD or other RF return currents in transmission lines. If intentional RF coupling is intended, such a configuration can be managed. Nevertheless, it is not recommended to cut ESD return current path in this manner.
8. Avoid stubs on transmission lines with flow-through routing techniques. **Do not route automatically!**
9. Keep out distances and edge limits from PCB.
10. Observe conservatively borders and inner antipads. If the design rule check allows, attempt a symmetric routing to the connector-side PCB.

#### 4.1 AC coupling caps

Consider placing any DC blocking capacitors (AC coupling capacitors) on the connector side of PESD1LVDS.

Additionally, rather place PESD1LVDS strictly in the bias domain of the local PHY Application-Specific Integrated Circuit (ASIC), rather than at an unknown bias set by the transceiver of the peripheral ASIC.

This topology puts the blocking capacitors in series with the ESD current at instantaneous voltages, obviously exceeding the absolute maximum ratings of these capacitors. However the ESD energy is concentrated into pulses of very short duration. There is a great deal of literature about potential degradation over time of ceramic and other capacitors. Additionally, the repeated pulsing of IEC 61000-4-2 strikes can significantly charge such capacitors to very high DC voltages, possibly sufficient to arc during an ESD strike. If these concerns cannot be addressed sufficiently, then place the capacitors behind the PESD1LVDS, on the ASIC side. In that case, the system is susceptible to DC shunt faults.

Obviously a balance between a low clamping voltage (protecting ASIC from ESD) and a medium voltage DC short circuit (TVS) involves some trade-offs between clamping, protection level and capacitive signal loading.

#### 4.2 Geometry of micro striplines (TMDS)

The design of a 100 Ω differential impedance has to be optimized for the PCB material and the number of layers. It is possible to calculate the impedance ( $Z_0$ ) and the differential impedance ( $Z_{diff}$ ) using the following equations (see also [Figure 6](#)).

$$Z_0 (\Omega) = \frac{60}{\sqrt{0,457\epsilon_r + 0,67}} \times \ln\left(\frac{4h}{0,67(0,8W + t)}\right) \tag{1}$$

$$Z_{diff} (\Omega) \approx 2Z_0 \left(1 - 0,48e^{\left(-0,96\frac{S}{h}\right)}\right) \tag{2}$$

The results are valid up to a few GHz.



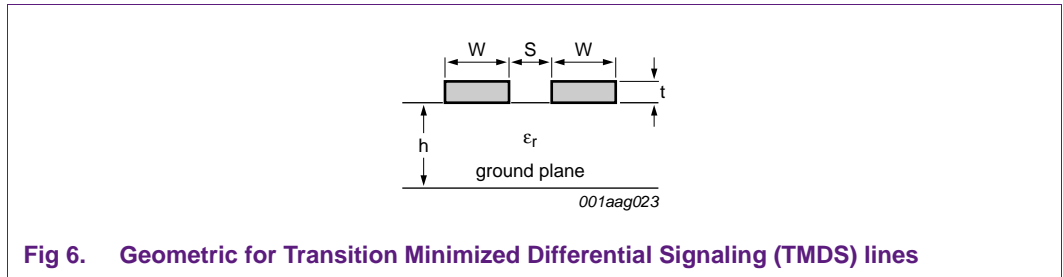


Fig 6. Geometric for Transition Minimized Differential Signaling (TMDs) lines

Solid ground plane underneath the micro striplines is part of the micro stripline design.

Table 3. Parameters for 2-layer and 4-layer PCB (FR4)

Parameter	4-layer PCB	2-layer PCB	Unit
Trace width (W)	5 (0.127)	8 (0.203)	mil (mm)
Spacing (S)	4 (0.102)	4 (0.102)	mil (mm)
Layer height (h)	4.5 (0.114)	63 (1.6)	mil (mm)
Relative permittivity ( $\epsilon_r$ )	4.3	4.3	-
Copper thickness (t)	1 (0.0254)	1 (0.0254)	mil (mm)
$Z_{diff}$	100.37	108.22	$\Omega$

As an example, [Table 3](#) shows all parameters which are necessary to design a 2-layer and a 4-layer board for a differential impedance ( $Z_{diff}$ ) of 100  $\Omega$ .

Demonstration versions of simple simulator software are available on the Internet to make the first steps.

## 5. Measurements

To evaluate the influence of PESD1LVDS, PCBs without and with a DUT were used to perform a TDR and an eye diagram measurement.

### 5.1 TDR measurement

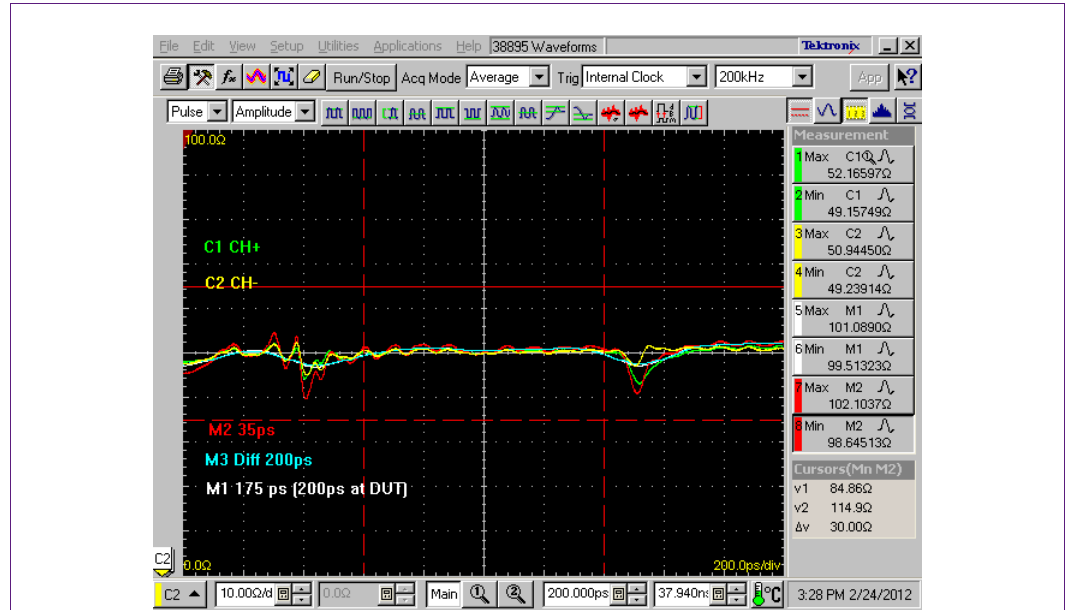


Fig 7. TDR measurement without DUT

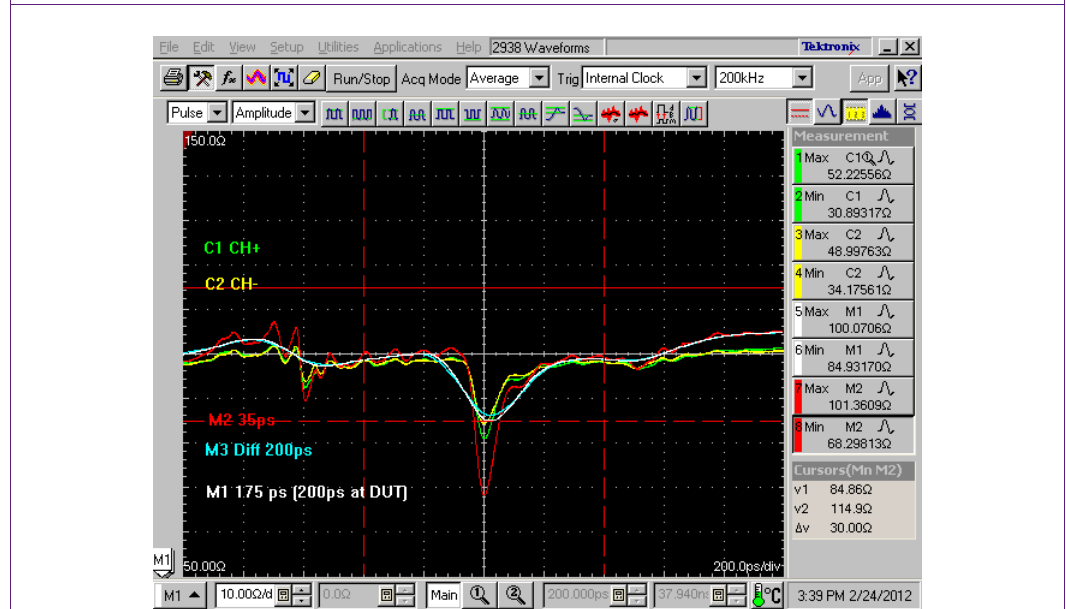


Fig 8. TDR measurement with DUT

Per definition, the impedance of the TDR is  $100 \Omega \pm 15 \%$  and can fall one time lower than  $85 \Omega$ . From TDR domain, PESD1LVDS fulfills the requirement.

5.2 Eye diagram measurement

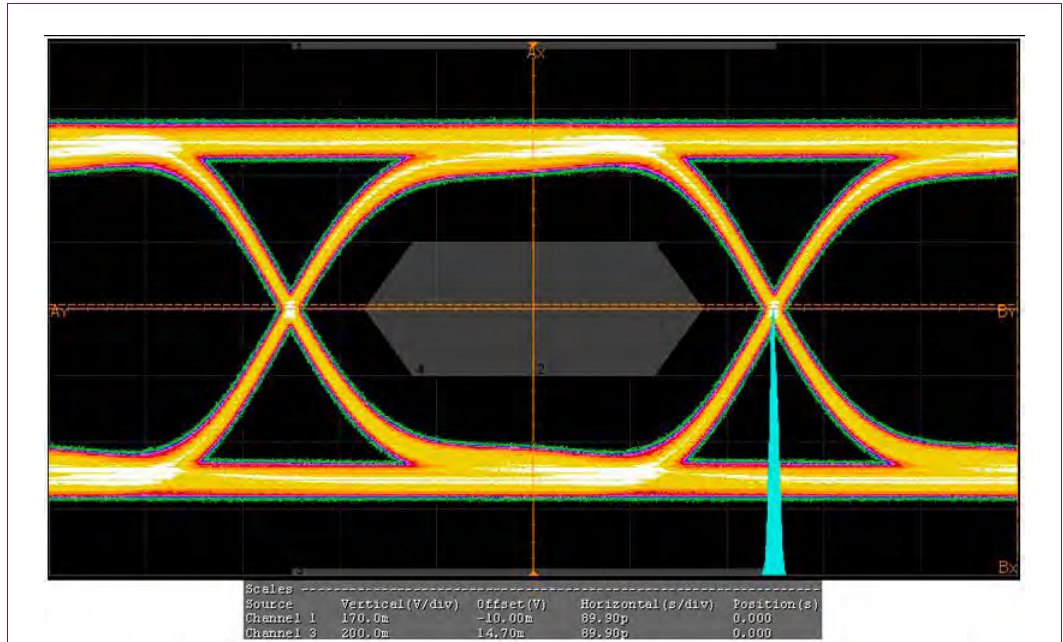


Fig 9. Eye diagram measurement without DUT

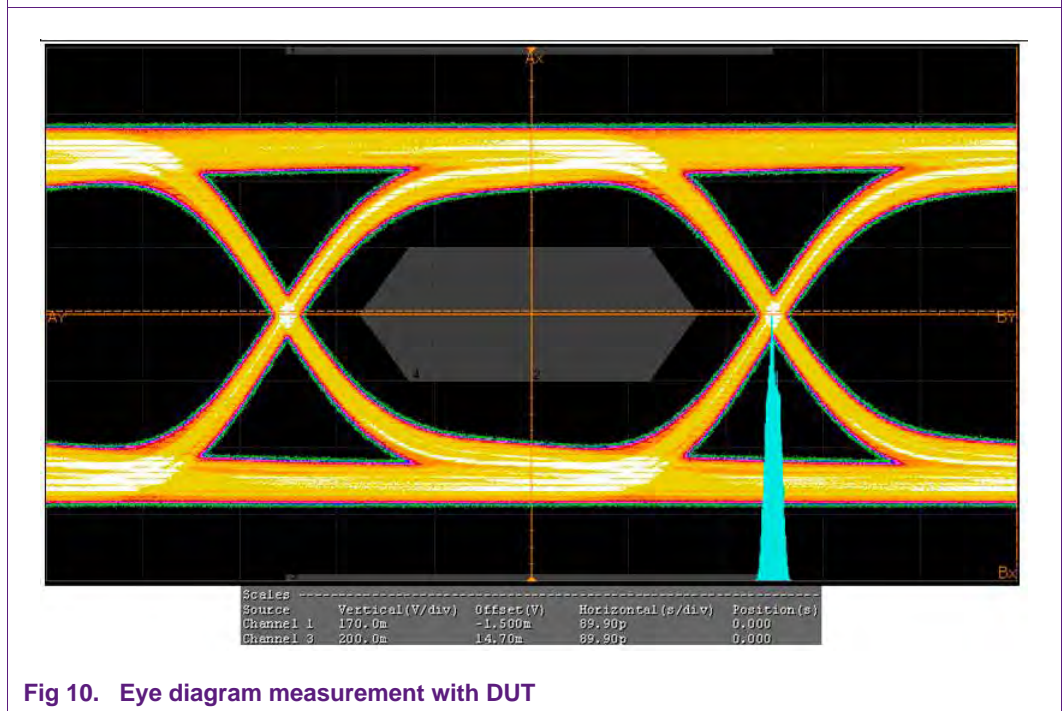


Fig 10. Eye diagram measurement with DUT

The influence of PESD1LVDS is visible but the eye is still not touched. PESD1LVDS passed all measurements of both tests and meets the requirements for high-speed LVDS interfaces.

## 6. Summary

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For high-speed interfaces such as LVDS, the use of high-level ESD protection is highly recommended. The cost of an application in an automotive environment is too high to risk field returns. A fail can also damage company brand names and images. The continuous trend towards submicron CMOS processes at 120 nm, 90 nm, 65 nm and 45 nm technology nodes also contributes to a very high sensitivity of core ICs, making ESD protection mandatory.

The high-speed ESD protection devices discussed in this application note fully comply with both crucial requirements:

- High-level ESD protection according to the international standards for consumer applications (IEC 61000-4-2 level 4)
- Ultra low line capacitance required for LVDS high-speed lines

PESD1LVDS allows and supports optimal routing of the TMDS lines to minimize parasitic influences.

NXP Semiconductors high-speed ESD protection PESD1LVDS is fully compliant with AEC-Q101 and supports easy routing and relaxed board layout at highest protection levels. Therefore, this device is the state-of-the-art protection device to be implemented on all new customer designs.

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