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SIM card EMI filtering and ESD protection using integrated discretes

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Document information

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Abstract	This document describes the use of NXP EMI filter and ESD protection devices for the SIM card interface and the boundary conditions. Furthermore, filter band width and driver strength requirements in dependence of the clock speed are explained.

Revision history

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1. Introduction

All mobile phones manufactured today using 2G or later mobile phone wireless standards use SIM or Universal Integrated Circuit Card (UICC) smart cards often referred to as USIM cards for 3G and beyond, following the ISO/IEC 7816-3 (“specifies electrical interface and transmission protocols for asynchronous cards”), ISO/IEC 7816-12 (“Cards with contacts - USB electrical interface and operating procedures”) and ETSI TS 102 221(“Smart Cards; UICC-Terminal interface; Physical and logical characteristics”) standards for the electrical interface compatibility and protocol.

No mobile phone will allow to make or receive calls - except emergency calls due to legal requirements in some countries - without a properly working (U)SIM card.

As this interface is of such basic need, it is typically protected against damage from ESD and very often also from EMI interference from the mobile phone transmitter. Especially in phone supporting the GSM standard, digital interfaces to external connectors are typically also protected against EMI radiation.

This document summarizes the application of different devices to protect (U)SIM interfaces from ESD discharges and EMI interference (both, radiation and injection).

Note: In the following text, SIM refers to USIM- and SIM cards as long as no differentiation is mandatory.

As defined in ISO/IEC 7816-12:2005(E): “Cards designed for ISO/IEC 7816-3 operating conditions shall not be damaged when activated under USB conditions. Conversely, cards designed for USB operation shall not be damaged when activated under ISO/IEC 7816-3 operating conditions (by definition, a damaged card no longer operates as specified or contains corrupt data).”

2. SIM card, electrical interface details

This section explains basics of the SIM and USIM electrical interfaces as described in ISO/IEC 7816-3, ISO/IEC7816-12 and ETSI TS 102 221 V8.0.0 (2008-08).

Please refer to the appropriate ISO/IEC documents to obtain access to the full specification.

2.1 The SIM card interface

This section summarizes parts of the electrical interface description of IEC/ISO 7816-3, issue 2006(E) and ETSI TS 102 221 V8.0.0 (2008-08). In case both standards are deviating from each other (i.e. specification of t_r, t_f of the reset signal RST), the technically more challenging value is used to describe or calculate other technical values.

The basic SIM card interface consists of the following signals:

- V_{CC}: provides card power supply (also named U_{CC})
- RST: provides card reset signal
- CLK: provides card clock signal
- I/O: data exchange between card and controller

- SPU: contact for standard or proprietary use (not taken into account in the further discussion)
- V_{PP}: programming voltage (may be used and set to V_{CC} on class A cards only)
- GND: card ground

2.1.1 SIM card supply voltage classes

The basic SIM interface reflects the development of decreasing supply voltages in the semiconductor industry over more than the last two decades. This is indicated by three different classes, A, B and C, each representing a different supply voltage level and maximum supply currents as summarized in Table 1

Table 1. Electrical characteristics of V_{CC} and I_{CC} under normal operating conditions

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC} [1]	supply voltage	class A	4.5	5.5	V
		class B	2.7	3.3	V
		class C	1.62	1.98	V
I_{CC}	supply current	at maximum allowed frequency			
		class A	-	60	mA
		class B	-	50	mA
		class C	-	30	mA
		when clock is stopped	-	0.5	mA

[1] V_{CC} is the SIM card supply voltage, also referred to as V_{SIM}.

2.1.2 SIM card control and data interface

The SIM card interface logic levels depend on the voltage class, as listed in Table 2 for class B and class C cards, as Class A is no longer used in new designs. Different SIM cards support different clock speeds. The default value is 5 MHz. Most cards contain a register called TA_1, which contains the supported clock frequency. The minimum clock frequency is 1 MHz, the maximum GSM clock frequency is 4 MHz, while the maximum SMART-card interface clock frequency can go up to 20 MHz. Any terminal (so e.g. the external pins of the EMI filter and ESD protection devices too) shall support frequencies up to 5 MHz.

Table 2. Electrical characteristics of SIM card data interface, RST, CLK and I/O

Under normal conditions, class B and class C unless otherwise specified.

Symbol	Parameter	Conditions		Min	Max	Unit
RST						
V_{IH}	high-level input voltage	all classes	[1]	$0.8V_{CC}$	V_{CC}	V
V_{IL}	low-level input voltage	all classes		0	$0.2V_{CC}$	V
t_r	rise time	C_l = 30 pF				
		open-drain driver	[3]	-	400	µs
			[2]	-	1	µs
		low impedance buffer		-	100	ns

Table 2. Electrical characteristics of SIM card data interface, RST, CLK and I/O *…continued*
Under normal conditions, class B and class C unless otherwise specified.

Symbol	Parameter	Conditions		Min	Max	Unit
t_f	fall time	C_I = 30 pF				
		open-drain driver	[3]	-	400	µs
			[2]	-	1	µs
		low impedance buffer		-	100	ns
CLK						
V_{IH}	high-level input voltage		[1]	$0.7V_{CC}$	V_{CC}	V
V_{IL}	low-level input voltage	class A and B		0	0.5	V
		class C		0	$0.2V_{CC}$	V
t_r	rise time	C_I = 30 pF		9 % of cycle		
t_f	fall time					
I/O						
V_{IH}	high-level input voltage	all classes	[1]	$0.7V_{CC}$	V_{CC}	V
V_{IL}	low-level input voltage	all classes	[2]	0	$0.15V_{CC}$	V
V_{OH}	high-level output voltage	external pull-up resistor: 20 kΩ to V_{CC}	[1]	$0.7V_{CC}$	V_{CC}	V
V_{OL}	low-level output voltage	I_{OL} = 1 mA				
		class A	[2][4]	0	$0.15V_{CC}$	V
		class B	[2][4]	0	$0.15V_{CC}$	V
			[3]	0	0.4	V
		class C	[3]	0	0.3	V
		I_{OL} = 500 µA; class C	[2][4]	0	$0.15V_{CC}$	V
All communication pins						
C_i	input capacitance			-	30	pF
C_O	output capacitance			-	30	pF
$R_{s(ch)}$	channel series resistance		[5]	47	100	Ω

[1] To allow overshoot the voltage shall remain between −0.3 V and V_{CC} + 0.3 V during dynamic operation.

[2] From ISO/IEC 7816-3:2006(E).

[3] From ETSI TS 102 221 V8.0.0 (2008-08).

[4] Interface device implementations should not require the card to sink more than 500 µA.

[5] Series resistor in channel to reduce short circuit current when low impedance drivers are used.

3. NXP SIM card, EMI filter and ESD protection devices

NXP Semiconductors offer a variety of EMI filter and ESD protection devices for the SIM card interface.

All devices contain the required series resistors 2 × 100 Ω and 1 × 47 Ω and offer different pitches (0.4 mm and 0.5 mm), several different channel capacitances ranging from 10 pF to 40 pF, and chip-scale packages as well as leadless plastic packages. Also a combination of standard digital interface EMI filtering and ESD protection and the USIM USB interface ESD protection is available (IP4365CX11).

A summary of the main parameters of the different NXP SIM card EMI filters and ESD protection devices is given in Table 3.

Table 3. Overview about NXP SIM card EMI filter and ESD protection devices main parameters

product name	channel capacitance (pF) V_{DC} = 0 V		package type	package size (mm); typical value	Remark
	typ	max			
IP4064CX8	-	20	WLCSP, 0.5 mm pitch	1.41 x 1.41 x 0.65	-
IP4364CX8	-	20	WLCSP, 0.4 mm pitch	1.16 x 1.16 x 0.61	-
IP4366CX8	10	12			
IP4365CX11	10	12	WLCSP, 0.4 mm pitch	1.16 x 1.56 x 0.61	incl. USB ESD protection
IP4264CZ8-10	10	12[1]	QFN-type, 0.4 mm pitch	1.35 x 1.7 x 0.45	USB ESD protection possible
IP4264CZ8-20	17	20[1]			
IP4264CZ8-40	35	40[1]			

[1] The single diodes in IP4264, pins 4 and 5 have a typical capacitance of 20 pF at 0 V bias.

The filter performance of EMI filters are typically characterized by their insertion loss, this measurement is performed in a well specified, terminated system as depicted in Figure 1. The results of the insertion loss measurements of various devices and their integrated filter channels are depicted in Figure 2 and Figure 3.

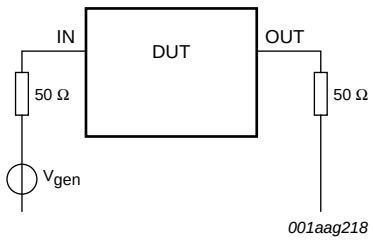
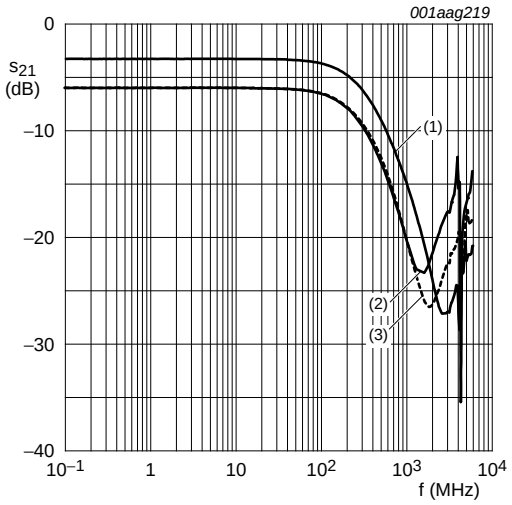
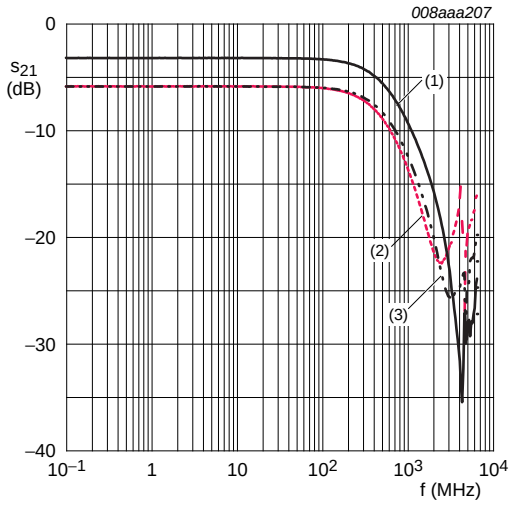


Fig 1. Typical insertion loss measurement set-up



(1) Pin B1 to B3
(2) Pin A2 to A3
(3) Pin C1 to C3

Fig 2. IP4064 and IP4364CX8: Insertion loss of (U)SIM EMI filter and ESD protection devices

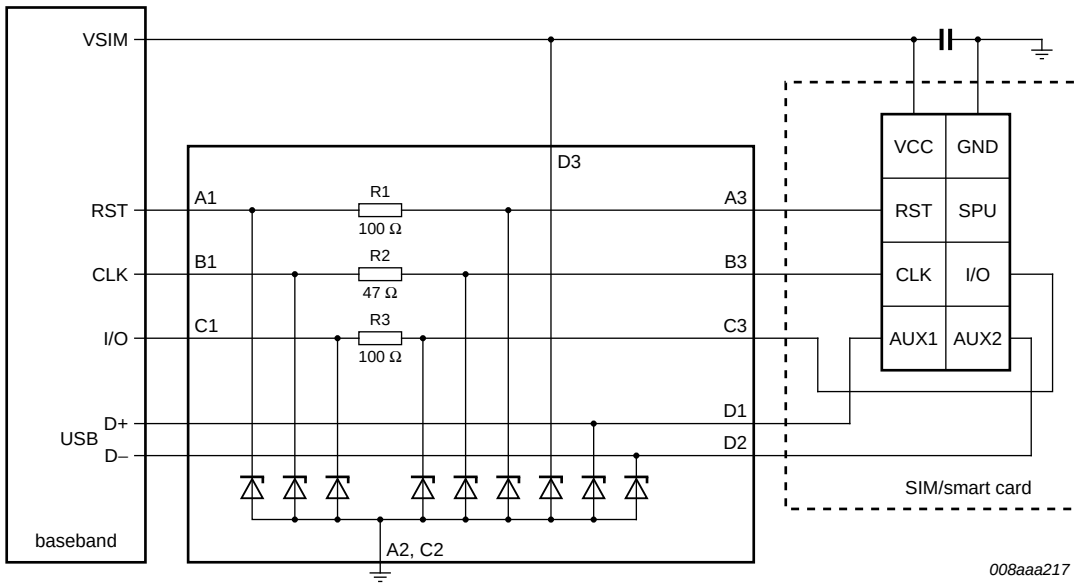


(1) Pin B1 to B3
(2) Pin A2 to A3
(3) Pin C1 to C3

Fig 3. IP4365CX11 and IP4366CX8: Insertion loss of (U)SIM EMI filter and ESD protection devices

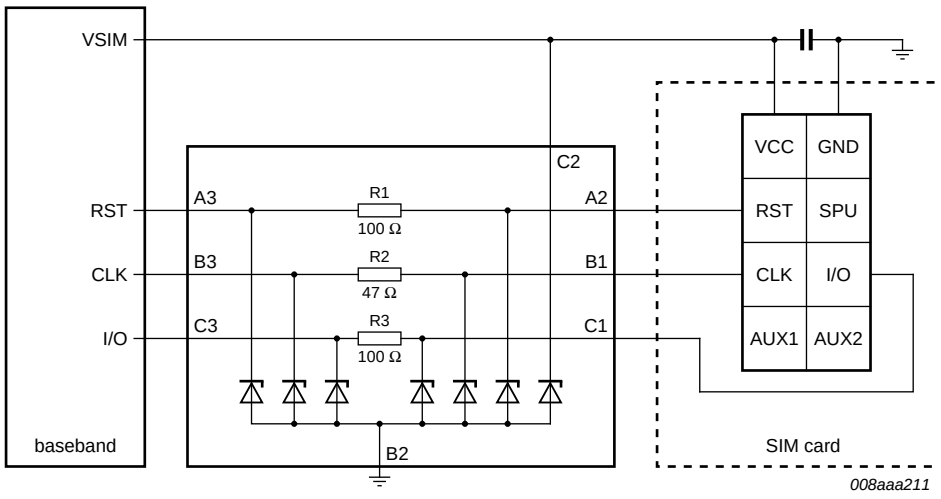
3.1 Application schematics

The following three application schematic diagrams demonstrate how the NXP SIM card EMI filter and ESD protection devices are used in a typical SIM interface application and also show the intrinsic structure of the different devices. Where possible, also the USIM USB interface protection is included in the schematic.



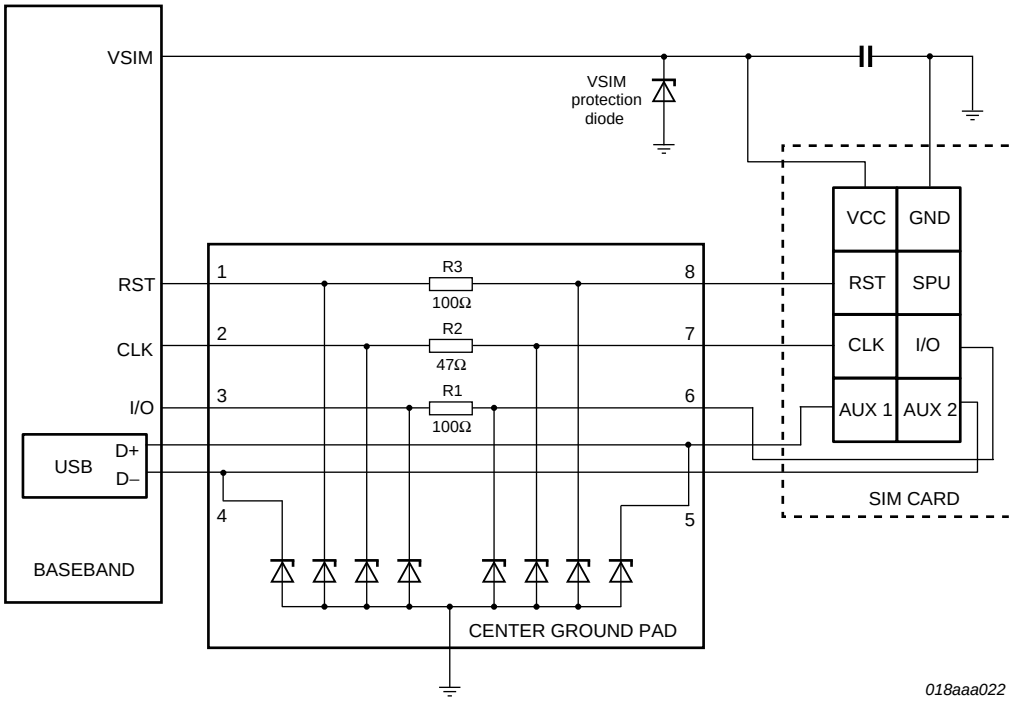
This is only one example. Dependent on layout constraints e.g. pins D1 can be swapped with D2 or channel A1-A3 can be swapped with channel C1-C3.

Fig 4. IP4366CX8 application schematic included USIM USB interface (AUX1, AUX2)



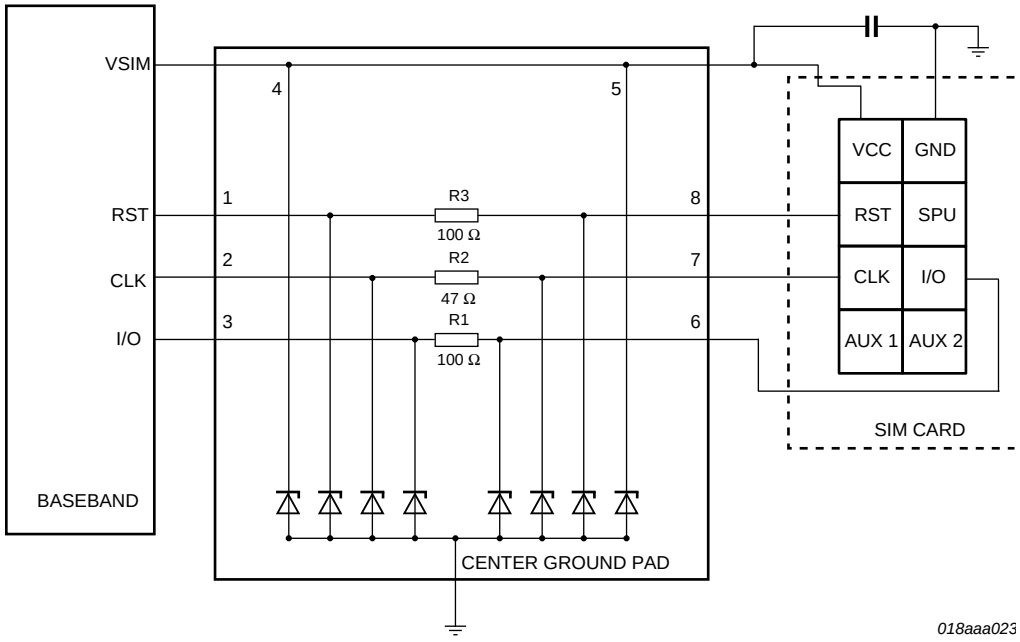
This is only one example. Dependent on layout constraints e.g. channel A1-A3 can be swapped with channel C1-C3.

Fig 5. IP4064CX8, IP4364CX8 and IP4366CX8 application schematic



This is only one example. Dependent on layout constraints e.g. channel 1-8 can be swapped with channel 3-6. Also USB ESD protection pin 4 and 5 can be exchanged. Due to both sides of the devices containing identical protection diodes, base band and SIM card side can be swapped, too.

Fig 6. IP4264CZ8 (-10, -20, -40) application schematic included USIM ESD protection



This is only one example. Dependent on layout constraints e.g. channel 1-8 can be swapped with channel 3-6. Due to both sides of the devices containing identical protection diodes, base band and SIM card side can be swapped, too.

Fig 7. IP4264CZ8 (-10, -20, -40) application schematic included VSIM ESD protection

4. NXP EMI filter and ESD protection devices investigation

In this chapter some basic EMI filter and ESD protection considerations based on the NXP SIM card EMI filter and ESD protection devices are explained. The first chapter seizes the calculations to evaluate the usage of the proposed filters, while the advantages with respect to ESD protection of these devices are demonstrated in the following chapter.

4.1 EMI filtering using NXP EMI filters (e.g. IP4364CX8)

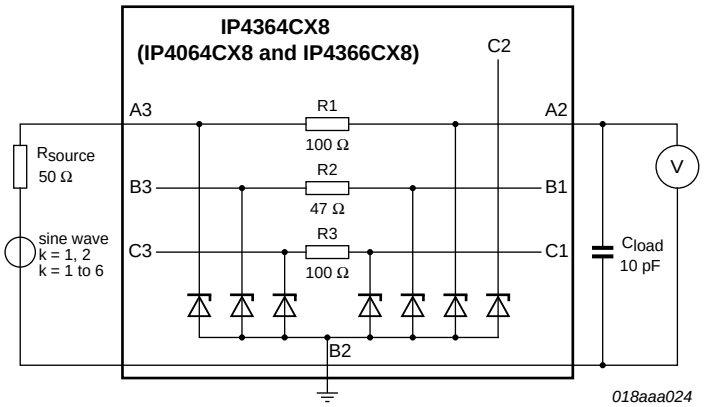
For the further investigations, electrical simulations based on APLAC models are used. The clock frequency for the following simulations is set to 5 MHz (even though 4 MHz is the maximum frequency for GSM) and the limit of 15 % / 70 % of 1.8 V for the high-level/low-level definition is kept to include some safety margin in the simulation. Using the same calculation as before, the maximum allowed rise time/fall time can be calculated to 9 % of the defined low-level/high-level window as 0.09 * 1/5 MHz = 18 ns.

In Figure 9 three simulation-results are compared showing the influence of the higher harmonics. For all three simulations a physical filter implementation taken from the NXP SIM card EMI filter and ESD protection device IP4364CX8 is used. A capacitive load from the SIM card of 10 pF is assumed and the driver series resistance is set to 50 Ω as depicted in Figure 8. These pi-filter (also called CRC-filter) EMI filter and ESD protection devices are basically build from two diodes and a channel resistor. The resistor values are aligned with the SIM card interface specification as reflected in Table 2, meaning the I/O and RST channels contain 100 Ω resistors while the CLK channel just contains a 47 Ω resistor.

One huge advantage of this type of pi-filter implementation is the good predictability of the filter solution with respect to the filter performance compared to discrete solutions just using a single capacitor in combination with a series resistor. In this example, the driver circuit shown in the schematic in Figure 8 contains a series resistor and is connected to the left side 'C' (diode at pin A3) which internally is connected to another resistor and the capacitance at right side of IP4364CX8 (diode of pin A2). So, by using only this single device, all three channels are automatically filtered using second-order low-pass filters which work similar in both directions.

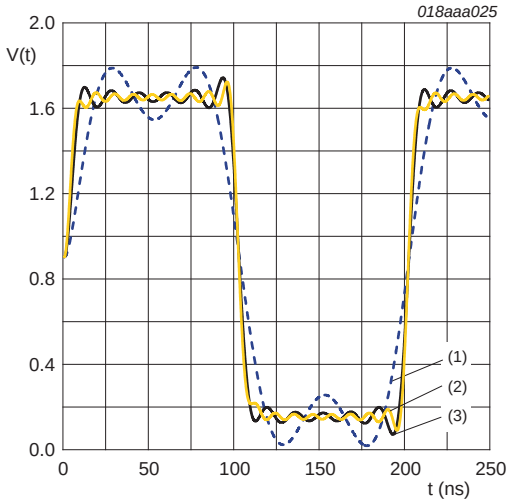
In case a discrete solution using one resistor and one capacitance (diode or small capacitor) is implemented, the filter will only work properly in one direction, which can create issues on the I/O bus.

One curve is simulated using the fundamental frequency plus the first harmonic only (k = 1, 2), one simulation is using the fundamental frequency plus five harmonics (k = 1 to 6) and the third simulation is using seven harmonics (k = 1 to 8) as a source signal.



IP4364CX8 simulation set-up

Fig 8. Simulation circuitry to setup a digital rectangular signal and evaluate its representation by sum of odd harmonics



Simulation results using k = 1,2 and k = 1 to 6

(1) k = 1, 2

(2) k = 1 to 8

(3) k = 1 to 6

Fig 9. Digital rectangular signal and its representation by sum of odd harmonics

The rise and fall time for all three waveforms is calculated within the 15 %/70 % window of a 1.8 V interface voltage level.

Table 4. rise time/fall time simulation results using IP4364CX8 and 10 pF load

Symbol	Parameter	Conditions	Result	Unit
t_r	rise time	15 % to 70 %		
		k = 1, 2	18.15	µs
		k = 1 to 6	7.20	µs
		k = 1 to 8	5.45	µs
t_f	fall time	70 % to 15 %		
		k = 1, 2	18.85	µs
		k = 1 to 6	7.85	µs
		k = 1 to 8	6.55	µs

From this, it can be derived, that for realistic signals such as e.g. k = 1 to 6, the rise time/fall time requirements can easily be fulfilled for the used 10 pF load.

In case the maximum specified load of 30 pF as listed in Table 2 is used, the values for k = 1 to 6 and k = 1 to 8 nearly double, but are still easily within the specified range.

The reason for the difference in rise and fall time is the changing junction capacitance of the diodes used in the IP4364CX8. Silicon-based diodes show a decrease of junction capacitance with a DC-bias voltage increase in reverse direction. A typical C = f(V) behavior of such a diode is shown in Figure 10.

Most EMI filter and ESD protection device will show a similar behavior. The gradient of the curve of the total filter is influenced e.g. by the diode break down voltage but also by parasitic elements, such a capacitance from pads to the substrate and may vary around the curve shown here.

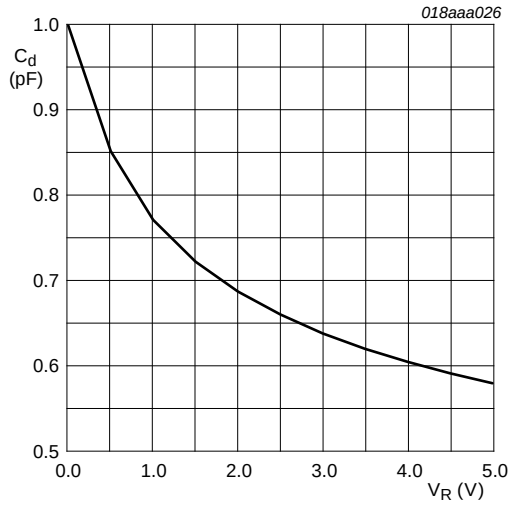


Fig 10. Diode capacitance as a function of reverse voltage; typical values

4.2 ESD protection using NXP EMI filters

A huge part of the silicon-based EMI filters and ESD protection devices use a so called pi-filter (also referred to as CRC or CLC filters, in case coils are used instead of resistors) structures. These are very effective to build an EMI filter with a broad stop band and at the same time help to achieve a very low ESD clamping voltage because of their clamping two-stage design.

Any incoming ESD strike is first clamped by the diode connected to the incoming pin and a major portion of the energy is derived to ground as indicated in Figure 11.

The typical clamping voltage of a single diode with similar capacitance as used in these EMI filter and ESD protection devices is in the range of several 10 V and can reach above 100 V if lower capacitance diodes are used.

The residual voltage/energy is then directed through the series resistor/coil to the second stage diode of the other pin which is typically connected to the sensitive circuit which it shall protect.

The channel resistor and the second diode act as a voltage divider, lowering the remaining ESD voltage to a very unspectacular level which typically exceeds either the diode's break-down voltage by a few volts only as depicted in Figure 12 (curve number 1) in case of a positive ESD strike or the diode forward voltage in case of a negative ESD discharge Figure 12 (curve number 2). The break-down voltage of the ESD protection diode of the measured device is around 7.1 V, the maximum peak clamping level of a positive discharge only reaches 10.8 V for a very short period in time of a few nanoseconds only.

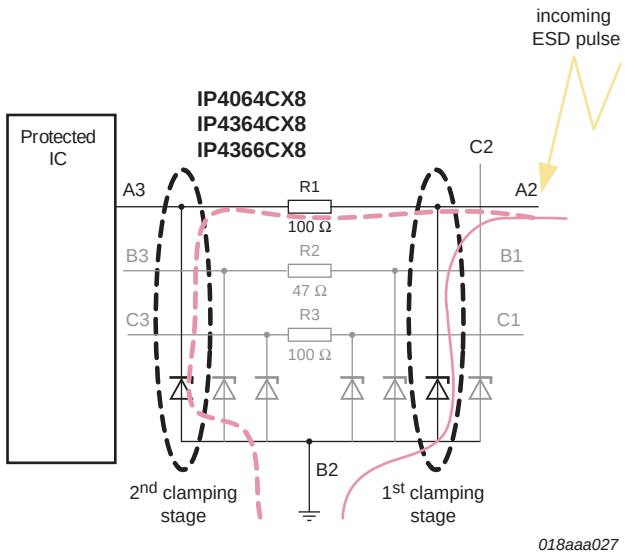
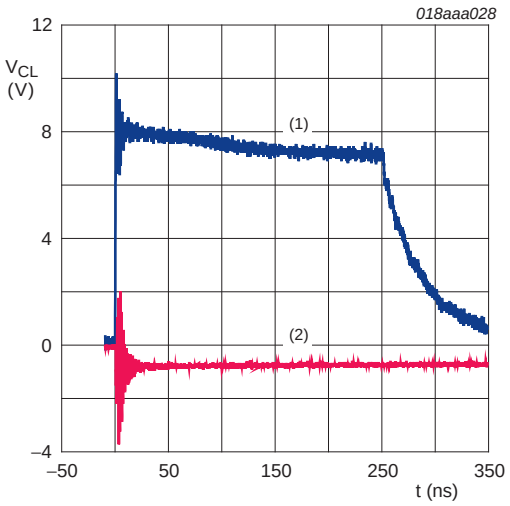


Fig 11. Current distribution scheme using a pi-filter structure



(1) Positive discharge

(2) Negative discharge

Fig 12. Typical clamping voltage at the second clamping stage of a pi-filter device (e.g. pin A3)

5. SIM interface, EMI filter and ESD protection devices application details

After the basic considerations in the former chapters, this chapter describes the details of the NXP EMI filter and ESD protection devices for SIM-interfaces.

Two basic scenarios are important for the SIM card application.

One is based on the assumption, that the involved interface driver I/O pins have enough driver strength to drive the attached capacitances (filter, card, holder, Printed-Circuit Board (PCB) traces etc.) with rise times/fall times which are short compared to the rise times/fall times at the filter output side using an unlimited driver strength.

The other scenario is based on designs using weak drivers, as the driver strength can typically be programmed in most base bands and SIM cards.

To reflect both considerations, two different sets of simulation are performed and the results for the various NXP ESD protection and EMI filters are listed in the following two chapters.

5.1 SIM interface considerations using strong drivers

To determine the maximum possible signal frequency that complies with the criteria listed in Table 2, an Input Output Buffer Information Specification (IBIS) model (74AVC2T45 from the (www.nxp.com) web page) representing the driver and APLAC/SPICE models of the filters are used.

The interface voltage level investigated is 1.8 V (class C) and the voltage low-levels and high-levels are set to 15 % and 70 % respectively. In this voltage level window, the required t_r/t_f (rise time/fall time) is calculated to be less than 9 % of the signal period

$$t_r / t_f = 0,09 \times \frac{1}{f}$$

Both available channel types, $R_{s(ch)}$ = 47 Ω and 100 Ω are investigated. Typically, the CLK signal will be propagated via the 47 Ω channel and therefore is determining the maximum signal speed, as the I/O is only running on the half clock-frequency.

A one channel simulation set-up is depicted in Figure 13 and shows the additional, package dependent, parasitic series inductors implemented in the EMI filter APLAC/SPICE models. For each simulation, the diode capacitance and parasitic inductor values are adopted to the individual implemented values per device.

The SIM card interface, the card holder and the PCB's parasitic capacitances are summarized in a lumped 30 pF capacitor on the right side of the schematic.

Due to the decrease of DC-voltage level of the filter's channel capacitance as shown in Figure 10, the evaluation of a class C interface level also embraces the class B type interface.

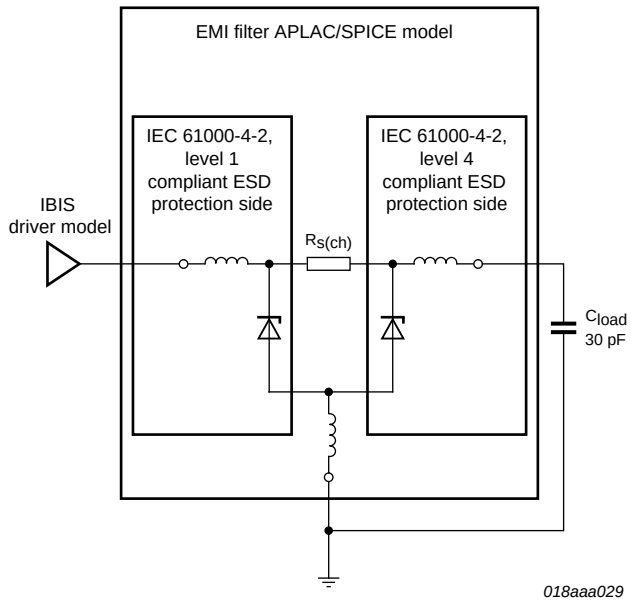


Fig 13. Basic APLAC/SPICE simulation set-up schematic of a single EMI filter channel

The SIM card interface, the card holder and the PCB's parasitic capacitances are summarized in a lumped 30 pF capacitor on the right side of the schematic.

A first approximation of the maximum signal frequency can be calculated from the f_{-3dB} point of the filter built from $R_{S(ch)}$, the external capacitive load (C_L) and the IEC61000-4-2, level 4 diode capacitance.

$$f_{-3dB} = \frac{1}{2\pi R_{S(ch)}(C_{load} + C_{diode})} = \frac{1}{2\pi 100\Omega(30pF + 12pF)} \cong 37MHz$$

This calculation is based on the assumption, that the driver is strong enough not to be the limiting factor so the aperture does not work in a slewing mode. The investigation conducted in Section 6.1 and Section 4.1 shows that the maximum signal frequency is typically less or equal to $^1\vee_3$ of f_{-3dB}, so in this case, it is approximately 12 MHz.

The equivalent rise time/fall time is calculated to be $t_r / t_f = 0,09 \times \frac{1}{f} = 7,5\ \text{ns}$.

The values simulated for the IP4064CX8 and IP4364CX8 listed in Table 5 show a t_f of 8.6 ns. This value implies, that the first order calculation is too optimistic to use the result without some deeper investigation or an additional safety margin of 10 % to 15 %.

Nevertheless, the difference is small enough to give a good feeling about the order of magnitude of the possible signal speed.

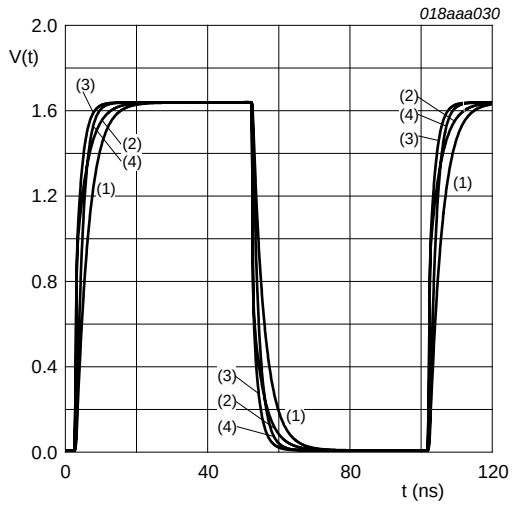
Further more, the example calculated here and also the simulation results listed in Table 5 are based on the assumption of a 30 pF from the SIM card interface, the card holder and the PCB parasitic capacitance, while most SIM cards used today will support a much lower pin capacitance!

Table 5. typical signal frequency and timing simulation results

Product name	Channel capacitance (pF) V_{DC} = 0 V		Typical signal frequency[1] (MHz)		Typical tr/tf (ns)		Package
	typ	max	$R_{s(ch)}$ = 47 Ω	$R_{s(ch)}$ = 100 Ω	$R_{s(ch)}$ = 47 Ω	$R_{s(ch)}$ = 100 Ω	
IP4064CX8	-	20	16	10	3.7/5.3	5.9/8.6	WLCSP, 0.5 mm pitch
IP4364CX8	-	20					WLCSP, 0.4 mm pitch
IP4366CX8	10	12	20	12	2.9/4.1	4.5/6.6	
IP4365CX11	10	12					
IP4264CZ8-10	10	12	<tbd>	<tbd>	<tbd>	<tbd>	QFN-type, 0.4 mm pitch
IP4264CZ8-20	17	20	16	10	3.3/4.8	5.3/7.7	
IP4264CZ8-40	35	40	15	8	4.1/5.8	6.3/9.3	

[1] The signal frequencies listed are the next lower available value according the possible frequencies listed under TA1 in ISO/IEC 7816-3:2006(E). The driver model used for the simulation determining the maximum clock frequency base on high-low levels of 15 % and 70 % of the nominal signal level of 1.8 V (class B) is based on an IBIS model of NXP's drive/level shifter device 74AVC2T45. Please refer to the NXP web site (www.nxp.com) for further details.

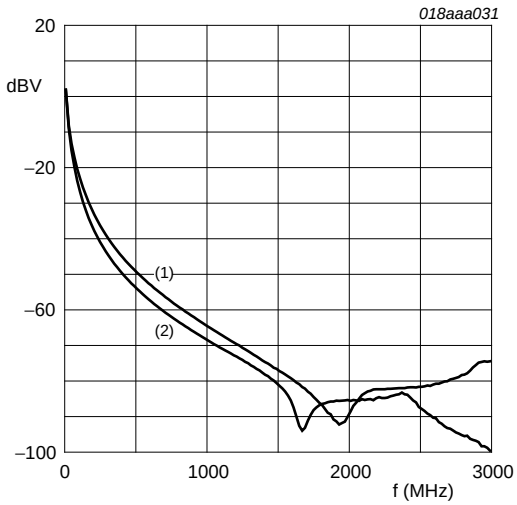
The simulated input and output signal waveform for nominal values of the IBIS model driver stage (same as for the analysis done for Table 5) and the IP4064CX8 EMI filter / ESD protection device (47 Ω channel, pins B1 to B3) are depicted in Figure 14. A Fast Fourier Transform (FFT) analysis, limited to just the odd harmonics of the fundamental signal frequency (10 MHz) is depicted in Figure 15. The analysis is performed using the setup as shown in Figure 13 and uses two different load capacitances. One simulation is done with a 30 pF load, the second simulation is using a 10 pF load.



Input and output; 47 W channel

(1) SIM interface 30 pF load
(2) Driver side to 30 pF load
(3) Driver side to 10 pF load
(4) SIM interface 10 pF load

Fig 14. IP4064CX8: transient simulation results



FFT result, limited to odd harmonics (10 MHz signal) of output signals.

(1) 10 pF load
(2) 30 pF load

Fig 15. IP4064CX8: FFT using different capacitive loads and a 74AVC2T45 IBIS model

5.2 SIM interface considerations using weak drivers

So far, all considerations were based on the assumption that the interface drivers are not a limiting factor to achieve rise times/fall times as required by the SIM card specification for certain frequencies (see Table 2 for details).

In case weaker drivers or drivers with a higher series resistor are used, the total data transmission channel capacitance including the EMI filter, the SIM interface, the card holder and parasitics has to be taken into account.

Even though weak drivers have the advantage to generate less EMI issues, as they generate weaker slopes and less overshots, they also increase the risk of being more receptive to EMI disturbances!

Due to this, an EMI filter can't be spared to guarantee proper operation of the interface.

Based on the technical boundary conditions as listed in Table 2, a 9 % value of the clock period is regarded to be the maximum rise time/fall time.

For a simple first order calculation we assume, that all capacitances such as EMI filter, SIM card, and parasitic capacitors can be summarized in one lumped capacitor and that the series resistor of the EMI filter is only a minor contributor to the rise time/fall time in this scenario. With these assumption, the rise time/fall time of a circuit similar to Figure 13 but using a constant current source, representing the average current of the driver circuit, can be calculated to:

$$I_{average} = \frac{C \cdot T}{\Delta U} = \frac{(C_{SIMcard} + C_{EMI-filter}) \cdot ((0,7-0,2) \cdot V_{I/O})}{t_r(ort_f)}$$

with $C_{SIMcard}$ = 30 pF, $V_{I/O}$ = 1.8 V (class C) and $C_{EMI\ filter}$ = either 20 pF for e.g. IP4364CX8 or 12 pF for e.g. IP4366CX8 (see Table 5 for the specified maximum channel capacitance values per device).

An overview of average current driving requirements in dependence of the EMI filter used and the required clock speed is given in Table 6.

Table 6. Driving current calculation based on the EMI filter capacitance

Table gives only a rough guidance for the setting of driver currents, as most CMOS-based digital driver circuits show a relatively strong voltage dependency.

Clock frequency	clock period (ns)	9 % of period (max t_r, t_f; ns)	$I_{average}$ (mA)	
			$C_{EMI\ filter}$ = 12 pF	$C_{EMI\ filter}$ = 20 pF
1	1000	90	0.42	0.5
2	500	45	0.84	1
4	250	22.5	1.68	2
5	200	18	2.1	2.5
8	125	11.25	3.36	4
10	100	9	4.2	5
12	83.3	7.5	5.04	6
14	71.43	6.42	5.88	7
15	66.67	6	6.3	7.5
16	62.5	5.62	6.72	8
20	50	4.5	8.4	10

The values calculated clearly show, that in cases where only limited drive currents are available, the lower channel capacitance devices such as IP4365CX11, IP4366CX8 or IP4264CZ8-10 should be used. This results in an ~15 % lower current requirements (based on maximum capacitance values).

In case the SIM card pin capacitance is e.g. 20 pF only, the relative influence of the filter channel capacitance is even bigger (~20 % for $C_{SIMcard}$ = 20 pF).

6. Basic EMI considerations

Especially the GSM standard contains harsh requirements for noise/EMI transmitted to the mobile phone receiver part.

Unfortunately, nearly every digital interface creates either conducted EMI and/or radiated EMI. Furthermore, every trace on a PCB conducting signals (not DC levels) is acting as a radiator and as a receiver antenna.

The transmitted frequencies are related to the signal conducted on the trace, its harmonics and also on the harmonics created within the transmission connection, creating e.g. reflection and distortion of the fundamental signal.

The radiated signal strength is related to the antenna matching with respect to the individual transmitted frequency (longer traces mean better reception and transmission of lower frequencies, shorter traces just support transmission and reception of higher frequencies).

To minimize radiation from and to digital interface, most mobile phones make extensive use of shielding. Functional blocks are enclosed in a metal shielded “chamber” representing a Faraday’s cage. This works perfectly fine with interfaces that do not require an external interface.

As the SIM card is accessible to the user, it can’t be integrated into a completely shielded area. At the same time, the SIM card is a crucial part of all GSM and 3G phones. Due to the number of different manufacturers and the long period of its existence, numerous versions of SIM cards with various different electrical parameters are on the market.

Any filter implemented in the SIM interface has to ensure proper operation of at least class B and class C type SIM cards (assuming, that 5 V SIM cards are no longer supported by any appliances which are designed at this point in time), regardless of its pin capacitance plus allow to operate the card at it’s specified maximum frequency (if supported by the mobile chip set interface) without violating any timing or voltage level constraint.

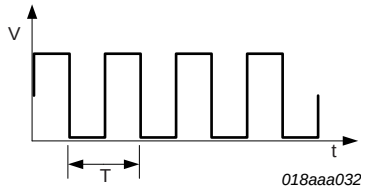
Typically low pass filters are used to protect mobile phones from EMI disturbances from and to digital buses.

The pass-band bandwidth and attenuation is determined by the digital interface requirements such as fundamental frequency (e.g clock speed or bits per second), the DC level attenuation (if relevant) and the rise time and fall time requirements. To achieve fast rise time and fall time, the number of harmonics has to be as high as possible while at the same time, the attenuation at the typical mobile frequencies of 840 MHz and above shall be attenuated as much as possible.

The relation between filter bandwidth, filter order, respectively the steepness of the roll-off, and rise time and fall time requirements is summarized in the next section.

6.1 Digital signals, harmonics, bandwidth and rise time/fall time

Digital signals, in this case rectangular periodic signals, so e.g. a voltage alternating between two different voltage levels, can be express as the sum of its harmonic frequencies. A rectangular signal as show in Figure 16 can be described as the sum of its odd harmonics, which are individually weighted.



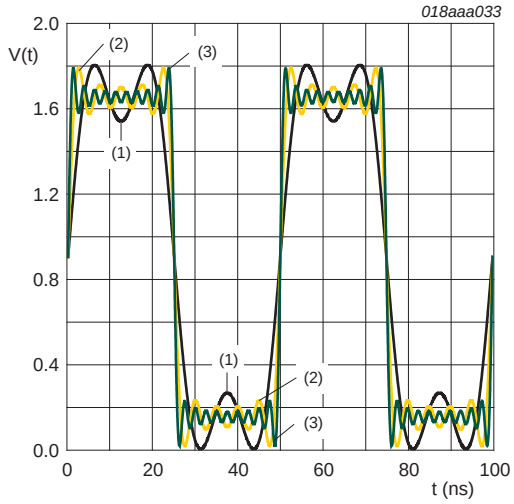
$$V(t) = A_0 + \sum_{k=1}^{\infty} A_k \frac{sin((2k-1)\cdot\omega_0\cdot t)}{2k-1}$$

Fig 16. Digital rectangular signal and its representation by sum of odd harmonics

For k = 1, the equation in Figure 16 results just in a sine wave with the offset A_0, amplitude A_1 and frequency f_0. Several different wave forms using different numbers of harmonics are depicted in Figure 17.

One difference between the various graphs is the difference in the rise time and fall time (~1/slope at V(t)/2), which is decreasing with an increase in the number of harmonics. While the waveforms for k_{max} = 2 and k_{max} = 5 show a noticeable difference in the gradient, the waveforms k_{max} = 5 and k_{max} = 10 differ only slightly. All three depicted waveforms show nearly identical minimum and maximum values.

The lowest rise time/fall time (higher gradient of the curve), occurs at the center of the amplitude and can be calculated by derivation of the formula shown in Figure 16.



$$\frac{d}{dt}\left(A_0 + \sum_{k=1}^{\infty} A_k \cdot \frac{sin((2k-1)\cdot\omega_0\cdot t)}{2k-1}\right) = \sum_{k=1}^{\infty} \omega_0 \cdot A_k cos((2k-1)\cdot\omega_0\cdot t)$$

assuming $cos(\omega_0 \cdot t) = 1$ and $\frac{\Delta V}{\Delta t}max = A_k \cdot (\omega_0 \cdot k)$

(1) k = 1,2

(2) k = 1,2...5

(3) k = 1,2...10

Fig 17. Digital rectangular signal and its representation by sum of odd harmonics

For an example we are using the signal level of a class C SIM card interface, the signal peak-to-peak amplitude is set to 1.8 V, representing the specified voltage level.

To calculate value for the coefficients A_0, A_1, A_2 etc., we assume that A_k is identical for all values of k and we only use values k = 1 and k = 2 neglecting the higher values of k. Looking at the graphs in Figure 17, the error is minor and the tolerance in any real life application will have much more impact on the signal than this deviation.

Further more, we want to filter all higher harmonics to avoid EMI, so the contribution should be small by purpose!

To achieve $V(t)_{max}$ = 1.8 V and $V(t)_{min}$ = 0 V, A_0 has to be:

$$1/2*(V(t)_{max} - V(t)_{min}) = 0,9\ \text{V}$$

For the calculation of $A_1 = A_2 = A_x$, the equation in Figure 16 has to be derivated with respect to time 't' as shown in Figure 17. To calculate the first local maximum of the equation, the first derivation has to be '0' (as we can see in the graphs in Figure 17, the first local maximum also seems to be the absolute maximum, see calculation below).

Digital rectangular signal with frequency and calculation of minimum rise time and fall time:

$$\sum_{k=1}^{\infty} \omega_0 \cdot A_k \cos((2k-1)\cdot\omega_0\cdot t) \text{ with k = 1 and k = 2} \tag{1}$$

$$\frac{d}{dt}\left(A_0 + \sum_{k=1}^{\infty} A_k \frac{\sin((2k-1)\cdot\omega_0\cdot t)}{2k-1}\right) = 0 \tag{2}$$

$$= A_1\cos(\omega_0\cdot t) + A_2\cos(3\cdot\omega_0\cdot t) \text{ with } A_1 = A_2 = A_x \tag{3}$$

$$\text{to solve this, we use: } \cos(A) + \cos(B) = 2\cos\frac{A+B}{2}\cdot\cos\frac{A-B}{2} \tag{4}$$

$$2\cdot\cos(2\cdot\omega_0\cdot t)\cdot\cos(-\omega_0\cdot t) = 0 \tag{5}$$

Two possible zero points (with multiples every π) are:

$$\text{for the left term: } \cos(2\cdot\omega_0\cdot t) = 0 \tag{6}$$

$$\cos(2\cdot\omega_0\cdot t) = 0 \text{ leading to } t = \frac{\pi}{4\cdot\omega_0} = \frac{1}{8\cdot f_0} \tag{7}$$

$$\text{for the right term: } \cos(-\omega_0\cdot t) = \cos(\omega_0\cdot t) = 0 \text{ leading to } t = \frac{1}{4\cdot f_0} \tag{8}$$

From the pulse shape for k = 2, we can derive that the first local optimum is also the global maximum and the second solution is a local minimum.

To calculate the coefficients A_x, we use: $t = \frac{1}{8\cdot f_0}$ in the equation of Figure 16. This leads to:

$$V\left(t = \frac{1}{8\cdot f_0}\right) = A_0 + A_x\sin\left(\frac{\omega_0}{8\cdot f_0}\right) + A_x\frac{\sin\left(\frac{3\cdot\omega_0}{8\cdot f_0}\right)}{3} \tag{9}$$

$$V\left(\frac{1}{8\cdot f_0}\right) = A_0 + A_x\sin\left(\frac{1}{4}\cdot\pi\right) + A_x\frac{\sin\left(\frac{3}{4}\cdot\pi\right)}{3} \tag{10}$$

$$V\left(\frac{1}{8\cdot f_0}\right) = A_0 + A_x\left(\frac{2}{3}\cdot\sqrt{2}\right) \tag{11}$$

We know that the signal is symmetrically oscillating around A_0 = 0.9 and $V(t)_{max}$ = 1.8, resulting in:

$$A_x = \frac{\dot{0},9 \cdot 3}{2 \cdot \sqrt{2}} \cong 0,\dot{9}546 \text{ for k = 1 and 2}$$

Now we have $A_1 = A_2$ = 0.9546 and can use this to calculate the maximum and minimum voltage level, the slope and the rise time/fall time etc. Using target values from Table 2, for a worst case calculation we want to achieve a t_r and t_f of 9 % of the minimum clock period which is 0.09 * 1/20 MHz = 4.5 ns. The voltage step from low to high level (for the I/O) limits are set from 15 % to 70 % of 1.8 V equaling a step of 0.99 V. As this is a worst case consideration, the minimum limit is set to a lower value than the actual specified limit. The resulting gradient of a rising or falling edge has to be:

$$|\Delta V/\Delta t| = 0,99 \text{ V}/4,5 \text{ ns} = 220 \times 10^6 \text{ V}/s^1$$

Using the equation from Figure 17, A_0 = 0.9, $A_1 = A_2$ = 0.9546 (see above), the slope of a rectangular signal just using the fundamental plus one harmonic waveform can be calculated to 239.9E6 V/s.

The maximum slope of the rising or falling edge is already exceeding the minimum requirement to achieve the timing requirements of $\Delta V/\Delta t$ = 0.99 V/4.5 ns = 220E6 V/s. Even though the gradient is below the calculated maximum for most of the rising or falling slopes, the higher harmonics also contribute to the signal although they might be attenuated by a filter of second or third order.

1. Other card interface such as SD2.0 for the SD-card put to 50 MHz clock or the MMC interface up to 52 MHz clock-speed generally have similar or weaker requirements.

7. Conclusion

NXP Semiconductors offers a comprehensive portfolio of USIM/SIM and smart card interface conditioning and protection devices.

These devices integrate system level ESD protection and EMI filtering in a very small footprint area.

As shown before, the devices are optimized for compliance with ISO/IEC 7816-3 and ISO/IEC 7816-12 interfaces in terms of channel capacitance and serial resistance, some also supporting integrated USB1.1 interfaces.

They protect from destruction from system level ESD and also prevent disturbance of e.g. wireless interfaces from the harmonics of the USIM/SIM interface while occupying the minimum of PCB space possible.

NXP’s strategy to offer footprint-compatible devices with different filter parameters enables uses to quickly adopt their designs to changing requirements such as clock speed or interface capacitance without the necessity of a re-design of the PCB layout.

All devices presented support a simple PCB layout, reduce the risk of EMI due to complex layout of scattered discrete components and allow to minimize compliance testing.

The high integration level and the final test of each device before shipment also improve the overall quality, as the Integrated Discretes' components reduce the number of individual components, solder joints and pick and places processes.

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