



IP4786CZ32S

**DVI and HDMI interface ESD and overcurrent protection,
DDC/CEC buffering, hot plug detect and backdrive protection**

Rev. 2 — 11 July 2013

Product data sheet

1. General description

The IP4786CZ32S is designed to protect High-Definition Multimedia Interface (HDMI) transmitter host interfaces. It includes HDMI 5 V overcurrent / overvoltage protection, Display Data Channel (DDC) buffering and decoupling, Hot Plug Detect (HPD), backdrive protection, Consumer Electronic Control (CEC) buffering and decoupling, and ± 8 kV contact ElectroStatic Discharge (ESD) protection for all I/Os in accordance with the IEC 61000-4-2, level 4 standard.

The IP4786CZ32S incorporates Transmission Line Clamping (TLC) technology on the high-speed Transition-Minimized Differential Signaling (TMDS) lines to simplify routing and help reduce impedance discontinuities. All TMDS lines are protected by an impedance-matched diode configuration that minimizes impedance discontinuities caused by typical shunt diodes.

The enhanced 60 mA overcurrent / overvoltage linear regulator guarantees HDMI-compliant 5 V output voltage levels with up to 6.5 V inputs.

The DDC lines use a new buffering concept which decouples the internal capacitive load from the external capacitive load for use with standard Complementary Metal Oxide Semiconductor (CMOS) or Low Voltage Transistor-Transistor Logic (LVTTTL) I/O cells down to 1.8 V. This buffering also re-drives the DDC and CEC signals, allowing the use of longer or cheaper HDMI cables with a higher capacitance. The internal hot plug detect module simplifies the application of the HDMI transmitter to control the hot plug signal.

All lines provide appropriate integrated pull-ups and pull-downs for HDMI compliance and backdrive protection to guarantee that HDMI interface signals are not pulled down if the system is powered down or enters Standby mode. Only a single external capacitor is required for operation.

2. Features and benefits

- HDMI High-Speed, 340 MHz, deep color and HDMI Ethernet and Audio return Channel (HEAC) compatible
- Impedance matched 100 Ω differential transmission line ESD protection for TMDS lines (± 10 Ω). No Printed-Circuit Board (PCB) pre-compensation required
- Simplified flow-through routing utilizing less overall PCB space
- DDC capacitive decoupling between system side and HDMI connector side and buffering to drive cable with high capacitive load (> 700 pF/25 m)
- All external I/O lines with ESD protection of at least ± 8 kV in accordance with the IEC 61000-4-2, level 4 standard
- Hot plug detect module



- CEC buffering and isolation, with integrated backdrive-protected 26 k Ω pull-up
- Robust ESD protection without degradation after repeated ESD strikes
- Highest integration in a small footprint, PCB level, optimized RF routing, 32-pin HXQFN leadless package

3. Applications

- The IP4786CZ32S can be used for a wide range of HDMI source devices, consumer and computing electronics:
 - ◆ Tablet and notebook PCs
 - ◆ Portable Media Players
 - ◆ Digital Still Cameras (DSC)
 - ◆ High-Definition (HD) and Standard-Definition (SD) Blu-ray and DVD players
 - ◆ Set-top boxes (STB)
 - ◆ PC graphic cards
 - ◆ Game consoles
 - ◆ HDMI picture performance quality enhancer modules
 - ◆ Digital Visual Interface (DVI)

4. Ordering information

Table 1. Ordering information

Type number	Package		
	Name	Description	Version
IP4786CZ32S	HXQFN32	plastic thermal enhanced extremely thin quad flat package; no leads; 32 terminals; body 4 × 4 × 0.5 mm	SOT1318-1

5. Functional diagram

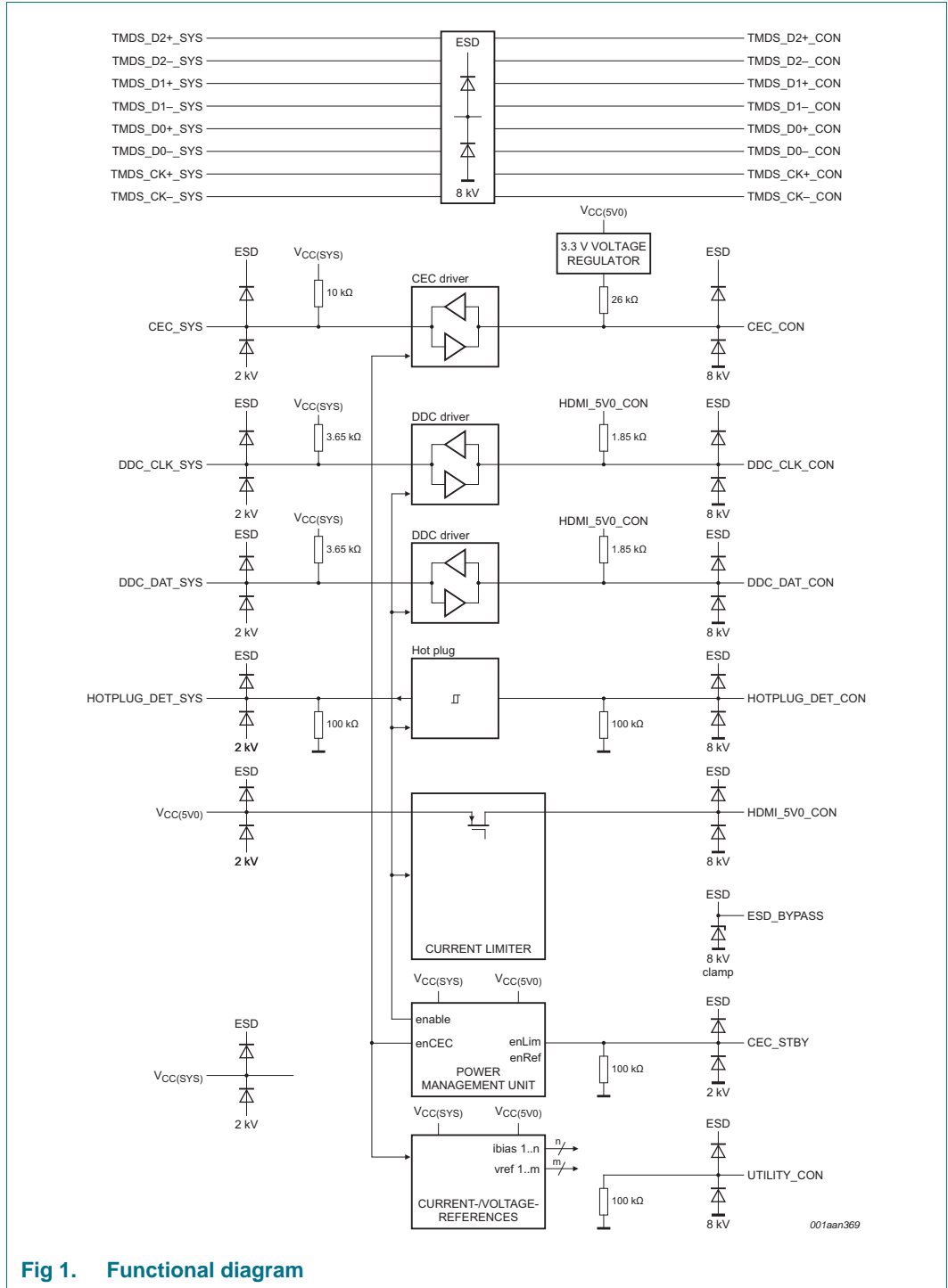
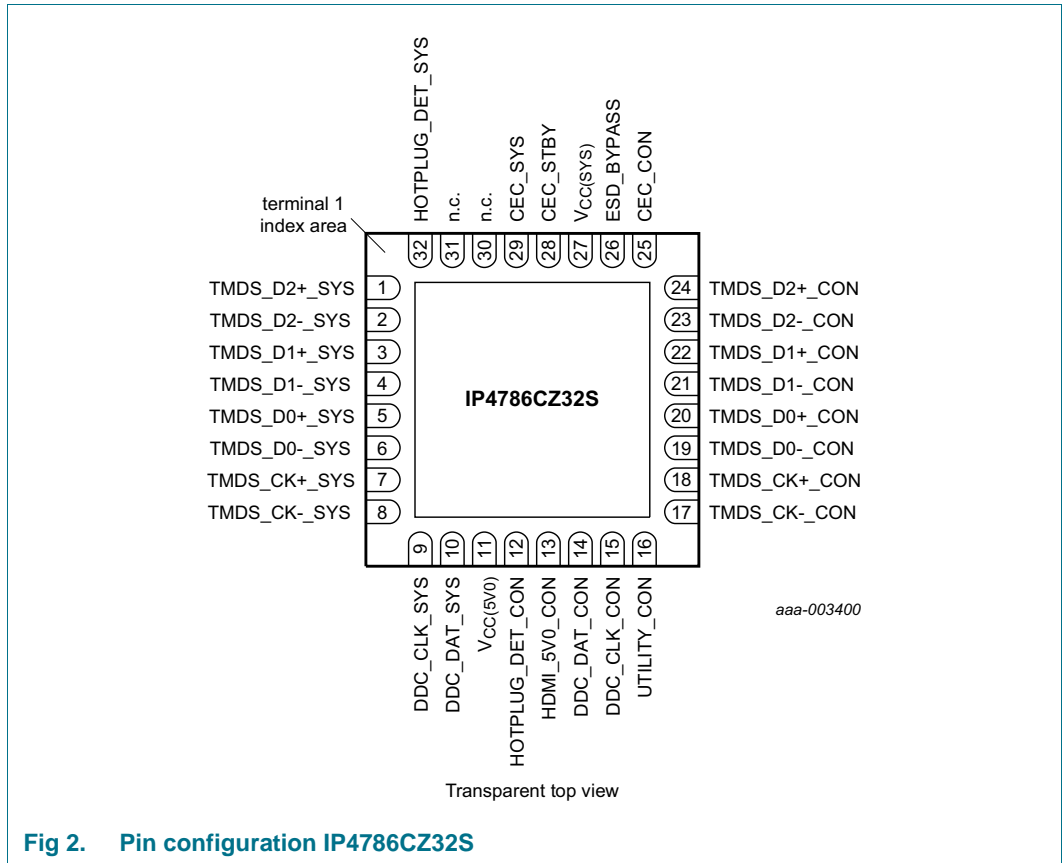


Fig 1. Functional diagram

6. Pinning information

6.1 Pinning



6.2 Pin description

Table 2. Pin description

Pin	Name	Description
1	TMDS_D2+_SYS	TMDS to ASIC inside system
2	TMDS_D2-_SYS	TMDS to ASIC inside system
3	TMDS_D1+_SYS	TMDS to ASIC inside system
4	TMDS_D1-_SYS	TMDS to ASIC inside system
5	TMDS_D0+_SYS	TMDS to ASIC inside system
6	TMDS_D0-_SYS	TMDS to ASIC inside system
7	TMDS_CK+_SYS	TMDS to ASIC inside system
8	TMDS_CK-_SYS	TMDS to ASIC inside system
9	DDC_CLK_SYS	DDC clock system side
10	DDC_DAT_SYS	DDC data system side
11	V _{CC(5V0)}	5 V supply input
12	HOTPLUG_DET_CON	hot plug detect connector side
13	HDMI_5V0_CON	5 V overcurrent out to connector

Table 2. Pin description ...continued

Pin	Name	Description
14	DDC_DAT_CON	DDC data connector side
15	DDC_CLK_CON	DDC clock connector side
16	UTILITY_CON	utility line ESD protection
17	TMDS_CK-_CON	TMDS ESD protection to connector
18	TMDS_CK+_CON	TMDS ESD protection to connector
19	TMDS_D0-_CON	TMDS ESD protection to connector
20	TMDS_D0+_CON	TMDS ESD protection to connector
21	TMDS_D1-_CON	TMDS ESD protection to connector
22	TMDS_D1+_CON	TMDS ESD protection to connector
23	TMDS_D2-_CON	TMDS ESD protection to connector
24	TMDS_D2+_CON	TMDS ESD protection to connector
25	CEC_CON	CEC signal connector side
26	ESD_BYPASS	ESD bias voltage
27	V _{CC(SYS)}	supply voltage for level shifting
28	CEC_STBY	CEC Standby mode control (LOW for lowest power, CEC-only mode)
29	CEC_SYS	CEC I/O signal system side
30	n.c.	not connected
31	n.c.	not connected
32	HOTPLUG_DET_SYS	hot plug detect system side
ground pad	GND	ground

7. Limiting values

Table 3. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V _{CC(5V0)}	supply voltage (5.0 V)		GND – 0.5	6.5	V
V _I	input voltage	I/O pins	GND – 0.5	5.5	V
V _{ESD}	electrostatic discharge voltage	IEC 61000-4-2, level 4 (contact)	[1] -	±8	kV
		IEC 61000-4-2, level 1 (contact)	[2] -	±2	kV
P _{tot}	total power dissipation	DDC operating at 100 kHz; CEC operating at 1 kHz; 50 % duty cycle; CEC_STBY = HIGH; no current at HDMI_5V0_CON	-	50	mW
		DDC and CEC bus in idle mode; CEC_STBY = HIGH; no current at HDMI_5V0_CON	-	3.0	mW
		DDC and CEC bus in idle mode; CEC_STBY = LOW	-	1.0	mW
T _{amb}	ambient temperature		-25	+85	°C
T _{stg}	storage temperature		-55	+125	°C

[1] Connector-side pins (typically denoted with “_CON” suffix) to ground.

[2] System-side pins: CEC_SYS, DDC_DAT_SYS, DDC_CLK_SYS, HOTPLUG_DET_SYS, CEC_STBY, V_{CC(SYS)} and V_{CC(5V0)}.

8. Static characteristics

Table 4. Supplies

$T_{amb} = -25\text{ }^{\circ}\text{C}$ to $+85\text{ }^{\circ}\text{C}$ unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{CC(5V0)}$	supply voltage (5.0 V)		[1] 4.5	5.0	6.5	V
$V_{CC(SYS)}$	system supply voltage		1.62	3.3	5.5	V

- [1] The IP4786CZ32S contains a 5 V voltage regulator function for higher input voltages. Any input voltage of $4.925\text{ V} < V_{CC(5V0)} < 6.50\text{ V}$ provides HDMI-compliant output levels of 4.8 V to 5.3 V on HDMI_5V0_CON.

Table 5. TMDS protection circuit

$T_{amb} = -25\text{ }^{\circ}\text{C}$ to $+85\text{ }^{\circ}\text{C}$ unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
TMDS channel						
$Z_{i(dif)}$	differential input impedance	TDR measured; $t_r = 200\text{ ps}$		90	100	110 Ω
C_{eff}	effective capacitance	equivalent shunt capacitance for TDR minimum; $t_r = 200\text{ ps}$	[1][2] -	0.6	-	pF
Protection diode						
V_{BRzd}	Zener diode breakdown voltage	$I = 1.0\text{ mA}$		6.0	-	9.0 V
r_{dyn}	dynamic resistance	surge; $I = 1.0\text{ A}$; IEC 61000-4-5/9				
		positive transient		-	1.0	- Ω
		negative transient		-	1.0	- Ω
		TLP	[3]			
		positive transient		-	1.0	- Ω
		negative transient		-	1.0	- Ω
I_{bck}	back current	$V_{CC(5V0)} < V_{ch(TMDS)}$	[4][5] -	0.1	1.0	μA
I_{LR}	reverse leakage current	$V_I = 3.0\text{ V}$		-	1.0	μA
V_F	forward voltage			-	0.7	V
$V_{CL(ch)trt(pos)}$	positive transient channel clamping voltage	100 ns TLP; 50 Ω pulser at 50 ns		-	8.0	V

- [1] This parameter is guaranteed by design.
- [2] Capacitive dip at HDMI Time Domain Reflectometer (TDR) measurement conditions.
- [3] ANSI-ESD SP5.5.1-2004, ESD sensitivity testing Transmission Line Pulse (TLP) component level method 50 TDR.
- [4] Signal pins:
TMDS_D0+_CON, TMDS_D0-_CON, TMDS_D1+_CON, TMDS_D1-_CON, TMDS_D2+_CON, TMDS_D2-_CON, TMDS_CK+_CON, TMDS_CK-_CON,
TMDS_D0+_SYS, TMDS_D0-_SYS, TMDS_D1+_SYS, TMDS_D1-_SYS, TMDS_D2+_SYS, TMDS_D2-_SYS, TMDS_CK+_SYS and TMDS_CK-_SYS.
- [5] Backdrive current from TMDS_x_SYS and TMDS_x_CON pins to local $V_{CC(5V0)}$ bias rail at power-down. Device does not block backdrive current leakage through the device to/from ASIC I/O pins connected to TMDS_x_SYS pins.

Table 6. HDMI_5V0_CON $T_{amb} = -25\text{ }^{\circ}\text{C}$ to $+85\text{ }^{\circ}\text{C}$ unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit	
r_{dyn}	dynamic resistance	TLP	[1]				
		positive transient	-	1.0	-	Ω	
		negative transient	-	1.0	-	Ω	
V_{CL}	clamping voltage	100 ns TLP; 50 Ω pulser at 50 ns	-	8	-	V	
$I_{O(max)}$	maximum output current	$V_{(HDMI_5V0_CON)} = 4.8\text{ V}$	55	-	-	mA	
I_{bck}	back current	$V_{CC(5V0)} < V_{(HDMI_5V0_CON)}$	-	-	10	μA	
$I_{O(sc)}$	short-circuit output current	$V_{(HDMI_5V0_CON)} = 0\text{ V}$	-	125	175	mA	
V_{do}	dropout voltage	$4.5\text{ V} < V_{CC(5V0)} < 4.925\text{ V}$; DDC = LOW	[2]				
		$I_O = 10\text{ mA}$	-	70	-	mV	
		$I_O = 55\text{ mA}$	-	-	125	mV	
$V_{O(LDO)}$	LDO output voltage	$I_O \leq 55\text{ mA}$; $4.925\text{ V} < V_{CC(5V0)} < 6.5\text{ V}$; DDC = LOW	[2]	4.8	5.05	5.3	V

[1] ANSI-ESD SP5.5.1-2004, ESD sensitivity testing TLP component level method 50 TDR.

[2] The IP4786CZ32S contains a 5 V voltage regulator function for higher input voltages. Any input voltage of $4.925\text{ V} < V_{CC(5V0)} < 6.50\text{ V}$ provides HDMI-compliant output levels of 4.8 V to 5.3 V on HDMI_5V0_CON.**Table 7. UTILITY_CON** $T_{amb} = -25\text{ }^{\circ}\text{C}$ to $+85\text{ }^{\circ}\text{C}$ unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Supplies: pins $V_{CC(5V0)}$ and $V_{CC(SYS)}$						
r_{dyn}	dynamic resistance	TLP	[1]			
		positive transient	-	1.0	-	Ω
		negative transient	-	1.0	-	Ω
V_{CL}	clamping voltage	100 ns TLP; 50 Ω pulser at 50 ns	-	8.0	-	V
C_i	input capacitance	$V_{CC(5V0)} = 0\text{ V}$; $V_{CC(SYS)} = 0\text{ V}$; $V_{bias} = 2.5\text{ V}$; AC input = $3.5\text{ V}_{(p-p)}$; $f = 100\text{ kHz}$	-	8.0	10	pF
R_{pd}	pull-down resistance		60	100	140	k Ω

[1] ANSI-ESD SP5.5.1-2004, ESD sensitivity testing TLP component level method 50 TDR.

Table 8. Static characteristics

$T_{amb} = -25\text{ °C to }+85\text{ °C unless otherwise specified.}$

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
DDC buffer on connector side [1]						
V_{IH}	HIGH-level input voltage		$0.5 \times V_{(HDMI_5V0_CON)}$	-	6.5	V
V_{IL}	LOW-level input voltage		-0.5	-	$0.3 \times V_{(HDMI_5V0_CON)}$	V
V_{OH}	HIGH-level output voltage		[2] $V_{(HDMI_5V0_CON)} - 0.02$	-	$V_{(HDMI_5V0_CON)} + 0.02$	V
V_{OL}	LOW-level output voltage	internal pull-up and external sink	-	100	200	mV
V_{IK}	input clamping voltage	$I_I = -18\text{ mA}$	-	-	-1.0	V
C_{IO}	input/output capacitance	$V_{CC(5V0)} = 5.0\text{ V};$ $V_{CC(SYS)} = 3.3\text{ V};$ $CEC_STBY = \text{HIGH}$	[2][3] -	8.0	10	pF
R_{pu}	pull-up resistance		1.6	1.8	2.0	k Ω
DDC buffer on system side [1][4]						
V_{IH}	HIGH-level input voltage	$V_{CC(SYS)} = 1.8\text{ V}$	450	-	-	mV
		$V_{CC(SYS)} = 2.5\text{ V}$	620	-	-	mV
		$V_{CC(SYS)} = 3.3\text{ V}$	760	-	-	mV
		$V_{CC(SYS)} = 5.0\text{ V}$	800	-	-	mV
V_{IL}	LOW-level input voltage	$V_{CC(SYS)} = 1.8\text{ V}$	-	-	330	mV
		$V_{CC(SYS)} = 2.5\text{ V}$	-	-	380	mV
		$V_{CC(SYS)} = 3.3\text{ V}$	-	-	400	mV
		$V_{CC(SYS)} = 5.0\text{ V}$	-	-	420	mV
V_{OH}	HIGH-level output voltage		[2] $V_{CC(SYS)} - 0.02$	-	$V_{CC(SYS)} + 0.02$	V
V_{OL}	LOW-level output voltage	$V_{CC(SYS)} = 1.8\text{ V}$	[5] -	490	500	mV
		$V_{CC(SYS)} = 2.5\text{ V}$	[5] -	640	690	mV
		$V_{CC(SYS)} = 3.3\text{ V}$	[5] -	685	790	mV
		$V_{CC(SYS)} = 5.0\text{ V}$	[5] -	720	820	mV
V_{IK}	input clamping voltage	$I_I = -18\text{ mA}$	-	-	-1.0	V
C_{IO}	input/output capacitance	$V_{CC(5V0)} = 0\text{ V};$ $V_{CC(SYS)} = 0\text{ V};$ $V_{bias} = 2.5\text{ V};$ AC input = $3.5\text{ V}_{(p-p)}$; $f = 100\text{ kHz}$	[2] -	6.0	8.0	pF
R_{pu}	pull-up resistance		3.2	3.65	4.1	k Ω

Table 8. Static characteristics ...continued
T_{amb} = -25 °C to +85 °C unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
CEC_CON[1]						
V _{IH}	HIGH-level input voltage		2.0	-	-	V
V _{IL}	LOW-level input voltage		-	-	0.80	V
V _{OH}	HIGH-level output voltage		2.88	3.3	3.63	V
V _{OL}	LOW-level output voltage	I _{OL} = 1.5 mA	-	100	200	mV
C _{IO}	input/output capacitance	V _{CC(SV0)} = 0 V; V _{CC(SYS)} = 0 V; V _{bias} = 1.65 V; AC input = 2.5 V _(p-p) ; f = 100 kHz	[2] -	8.0	10	pF
R _{pu}	pull-up resistance		23.4	26.0	28.6	kΩ
CEC_SYS[1][4]						
V _{IH}	HIGH-level input voltage	V _{CC(SYS)} = 1.8 V	450	-	-	mV
		V _{CC(SYS)} = 2.5 V	620	-	-	mV
		V _{CC(SYS)} = 3.3 V	760	-	-	mV
		V _{CC(SYS)} = 5.0 V	800	-	-	mV
V _{IL}	LOW-level input voltage	V _{CC(SYS)} = 1.8 V	-	-	330	mV
		V _{CC(SYS)} = 2.5 V	-	-	380	mV
		V _{CC(SYS)} = 3.3 V	-	-	400	mV
		V _{CC(SYS)} = 5.0 V	-	-	420	mV
V _{OH}	HIGH-level output voltage	[2] V _{CC(SYS)} - 0.02	-	V _{CC(SYS)} + 0.02	V	
V _{OL}	LOW-level output voltage	V _{CC(SYS)} = 1.8 V	[5] -	490	500	mV
		V _{CC(SYS)} = 2.5 V	[5] -	640	690	mV
		V _{CC(SYS)} = 3.3 V	[5] -	675	770	mV
		V _{CC(SYS)} = 5.0 V	[5] -	710	800	mV
C _{IO}	input/output capacitance	V _{CC(SV0)} = 0 V; V _{CC(SYS)} = 0 V; V _{bias} = 1.65 V; AC input = 2.5 V _(p-p) ; f = 100 kHz	[2] -	6.0	7.0	pF
R _{pu}	pull-up resistance		8.5	10	11.5	kΩ
HOTPLUG_DET_CON[1]						
V _{IH}	HIGH-level input voltage		2.0	-	-	V
V _{IL}	LOW-level input voltage		-	-	0.8	V
R _{pd}	pull-down resistance		60	100	140	kΩ
C _i	input capacitance	V _{CC(SV0)} = 0 V; V _{CC(SYS)} = 0 V; V _{bias} = 2.5 V; AC input = 3.5 V _(p-p) ; f = 100 kHz	[2] -	8.0	10	pF

Table 8. Static characteristics ...continued
 $T_{amb} = -25\text{ }^{\circ}\text{C}$ to $+85\text{ }^{\circ}\text{C}$ unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
HOTPLUG_DET_SYS ^[1]						
V_{OH}	HIGH-level output voltage	$I_{OL} = 1\text{ mA}$	$0.7 \times V_{CC(SYS)}$	-	-	V
V_{OL}	LOW-level output voltage	$I_{OL} = -1\text{ mA}$	-	200	300	mV
R_{pd}	pull-down resistance		60	100	140	k Ω

[1] The device is active if the input voltage at pin CEC_STBY is above the HIGH level.

[2] This parameter is guaranteed by design.

[3] Capacitive load measured at power-on.

[4] No external pull-up resistor attached.

[5] Typical value at $T_{amb} = +25\text{ }^{\circ}\text{C}$.

Table 9. CEC_STBY power management circuit

$V_{CC(SYS)} = 1.62\text{ V}$ to 5.5 V ; $V_{CC(5V0)} = 4.5\text{ V}$ to 6.5 V ; $GND = 0\text{ V}$; $T_{amb} = -25\text{ }^{\circ}\text{C}$ to $+85\text{ }^{\circ}\text{C}$ unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Board side: input pin CEC_STBY ^[1]						
V_{IH}	HIGH-level input voltage	HIGH = active	^[2] 1.2	-	6.5	V
V_{IL}	LOW-level input voltage	LOW = standby	^[3] -0.5	-	0.8	V
R_{pd}	pull-down resistance		60	100	140	k Ω
C_i	input capacitance	$V_i = 3\text{ V}$ or 0 V	-	6	7	pF

[1] The CEC_STBY pin should be connected permanently to $V_{CC(5V0)}$ or $V_{CC(SYS)}$ if no enable control is needed.

[2] DDC buffers, HPD buffer, and HDMI_5V0_CON out enabled; CEC buffer enabled.

[3] DDC buffers, HPD buffer, and HDMI_5V0_CON out disabled; CEC buffer enabled.

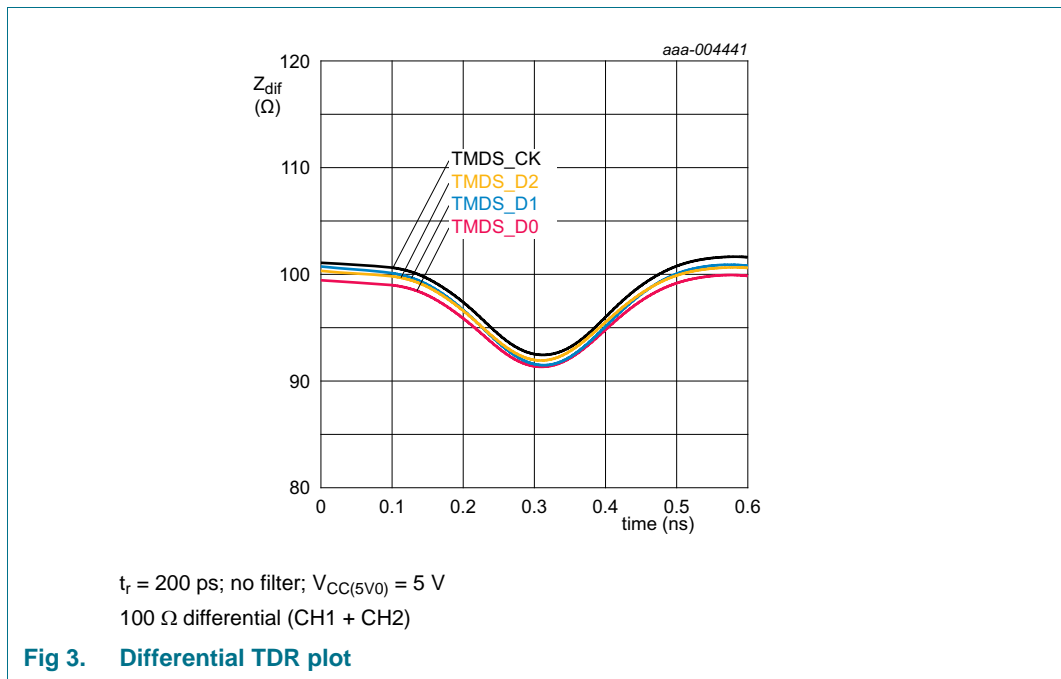
9. Dynamic characteristics

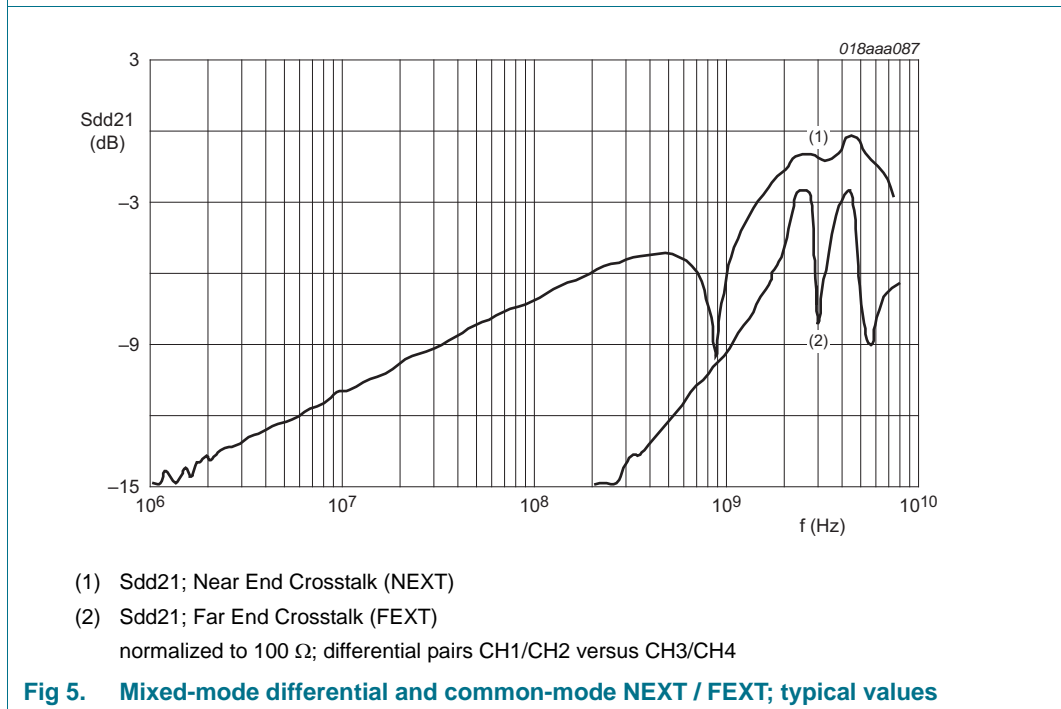
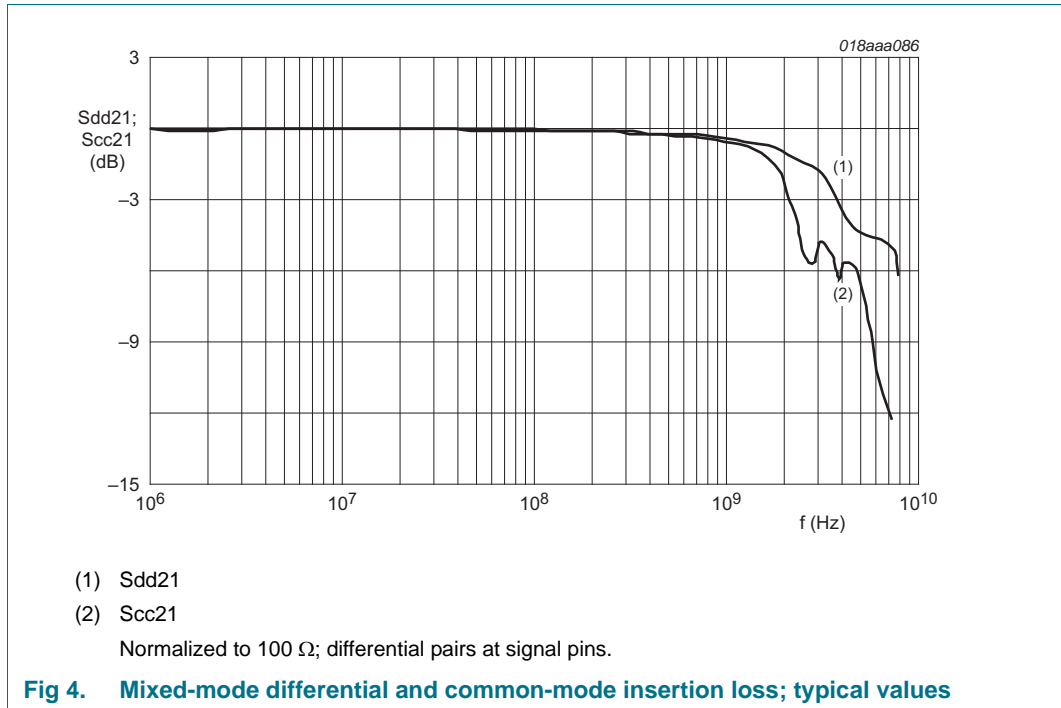
Table 10. Dynamic characteristics

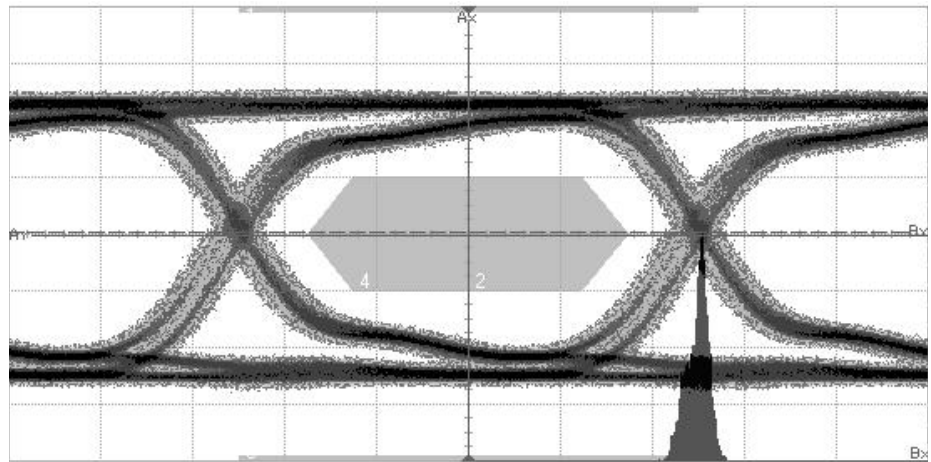
$V_{CC(5V0)} = 5.0\text{ V}$; $V_{CC(SYS)} = 1.8\text{ V}$; $GND = 0\text{ V}$; $T_{amb} = -25\text{ }^{\circ}\text{C}$ to $+85\text{ }^{\circ}\text{C}$ unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
DDC_DAT_SYS, DDC_CLK_SYS, DDC_DAT_CON, DDC_CLK_CON^[1]						
t _{PLH}	LOW to HIGH propagation delay	system side to connector side Figure 15	-	80	-	ns
t _{PHL}	HIGH to LOW propagation delay	system side to connector side Figure 15	-	60	-	ns
t _{PLH}	LOW to HIGH propagation delay	connector side to system side Figure 16	-	120	-	ns
t _{PHL}	HIGH to LOW propagation delay	connector side to system side Figure 16	-	80	-	ns
t _{TLH}	LOW to HIGH transition time	connector side Figure 17	-	150	-	ns
t _{THL}	HIGH to LOW transition time	connector side Figure 17	-	100	-	ns
t _{TLH}	LOW to HIGH transition time	system side Figure 18	-	250	-	ns
t _{THL}	HIGH to LOW transition time	system side Figure 18	-	80	-	ns

[1] All dynamic measurements are done with a 75 pF load. Rise times are determined by internal pull-up resistors.

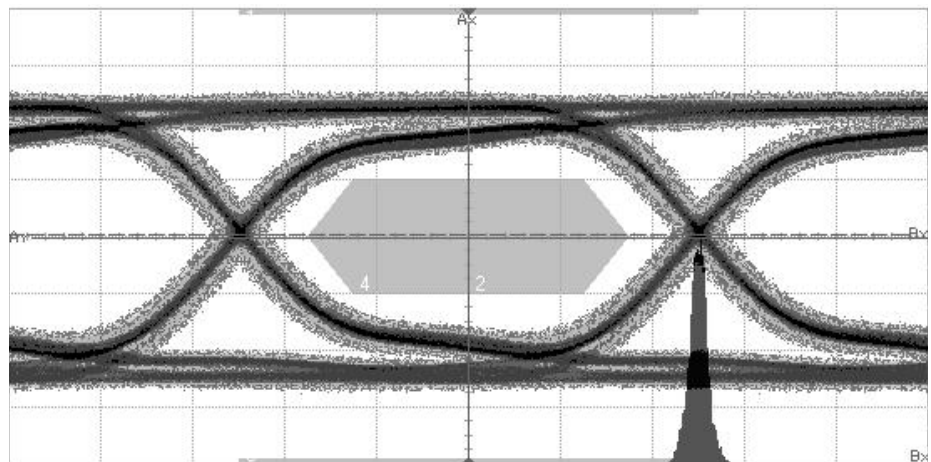






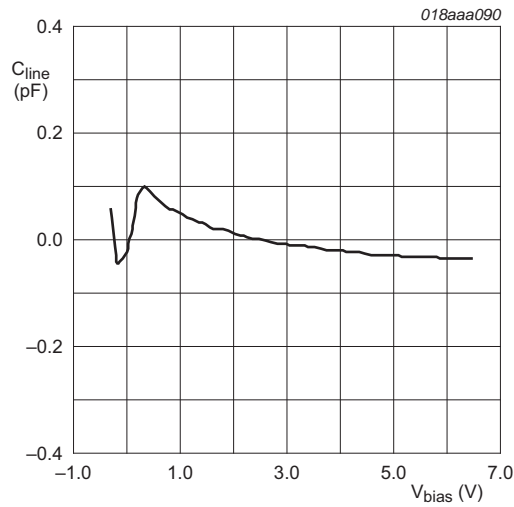
227 MHz pixel clock
 Horizontal scale: 90 ps/div
 Vertical scale: 200 mV/div
 Offset: 42.6 mV

Fig 6. Eye diagram using IP4786CZ32S (1080p, 12 bit)



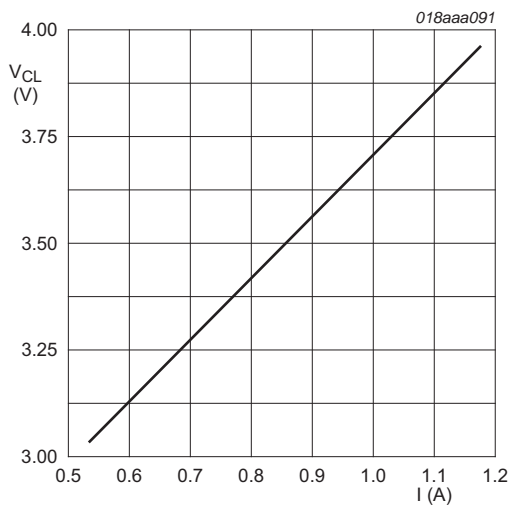
297 MHz pixel clock
 Horizontal scale: 67.5 ps/div
 Vertical scale: 200 mV/div
 Offset: 42.6 mV

Fig 7. Eye diagram using IP4786CZ32S (1080p, 16 bit)



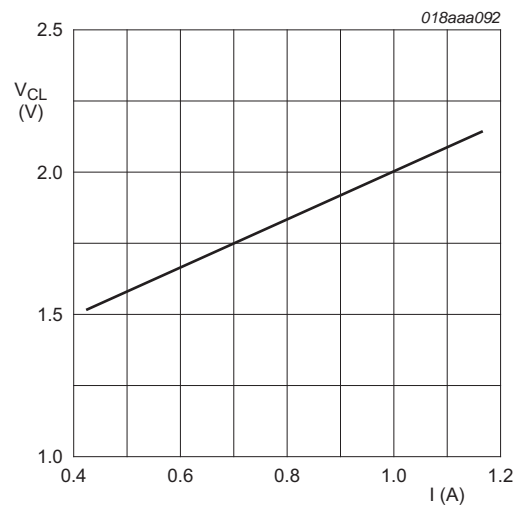
Deviation from typical capacitance normalized at V_{bias} = 2.5 V

Fig 8. Line capacitance as a function of bias voltage; typical values



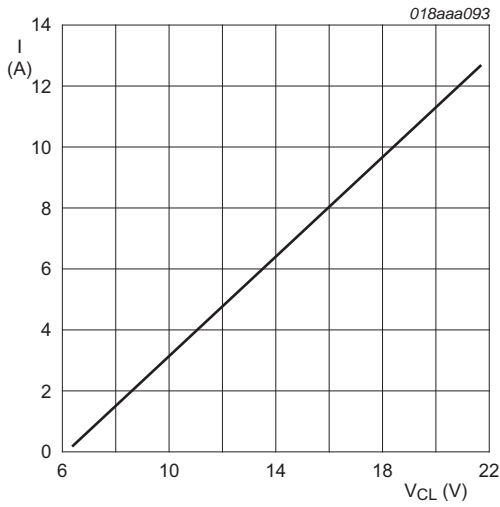
IEC 61000-4-5; t_p = 8/20 μs; positive pulse

Fig 9. Dynamic resistance with positive clamping



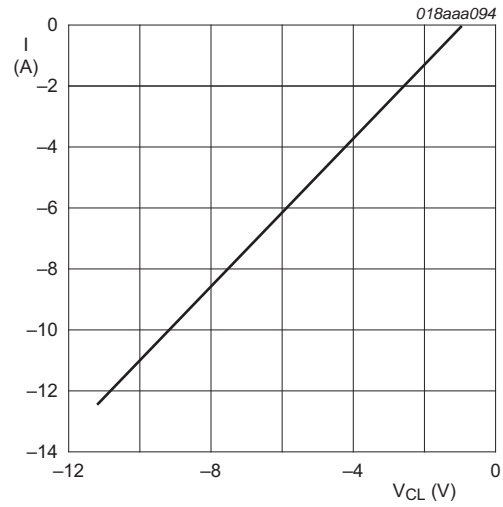
IEC 61000-4-5; t_p = 8/20 μs; negative pulse

Fig 10. Dynamic resistance with negative clamping



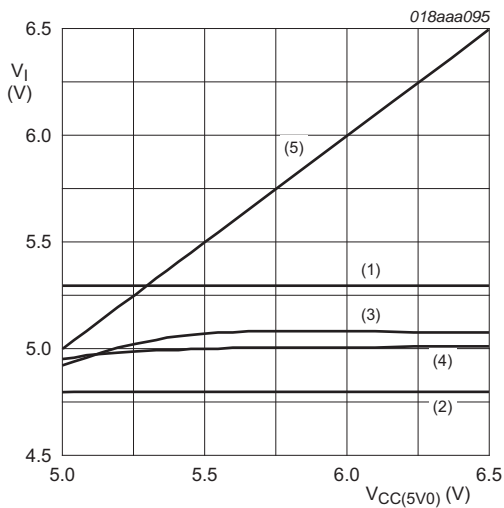
$t_p = 100$ ns; TLP; signal pins; typical values

Fig 11. Dynamic resistance with positive clamping



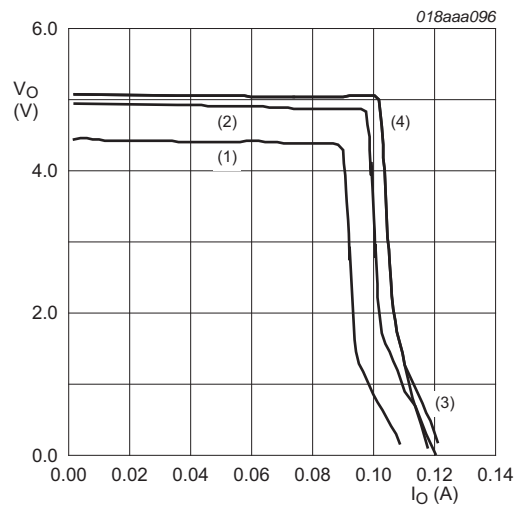
$t_p = 100$ ns; TLP; signal pins; typical values

Fig 12. Dynamic resistance with negative clamping



- (1) 5.3 V; maximum values; HDMI CTS TID 7-11
- (2) 4.8 V; minimum values; HDMI CTS TID 7-11
- (3) $I = 0$ mA
- (4) $I = 55$ mA
- (5) $V_{CC(5V0)}$ supply input; 4.925 V to 6.5 V

Fig 13. Overvoltage limiter function (HDMI_5V0_CON)



- (1) $V_{CC(5V0)} = 4.5$ V
- (2) $V_{CC(5V0)} = 5.0$ V
- (3) $V_{CC(5V0)} = 5.5$ V
- (4) $V_{CC(5V0)} = 6.5$ V

Fig 14. Overcurrent limiter function (HDMI_5V0_CON)

10. AC waveforms

10.1 DDC propagation delay

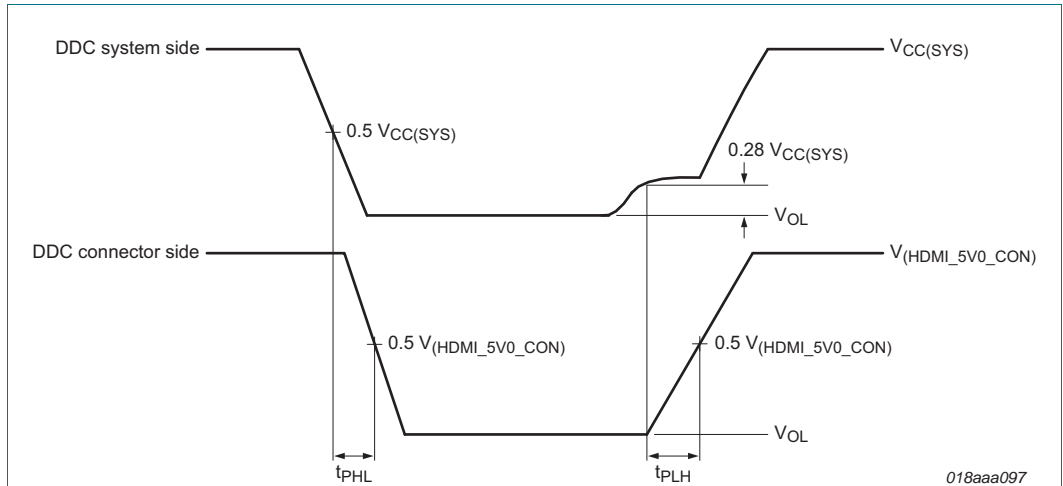


Fig 15. Propagation delay DDC, DDC system side to DDC connector side

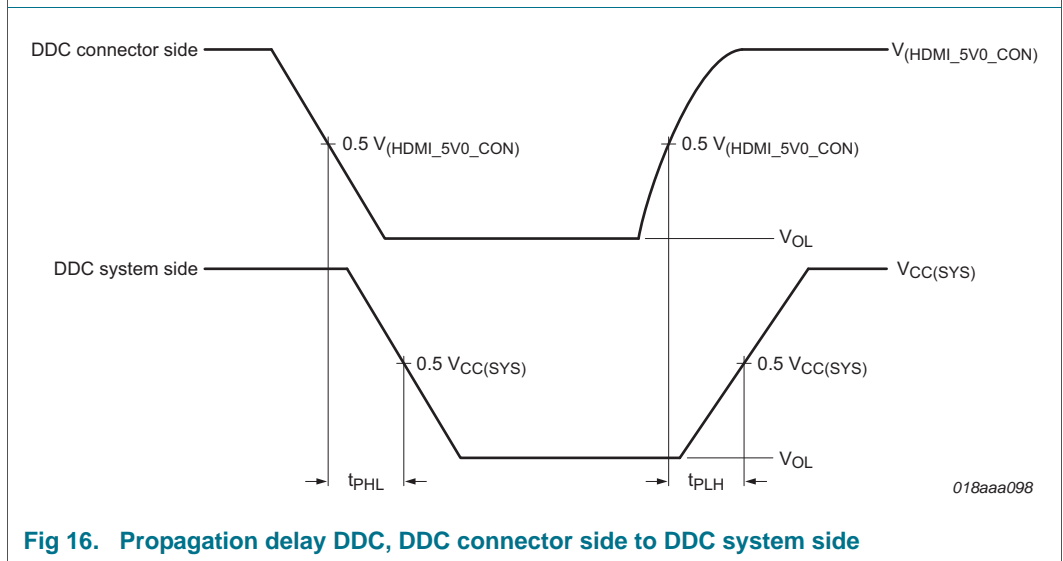


Fig 16. Propagation delay DDC, DDC connector side to DDC system side

10.2 DDC transition time

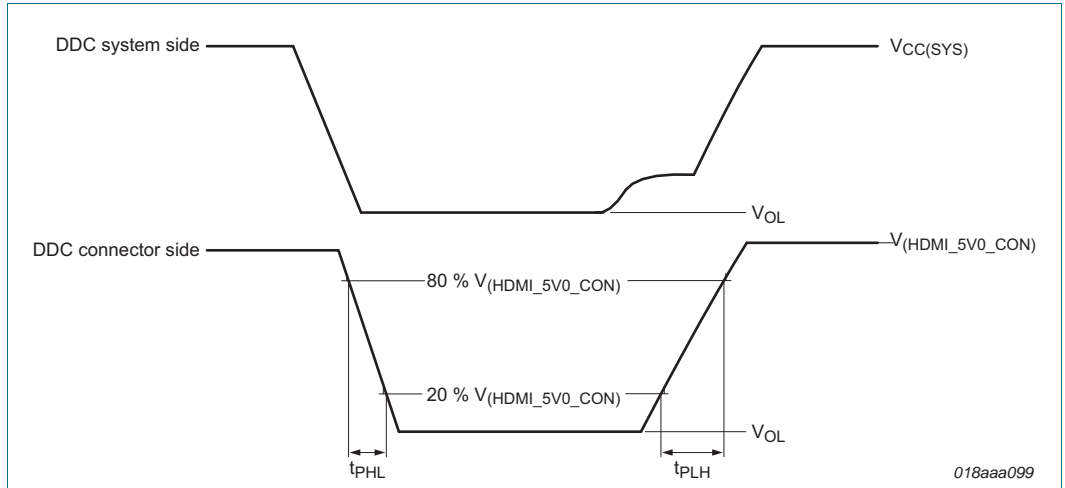


Fig 17. Transition time DDC connector side

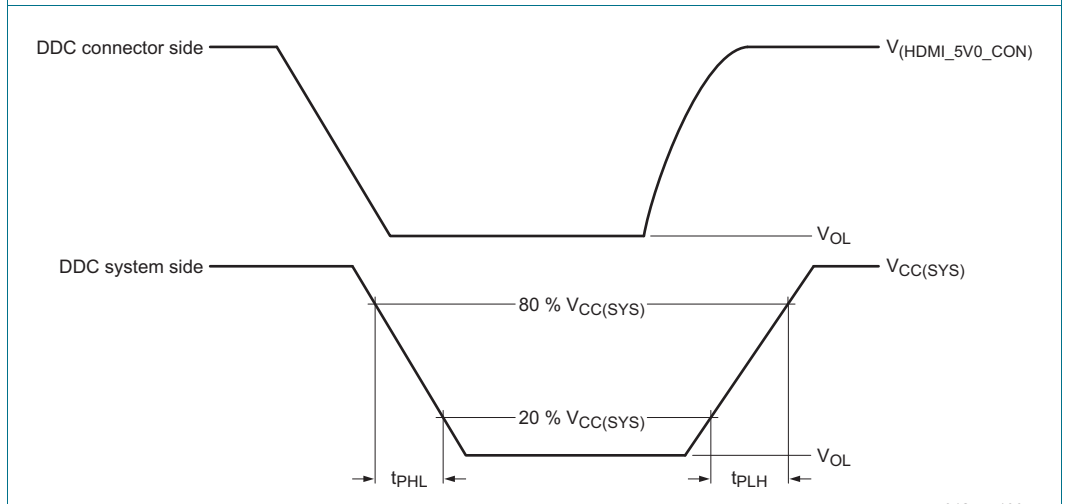


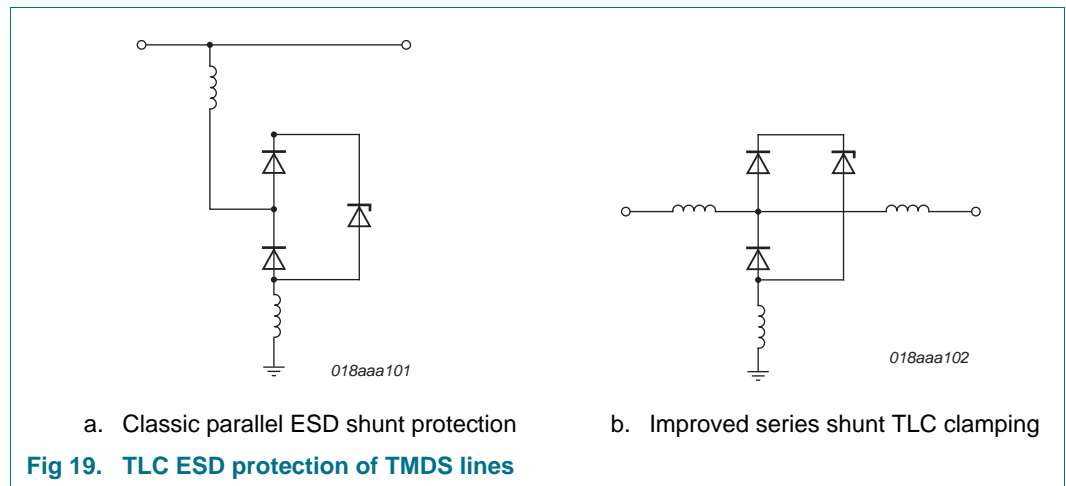
Fig 18. Transition time DDC system side

11. Application information

11.1 TMDS ESD

To protect the TMDS lines and also to comply with the impedance requirements of the HDMI specification, the IP4786CZ32S provides ESD protection with matched TLC ESD structures. Typical Dual Rail Clamp (DRC) or rail-to-rail shunt structures are common for low-capacitance ESD protection (Figure 19; left side) where the dominant factor for the TMDS line impedance dip is determined by the capacitive load to ground. Parasitic lead inductances of the packaging in this case work against the ESD clamping performance by including the $\Delta I/\Delta t$ reactance of the inductance into the path of the ESD shunt.

The IP4786CZ32S utilizes these inherent inductances in series with the transmission line in order to present an effective capacitive load of roughly only 0.7 pF. This TLC structure minimizes the capacitive dip, for ideal signal integrity (Figure 19; right side) without complicated PCB pre-compensation. As a beneficial side effect, this enhances the ESD performance of the device as well, since the reactance of the series inductance attenuates the fast initial peak of the ESD pulse, for a lower residual pulse delivered to the Application Specific Integrated Circuit (ASIC).



11.2 Operating and standby modes

The operating mode of IP4786CZ32S depends on the availability of the $V_{CC(5V0)}$ and $V_{CC(SYS)}$ supply voltages and on the state of the CEC_STBY input signal. Without availability of both supplies, IP4786CZ32S is in Standby mode. As soon as $V_{CC(5V0)}$ and $V_{CC(SYS)}$ are within the range specified in [Section 8](#), the part is in an operating mode that can be controlled via the CEC_STBY input signal. In case CEC_STBY is LOW, only the CEC buffer is active and enabled to receive or send CEC commands. All other outputs are in a high-ohmic state. A HIGH input signal enables all parts of IP4786CZ32S and puts the device into full operating mode.

Table 11. IP4786CZ32S operating modes

$V_{CC(SYS)}$	$V_{CC(5V0)}$	CEC_STBY ^[1]	Mode	Description
< 1.1 V	< 4.5 V	X	Standby mode	all outputs high-ohmic
≥ 1.1 V	≥ 4.5 V	L	CEC Standby mode	CEC circuit active; all other outputs high-ohmic
		H	full operating mode	all functional blocks active

[1] X = Don't care (either LOW or HIGH level); L = LOW-level input; H = HIGH-level input

If no CEC Standby mode is required, or if no special Power-down modes are desired, the CEC_STBY pin can be pulled HIGH to $V_{CC(5V0)}$ or $V_{CC(SYS)}$ for continuous HDMI and CEC operation as soon as the supplies are available.

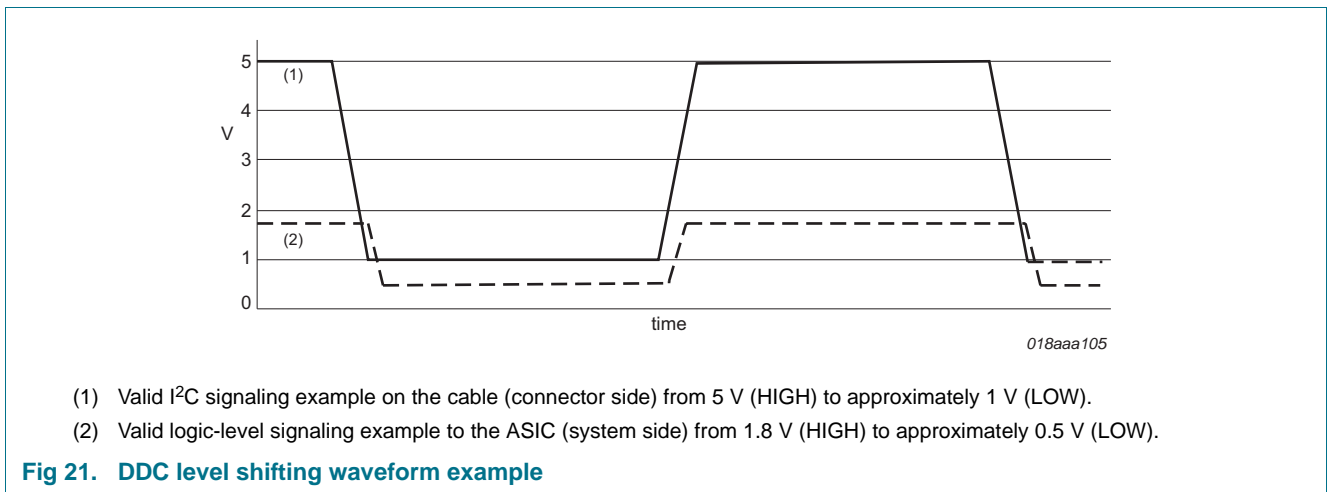
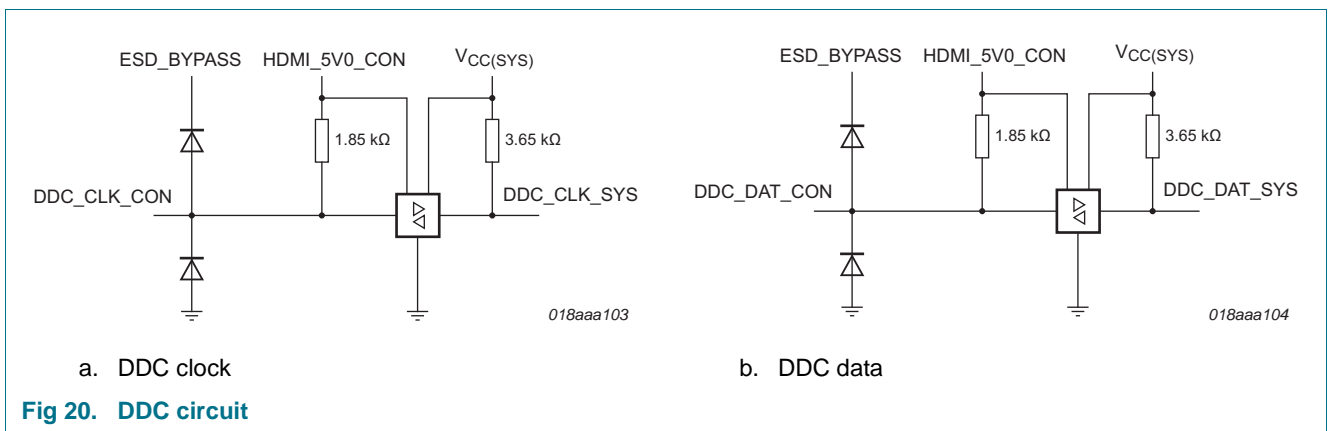
Strapping the CEC_STBY = $V_{CC(SYS)}$ = V_{DD} of the ASIC guarantees that all interface signals ending with the suffix “_SYS” on the system side are disabled when $V_{CC(SYS)}$ goes LOW. This configuration protects the ASIC I/O signals from exceeding its local V_{DD} . In this mode, even if $V_{CC(5V0)}$ is powered, HDMI_5V0_CON goes active and hot plug events can be detected only when the ASIC power supply rail is on.

Strapping CEC_STBY = $V_{CC(5V0)}$ is the most basic configuration where the buffers are enabled whenever the local $V_{CC(5V0)}$ and $V_{CC(SYS)}$ supplies reach minimum operating levels.

11.3 DDC circuit

The DDC bus circuit integrates all required pull-ups, and provides full capacitive decoupling between the HDMI connector and the DDC bus lines on the PCB. The capacitive decoupling ensures that the maximum capacitive load is well within the 50 pF maximum of the HDMI specification. No external pull-ups or pull-downs are required.

The bidirectional buffers support high-capacitive load on the HDMI cable-side. Various non-compliant but prevalent low-cost cables have been observed with a capacitive load of up to 6 nF on the DDC lines, far exceeding the 700 pF HDMI limit. The IP4786CZ32S can easily decouple this from the weaker ASIC I/O buffers, and drive the rogue cable successfully.

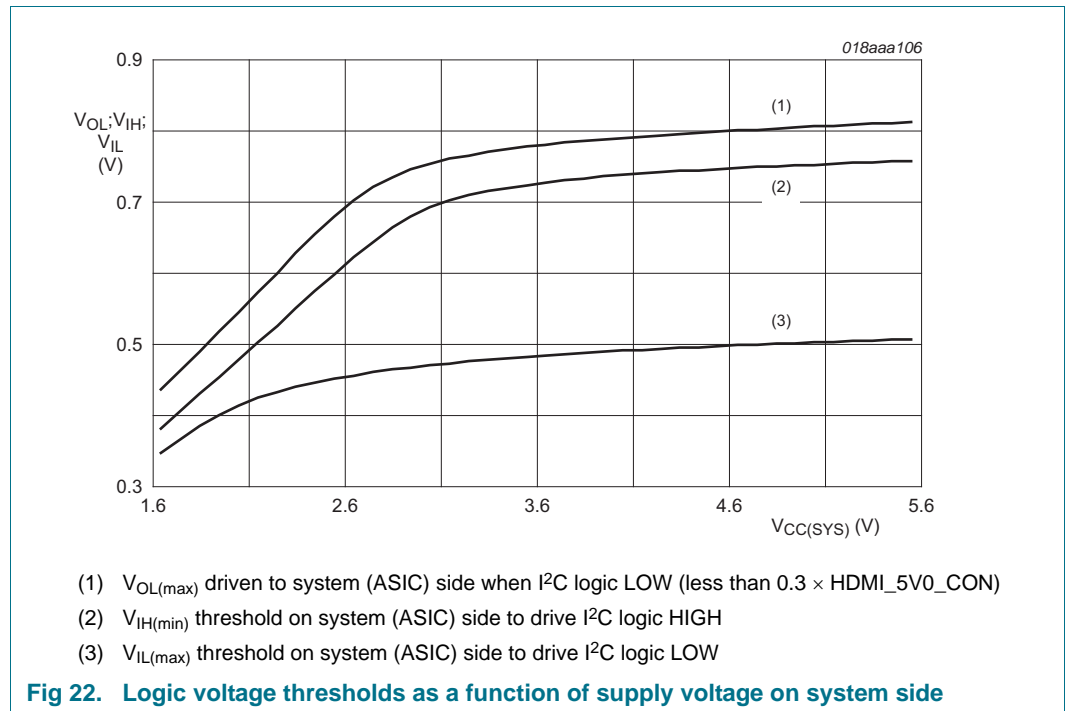


11.4 Logic low I²C voltage shifter

The DDC buffers provide an additional feature commonly required for high-integration HDMI ASICs. In order to be compatible with the 5 V I²C standard used for DDC communication, I/O buffer cells of many HDMI modern transmitter chips require level shifting. As FET-based level shifting just limits the HIGH level of the signal, the LOW level remains unchanged. As a result, the LOW-level voltages on the DDC bus often exceed the 0.3 V_{DD} LOW-level input voltage (V_{IL}) limit of low-voltage I/O buffers.

To enable proper operation that is independent of the system side I/O voltage, the DDC buffers inside IP4786CZ32S shift both the HIGH and the LOW levels by the required amount. This ensures that LOW levels on the system side DDC bus match the LOW-level input voltage requirements down to I/O voltages of 1.8 V.

Besides the DDC buffers, this feature is also included in the CEC buffer, allowing standard I/O buffer cells to be used in HDMI ASICs and microcontrollers.



11.5 Hot plug detect circuit and HEAC support

The IP4786CZ32S includes a hot plug detect circuit that simplifies the hot plug application. The circuit generates a standard logic level from the hot plug signal.

The hot plug detect circuit is pulling down the signal to avoid any floating signal. The comparator guarantees a safe detection of the 2 V hot plug signal without any glitches or oscillation at the hot plug output.

The IP4786CZ32S also provides an additional ESD pin to protect the reserved / HEAC pin along with hot plug detect to 8 kV IEC 61000-4-2, level 4.

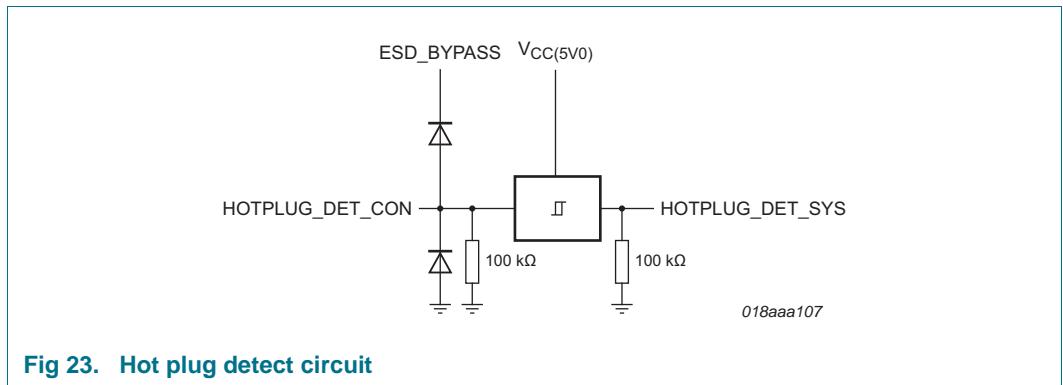


Fig 23. Hot plug detect circuit

11.6 CEC

The logical multidrop topology of the CEC bus can include complex physical stubs, loading cables, and interconnects that may deteriorate signal quality. The IP4786CZ32S includes a full bidirectional buffer to drive the CEC bus and isolate the CEC microcontroller or ASIC General-Purpose Input/Output (GPIO).

The CEC buffer derives power from an on-board 3.3 V regulator from the $V_{CC(5V0)}$ domain (see [Figure 24](#)). This allows extensive system power management configurations and guarantees an HDMI-compliant $V_{(CEC_CON)}$ on the connector, as well as the backdrive-protected 125 μ A nominal CEC pull-up which does not degrade the bus when powered down.

By placing the CEC microcontroller and $V_{CC(5V0)}$ input on a 5 V rail as shown in [Figure 27](#), the CEC microcontroller can communicate over CEC for power commands, and then enable the HDMI port via the CEC_STBY pin, as well as the rest of the system as needed.

The CEC buffer is always active as soon as both supply voltages are present. For details on the operating and Standby modes of IP4786CZ32S, see [Section 11.2](#).

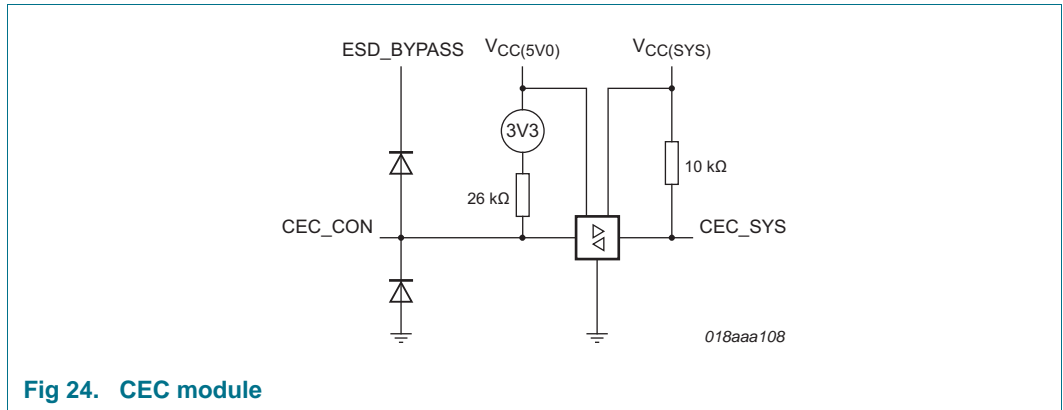


Fig 24. CEC module

11.7 Backdrive protection

The HDMI connector contains various signals which can partly supply current into an HDMI device that is powered down.

Typically, the DDC lines and the CEC signals can force significant current back into the powered-down rails as shown in [Figure 25](#), causing power-on reset problems with the system, and possible damage. The IP4786CZ32S prevents this backdrive condition whenever the I/O voltage is greater than the local supply.

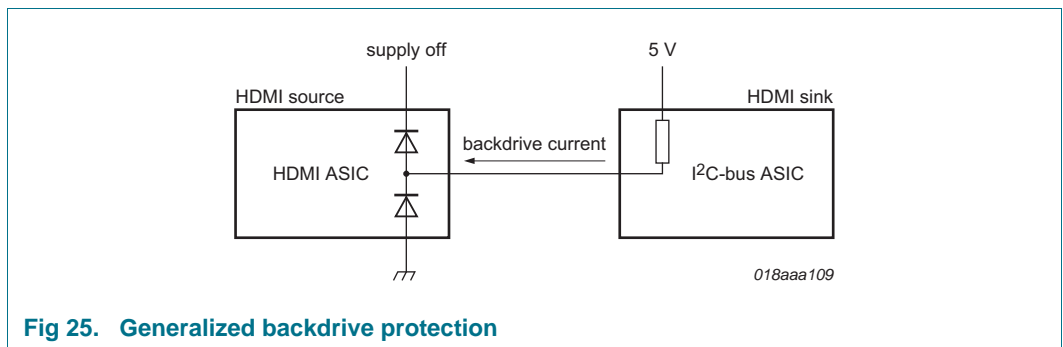


Fig 25. Generalized backdrive protection

11.8 55 mA overcurrent / overvoltage LDO function

To isolate faults from the source power supply while still meeting HDMI output specifications, IP4786CZ32S integrates a complete linear output overcurrent protection.

The Low DropOut (LDO) design provides a low-cost solution requiring just a single output capacitor (1 μ F or higher, Equivalent Series Resistance (ESR) < 1 Ω), eliminating start-up and ripple concerns (see [Figure 26](#)).

A typical 100 mV dropout voltage V_{do} overcurrent-only solution would require a 5.1 V \pm 3 % input supply to guarantee 4.8 V to 5.3 V over 0 mA to 55 mA at the HDMI connector. The overcurrent / overvoltage feature of the IP4786CZ32S allows the use of wider tolerance input supplies up to 6.5 V while still meeting the 4.8 V-to-5.3 V output limit required by HDMI. This means, for example, a cost-reduced 5.2 V \pm 5 % or even a 5.5 V \pm 10 % supply can be used with the IP4786CZ32S.

As with all the I/O pins, this block is ESD-protected and also provides backdrive protection when a rogue HDMI sink powers the HDMI cable unexpectedly.

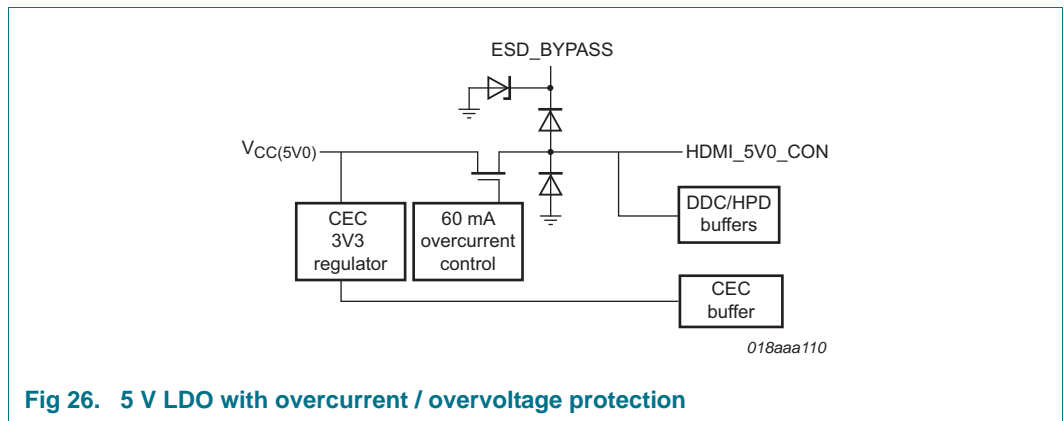


Fig 26. 5 V LDO with overcurrent / overvoltage protection

11.9 Schematic view of application

Only a single external component ($C_O = 1 \mu\text{F}$) is required to protect and interface the ASIC to a complete and compliant HDMI port. The 100 nF ESD bypass capacitor is optional.

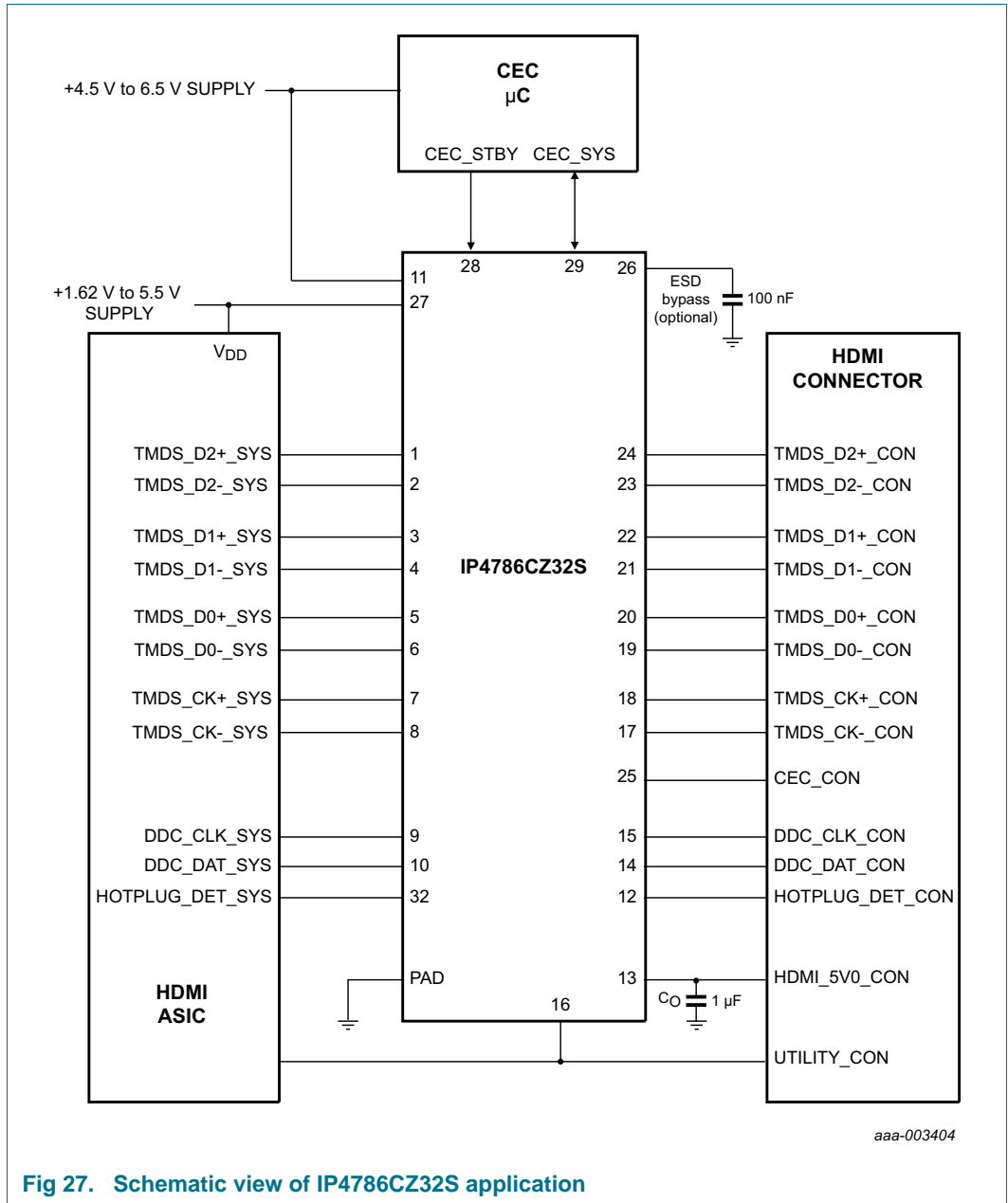


Fig 27. Schematic view of IP4786CZ32S application

11.10 Typical application

The IP4786CZ32S is designed to simplify routing to the HDMI connector, and ease the incorporation of high-level ESD protection into delicately balanced high-speed TMDS lines. These lines rely on tightly controlled microstrip or stripline transmission lines with minimal impedance discontinuities, which can deteriorate return loss, increase deterministic jitter and generally erode overall link signal integrity.

Normally when designing the PCB with standard shunt ESD clamps, careful consideration must be given to manual pre-compensation of the additional load of the added ESD component. With the IP4786CZ32S TLCs, the ESD suppressor is designed to maintain the characteristic impedance of the PCB microstrip or stripline, and therefore the designer needs only be concerned with the standard-controlled impedance of the unloaded PCB lines. This simplifies the task of the PCB designer, and minimizes the tuning cycles, which are sometimes required when pre-compensation misses the mark. A basic application diagram for the ESD protection of an HDMI interface is shown in [Figure 28](#) for a type-C HDMI connector.

The optimized HXQFN32 pinning simplifies the PCB design to keep the ESD protection close to the connector where it can minimize the coupling of the ESD pulse onto other lines in the system during a strike.

Due to the integrated pull-up and pull-down resistors, only two external capacitors are required to implement a fully compliant HDMI port.

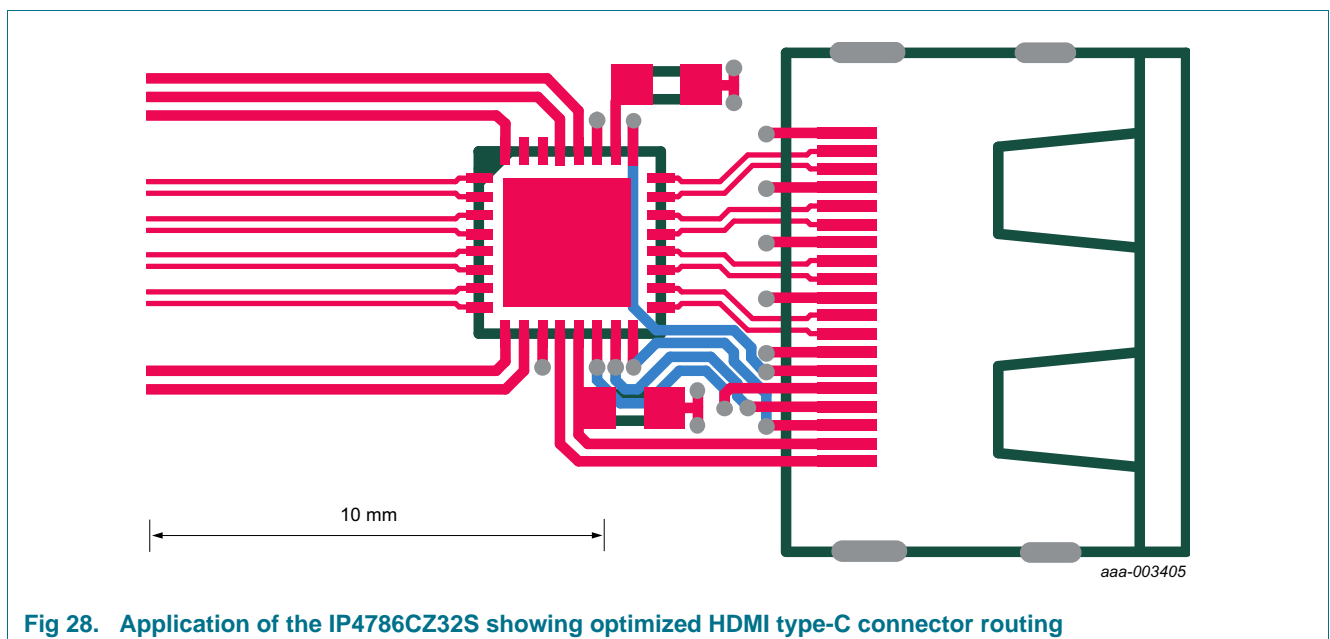


Fig 28. Application of the IP4786CZ32S showing optimized HDMI type-C connector routing

12. Package outline

HXQFN32: plastic thermal enhanced extremely thin quad flat package; no leads;
32 terminals; body 4 x 4 x 0.5 mm

SOT1318-1

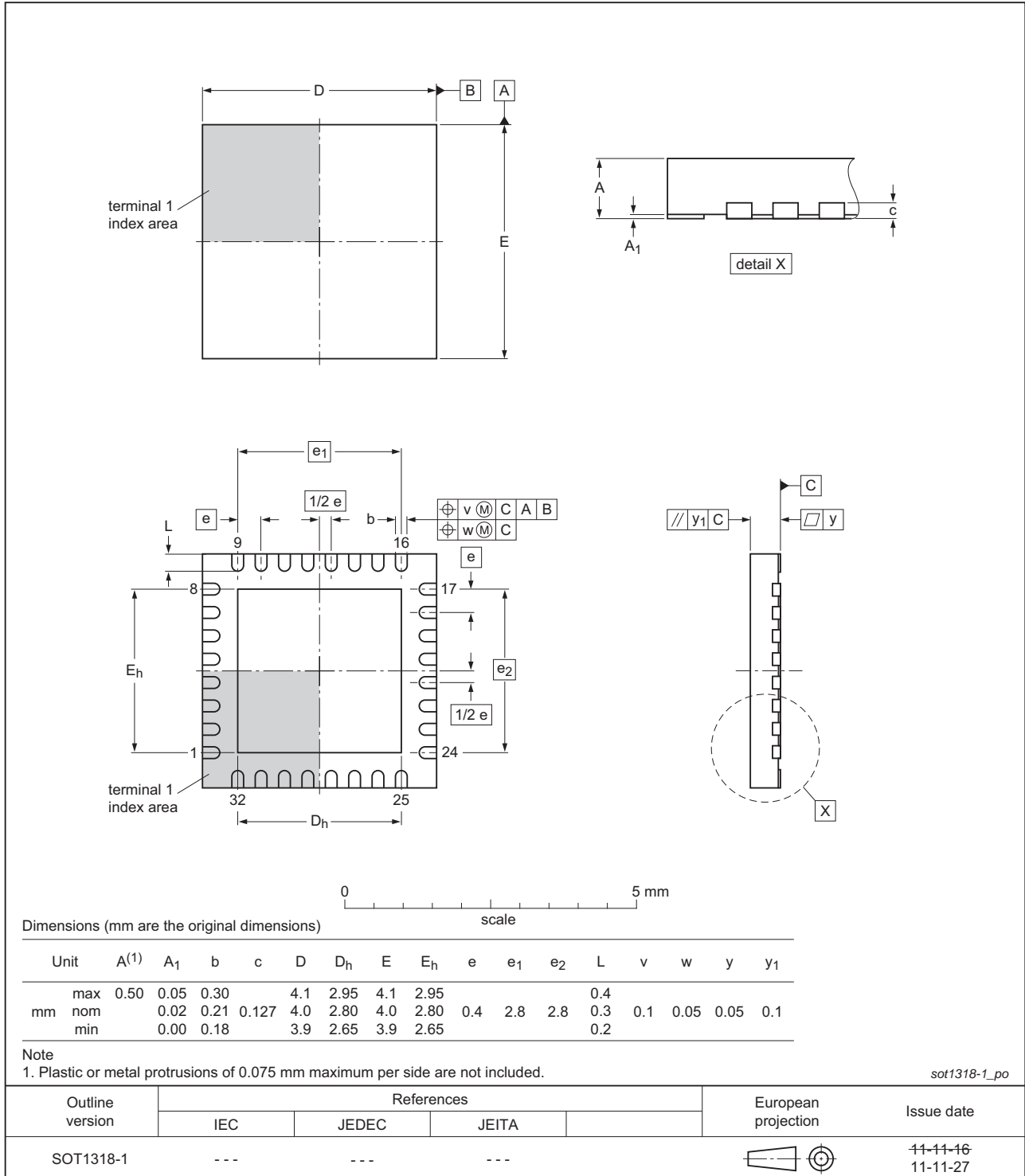


Fig 29. Package outline SOT1318-1 (HXQFN32)

13. Soldering of SMD packages

This text provides a very brief insight into a complex technology. A more in-depth account of soldering ICs can be found in Application Note *AN10365 "Surface mount reflow soldering description"*.

13.1 Introduction to soldering

Soldering is one of the most common methods through which packages are attached to Printed Circuit Boards (PCBs), to form electrical circuits. The soldered joint provides both the mechanical and the electrical connection. There is no single soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and Surface Mount Devices (SMDs) are mixed on one printed wiring board; however, it is not suitable for fine pitch SMDs. Reflow soldering is ideal for the small pitches and high densities that come with increased miniaturization.

13.2 Wave and reflow soldering

Wave soldering is a joining technology in which the joints are made by solder coming from a standing wave of liquid solder. The wave soldering process is suitable for the following:

- Through-hole components
- Leaded or leadless SMDs, which are glued to the surface of the printed circuit board

Not all SMDs can be wave soldered. Packages with solder balls, and some leadless packages which have solder lands underneath the body, cannot be wave soldered. Also, leaded SMDs with leads having a pitch smaller than ~0.6 mm cannot be wave soldered, due to an increased probability of bridging.

The reflow soldering process involves applying solder paste to a board, followed by component placement and exposure to a temperature profile. Leaded packages, packages with solder balls, and leadless packages are all reflow solderable.

Key characteristics in both wave and reflow soldering are:

- Board specifications, including the board finish, solder masks and vias
- Package footprints, including solder thieves and orientation
- The moisture sensitivity level of the packages
- Package placement
- Inspection and repair
- Lead-free soldering versus SnPb soldering

13.3 Wave soldering

Key characteristics in wave soldering are:

- Process issues, such as application of adhesive and flux, clinching of leads, board transport, the solder wave parameters, and the time during which components are exposed to the wave
- Solder bath specifications, including temperature and impurities

13.4 Reflow soldering

Key characteristics in reflow soldering are:

- Lead-free versus SnPb soldering; note that a lead-free reflow process usually leads to higher minimum peak temperatures (see [Figure 30](#)) than a SnPb process, thus reducing the process window
- Solder paste printing issues including smearing, release, and adjusting the process window for a mix of large and small components on one board
- Reflow temperature profile; this profile includes preheat, reflow (in which the board is heated to the peak temperature) and cooling down. It is imperative that the peak temperature is high enough for the solder to make reliable solder joints (a solder paste characteristic). In addition, the peak temperature must be low enough that the packages and/or boards are not damaged. The peak temperature of the package depends on package thickness and volume and is classified in accordance with [Table 12](#) and [13](#)

Table 12. SnPb eutectic process (from J-STD-020D)

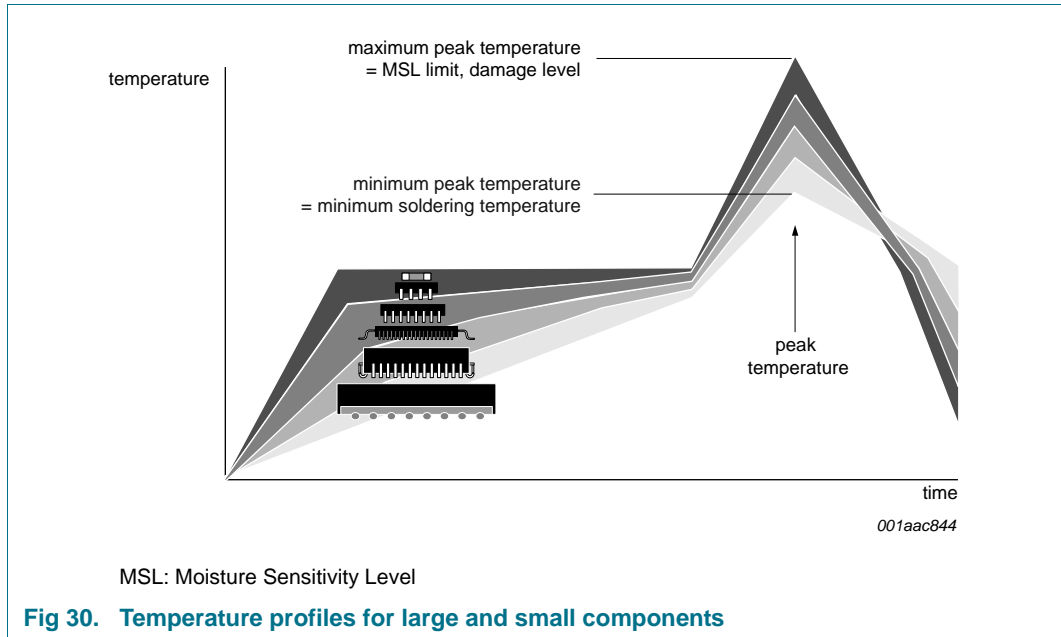
Package thickness (mm)	Package reflow temperature (°C)	
	Volume (mm ³)	
	< 350	≥ 350
< 2.5	235	220
≥ 2.5	220	220

Table 13. Lead-free process (from J-STD-020D)

Package thickness (mm)	Package reflow temperature (°C)		
	Volume (mm ³)		
	< 350	350 to 2000	> 2000
< 1.6	260	260	260
1.6 to 2.5	260	250	245
> 2.5	250	245	245

Moisture sensitivity precautions, as indicated on the packing, must be respected at all times.

Studies have shown that small packages reach higher temperatures during reflow soldering, see [Figure 30](#).



For further information on temperature profiles, refer to Application Note AN10365 “Surface mount reflow soldering description”.

14. Glossary

HDMI sink — Device which receives HDMI signals for example, a TV set.

HDMI source — Device which transmits HDMI signal for example, DVD player.

15. Revision history

Table 14. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
IP4786CZ32S v.2	20130711	Product data sheet	-	IP4786CZ32S v.1
Modifications:		<ul style="list-style-type: none">• Section 2 "Features and benefits": updated• Section 3 "Applications": updated• Figure 6 and Figure 7: corrected• Section 11.2 "Operating and standby modes": added• Section 11.4 "Logic low I²C voltage shifter": updated• Section 11.6 "CEC": updated		
IP4786CZ32S v.1	20120727	Preliminary data sheet	-	-

16. Legal information

16.1 Data sheet status

Document status ^{[1][2]}	Product status ^[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL <http://www.nxp.com>.

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For sales office addresses, please send an email to: salesaddresses@nxp.com

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