# LM555 Timer

**Check for Samples: LM555**

## FEATURES

- **Direct Replacement for SE555/NE555**
- **Timing from Microseconds through Hours**
- **Operates in Both Astable and Monostable Modes**
- **Adjustable Duty Cycle**
- **Output Can Source or Sink 200 mA**
- **Output and Supply TTL Compatible**
- **Temperature Stability Better than 0.005% per °C**
- **Normally On and Normally Off Output**
- **Available in 8-pin VSSOP Package**

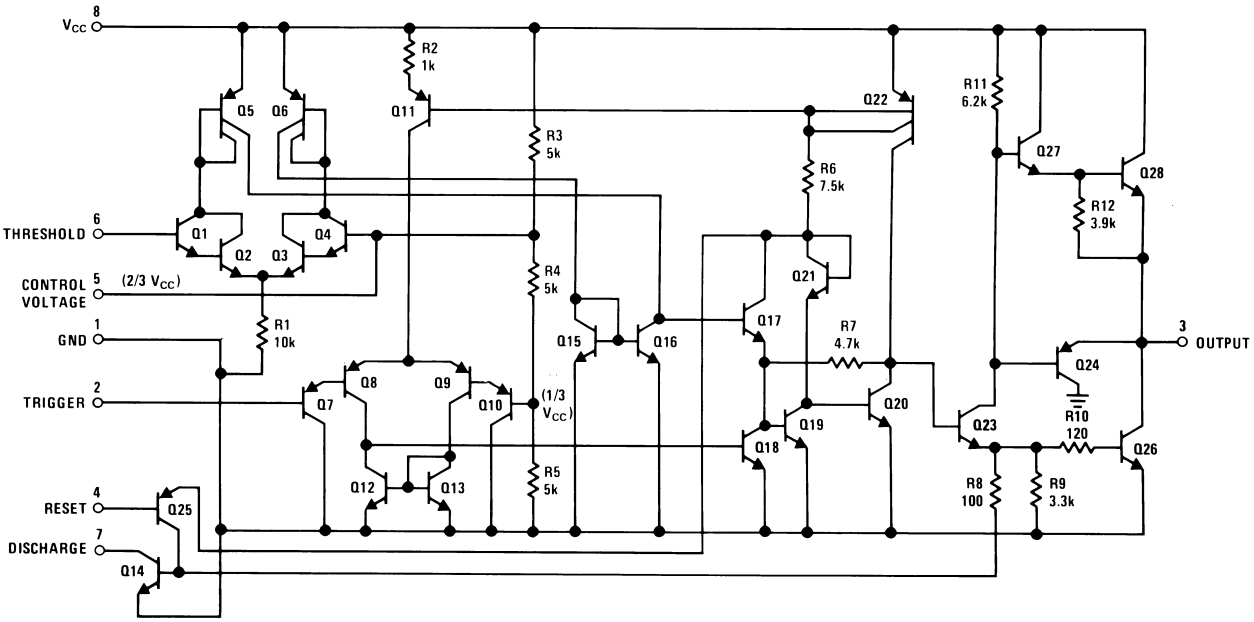
## APPLICATIONS

- **Precision Timing**
- **Pulse Generation**
- **Sequential Timing**
- **Time Delay Generation**
- **Pulse Width Modulation**
- **Pulse Position Modulation**
- **Linear Ramp Generator**

## DESCRIPTION

The LM555 is a highly stable device for generating accurate time delays or oscillation. Additional terminals are provided for triggering or resetting if desired. In the time delay mode of operation, the time is precisely controlled by one external resistor and capacitor. For astable operation as an oscillator, the free running frequency and duty cycle are accurately controlled with two external resistors and one capacitor. The circuit may be triggered and reset on falling waveforms, and the output circuit can source or sink up to 200mA or drive TTL circuits.

### Schematic Diagram

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## Connection Diagram

**Top View**

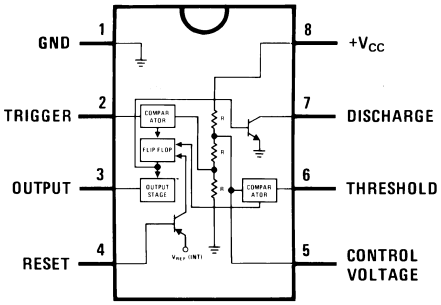



**Figure 1. PDIP, SOIC, and VSSOP Packages**

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

## Absolute Maximum Ratings(1)(2)

| | |
|---|---|
| Supply Voltage | +18V |
| Power Dissipation (3) | |
| LM555CM, LM555CN(4) | 1180 mW |
| LM555CMM | 613 mW |
| Operating Temperature Ranges | |
| LM555C | 0°C to +70°C |
| Storage Temperature Range | −65°C to +150°C |
| Soldering Information | |
| PDIP Package | |
| Soldering (10 Seconds) | 260°C |
| Small Outline Packages (SOIC and VSSOP) | |
| Vapor Phase (60 Seconds) | 215°C |
| Infrared (15 Seconds) | 220°C |

(1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is functional, but do not ensure specific performance limits. Electrical Characteristics state DC and AC electrical specifications under particular test conditions which ensures specific performance limits. This assumes that the device is within the Operating Ratings. Specifications are not ensured for parameters where no limit is given, however, the typical value is a good indication of device performance.
(2) If Military/Aerospace specified devices are required, please contact the TI Sales Office/Distributors for availability and specifications.
(3) For operating at elevated temperatures the device must be derated above 25°C based on a +150°C maximum junction temperature and a thermal resistance of 106°C/W (PDIP), 170°C/W (S0IC-8), and 204°C/W (VSSOP) junction to ambient.
(4) Refer to RETS555X drawing of military LM555H and LM555J versions for specifications.

## Electrical Characteristics (1) (2)

($T_A$ = 25°C, $V_{CC}$ = +5V to +15V, unless otherwise specified)

| Parameter | Test Conditions | Limits | | | Units |
|---|---|---|---|---|---|
| | | LM555C | | | |
| | | Min | Typ | Max | |
| Supply Voltage | | 4.5 | | 16 | V |
| Supply Current | $V_{CC}$ = 5V, $R_L$ = ∞ | | 3 | 6 | mA |
| | $V_{CC}$ = 15V, $R_L$ = ∞ (Low State) (3) | | 10 | 15 | |
| Timing Error, Monostable | | | | | |
| Initial Accuracy | | | 1 | | % |
| Drift with Temperature | $R_A$ = 1k to 100kΩ, C = 0.1µF, (4) | | 50 | | ppm/°C |
| Accuracy over Temperature | | | 1.5 | | % |
| Drift with Supply | | | 0.1 | | %/V |
| Timing Error, Astable | | | | | |
| Initial Accuracy | | | 2.25 | | % |
| Drift with Temperature | $R_A$, $R_B$ = 1k to 100kΩ, C = 0.1µF, (4) | | 150 | | ppm/°C |
| Accuracy over Temperature | | | 3.0 | | % |
| Drift with Supply | | | 0.30 | | %/V |
| Threshold Voltage | | | 0.667 | | x $V_{CC}$ |
| Trigger Voltage | $V_{CC}$ = 15V | | 5 | | V |
| | $V_{CC}$ = 5V | | 1.67 | | V |
| Trigger Current | | | 0.5 | 0.9 | µA |
| Reset Voltage | | 0.4 | 0.5 | 1 | V |
| Reset Current | | | 0.1 | 0.4 | mA |
| Threshold Current | (5) | | 0.1 | 0.25 | µA |
| Control Voltage Level | $V_{CC}$ = 15V | 9 | 10 | 11 | V |
| | $V_{CC}$ = 5V | 2.6 | 3.33 | 4 | |
| Pin 7 Leakage Output High | | | 1 | 100 | nA |
| Pin 7 Sat (6) | | | | | |
| Output Low | $V_{CC}$ = 15V, $I_7$ = 15mA | | 180 | | mV |
| Output Low | $V_{CC}$ = 4.5V, $I_7$ = 4.5mA | | 80 | 200 | mV |
| Output Voltage Drop (Low) | $V_{CC}$ = 15V | | | | |
| | $I_{SINK}$ = 10mA | | 0.1 | 0.25 | V |
| | $I_{SINK}$ = 50mA | | 0.4 | 0.75 | V |
| | $I_{SINK}$ = 100mA | | 2 | 2.5 | V |
| | $I_{SINK}$ = 200mA | | 2.5 | | V |
| | $V_{CC}$ = 5V | | | | |
| | $I_{SINK}$ = 8mA | | | | V |
| | $I_{SINK}$ = 5mA | | 0.25 | 0.35 | V |

(1) All voltages are measured with respect to the ground pin, unless otherwise specified.
(2) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is functional, but do not ensure specific performance limits. Electrical Characteristics state DC and AC electrical specifications under particular test conditions which ensures specific performance limits. This assumes that the device is within the Operating Ratings. Specifications are not ensured for parameters where no limit is given, however, the typical value is a good indication of device performance.
(3) Supply current when output high typically 1 mA less at $V_{CC}$ = 5V.
(4) Tested at $V_{CC}$ = 5V and $V_{CC}$ = 15V.
(5) This will determine the maximum value of $R_A$ + $R_B$ for 15V operation. The maximum total ($R_A$ + $R_B$) is 20MΩ.
(6) No protection against excessive pin 7 current is necessary providing the package dissipation rating will not be exceeded.

## Electrical Characteristics [1] [2] (continued)

($T_A$ = 25°C, $V_{CC}$ = +5V to +15V, unless otherwise specified)

| Parameter | Test Conditions | Limits | | | Units |
|---|---|---|---|---|---|
| | | LM555C | | | |
| | | Min | Typ | Max | |
| Output Voltage Drop (High) | $I_{SOURCE}$ = 200mA, $V_{CC}$ = 15V | | 12.5 | | V |
| | $I_{SOURCE}$ = 100mA, $V_{CC}$ = 15V | 12.75 | 13.3 | | V |
| | $V_{CC}$ = 5V | 2.75 | 3.3 | | V |
| Rise Time of Output | | | 100 | | ns |
| Fall Time of Output | | | 100 | | ns |

## Typical Performance Characteristics

**Minimum Pulse Width Required for Triggering**

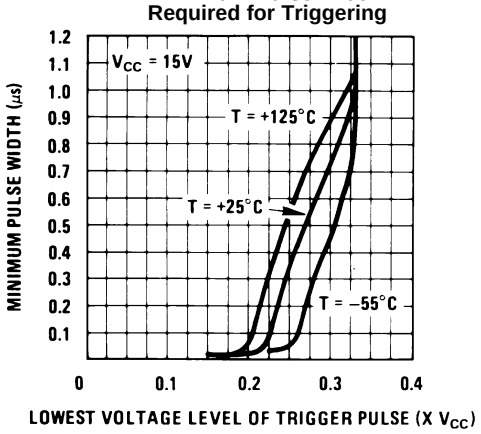



Figure 2.

**Supply Current vs. Supply Voltage**

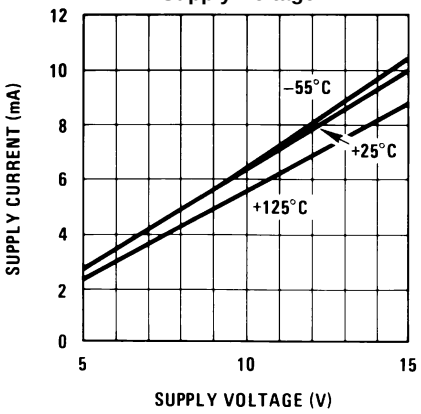



Figure 3.

**High Output Voltage vs. Output Source Current**

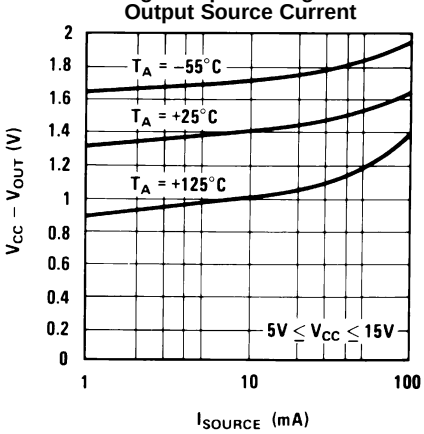



Figure 4.

**Low Output Voltage vs. Output Sink Current**

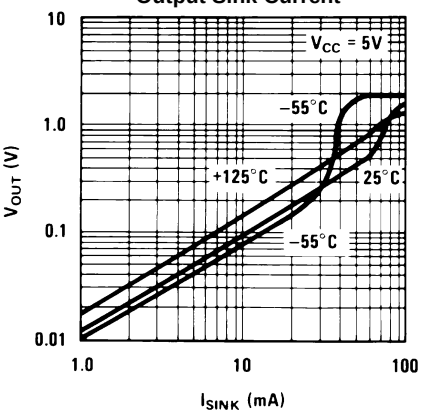



Figure 5.

**Low Output Voltage vs. Output Sink Current**

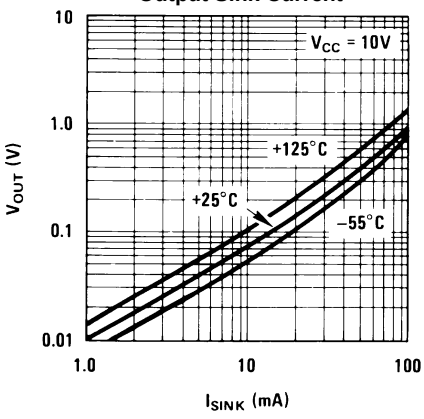



Figure 6.

**Low Output Voltage vs. Output Sink Current**

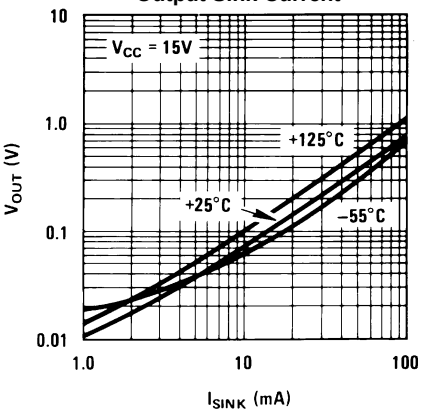



Figure 7.

## Typical Performance Characteristics (continued)

**Output Propagation Delay vs. Voltage Level of Trigger Pulse**

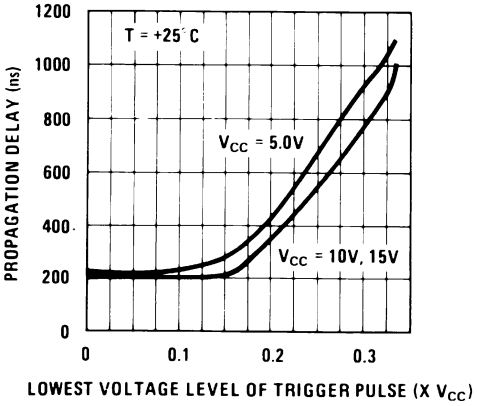



**Figure 8.**

**Output Propagation Delay vs. Voltage Level of Trigger Pulse**

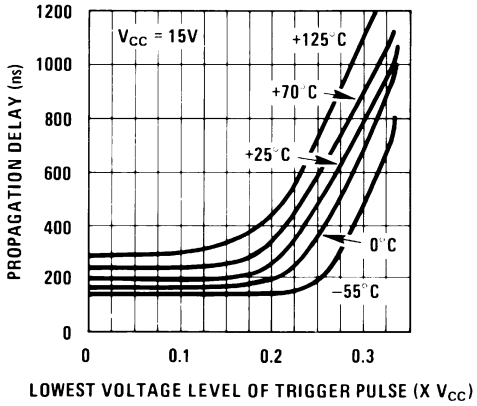



**Figure 9.**

**Discharge Transistor (Pin 7) Voltage vs. Sink Current**

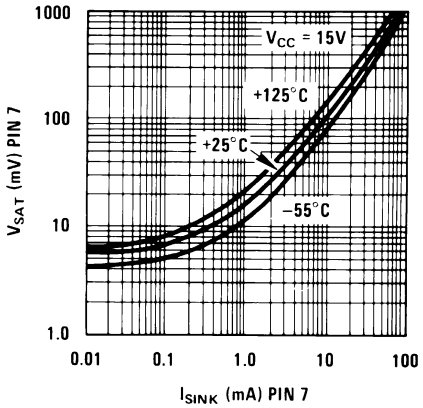



**Figure 10.**

**Discharge Transistor (Pin 7) Voltage vs. Sink Current**

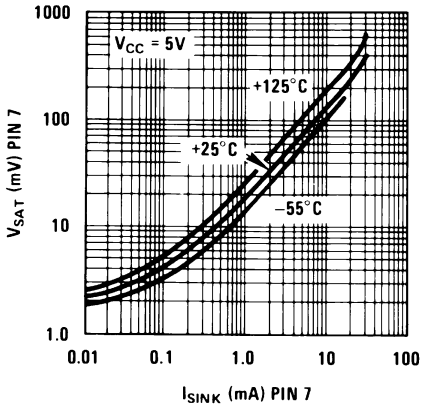



**Figure 11.**

## APPLICATIONS INFORMATION

### MONOSTABLE OPERATION

In this mode of operation, the timer functions as a one-shot (Figure 12). The external capacitor is initially held discharged by a transistor inside the timer. Upon application of a negative trigger pulse of less than 1/3 $V_{CC}$ to pin 2, the flip-flop is set which both releases the short circuit across the capacitor and drives the output high.

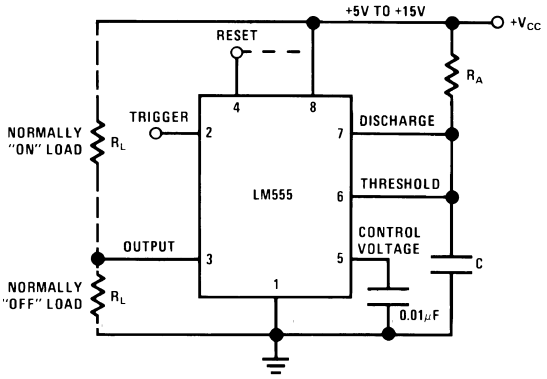
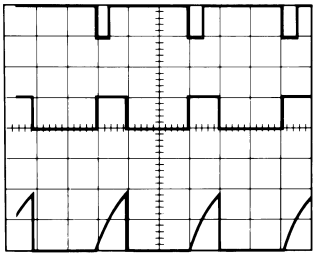



**Figure 12. Monostable**

The voltage across the capacitor then increases exponentially for a period of t = 1.1 $R_A$ C, at the end of which time the voltage equals 2/3 $V_{CC}$. The comparator then resets the flip-flop which in turn discharges the capacitor and drives the output to its low state. Figure 13 shows the waveforms generated in this mode of operation. Since the charge and the threshold level of the comparator are both directly proportional to supply voltage, the timing interval is independent of supply.



$V_{CC}$ = 5V
TIME = 0.1 ms/DIV.
$R_A$ = 9.1kΩ
C = 0.01μF

Top Trace: Input 5V/Div.
Middle Trace: Output 5V/Div.
Bottom Trace: Capacitor Voltage 2V/Div.

**Figure 13. Monostable Waveforms**

During the timing cycle when the output is high, the further application of a trigger pulse will not effect the circuit so long as the trigger input is returned high at least 10μs before the end of the timing interval. However the circuit can be reset during this time by the application of a negative pulse to the reset terminal (pin 4). The output will then remain in the low state until a trigger pulse is again applied.

When the reset function is not in use, it is recommended that it be connected to $V_{CC}$ to avoid any possibility of false triggering.

Figure 14 is a nomograph for easy determination of R, C values for various time delays.

**NOTE**

In monostable operation, the trigger should be driven high before the end of timing cycle.

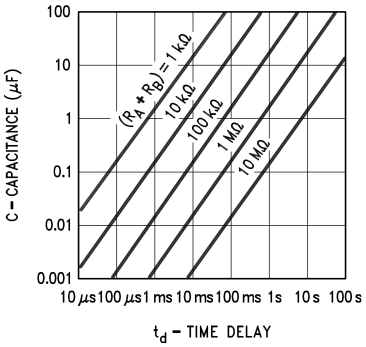



**Figure 14. Time Delay**

## ASTABLE OPERATION

If the circuit is connected as shown in Figure 15 (pins 2 and 6 connected) it will trigger itself and free run as a multivibrator. The external capacitor charges through $R_A$ + $R_B$ and discharges through $R_B$. Thus the duty cycle may be precisely set by the ratio of these two resistors.

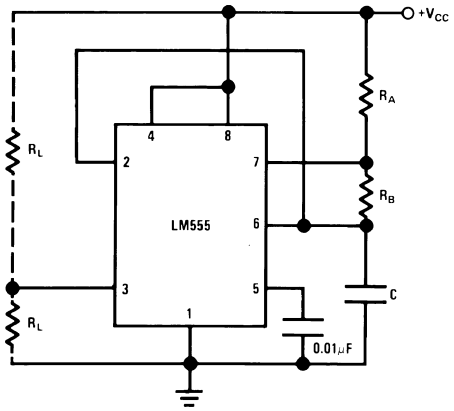
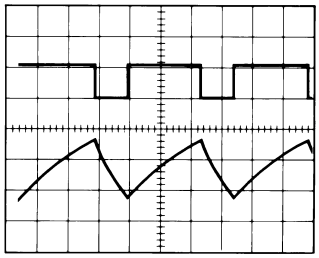



**Figure 15. Astable**

In this mode of operation, the capacitor charges and discharges between 1/3 $V_{CC}$ and 2/3 $V_{CC}$. As in the triggered mode, the charge and discharge times, and therefore the frequency are independent of the supply voltage.

Figure 16 shows the waveforms generated in this mode of operation.



$V_{CC}$ = 5V Top Trace: Output 5V/Div.
TIME = 20μs/DIV. Bottom Trace: Capacitor Voltage 1V/Div.
$R_A$ = 3.9kΩ
$R_B$ = 3kΩ
C = 0.01μF

**Figure 16. Astable Waveforms**

The charge time (output high) is given by:

$$t_1 = 0.693\ (R_A + R_B)\ C \quad (1)$$

And the discharge time (output low) by:

$$t_2 = 0.693\ (R_B)\ C \quad (2)$$

Thus the total period is:

$$T = t_1 + t_2 = 0.693\ (R_A + 2R_B)\ C \quad (3)$$

The frequency of oscillation is:

$$f = \frac{1}{T} = \frac{1.44}{(R_A + 2\,R_B)\,C} \quad (4)$$

Figure 17 may be used for quick determination of these RC values.

The duty cycle is:

$$D = \frac{R_B}{R_A + 2R_B} \quad (5)$$

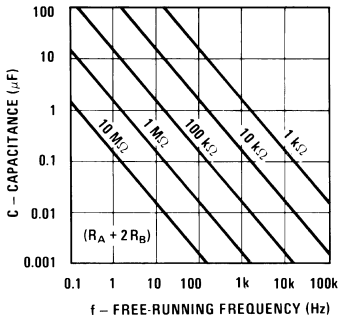
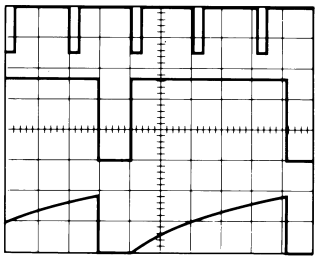



**Figure 17. Free Running Frequency**

## FREQUENCY DIVIDER

The monostable circuit of Figure 12 can be used as a frequency divider by adjusting the length of the timing cycle. Figure 18 shows the waveforms generated in a divide by three circuit.



$V_{CC}$ = 5V
TIME = 20μs/DIV.
$R_A$ = 9.1kΩ
C = 0.01μF

Top Trace: Input 4V/Div.
Middle Trace: Output 2V/Div.
Bottom Trace: Capacitor 2V/Div.

**Figure 18. Frequency Divider**

## PULSE WIDTH MODULATOR

When the timer is connected in the monostable mode and triggered with a continuous pulse train, the output pulse width can be modulated by a signal applied to pin 5. Figure 19 shows the circuit, and in Figure 20 are some waveform examples.

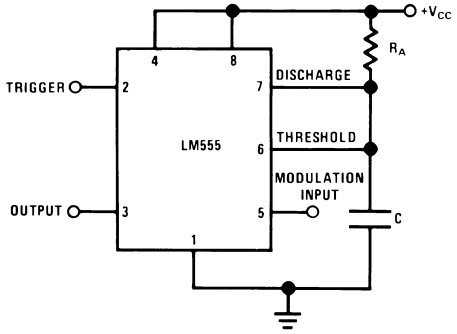
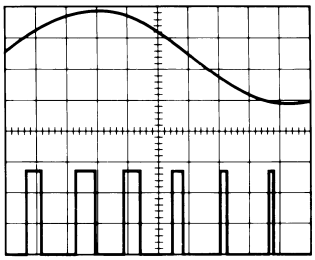



**Figure 19. Pulse Width Modulator**



$V_{CC}$ = 5V Top Trace: Modulation 1V/Div.
TIME = 0.2 ms/DIV. Bottom Trace: Output Voltage 2V/Div.
$R_A$ = 9.1kΩ
C = 0.01µF

**Figure 20. Pulse Width Modulator**

## PULSE POSITION MODULATOR

This application uses the timer connected for astable operation, as in Figure 21, with a modulating signal again applied to the control voltage terminal. The pulse position varies with the modulating signal, since the threshold voltage and hence the time delay is varied. Figure 22 shows the waveforms generated for a triangle wave modulation signal.

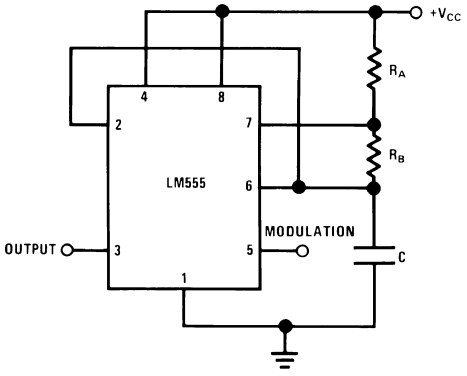
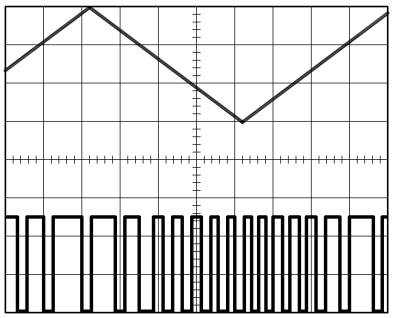



**Figure 21. Pulse Position Modulator**



$V_{CC}$ = 5V
TIME = 0.1 ms/DIV.
$R_A$ = 3.9kΩ
$R_B$ = 3kΩ
C = 0.01µF

Top Trace: Modulation Input 1V/Div.
Bottom Trace: Output 2V/Div.

**Figure 22. Pulse Position Modulator**

## LINEAR RAMP

When the pullup resistor, $R_A$, in the monostable circuit is replaced by a constant current source, a linear ramp is generated. Figure 23 shows a circuit configuration that will perform this function.

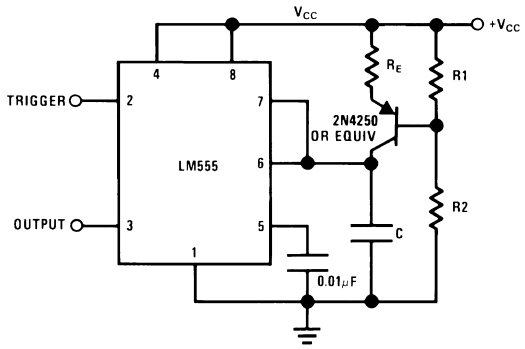


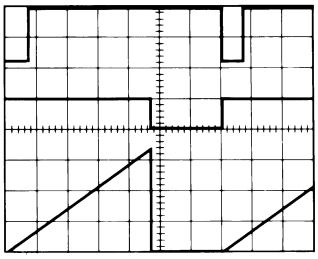

**Figure 23.**

Figure 24 shows waveforms generated by the linear ramp.

The time interval is given by:

$$T = \frac{2/3\ V_{CC}\ R_E\ (R_1 + R_2)\ C}{R_1\ V_{CC} - V_{BE}\ (R_1 + R_2)} \qquad V_{BE} \cong 0.6V \tag{6}$$

$$V_{BE} \simeq 0.6V \tag{7}$$



$V_{CC}$ = 5V Top Trace: Input 3V/Div.
TIME = 20µs/DIV. Middle Trace: Output 5V/Div.
$R_1$ = 47kΩ Bottom Trace: Capacitor Voltage 1V/Div.
$R_2$ = 100kΩ
$R_E$ = 2.7 kΩ
C = 0.01 µF

**Figure 24. Linear Ramp**

## 50% DUTY CYCLE OSCILLATOR

For a 50% duty cycle, the resistors $R_A$ and $R_B$ may be connected as in Figure 25. The time period for the output high is the same as previous, $t_1 = 0.693\ R_A\ C$. For the output low it is $t_2$ =

$$\left[(R_A R_B)/(R_A + R_B)\right] C\ \ell n\left[\frac{R_B - 2R_A}{2R_B - R_A}\right] \quad (8)$$

Thus the frequency of oscillation is:

$$f = \frac{1}{t_1 + t_2} \quad (9)$$

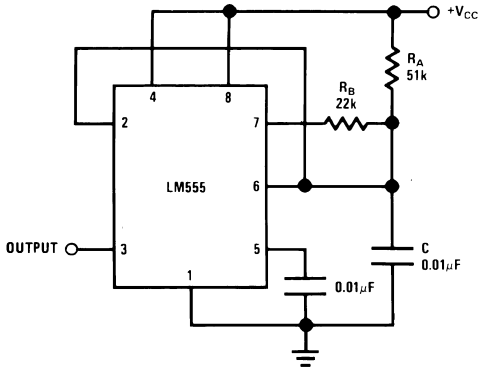



**Figure 25. 50% Duty Cycle Oscillator**

Note that this circuit will not oscillate if $R_B$ is greater than 1/2 $R_A$ because the junction of $R_A$ and $R_B$ cannot bring pin 2 down to 1/3 $V_{CC}$ and trigger the lower comparator.

## ADDITIONAL INFORMATION

Adequate power supply bypassing is necessary to protect associated circuitry. Minimum recommended is 0.1µF in parallel with 1µF electrolytic.

Lower comparator storage time can be as long as 10µs when pin 2 is driven fully to ground for triggering. This limits the monostable pulse width to 10µs minimum.

Delay time reset to output is 0.47µs typical. Minimum reset pulse width must be 0.3µs, typical.

Pin 7 current switches within 30ns of the output (pin 3) voltage.

## REVISION HISTORY

**Changes from Revision B (March 2013) to Revision C** **Page**

- Changed layout of National Data Sheet to TI format ..... 12

## PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead/Ball Finish (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|---|---|---|---|---|---|---|---|---|---|---|---|
| LM555CM | ACTIVE | SOIC | D | 8 | 95 | TBD | Call TI | Call TI | 0 to 70 | LM 555CM | Samples |
| LM555CM/NOPB | ACTIVE | SOIC | D | 8 | 95 | Green (RoHS & no Sb/Br) | SN \| CU SN | Level-1-260C-UNLIM | 0 to 70 | LM 555CM | Samples |
| LM555CMM | ACTIVE | VSSOP | DGK | 8 | 1000 | TBD | Call TI | Call TI | 0 to 70 | Z55 | Samples |
| LM555CMM/NOPB | ACTIVE | VSSOP | DGK | 8 | 1000 | Green (RoHS & no Sb/Br) | CU SN | Level-1-260C-UNLIM | 0 to 70 | Z55 | Samples |
| LM555CMMX/NOPB | ACTIVE | VSSOP | DGK | 8 | 3500 | Green (RoHS & no Sb/Br) | CU SN | Level-1-260C-UNLIM | 0 to 70 | Z55 | Samples |
| LM555CMX | ACTIVE | SOIC | D | 8 | 2500 | TBD | Call TI | Call TI | 0 to 70 | LM 555CM | Samples |
| LM555CMX/NOPB | ACTIVE | SOIC | D | 8 | 2500 | Green (RoHS & no Sb/Br) | SN \| CU SN | Level-1-260C-UNLIM | 0 to 70 | LM 555CM | Samples |
| LM555CN | ACTIVE | PDIP | P | 8 | 40 | TBD | Call TI | Call TI | 0 to 70 | LM 555CN | Samples |
| LM555CN/NOPB | ACTIVE | PDIP | P | 8 | 40 | Green (RoHS & no Sb/Br) | CU SN | Level-1-NA-UNLIM | 0 to 70 | LM 555CN | Samples |
| MC1455P1 | NRND | PDIP | P | 8 | 40 | TBD | Call TI | Call TI | 0 to 70 | LM 555CN | |
| NE555V | NRND | PDIP | P | 8 | 40 | TBD | Call TI | Call TI | 0 to 70 | LM 555CN | |

(1) The marketing status values are defined as follows:
**ACTIVE:** Product device recommended for new designs.
**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.
**OBSOLETE:** TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
**TBD:** The Pb-Free/Green conversion plan has not been defined.
**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

**(3)** MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

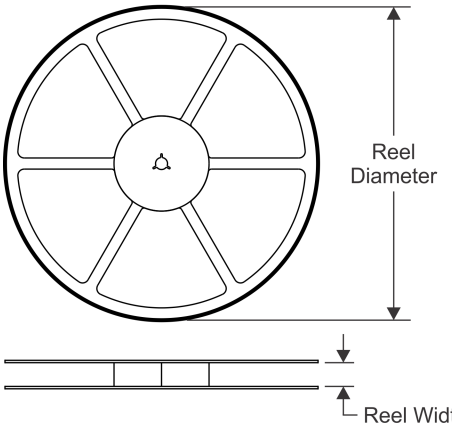
**(4)** There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

**(5)** Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

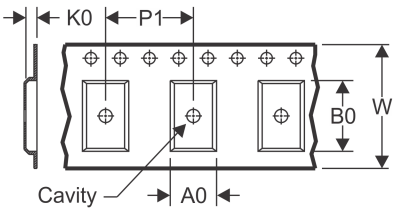
**(6)** Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

## TAPE AND REEL INFORMATION

**REEL DIMENSIONS**

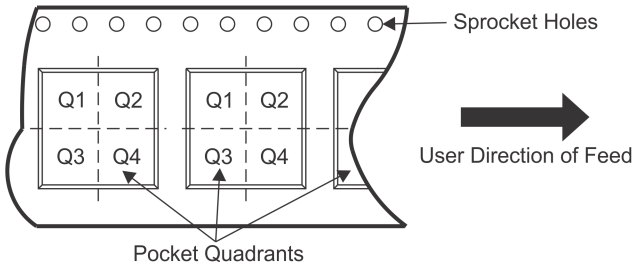



**TAPE DIMENSIONS**




| | |
|---|---|
| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

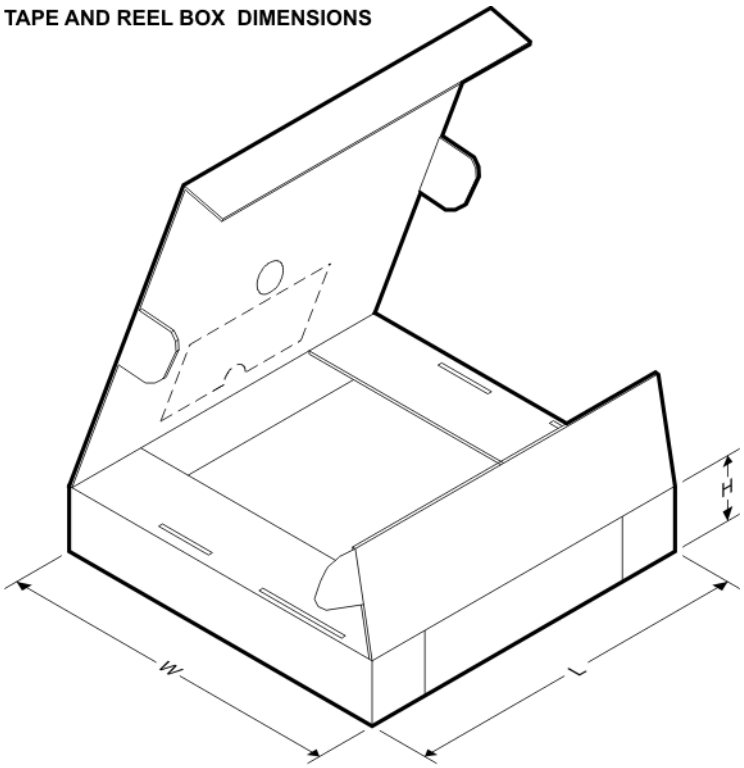
**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| LM555CMM | VSSOP | DGK | 8 | 1000 | 178.0 | 12.4 | 5.3 | 3.4 | 1.4 | 8.0 | 12.0 | Q1 |
| LM555CMM/NOPB | VSSOP | DGK | 8 | 1000 | 178.0 | 12.4 | 5.3 | 3.4 | 1.4 | 8.0 | 12.0 | Q1 |
| LM555CMMX/NOPB | VSSOP | DGK | 8 | 3500 | 330.0 | 12.4 | 5.3 | 3.4 | 1.4 | 8.0 | 12.0 | Q1 |
| LM555CMX | SOIC | D | 8 | 2500 | 330.0 | 12.4 | 6.5 | 5.4 | 2.0 | 8.0 | 12.0 | Q1 |
| LM555CMX/NOPB | SOIC | D | 8 | 2500 | 330.0 | 12.4 | 6.5 | 5.4 | 2.0 | 8.0 | 12.0 | Q1 |

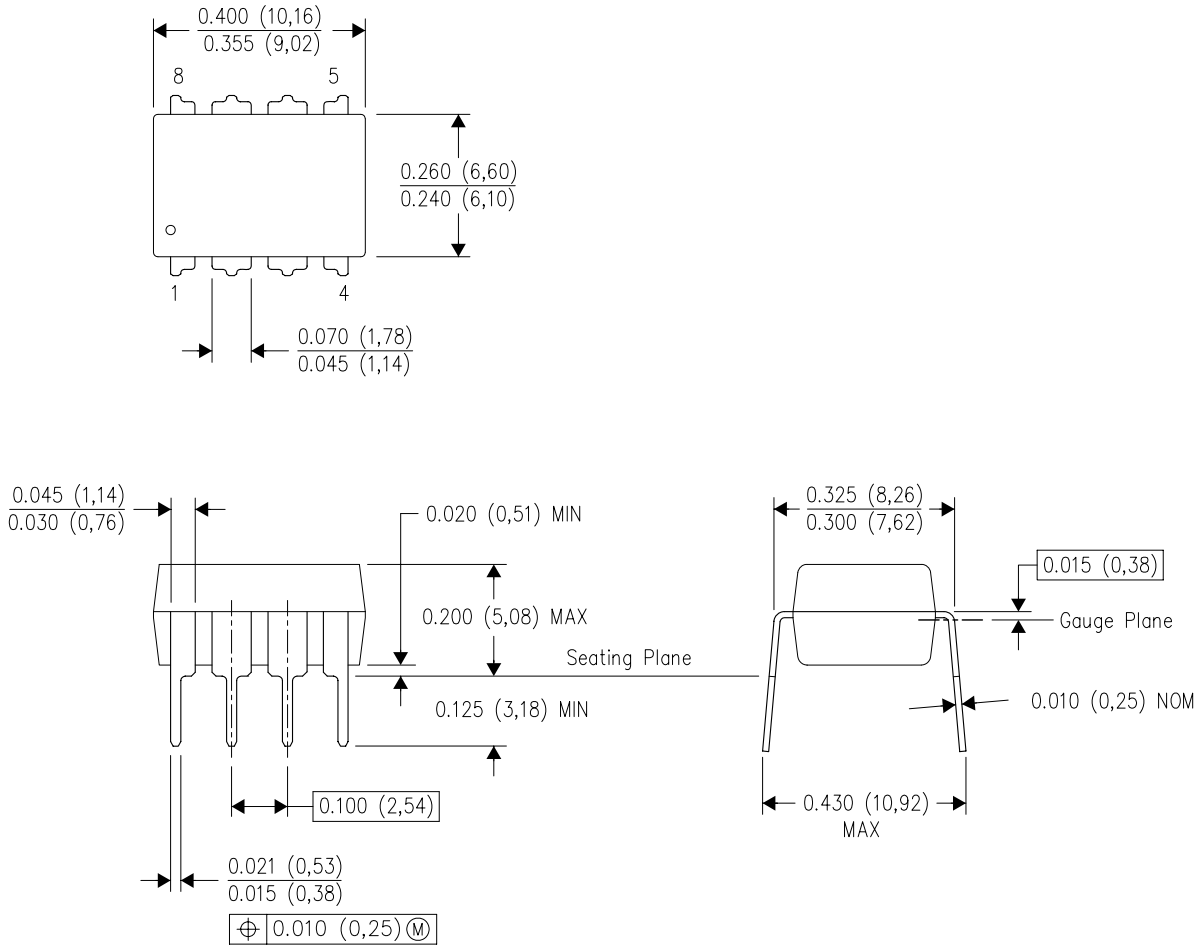
TAPE AND REEL BOX DIMENSIONS




*All dimensions are nominal

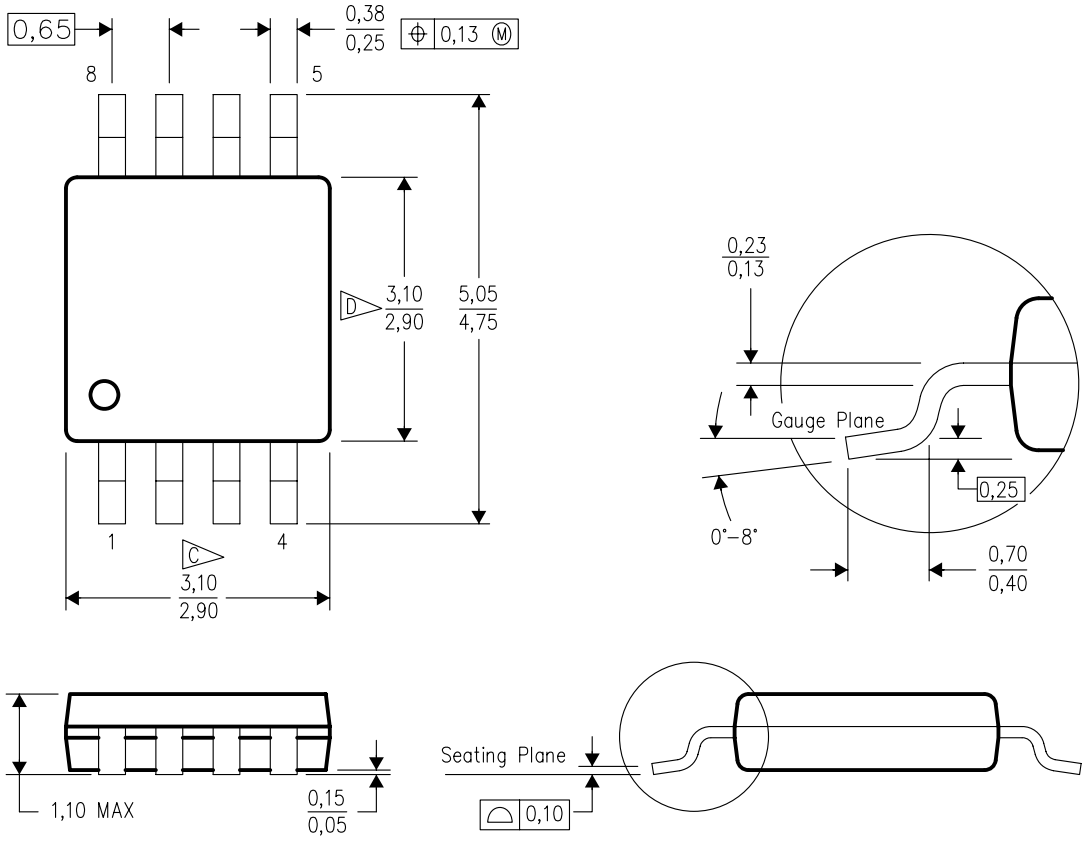
| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---|---|---|---|---|---|---|---|
| LM555CMM | VSSOP | DGK | 8 | 1000 | 210.0 | 185.0 | 35.0 |
| LM555CMM/NOPB | VSSOP | DGK | 8 | 1000 | 210.0 | 185.0 | 35.0 |
| LM555CMMX/NOPB | VSSOP | DGK | 8 | 3500 | 367.0 | 367.0 | 35.0 |
| LM555CMX | SOIC | D | 8 | 2500 | 367.0 | 367.0 | 35.0 |
| LM555CMX/NOPB | SOIC | D | 8 | 2500 | 367.0 | 367.0 | 35.0 |

P (R–PDIP–T8) PLASTIC DUAL–IN–LINE PACKAGE




NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001 variation BA.

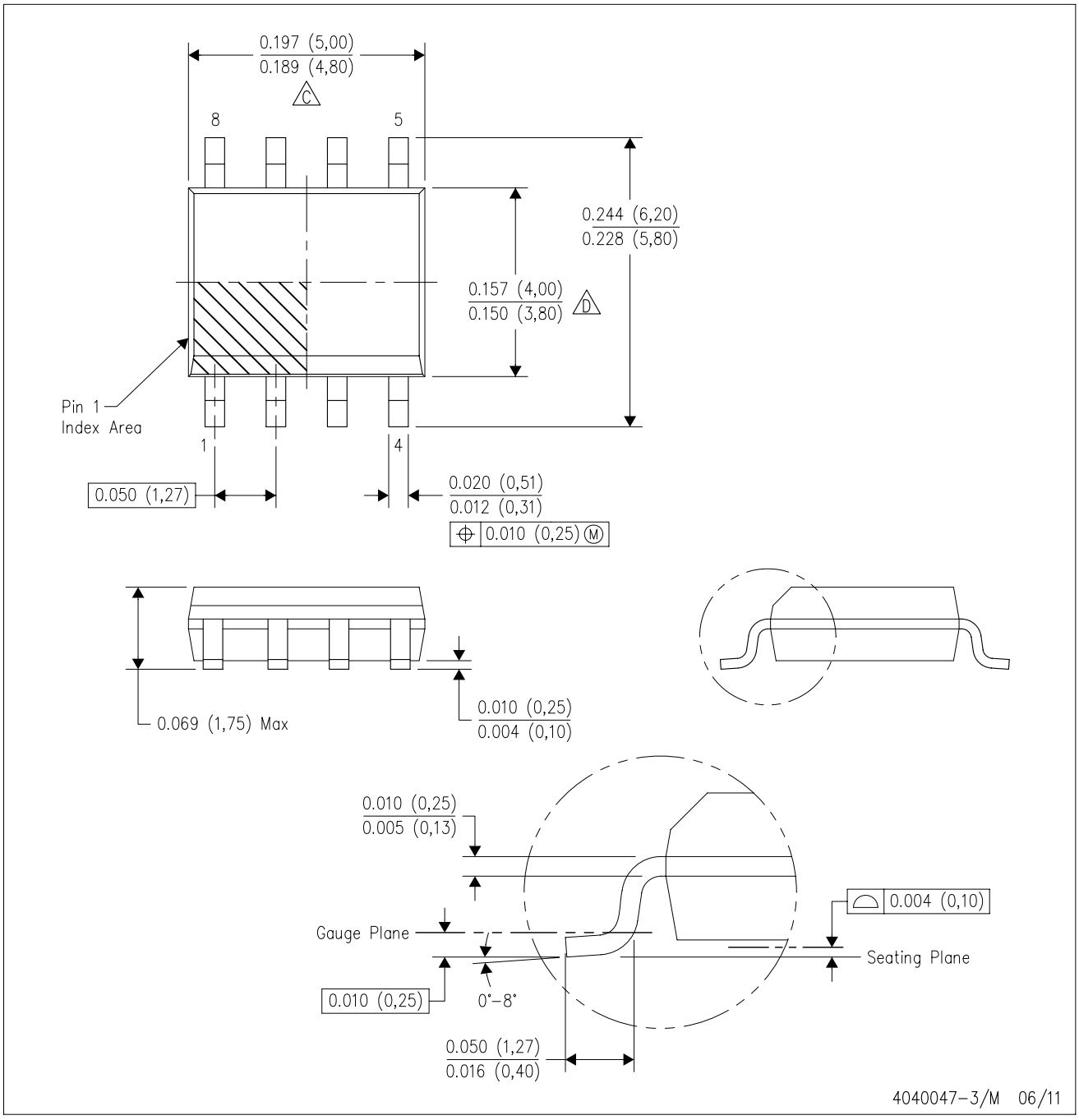
## DGK (S–PDSO–G8) PLASTIC SMALL–OUTLINE PACKAGE




4073329/E 05/06

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 per end.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.50 per side.
E. Falls within JEDEC MO–187 variation AA, except interlead flash.

D (R–PDSO–G8) PLASTIC SMALL OUTLINE




NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS–012 variation AA.

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