4 MHz, 7 nV/√Hz, Low Offset and Drift, High Precision Amplifiers

Data Sheet

ADA4077-2/ADA4077-4

FEATURES

- Low offset voltage and offset voltage drift
  - B Grade at 25 µV and 0.25 µV/°C
  - A Grade as low as 50 µV and 0.55 µV/°C
  - Offset voltage maximum specified at T_A = 25°C
  - Drift maximum specified from −40°C to +125°C
- MSL1 rated
- Low input bias current: 1 nA maximum
- Low voltage noise density: 7 nV/√Hz typical
- CMRR, PSRR, and A_V > 120 dB minimum
- Low supply current: 400 µA per amplifier typical
- Wide gain bandwidth product: 3.9 MHz
- Dual-supply operation: ±2.5 V to ±15 V
- Unity-gain stable
- No phase reversal

APPLICATIONS

- Process control front-end amplifiers
- Wireless base station control circuits
- Optical network control circuits
- Instrumentation
- Sensors and controls: thermocouples, RTDs, strain bridges, and shunt current measurements
- Precision filters

GENERAL DESCRIPTION

The ADA4077-2 dual and ADA4077-4 quad amplifiers feature extremely low offset voltage and drift and low input bias current, noise, and power consumption. Outputs are stable with capacitive loads of more than 1000 pF with no external compensation.

Applications for this amplifier include sensor signal conditioning (such as thermocouples, RTDs, strain gauges), process control front-end amplifiers, and precision diode power measurement in optical and wireless transmission systems. The ADA4077-2 and ADA4077-4 are useful in line powered and portable instrumentation, precision filters, and voltage or current measurement and level setting.

Unlike amplifiers by some competitors, the ADA4077-2 and ADA4077-4 have a MSL1 rating that is compliant with the most stringent of assembly processes, and they are specified over the extended industrial temperature range from −40°C to +125°C for the most demanding operating environments. The ADA4077-2 is available in an 8-lead SOIC package, including the B Grade, and an 8-lead MSOP package (A Grade only). The ADA4077-4 is offered in a 14-lead TSSOP package and a 14-lead SOIC package.

PIN CONNECTION DIAGRAMS

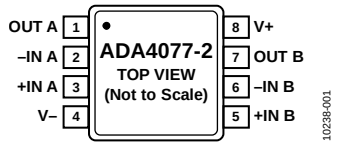

Figure 1. ADA4077-2, 8-Lead MSOP and 8-Lead SOIC

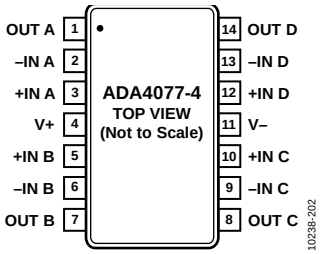

Figure 2. ADA4077-4, 14-Lead TSSOP and 14-Lead SOIC

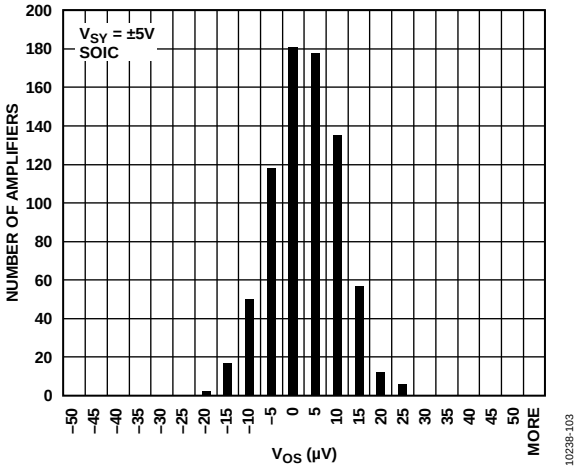

Figure 3. Offset Voltage Distribution

Table 1. Evolution of Precision Devices by Generation

Op Amp	First	Second	Third	Fourth	Fifth	Sixth
Single	OP07	OP77	OP177	OP1177	AD8677	
Dual				OP2177		ADA4077-2
Quad				OP4177		ADA4077-4

Rev. A
Document Feedback

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Changes to Ordering Guide ... 23

10/12—Revision 0: Initial Version

SPECIFICATIONS

ELECTRICAL CHARACTERISTICS, ±5 V

V_{SY} = ±5.0 V, V_{CM} = 0 V, T_A = 25°C, unless otherwise noted.

Table 2.

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
INPUT CHARACTERISTICS						
Offset Voltage (B Grade, 8-Lead SOIC)	V_{OS}			10	25	µV
		−40°C < T_A < +125°C			65	µV
Offset Voltage Drift (B Grade, 8-Lead SOIC)	$\Delta V_{OS}/\Delta T$	−40°C < T_A < +125°C		0.1	0.25	µV/°C
Offset Voltage (A Grade)	V_{OS}					
8-Lead SOIC and 14-Lead SOIC				15	50	µV
		−40°C < T_A < +125°C			105	µV
8-Lead MSOP				50	90	µV
		−40°C < T_A < +125°C			220	µV
14-Lead TSSOP				15	120	µV
		−40°C < T_A < +125°C			220	µV
Offset Voltage Drift (A Grade)	$\Delta V_{OS}/\Delta T$	−40°C < T_A < +125°C				
8-Lead SOIC				0.25	0.55	µV/°C
8-Lead MSOP and 14-Lead TSSOP				0.5	1.2	µV/°C
14-Lead SOIC				0.4	0.75	µV/°C
Input Bias Current	I_B		−1	−0.4	+1	nA
		−40°C < T_A < +125°C	−1.5		+1.5	nA
Input Offset Current	I_{OS}		−0.5	+0.1	+0.5	nA
		−40°C < T_A < +125°C	−1.0		+1.0	nA
Input Voltage Range			−3.8		+3	V
Common-Mode Rejection Ratio	CMRR	V_{CM} = −3.8 V to +3 V	122	140		dB
		−40°C < T_A < +125°C	120			dB
Large Signal Voltage Gain	A_V	R_L = 2 kΩ, V_O = −3.0 V to +3.0 V	121	130		dB
		−40°C < T_A < +125°C	120			dB
Input Capacitance	C_{INCM}	Common mode		5		pF
Input Resistance	R_{IN}	Common mode		70		GΩ
OUTPUT CHARACTERISTICS						
Output Voltage High	V_{OH}	I_L = 1 mA	4.1			V
		−40°C < T_A < +125°C	4			V
Output Voltage Low	V_{OL}	I_L = 1 mA			−3.5	V
		−40°C < T_A < +125°C			−3.2	V
Output Current	I_{OUT}	$V_{DROPOUT}$ < 1.6 V		±10		mA
Short-Circuit Current	I_{SC}	T_A = 25°C		22		mA
Closed-Loop Output Impedance	Z_{OUT}	f = 1 kHz, A = +1		0.05		Ω
POWER SUPPLY						
Power Supply Rejection Ratio	PSRR	V_S = ±2.5 V to ±18 V	123	128		dB
		−40°C < T_A < +125°C	120			dB
Supply Current per Amplifier	I_{SY}	V_O = 0 V		400	450	µA
		−40°C < T_A < +125°C			650	µA
DYNAMIC PERFORMANCE						
Slew Rate	SR	R_L = 2 kΩ		1.2		V/µs
Settling Time to 0.1%	t_S	V_{IN} = 1 V step, R_L = 2 kΩ, A = −1		3		µs
Gain Bandwidth Product	GBP	V_{IN} = 10 mV p-p, R_L = 2 kΩ, A_V = +100		3.9		MHz
Unity-Gain Crossover	UGC	V_{IN} = 10 mV p-p, R_L = 2 kΩ, A_V = +1		3.9		MHz
−3 dB Closed-Loop Bandwidth	−3 dB	A_V = +1, V_{IN} = 10 mV p-p, R_L = 2 kΩ		5.9		MHz
Phase Margin	ΦM	V_{IN} = 10 mV p-p, R_L = 2 kΩ, A_V = +1		55		Degrees
Total Harmonic Distortion Plus Noise	THD + N	V_{IN} = 1 V rms, A = +1, R_L = 2 kΩ, f = 1 kHz		0.004		%

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
NOISE PERFORMANCE						
Voltage Noise	e_n p-p	0.1 Hz to 10 Hz		0.25		μV p-p
Voltage Noise Density	e_n	f = 1 Hz		13		nV/√Hz
		f = 100 Hz		7		nV/√Hz
		f = 1000 Hz		6.9		nV/√Hz
Current Noise Density	i_n	f = 1 kHz		0.2		pA/√Hz
MULTIPLE AMPLIFIERS CHANNEL SEPARATION	C_S	f = 1 kHz, R_L = 10 kΩ		−125		dB

ELECTRICAL CHARACTERISTICS, ±15 V

V_{SY} = ±15 V, V_{CM} = 0 V, T_A = 25°C, unless otherwise noted.

Table 3.

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
INPUT CHARACTERISTICS						
Offset Voltage (B Grade, 8-Lead SOIC)	V_{OS}			10	35	μV
		−40°C < T_A < +125°C			65	μV
Offset Voltage Drift (B Grade, 8-Lead SOIC)	$\Delta V_{OS}/\Delta T$	−40°C < T_A < +125°C		0.1	0.25	μV/°C
Offset Voltage (A Grade)	V_{OS}					
8-Lead SOIC and 14-Lead SOIC				15	50	μV
		−40°C < T_A < +125°C			105	μV
8-Lead MSOP				50	90	μV
		−40°C < T_A < +125°C			220	μV
14-Lead TSSOP				15	120	μV
		−40°C < T_A < +125°C			220	μV
Offset Voltage Drift (A Grade)	$\Delta V_{OS}/\Delta T$	−40°C < T_A < +125°C				
8-Lead SOIC				0.2	0.55	μV/°C
8-Lead MSOP and 14-Lead TSSOP				0.5	1.2	μV/°C
14-Lead SOIC				0.4	0.75	μV/°C
Input Bias Current	I_B		−1	−0.4	+1	nA
		−40°C < T_A < +125°C	−1.5		+1.5	nA
Input Offset Current	I_{OS}		−0.5	+0.1	+0.5	nA
		−40°C < T_A < +125°C	−1.0		+1.0	nA
Input Voltage Range			−13.8		+13	V
Common-Mode Rejection Ratio	CMRR	V_{CM} = −13.8 V to +13 V	132	150		dB
		−40°C < T_A < +125°C	130			dB
Large Signal Voltage Gain						
8-Lead SOIC and 8-Lead MSOP	A_V	R_L = 2 kΩ, V_O = −13.0 V to +13.0 V	125	130		dB
		−40°C < T_A < +125°C	120			dB
14-Lead TSSOP and 14-Lead SOIC	A_V	R_L = 2 kΩ, V_O = −13.0 V to +13.0 V	122	130		dB
		−40°C < T_A < +125°C	120			dB
Input Capacitance	C_{INDM}	Differential mode		3		pF
	C_{INCM}	Common mode		5		pF
Input Resistance	R_{IN}	Common mode		100		GΩ
OUTPUT CHARACTERISTICS						
Output Voltage High	V_{OH}	I_L = 1 mA	14.1			V
		−40°C < T_A < +125°C	14			V
Output Voltage Low	V_{OL}	I_L = 1 mA			−13.5	V
		−40°C < T_A < +125°C			−13.2	V
Output Current	I_{OUT}	$V_{DROPOUT}$ < 1.2 V		±10		mA
Short-Circuit Current	I_{SC}	T_A = 25°C		22		mA
Closed-Loop Output Impedance	Z_{OUT}	f = 1 kHz, A = +1		0.05		Ω

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
POWER SUPPLY						
Power Supply Rejection Ratio	PSRR	V_S = ±2.5 V to ±18 V	123	128		dB
		−40°C < T_A < +125°C	120			dB
Supply Current per Amplifier	I_{SY}	V_O = 0 V		400	500	µA
		−40°C < T_A < +125°C			650	µA
DYNAMIC PERFORMANCE						
Slew Rate	SR	R_L = 2 kΩ		1.2		V/µs
Settling Time to 0.01%	t_s	V_{IN} = 10 V p-p, R_L = 2 kΩ, A = −1		16		µs
Settling Time to 0.1%	t_s	V_{IN} = 10 V p-p, R_L = 2 kΩ, A = −1		10		µs
Gain Bandwidth Product	GBP	V_{IN} = 10 mV p-p, R_L = 2 kΩ, A_V = +100		3.6		MHz
Unity-Gain Crossover	UGC	V_{IN} = 10 mV p-p, R_L = 2 kΩ, A_V = +1		3.9		MHz
−3 dB Closed-Loop Bandwidth	−3 dB	A_V = +1, V_{IN} = 10 mV p-p, R_L = 2 kΩ		5.5		MHz
Phase Margin	ΦM	V_{IN} = 10 mV p-p, R_L = 2 kΩ, A_V = +1		58		Degrees
Total Harmonic Distortion Plus Noise	THD + N	V_{IN} = 1 V rms, A = +1, R_L = 2 kΩ, f = 1 kHz		0.004		%
NOISE PERFORMANCE						
Voltage Noise	e_n p-p	0.1 Hz to 10 Hz		0.25		µV p-p
Voltage Noise Density	e_n	f = 1 Hz		13		nV/√Hz
		f = 100 Hz		7		nV/√Hz
		f = 1000 Hz		6.9		nV/√Hz
Current Noise Density	i_n	f = 1 kHz		0.2		pA/√Hz
MULTIPLE AMPLIFIERS CHANNEL SEPARATION	C_S	f = 1 kHz, R_L = 10 kΩ		−125		dB

ABSOLUTE MAXIMUM RATINGS

Table 4.

Parameter	Rating
Supply Voltage	36 V
Input Voltage	$\pm V_{SY}$
Input Current[1]	±10 mA
Differential Input Voltage	$\pm V_{SY}$
Output Short-Circuit Duration to GND	Indefinite
Storage Temperature Range	−65°C to +150°C
Operating Temperature Range	−40°C to +125°C
Junction Temperature Range	−65°C to +150°C
Lead Temperature, Soldering (10 sec)	300°C
ESD Human Body Model[2]	6 kV
Field Induced Charge Device Model (FICDM)[3]	1.25 kV

[1] The input pins have clamp diodes to the power supply pins and to each other. Limit the input current to 10 mA or less whenever input signals exceed the power supply rail by 0.3 V.
[2] ESDA/JEDEC JS-001-2011 applicable standard.
[3] JESD22-C101 (ESD FICDM standard of JEDEC) applicable standard.

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

THERMAL RESISTANCE

θ_{JA} is specified for the worst-case conditions, that is, a device soldered in a circuit board for surface-mount packages.

Table 5. Thermal Resistance

Package Type	θ_{JA}	θ_{JC}	Unit
8-Lead MSOP	190	44	°C/W
8-Lead SOIC	158	43	°C/W
14-Lead TSSOP	240	43	°C/W
14-Lead SOIC	115	36	°C/W

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS

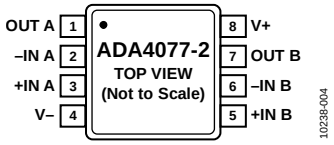


Figure 4. ADA4077-2 Pin Configuration, 8-Lead MSOP

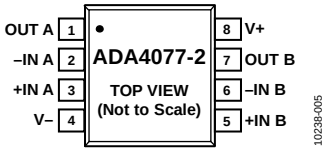


Figure 5. ADA4077-2 Pin Configuration, 8-Lead SOIC

Table 6. ADA4077-2 Pin Function Descriptions, 8-Lead MSOP and 8-Lead SOIC

Pin No.	Mnemonic	Description
1	OUT A	Output, Channel A
2	−IN A	Inverting Input, Channel A
3	+IN A	Noninverting Input, Channel A
4	V−	Negative Supply Voltage
5	+IN B	Noninverting Input, Channel B
6	−IN B	Inverting Input, Channel B
7	OUT B	Output, Channel B
8	V+	Positive Supply Voltage

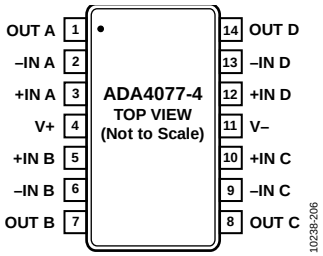


Figure 6. ADA4077-4 Pin Configuration, 14-Lead TSSOP

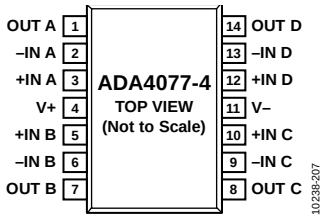


Figure 7. ADA4077-4 Pin Configuration, 14-Lead SOIC

Table 7. ADA4077-4 Pin Function Descriptions, 14-Lead TSSOP and 14-Lead SOIC

Pin No.	Mnemonic	Description
1	OUT A	Output Channel A
2	−IN A	Negative Input Channel A
3	+IN A	Positive Input Channel A
4	V+	Positive Supply Voltage
5	+IN B	Positive Input Channel B
6	−IN B	Negative Input Channel B
7	OUT B	Output Channel B
8	OUT C	Output Channel C
9	−IN C	Negative Input Channel C
10	+IN C	Positive Input Channel C
11	V−	Negative Supply Voltage
12	+IN D	Positive Input Channel D
13	−IN D	Negative Input Channel D
14	OUT D	Output Channel D

TYPICAL PERFORMANCE CHARACTERISTICS

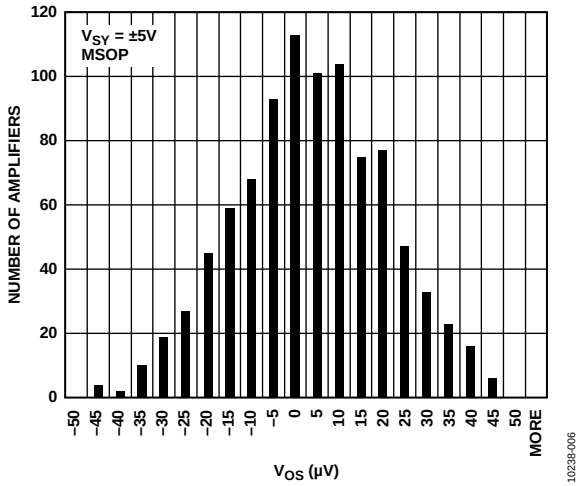


Figure 8. ADA4077-2 Offset Voltage (V_{OS}) Distribution, V_{SY} = ±5 V

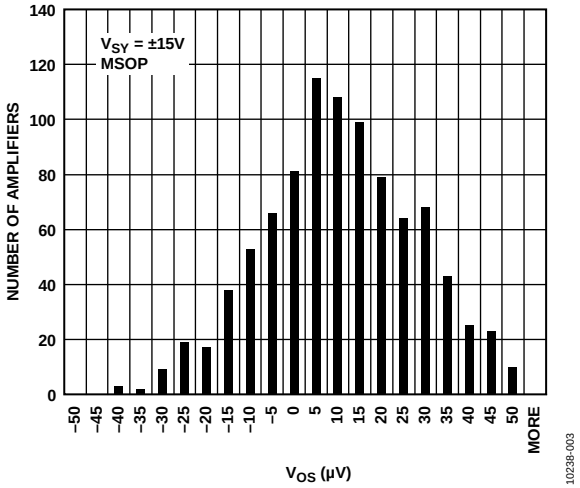


Figure 11. ADA4077-2 Offset Voltage (V_{OS}) Distribution, V_{SY} = ±15 V

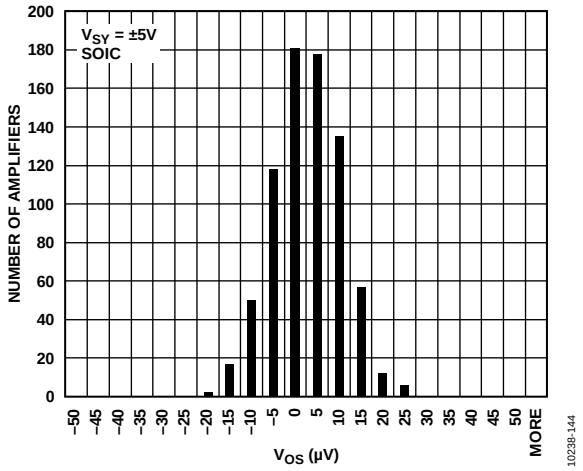


Figure 9. ADA4077-2 Offset Voltage (V_{OS}) Distribution, V_{SY} = ±5 V

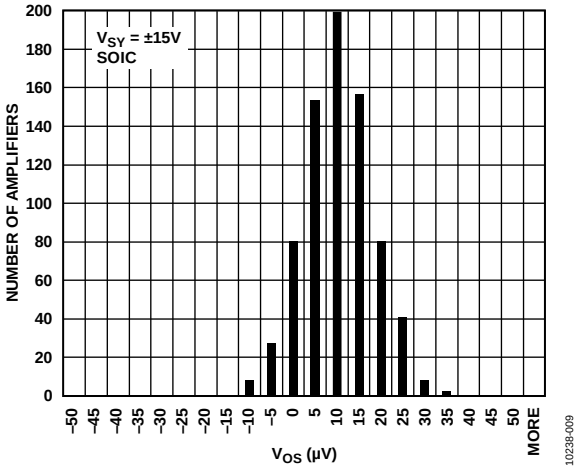


Figure 12. ADA4077-2 Offset Voltage (V_{OS}) Distribution, V_{SY} = ±15 V

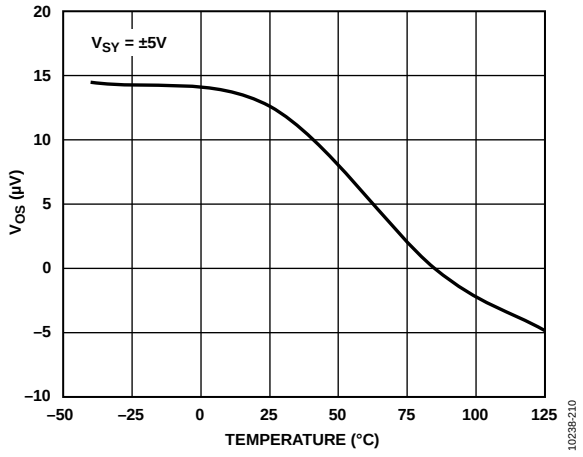


Figure 10. Offset Voltage (V_{OS}) vs. Temperature, V_{SY} = ±5 V

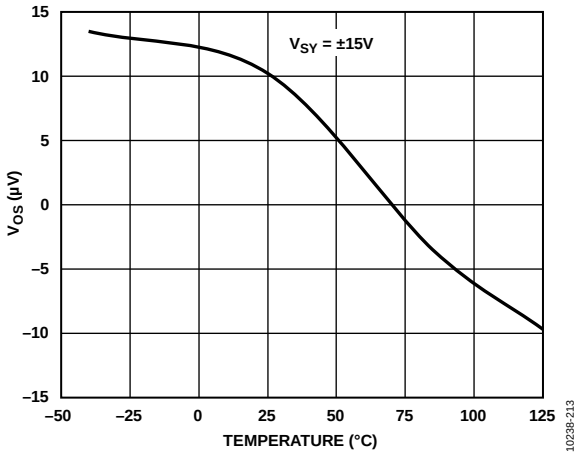


Figure 13. Offset Voltage (V_{OS}) vs. Temperature, V_{SY} = ±15 V

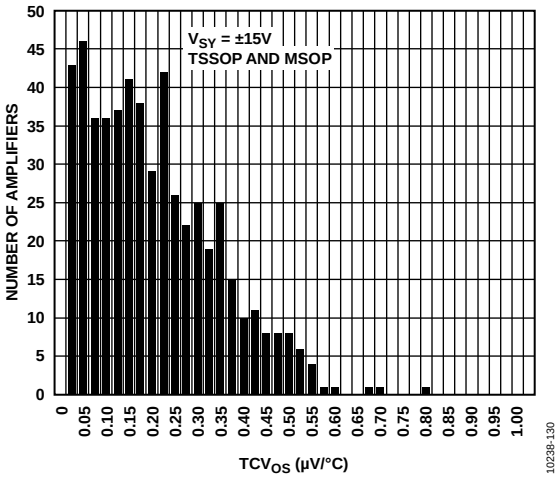


Figure 14. TCV_{OS} (TSSOP and MSOP, A Grade)

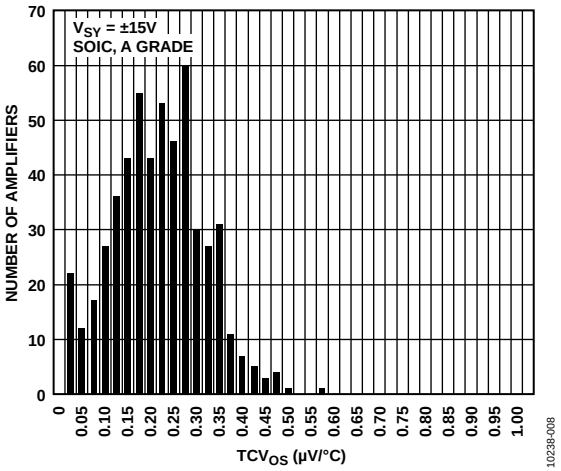


Figure 17. TCV_{OS} (SOIC, A Grade)

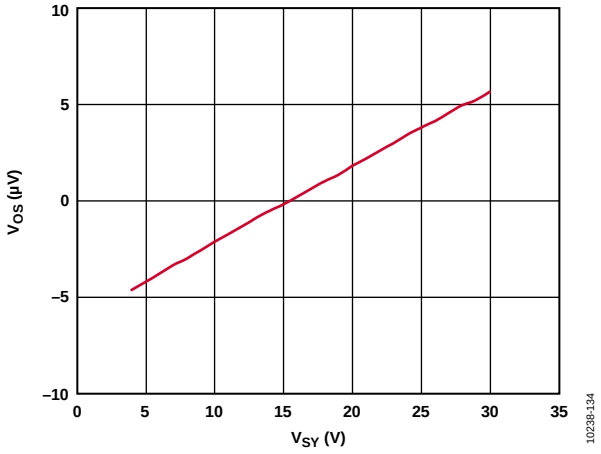


Figure 15. Offset Voltage (V_{OS}) vs. Voltage Supplies (V_{SY})

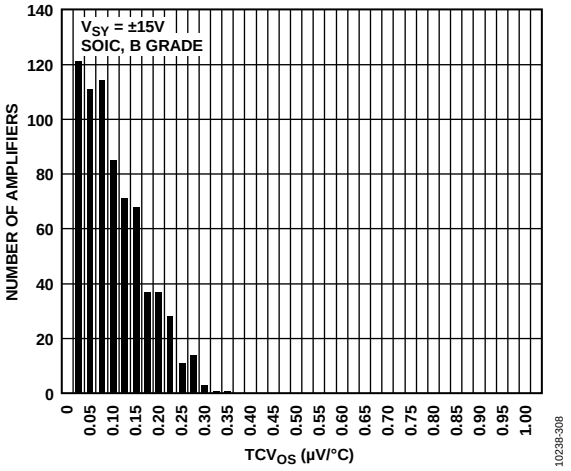


Figure 18. TCV_{OS} (SOIC, B Grade)

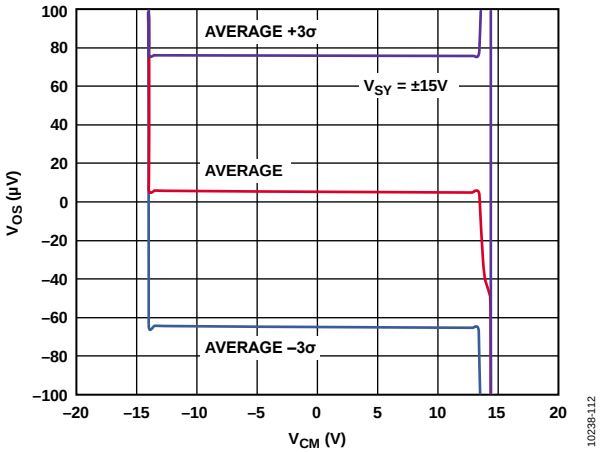


Figure 16. Offset Voltage (V_{OS}) vs. Common-Mode Voltage (V_{CM})

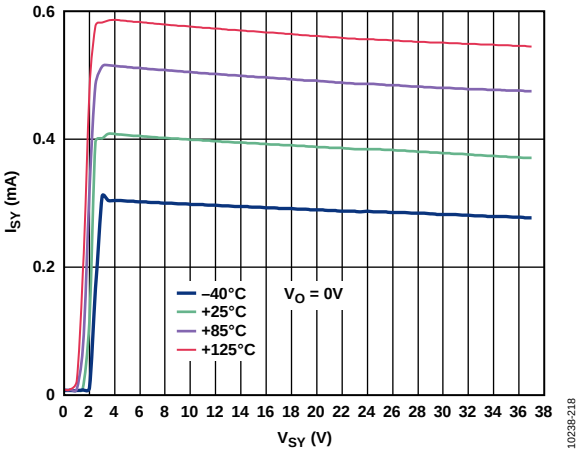


Figure 19. I_{SY} vs. V_{SY}

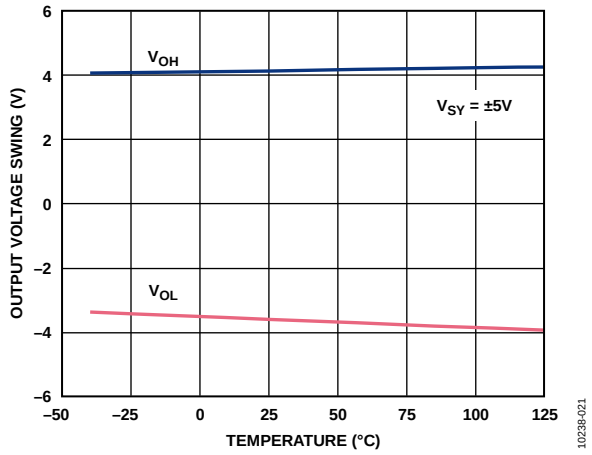


Figure 20. Output Voltage Swing vs. Temperature, V_{SY} = ±5 V

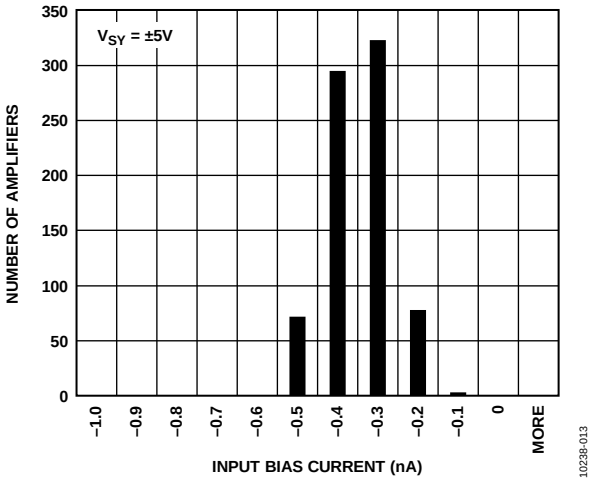


Figure 21. Input Bias Current, V_{SY} = ±5 V

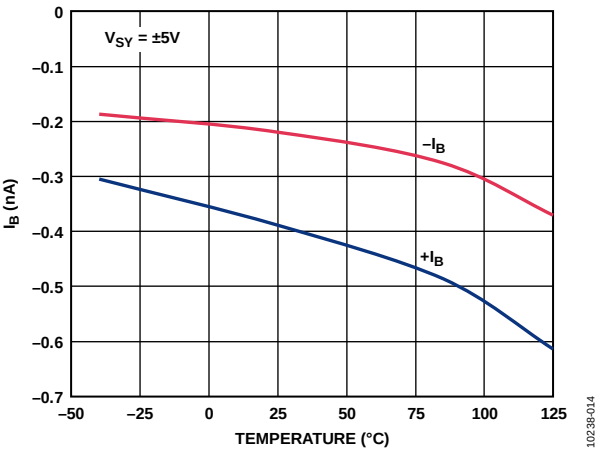


Figure 22. Input Bias Current (I_B) vs. Temperature, V_{SY} = ±5 V

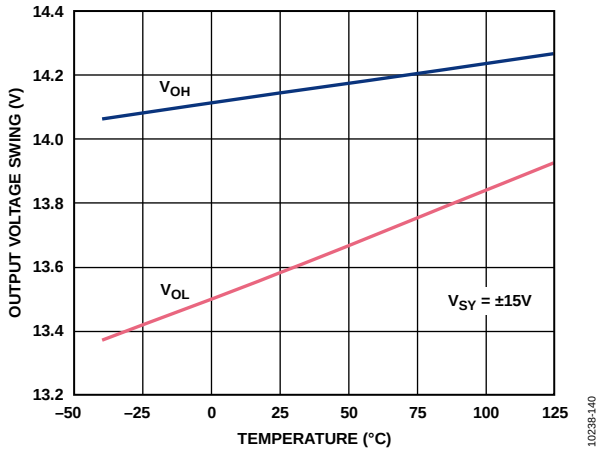


Figure 23. Output Voltage Swing vs. Temperature, V_{SY} = ±15 V

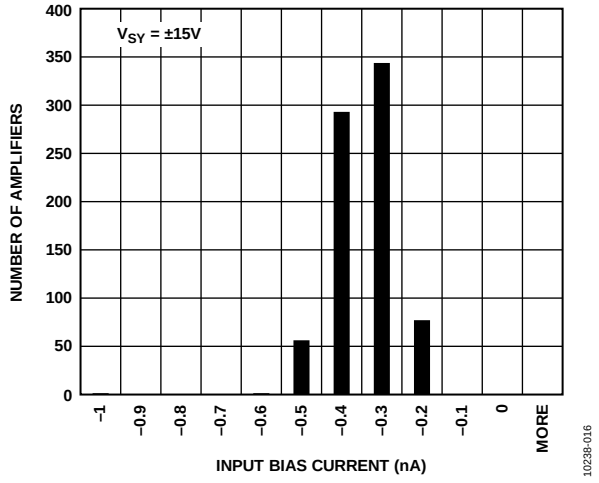


Figure 24. Input Bias Current, V_{SY} = ±15 V

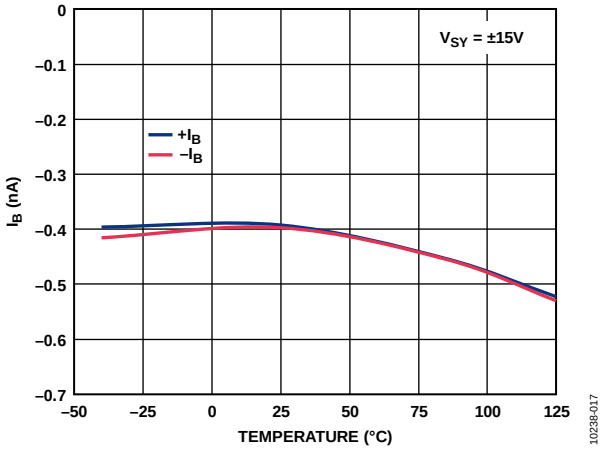


Figure 25. Input Bias Current (I_B) vs. Temperature, V_{SY} = ±15 V

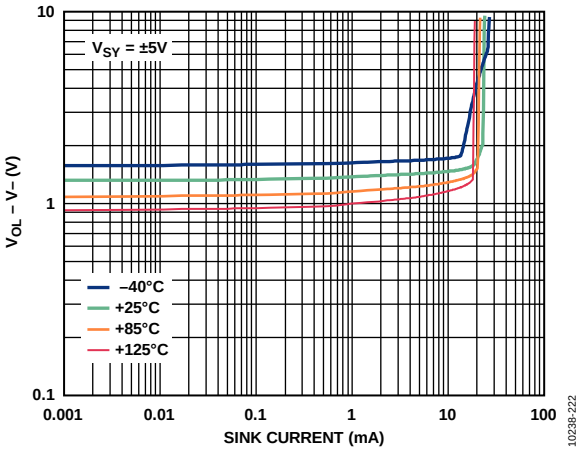


Figure 26. Output Dropout Voltage vs. Sink Current, V_{SY} = ±5 V

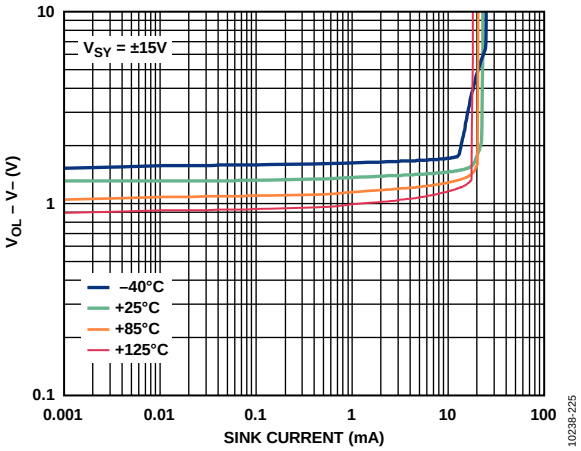


Figure 29. Output Dropout Voltage vs. Sink Current, V_{SY} = ±15 V

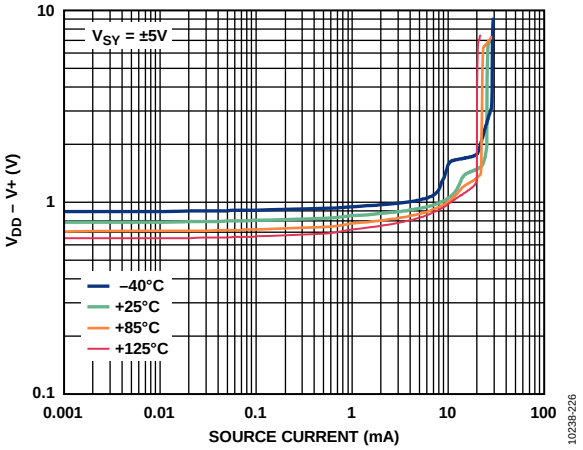


Figure 27. Output Dropout Voltage vs. Source Current, V_{SY} = ±5 V

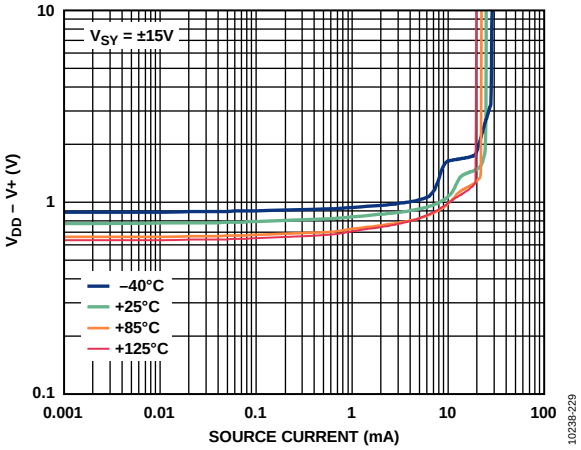


Figure 30. Output Dropout Voltage vs. Source Current, V_{SY} = ±15 V

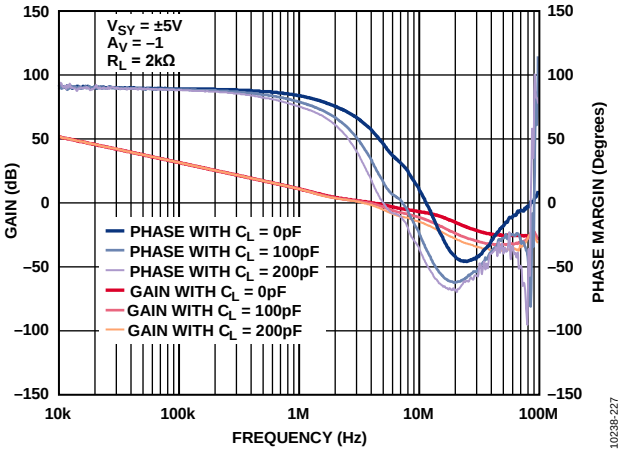


Figure 28. Open-Loop Gain and Phase vs. Frequency, V_{SY} = ±5 V

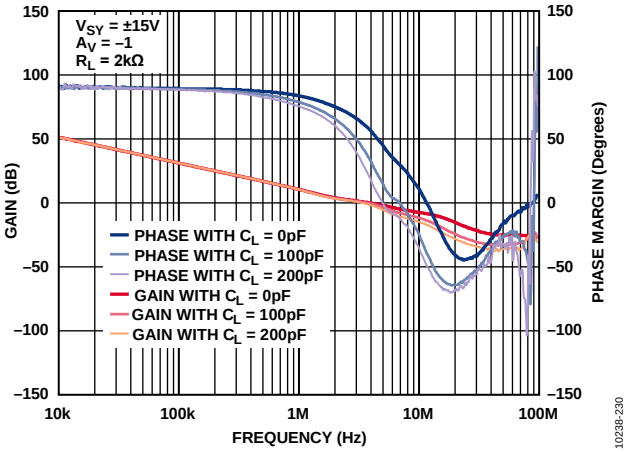


Figure 31. Open-Loop Gain and Phase vs. Frequency, V_{SY} = ±15 V

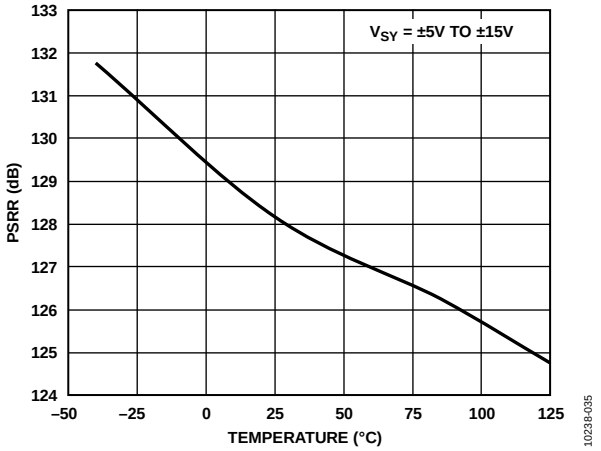


Figure 32. PSRR vs. Temperature

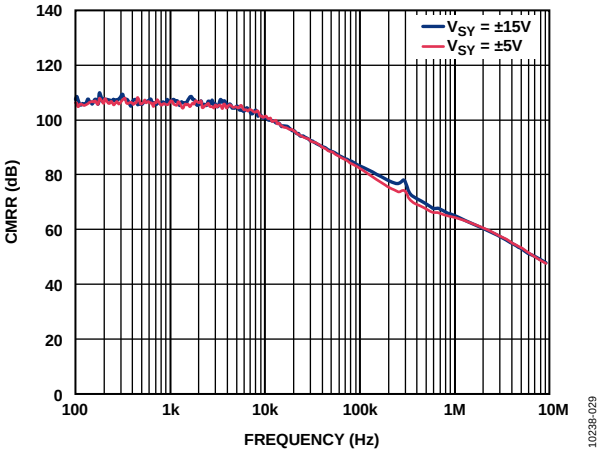


Figure 35. CMRR vs. Frequency

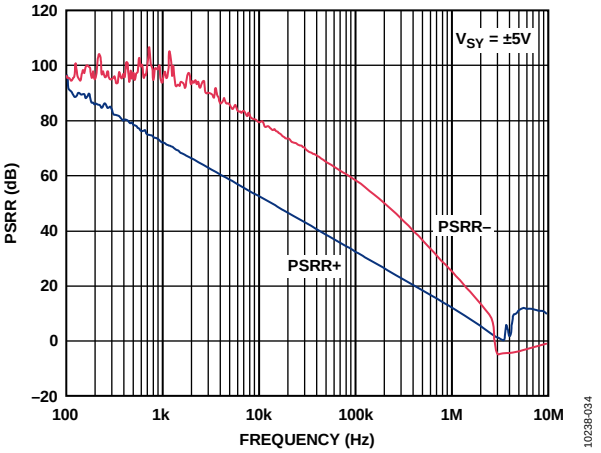


Figure 33. PSRR vs. Frequency, V_{SY} = ±5 V

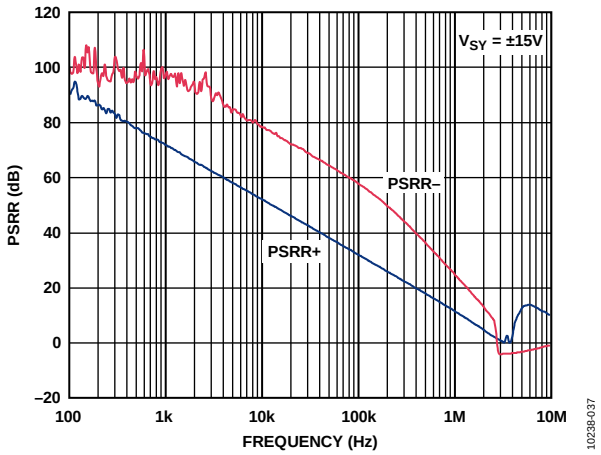


Figure 36. PSRR vs. Frequency, V_{SY} = ±15 V

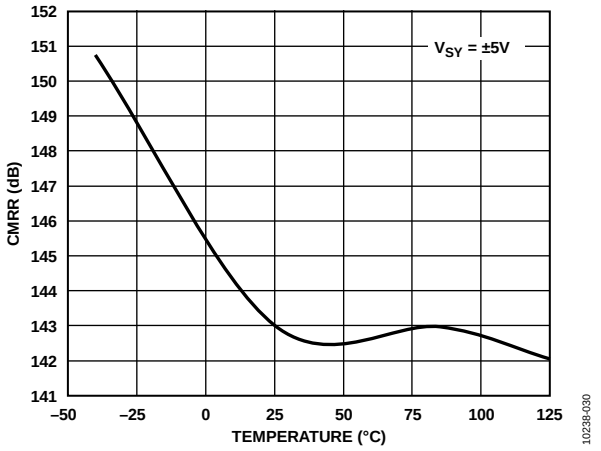


Figure 34. CMRR vs. Temperature, V_{SY} = ±5 V

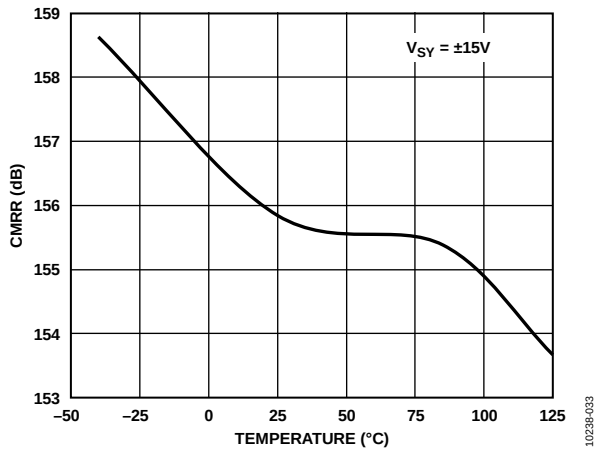


Figure 37. CMRR vs. Temperature, V_{SY} = ±15 V

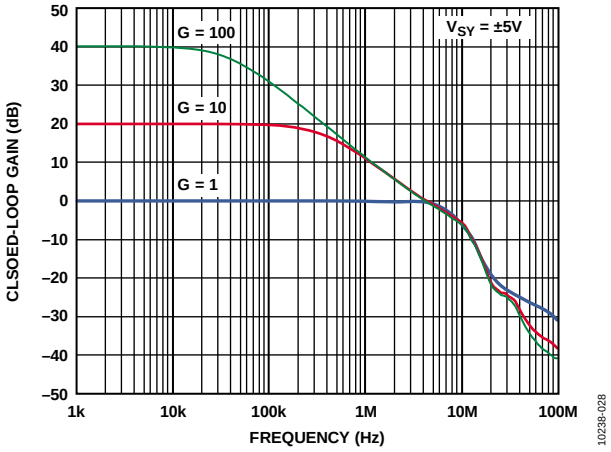


Figure 38. Closed-Loop Gain vs. Frequency, V_{SY} = ±5 V

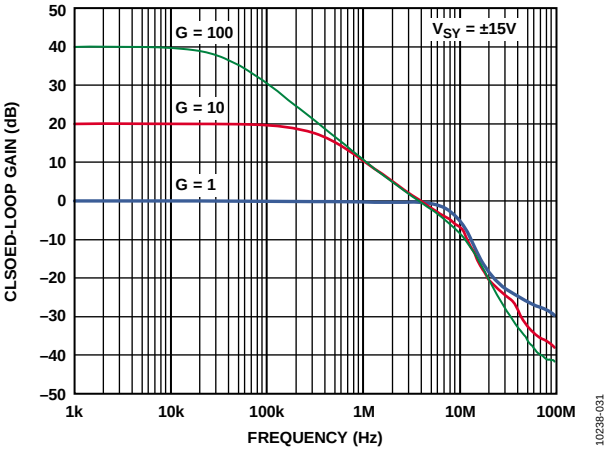


Figure 41. Closed-Loop Gain vs. Frequency, V_{SY} = ±15 V

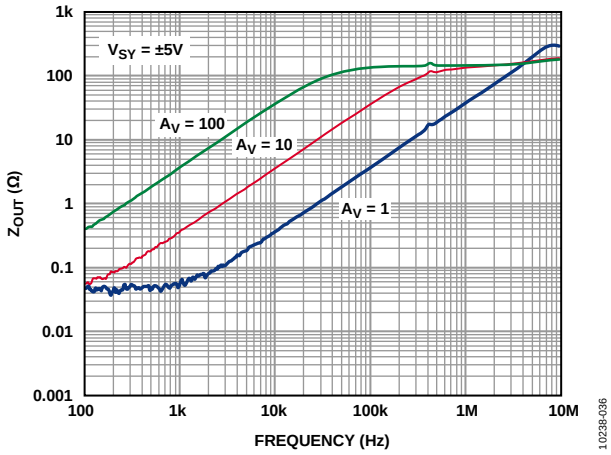


Figure 39. Output Impedance (Z_{OUT}) vs. Frequency, V_{SY} = ±5 V

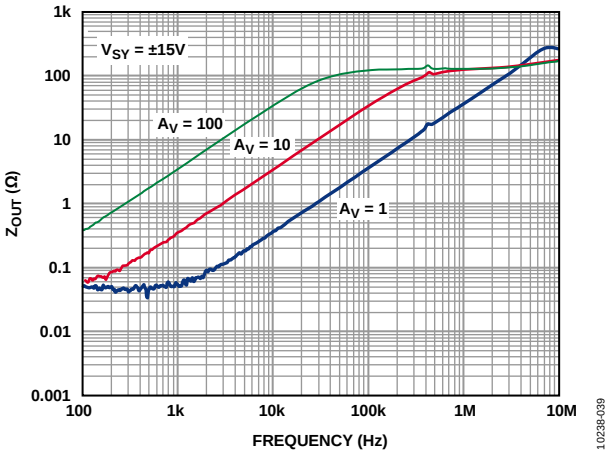


Figure 42. Output Impedance (Z_{OUT}) vs. Frequency, V_{SY} = ±15 V

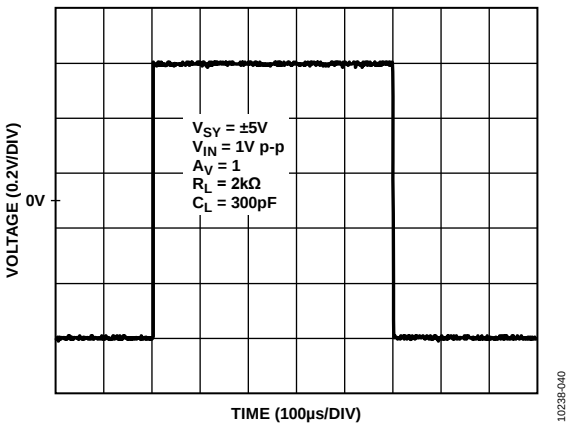


Figure 40. Large Signal Transient Response, V_{SY} = ±5 V

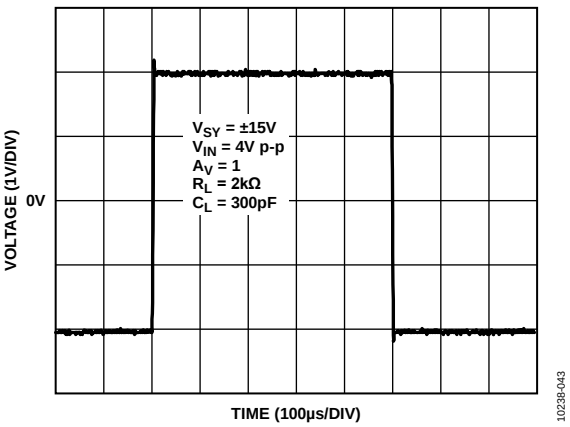


Figure 43. Large Signal Transient Response, V_{SY} = ±15 V

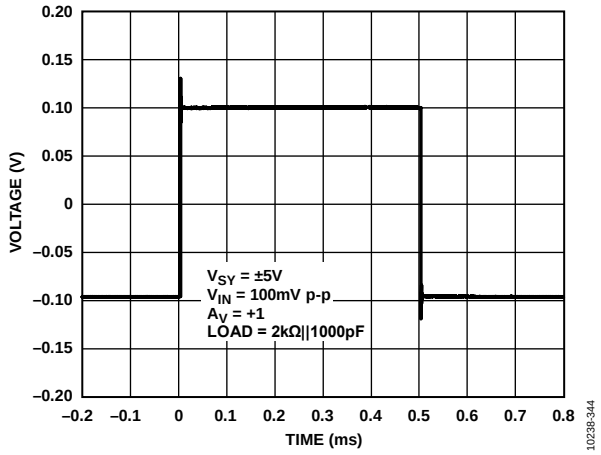


Figure 44. Small Signal Transient Response, V_{SY} = ±5 V

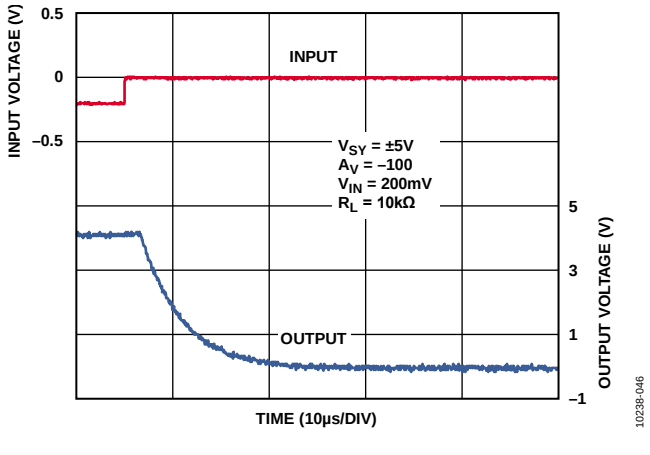


Figure 45. Positive Overload Recovery, V_{SY} = ±5 V

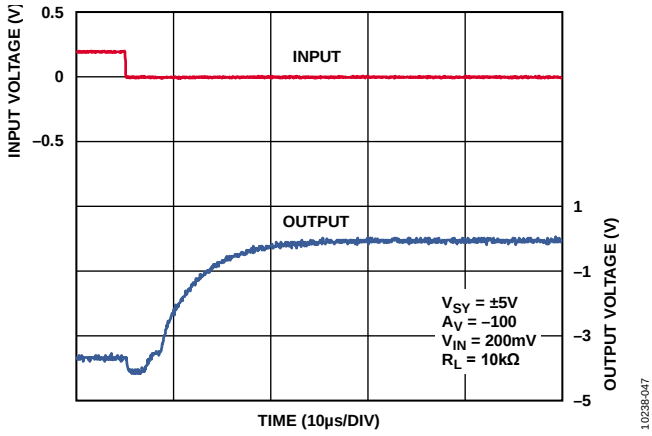


Figure 46. Negative Overload Recovery, V_{SY} = ±5 V

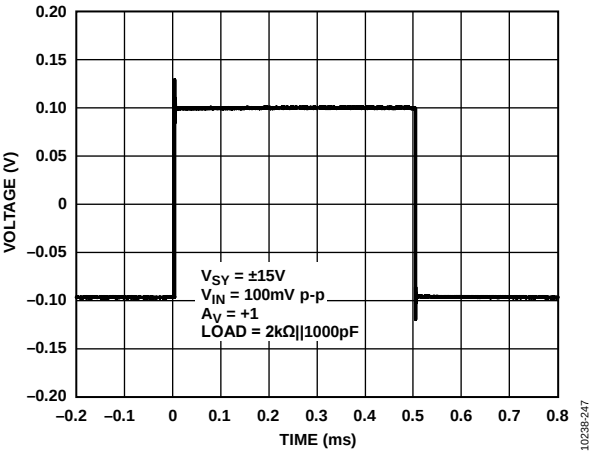


Figure 47. Small Signal Transient Response, V_{SY} = ±15 V

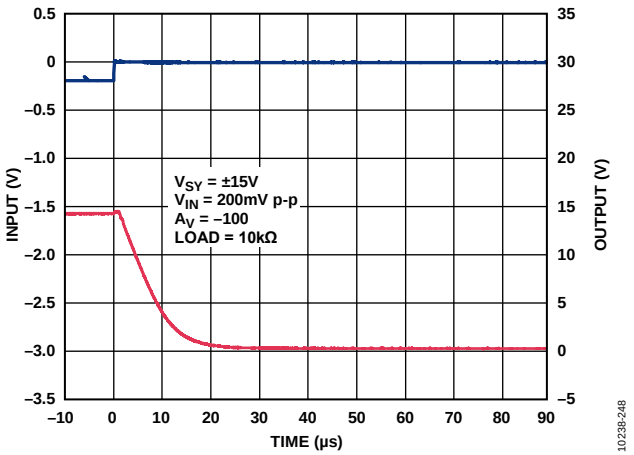


Figure 48. Positive Overload Recovery, V_{SY} = ±15 V

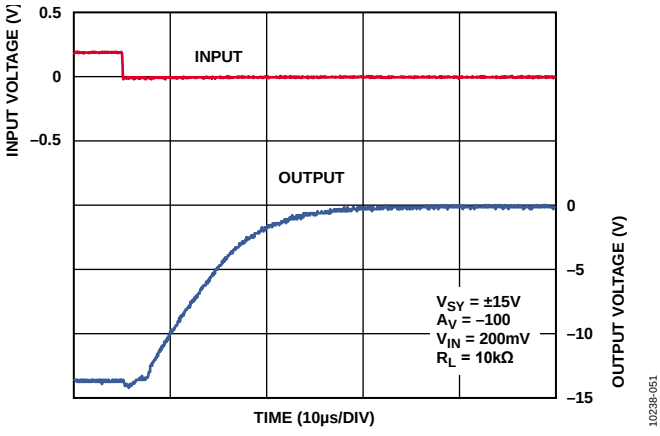


Figure 49. Negative Overload Recovery, V_{SY} = ±15 V

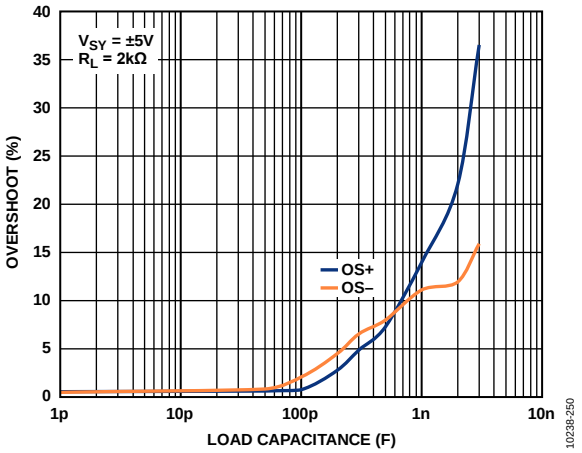


Figure 50. Small Signal Overshoot vs. Load Capacitance, V_{SY} = ±5 V

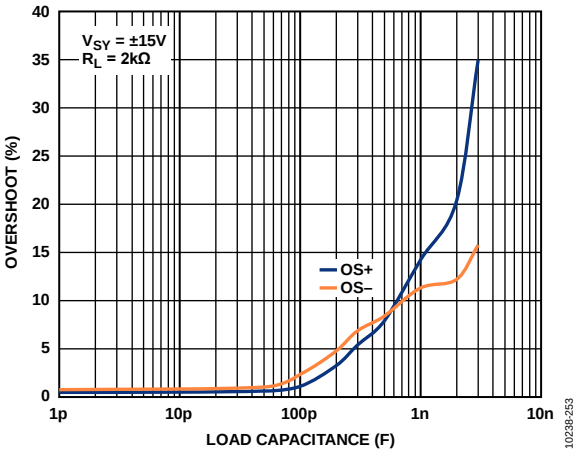


Figure 53. Small Signal Overshoot vs. Load Capacitance, V_{SY} = ±15 V

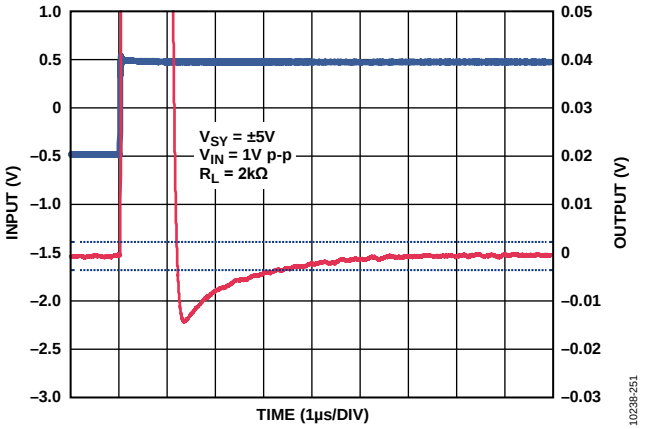


Figure 51. Positive 0.1% Settling Time, V_{SY} = ±5 V

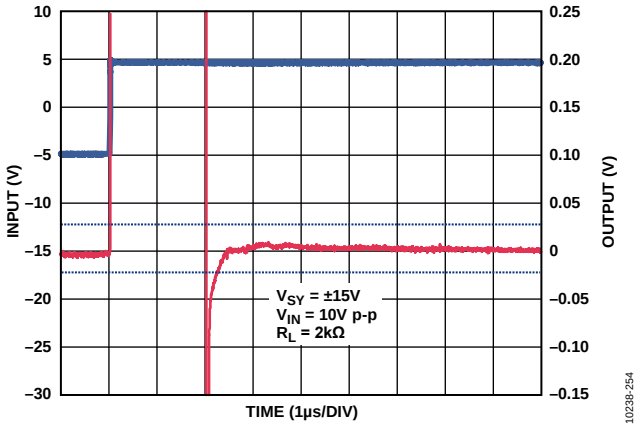


Figure 54. Positive 0.1% Settling Time, V_{SY} = ±15 V

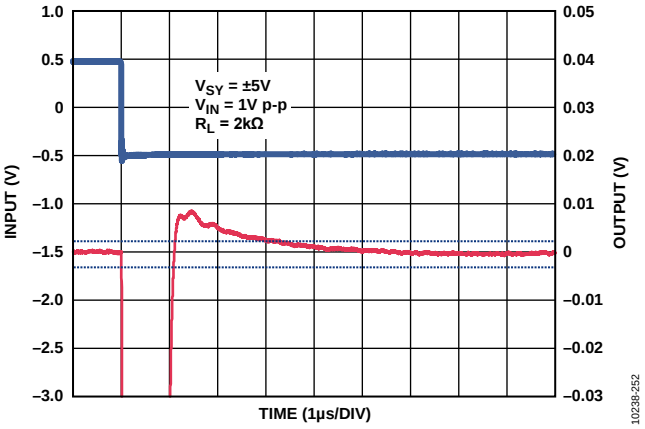


Figure 52. Negative 0.1% Settling Time, V_{SY} = ±5 V

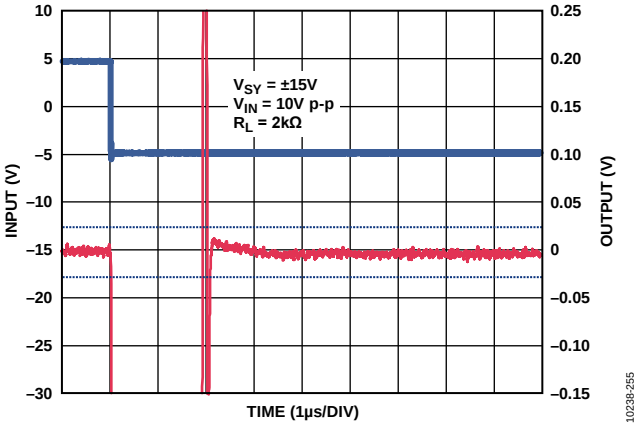


Figure 55. Negative 0.1% Settling Time, V_{SY} = ±15 V

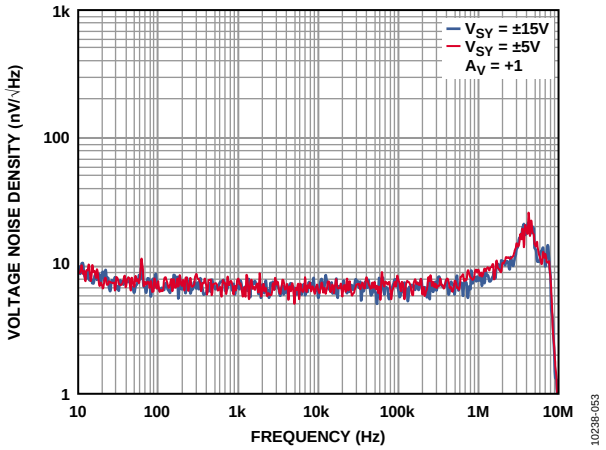


Figure 56. Voltage Noise Density vs. Frequency

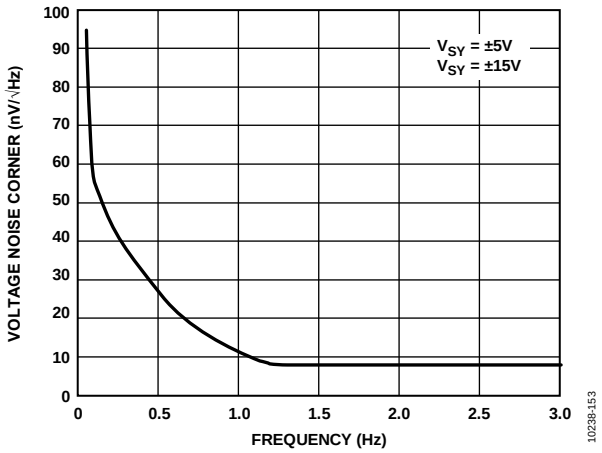


Figure 59. Voltage Noise Corner vs. Frequency, V_{SY} = ±15 V and V_{SY} = ±5 V

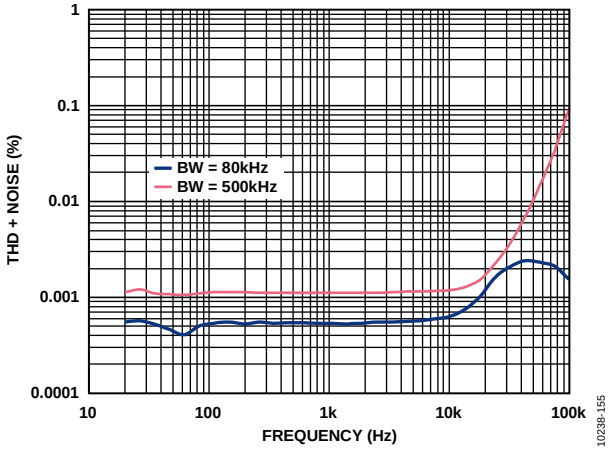


Figure 57. THD + N vs. Frequency, V_{SY} = ±5 V

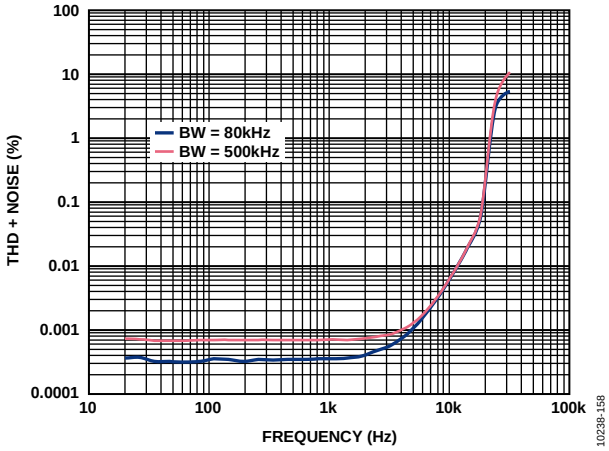


Figure 60. THD + N vs. Frequency, V_{SY} = ±15 V

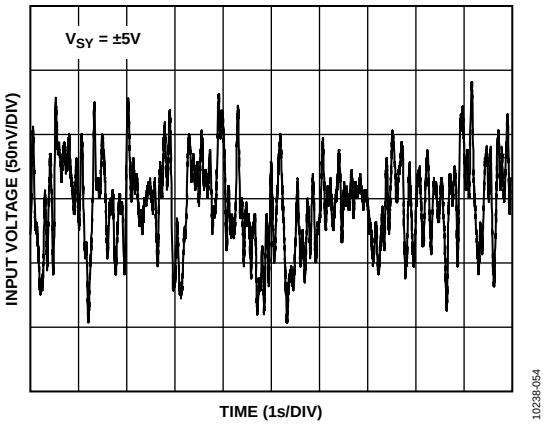


Figure 58. 0.1 Hz to 10 Hz Noise, V_{SY} = ±5 V

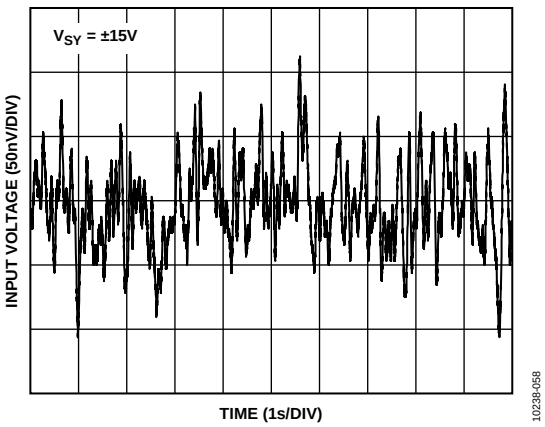


Figure 61. 0.1 Hz to 10 Hz Noise, V_{SY} = ±15 V

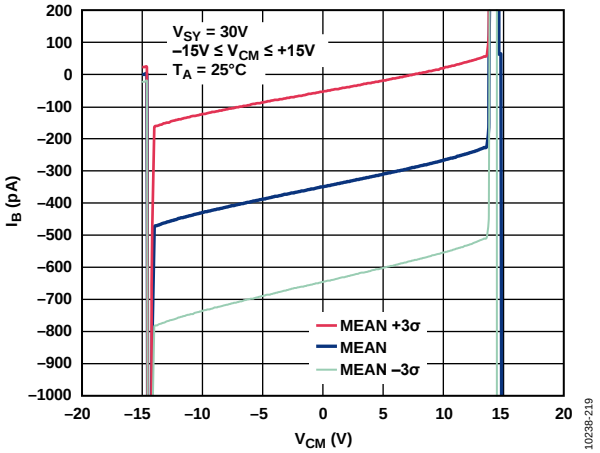


Figure 62. Input Bias Current (I_B) vs. Common-Mode Voltage (V_{CM})

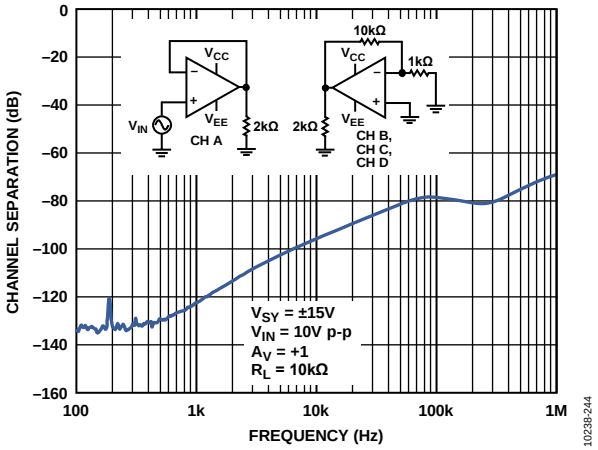


Figure 63. Channel Separation, V_{SY} = ±15 V

THEORY OF OPERATION

The ADA4077-2 and ADA4077-4 are the sixth generation of the Analog Devices, Inc., industry-standard OP07 amplifier family. The ADA4077-2 and ADA4077-4 are high precision, low noise operational amplifiers with a combination of extremely low offset voltage and very low input bias currents. Unlike JFET amplifiers, the low bias and offset currents are relatively insensitive to ambient temperatures, even up to 125°C.

The Analog Devices proprietary process technology and linear design expertise have produced a high voltage amplifier with superior performance to the OP07, OP77, OP177, and OP1177 in tiny, 8-lead SOIC and 8-lead MSOP packages (ADA4077-2) and 14-lead TSSOP and 14-lead SOIC packages (ADA4077-4). Despite its small size, the ADA4077-2 and ADA4077-4 offer numerous improvements, including low wideband noise, wide bandwidth, lower offset and offset drift, lower input bias current, and complete freedom from phase inversion.

The ADA4077-2 and ADA4077-4 have a specified operating temperature range of −40°C to +125°C with a MSL1 rating, which is as wide as any similar device in a plastic surface-mount package. This is increasingly important as PCB and overall system sizes continue to shrink, causing internal system temperatures to rise.

In the ADA4077-2 and the ADA4077-4, the power consumption is reduced by a factor of four from the OP177, and bandwidth and slew rate have both increased by a factor of six. The low power dissipation and very stable performance vs. temperature also act to reduce warm-up drift errors to insignificant levels.

Inputs are protected internally from overvoltage conditions referenced to either supply rail. Like any high performance amplifier, maximum performance is achieved by following appropriate circuit and PCB guidelines.

APPLICATIONS INFORMATION

OUTPUT PHASE REVERSAL

Phase reversal is defined as a change of polarity in the amplifier transfer function. Many operational amplifiers exhibit phase reversal when the voltage applied to the input is greater than the maximum common-mode voltage. In some instances, this can cause permanent damage to the amplifier. In feedback loops, it can result in system lockups or equipment damage. The ADA4077-2 and the ADA4077-4 are immune to phase reversal problems even at input voltages beyond the supplies.

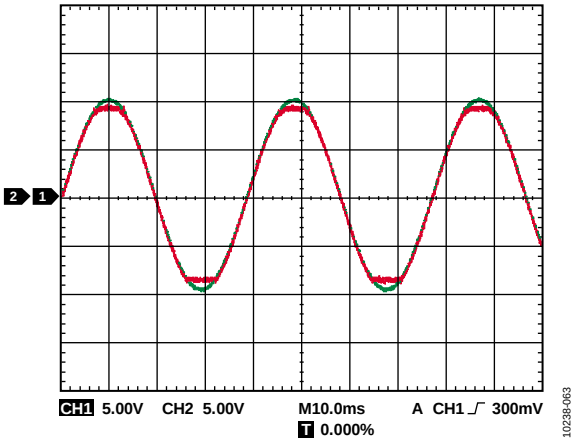


Figure 64. No Phase Reversal

LOW POWER LINEARIZED RTD

A common application for a single element varying bridge is an RTD thermometer amplifier, as shown in Figure 65. The excitation is delivered to the bridge by a 2.5 V reference applied at the top of the bridge.

RTDs can have a thermal resistance as high as 0.5°C to 0.8°C per mW. To minimize errors due to resistor drift, the current through each leg of the bridge must be kept low. In this circuit, the amplifier supply current flows through the bridge. However, at a maximum supply current of 500 µA for the ADA4077-2, the RTD dissipates less than 0.1 mW of power, even at the highest resistance. Errors due to power dissipation in the bridge are kept under 0.1°C.

Calibration of the bridge is made at the minimum value of the temperature to be measured by adjusting RP until the output is zero.

To calibrate the output span, set the full-scale and linearity potentiometers to midpoint and apply a 500°C temperature to the sensor or substitute the equivalent 500°C RTD resistance.

Adjust the full-scale potentiometer for a 5 V output. Finally, apply 250°C or the equivalent RTD resistance and adjust the linearity potentiometer for 2.5 V output. The circuit achieves better than ±0.5°C accuracy after adjustment.

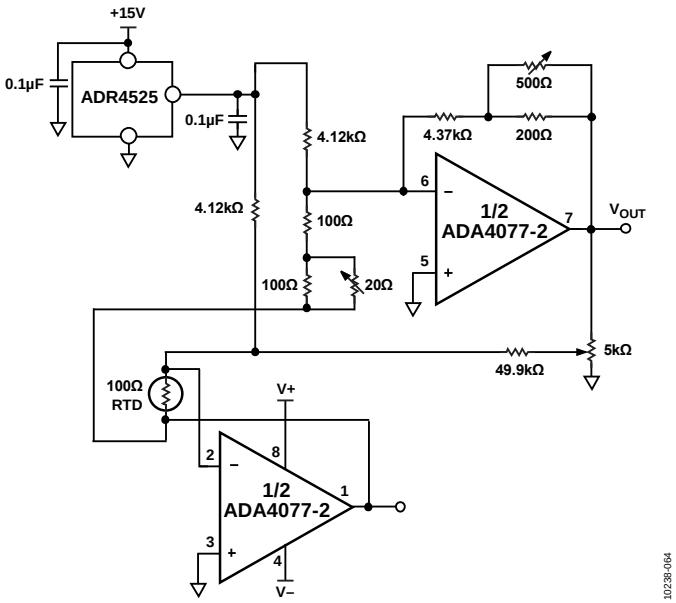


Figure 65. Low Power Linearized RTD Circuit

PROPER BOARD LAYOUT

The ADA4077-2 and ADA4077-4 are high precision devices. To ensure optimum performance at the PCB level, care must be taken in the design of the board layout.

To avoid leakage currents, maintain a clean and moisture-free board surface. Coating the surface creates a barrier to moisture accumulation and helps reduce parasitic resistance on the board.

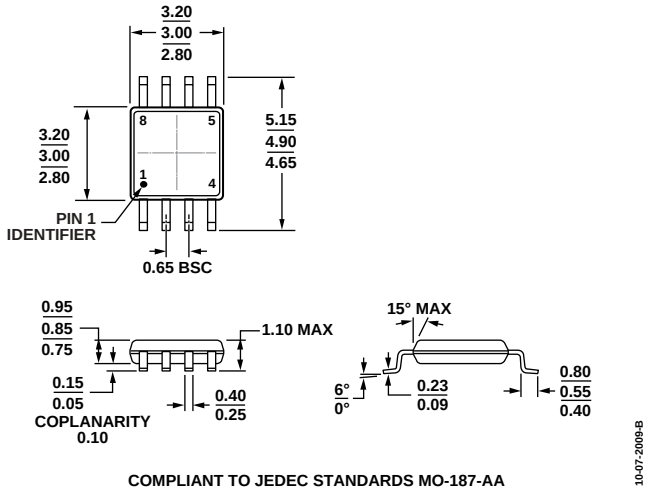
Keeping supply traces short and properly bypassing the power supplies minimizes power supply disturbances caused by output current variation, such as when driving an ac signal into a heavy load. Connect bypass capacitors as closely as possible to the device supply pins. Stray capacitances are a concern at the outputs and the inputs of the amplifier. It is recommended that signal traces be kept at least 5 mm from supply lines to minimize coupling.

A variation in temperature across the PCB can cause a mismatch in the Seebeck voltages at solder joints and other points where dissimilar metals are in contact, resulting in thermal voltage errors. To minimize these thermocouple effects, orient resistors so heat sources warm both ends equally. Input signal paths should contain matching numbers and types of components, where possible, to match the number and type of thermocouple junctions. For example, dummy components such as zero value resistors can be used to match real resistors in the opposite input path. Place matching components in close proximity to each other and orient them in the same manner. Ensure that leads are of equal length so that thermal conduction is in equilibrium. Keep heat sources on the PCB as far away from amplifier input circuitry as is practical.

The use of a ground plane is highly recommended. A ground plane reduces EMI noise and helps to maintain a constant temperature across the circuit board.

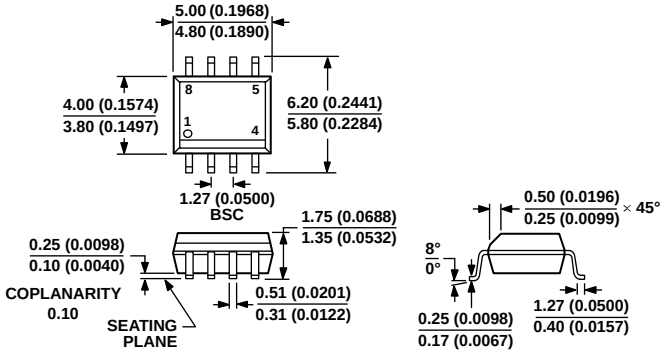
PACKAGING AND ORDERING INFORMATION

OUTLINE DIMENSIONS



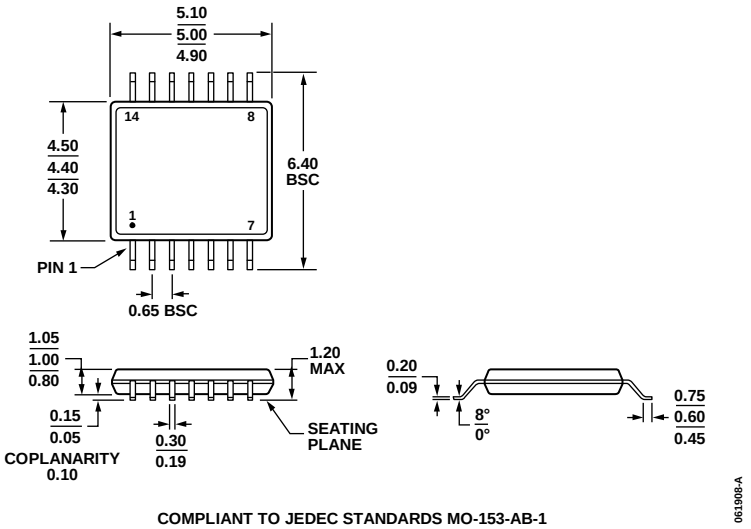
COMPLIANT TO JEDEC STANDARDS MO-187-AA

Figure 66. 8-Lead Mini Small Outline Package [MSOP]
(RM-8)
Dimensions shown in millimeters



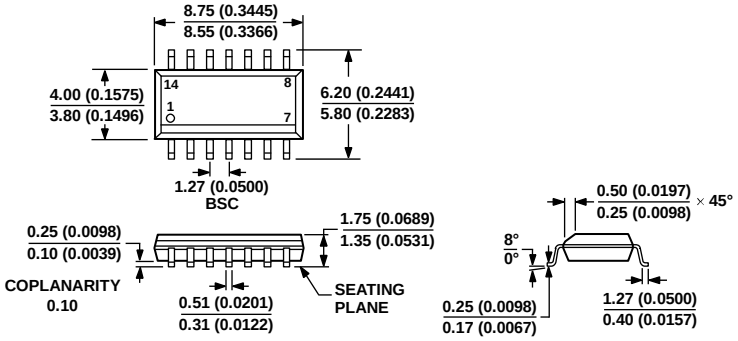
COMPLIANT TO JEDEC STANDARDS MS-012-AA
CONTROLLING DIMENSIONS ARE IN MILLIMETERS; INCH DIMENSIONS (IN PARENTHESES) ARE ROUNDED-OFF MILLIMETER EQUIVALENTS FOR REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN.

Figure 67. 8-Lead Standard Small Outline Package [SOIC_N]
Narrow Body
(R-8)
Dimensions shown in millimeters and (inches)



COMPLIANT TO JEDEC STANDARDS MO-153-AB-1

Figure 68. 14-Lead Thin Shrink Small Outline Package [TSSOP]
(RU-14)
Dimensions shown in millimeters



COMPLIANT TO JEDEC STANDARDS MS-012-AB
CONTROLLING DIMENSIONS ARE IN MILLIMETERS; INCH DIMENSIONS (IN PARENTHESES) ARE ROUNDED-OFF MILLIMETER EQUIVALENTS FOR REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN.

Figure 69. 14-Lead Standard Small Outline Package [SOIC_N]
Narrow Body
(R-14)
Dimensions shown in millimeters and (inches)

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Package Option	Branding
ADA4077-2ARMZ	−40°C to +125°C	8-Lead Mini Small Outline Package [MSOP]	RM-8	A2X
ADA4077-2ARMZ-R7	−40°C to +125°C	8-Lead Mini Small Outline Package [MSOP]	RM-8	A2X
ADA4077-2ARMZ-RL	−40°C to +125°C	8-Lead Mini Small Outline Package [MSOP]	RM-8	A2X
ADA4077-2ARZ	−40°C to +125°C	8-Lead Standard Small Outline Package [SOIC_N]	R-8	
ADA4077-2ARZ-R7	−40°C to +125°C	8-Lead Standard Small Outline Package [SOIC_N]	R-8	
ADA4077-2ARZ-RL	−40°C to +125°C	8-Lead Standard Small Outline Package [SOIC_N]	R-8	
ADA4077-2BRZ	−40°C to +125°C	8-Lead Standard Small Outline Package [SOIC_N]	R-8	
ADA4077-2BRZ-R7	−40°C to +125°C	8-Lead Standard Small Outline Package [SOIC_N]	R-8	
ADA4077-2BRZ-RL	−40°C to +125°C	8-Lead Standard Small Outline Package [SOIC_N]	R-8	
ADA4077-4ARUZ	−40°C to +125°C	14-Lead Thin Shrink Small Outline Package [TSSOP]	RU-14	
ADA4077-4ARUZ-R7	−40°C to +125°C	14-Lead Thin Shrink Small Outline Package [TSSOP]	RU-14	
ADA4077-4ARUZ-RL	−40°C to +125°C	14-Lead Thin Shrink Small Outline Package [TSSOP]	RU-14	
ADA4077-4ARZ	−40°C to +125°C	14-Lead Standard Small Outline Package [SOIC_N]	R-14	
ADA4077-4ARZ-R7	−40°C to +125°C	14-Lead Standard Small Outline Package [SOIC_N]	R-14	
ADA4077-4ARZ-RL	−40°C to +125°C	14-Lead Standard Small Outline Package [SOIC_N]	R-14	

[1] Z = RoHS Compliant Part.

NOTES

D10238-0-10/13(A)