

FEATURES

Latch-up immune under all circumstances
 Human body model (HBM) ESD rating: 8 kV
 Low on resistance: 13.5 Ω
 ± 9 V to ± 22 V dual-supply operation
 9 V to 40 V single-supply operation
 48 V supply maximum ratings
 Fully specified at ± 15 V, ± 20 V, +12 V, and +36 V
 V_{DD} to V_{SS} analog signal range

APPLICATIONS

High voltage signal routing
 Automatic test equipment
 Analog front-end circuits
 Precision data acquisition
 Industrial instrumentation
 Amplifier gain select
 Relay replacement

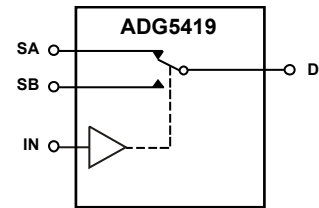
GENERAL DESCRIPTION

The **ADG5419** is a monolithic industrial, complementary metal oxide semiconductor (CMOS) analog switch containing a latch-up immune single-pole/double-throw (SPDT) switch.

Each switch conducts equally well in both directions when on, and each switch has an input signal range that extends to the power supplies. In the off condition, signal levels up to the supplies are blocked. The **ADG5419** exhibits break-before-make switching action for use in multiplexer applications.

The ultralow on resistance and on-resistance flatness of these switches make them ideal solutions for data acquisition and gain switching applications where low distortion is critical. The latch-up immune construction and high ESD rating make these switches more robust in harsh environments.

FUNCTIONAL BLOCK DIAGRAM



SWITCHES SHOWN FOR A LOGIC 0 INPUT.

Figure 1.

11370-001

PRODUCT HIGHLIGHTS

1. Trench isolation guards against latch-up. A dielectric trench separates the P channel and N channel transistors, thereby preventing latch-up even under severe overvoltage conditions.
2. Low R_{ON} of 13.5 Ω .
3. Dual-supply operation. For applications where the analog signal is bipolar, the **ADG5419** can be operated from dual supplies up to ± 22 V.
4. Single-supply operation. For applications where the analog signal is unipolar, the **ADG5419** can be operated from a single-rail power supply up to 40 V.
5. 3 V logic compatible digital inputs: $V_{INH} = 2.0$ V, $V_{INL} = 0.8$ V.
6. No V_L logic power supply required.
7. Available in 8-lead MSOP package.

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REVISION HISTORY

9/13—Revision 0: Initial Version

SPECIFICATIONS

±15 V DUAL SUPPLY

$V_{DD} = +15\text{ V} \pm 10\%$, $V_{SS} = -15\text{ V} \pm 10\%$, $GND = 0\text{ V}$, unless otherwise noted.

Table 1.

Parameter	25°C	-40°C to +85°C	-40°C to +125°C	Unit	Test Conditions/Comments
ANALOG SWITCH					
Analog Signal Range			V_{DD} to V_{SS}	V	
On Resistance, R_{ON}	13.5			Ω typ	$V_S = \pm 10\text{ V}$, $I_S = -10\text{ mA}$; see Figure 22
	15	19	23	Ω max	$V_{DD} = +13.5\text{ V}$, $V_{SS} = -13.5\text{ V}$
On-Resistance Match Between Channels, ΔR_{ON}	0.1			Ω typ	$V_S = \pm 10\text{ V}$, $I_S = -10\text{ mA}$
	0.8	1.3	1.4	Ω max	
On-Resistance Flatness, $R_{FLAT(ON)}$	1.8			Ω typ	$V_S = \pm 10\text{ V}$, $I_S = -10\text{ mA}$
	2.2	2.7	3.1	Ω max	
LEAKAGE CURRENTS					
Source Off Leakage, I_S (Off)	± 0.1			nA typ	$V_{DD} = +16.5\text{ V}$, $V_{SS} = -16.5\text{ V}$
	± 0.25	± 1	± 10	nA max	$V_S = \pm 10\text{ V}$, $V_D = \mp 10\text{ V}$; see Figure 21
Channel On Leakage, I_D (On), I_S (On)	± 0.1			nA typ	$V_S = V_D = \pm 10\text{ V}$; see Figure 21
	± 0.4	± 4	± 10	nA max	
DIGITAL INPUTS					
Input High Voltage, V_{INH}			2.0	V min	
Input Low Voltage, V_{INL}			0.8	V max	
Input Current, I_{INL} or I_{INH}	0.002			μA typ	$V_{IN} = V_{GND}$ or V_{DD}
			± 0.1	μA max	
Digital Input Capacitance, C_{IN}	6			pF typ	
DYNAMIC CHARACTERISTICS¹					
Transition Time, $t_{TRANSITION}$	217			ns typ	$R_L = 300\ \Omega$, $C_L = 35\text{ pF}$
	260	310	336	ns max	$V_S = 10\text{ V}$; see Figure 27
Break-Before-Make Time Delay, t_D	86			ns typ	$R_L = 300\ \Omega$, $C_L = 35\text{ pF}$
			45	ns min	$V_S = 10\text{ V}$; see Figure 28
Charge Injection, Q_{INJ}	130			pC typ	$V_S = 0\text{ V}$, $R_S = 0\ \Omega$, $C_L = 1\text{ nF}$; see Figure 29
Off Isolation	-60			dB typ	$R_L = 50\ \Omega$, $C_L = 5\text{ pF}$, $f = 1\text{ MHz}$; see Figure 24
Channel-to-Channel Crosstalk	-80			dB typ	$R_L = 50\ \Omega$, $C_L = 5\text{ pF}$, $f = 1\text{ MHz}$; see Figure 23
Total Harmonic Distortion + Noise	0.01			% typ	$R_L = 1\text{ k}\Omega$, 15 V p-p , $f = 20\text{ Hz to }20\text{ kHz}$; see Figure 25
-3 dB Bandwidth	190			MHz typ	$R_L = 50\ \Omega$, $C_L = 5\text{ pF}$; see Figure 26
Insertion Loss	-0.8			dB typ	$R_L = 50\ \Omega$, $C_L = 5\text{ pF}$, $f = 1\text{ MHz}$; see Figure 26
C_S (Off)	12			pF typ	$V_S = 0\text{ V}$, $f = 1\text{ MHz}$
C_D (On), C_S (On)	55			pF typ	$V_S = 0\text{ V}$, $f = 1\text{ MHz}$
POWER REQUIREMENTS					
I_{DD}	45			μA typ	$V_{DD} = +16.5\text{ V}$, $V_{SS} = -16.5\text{ V}$
	55		70	μA max	Digital inputs = 0 V or V_{DD}
I_{SS}	0.001			μA typ	Digital inputs = 0 V or V_{DD}
			1	μA max	
V_{DD}/V_{SS}			$\pm 9/\pm 22$	V min/V max	$GND = 0\text{ V}$

¹ Guaranteed by design; not subject to production test.

±20 V DUAL SUPPLY

$V_{DD} = +20\text{ V} \pm 10\%$, $V_{SS} = -20\text{ V} \pm 10\%$, GND = 0 V, unless otherwise noted.

Table 2.

Parameter	25°C	-40°C to +85°C	-40°C to +125°C	Unit	Test Conditions/Comments
ANALOG SWITCH					
Analog Signal Range			V_{DD} to V_{SS}	V	
On Resistance, R_{ON}	12.5			Ω typ	$V_S = \pm 15\text{ V}$, $I_S = -10\text{ mA}$; see Figure 22
	14	18	22	Ω max	$V_{DD} = +18\text{ V}$, $V_{SS} = -18\text{ V}$
On-Resistance Match Between Channels, ΔR_{ON}	0.1			Ω typ	$V_S = \pm 15\text{ V}$, $I_S = -10\text{ mA}$
	0.8	1.3	1.4	Ω max	
On-Resistance Flatness, $R_{FLAT(ON)}$	2.3			Ω typ	$V_S = \pm 15\text{ V}$, $I_S = -10\text{ mA}$
	2.7	3.3	3.7	Ω max	
LEAKAGE CURRENTS					
Source Off Leakage, I_S (Off)	± 0.1			nA typ	$V_{DD} = +22\text{ V}$, $V_{SS} = -22\text{ V}$
	± 0.25	± 1	± 10	nA max	$V_S = \pm 15\text{ V}$, $V_D = \mp 15\text{ V}$; see Figure 21
Channel On Leakage, I_D (On), I_S (On)	± 0.1			nA typ	$V_S = V_D = \pm 15\text{ V}$; see Figure 21
	± 0.4	± 4	± 10	nA max	
DIGITAL INPUTS					
Input High Voltage, V_{INH}			2.0	V min	
Input Low Voltage, V_{INL}			0.8	V max	
Input Current, I_{INL} or I_{INH}	0.002			μA typ	$V_{IN} = V_{GND}$ or V_{DD}
			± 0.1	μA max	
Digital Input Capacitance, C_{IN}	6			pF typ	
DYNAMIC CHARACTERISTICS¹					
Transition Time, $t_{TRANSITION}$	200			ns typ	$R_L = 300\ \Omega$, $C_L = 35\text{ pF}$
	235	279	294	ns max	$V_S = 10\text{ V}$; see Figure 27
Break-Before-Make Time Delay, t_D	77			ns typ	$R_L = 300\ \Omega$, $C_L = 35\text{ pF}$
			46	ns min	$V_S = 10\text{ V}$; see Figure 28
Charge Injection, Q_{INJ}	160			pC typ	$V_S = 0\text{ V}$, $R_S = 0\ \Omega$, $C_L = 1\text{ nF}$; see Figure 29
Off Isolation	-60			dB typ	$R_L = 50\ \Omega$, $C_L = 5\text{ pF}$, $f = 1\text{ MHz}$; see Figure 24
Channel-to-Channel Crosstalk	-80			dB typ	$R_L = 50\ \Omega$, $C_L = 5\text{ pF}$, $f = 1\text{ MHz}$; see Figure 23
Total Harmonic Distortion + Noise	0.01			% typ	$R_L = 1\text{ k}\Omega$, 20 V p-p, $f = 20\text{ Hz}$ to 20 kHz; see Figure 25
-3 dB Bandwidth	190			MHz typ	$R_L = 50\ \Omega$, $C_L = 5\text{ pF}$; see Figure 26
Insertion Loss	-0.7			dB typ	$R_L = 50\ \Omega$, $C_L = 5\text{ pF}$, $f = 1\text{ MHz}$; see Figure 26
C_S (Off)	11			pF typ	$V_S = 0\text{ V}$, $f = 1\text{ MHz}$
C_D (On), C_S (On)	55			pF typ	$V_S = 0\text{ V}$, $f = 1\text{ MHz}$
POWER REQUIREMENTS					
I_{DD}	50			μA typ	$V_{DD} = +22\text{ V}$, $V_{SS} = -22\text{ V}$
	70		110	μA max	Digital inputs = 0 V or V_{DD}
I_{SS}	0.001			μA typ	Digital inputs = 0 V or V_{DD}
			1	μA max	
V_{DD}/V_{SS}			$\pm 9/\pm 22$	V min/V max	GND = 0 V

¹ Guaranteed by design; not subject to production test.

12 V SINGLE SUPPLY

$V_{DD} = 12\text{ V} \pm 10\%$, $V_{SS} = 0\text{ V}$, $GND = 0\text{ V}$, unless otherwise noted.

Table 3.

Parameter	25°C	-40°C to +85°C	-40°C to +125°C	Unit	Test Conditions/Comments
ANALOG SWITCH					
Analog Signal Range			0 V to V_{DD}	V	
On Resistance, R_{ON}	26			Ω typ	$V_S = 0\text{ V to }10\text{ V}$, $I_S = -10\text{ mA}$; see Figure 22
	30	38	44	Ω max	$V_{DD} = 10.8\text{ V}$, $V_{SS} = 0\text{ V}$
On-Resistance Match Between Channels, ΔR_{ON}	0.1			Ω typ	$V_S = 0\text{ V to }10\text{ V}$, $I_S = -10\text{ mA}$
	1	1.5	1.6	Ω max	
On-Resistance Flatness, $R_{FLAT(ON)}$	5.5			Ω typ	$V_S = 0\text{ V to }10\text{ V}$, $I_S = -10\text{ mA}$
	6.8	8.3	12.3	Ω max	
LEAKAGE CURRENTS					
Source Off Leakage, I_S (Off)	± 0.1			nA typ	$V_{DD} = +13.2\text{ V}$, $V_{SS} = 0\text{ V}$ $V_S = 1\text{ V to }10\text{ V}$, $V_D = 10\text{ V to }1\text{ V}$; see Figure 21
	± 0.25	± 1	± 10	nA max	
Channel On Leakage, I_D (On), I_S (On)	± 0.1			nA typ	$V_S = V_D = 1\text{ V to }10\text{ V}$; see Figure 21
	± 0.4	± 4	± 10	nA max	
DIGITAL INPUTS					
Input High Voltage, V_{INH}			2.0	V min	
Input Low Voltage, V_{INL}			0.8	V max	
Input Current, I_{INL} or I_{INH}	0.002			μA typ	$V_{IN} = V_{GND}$ or V_{DD}
			± 0.1	μA max	
Digital Input Capacitance, C_{IN}	6			pF typ	
DYNAMIC CHARACTERISTICS¹					
Transition Time, $t_{TRANSITION}$	333			ns typ	$R_L = 300\ \Omega$, $C_L = 35\text{ pF}$
	414	508	567	ns max	$V_S = 8\text{ V}$; see Figure 27
Break-Before-Make Time Delay, t_D	176			ns typ	$R_L = 300\ \Omega$, $C_L = 35\text{ pF}$
			97	ns min	$V_S = 8\text{ V}$; see Figure 28
Charge Injection, Q_{INJ}	55			pC typ	$V_S = 6\text{ V}$, $R_S = 0\ \Omega$, $C_L = 1\text{ nF}$; see Figure 29
Off Isolation	-60			dB typ	$R_L = 50\ \Omega$, $C_L = 5\text{ pF}$, $f = 1\text{ MHz}$; see Figure 24
Channel-to-Channel Crosstalk	-80			dB typ	$R_L = 50\ \Omega$, $C_L = 5\text{ pF}$, $f = 1\text{ MHz}$; see Figure 23
Total Harmonic Distortion + Noise	0.03			% typ	$R_L = 1\text{ k}\Omega$, 6 V p-p, $f = 20\text{ Hz to }20\text{ kHz}$; see Figure 25
-3 dB Bandwidth	170			MHz typ	$R_L = 50\ \Omega$, $C_L = 5\text{ pF}$; see Figure 26
Insertion Loss	-1.7			dB typ	$R_L = 50\ \Omega$, $C_L = 5\text{ pF}$, $f = 1\text{ MHz}$; see Figure 26
C_S (Off)	15			pF typ	$V_S = 6\text{ V}$, $f = 1\text{ MHz}$
C_D (On), C_S (On)	50			pF typ	$V_S = 6\text{ V}$, $f = 1\text{ MHz}$
POWER REQUIREMENTS					
I_{DD}	40			μA typ	$V_{DD} = 13.2\text{ V}$
	50		65	μA max	Digital inputs = 0 V or V_{DD}
V_{DD}			9/40	V min/V max	$GND = 0\text{ V}$, $V_{SS} = 0\text{ V}$

¹ Guaranteed by design; not subject to production test.

36 V SINGLE SUPPLY

$V_{DD} = 36\text{ V} \pm 10\%$, $V_{SS} = 0\text{ V}$, $GND = 0\text{ V}$, unless otherwise noted.

Table 4.

Parameter	25°C	-40°C to +85°C	-40°C to +125°C	Unit	Test Conditions/Comments
ANALOG SWITCH					
Analog Signal Range			0 V to V_{DD}	V	
On Resistance, R_{ON}	14.5			Ω typ	$V_S = 0\text{ V to }30\text{ V}$, $I_S = -10\text{ mA}$; see Figure 22
On-Resistance Match Between Channels, ΔR_{ON}	16 0.1	20	24	Ω max Ω typ	$V_{DD} = 32.4\text{ V}$, $V_{SS} = 0\text{ V}$ $V_S = 0\text{ V to }30\text{ V}$, $I_S = -10\text{ mA}$
On-Resistance Flatness, $R_{FLAT(ON)}$	0.8 3.5 4.3	1.3	1.4	Ω max Ω typ Ω max	$V_S = 0\text{ V to }30\text{ V}$, $I_S = -10\text{ mA}$
LEAKAGE CURRENTS					
Source Off Leakage, I_S (Off)	± 0.1			nA typ	$V_{DD} = 39.6\text{ V}$, $V_{SS} = 0\text{ V}$ $V_S = 1\text{ V to }30\text{ V}$, $V_D = 30\text{ V to }1\text{ V}$; see Figure 21
Channel On Leakage, I_D (On), I_S (On)	± 0.25 ± 0.1	± 1	± 10	nA max nA typ	$V_S = V_D = 1\text{ V to }30\text{ V}$; see Figure 21
	± 0.4	± 4	± 10	nA max	
DIGITAL INPUTS					
Input High Voltage, V_{INH}			2.0	V min	
Input Low Voltage, V_{INL}			0.8	V max	
Input Current, I_{INL} or I_{INH}	0.002			μA typ μA max	$V_{IN} = V_{GND}$ or V_{DD}
Digital Input Capacitance, C_{IN}	6			pF typ	
DYNAMIC CHARACTERISTICS¹					
Transition Time, $t_{TRANSITION}$	216 250	286	310	ns typ ns max	$R_L = 300\ \Omega$, $C_L = 35\text{ pF}$ $V_S = 18\text{ V}$; see Figure 27
Break-Before-Make Time Delay, t_D	80		47	ns typ ns min	$R_L = 300\ \Omega$, $C_L = 35\text{ pF}$ $V_S = 18\text{ V}$; see Figure 28
Charge Injection, Q_{INJ}	135			pC typ	$V_S = 18\text{ V}$, $R_S = 0\ \Omega$, $C_L = 1\text{ nF}$; see Figure 29
Off Isolation	-60			dB typ	$R_L = 50\ \Omega$, $C_L = 5\text{ pF}$, $f = 1\text{ MHz}$; see Figure 24
Channel-to-Channel Crosstalk	-80			dB typ	$R_L = 50\ \Omega$, $C_L = 5\text{ pF}$, $f = 1\text{ MHz}$; see Figure 23
Total Harmonic Distortion + Noise	0.01			% typ	$R_L = 1\text{ k}\Omega$, 18 V p-p , $f = 20\text{ Hz to }20\text{ kHz}$; see Figure 25
-3 dB Bandwidth	170			MHz typ	$R_L = 50\ \Omega$, $C_L = 5\text{ pF}$; see Figure 26
Insertion Loss	-1			dB typ	$R_L = 50\ \Omega$, $C_L = 5\text{ pF}$, $f = 1\text{ MHz}$; see Figure 26
C_S (Off)	14			pF typ	$V_S = 18\text{ V}$, $f = 1\text{ MHz}$
C_D (On), C_S (On)	50			pF typ	$V_S = 18\text{ V}$, $f = 1\text{ MHz}$
POWER REQUIREMENTS					
I_{DD}	80 100		130	μA typ μA max	$V_{DD} = 39.6\text{ V}$ Digital inputs = 0 V or V_{DD}
V_{DD}			9/40	V min/V max	$GND = 0\text{ V}$, $V_{SS} = 0\text{ V}$

¹ Guaranteed by design; not subject to production test.

CONTINUOUS CURRENT PER CHANNEL, Sx OR D

Table 5.

Parameter	25°C	85°C	125°C	Unit	Test Conditions/Comments
CONTINUOUS CURRENT, Sx OR D					MSOP ($\theta_{JA} = 133.1^{\circ}\text{C/W}$)
$V_{DD} = +15\text{ V}, V_{SS} = -15\text{ V}$	113	73	46	mA maximum	
$V_{DD} = +20\text{ V}, V_{SS} = -20\text{ V}$	118	76	47	mA maximum	
$V_{DD} = 12\text{ V}, V_{SS} = 0\text{ V}$	90	60	41	mA maximum	
$V_{DD} = 36\text{ V}, V_{SS} = 0\text{ V}$	116	74	46	mA maximum	

ABSOLUTE MAXIMUM RATINGS

$T_A = 25^\circ\text{C}$, unless otherwise noted.

Table 6.

Parameter	Rating
V_{DD} to V_{SS}	48 V
V_{DD} to GND	-0.3 V to +48 V
V_{SS} to GND	+0.3 V to -48 V
Analog Inputs ¹	$V_{SS} - 0.3\text{ V}$ to $V_{DD} + 0.3\text{ V}$ or 30 mA, whichever occurs first
Digital Inputs ¹	$V_{SS} - 0.3\text{ V}$ to $V_{DD} + 0.3\text{ V}$ or 30 mA, whichever occurs first
Peak Current, Sx or D Pins	410 mA (pulsed at 1 ms, 10% duty cycle maximum)
Continuous Current, Sx or D ²	Data + 15%
Temperature Range	
Operating	-40°C to +125°C
Storage	-65°C to +150°C
Junction Temperature	150°C
Thermal Impedance, θ_{JA}	
8-Lead MSOP (4-Layer Board)	133.1°C/W
Reflow Soldering Peak Temperature, Pb Free	As per JEDEC J-STD-020
Human Body Model (HBM) ESD	8 kV

¹ Overvoltages at the IN, Sx, and D pins are clamped by internal diodes. Limit current to the maximum ratings given.

² See Table 5.

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Only one absolute maximum rating can be applied at any one time.

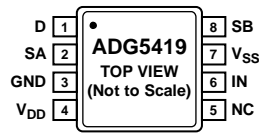
ESD CAUTION



ESD (electrostatic discharge) sensitive device.

Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS



NOTES
1. NC = NO CONNECT. NOT INTERNALLY CONNECTED.

113779-012

Figure 2. Pin Configuration

Table 7. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	D	Drain Terminal. This pin can be an input or output.
2	SA	Source Terminal. This pin can be an input or output.
3	GND	Ground (0 V) Reference.
4	V _{DD}	Most Positive Power Supply Potential.
5	NC	No Connect. Not internally connected.
6	IN	Logic Control Input.
7	V _{SS}	Most Negative Power Supply Potential.
8	SB	Source Terminal. This pin can be an input or output.

Table 8. Truth Table

IN	Switch A	Switch B
0	On	Off
1	Off	On

TYPICAL PERFORMANCE CHARACTERISTICS

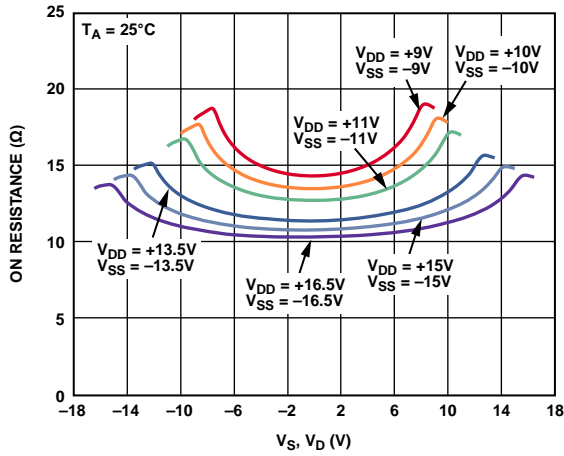


Figure 3. On Resistance as a Function of V_S, V_D (Dual Supply)

11370-003

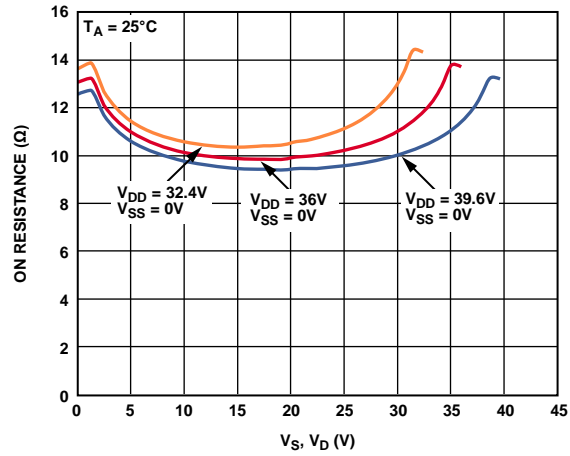


Figure 6. On Resistance as a Function of V_S, V_D (Single Supply)

11370-006

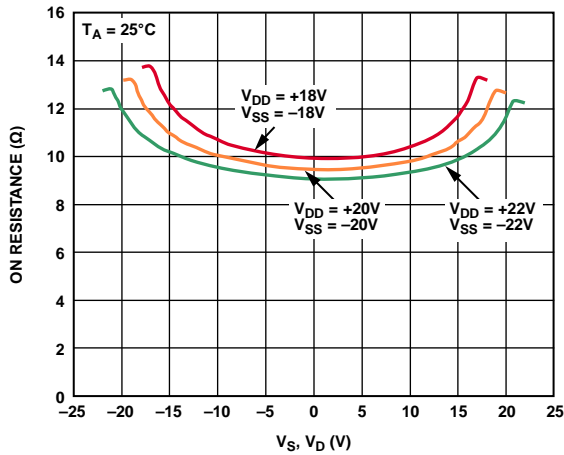


Figure 4. On Resistance as a Function of V_S, V_D (Dual Supply)

11370-004

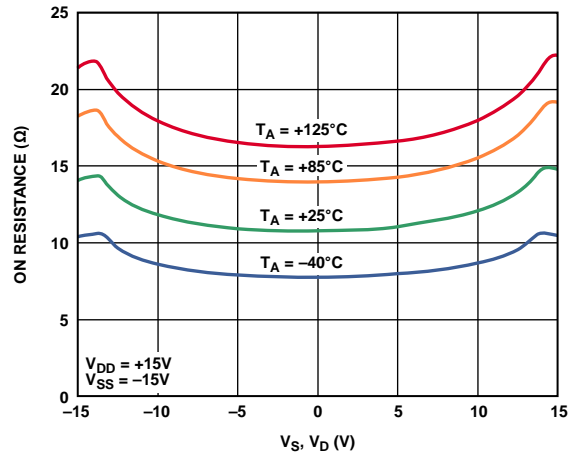


Figure 7. On Resistance as a Function of $V_S (V_D)$ for Different Temperatures, ± 15 V Dual Supply

11370-007

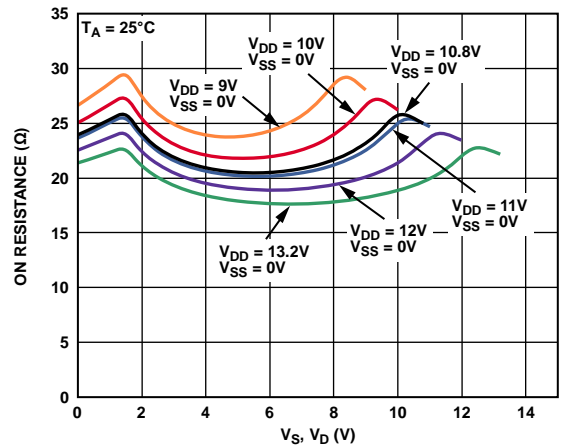


Figure 5. On Resistance as a Function of V_S, V_D (Single Supply)

11370-005

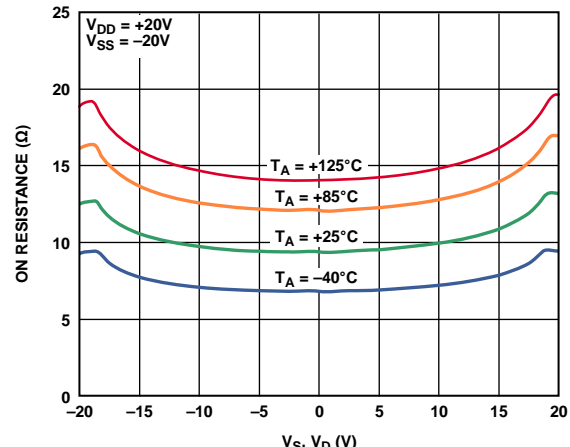


Figure 8. On Resistance as a Function of $V_S (V_D)$ for Different Temperatures, ± 20 V Dual Supply

11370-008

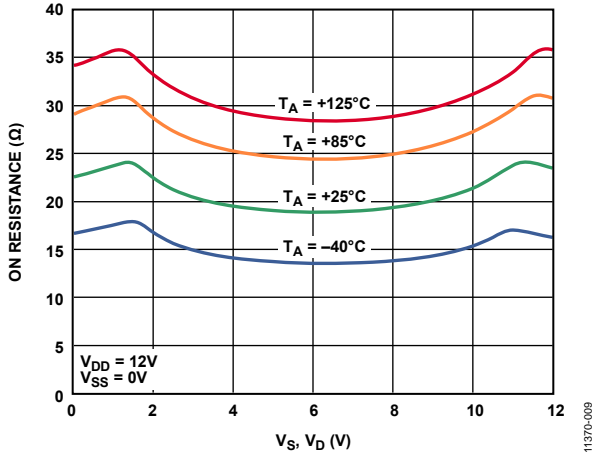


Figure 9. On Resistance as a Function of V_S (V_D) for Different Temperatures, 12 V Single Supply

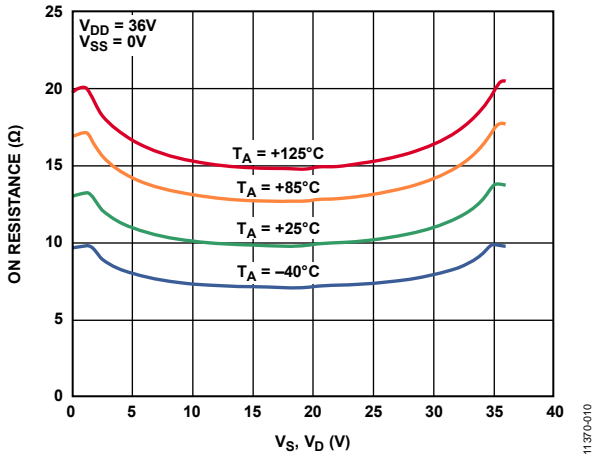


Figure 10. On Resistance as a Function of V_S (V_D) for Different Temperatures, 36 V Single Supply

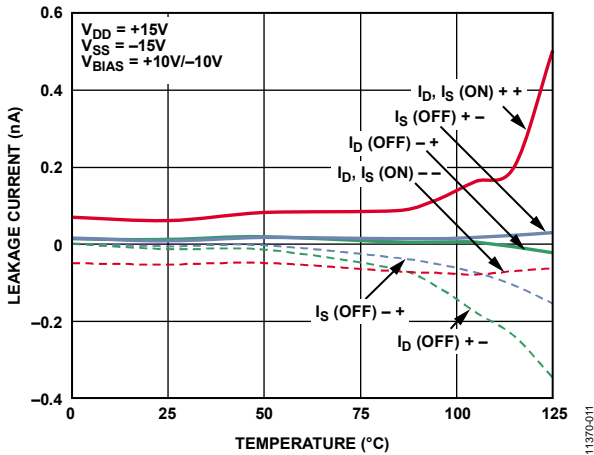


Figure 11. Leakage Currents as a Function of Temperature, ± 15 V Dual Supply

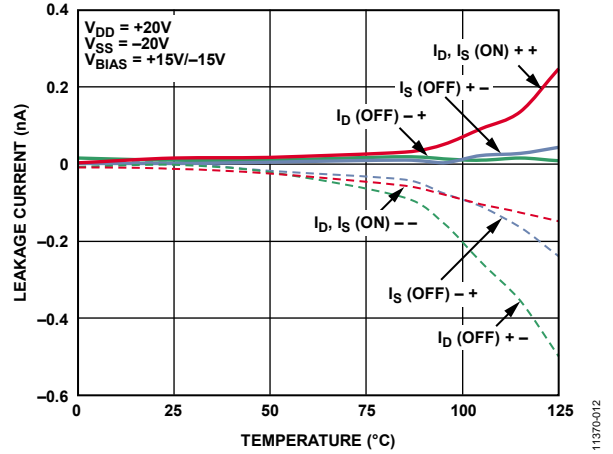


Figure 12. Leakage Currents as a Function of Temperature, ± 20 V Dual Supply

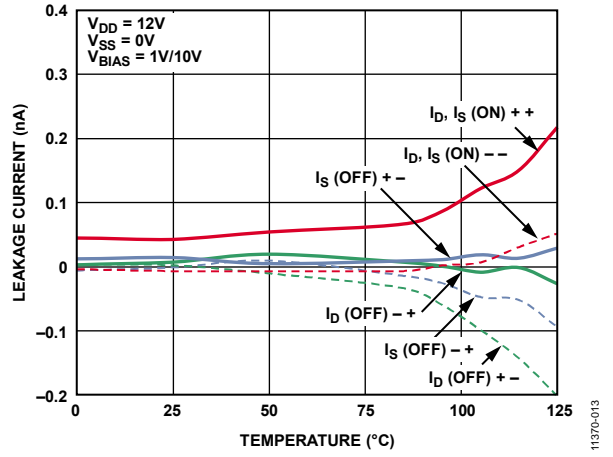


Figure 13. Leakage Currents as a Function of Temperature, 12 V Single Supply

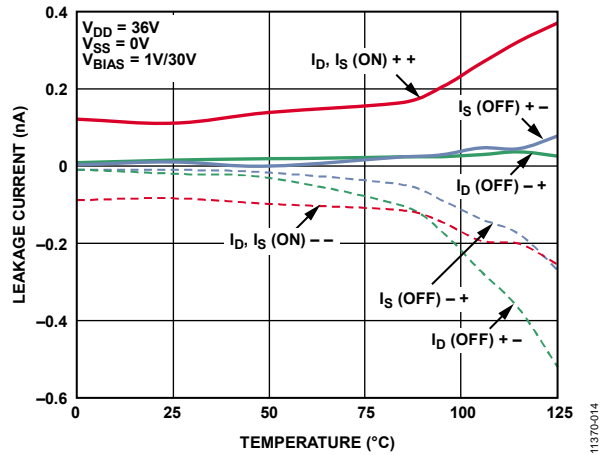


Figure 14. Leakage Currents as a Function of Temperature, 36 V Single Supply

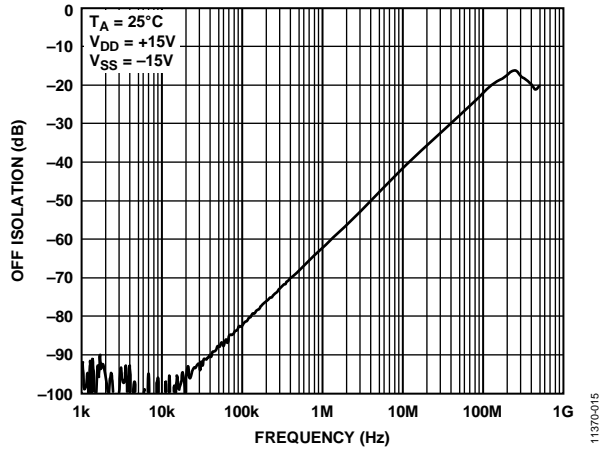


Figure 15. Off Isolation vs. Frequency

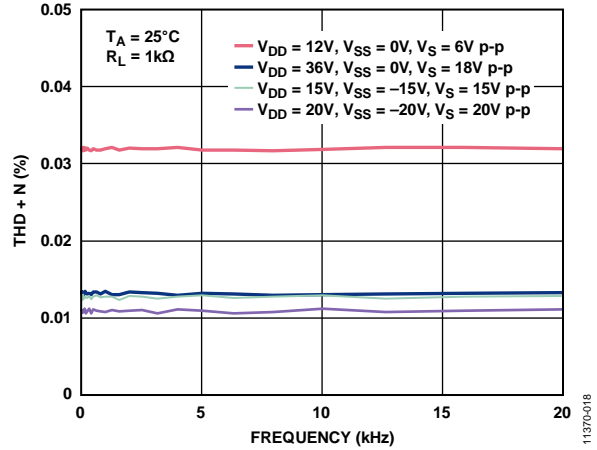


Figure 18. THD + N vs. Frequency

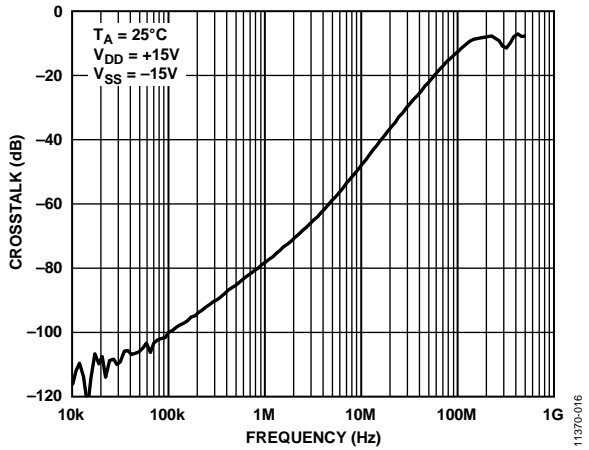


Figure 16. Crosstalk vs. Frequency

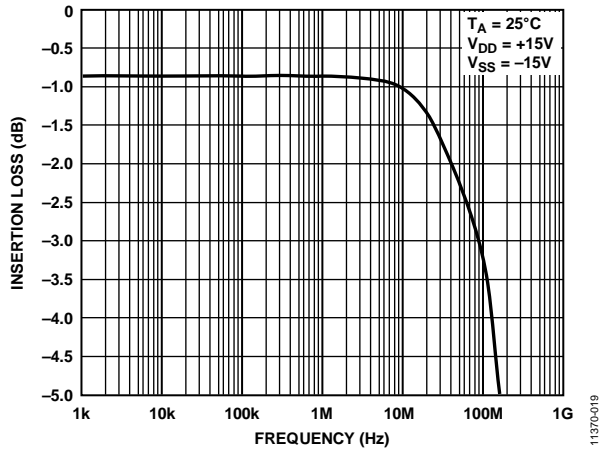


Figure 19. Bandwidth

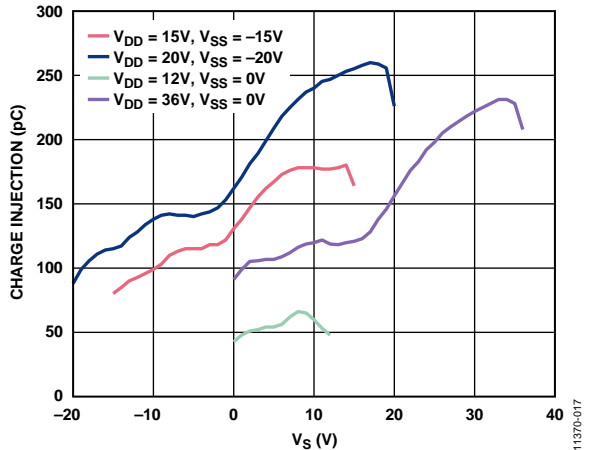


Figure 17. Charge Injection vs. Source Voltage

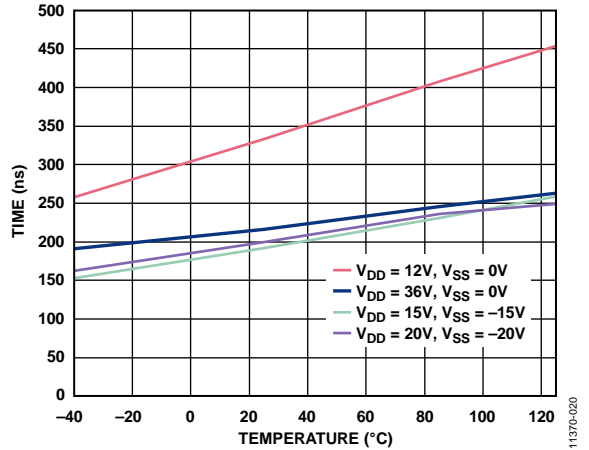


Figure 20. $t_{TRANSITION}$ Times vs. Temperature

TEST CIRCUITS

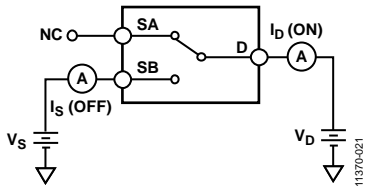


Figure 21. On and Off Leakage

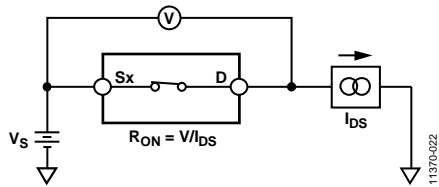


Figure 22. On Resistance

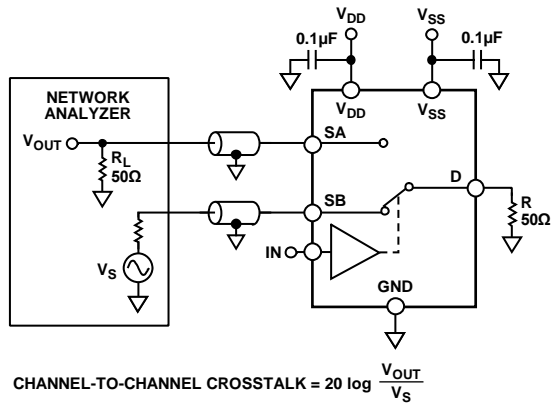


Figure 23. Channel-to-Channel Crosstalk

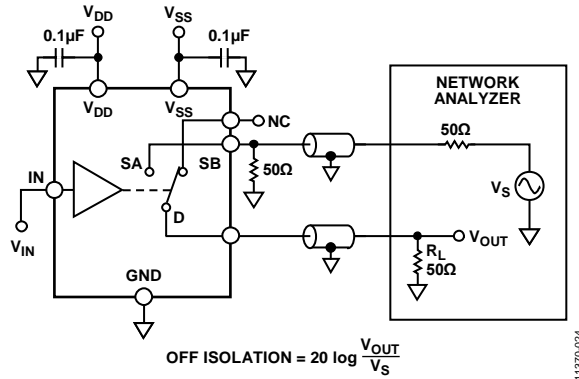


Figure 24. Off Isolation

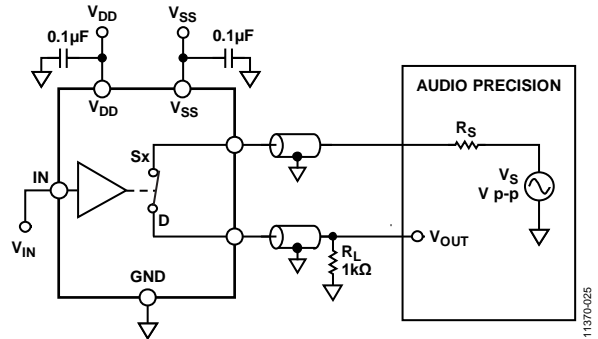


Figure 25. THD + Noise

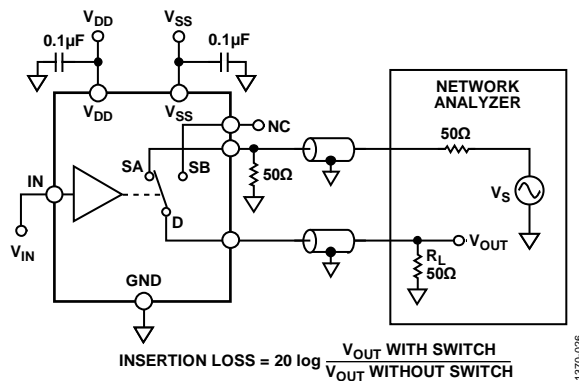


Figure 26. Bandwidth

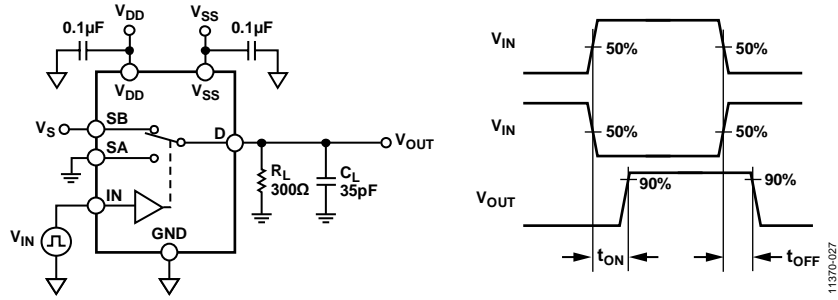


Figure 27. Switching Timing

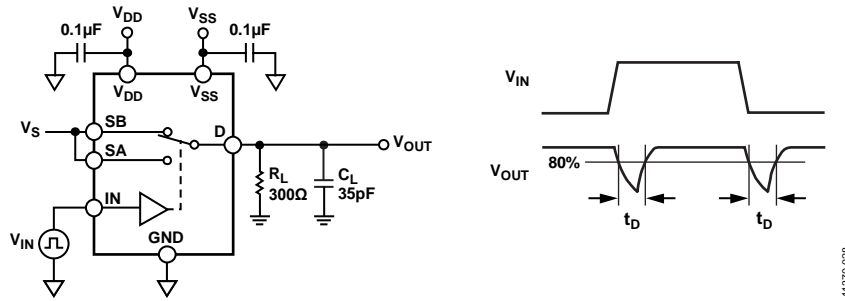


Figure 28. Break-Before-Make Delay, t_D

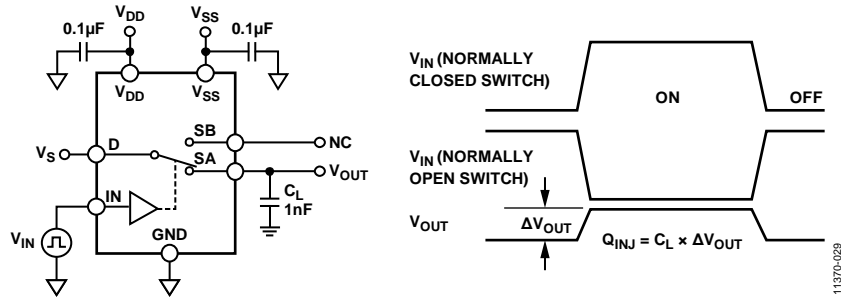


Figure 29. Charge Injection

TERMINOLOGY

I_{DD}

I_{DD} represents the positive supply current.

I_{SS}

I_{SS} represents the negative supply current.

V_D, V_S

V_D and V_S represent the analog voltage on Terminal D and Terminal S, respectively.

R_{ON}

R_{ON} is the ohmic resistance between Terminal D and Terminal S.

ΔR_{ON}

ΔR_{ON} represents the difference between the R_{ON} of any two channels.

R_{FLAT (ON)}

The difference between the maximum and minimum value of on resistance as measured over the specified analog signal range is represented by R_{FLAT (ON)}.

I_S (Off)

I_S (Off) is the source leakage current with the switch off.

I_D (On), I_S (On)

I_D (On) and I_S (On) represent the channel leakage currents with the switch on.

V_{INL}

V_{INL} is the maximum input voltage for Logic 0.

V_{INH}

V_{INH} is the minimum input voltage for Logic 1.

I_{INL}, I_{INH}

I_{INL} and I_{INH} represent the low and high input currents of the digital inputs.

C_S (Off)

C_S (Off) represents the off switch source capacitance, which is measured with reference to ground.

C_D (On), C_S (On)

C_D (On) and C_S (On) represent on switch capacitances, which are measured with reference to ground.

C_{IN}

C_{IN} represents digital input capacitance.

t_{TRANSITION}

Delay time between the 50% and 90% points of the digital inputs and the switch on condition when switching from one address state to another.

t_D

t_D represents the off time measured between the 80% point of both switches when switching from one address state to another.

Off Isolation

Off isolation is a measure of unwanted signal coupling through an off channel.

Charge Injection

Charge injection is a measure of the glitch impulse transferred from the digital input to the analog output during switching.

Crosstalk

Crosstalk is a measure of unwanted signal that is coupled through from one channel to another as a result of parasitic capacitance.

Bandwidth

Bandwidth is the frequency at which the output is attenuated by 3 dB, from its dc level.

Total Harmonic Distortion + Noise (THD + N)

The ratio of the harmonic amplitude plus noise of the signal to the fundamental is represented by THD + N.

APPLICATIONS INFORMATION

The [ADG54xx](#) family of switches and multiplexers provide a robust solution for instrumentation, industrial, aerospace, and other harsh environments that are prone to latch-up, which is an undesirable high current state that can lead to device failure and persists until the power supply is turned off. The [ADG5419](#) high voltage switch allows single-supply operation from 9 V to 40 V and dual-supply operation from ± 9 V to ± 22 V. The [ADG5419](#) (as well as other select devices within this family) achieves an 8 kV human body model ESD rating, which provides a robust solution, eliminating the need for separate protection circuitry designs in some applications.

TRENCH ISOLATION

In the [ADG5419](#), an insulating oxide layer (trench) is placed between the NMOS and the PMOS transistors of each CMOS switch. Parasitic junctions, which occur between the transistors in junction-isolated switches, are eliminated, and the result is a completely latch-up immune switch.

In junction isolation, the N and P wells of the PMOS and NMOS transistors form a diode that is reverse-biased under normal operation. However, during overvoltage conditions, this diode can become forward-biased. The two transistors form a silicon-controlled rectifier (SCR) type circuit, causing a significant amplification of the current that, in turn, leads to latch-up. With trench isolation, this diode is removed, and the result is a latch-up immune switch.

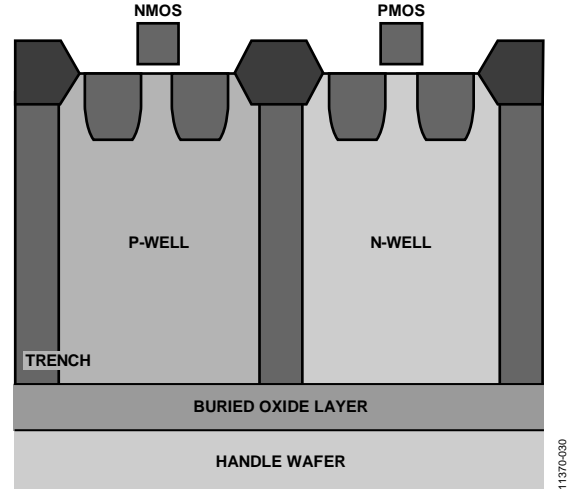
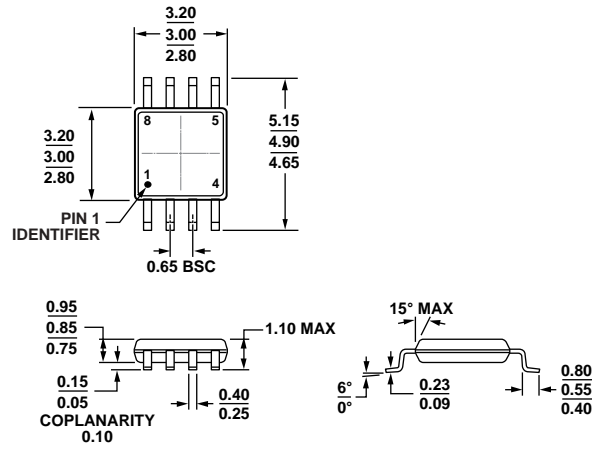


Figure 30. Trench Isolation

OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MO-187-AA

Figure 31. 8-Lead Mini Small Outline Package [MSOP] (RM-8)

Dimensions shown in millimeters

100708-B

ORDERING GUIDE

Model ¹	Temperature Range	Package Description	Package Option	Branding
ADG5419BRMZ	-40°C to +125°C	8-Lead Mini Small Outline Package [MSOP]	RM-8	S48
ADG5419BRMZ-RL7	-40°C to +125°C	8-Lead Mini Small Outline Package [MSOP]	RM-8	S48

¹ Z = RoHS Compliant Part.

NOTES

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