Quad IO-Link Master Hot Swap Controller and PHY

FEATURES

- **IO-Link™ Compatible (COM1/COM2/COM3)**
- **8V to 30V Operation**
- **Hot Swap™ Controller Protected Supply Outputs**
- **Discrete Power MOSFETs for Ruggedness and Flexibility**
- **Configurable 100mA (4-Port), 200mA (2-Port), or 400mA (1-Port) CQ Drive Capability**
- **Automatic Wake-Up Pulse Generation**
- **Automatic Cable Sensing**
- **±50V Line Protection**
- Configurable L+ Current Limit with Foldback
- Short Circuit, Input UV/OV and Thermal Protection
- Optional Interrupt and Auto-Retry after Faults
- 2.9V to 5.5V Logic Supply for Flexible Digital Interface
- No Damage or Latchup to ±8kV HBM ESD
- 38-Lead (5mm × 7mm) QFN and TSSOP Packages

APPLICATIONS

- IO-Link Masters
- Intelligent Sensors and Actuators
- Factory Automation Networks

DESCRIPTION

The LTC®2874 provides a rugged, 4-port IO-Link power and communications interface to remote devices connected by cables up to 20m in length.

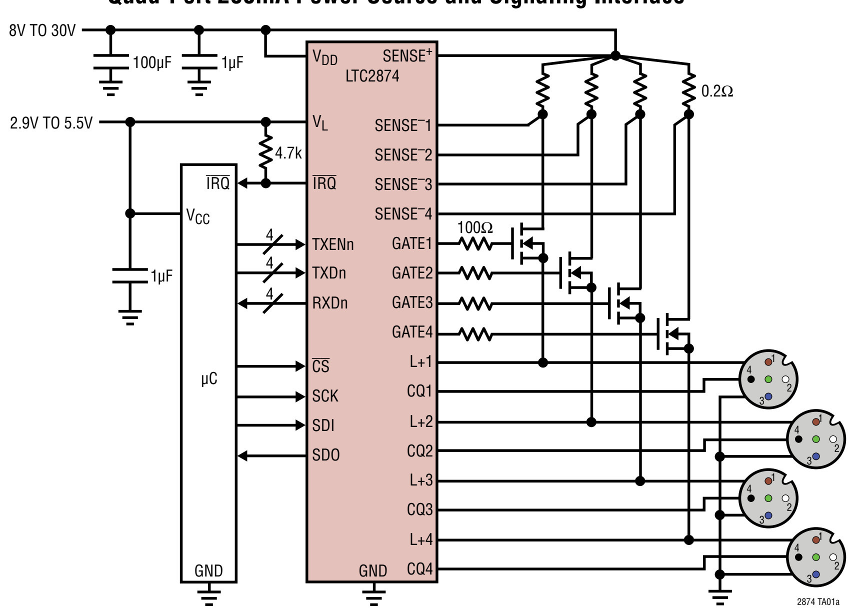
Output supply voltage and inrush current are ramped up in a controlled manner using external N-channel MOSFETs, providing improved robustness compared to fully integrated solutions.

Wake-up pulse generation, line noise suppression, connection sensing and automatic restart after fault conditions are supported, along with signaling at 4.8kb/s, 38.4kb/s, and 230.4kb/s.

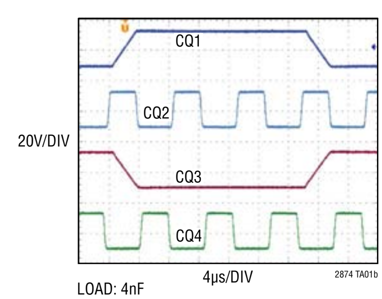
Configuration and fault reporting are exchanged using a SPI-compatible 4-wire interface that operates at clock rates up to 20MHz.

TYPICAL APPLICATION

Quad-Port 200mA Power Source and Signaling Interface



Operating Waveforms



LOAD: 4nF
CQ1, CQ3: SLEW = 0
CQ2, CQ4: SLEW = 1

ABSOLUTE MAXIMUM RATINGS

(Notes 1, 2, 3)

Input Supplies
- V_{DD} .... –0.3V to 40V
- V_L .... –0.3V to 6V

Input Voltages
- $\overline{CS}$, SCK, SDI, TXD .... –0.3V to 6V
- TXEN .... –0.3V to V_L + 0.3V
- CQ.......... V_{DD} – 50V to 50V
- GATE – L+ (Note 4) .... –0.3V to 10V
- L+ .... –6V to 50V
- $SENSE^+$, $SENSE^-$ .... V_{DD} – 2V to V_{DD} + 2V

Output Voltages
- GATE.......... –0.3V to (V_{L+}) + 15V
- $\overline{IRQ}$ .... –0.3V to 6V
- RXD, SDO .... –0.3V to V_L + 0.3V

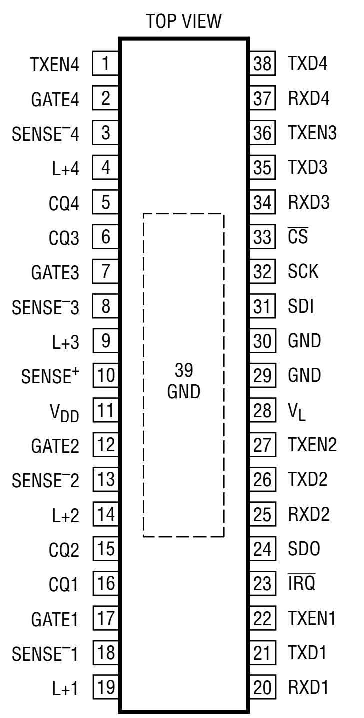
Operating Temperature Range
- LTC2874I.......... –40°C to 85°C

Maximum Junction Temperature .... 150°C

Storage Temperature Range .... –65°C to 150°C

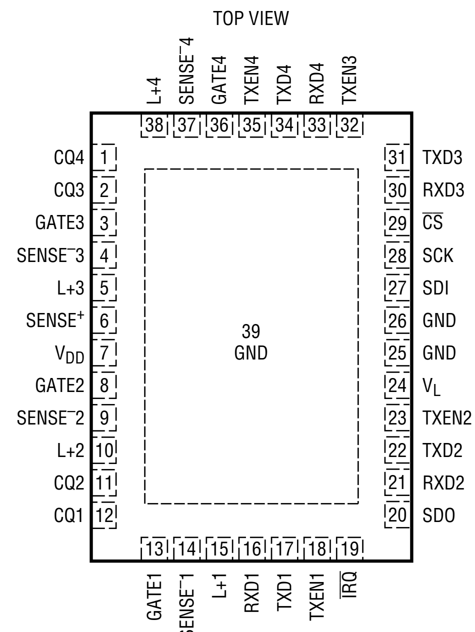
Lead Temperature (Soldering, 10 sec)
- FE Package .... 300°C

PIN CONFIGURATION



FE PACKAGE
38-LEAD PLASTIC TSSOP

T_{JMAX} = 150°C, θ_{JA} = 25°C/W (NOTE 5)
EXPOSED PAD (PIN 39) IS GND, MUST BE SOLDERED TO PCB



UHF PACKAGE
38-LEAD (5mm × 7mm) PLASTIC QFN

T_{JMAX} = 150°C, θ_{JA} = 34°C/W (NOTE 5)
EXPOSED PAD (PIN 39) IS GND, MUST BE SOLDERED TO PCB

ORDER INFORMATION

LEAD FREE FINISH	TAPE AND REEL	PART MARKING	PACKAGE DESCRIPTION	TEMPERATURE RANGE
LTC2874IFE#PBF	LTC2874IFE#TRPBF	LTC2874FE	38-Lead Plastic TSSOP	–40°C to 85°C
LTC2874IUHF#PBF	LTC2874IUHF#TRPBF	2874	38-Lead (5mm × 7mm) Plastic QFN	–40°C to 85°C

Consult LTC Marketing for parts specified with wider operating temperature ranges.
Consult LTC Marketing for information on nonstandard lead based finish parts.

For more information on lead free part marking, go to: http://www.linear.com/leadfree/
For more information on tape and reel specifications, go to: http://www.linear.com/tapeandreel/

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. Unless otherwise noted, V_{DD} = 24V, V_L = 3.3V, and registers are reset to their default states. (Note 2)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Input Supply							
V_{DD}	Input Supply Operating Range	24VMODE = 0 24VMODE = 1	● ●	8 20		30 30	V V
I_{DD}	V_{DD} Input Supply Current, All Ports Enabled	DRVEN = 0xF, ENL+ = 0xF, ILLM = 0x0	●		5	8	mA
$V_{DD(UVL)}$	UV Lockout	V_{DD} Rising	●	5.5	6	6.5	V
	UV Lockout Hysteresis				0.13		V
$V_{DD(UVTH)}$	UV Bit Threshold	V_{DD} Rising 24VMODE = 1 24VMODE = 0	 ● ●	 16.2 6.8	 16.8 7.1	 17.4 7.4	 V V
	UV Bit Threshold Hysteresis				0.2		V
$V_{DD(OVTH)}$	OV Bit Threshold	V_{DD} Rising, OV_TH = 0x1	●	31	32	33	V
	OV Bit Threshold Hysteresis				0.4		V
Logic Supply							
V_L	Logic Supply Range		●	2.9		5.5	V
I_L	V_L Logic Supply Current	Digital Inputs at 0V or V_L	●		0.1	1	mA
L+ Power Supply Output							
$V_{L+(PGTH)}$	L+ Power Good Threshold	$V_{L+(PGTH)} = V_{DD} – V(L+)$	●	1.2	1.5	1.9	V
	L+ Power Good Hysteresis				100		mV
$ΔV_{CB(TH)}$	Circuit Breaker Threshold	$ΔV_{CB(TH)}$ = V(SENSE⁺) – V(SENSE⁻) (Note 7)			$ΔV_{ACL}$ – 0.8		mV
$ΔV_{ACL}$	Analog Current Limit Voltage	$ΔV_{ACL}$ = V(SENSE⁺) – V(SENSE⁻) V(L+) = 0V, FLDBK_MODE = 1 V(L+) = V_{DD} – 1V Start-Up, 2XPTC Enabled, V(L+) > 18V (Note 7)	 ● ● 	 9.2 42 	 16.7 50 100	 24.2 58 	 mV mV mV
$t_{OC(L+)}$	L+ Pin OC Fault Filter	V(SENSE⁺) – V(SENSE⁻) = 250mV, LPTC = 0x03 (Figure 1)	●	110	122.5	135	µs
$t_{D(ACL)}$	$ΔV_{SENSE}$ to GATE Low	V(SENSE⁺) – V(SENSE⁻) = 250mV, LPTC = 0x03 (Figure 1) C_G = 0nF C_G = 10nF	 ● 		 19 24	 25 	 µs µs
	Start-Up Current Pulse Duration	2XPTC = 0x0	●	52	62	72	ms
	SENSE⁻ Pin Input Current	V(SENSE⁻) = 24V	●	0	10	25	µA

ELECTRICAL CHARACTERISTICS

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SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Gate Drive							
ΔV_{GATE}	External N-Channel Gate Drive ($V_{GATE} - V_{L+}$)	I(GATE) = –1µA V_{DD} = 17V to 30V V_{DD} = 8V	 ● ●	 10 4.5	 13	 15 15	 V V
$I_{GATE(UP)}$	GATE Pin Output Current, Sourcing	V(SENSE⁺) – V(SENSE⁻) = 0V, V(GATE) = 1V	●	–10	–14	–20	µA
$I_{GATE(DN)}$	GATE Pin Output Current, Sinking	ENL+ = 0, V(GATE) = 10V			1.2		mA
I_{GATE}(LIM)	Pull-Down Current from GATE to SOURCE During UVLO or L+ OC Timeout Event	V(SENSE⁺) – V(SENSE⁻) = 0.2V, ΔV_{GATE} = 10V			90		mA
	($V_{GATE} - V_{L+}$) for Power Good	V(L+) = 8V to 30V	●	3.0	3.8	4.5	V
CQ Line Driver							
V_{RQH}, V_{RQL}	Residual Voltage (Note 6)	Output High, I(CQ) = –100mA Output Low, I(CQ) = 100mA	● ●		1.2 1.1	1.6 1.5	V V
I_{QPKH}, I_{QPKL}	Wake-Up Request (WURQ) Current	(Figure 2)	●	±500	±700		mA
I_{QH}, I_{QL}	Current Limit	(Figure 3)	●	±110	±160	±230	mA
$t_{OC(CQ)}$	Overcurrent Timeout	C_L = 100pF, V_{DD} – CQ or CQ = 5V (Figure 3) SLEW = 0, SIO = 0 SLEW = 1, SIO = 0	 ● ●	 13 13		 24 24	 µs µs
CQ Line Receiver							
V_{THH}	Input High Threshold Voltage	24VMODE = 1 24VMODE = 0	● ●	10.5 0.5 • V_{DD}	11.9	13 0.7 • V_{DD}	V V
V_{THL}	Input Low Threshold Voltage	24VMODE = 1 24VMODE = 0	● ●	8 0.3 • V_{DD}	9.4	11.5 0.5 • V_{DD}	V V
V_{HYS}	Input Hysteresis	24VMODE = 1 24VMODE = 0	● ●	2.0 0.05 • V_{DD}	2.5	2.9 0.2 • V_{DD}	V V
	Input Resistance	V(CQ) = V_{DD} – 1V, ILLM = 0x0	●	390	510	630	kΩ
V_{OH}	Output High Voltage	I(RXD) = –100µA	●	V_L – 0.4			V
V_{OL}	Output Low Voltage	I(RXD) = 100µA	●			0.4	V
Digital I/O							
	Input Threshold Voltage	2.9V ≤ V_L ≤ 5.5V	●	0.33 • V_L		0.67 • V_L	V
	Input Leakage Current	0V ≤ V_{IN} ≤ V_L $\overline{CS}$, TXD SCK, SDI, TXEN	 ● ●	 –10 –1		 1 10	 µA µA
	Input Capacitance	(Note 7)	●			2.5	pF
$V_{OH(SDO)}$	SDO Output High Voltage	I(SDO) = –1mA	●	V_L – 0.4			V
$V_{OL(SDO)}$	SDO Output Low Voltage	I(SDO) = 1mA	●			0.4	V
$V_{OL(\overline{IRQ})}$	$\overline{IRQ}$ Open Drain Output Low Voltage	I($\overline{IRQ}$) = 3mA I($\overline{IRQ}$) = 5mA	● ●			0.4 0.7	V V
Other Pin Functions							
I_{LL}	Receive-Mode Load/Discharge Current	ILLM = 0x3, 0V ≤ V(CQ) ≤ 5V ILLM = 0x3, 5V < V(CQ) ≤ 30V ILLM = 0x2, 5V < V(CQ) ≤ 30V ILLM = 0x1, 5V < V(CQ) ≤ 30V	● ● ● ●	0 5 3.2 2.2	6.2 6.2 3.7 2.5	6.8 6.8 4.2 2.8	mA mA mA mA
	Input to GATE Off Propagation Delay	ENL+ UVLO_VDD (Note 7) or OV_VDD Event	● ●		2 10	4 15	µs µs

2874f

SWITCHING CHARACTERISTICS

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SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
	GATE Turn-On Delay		●		10	20	µs
t_{RETRY}	Auto-Retry Delay	RETRYTC = 0x5			3.9		s
	ESD Protection CQ and L+ Pins All Other Pins	Human Body Model (Note 7)			 ±8 ±6		 kV kV
Driver and Receiver							
f_{DTR}	Maximum Data Transfer Rate	C_L = 4nF SLEW = 0 SLEW = 1	 ● ●	 38.4 230.4			 kb/s kb/s
T_{BIT}	Bit Time	SLEW = 0 SLEW = 1			26.04 4.34		µs µs
C_{CQ}	CQ Pin Input Capacitance	(Note 7)				100	pF
Driver							
t_{DR}, t_{DF}	Rise or Fall Time	SLEW = 0 (Figure 4) C_L = 100pF C_L = 4nF	 ● ●		 3 3	 5.2 5.2	 µs µs
		SLEW = 1 (Figure 4) C_L = 100pF C_L = 4nF	 ● ●		 0.5 0.5	 0.869 0.869	 µs µs
t_{PHLD}, t_{PLHD}	Propagation Delay	C_L = 100pF (Figure 5) SLEW = 0 SLEW = 1	 ● ●		 4 1.3	 8 3	 µs µs
t_{SKEWD}	Skew	C_L = 100pF (Figure 5) SLEW = 0 SLEW = 1			 0.5 0.5		 µs µs
t_{ZHD}, t_{ZLD}	Enable Time	R_L = 10kΩ, C_L = 100pF, ILLM = 0x0 (Figure 6) SLEW = 0 SLEW = 1	 ● ●			 12 3	 µs µs
t_{HZD}, t_{LZD}	Disable Time	R_L = 10kΩ, C_L = 100pF, ILLM = 0x0 (Figure 6)	●			3	µs
t_{WUDLY}	Wake-Up Request (WURQ) Delay	(Figure 2)	●		7.5	20	µs
t_{WU}	WURQ Pulse Duration	(Figure 2)	●	75	80	85	µs
	WURQ Cooldown Timer		●		8.3	10	ms
Receiver							
t_H, t_L	Detection Time	(Figure 7) T_{BIT} = 208.3µs (COM1), NSF = 0x1 T_{BIT} = 26.0µs (COM2), NSF = 0x2 T_{BIT} = 4.34µs (COM3), NSF = 0x3	 ● ● ●	 1/16 1/16 1/16	 1/10 1/9 1/7		 T_{BIT} T_{BIT} T_{BIT}
t_{ND}	Noise Suppression Time	(Figure 8, Note 9) T_{BIT} = 208.3µs (COM1), NSF = 0x1 T_{BIT} = 26.0µs (COM2), NSF = 0x2 T_{BIT} = 4.34µs (COM3), NSF = 0x3	 ● ● ●		 1/10 1/9 1/7	 1/16 1/16 1/16	 T_{BIT} T_{BIT} T_{BIT}
t_{PHLR}, t_{PLHR}	Receiver Propagation Delay	NSF = 0x0, C_L = 100pF (Figure 7)	●		200	600	ns
t_{SKEWR}	Receiver Skew	NSF = 0x0, C_L = 100pF (Figure 7)			100		ns

TIMING CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_{DD} = 24V, V_L = 2.9V to 5.5V unless otherwise noted. (See Figure 9) (Note 7)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
SPI Interface							
t_{SU}	$\overline{CS}$ to SCK Set-Up Time		●	7			ns
t_{HD}	SCK Falling to $\overline{CS}$ Hold Time		●	7			ns
t_{CH}	SCK High Time		●	19			ns
t_{CL}	SCK Low Time		●	19			ns
t_{DS}	SDI Set-Up Time		●	4			ns
t_{DH}	SDI Hold Time		●	4			ns
t_{DO}	SCK Falling to SDO Valid	C(SDO) = 10pF 4.5V ≤ V_L ≤ 5.5V 2.9V ≤ V_L < 4.5V	 ● ●			 20 40	 ns ns
	SCK Frequency	50% Duty Cycle (Note 8)	●			20	MHz

Note 1. Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2. All voltages are with respect to GND. All currents into device pins are positive; all currents out of device pins are negative.

Note 3. Numerical subscripts corresponding to port number are sometimes omitted from pin names for brevity.

Note 4. An internal clamp limits each GATE pin to a minimum of 10V above its respective L+ pin. Externally driving these pins to voltages beyond the clamp may damage the device.

Note 5. This IC includes current limiting and overtemperature protection that are intended to protect the device during momentary overload conditions. Junction temperature can exceed the rated maximum during current limiting. Overtemperature protection will become active at a junction temperature greater than the rated maximum operating temperature. Continuous operation above the specified maximum operating junction temperature may impair device reliability.

Note 6. Residual voltages are defined as follows: $V_{RQH} = V_{DD} – V(CQ)$, and $V_{RQL} = V(CQ) – V(GND)$.

Note 7. Guaranteed by design and not production tested.

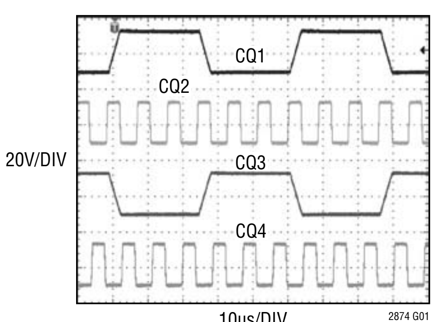
Note 8. SCK frequency is limited by SDO propagation delay as follows: $t_{SCK} \geq 2 \bullet (t_{DO} + t_s)$, where t_s is the setup time of the receiving device.

Note 9. Guaranteed by production testing of t_H and t_L.

TYPICAL PERFORMANCE CHARACTERISTICS

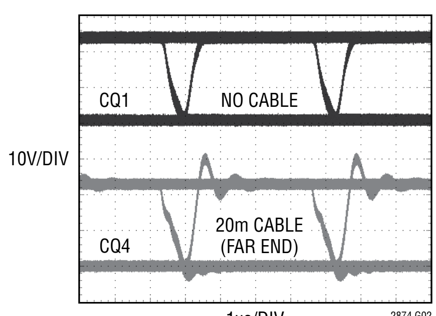
T_A = 25°C, V_{DD} = 24V, V_L = 3.3V, unless otherwise noted.

Operation at 230.4kb/s (COM3) and 38.4kb/s (COM2)



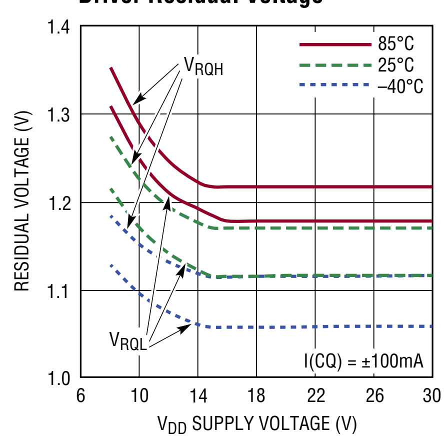
LOAD: 4nF
CQ1, CQ3: SLEW = 0
CQ2, CQ4: SLEW = 1

Driver Eye Diagram (COM3)



PRBS = $2^8 – 1$
CQ1: LOAD = 4nF
CQ4: 20m CABLE + 1nF + 300Ω
CQ2, CQ3: ASYNCHRONOUS COM3 SWITCHING
L+1 TO L+4: ENABLED AND BYPASSED AT FAR END

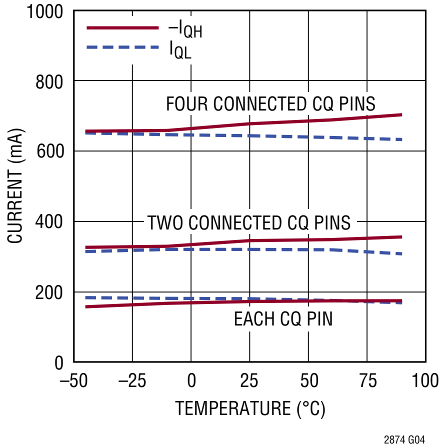
Driver Residual Voltage



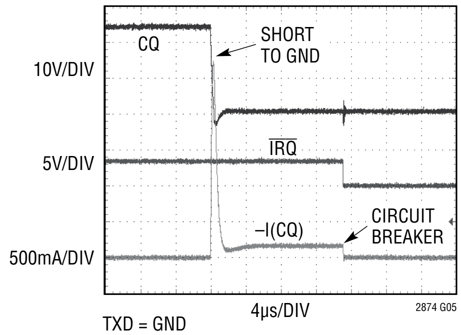
TYPICAL PERFORMANCE CHARACTERISTICS

$T_A = 25°C$, $V_{DD} = 24V$, $V_L = 3.3V$, unless otherwise noted.

Driver Current Limit vs Temperature

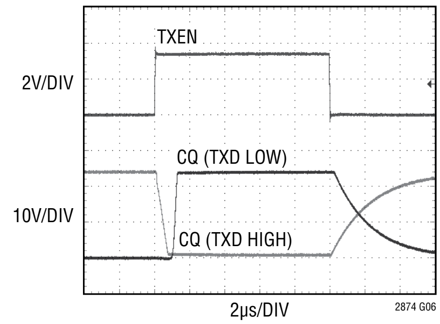


CQ Short Circuit Protection



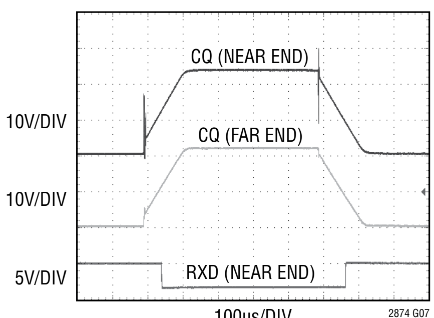
TXD = GND
SIO_MODE = 0
LOAD: 50pF

Driver Enable/Disable



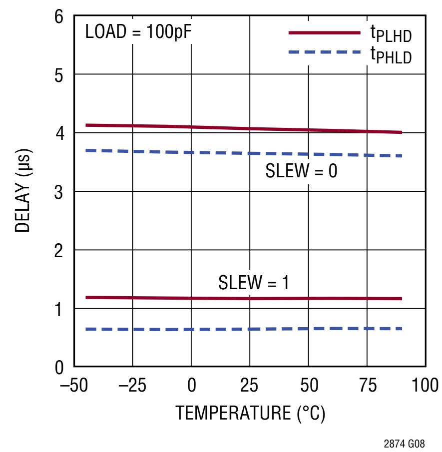
SLEW = 1, ILLM = 0x0
LOAD: 100pF (GND) + 10kΩ (V_{DD} OR GND)

Driving 20m Cable to 1µF Load

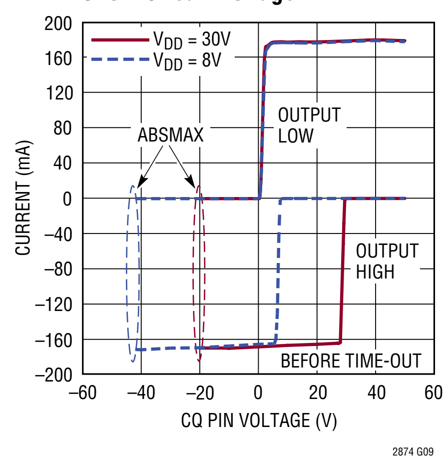


NSF = 0x2

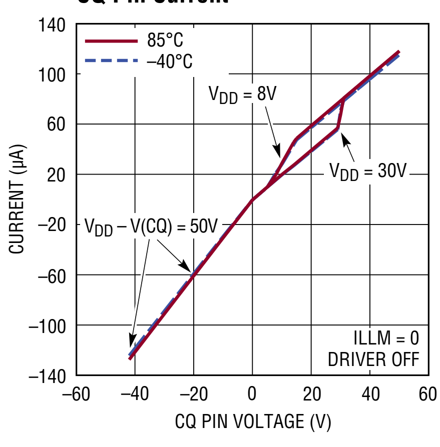
Driver Propagation Delay vs Temperature



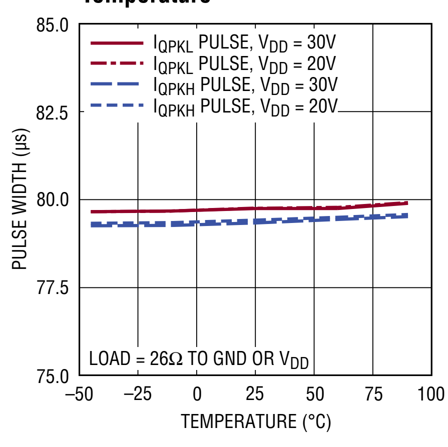
CQ Driver Short-Circuit Current vs Short-Circuit Voltage



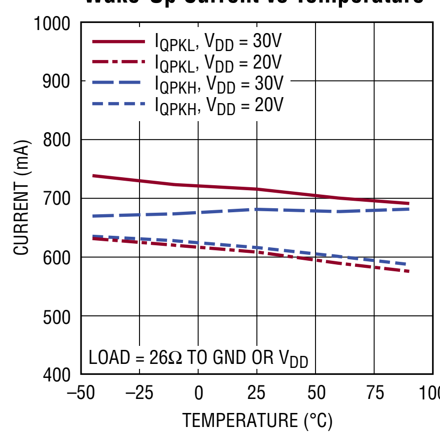
CQ Pin Current



Wake-Up Pulse Width vs Temperature



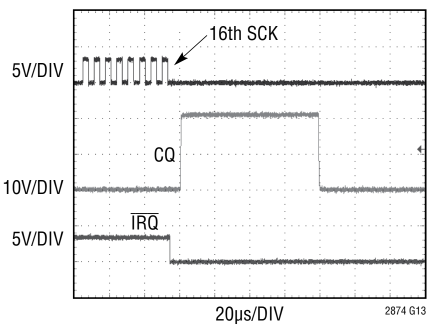
Wake-Up Current vs Temperature



TYPICAL PERFORMANCE CHARACTERISTICS

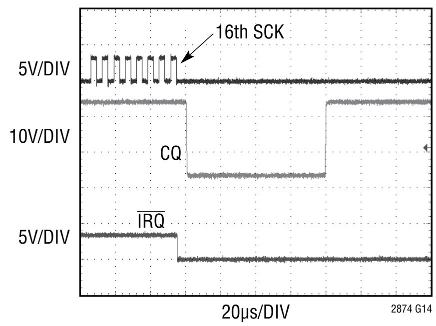
T_A = 25°C, V_{DD} = 24V, V_L = 3.3V, unless otherwise noted.

Wake-Up Pulse: I_{QPKH}



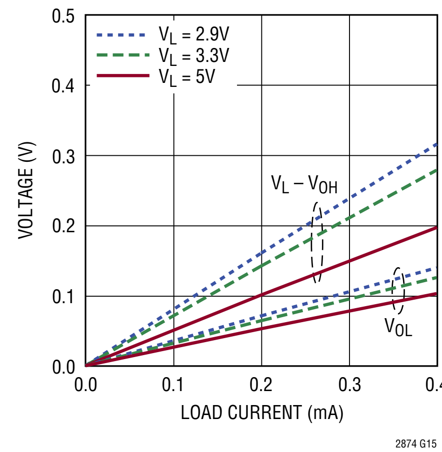
CQ LOAD: 4nF + 100Ω

Wake-Up Pulse: I_{QPKL}

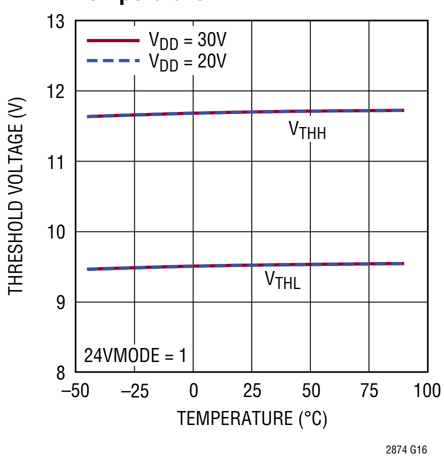


CQ LOAD: 4nF + 100Ω

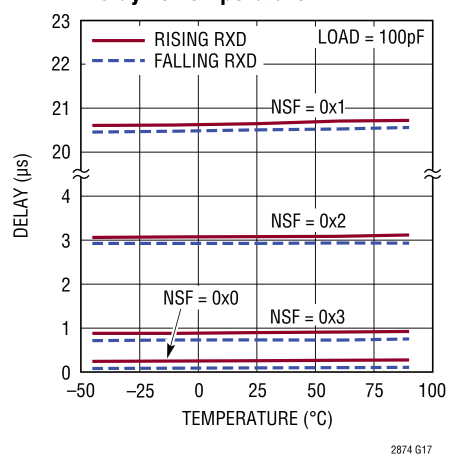
Receiver Output Voltage vs Load Current



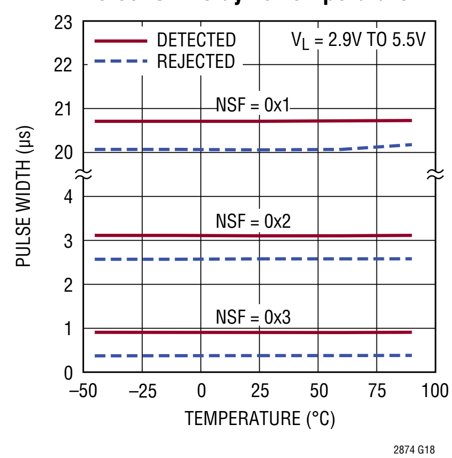
Receiver Input Threshold vs Temperature



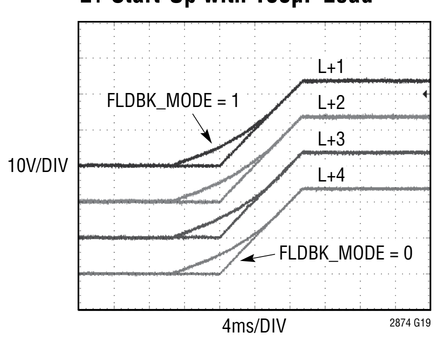
Receiver Propagation or Filter Delay vs Temperature



Receiver Pulse Rejection and Detection Delay vs Temperature

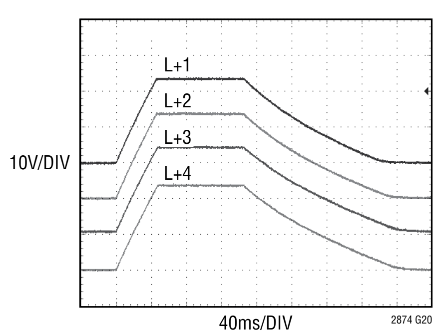


L+ Start-Up with 100µF Load



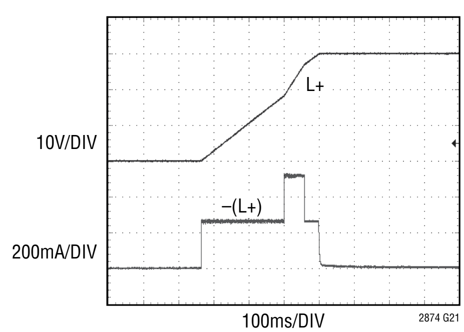
2XPTC = 0x1
LPTC = 0xB

L+ Start-Up (Set by C_G) and Disable



2XPTC = 0x1
FLDBK_MODE = 0
LOAD: 10µF
LPTC = 0xD
C_G: 22nF

2X Current Pulse at 18V

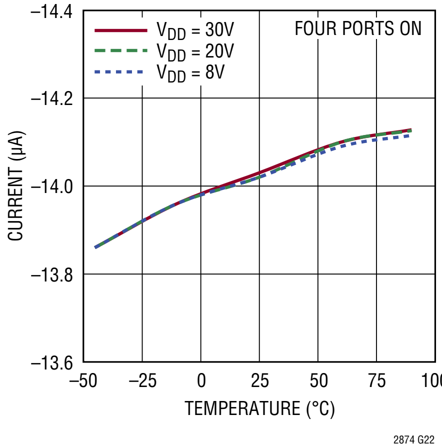


2XPTC = 0x0
FLDBK_MODE = 0
LOAD: 3500µF

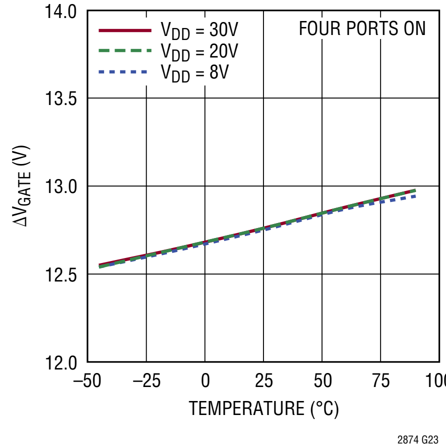
TYPICAL PERFORMANCE CHARACTERISTICS

T_A = 25°C, V_{DD} = 24V, V_L = 3.3V, unless otherwise noted.

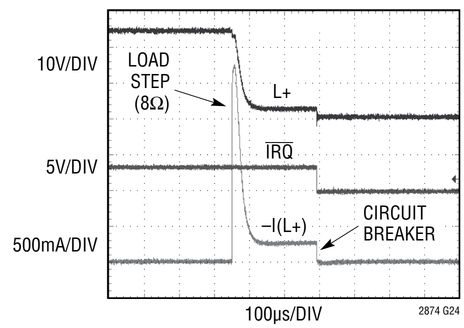
$I_{GATE(UP)}$ vs Temperature



External MOSFET V_{GS} (ΔV_{GATE}) vs Temperature

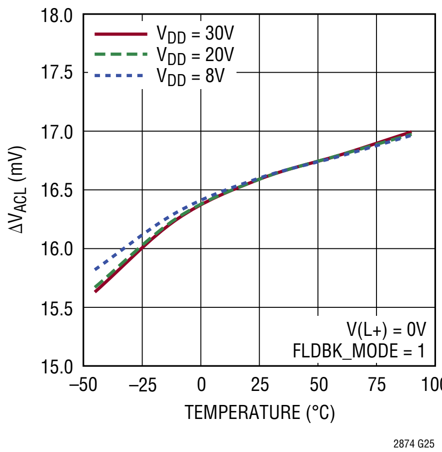


L+ Overcurrent Behavior

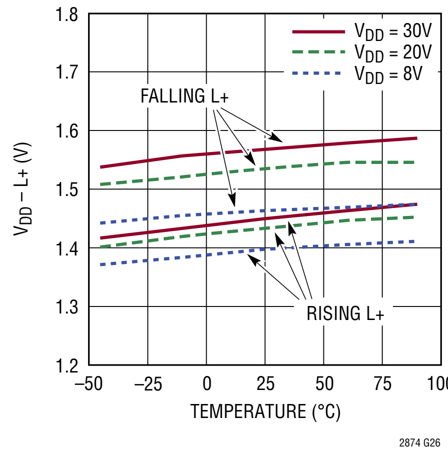


LPTC = 0x4
IRQMASK = 0xF6
FLDBK_MODE = 0
LOAD: 50pF

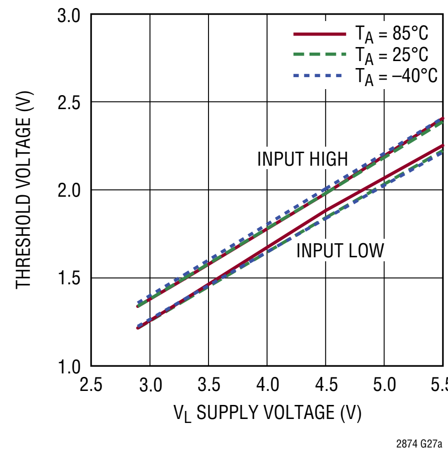
L+ Current Limit Sense Voltage vs Temperature



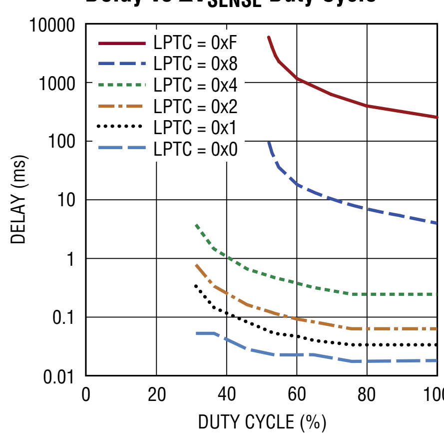
L+ Power Good Threshold vs Temperature



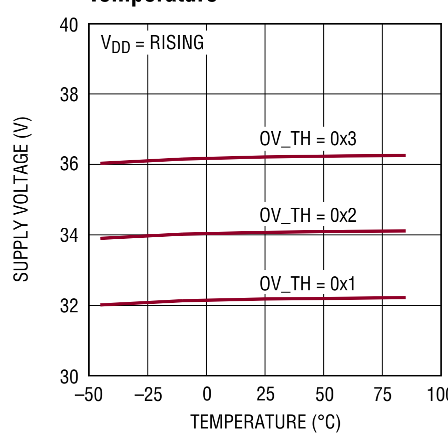
Logic Input Threshold vs V_L Supply Voltage



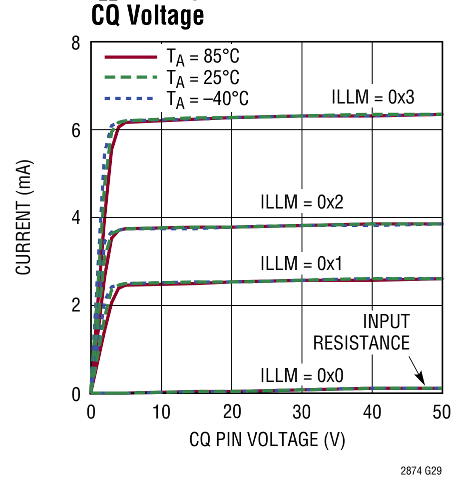
L+ Overcurrent Circuit Breaker Delay vs ΔV_{SENSE} Duty Cycle



V_{DD} Overvoltage Indicator vs Temperature

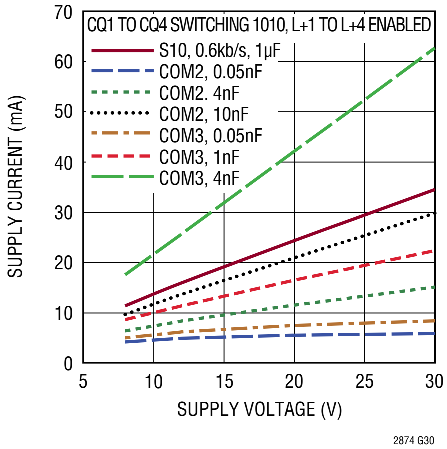


I_{LL} Sinking Current vs CQ Voltage

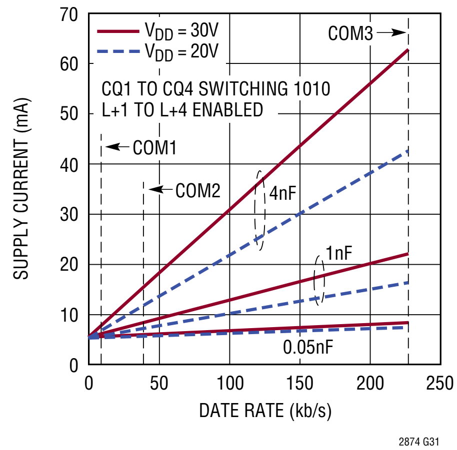


TYPICAL PERFORMANCE CHARACTERISTICS $T_A = 25°C$, $V_{DD} = 24V$, $V_L = 3.3V$, unless otherwise noted.

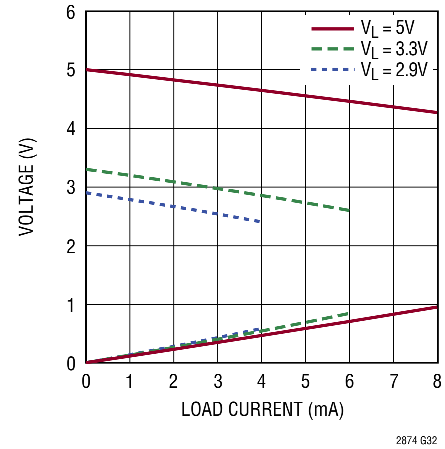
V_{DD} Supply Current vs Supply Voltage



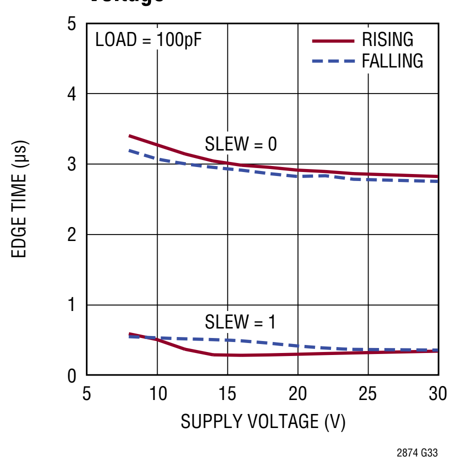
V_{DD} Supply Current vs Data Rate



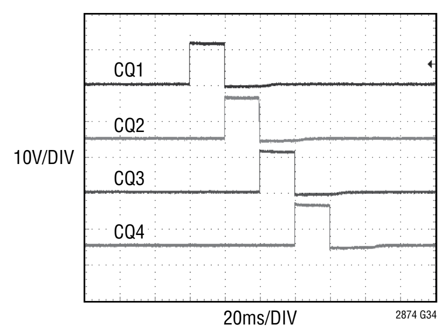
SDO Voltage vs Load Current



CQ Driver Edge Time vs Supply Voltage



Driving 12V Relay Coils



24VMODE = 0
RELAYS: G2R-1-E-T130 DC12 + CATCH DIODE
$V_{DD} = 12V$

PIN FUNCTIONS (FE/UHF)

TXEN4 (Pin 1/Pin 35): Port 4 CQ4 Driver Enable. See TXEN1.

GATE4 (Pin 2/Pin 36): Port 4 Gate Drive. See GATE1.

SENSE⁻4 (Pin 3/Pin 37): L+4 Supply Current Sense Negative Input. See SENSE⁻1.

L+4 (Pin 4/Pin 38): Port 4 Power Supply Output. See L+1.

CQ4 (Pin 5/Pin 1): Port 4 C/Q line. See CQ1.

CQ3 (Pin 6/Pin 2): Port 3 C/Q line. See CQ1.

GATE3 (Pin 7/Pin 3): Port 3 Gate Drive. See GATE1.

SENSE⁻3 (Pin 8/Pin 4): L+3 Supply Current Sense Negative Input. See SENSE⁻1.

L+3 (Pin 9/Pin 5): Port 3 Power Supply Output. See L+1.

SENSE⁺ (Pin 10/Pin 6): L+ Current Sense Common Positive Input. Connect external sense resistors RS1 through RS4, normally 0.2Ω, between this pin and each of the SENSE⁻ pins in a star configuration. See Applications Information. Tie to V_{DD} if unused. Do not leave open.

V_{DD} (Pin 11/Pin 7): Supply Voltage Input (8V to 30V). Bypass to GND with a 1µF ceramic capacitor placed near the pin and at least 100µF additional bulk capacitance.

PIN FUNCTIONS (FE/UHF)

GATE2 (Pin 12/Pin 8): Port 2 Gate Drive. See GATE1.

SENSE⁻2 (Pin 13/Pin 9): L+2 Supply Current Sense Negative Input. See SENSE⁻1.

L+2 (Pin 14/Pin 10): Port 2 Power Supply Output. See L+1.

CQ2 (Pin 15/Pin 11): Port 2 C/Q line. See CQ1.

CQ1 (Pin 16/Pin 12): Port 1 Bidirectional Communication or Signaling (C/Q) Line. When the port 1 driver is enabled (either by TXEN1 or under SPI control), this pin is an output referenced to GND, inverted in polarity with respect to the TXD1 input. Otherwise, this pin is an input that a remote device may drive and an optional, programmable current sink is active. Receiver output RXD1 monitors this pin in both cases.

GATE1 (Pin 17/Pin 13): Gate Drive for External N-Channel MOSFET, Port 1. When the MOSFET is turned on, a 14μA current drives the gate to 13V above the L+1 output supply voltage. During a current limit condition, the voltage at GATE1 reduces to maintain constant L+ port current. If a timer expires, GATE1 pulls down, turning off the MOSFET, and a TOC_L+ event is recorded.

SENSE⁻1 (Pin 18/Pin 14): L+1 Supply Current Sense Negative Input. Load current is programmed using an external sense resistor RS1, normally 0.2Ω, connected between this pin and $SENSE^+$. Current is controlled by an analog current limit amplifier and timed circuit breaker. See L+ PIN POWER CONTROL in the Applications Information section. Tie to V_{DD} if unused. Do not leave open.

L+1 (Pin 19/Pin 15): Port 1 Output Supply Monitor and Source Connection. Connect this pin to the source of the external MOSFET for port 1.

RXD1 (Pin 20/Pin 16): Port 1 Data Output from CQ1 Receiver, Referenced to V_L. Active even when the driver is on. RXD1 polarity is inverted with respect to the line data at the CQ1 pin.

TXD1 (Pin 21/Pin 17): Port 1 Data Input to CQ1 Driver, Referenced to V_L. Tie to V_L if unused.

TXEN1 (Pin 22/Pin 18): Port 1 CQ1 Driver Enable, Referenced to V_L. Tie to GND if unused.

$\overline{IRQ}$ (Pin 23/Pin 19): Interrupt Output. Open drain output that pulls low to alert the host microcontroller when an event occurs, eliminating the need for continuous software polling. Disable individual $\overline{IRQ}$ events using the IRQMASK register. $\overline{IRQ}$ typically has a pull-up resistor to V_L.

SDO (Pin 24/Pin 20): SPI Interface Data Output, Referenced to V_L.

RXD2 (Pin 25/Pin 21): Port 2 Data Output from CQ2 Receiver. See RXD1.

TXD2 (Pin 26/Pin 22): Port 2 Data Input to CQ2 Driver. See TXD1.

TXEN2 (Pin 27/Pin 23): Port 2 CQ2 Driver Enable. See TXEN1.

V_L (Pin 28/Pin 24): Logic supply (2.9V to 5.5V) for the control logic, registers, receiver outputs, driver inputs, and SPI interface. Bypass to GND with at least a 0.1μF capacitor.

GND (Pins 29, 30, Exposed Pad Pin 39/Pins 25, 26, Exposed Pad Pin 39): Device Ground. The exposed pad metal of the package provides both electrical contact to ground and good thermal contact to the PCB. Solder to the board and tie directly to the ground plane using thermal vias.

SDI (Pin 31/Pin 27): SPI Interface Data Input, Referenced to V_L. Tie to GND if unused.

SCK (Pin 32/Pin 28): SPI Interface Clock Input, Referenced to V_L. Tie to GND if unused.

$\overline{CS}$ (Pin 33/Pin 29): SPI Interface Chip Select Input (Active Low), Referenced to V_L. Tie to V_L if unused.

RXD3 (Pin 34/Pin 30): Port 3 Data Output from CQ3 Receiver. See RXD1.

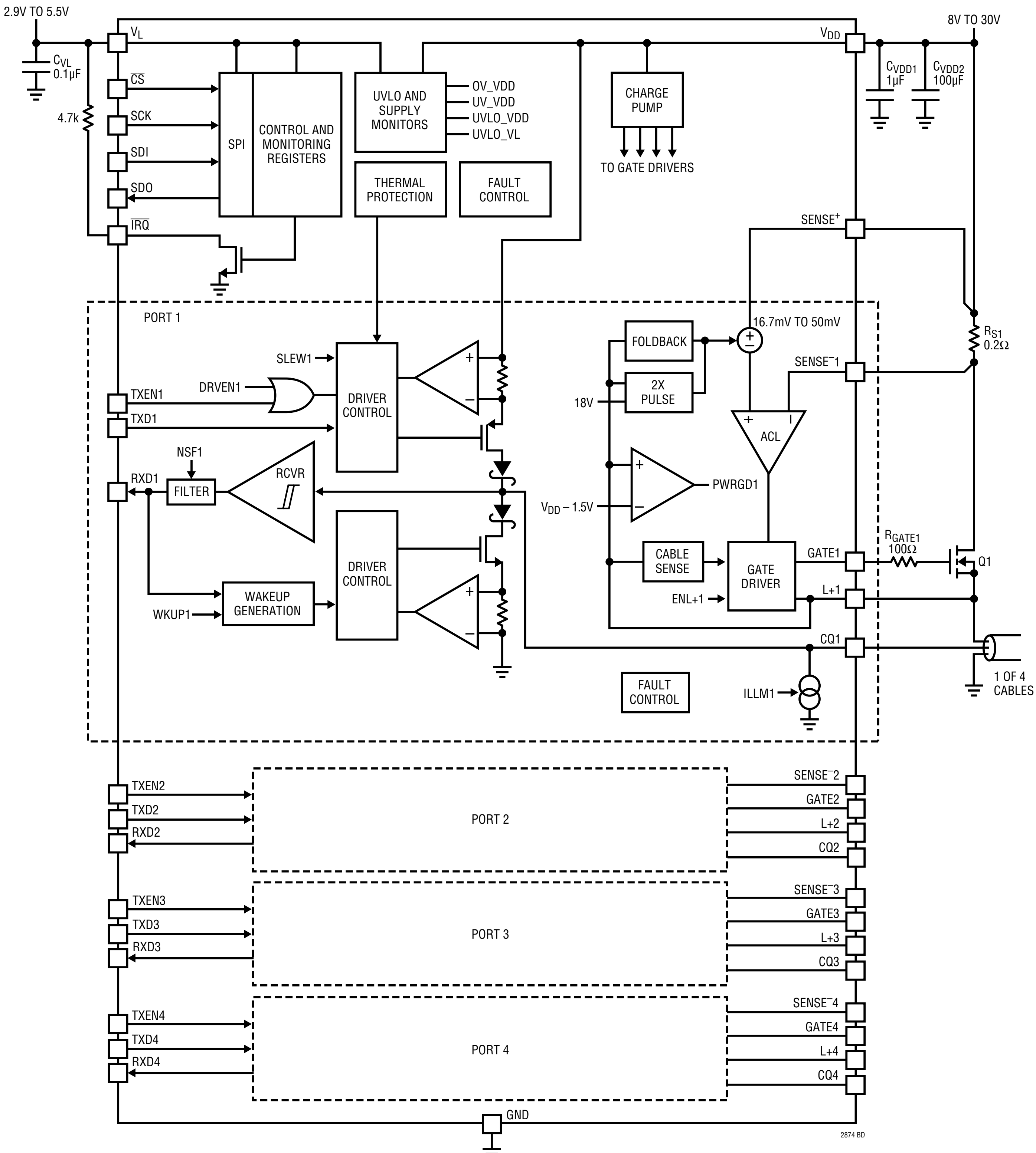
TXD3 (Pin 35/Pin 31): Port 3 Data Input to CQ3 Driver. See TXD1.

TXEN3 (Pin 36/Pin 32): Port 3 CQ3 Driver Enable. See TXEN1.

RXD4 (Pin 37/Pin 33): Port 4 Data Output from CQ4 Receiver. See RXD1.

TXD4 (Pin 38/Pin 34): Port 4 Data Input to CQ4 Driver. See TXD1.

BLOCK DIAGRAM



TEST CIRCUITS / TIMING DIAGRAMS

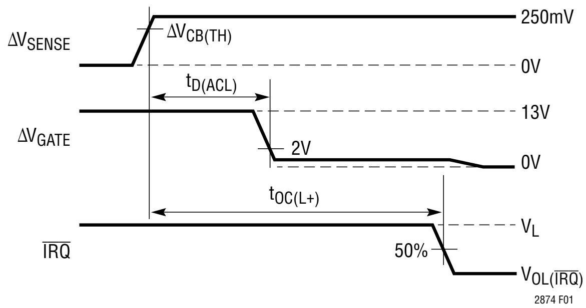


Figure 1. L+ Pin Overcurrent

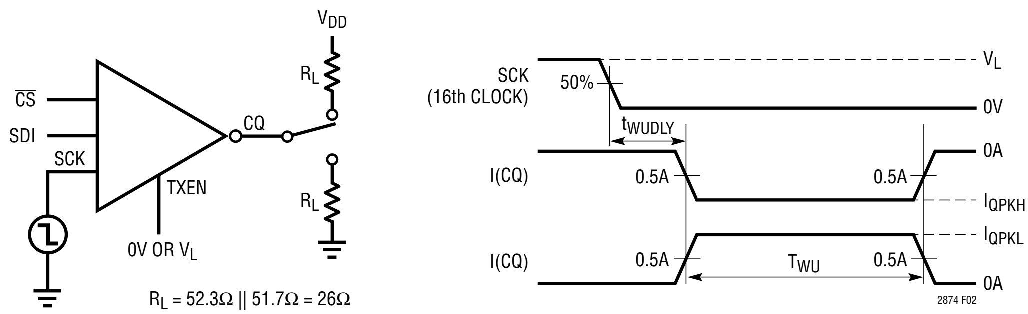


Figure 2. Wake-Up Parameters

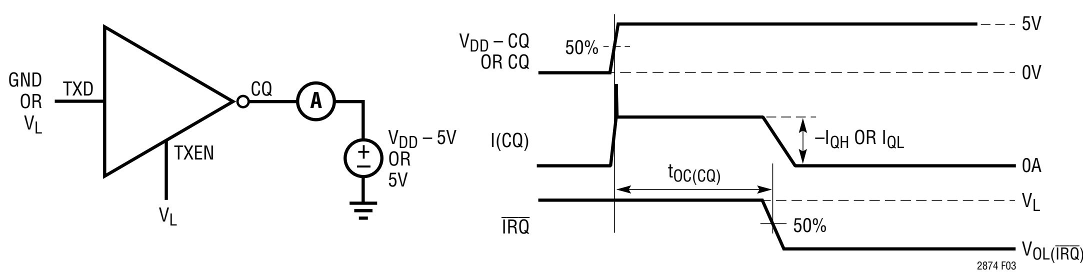


Figure 3. CQ Pin Overcurrent

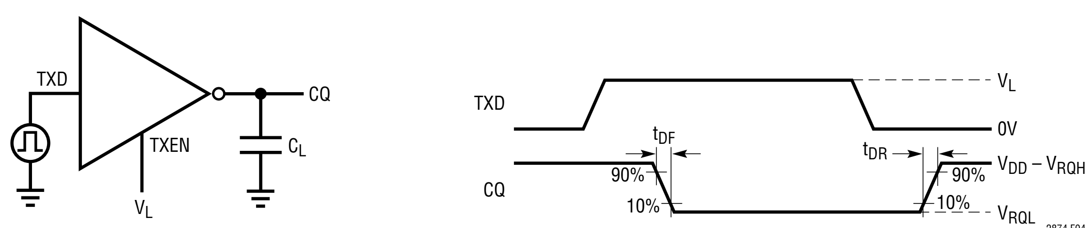


Figure 4. Driver Edge Rate

TEST CIRCUITS / TIMING DIAGRAMS

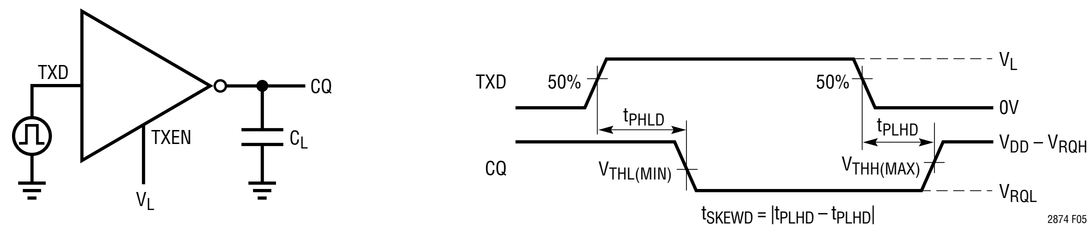


Figure 5. Driver Timing

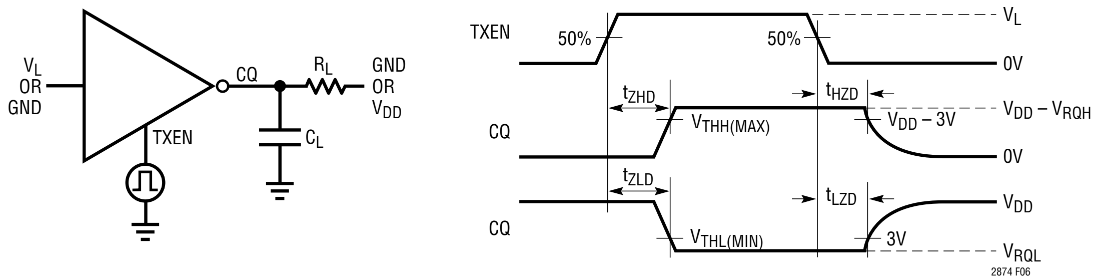


Figure 6. Driver Enable/Disable Timing

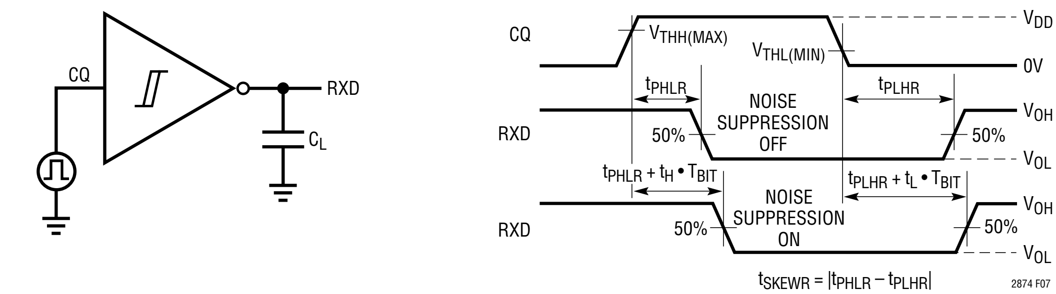


Figure 7. Receiver Timing

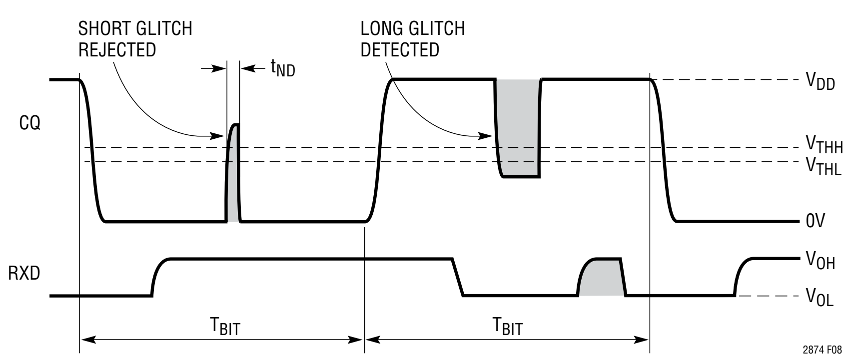


Figure 8. Receiver Noise Suppression

TEST CIRCUITS / TIMING DIAGRAMS

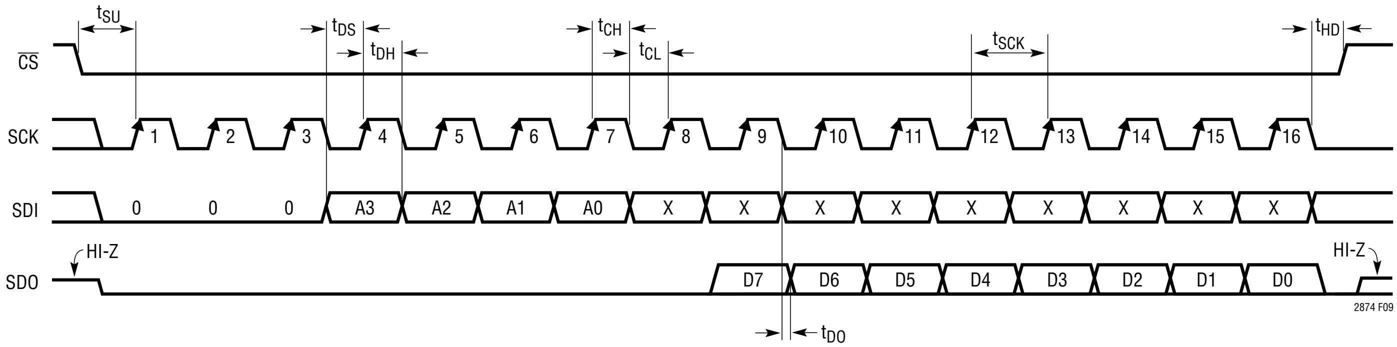


Figure 9. SPI Interface Timing (Read)

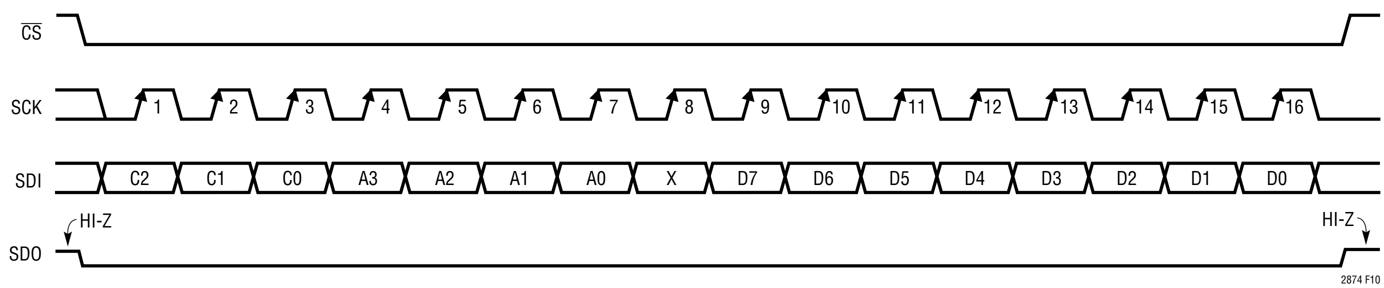


Figure 10. SPI Interface Timing (Write or WrtUpd)

OPERATION

The LTC2874 is an industrial master Hot Swap bus controller and physical interface (PHY) that provides power and communication to four independent 3-wire ports through cables up to 20m in length (see Figure 11A). The primary applications are 24V systems specified by IEC 61131-9 single-drop communication interface (SDCI) for small sensors and actuators, commonly known as IO-Link. Each port on the LTC2874 includes a Hot Swap power supply output, data transceiver, and a current sink, as shown in Figure 11B. This set of features allows a typical master controller for four ports to be built with the LTC2874, a host microcontroller, and four power MOSFETs.

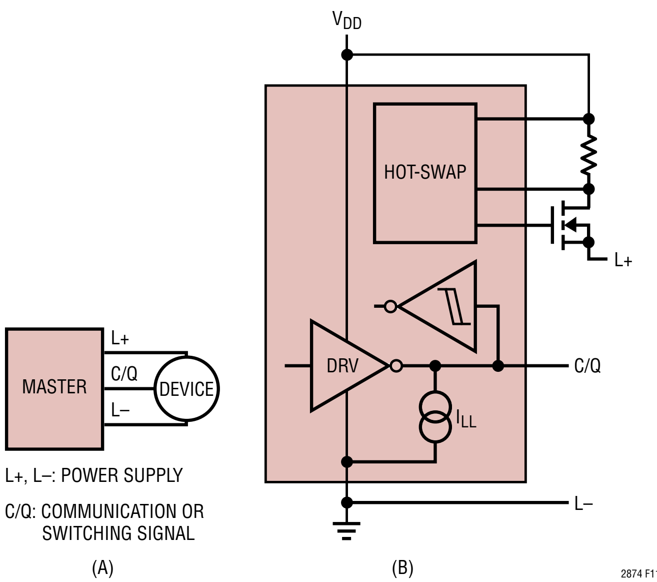


Figure 11. (A) SDCI Class A 3-Wire Interface (B) LTC2874 Master 3-Wire Interface Port

The bidirectional CQ pins are individually programmable to operate in coded switching (COM) or switching signal (standard IO, or SIO) format with reconfigurable behavior including slew rate, noise suppression filter, and sinking current. Drivers are protected against overcurrent faults by circuit breakers that respond to a fault condition after a mode-specific delay. For IO-Link compatibility, under SPI control, the LTC2874 automatically generates 80μs wake-up request (WURQ) pulses with correct polarity.

The LTC2874 turns each port's supply voltage on and off in a controlled manner using external N-channel MOSFETs. External sense resistors individually set the current limits for each port. Optional foldback behavior reduces maximum power dissipation in the external MOSFETs over their operating range. Each output is protected by a circuit breaker that responds to an overcurrent fault after a programmable timeout delay. A current-pulse-upon-18V feature provides additional IO-Link capability for driving heavy, nonlinear loads.

The rugged LTC2874 line interface has been designed to tolerate abusive conditions encountered on cable interfaces. The CQ pins will tolerate 50V above L– (GND) and –50V from V_{DD}. The L+ pins offer commensurate ruggedness for power supply outputs (see Absolute Maximum Ratings).

Discrete power MOSFETs offer the best possible system ruggedness and allow design flexibility. They also ensure that ports remain fully independent in the event of extreme fault conditions.

Normally, the LTC2874 will automatically restart after supply overvoltage or port overcurrent timeout faults. The auto-retry delay is programmable. Alternatively, latchoff behavior is available. Overcurrent circuit breaker delays for CQ pins are mode dependent; for L+ pins they are programmable.

The LTC2874 provides a 4-wire SPI-compatible interface for configuration and monitoring. The host can detect faults and other events by polling four event registers or by monitoring the $\overline{IRQ}$ pin, a programmable interrupt request.

Standalone Operation

The LTC2874 is designed for use with a host controller. The SPI-compatible interface is the only means of operating the Hot Swap power supply outputs. The transceivers can operate standalone without the serial interface, restricted by the default register configuration settings.

APPLICATIONS INFORMATION

Drivers

The LTC2874 line drivers convert digital levels at the TXD pins to inverted polarity line levels at the CQ pins. Drive at data rates of up to 230.4kb/s. For IO-Link operation, they support COM1, COM2, and COM3 transmission. The four drivers operate concurrently and independently.

The LTC2874 line drivers are current limited to 160mA. Each is protected by an overcurrent circuit breaker with mode-selectable timeout. For normal signaling (SIO = 0), the circuit breaker will trip after being in current limit for 15µs. This timeout is more than sufficient to support IO-link requirements.

The drivers feature a controlled programmable slew rate for optimum EMC performance. Rise and fall times are programmed using a register bit and are independent of the V_{DD} supply voltage. Set each driver's SLEW bit high for edge times of 0.5µs, or low for edge times of 3µs.

Each driver is enabled either by its TXEN pin or DRVEN register bit. When disabled, drivers are Hi-Z and the CQ pin impedance is dominated by the I_{LL} current sink (unless disabled) and the receiver input resistance.

While the line drivers normally operate push-pull, each can also operate in open-drain mode by driving the data signal into its TXEN pin. For operation with an external pull-up, tie its TXD pin high. For an external pull-down, disable that port's current sink (ILLM = 0) and tie its TXD pin low.

SIO Mode

Up to 1µF of load capacitance can be driven in SIO, or standard I/O, mode. Set SIO = 1 and reduce the edge rate (SLEW = 0). In this mode, the overcurrent circuit breaker timeout is extended to 480µs.

Configuring CQ Outputs for 200mA or 400mA

The LTC2874 driving capability can be increased by connecting CQ outputs and operating drivers in parallel. Figure 36 shows a 2-port configuration that guarantees a minimum CQ drive strength of 200mA, and Figure 37 shows a configuration for 400mA. Combine only CQ outputs from a single LTC2874.

Receivers

The four receivers convert 24V signals detected at the CQ line inputs to inverted-polarity logic levels at the RXD outputs. Receiver threshold behavior is selectable, as shown in Figure 12. When the 24VMODE bit is set low, the receiver thresholds for all four ports track the input V_{DD} supply.

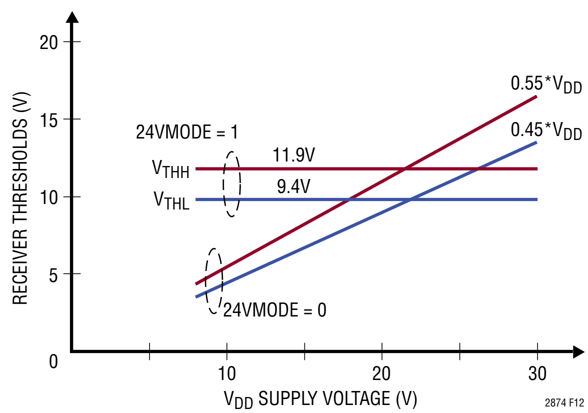


Figure 12. CQ Receiver Input Threshold (Typical)

Each receiver has an optional digital noise filter that rejects narrow pulses on the CQ line. Filter delays of 0.6µs, 2.8µs or 20.3µs are selected using port-specific NSF register bits. Setting NSF = 0x0 disables the filter.

When the receiver is operated at an IO-Link compatible data rate (COM3, COM2 or COM1) and the NSF bits are set accordingly, the filter rejects pulses shorter than 1/16 of the bit time. Figure 13 illustrates the rejection and detection bands for a positive noise glitch.

Except when Hi-Z at start-up (see Figure 26), receivers are always active.

Driver and receiver settings appropriate for SIO mode and IO-Link operation are summarized in Table 1.

Table 1. Recommended Driver and Receiver Settings

OPERATION	SLEW	NSF	SIO_MODE
SIO	0	0x1	1
COM1	0	0x1	0
COM2	0	0x2	0
COM3	1	0x3	0

APPLICATIONS INFORMATION

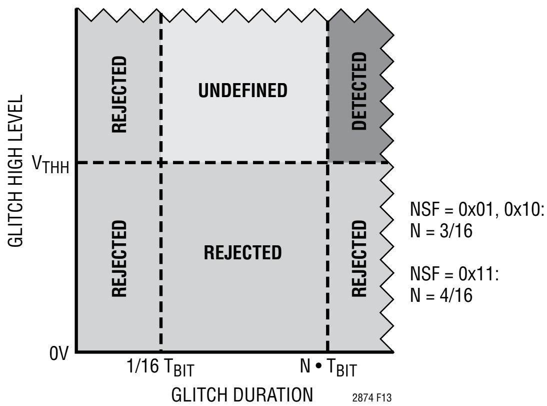


Figure 13. Receiver Noise Rejection and Detection Behavior for CQ Positive Glitch

Current Sinks

Each CQ pin has a programmable current sink for use with sensors having high side outputs. Each port's current sink is independently set to a value of 0mA, 2.5mA, 3.7mA, or 6.2mA with port-specific ILLM register bits. The highest setting guarantees 5mA for IO-link. The second setting guarantees 2.2mA for compatibility with IEC 61131-2 digital inputs. Each current sink disables when its driver is enabled or a wake-up request is in progress on that port.

Automatic Wake-Up Generation

The LTC2874 generates an 80µs 500mA wake-up pulse for the purpose of gaining the attention of a remote IO-Link device. To initiate WURQ generation on a particular port, the respective WKUP bit must be set high. Acting as a pushbutton, the bit will self-clear once the WURQ is underway. The sequence begins by automatically determining the correct polarity for the pulse, first by disabling the driver (as needed) and sensing the CQ line for 5µs. The driver switches on to generate the pulse, then returns to its state prior to the WURQ (normally off). The complete sequence is shown in Figure 14.

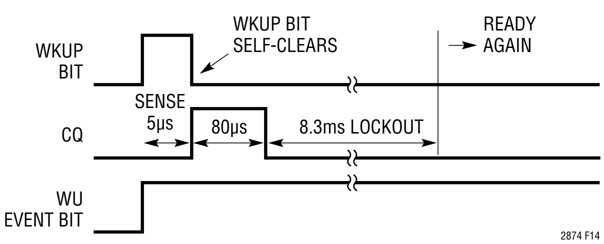


Figure 14. Wake-up Sequence

Although WURQs may be generated with the driver enabled, we recommend the following procedure for best results:

1. Disable driver.
2. Clear any driver fault by setting TOC_CQ event bit low.
3. Generate WURQ by setting WKUP bit high.

Several measures prevent overheating during WURQ, when driver power dissipation can be high (for example, easily 15W at maximum operating voltage). First, if any overtemperature condition is detected when the WKUP bit is first set high, polarity sensing and pulse generation are delayed until the condition clears. Second, only one port at a time is allowed a WURQ, determined by lowest port number in the event of a simultaneous request. Third, upon completion of a WURQ, an 8.3ms cool-down interval is enforced before another WURQ can be generated. While a WURQ is underway on any port, the WKUP bits cannot be set. (Their holding latches can be set high with a write command, and even read out, but when updated by an update or WrtUpd command, they will clear and not change the register bits themselves. See the Serial Interface section for more information.) Finally, a thermal shutdown condition will cause the driver to turn off. Normal overcurrent circuit breaker timers are disabled during wake-up.

Setting the 24VMODE register bit low disables wake-up generation; the WKUP bits have no effect and will not self clear.

L+ PIN POWER CONTROL

External MOSFET, Sense R Summary

One function of the LTC2874 is to control delivery of power through cables to four remote devices. On each port it does this by controlling the gate voltage of an external power MOSFET based on the current monitored by an external sense resistor and the output voltage at the L+ pin. This circuitry couples the raw V_{DD} input supply to each port through the MOSFET in a controlled manner that satisfies the power needs of the connected device while minimizing power dissipation in the MOSFET and disturbances on the V_{DD} backplane.

APPLICATIONS INFORMATION

The current limit of each LTC2874 L+ port is set with a resistor of value $\Delta V_{ACL}/I_{LIMIT}$. Specified variation in ΔV_{ACL} (±10%) and tolerance of the resistor must be taken into account. For IO-Link applications (which require a guaranteed minimum of 0.2A), 0.2Ω sense resistors (R_{S1} to R_{S4}) will set the typical limit 25% above the required minimum.

Inrush Control

When the L+ supply of any port is enabled (ENL+ = 1), the LTC2874 ramps up the GATE pin of that port's external MOSFET in a controlled manner. The gate drivers use a shared charge pump that derives its power from V_{DD}. Under normal power-up circumstances, the MOSFET gate rises until the port current reaches the current limit, at which point the GATE pin is servoed to maintain the current limit. The ramp rate of the L+ port output voltage is:

$$\frac{dV(L+)}{dt} = \frac{I(L+)}{C_{L+}} = \frac{\Delta V_{ACL}}{R_S \bullet C_{L+}}$$

where C_{L+} is the capacitance on the L+ pin, including supply bypass capacitance of the connected device.

During this inrush period, an integrating up/down counter times the duration that the current exceeds the circuit breaker threshold $\Delta V_{CB(TH)}$. When output charging is complete, the port current falls and the GATE pin resumes rising to fully enhance the MOSFET and minimize its on-resistance. The final V_{GS} is nominally 13V. If the timer expires before the inrush period completes, the port is turned off and a TOC_L+ fault is reported. The timer delay is adjustable from 17.5µs to 0.25s using the LPTC register bits.

Optionally, the L+ pin ramp rate can be slowed further using the R_GC_G network shown in Figure 22. For a sufficiently large capacitor, the ramp rate is:

$$\frac{dV(L+)}{dt} = \frac{dV(GATE)}{dt} = \frac{I(GATE)}{C_G} = \frac{14\mu A}{C_G}$$

Using a C_G of 10nF will cause L+ to ramp on in about 20ms.

L+ Current Limit

The LTC2874 actively controls the MOSFET gate drive to keep the port current below $\Delta V_{ACL}/R_S$. It allows the port current to exceed $\Delta V_{CB(TH)}/R_S$ for a limited time before powering down the port. This duration is timed by an integrating up/down counter for that port whose minimum timeout, which is common to all ports, is set in the TMRCTRL register (0xC). If the current drops below the circuit breaker current threshold before the timer expires, the timer counts back down at the same rate. This allows the current limit circuitry to tolerate intermittent overload signals with duty cycles below about 50%; longer duty cycle overloads will turn the port off.

L+ Current Limit Foldback Protection

During port start-up (inrush) or when a cable is connected (hot-plugged) to an enabled port, most of the supply voltage is dropped across the MOSFET as it begins to supply charging current to the remote device. To protect the MOSFET from overheating, the LTC2874 has a current limit foldback circuit that limits the maximum power dissipated by the external MOSFET, thereby increasing its robustness. Figure 15 shows how ΔV_{ACL} is linearly reduced (folded back) according to the voltage on the L+ pin. The circuit breaker voltage $\Delta V_{CB(TH)}$ is also folded back and remains no higher than ΔV_{ACL}. Figure 16 shows typical power-on behavior with foldback.

Foldback mode may interfere with start-up into some resistive loads. Setting the FLDBK_MODE bit low disables foldback behavior.

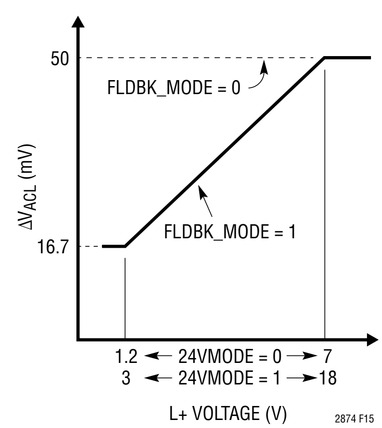


Figure 15. L+ Foldback Characteristic

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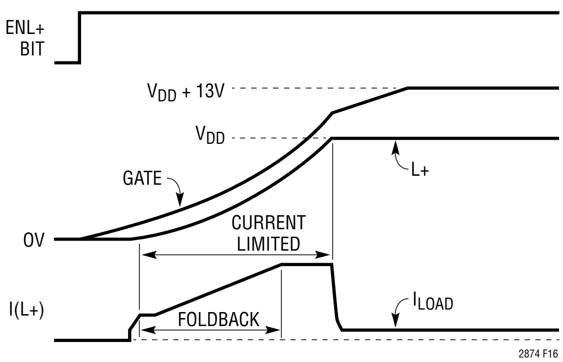

Figure 16. L+ Enable Behavior with Foldback

L+ Overcurrent Fault

When a circuit breaker timeout occurs, the corresponding timeout fault event bit (TOC_L+) is set and the GATE pin is pulled down to the L+ pin with a 90mA current. The remaining ports of the LTC2874 are unaffected, and the ENL+ bit remains set. If the RETRY_L+ bit is set, auto-retry will re-enable the port after a delay; otherwise, the port latches off until the event bit is cleared. Figure 24 and Figure 25 show example behavior.

L+ Supply Current Pulse Capability

The LTC2874 can optionally double the available current (to $2 \bullet \Delta V_{ACL}/R_S$) when an L+ output supply is first powered on, accommodating connected devices that require higher current during their own start-up phase. This function may be useful in applications where there is no signaling that it's safe to turn on downstream dynamic loads.

Figure 17 shows simplified behavior when connected to a 100µF load with a 0.2Ω sense resistor and foldback disabled (FLDBK_MODE = 0).

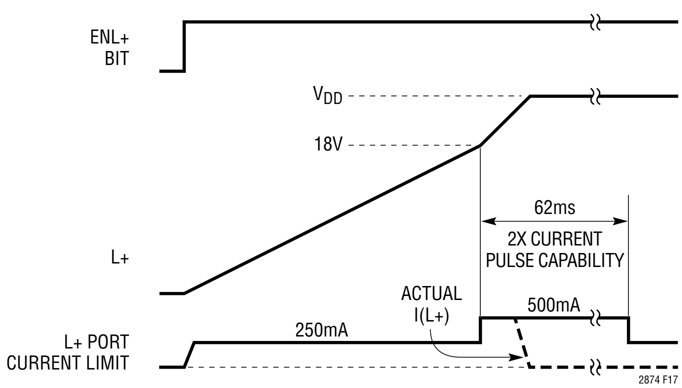

Figure 17. L+ Current Pulse Capability

When the L+ pin voltage first reaches 18V, the L+ port current limit is doubled for a timed interval. The current sense voltage ΔV_{ACL} and overcurrent circuit breaker threshold voltage $\Delta V_{CB(TH)}$ are both increased 100% until the timer expires.

The start-up pulse duration is set using the 2XPTC register bits. The default setting of 62ms satisfies the required minimum of 50ms for IO-Link compatibility. Durations of 31ms and 124ms are also available. Set the L+ overcurrent timer (adjusted with the LPTC register bits) longer than the start-up pulse timer to ensure that the circuit breaker doesn't interfere. Setting 2XPTC to 0x1 disables the start-up pulse function.

L+ Power Good and Power Changed

Power good status is signalled when the L+ pin voltage rises to within $V_{L+(PGTH)}$ of the V_{DD} supply rail and the GATE to L+ voltage exceeds 3.8V, indicating that the MOSFET is almost fully enhanced.

After a 10µs delay, a PWRCHNG event indicates that the PWRGD status has changed, as shown in Figure 18.

Once an L+ output is disabled, the PWRGD status bit clears and the PWRCHNG event bit no longer signals.

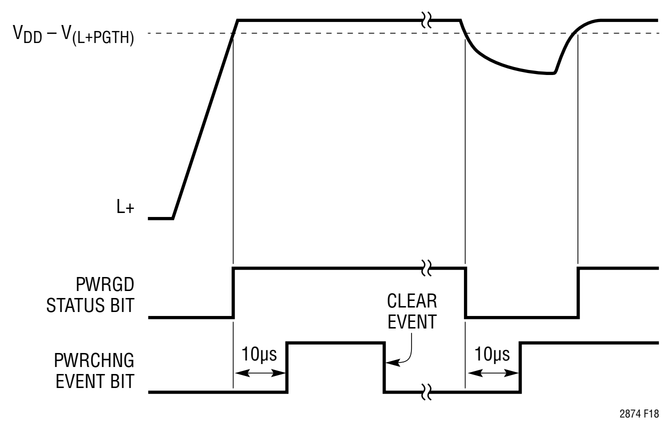

Figure 18. Power Good Status and Power Changed Event

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Gate Turn-Off

When a port is disabled (ENL+ = 0), its MOSFET is turned off with a 1.2mA current pulling down the GATE pin to GND. The L+ pin voltage drops as C_{L+} discharges.

The LTC2874 is designed to turn off the GATE rapidly during certain fault conditions to prevent damage to the MOSFET. The fault events that initiate a faster shut down include UVLO of either supply, V_{DD} overvoltage (unless OV_ALLOW = 1), and overcurrent circuit breaker timeout (TOC_L+). In these cases the GATE pin is discharged to the L+ pin with a 90mA current.

Cable Sensing

Hot-plugging, or the connection and disconnection of cables to an already enabled port, can cause sparking and reliability problems as connector plating wears off over time. Connection sensing mode (CSENSE_MODE = 1) mitigates this problem, extending connector lifetime. When a port is enabled with this feature active, the LTC2874 waits until it detects an external connection to its L+ pin before enhancing the external MOSFET supplying it.

The cable sense function identifies cable connections by measuring capacitive loading. The concept is shown in Figure 19. When a given port is enabled, the L+ and GATE pins are trickle-charged positive with 200µA, keeping ΔV_{GATE} close to 0V. The LTC2874 determines that a cable is connected if either L+ doesn't rise in 20.5ms (because it is loaded) or L+ subsequently pulls low (because a connected cable steals trickle current charge). Figure 20 and Figure 21 illustrate the behavior.

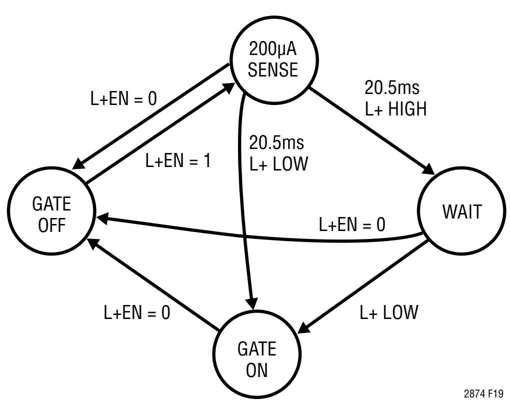

Figure 19. Cable Sensing State Diagram

At the maximum operating supply, the timer delay accommodates typically 100nF of combined L+ and GATE pin loading on the master board without falsely detecting a connection. Cable disconnection is not sensed.

Power good (PWRGD) status is low during the SENSE and WAIT states.

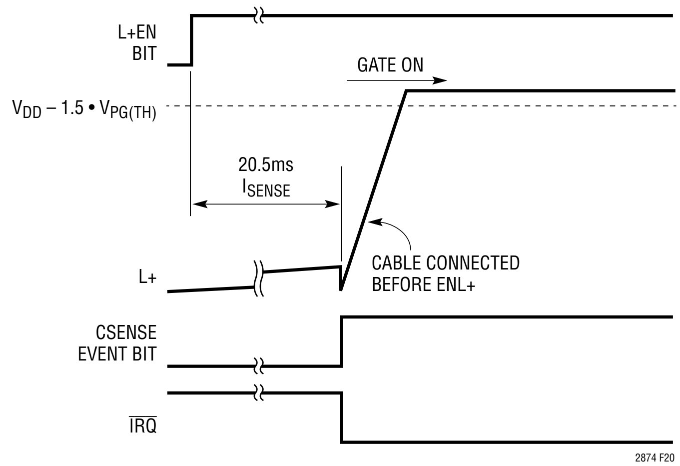

Figure 20. Cable Sense Behavior: Connection Before ENL+

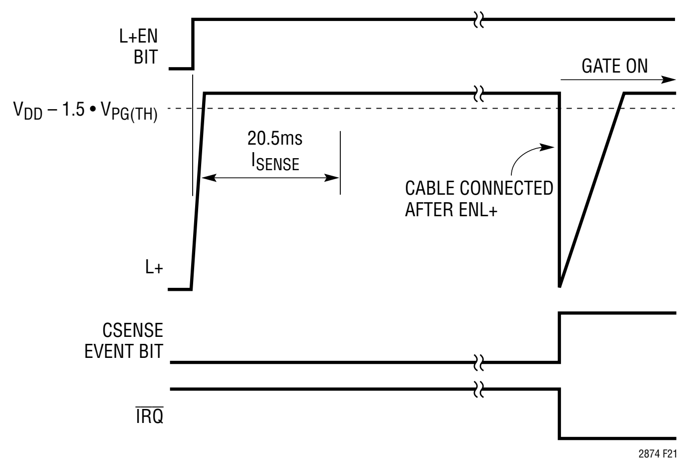

Figure 21. Cable Sense Behavior: Connection After ENL+

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L+ Current Limit Stability

For many applications the LTC2874 current limit is stable with a minimum of external components. In Figure 22, R_{GATE} is required to suppress the tendancy for Q1 to develop parasitic self-oscillation. A value between 10Ω and 100Ω is recommended. The bypass capacitors on the V_{DD} input supply play an essential role as well.

In some applications, additional components are needed to improve stability. Small MOSFETs with especially low C_{GS} are less stable, as are larger sense resistors R_S. Improve stability using the R_GC_G compensation network in Figure 22. For R_G, choose a value between 100Ω (normally sufficient) and 1kΩ; for C_G, use between 2nF and 10nF. Do not connect C_G directly between the GATE pin and ground.

Board level short-circuit testing is recommended. The worst-case condition for current limit stability occurs when the output is shorted to ground after a normal start-up.

The capacitor C_G serves a dual purpose, also setting the L+ pin ramp rate described in the Inrush Control section.

MOSFET Selection

Careful selection of the power MOSFET is critical to system reliability. For IO-Link compatibility, Linear Technology recommends Fairchild FQT7N10, or a similar planar process device in a SOT-223 package. Larger devices may degrade transient performance of current limiting, while smaller devices are more likely to require external compensation (see L+ Current Limit Stability) and require more care to stay within the rated safe operating area (SOA).

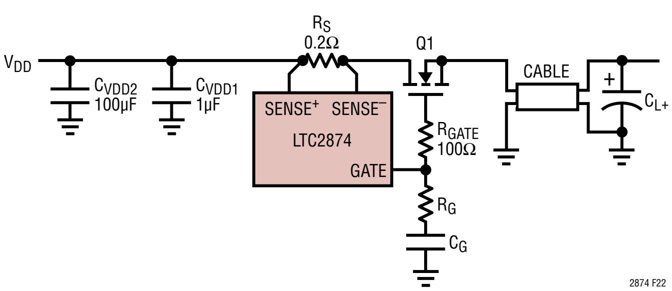

Figure 22. External Components for Improving Stability and Controlling Inrush Current

Design Example

The MOSFET is sized to handle power dissipation during inrush when L+ loads are being charged. Considering the case of a load capacitor C_{L+}, power dissipation during inrush can be determined based on the principle that:

Energy in the MOSFET = Energy in C_{L+}

This stored energy is $0.5 \cdot CV^2$. For example:

Energy in $C_{L+} = 0.5 \cdot 100\mu F \cdot (30V)^2 = 0.045J$

With foldback mode disabled, the time it takes to charge up C_{L+} is:

$$t_{STARTUP} = \frac{V_{DD} \cdot C_{L+}}{\frac{\Delta V_{ACL}}{R_S}} = \frac{30V \cdot 100\mu F}{\frac{50mV}{0.2\Omega}} = 12ms$$

MOSFET power dissipation is:

$$P = \frac{\text{Energy in } C_{L+}}{t_{STARTUP}} = 3.75W$$

In foldback mode, this power is reduced further.

For IO-Link applications, another case to consider is the start-up current pulse (see L+ Supply Current Pulse Capability), in which a heavy nonlinear load could be supplied twice the normal current, or $2 \cdot \Delta V_{ACL}/R_S$, for up to 72ms. Again assuming 0.2Ω sense resistors and no benefit from foldback, average MOSFET power dissipation is:

$$P = \left[30V - \frac{(0V + 18V)}{2}\right] \cdot 0.5A = 3.0W$$

The SOA (safe operating area) curves of candidate MOSFETs must be evaluated to ensure that the heat capacity of the package tolerates the more extreme case, 3W for 72ms. The SOA curves of the Fairchild FQT7N10 provide for 350mA at 30V (>10W) for 100ms, satisfying this requirement.

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Power Considerations

The LTC2874 has two power supply pins: a logic supply pin (V_L) and the primary supply (V_{DD}). The V_L supply powers the control logic, serial interface and SPI registers, and allows the LTC2874 to interface with any logic signal from 2.9V to 5.5V. Bypass V_L to GND with at least a 0.1µF ceramic capacitor. There is no power supply sequencing requirement.

Bypass capacitance between V_{DD} and GND is important for reliable operation. If a short circuit occurs at one of the L+ output ports, it can take more than 20µs for the LTC2874 to begin regulating the current. During this time the current is limited only by minimal impedance, so a high current spike can cause a voltage transient on the V_{DD} supply with the possibility that the LTC2874 resets due to a UVLO fault. Decouple V_{DD} to ground with at least 100µF bulk capacitance and a 1µF, 100V X7R ceramic capacitor placed near the V_{DD} pin to minimize spurious resets.

Supply Monitors

The LTC2874 monitors various conditions on its two input power supplies, and alerts the host microcontroller when supply levels move outside of their operating range. Event bits record when the logic supply V_L has moved below its UVLO threshold or when the main supply V_{DD} has moved below its UVLO threshold, below its mode-dependent UV level, or above its programmable OV level (see Figure 23).

To provide immunity against supply voltage spikes, the V_{DD} event bits have a 10µs filter time. Status bits are live (no-delay) indicators.

Auto-Retry or Latchoff Fault Response

When a line output is shorted or the $\Delta V_{CB(TH)}$ threshold is otherwise exceeded, a timed circuit breaker disables the L+ power supply output or CQ driver before overheating can damage the MOSFET (L+) or master (CQ). Normally the LTC2874 periodically re-enables the pin to check if the fault condition is still present. The RETRYTC[2:0] register bits adjust the retry timer delay from 0.12s to 15.7s to allow for cooling.

Register bits RETRY_L+ and RETRY_CQ allow independent fault behavior for L+ and CQ pins. Set these bits high for auto-retry behavior and low for latchoff. Default behavior is auto-retry.

When configured for latchoff behavior, the LTC2874 disables the respective L+ or CQ pin until the overcurrent event bit is cleared. In this case, clearing the event register initiates a manual retry. The host is responsible for

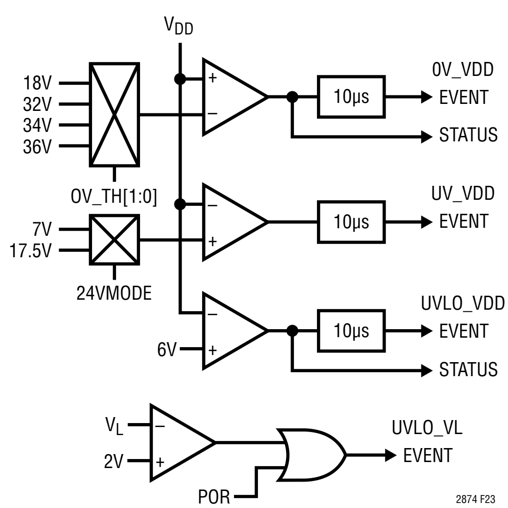

Figure 23. Supply UVLO, UV, and OV Monitors

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limiting the duty cycle of the fault condition. Choose retry (RETRYTC) and overcurrent timer (LPTC) settings in tandem to keep the duty cycle of an L+ fault condition sufficiently low to allow for cooling of the external MOSFET. In the case of a CQ fault condition, even the fastest RETRYTC setting limits the duty cycle to <1% to allow for cooling of one or more drivers. Examples of both responses to an L+ fault are shown in Figure 24 and Figure 25.

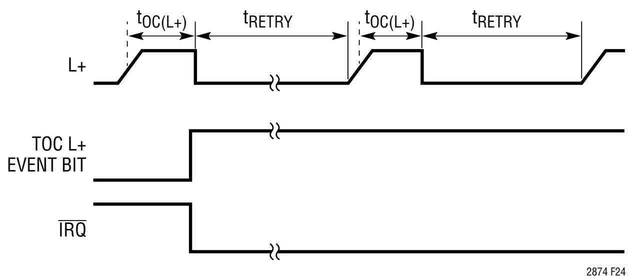

Figure 24. Auto-Retry Fault Behavior (for L+ Short)

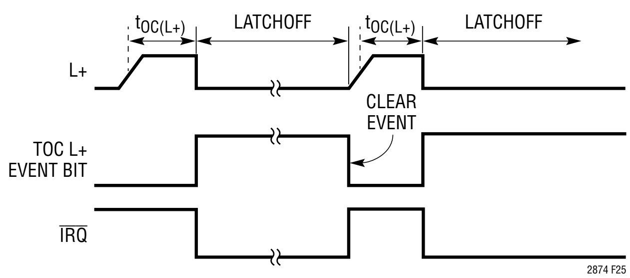

Figure 25. Latchoff Fault Behavior (for L+ Short)

The LTC2874 allows the response to V_{DD} supply overvoltage faults to be tailored with similar flexibility. Normally, this fault causes the L+ and CQ pins of all four ports to be disabled. The RETRY_OV bit selects between auto-retry and latchoff behavior. If the OV_ALLOW bit is set high, the LTC2874 will tolerate overvoltage conditions, signaling the event but not disabling any functions.

Auto-retry doesn't clear any event registers, nor does writing any event register bit high disable any function.

Start-Up Behavior

Both external supplies must exceed their undervoltage lockout levels for 10ms before the CQ and L+ outputs are allowed to turn on and before V_{DD} events are reported. During that settling interval, the RXD pins are Hi-Z. Figure 26 shows typical start-up behavior, assuming the V_{DD} supply is the last to power on.

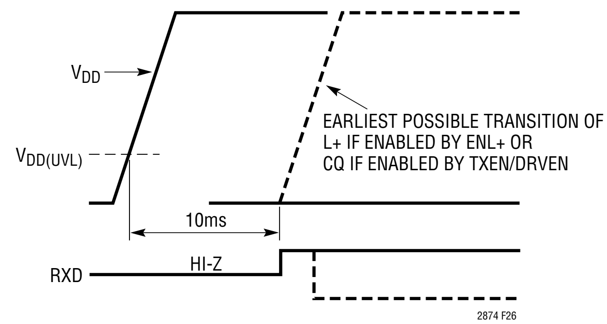

Figure 26. CQ or L+ Pin Start-Up Behavior

SPI Interface

The LTC2874 communicates with the host using a SPI-compatible 4-wire interface. Figure 9 and Figure 10 show typical communication waveforms and timing relationships. Interrupts are signaled to the host via the $\overline{IRQ}$ pin.

When the chip select input $\overline{CS}$ is set low, it enables the SCK input buffer and the SDO output. Data at the SDI pin is transferred into the shift register at subsequent rising SCK edges. For each 16-bit word, the command bits C2 to C0 are loaded first; then address bits A3 to A0; then a don't-care bit; and finally bits D7 to D0, which supply a byte of data (ordered MSB-to-LSB) for some commands. Data can be transferred to the LTC2874 only when $\overline{CS}$ is low.

SCK may be high or low at the falling edge of $\overline{CS}$. Keep SCK low between commands to ensure timely completion of all commands.

Commands and their formats are shown in Table 2. Command codes not shown are reserved and should not be used.

Table 2. LTC2874 Command List and Format

COMMAND	DETAIL	(FIRST) c2…c0	a3…a0	Bit-8	(LAST) d7…d0
READ	Read Register	000	AAAA	X	XXXXXXXX
WRITE	Write Register (No Update)	001	AAAA	X	DDDDDDDD
UPDATE	Update All Registers	010	XXXX	X	XXXXXXXX
WRTUPD	Write One Register and Update All	011	AAAA	X	DDDDDDDD
RESET	Reset	111	XXXX	X	XXXXXXXX

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SPI Write, Update, and WrtUpd Commands

Three of the commands relate to writing data to the registers. The write command transfers data from the shift register to the holding latches of any writable register. The update command transfers data from all holding latches to the SPI registers. The WrtUpd combines these two commands.

For the write and WrtUpd commands, data is transferred from the shift register on the 16th falling edge of SCK.

SPI Read Command

The read command transfers a byte of data from the holding latches of a SPI register to the serial output pin (SDO). Transitions occur on falling clock edges, allowing data to be sampled by the SPI master on the rising edges, beginning with the 8th SCK. When $\overline{CS}$ is low, the SDO pin is low except when a high register bit is being read out. When $\overline{CS}$ is high, SDO is Hi-Z.

COMMAND			SEQUENCE AT SDI PIN (FIRST) … (LAST)
RESET			1 1 1 0 0 0 0 0 0 0 0 0 0 0 0 0
WRITE	0x8	0x1F	0 0 1 1 0 0 0 0 0 0 0 1 1 1 1 1
WRITE	0x9	0xF0	0 0 1 1 0 0 1 0 1 1 1 1 0 0 0 0
WRITE	0xA	0x00	0 0 1 1 0 1 0 0 0 0 0 0 0 0 0 0
UPDATE			0 1 0 0 0 0 0 0 0 0 0 0 0 0 0 0
READ	0x0		0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

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Figure 27. Example SPI Commands

Data written to the internal data holding latches can be verified prior to committing data to the SPI registers by reading it before an update command is sent.

SPI Reset Command

The reset command returns default values to the SPI register and clears internal latches. It has no effect on the SPI data path itself. This command has sticky behavior, not releasing until a subsequent command (besides reset) is received.

Continuous Transfer Capability

Commonly for SPI communication, $\overline{CS}$ is asserted low once per command word. The LTC2874 also supports continuous transfer in which multiple command words, each accompanied by 16 SCK pulses, are grouped in a sequence (Figure 28). This feature is useful for software polling or writing to multiple registers. Keep $\overline{CS}$ low until after the last command word in the group.

Chip Select Addressing

Combine LTC2874 devices to build larger masters by assigning each its own $\overline{CS}$ and sharing the remaining SPI interface wires. See Figure 40.

SPI Registers

The LTC2874 has 15 registers for configuration and monitoring: seven for control, two for status, four to record events, and two to handle interrupts. Register bit assignments are summarized in Table 3.

When V_L is below approximately 2V, the SPI serial port resets to power-on states and registers are set to default values. The reset command similarly sets the registers to default values (with minor differences listed in the last column of Table 3) and resets internal control circuits.

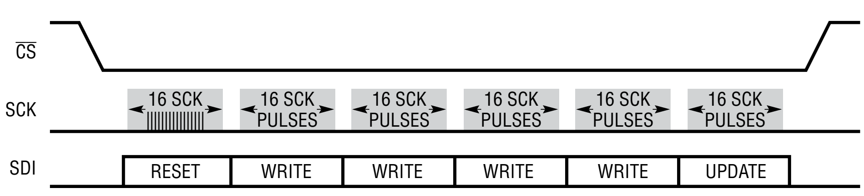

Figure 28. Continuous Transfer Capability

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Table 3. SPI Register Table

REG	NAME	D7	D6	D5	D4	D3	D2	D1	D0	DEFAULT
0x0	IRQREG (Read Only)	**OT** Overtemp Event Occurred	**SUPPLY** Supply Event Occurred	**WU** Wake-Up Event Occurred	**TOC_L+** L+ OC Timeout Event Occurred	**PWRCHNG** L+ Power Changed Event Occurred	**TOC_CQ** CQ OC Timeout Event Occurred	**CSENSE** Cable Sense Event Occurred	Reserved	0100,0000 (V_L-on Reset) 0000,0000 (SPI Reset)
0x1	IRQMASK	**OT** Overtemp IRQ Mask	**SUPPLY** Supply IRQ Mask	**WU** Wake-Up IRQ Mask	**TOC_L+** L+ OC Timeout IRQ Mask	**PWRCHNG** L+ Power Changed IRQ Mask	**TOC_CQ** CQ OC Timeout IRQ Mask	**CSENSE** Cable Sense IRQ Mask	Reserved	1111,1110
0x2	EVENT1	**OT_SD** Overtemp Shutdown Occurred	**OT_WARN** Overtemp Warning Occurred	Reserved	**UVLO_VL** V_L UVLO Event Occurred	**UVLO_VDD** V_{DD} UVLO Event Occurred	**UV_VDD** V_{DD} UV Event Occurred	**OV_VDD** V_{DD} OV Event Occurred	Reserved	0001,0000 (V_L-on Reset) 0000,0000 (SPI Reset)
0x3	EVENT2	**WU4** Wake-Up Event CQ4 Occurred	**WU3** Wake-Up Event CQ3 Occurred	**WU2** Wake-Up Event CQ2 Occurred	**WU1** Wake-Up Event CQ1 Occurred	**TOC_L+4** L+4 OC Timeout Event Occurred	**TOC_L+3** L+3 OC Timeout Event Occurred	**TOC_L+2** L+2 OC Timeout Event Occurred	**TOC_L+1** L+1 OC Timeout Event Occurred	0000,0000
0x4	EVENT3	**PWRCHNG4** L+4 Power Changed Event Occurred	**PWRCHNG3** L+3 Power Changed Event Occurred	**PWRCHNG2** L+2 Power Changed Event Occurred	**PWRCHNG1** L+1 Power Changed Event Occurred	**TOC_CQ4** CQ4 OC Timeout Event Occurred	**TOC_CQ3** CQ3 OC Timeout Event Occurred	**TOC_CQ2** CQ2 OC Timeout Event Occurred	**TOC_CQ1** CQ1 OC Timeout Event Occurred	0000,0000
0x5	EVENT4	**CQ_SNS4** CQ4 Sense: 0 = CQ High 1 = CQ Low	**CQ_SNS3** CQ3 Sense: 0 = CQ High 1 = CQ Low	**CQ_SNS2** CQ2 Sense: 0 = CQ High 1 = CQ Low	**CQ_SNS1** CQ1 Sense: 0 = CQ High 1 = CQ Low	**CSENSE4** L+4 Cable Sense Event Occurred	**CSENSE3** L+3 Cable Sense Event Occurred	**CSENSE2** L+2 Cable Sense Event Occurred	**CSENSE1** L+1 Cable Sense Event Occurred	0000,0000
0x6	STATUS1 (Read Only)	**OT** Over-temperature Condition	**WU_COOL** WURQ or Cooldown Condition	**UVLO_VDD** V_{DD} UVLO Condition	**OV_VDD** V_{DD} Over-voltage Condition	**OC_L+4** L+4 Over-current Condition	**OC_L+3** L+3 Over-current Condition	**OC_L+2** L+2 Over-current Condition	**OC_L+1** L+1 Over-current Condition	0000,0000
0x7	STATUS2 (Read Only)	**PWRGD4** L+4 Power Good	**PWRGD3** L+3 Power Good	**PWRGD2** L+2 Power Good	**PWRGD1** L+1 Power Good	**OC_CQ4** CQ4 Over-current Condition	**OC_CQ3** CQ3 Over-current Condition	**OC_CQ2** CQ2 Over-current Condition	**OC_CQ1** CQ1 Over-current Condition	0000,0000
0x8	MODE1	**24VMODE** Enable IO-Link Compatible Mode	**CSENSE_ MODE** Enable Cable Sense Mode	**2XPTC[1:0]** L+ Start-Up 2X Current Pulse Timer Control: 00 = 62ms 01 = Disabled 10 = 31ms 11 = 124ms		**FLDBK_ MODE** Enable Foldback Mode	**RETRY_OV** Enable V_{DD} OV Auto-Retry	**RETRY_L+** Enable L+ Pin Auto-Retry	**RETRY_CQ** Enable CQ Pin Auto-Retry	1000,1111
0x9	MODE2	**SLEW4** CQ4 Edge Rate: 0 = SLOW 1 = FAST	**SLEW3** CQ3 Edge Rate: 0 = SLOW 1 = FAST	**SLEW2** CQ2 Edge Rate: 0 = SLOW 1 = FAST	**SLEW1** CQ1 Edge Rate: 0 = SLOW 1 = FAST	**OV_TH[1:0]** V_{DD} Overvoltage Threshold Select: 00 = 18V 01 = 32V 10 = 34V 11 = 36V		**OV_ALLOW** Allow V_{DD} Overvoltage	**CQ_SNS_ MODE** Enable CQ Sense Mode	1111,0100

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Table 3. SPI Register Table

REG	NAME	D7	D6	D5	D4	D3	D2	D1	D0	DEFAULT
0xA	NSF	**NSF4[1:0]** Noise Suppression Filter, Port 4: 00 = Disabled 01 = 20.3µs 10 = 2.8µs 11 = 0.6µs		**NSF3[1:0]** Noise Suppression Filter, Port 3: 00 = Disabled 01 = 20.3µs 10 = 2.8µs 11 = 0.6µs		**NSF2[1:0]** Noise Suppression Filter, Port 2: 00 = Disabled 01 = 20.3µs 10 = 2.8µs 11 = 0.6µs		**NSF1[1:0]** Noise Suppression Filter, Port 1: 00 = Disabled 01 = 20.3µs 10 = 2.8µs 11 = 0.6µs		1111,1111
0xB	ILLM	**ILLM4[1:0]** Sinking Current, Port 4: 00 = 500kΩ 01 = 2.5mA 10 = 3.7mA 11 = 6.2mA		**ILLM3[1:0]** Sinking Current, Port 3: 00 = 500kΩ 01 = 2.5mA 10 = 3.7mA 11 = 6.2mA		**ILLM2[1:0]** Sinking Current, Port 2: 00 = 500kΩ 01 = 2.5mA 10 = 3.7mA 11 = 6.2mA		**ILLM1[1:0]** Sinking Current, Port 1: 00 = 500kΩ 01 = 2.5mA 10 = 3.7mA 11 = 6.2mA		1111,1111
0xC	TMRCTRL	**LPTC[3:0]** L+ Overcurrent Timer Control (Ports 1 to 4): 0000 = 15µs 1000 = 3.9ms 0001 = 30µs 1001 = 7.8ms 0010 = 60µs 1010 = 16ms 0011 = 120µs 1011 = 30ms 0100 = 0.24ms 1100 = 60ms 0101 = 0.5ms 1101 = 0.12s 0110 = 1.0ms 1110 = 0.25s 0111 = 2.0ms 1111 = 0.25s				Reserved	**RETRYTC[2:0]** Auto-Retry Timer Control (Ports 1 to 4): 000 = 0.12s 001 = 0.24s 010 = 0.5s 011 = 1.0s 100 = 2.0s 101 = 3.9s 110 = 7.9s 111 = 15.7s			1000, 0101
0xD	CTRL1	**WKUP4** Generate WURQ on CQ4	**WKUP3** Generate WURQ on CQ3	**WKUP2** Generate WURQ on CQ2	**WKUP1** Generate WURQ on CQ1	**DRVEN4** Enable CQ4 driver	**DRVEN3** Enable CQ3 driver	**DRVEN2** Enable CQ2 driver	**DRVEN1** Enable CQ1 driver	0000,0000
0xE	CTRL2	**ENL+4** Enable L+4 Power Supply	**ENL+3** Enable L+3 Power Supply	**ENL+2** Enable L+2 Power Supply	**ENL+1** Enable L+1 Power Supply	**SIO_MODE4** Enable CQ4 Standard IO Mode	**SIO_MODE3** Enable CQ3 Standard IO Mode	**SIO_MODE2** Enable CQ2 Standard IO Mode	**SIO_MODE1** Enable CQ1 Standard IO Mode	0000,0000

Notes:

1: Delays are typical unless otherwise noted.

2: Underlined settings are default values.

3: Gray shading indicates Read-Only register bits.

4: Register 0xD WKUP bits are pushbuttons that self-clear.

5: Reserved bits may be converted to features in a future release of the product.

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Table 4. Summary of LTC2874 Event Reporting

EVENT	EVENT REGISTER/ EVENT BITS	IRQREG MASK BIT	BEHAVIOR	NOTE
Overtemperature Shutdown Level	EVENT1 (0x2) OT_SD	7	Thermal Recovery	Temperature has reached shutdown level. L+ and CQ pins are disabled until condition clears.
Overtemperature Warning Level	EVENT1 (0x2) OT_WARN	7	Thermal Recovery	Temperature has reached warning level. Wake-up requests (WURQ) are blocked.
V_L Supply UVLO	EVENT1 (0x2) SUPPLY	6	10ms Recovery	V_L below UVLO threshold for 10µs.
V_{DD} Supply UVLO	EVENT1 (0x2) SUPPLY	6	10ms Recovery	V_{DD} below UVLO threshold for 10µs.
V_{DD} Supply UV	EVENT1 (0x2) SUPPLY	6	Signal Event Only	V_{DD} below UV threshold for 10µs.
V_{DD} Supply OV	EVENT1 (0x2) SUPPLY	6	Latchoff or Auto-Retry	V_{DD} above OV threshold for 10µs. L+ and CQ pins are disabled unless OV_ALLOW bit set.
Wake-Up	EVENT2 (0x3) WU	5	8.3ms Wait	Wake-up request (WURQ) has started. Additional WURQs are blocked for 8.3ms.
L+ Overcurrent Timeout	EVENT2 (0x3) TOC_L+	4	Latchoff or Auto-Retry	Duration of L+ current limiting has exceeded programmable timeout.
L+ Power Changed	EVENT3 (0x4) PWRCHNG	3	Signal Event Only	L+ power status has changed (10µs filter).
CQ Overcurrent Timeout	EVENT3 (0x4) TOC_CQ	2	Latchoff or Auto-Retry	Duration of current limiting has exceeded mode-dependent timeout.
CQ Sense	EVENT4 (0x5) CQ_SNS	n/a	CQ Receiver Output (Read Only)	Indicates CQ level (inverted polarity like RXD) when CQ_SNS_MODE bit set high. Doesn't signal $\overline{IRQ}$.
Cable Sense	EVENT4 (0x5) CSENSE	1	L+ Supply Turns On	Signals cable or load detected when CSENSE_MODE bit set high.

APPLICATIONS INFORMATION

Event Signaling

When an event bit is set, in most cases a bit corresponding to the event type also signals high in the IRQREG register (0x0). If the corresponding bit in the IRQMASK register (0x1) is high, the event causes the $\overline{IRQ}$ pin to pull low. The $\overline{IRQ}$ signal generates an interrupt to the host microcontroller, eliminating the need for continuous software polling. The IRQMASK register selects which events can gain the host's attention at a given time.

SPI Receiver

The serial interface monitors the CQ line interface pins if the CQ_SNS_MODE bit is set. The polarity of the four CQ_SNS bits matches the polarity of the RXD pins. These bits are reset low when CQ_SNS_MODE isn't enabled (default).

Driving Light Bulbs

The CQ drivers can safely drive small incandescent light bulbs. Use SIO mode (SIOMODE = 1) and the fastest autoretry delay (RETRY_CQ = 1, RETRYTC = 0x0). The drivers will pulse on and off while the filament initially draws high current as it heats up. Figure 29 shows typical waveforms.

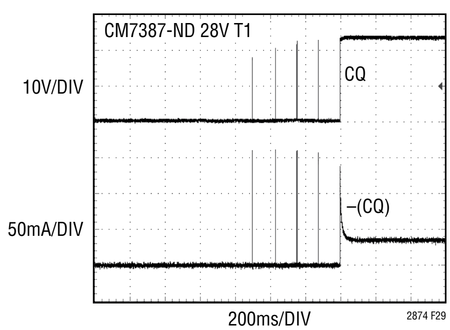

Figure 29. Driving an Incandescent Bulb Using SIO Mode and Auto-Retry

Larger light bulbs can be driven if microcode defines a faster driver cooling interval between pulses during bulb ignition. Set RETRY_CQ = 0 and clear register 0x4 to begin each new pulse. Because this technique defeats built-in protection against driver self-heating, it must be applied carefully.

Driving Relays

Having 100mA drive capability, the CQ drivers are capable of energizing the coils of many relays. For some applications requiring higher current, the L+ lines may operate as low data rate outputs. Figure 39 shows an example of the L+ pins driving 0.5A relays, with the CQ lines connected as relay sense lines. CQ line drivers are disabled by pin-strapping TXEN1 through TXEN4 low, and CQ pin load currents are disabled by setting ILLM = 0x0 for each port. Activate any relay by setting its ENL+ bit high. The relay sense points are converted to logic levels at the RXD pins. If the CQ_SNS_MODE bit is set high, the sense points may be read from register 0x5 via the serial interface.

IO-Link Compatible Operation

Table 5 shows typical register settings for IO-Link compatible operation.

Setting the 24VMODE bit high programs the receivers and L^+ foldback for 24V operation per Figures 12 and 15.

Table 5. Example Settings for IO-Link Compatibility

REG	VALUE	DEFAULT	NOTE
0x8	0x8F	Y	IO-Link Compatibility Mode Enabled; L+ Startup 2x Current Pulse Enabled
0x9	0xF4	Y	32V V_{DD} Overvoltage Threshold
0xA	0xFF	Y	0.5µs Noise Suppression Filters
0xB	0xFF	Y	6mA Sinking Currents
0xC	0x85	Y	TOC_L+ Timer NOT Required to be Set Longer Than 62ms Startup Current Pulse

Applications Other than IO-Link

Table 6 shows typical SPI register settings for operating the LTC2874 in a 12V application.

Setting the 24VMODE bit low selects V_{DD}-ratioed receiver thresholds (Figure 12) and L+ foldback optimized for 12V operation (Figure 15). Additionally, the WKUP register bits are deactivated.

Table 6. Example Settings for 12V Application

REG	VALUE	DEFAULT	NOTE
0x8	0x5F	N	IO-Link Compatibility Mode Disabled; L+ Start-Up 2x Current Pulse Disabled
0x9	0xF0	N	18V V_{DD} Overvoltage Threshold
0xA	See Note	–	Noise Suppression Filtering as Needed
0xB	0x00	N	Sinking Currents Disabled

APPLICATIONS INFORMATION

Reverse Current Protection

To isolate the V_{DD} input supply against reverse current from L+ outputs and isolate L+ pins against cable disturbances on other L+ outputs, use the approach shown with diodes D1 through D4 in Figure 30. Locate the diodes on the MOSFET drains rather than sources to avoid reducing the MOSFET V_{GS}.

Surge and ESD Protection Considerations

Cable interfaces are subject to significant ESD events because long cables can store large reservoirs of charge. The LTC2874 CQ and L+ line pins feature protection to ±8kV HBM with respect to GND without latchup or damage during all modes of operation and while unpowered. All the other pins are protected to ±6kV HBM.

In order to further protect the LTC2874 interface ports against surge and contact/air discharge events based on the IEC 61000-4-5 standard, additional external protection is required.

SM6T36A or equivalent TVS clamps are recommended for IO-Link and most other applications. In 24V applications in which the input supply tolerance does not exceed 15%, SM6T33A or equivalent clamps are also suitable.

Figure 30 shows the placement of TVS diodes for protecting the L+ outputs, while Figure 31 shows how to protect the CQ pins.

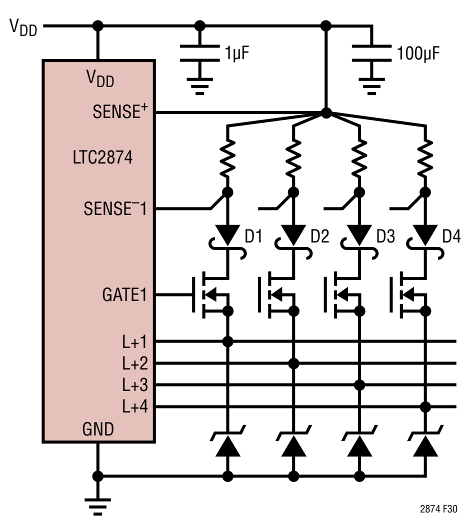

Figure 30. Reverse Protection and TVS Diode Protection for L+ Outputs

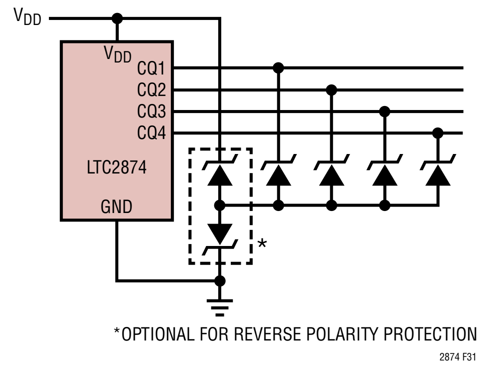

Figure 31. TVS Diode Protection for CQ pins

MOSFET Fault Detection

The L+ supply outputs are designed to tolerate significant levels of abuse, but in extreme cases it is possible for the external MOSFET to be damaged. A failed MOSFET may short from source to drain, which will make the port appear to be on when it should be off. The LTC2874 will disable the port if an overcurrent timeout occurs.

A failed MOSFET may also short from gate to source. This type of short will prevent the LTC2874 from enhancing the MOSFET. The host can detect this condition by the permanent absence of PWRGD. An open or missing MOSFET will similarly not produce PWRGD.

Normally a damaged MOSFET will not affect other ports. However, if it causes the sense resistor R_S to fuse open, the $SENSE^-$ pin will exceed its absolute maximum rating, which might damage the LTC2874. This condition is signalled to the host by an OC_L+ status bit that remains high even when the supply output is disabled (ENL+ = 0). Avoid this situation by performing adequate board-level short circuit testing and using surge-rated sense resistors.

High Temperature Considerations

For some applications, the PCB must provide heat sinking to keep the LTC2874 cool. Solder the exposed pad on the bottom of the package to ground and tie to large copper layers below using thermal vias.

LTC2874 power dissipation can be estimated by considering the contributions of drivers and sinking currents for a given application, along with quiescent power dissipated by internal circuits operating from two supplies. In general, use the higher case of drive mode and receive mode

APPLICATIONS INFORMATION

(sinking current) and ignore the other. Calculate driver power dissipation by taking the product of CQ residual voltage and load current for each port. Here we also factor in worst-case limits and maximum possible DC loading on all ports:

$$PD = 4 \bullet MAX((I_{LL} \bullet V_{DD}), (I_{RQH/L} \bullet V_{RQH/L})) + (V_{DD} \bullet I_{DD}) + (V_L \bullet I_L)$$

$$PD = 4 \bullet MAX((6.8mA \bullet 30V), (0.23A \bullet 1.6V)) + (30V \bullet 8mA) + (5.5V \bullet 1mA) = 1.7W$$

For θ_{JA} of 34°C/W, the increase in junction temperature compared to ambient is 51°C.

The thermal shutdown circuit signals an OT_SD event and disables the drivers if the internal die temperature is above about 170°C. The drivers turn back on when the internal die temperature drops approximately 15°C.

When the internal die temperature is above about 140°C, the OT status bit and OT_WARN event bit signal, enabling an informed host to intervene.

Layout Guidelines

Standard power layout guidelines apply to the LTC2874: place the decoupling caps for the V_{DD} and V_L supplies near their respective supply pins, use ground planes, and use wide traces wherever there are significant currents.

The main layout challenge involves the arrangement of the current sense resistors, and their connections to the LTC2874. Because the sense resistor values are small, layout parasitics can cause significant errors. Care is required to achieve specified accuracy.

Figure 32 illustrates the problem. In example Figure 32A, two ports have load currents I_1 and I_2 that connect to V_{DD} through a mutual resistance R_M. R_M represents the combined resistances of any traces, planes, and vias in the PCB that I_1 and I_2 share. The LTC2874 measures the voltage difference between its SENSE+ and SENSE– pins to sense the voltage drop across R_{S1}, but as the example shows, R_M introduces errors.

The second example (Figure 32B) shows how to minimize errors using good layout. The circuit is rearranged so that R_M no longer affects V_S, and the SENSE+ connection to the LTC2874 is used as a Kelvin sense trace. It is not a perfect Kelvin connection because all four ports controlled by the LTC2874 share the same sense trace, and because the current through the trace (I_K) is not zero. However, as the equation in Figure 32(B) shows, the remaining error is a small offset term.

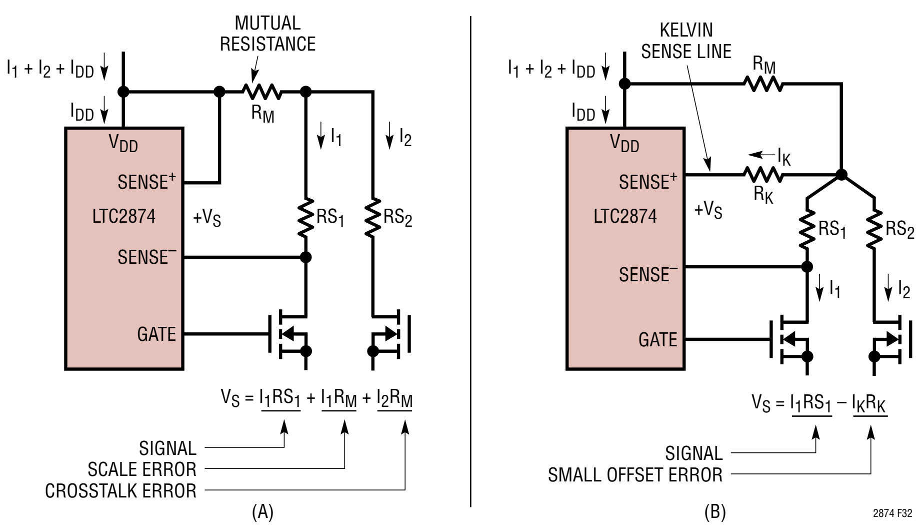

Figure 32. Layout Affects Current Limit Accuracy: (A) Poor and (B) Good Layouts

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Figure 33 shows two LTC2874 chips controlling eight ports (A through H). The ports are separated into two groups of four; each has its own trace on the top PCB layer that connects to the V_{DD} plane through a via. Currents from the U1 sub-circuit are effectively isolated from the U2 subcircuit, reducing the layout problem down to 4-port subsections; this arrangement can be expanded for any number of ports.

Figure 34 shows an example of good 4-port layout. In this case, each sense resistor consists of two resistors in parallel. The four groups of resistors are arranged to minimize the overlap in their current flows, reducing mutual resistance. Wide copper paths connect each group of resistors to the vias at the center.

The $SENSE^+$ Kelvin trace connects to the center of the resistor array. The via at the center of the sense resistor array has a matching hole in the V_{DD} plane. This arrangement prevents the mutual resistance of the four large vias from influencing the current measurements and introducing errors. An alternative layout is shown in Figure 35.

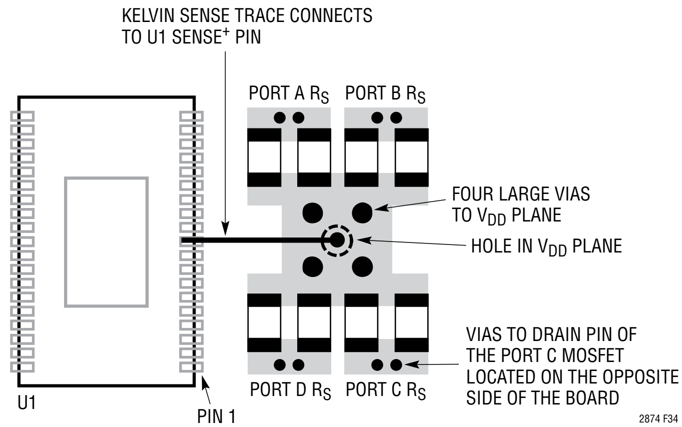


Figure 34. Good PCB Layout Example

IO-Link Disclaimer

Linear Technology Corporation attempts to maintain compatibility with the IO-Link interface and system specification. LTC is not a member of the IO-Link Consortium as set forth by PROFIBUS Nutzeroganisation (PNO) e.V.

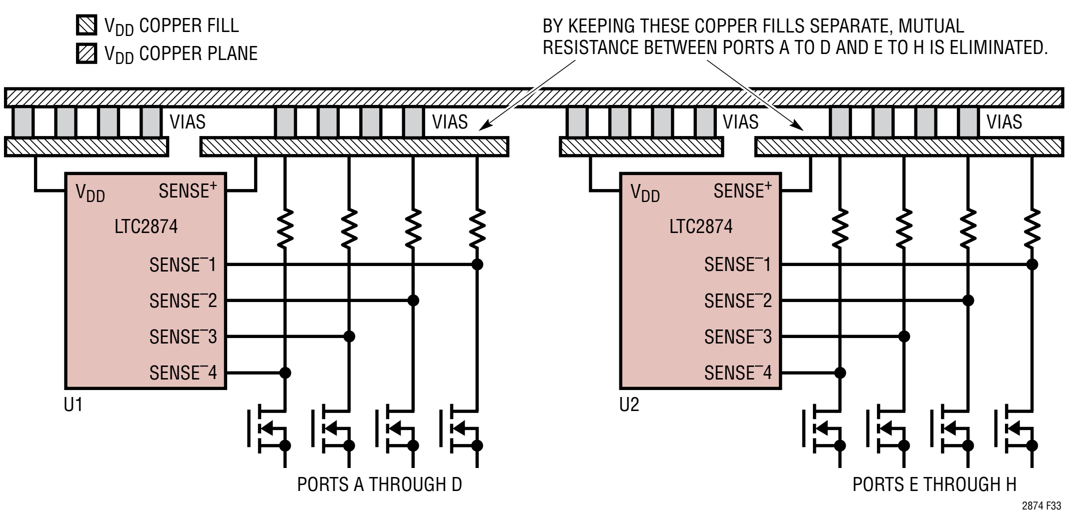
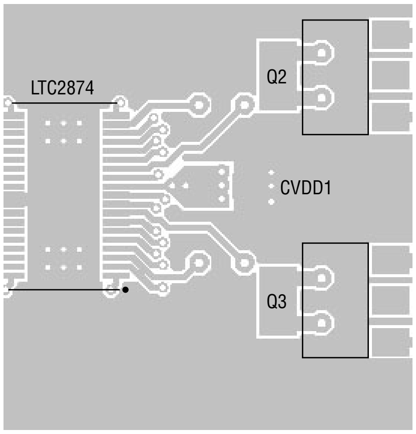
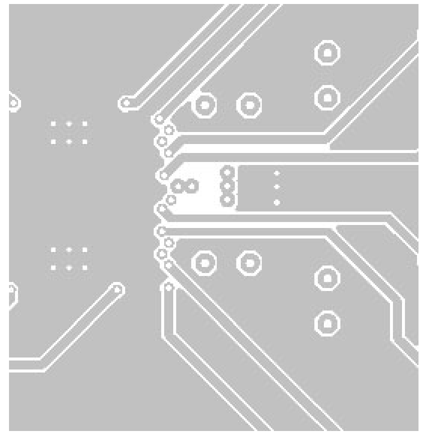


Figure 33. Layout Strategy to Reduce Mutual Resistance

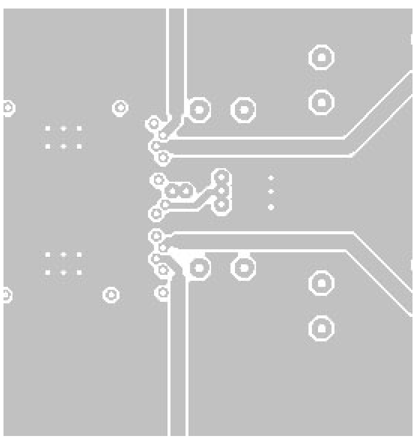
APPLICATIONS INFORMATION



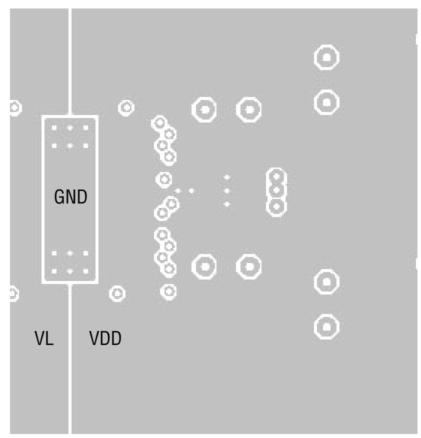
A. Top Layer



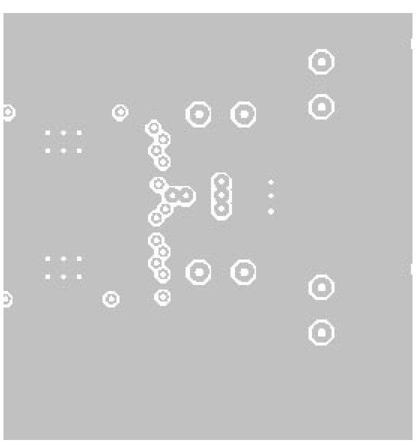
B. Inner Layer 2



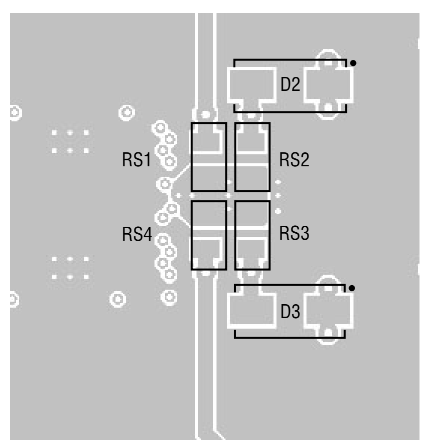
C. Inner Layer 3



D. Inner Layer 4



E. Inner Layer 5



F. Bottom Layer

Figure 35. Demo Board DC1880A Layout Showing Sense Resistors (on Bottom Layer) and Two of Four MOSFETs

TYPICAL APPLICATIONS

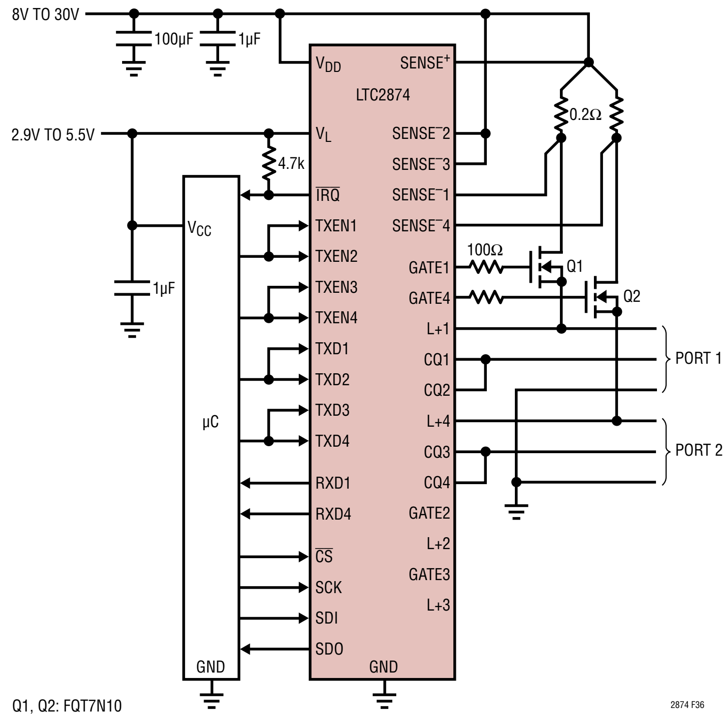


Figure 36. 2-Port Configuration with Guaranteed 200mA CQ Drive Capability (and 200mA L+ Supply)

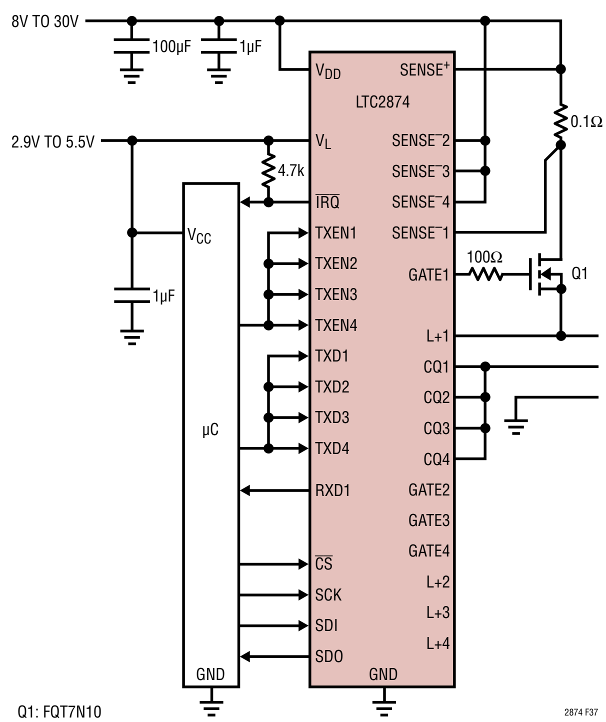


Figure 37. 1-Port Configuration with Guaranteed 400mA CQ Drive Capability (and 400mA L+ Supply)

TYPICAL APPLICATIONS

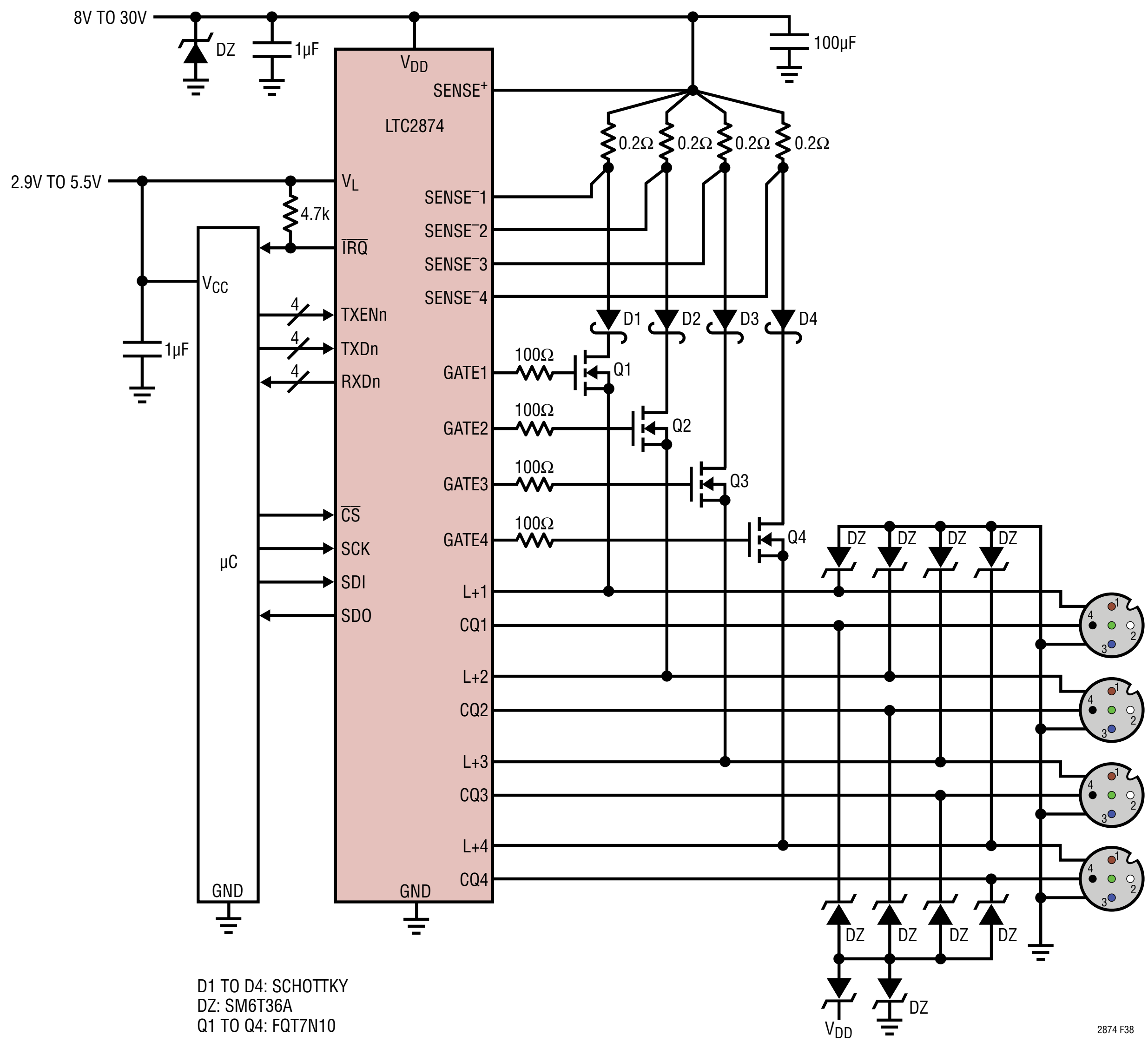


Figure 38. Diodes Reverse-Protect V_{DD} Supply (and TVS Diodes Surge-Protect Line Interface)

TYPICAL APPLICATIONS

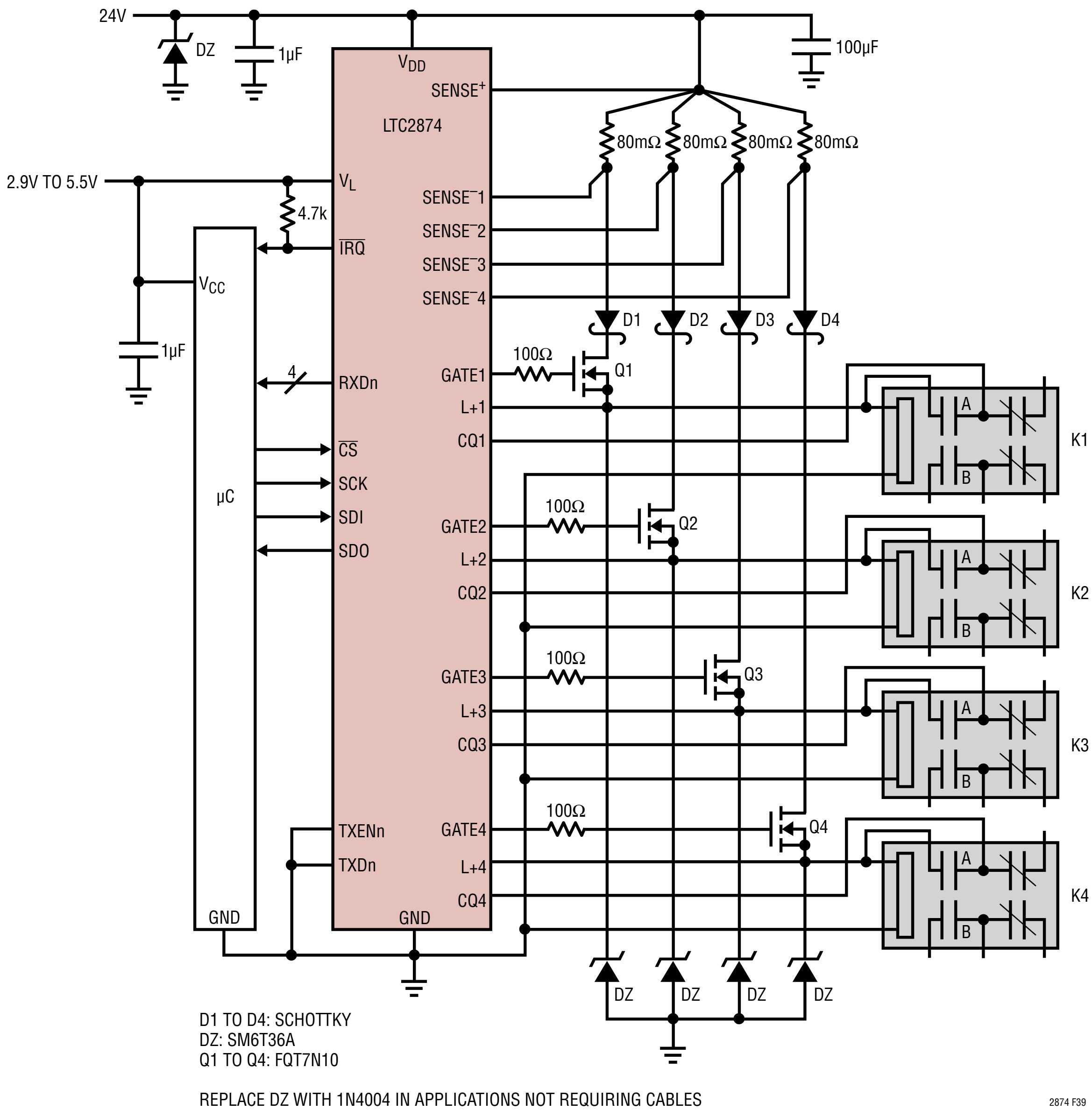


Figure 39. SPI-Operated Quad Relay Driver (with CQ Relay Sense) Guaranteeing 0.5A Coil Current

TYPICAL APPLICATIONS

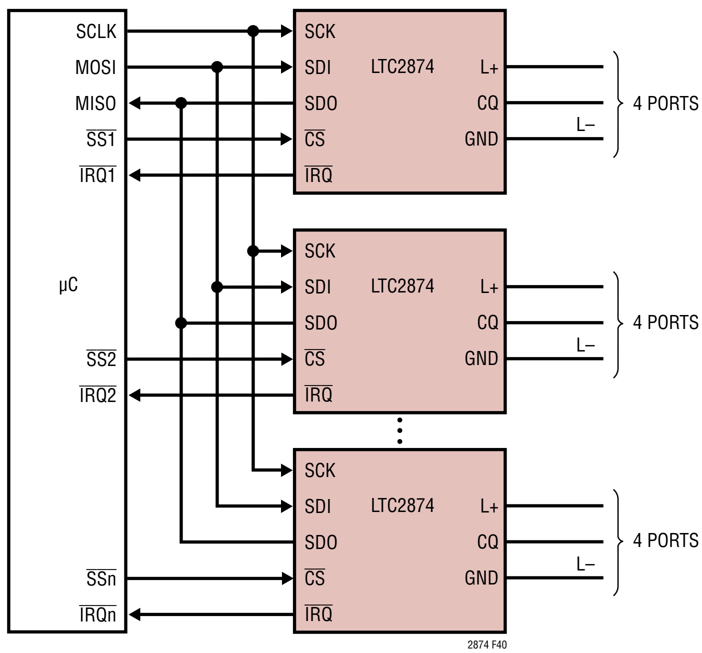
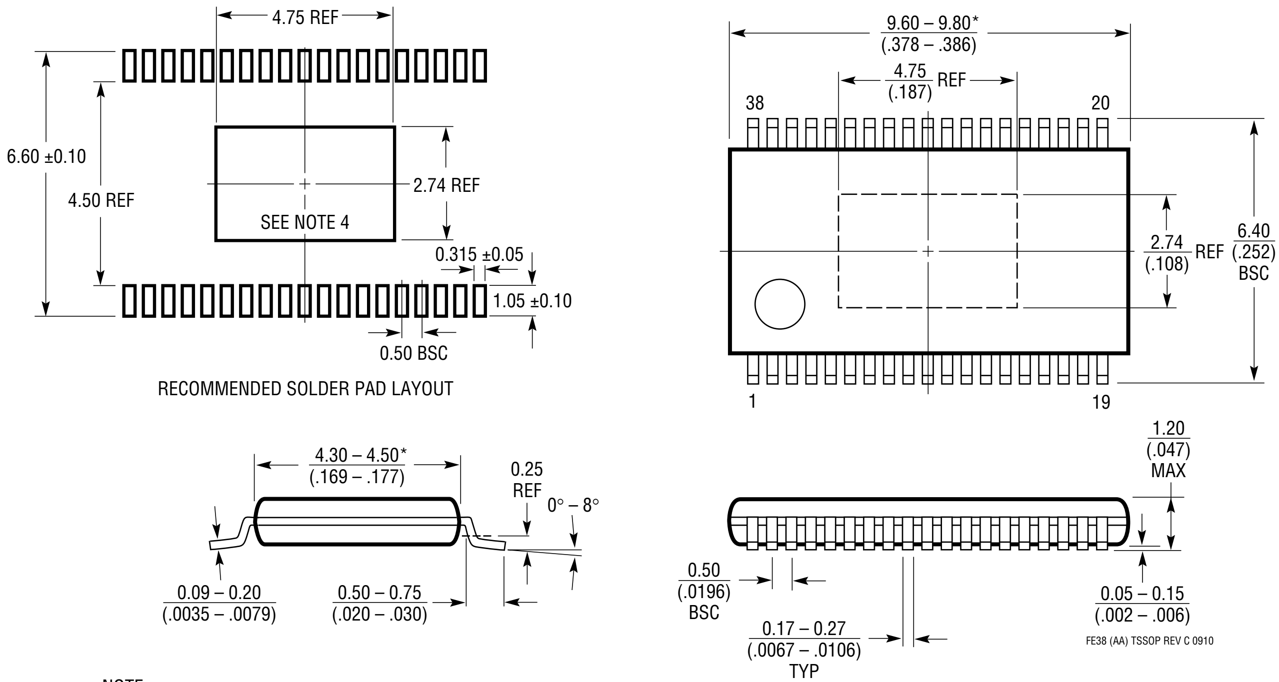


Figure 40. N-Port Master Hot Swap Controller and PHY

PACKAGE DESCRIPTION

Please refer to http://www.linear.com/designtools/packaging/ for the most recent package drawings.

FE Package
38-Lead Plastic TSSOP (4.4mm)
(Reference LTC DWG # 05-08-1772 Rev C)
Exposed Pad Variation AA



NOTE:
1. CONTROLLING DIMENSION: MILLIMETERS
2. DIMENSIONS ARE IN MILLIMETERS / (INCHES)
3. DRAWING NOT TO SCALE
4. RECOMMENDED MINIMUM PCB METAL SIZE FOR EXPOSED PAD ATTACHMENT

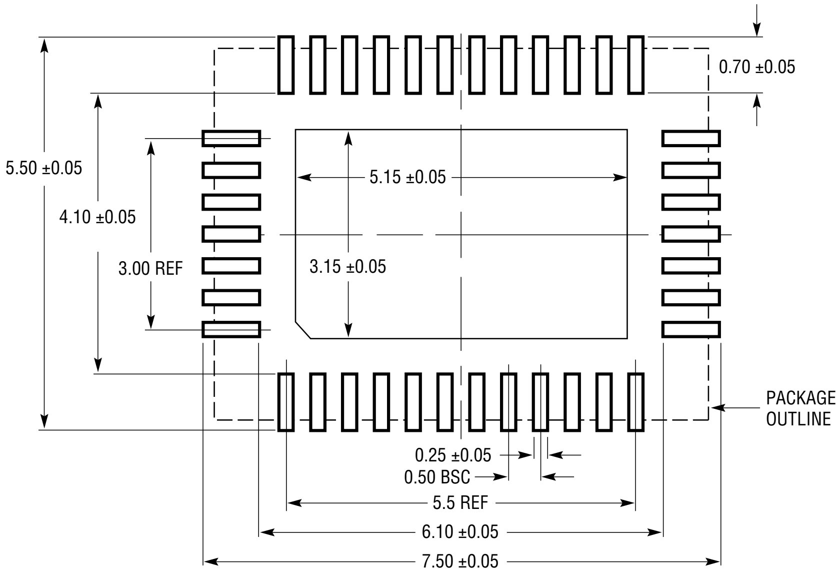
*DIMENSIONS DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.150mm (.006") PER SIDE

2874f

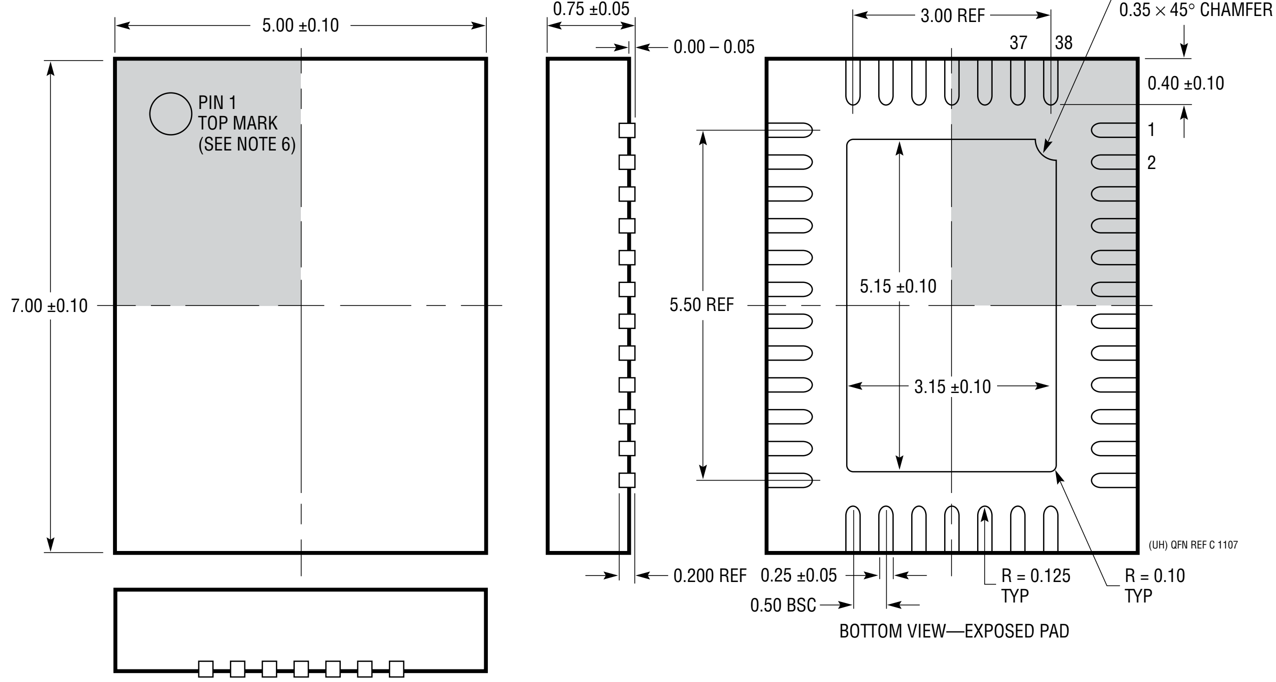
PACKAGE DESCRIPTION

Please refer to http://www.linear.com/designtools/packaging/ for the most recent package drawings.

UHF Package
38-Lead Plastic QFN (5mm × 7mm)
(Reference LTC DWG # 05-08-1701 Rev C)



RECOMMENDED SOLDER PAD LAYOUT
APPLY SOLDER MASK TO AREAS THAT ARE NOT SOLDERED

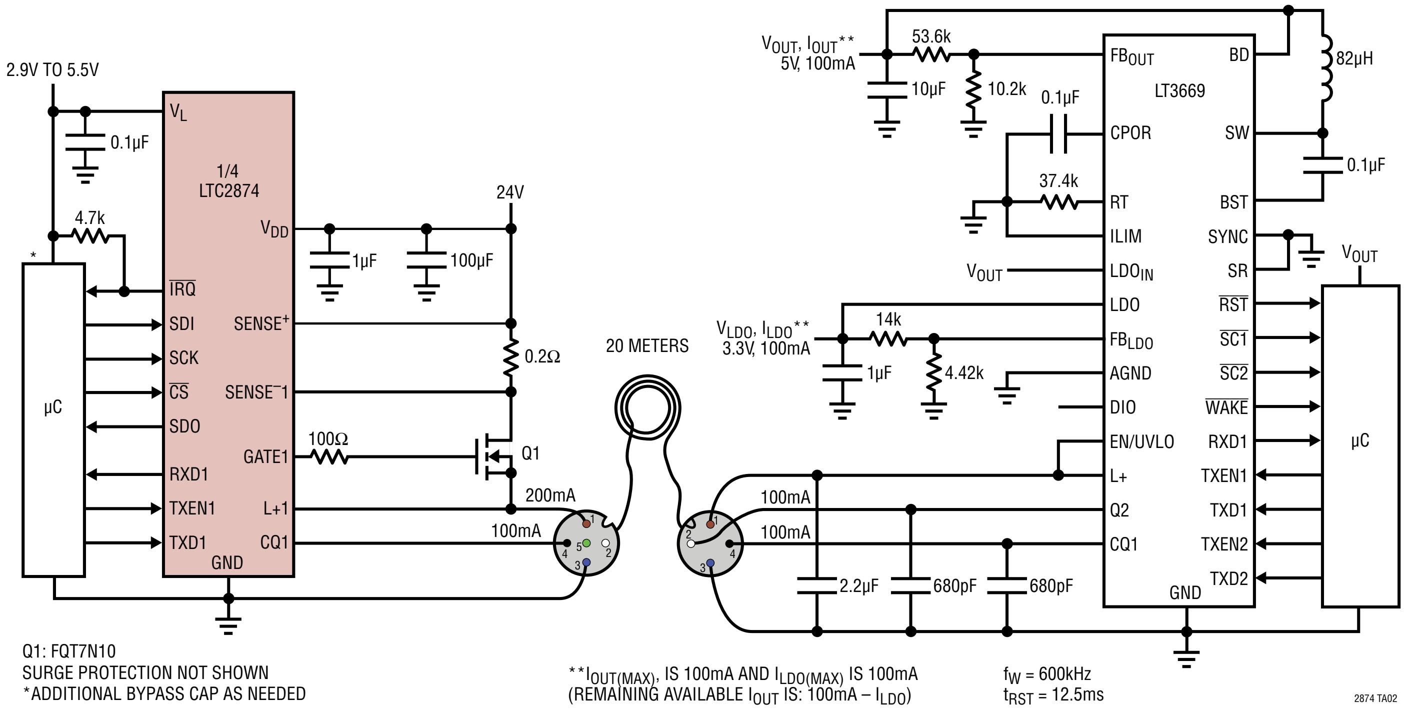


BOTTOM VIEW—EXPOSED PAD

NOTE:
1. DRAWING CONFORMS TO JEDEC PACKAGE OUTLINE M0-220 VARIATION WHKD
2. DRAWING NOT TO SCALE
3. ALL DIMENSIONS ARE IN MILLIMETERS
4. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.20mm ON ANY SIDE
5. EXPOSED PAD SHALL BE SOLDER PLATED
6. SHADED AREA IS ONLY A REFERENCE FOR PIN 1 LOCATION ON THE TOP AND BOTTOM OF PACKAGE

TYPICAL APPLICATION

Complete 24V 3-Wire Power and Signaling Interface to Sensor or Actuator (One of Four Available Master Ports is Shown)



RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LT3669/LT3669-2	Industrial Transceivers with Integrated Step Down Regulator and LDO	Compatible with IO-Link Communication Standard, Operates from 7.5V to 40V, Integrated 100mA/300mA Buck and 150mA LDO, 28-Lead (4mm × 5mm) QFN
LTC2854/LTC2855	3.3V 20Mbps RS485 Transceivers with Integrated Switchable Termination	3.3V Supply, Integrated, Switchable 120Ω Termination Resistor, ±25kV ESD
LTC2859/LTC2861	20Mbps RS485 Transceivers with Integrated Switchable Termination	5V Supply, Integrated, Switchable 120Ω Termination Resistor, ±15kV ESD
LTC2862/LTC2865	±60V Fault Protected 3V to 5.5V RS485/RS422 Transceivers	20Mbps, Protected from Overvoltage Line Faults to ±60V, ±15kV ESD
LTC2870/LTC2871/LTC2872	RS232/RS485 Multiprotocol Transceivers with Integrated Termination	3V to 5.5V Supply, Automatic Selection of Termination Resistors, Duplex Control, Logic Supply Pin, Up to ±26kV ESD
LTM2881	Complete Isolated RS485/RS422 μModule® Transceiver + Power	3V or 5V Supply, 20Mbps, 2500V_{RMS} Isolation with Integrated DC/DC Converter, Integrated Switchable 120Ω Termination Resistor, ±15kV ESD
LTM2882	Dual Isolated RS232 μModule Transceiver + Power	3V or 5V Supply, 1Mbps, 2500V_{RMS} Isolation with Integrated DC/DC Converter, ±10kV ESD

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