20V, 350mA, Rail-to-Rail Operational Amplifier

General Description

The RT9148/9 consists of a low power, high slew rate, single supply rail-to-rail input and output operational amplifier. The RT9148 contains a single amplifier and RT9149 contains two amplifiers in one package.

The RT9148/9 has a high slew rate (35V/μs), 350mA peak output current and offset voltage below 15mV. The RT9148/9 is ideal for Thin Film Transistor Liquid Crystal Displays (TFT-LCD).

The RT9148 is available in the WDFN-6L 2x2, TSOT-23-5 and UDFN-6L 2x2 packages. The RT9149 is available in the WDFN-8L 3x3 package. The RT9148/9 are specified for operation over the full temperature range from –40°C to 85°C.

Features

- **Rail-to-Rail Output Swing**
- **Supply Voltage : 6V to 20V**
- **Peak Output Current : 350mA**
- **High Slew Rate : 35V/μs**
- **Unity Gain Stable**
- **RoHS Compliant and Halogen Free**

Applications

- TFT LCD Panels
- Notebook Computers
- Monitors
- LCD TVs

Marking Information

RT9148ZQW

0EW

0E : Product Code
W : Date Code

RT9148GJ5

00=DNN

00 : Product Code
DNN : Date Code

RT9148GQU

2DW

2D : Product Code
W : Date Code

RT9149ZQW

86 YM
DNN

86 : Product Code
YMDNN : Date Code

Ordering Information

RT9148 □□
- Package Type
  QW : WDFN-6L 2x2 (W-Type)
- Lead Plating System
  Z : ECO (Ecological Element with Halogen Free and Pb free)

RT9148 □□
- Package Type
  J5 : TSOT-23-5
  QU : UDFN-6L 2x2 (U-Type)
- Lead Plating System
  G : Green (Halogen Free and Pb Free)

RT9149 □□
- Package Type
  QW : WDFN-8L 3x3 (W-Type)
- Lead Plating System
  Z : ECO (Ecological Element with Halogen Free and Pb free)

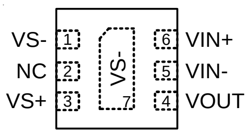
Note :

Richtek products are :

- RoHS compliant and compatible with the current requirements of IPC/JEDEC J-STD-020.
- Suitable for use in SnPb or Pb-free soldering processes.

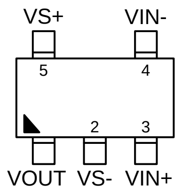
Pin Configurations

(TOP VIEW)



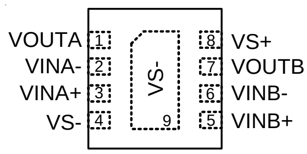
WDFN-6L 2x2 / UDFN-6L 2x2

RT9148



TSOT-23-5

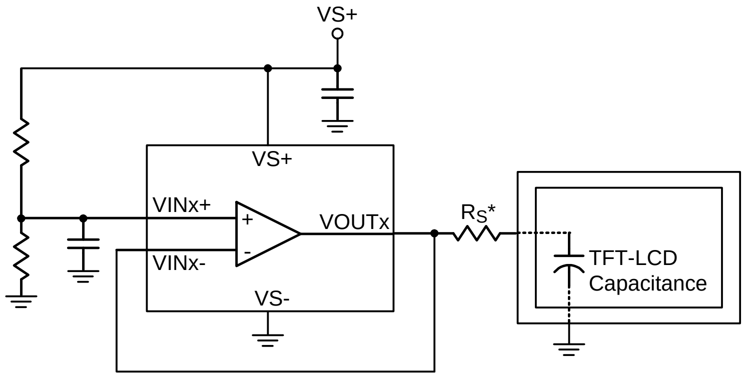
RT9148



WDFN-8L 3x3

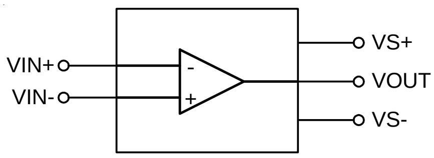
RT9149

Typical Application Circuit



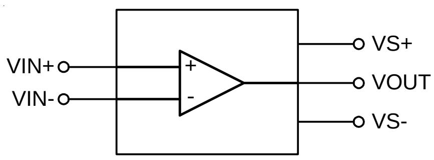
* : R_S may be needed for some applications.

Function Block Diagram



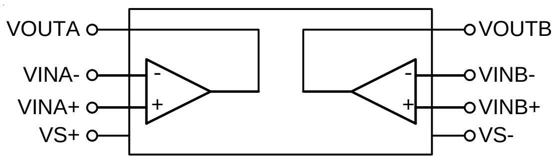
WDFN-6L 2x2 / UDFN-6L 2x2

RT9148



TSOT-23-5

RT9148



WDFN-8L 3x3

RT9149

Functional Pin Description

RT9148

Pin No.		Pin Name	Pin Function
WDFN-6L 2x2, UDFN-6L 2x2	TSOT-23-5		
1, 7 (Exposed Pad)	2	VS–	Negative Supply Input.
2	--	NC	No Internal Connection.
3	5	VS+	Positive Supply Input.
4	1	VOUT	Output.
5	4	VIN–	Negative Input.
6	3	VIN+	Positive Input.

RT9149

Pin No.	Pin Name	Pin Function
1	VOUTA	Output of Amplifier A.
2	VINA–	Negative Input of Amplifier A.
3	VINA+	Positive Input of Amplifier A.
4, 9 (Exposed Pad)	VS–	Negative Supply Input.
5	VINB+	Positive Input of Amplifier B.
6	VINB–	Negative Input of Amplifier B.
7	VOUTB	Output of Amplifier B.
8	VS+	Positive Supply Input.

Absolute Maximum Ratings (Note 1)

- Supply Voltage, (VS+ to VS–) ---------- 24V
- VINx+, VINx– to VS– ---------- –0.3V to 24V
- VINx+ to VINx– ---------- ±5V
- Power Dissipation, P_D @ T_A = 25°C
  - WDFN-6L 2x2 ---------- 2.1W
  - TSOT-23-5 ---------- 0.43W
  - UDFN-6L 2x2 ---------- 2.09W
  - WDFN-8L 3x3 ---------- 3.22W
- Package Thermal Resistance (Note 2)
  - WDFN-6L 2x2, θ_{JA} ---------- 47.5°C/W
  - TSOT-23-5, θ_{JA} ---------- 230.6°C/W
  - UDFN-6L 2x2, θ_{JA} ---------- 47.7°C/W
  - WDFN-8L 3x3, θ_{JA} ---------- 31°C/W
  - WDFN-8L 3x3, θ_{JC} ---------- 8°C/W
- Lead Temperature (Soldering, 10 sec.) ---------- 260°C
- Junction Temperature ---------- 150°C
- Storage Temperature Range ---------- –65°C to 150°C
- ESD Susceptibility (Note 3)
  - HBM (Human Body Model) ---------- 2kV
  - MM (Machine Model) ---------- 200V

Recommended Operating Conditions (Note 4)

- Supply Voltage, VS– = 0V, VS+ ---------- 6V to 20V
- Junction Temperature Range ---------- –40°C to 125°C
- Ambient Temperature Range ---------- –40°C to 85°C

Electrical Characteristics

(V_{S+} = 16V, V_{S-} = 0V, V_{INx+} = V_{OUTx} = V_{S+} / 2, R_L = 10kΩ and C_L = 10pF, T_A = 25°C, unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Input Characteristics						
Input Offset Voltage	V_{OS}	$V_{CM} = V_{S+} / 2$	--	2	15	mV
Input Bias Current	I_B	$V_{CM} = V_{S+} / 2$	--	2	50	nA
Load Regulation	ΔV_{LOAD}	I_L = 0 to –80mA	--	0.1	--	mV/mA
		I_L = 0 to 80mA	--	–0.1	--	
Common Mode Input Range	CMIR		0.5	--	V_{S+} –0.5	V
Common Mode Rejection Ratio	CMRR	$0.5V \le V_{OUTx} \le V_{S+} - 0.5V$	--	95	--	dB
Open Loop Gain	A_{VOL}	$0.5V \le V_{OUTx} \le V_{S+} - 0.5V$	--	118	--	dB

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Output Characteristics						
Output Swing Low	V_{OL}	I_L = –50mA	--	0.6	1.5	V
Output Swing High	V_{OH}	I_L = 50mA	V_{S+} –1.5	V_{S+} –0.3	--	V
Transient Peak Output Current	I_{PK}		300	350	400	mA
Power Supply						
Power Supply Rejection Ratio	PSRR	V_{S+} = 6V to 20V, V_{CM} = V_{OUTx} = V_{S+} / 2	--	96	--	dB
Quiescent Current	I_{DD}	No Load	--	4	--	mA
Dynamic Performance						
Slew Rate	SR	4V step, 20% to 80%, A_V = 1	--	35	--	V/μs
Setting to ±0.1% (AV = 1)	t_S	A_V = 1, V_{OUTx} = 2V step R_L = 10kΩ, C_L = 10pF	--	270	--	ns
–3dB Bandwidth	BW	R_L = 10kΩ, C_L = 10pF	--	16	--	MHz
Gain-Bandwidth Product	GBWP	R_L = 10kΩ, C_L = 10pF	--	12	--	MHz
Phase Margin	PM	R_L = 10kΩ, C_L = 10pF	--	50°	--	--

Note 1. Stresses beyond those listed "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions may affect device reliability.

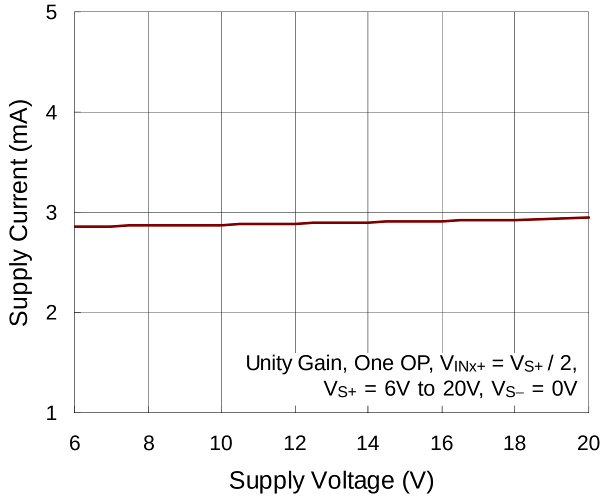
Note 2. θ_{JA} is measured at T_A = 25°C on a high effective thermal conductivity four-layer test board per JEDEC 51-7. θ_{JC} is measured at the exposed pad of the package.

Note 3. Devices are ESD sensitive. Handling precaution is recommended.

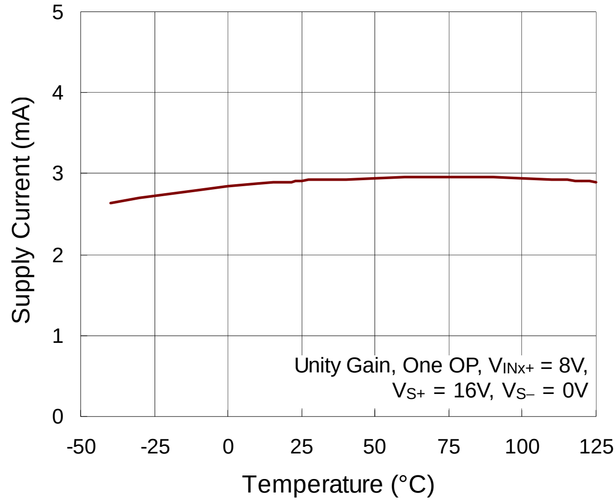
Note 4. The device is not guaranteed to function outside its operating conditions.

Typical Operating Characteristics

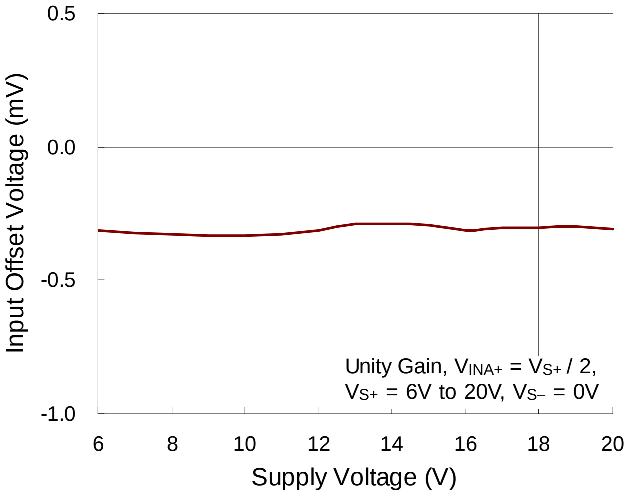
Supply Current / Amplifier vs. Supply Voltage



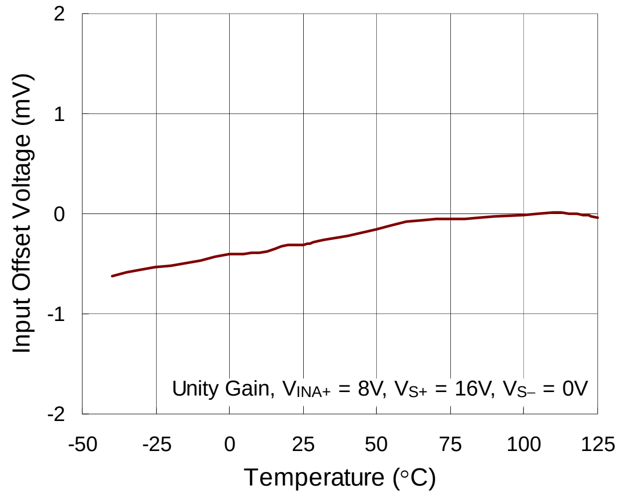
Supply Current / Amplifier vs. Temperature



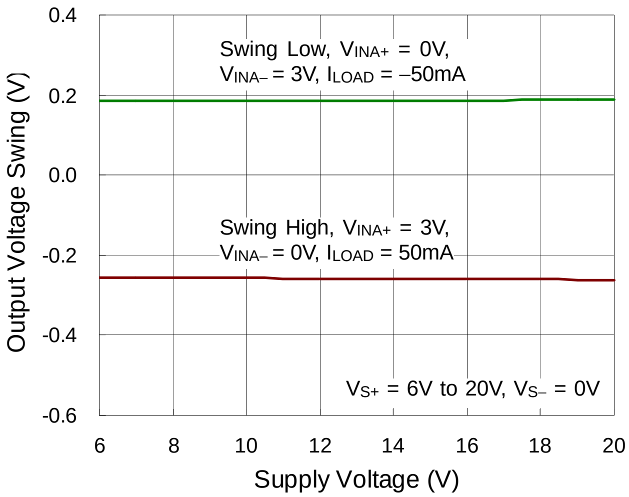
Input Offset Voltage vs. Supply Voltage



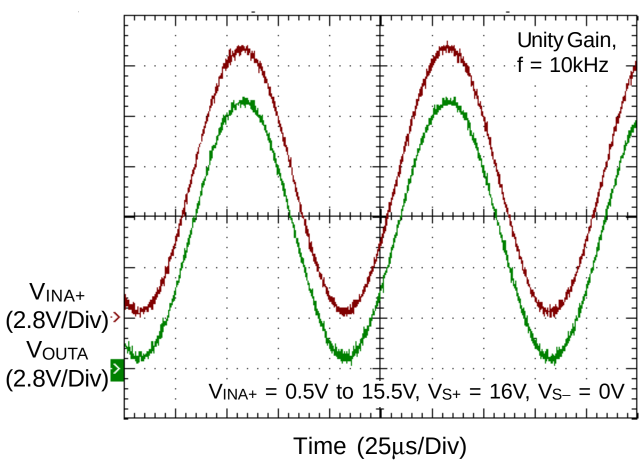
Input Offset Voltage vs. Temperature



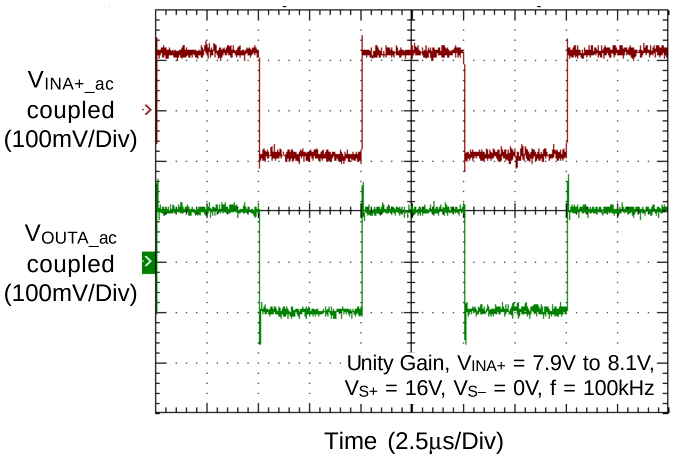
Output Voltage Swing vs. Supply Voltage



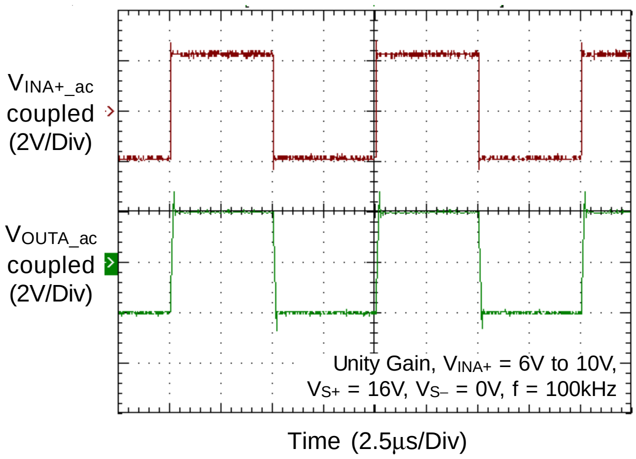
Rail to Rail



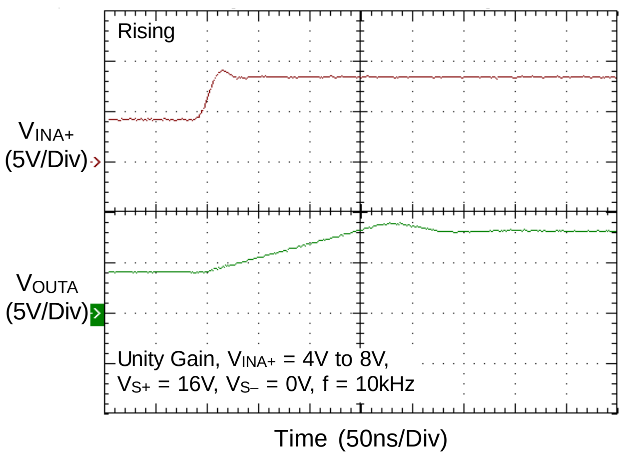
Small Signal Response



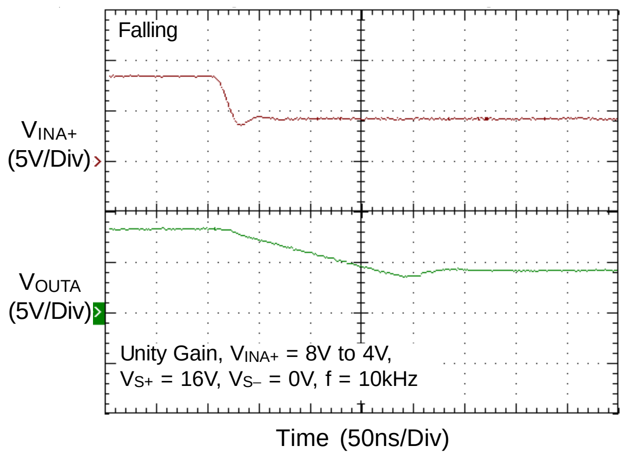
Large Signal Response



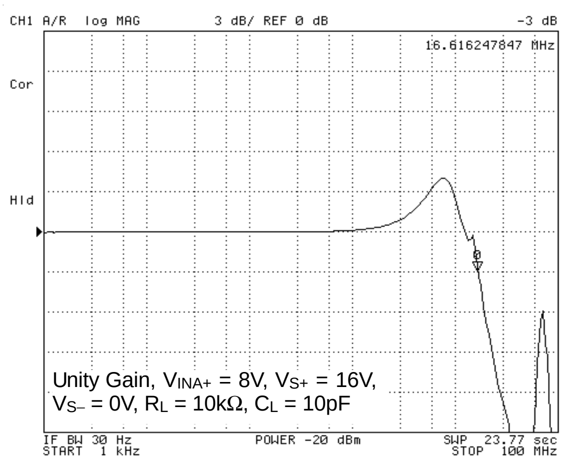
Slew Rate



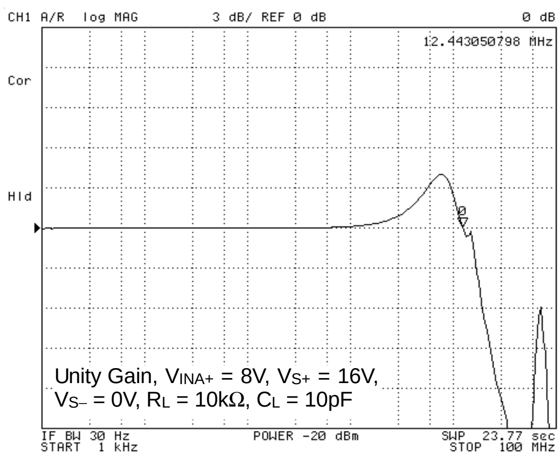
Slew Rate



–3dB Bandwidth



Gain Bandwidth Product



Applications Information

The RT9148/9 is a high performance operational amplifier capable of driving large loads for different applications. A high slew rates, rail-to-rail input and output capability, and low power consumption are the features which make the RT9148/9 ideal for LCD applications. The RT9148/9 also has wide bandwidth and phase margin to drive a load with 10kΩ resistance and 10pF capacitance.

Operating Voltage

The RT9148/9 total supply voltage range is guaranteed from 6V to 20V. The specifications are stable over both the full supply range and operating temperatures from −40°C to 85°C. The output swing of the RT9148/9 typically extends to within 1.5V of positive/negative supply rails with 50mA load current source/sink. Decreasing the load current will obtain an output swing even closer to the supply rails.

Short Circuit Condition

An internal short circuit protection is implemented to protect the device from output short circuit. The RT9148/9 limits the short circuit current to ±350mA if the output is directly shorted to positive/negative supply rails.

LCD Panel Applications

The RT9148/9 is mainly designed for LCD V-com buffer. The operational amplifier has 350mA instantaneous source/sink peak current.

Thermal Considerations

For continuous operation, do not exceed absolute maximum junction temperature. The maximum power dissipation depends on the thermal resistance of the IC package, PCB layout, rate of surrounding airflow, and difference between junction and ambient temperature. The maximum power dissipation can be calculated by the following formula :

$P_{D(MAX)} = (T_{J(MAX)} - T_A) / \theta_{JA}$

where $T_{J(MAX)}$ is the maximum junction temperature, T_A is the ambient temperature, and θ_{JA} is the junction to ambient thermal resistance.

For recommended operating condition specifications, the maximum junction temperature is 125°C. The junction to ambient thermal resistance, θ_{JA}, is layout dependent. For WDFN-6L 2x2 packages, the thermal resistance, θ_{JA}, is 47.5°C/W on a standard JEDEC 51-7 four-layer thermal test board. For TSOT-23-5 packages, the thermal resistance, θ_{JA}, is 230.6°C/W on a standard JEDEC 51-7 four-layer thermal test board. For UDFN-6L 2x2 packages, the thermal resistance, θ_{JA}, is 47.7°C/W on a standard JEDEC 51-7 four-layer thermal test board. For WDFN-8L 3x3 packages, the thermal resistance, θ_{JA}, is 31°C/W on a standard JEDEC 51-7 four-layer thermal test board. The maximum power dissipation at T_A = 25°C can be calculated by the following formula :

$P_{D(MAX)}$ = (125°C − 25°C) / (47.5°C/W) = 2.1W for WDFN-6L 2x2 package

$P_{D(MAX)}$ = (125°C − 25°C) / (230.6°C/W) = 0.43W for TSOT-23-5 package

$P_{D(MAX)}$ = (125°C − 25°C) / (47.7°C/W) = 2.09W for WDFN-6L 2x2 package

$P_{D(MAX)}$ = (125°C − 25°C) / (31°C/W) = 3.22W for WDFN-8L 3x3 package

The maximum power dissipation depends on the operating ambient temperature for fixed $T_{J(MAX)}$ and thermal resistance, θ_{JA}. The derating curve in Figure 1 allows the designer to see the effect of rising ambient temperature on the maximum power dissipation.

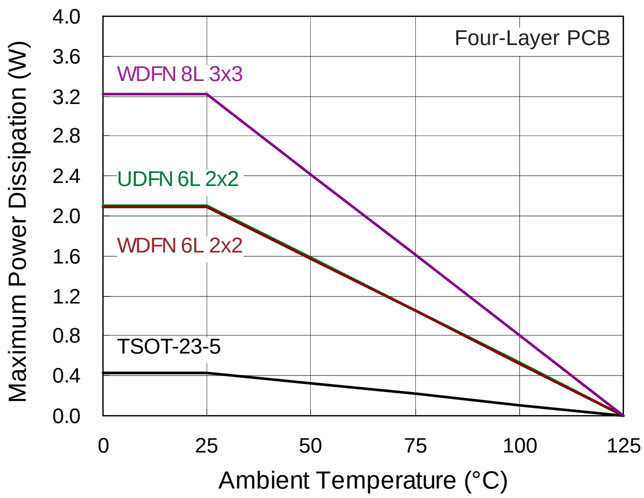


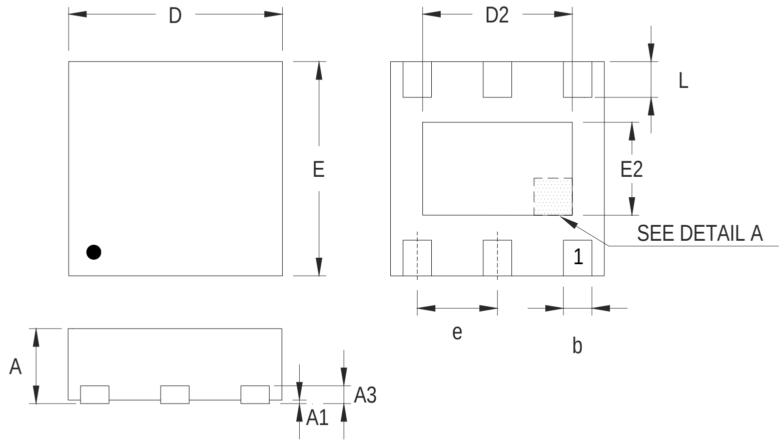
Figure 1. Derating Curve of Maximum Power Dissipation

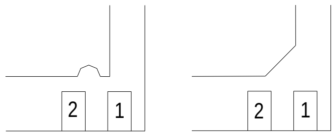
Layout Consideration

PCB layout is very important for designing power converter circuits. The following layout guidelines should be strictly followed for best performance of the RT9148/9.

- Place the power components as close to the IC as possible. The traces should be wide and short, especially for the high current loop.
- A series resistance may be needed at the output for some applications.
- Connect a 0.1μF capacitor from VINx+ to ground and place it as close to the IC as possible for better performance.
- The exposed pad of the chip should be connected to a large PCB plane for maximum thermal consideration.

Outline Dimension





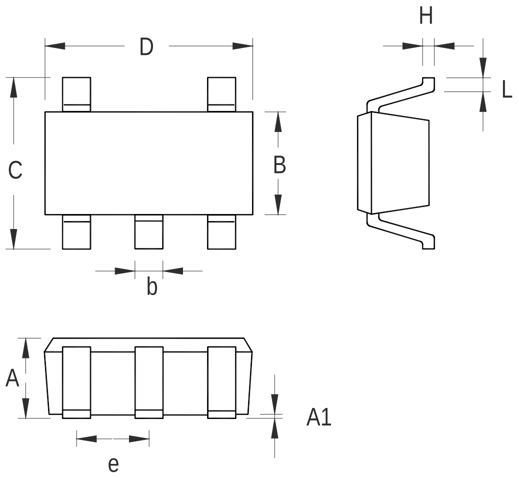
DETAIL A

Pin #1 ID and Tie Bar Mark Options

Note : The configuration of the Pin #1 identifier is optional, but must be located within the zone indicated.

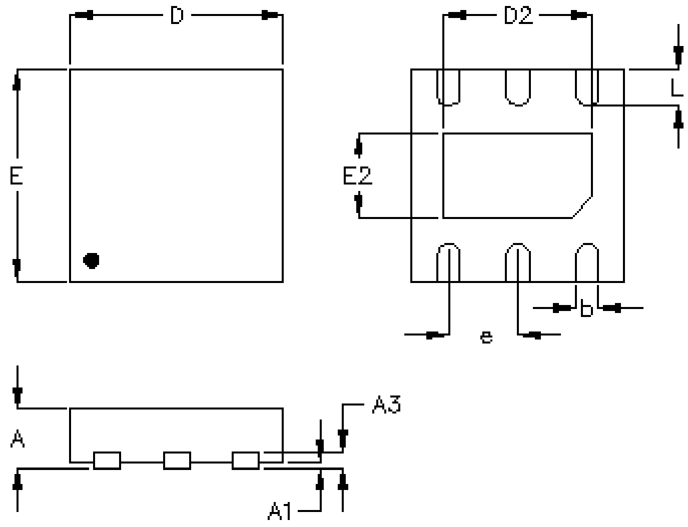
Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	0.700	0.800	0.028	0.031
A1	0.000	0.050	0.000	0.002
A3	0.175	0.250	0.007	0.010
b	0.200	0.350	0.008	0.014
D	1.950	2.050	0.077	0.081
D2	1.000	1.450	0.039	0.057
E	1.950	2.050	0.077	0.081
E2	0.500	0.850	0.020	0.033
e	0.650		0.026	
L	0.300	0.400	0.012	0.016

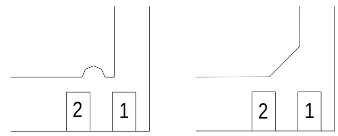
W-Type 6L DFN 2x2 Package



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	0.700	1.000	0.028	0.039
A1	0.000	0.100	0.000	0.004
B	1.397	1.803	0.055	0.071
b	0.300	0.559	0.012	0.022
C	2.591	3.000	0.102	0.118
D	2.692	3.099	0.106	0.122
e	0.838	1.041	0.033	0.041
H	0.080	0.254	0.003	0.010
L	0.300	0.610	0.012	0.024

TSOT-23-5 Surface Mount Package





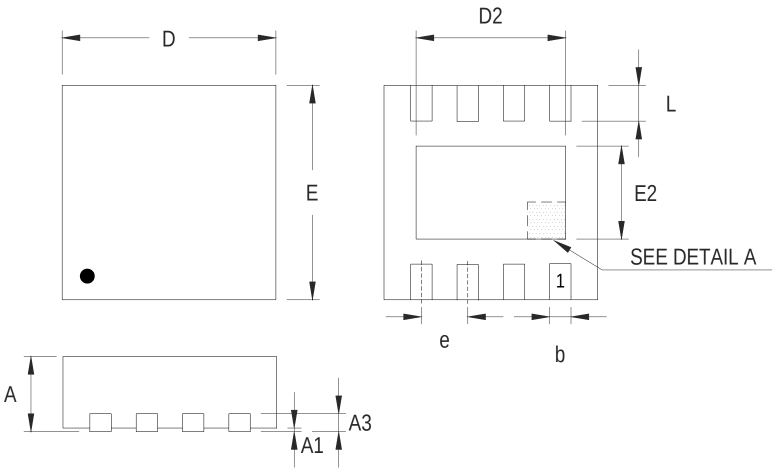
DETAIL A

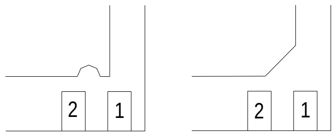
Pin #1 ID and Tie Bar Mark Options

Note : The configuration of the Pin #1 identifier is optional, but must be located within the zone indicated.

Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min.	Max.	Min.	Max.
A	0.500	0.600	0.020	0.024
A1	0.000	0.050	0.000	0.002
A3	0.100	0.175	0.004	0.007
b	0.200	0.300	0.008	0.012
D	1.900	2.100	0.075	0.083
D2	1.350	1.450	0.053	0.057
E	1.900	2.100	0.075	0.083
E2	0.750	0.850	0.030	0.033
e	0.650		0.026	
L	0.300	0.400	0.012	0.016

U-Type 6L DFN 2x2 Package





DETAIL A

Pin #1 ID and Tie Bar Mark Options

Note : The configuration of the Pin #1 identifier is optional, but must be located within the zone indicated.

Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	0.700	0.800	0.028	0.031
A1	0.000	0.050	0.000	0.002
A3	0.175	0.250	0.007	0.010
b	0.200	0.300	0.008	0.012
D	2.950	3.050	0.116	0.120
D2	2.100	2.350	0.083	0.093
E	2.950	3.050	0.116	0.120
E2	1.350	1.600	0.053	0.063
e	0.650		0.026	
L	0.425	0.525	0.017	0.021

W-Type 8L DFN 3x3 Package

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