1.5MHz, 1A, High Efficiency PWM Step-Down DC/DC Converter

General Description

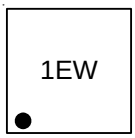
The RT8010C is a high efficiency Pulse-Width-Modulated (PWM) step-down DC/DC converter, and is capable of delivering 1A output current over a wide input voltage range from 2.5V to 5.5V. The RT8010C is ideally suited for portable electronic devices that are powered from 1-cell Li-ion battery or from other power sources such as cellular phones, PDAs and hand-held devices.

Two operating modes are available including : PWM/Low-Dropout autoswitch and shutdown modes. The Internal synchronous rectifier with low $R_{DS(ON)}$ dramatically reduces conduction loss at PWM mode. No external Schottky diode is required in practical application.

The RT8010C enters Low Dropout mode when normal PWM cannot provide regulated output voltage by continuously turning on the upper P-MOSFET. RT8010C enters shut-down mode and consumes less than 0.1μA when the EN pin is pulled low.

The switching ripple is easily smoothed-out by small package filtering elements due to a fixed operating frequency of 1.5MHz. Small WDFN-6L 2x2 package provides small PCB area application. Other features include soft start, lower internal reference voltage with 2% accuracy, over temperature protection, and over current protection.

Marking Information



1E : Product Code

W : Date Code

Features

- **2.5V to 5.5V Input Voltage Range**
- **Output Voltage (Adjustable Output From 0.6V to V_{IN})**
- **1A Output Current**
- **Up to 95% Efficiency**
- **No Schottky Diode Required**
- **1.5MHz Fixed Switching Frequency**
- **Current Limit**
- **Input UVLO Protection**
- **Thermal Shutdown**
- **Small 6-Lead WDFN Package**
- **RoHS Compliant and Halogen Free**

Applications

- Mobile Phones
- Personal Information Appliances
- Wireless and DSL Modems
- MP3 Players
- Portable Instruments

Ordering Information

RT8010C □□

Package Type
QW : WDFN-6L 2x2 (W-Type)

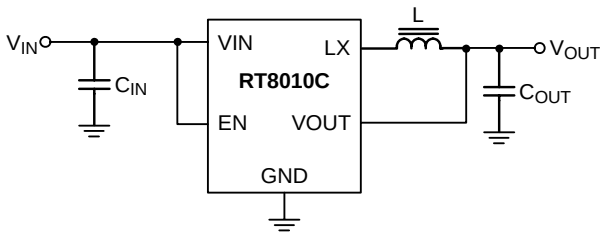
Lead Plating System
G : Green (Halogen Free and Pb Free)

Note :

Richtek products are :

- RoHS compliant and compatible with the current requirements of IPC/JEDEC J-STD-020.
- Suitable for use in SnPb or Pb-free soldering processes.

Simplified Application Circuit



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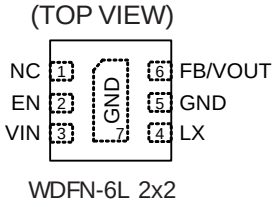
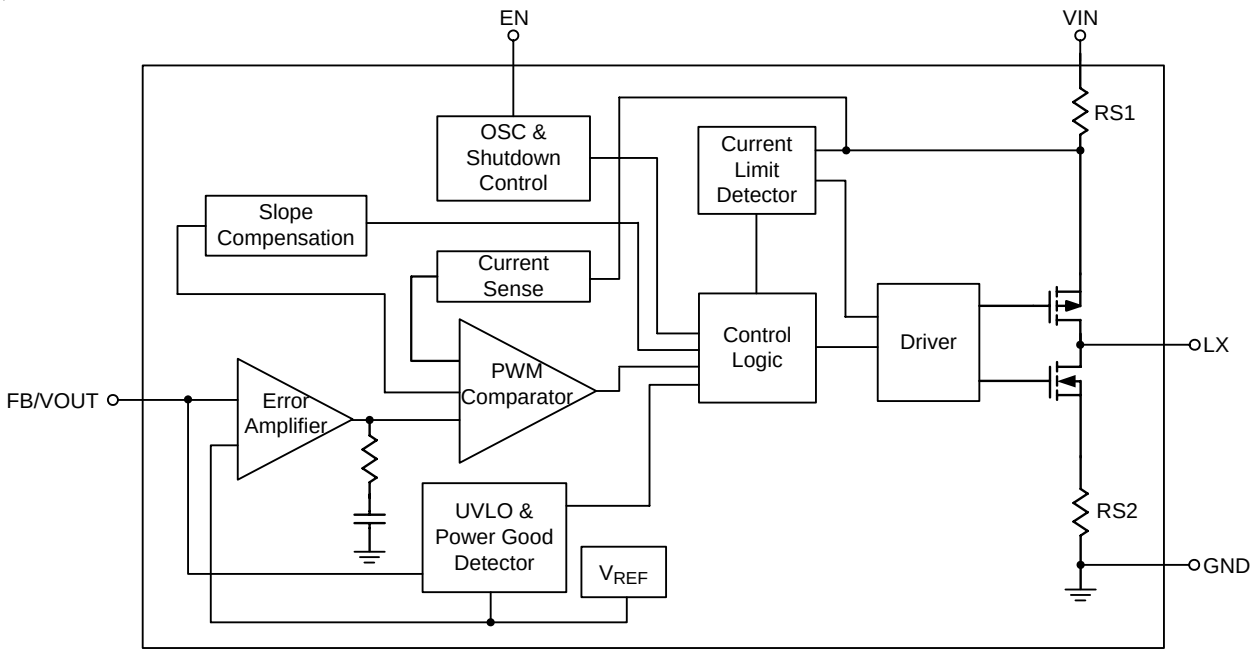
Pin Configurations



Functional Pin Description

Pin No.	Pin Name	Pin Function
1	NC	No Internal Connection. Leave floating or connect to ground.
2	EN	Chip Enable (Active High).
3	VIN	Power Input.
4	LX	Switch Node. Connect this pin to the external inductor.
5, 7 (Exposed Pad)	GND	Ground. The exposed pad must be soldered to a large PCB and connected to GND for maximum power dissipation.
6	FB/VOUT	Feedback/Output Voltage Sense Input.

Function Block Diagram



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Operation

The RT8010C is a synchronous step-down DC/DC converter with two integrated power MOSFETs and operates at 1.5MHz fixed frequency. Daring normal operation, the internal high side power switch (P-MOSFET) is turned on at the beginning of each clock cycle. Current in the inductor increases until the peak inductor current reaches the value defined by the output voltage of the error amplifier. The error amplifier adjusts its output voltage by comparing the feedback signal on the FB pin with an internal 0.6V reference. When the load current increases, it causes a drop in the feedback voltage relative to the reference, and the COMP voltage will rise to allow higher inductor current to match the load current.

OSC

The internal oscillator typically runs at 1.5 MHz switching frequency.

Over Temperature Protection (OTP)

The RT8010C implement an internal over temperature protection. When junction temperature is higher than 160°C, it will stop switching. Once the junction temperature cools down, the RT8010C will automatically resume switching.

Enable Comparator

A logic-high enable the converter, a logic-low forces the IC into shutdown mode.

Soft-Start (SS)

An internal current source charges an internal capacitor to build the soft-start ramp voltage. The FB voltage will track the internal ramp voltage during the soft-start interval.

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Absolute Maximum Ratings (Note 1)

- Supply Input Voltage, VIN ---------- 6.5V
- EN, FB Pin Voltage ---------- –0.3V to V_{IN}
- LX Pin Switch Voltage ---------- –0.3V to (V_{IN} + 0.3V)
  <20ns ---------- –4.5V to 7.5V
- LX Pin Switch Current ---------- 2A
- Power Dissipation, P_D @ T_A = 25°C
  WDFN-6L 2x2 ---------- 0.833W
- Package Thermal Resistance (Note 2)
  WDFN-6L 2x2, θ_{JA} ---------- 120°C/W
  WDFN-6L 2x2, θ_{JC} ---------- 8°C/W
- Lead Temperature (Soldering, 10 sec.) ---------- 260°C
- Storage Temperature Range ---------- –65°C to 150°C
- Junction Temperature ---------- 150°C
- ESD Susceptibility (Note 3)
  HBM (Human Body Model) ---------- 2kV

Recommended Operating Conditions (Note 4)

- Supply Input Voltage ---------- 2.5V to 5.5V
- Junction Temperature Range ---------- –40°C to 125°C
- Ambient Temperature Range ---------- –40°C to 85°C

Electrical Characteristics

(V_{IN} = 3.6V, V_{OUT} = 2.5V, L = 2.2µH, C_{IN} = 4.7µF, C_{OUT} = 10µF, T_A = 25°C, I_{MAX} = 1A unless otherwise specified)

Parameter		Symbol	Test Conditions		Min	Typ	Max	Unit
Input Voltage Range		V_{IN}			2.5	--	5.5	V
Quiescent Current		I_Q	I_{OUT} = 0mA, V_{FB} = V_{REF} + 5%		--	50	70	µA
Shutdown Current		I_{SHDN}	EN = GND		--	1	10	µA
Reference Voltage		V_{REF}	For Adjustable Output Voltage		0.588	0.6	0.612	V
Adjustable Output Range		V_{OUT}	(Note 5)		V_{REF}	--	V_{IN} – 0.2V	V
Output Voltage Accuracy	Adjustable	ΔV_{OUT}	V_{IN} = V_{OUT} + ΔV to 5.5V (Note 6) 0A < I_{OUT} < 1A		–3	--	3	%
FB Input Current		I_{FB}	V_{FB} = V_{IN}		–50	--	50	nA
P-MOSFET R_{ON}		$R_{DS(ON)\_P}$	I_{OUT} = 200mA	V_{IN} = 3.6V	--	0.28	--	Ω
				V_{IN} = 2.5V	--	0.38	--	
N-MOSFET R_{ON}		$R_{DS(ON)\_N}$	I_{OUT} = 200mA	V_{IN} = 3.6V	--	0.25	--	Ω
				V_{IN} = 2.5V	--	0.35	--	
P-Channel Current Limit		I_{LIM_P}	V_{IN} = 2.5V to 5.5V		1.4	1.5	--	A
EN Input Voltage	Logic-High	V_{EN_H}	V_{IN} = 2.5V to 5.5V		1.5	--	V_{IN}	V
	Logic-Low	V_{EN_L}	V_{IN} = 2.5V to 5.5V		--	--	0.4	

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Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Under Voltage Lockout Threshold	UVLO		--	1.8	--	V
UVLO Hysteresis			--	0.1	--	V
Oscillator Frequency	f_{OSC}	V_{IN} = 3.6V, I_{OUT} = 100mA	1.2	1.5	1.8	MHz
Thermal Shutdown Temperature	T_{SD}		--	160	--	°C
Maximum Duty Cycle			100	--	--	%
LX Leakage Current		V_{IN} = 3.6V, V_{LX} = 0V or V_{LX} = 3.6V	–1	--	1	μA

Note 1. Stresses beyond those listed "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions may affect device reliability.

Note 2. θ_{JA} is measured at T_A = 25°C on a high effective thermal conductivity four-layer test board per JEDEC 51-7. θ_{JC} is measured at the exposed pad of the package.

Note 3. Devices are ESD sensitive. Handling precaution recommended.

Note 4. The device is not guaranteed to function outside its operating conditions.

Note 5. Guarantee by design.

Note 6. $\Delta V = I_{OUT} \times P_{RDS(ON)}$

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Typical Application Circuit

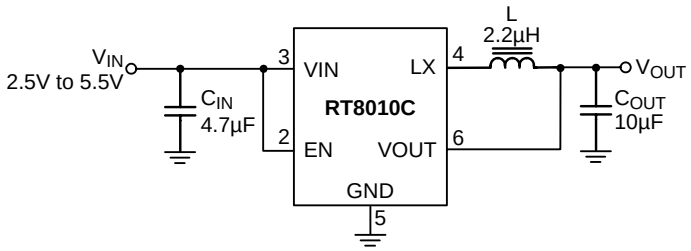
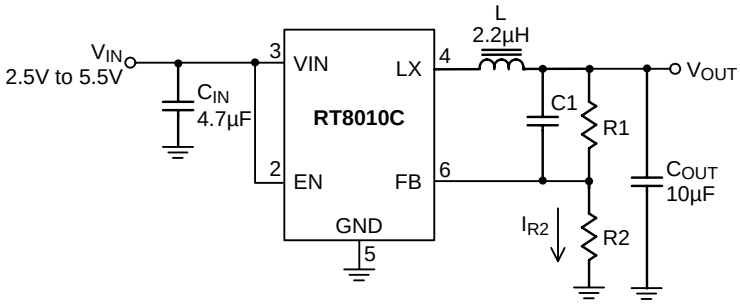


Figure 1. Fixed Output Voltage



$$V_{OUT} = V_{REF} \times \left(1 + \frac{R1}{R2}\right)$$

with R2 = 300kΩ to 60kΩ so the I_{R2} = 2µA to 10µA,

and (R1 x C1) should be in the range between $3x10^{-6}$ and $6x10^{-6}$ for component selection.

Figure 2. Adjustable Output Voltage

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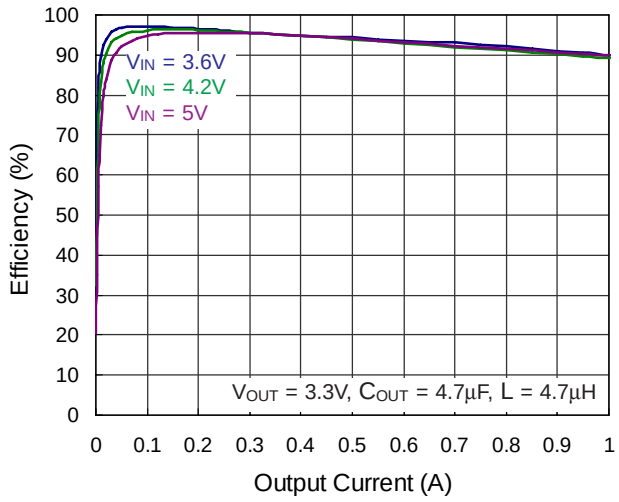
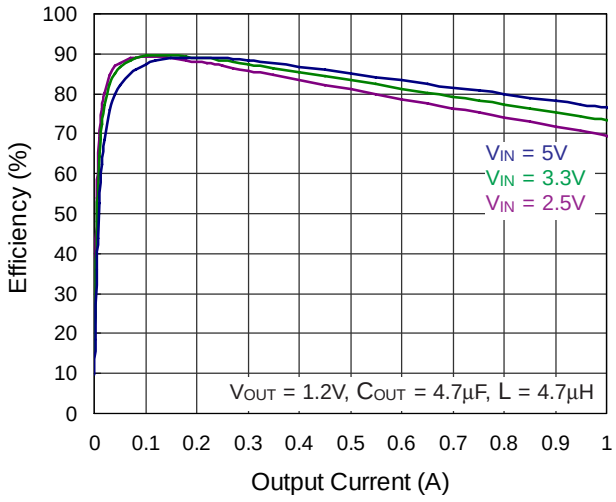
Typical Operating Characteristics

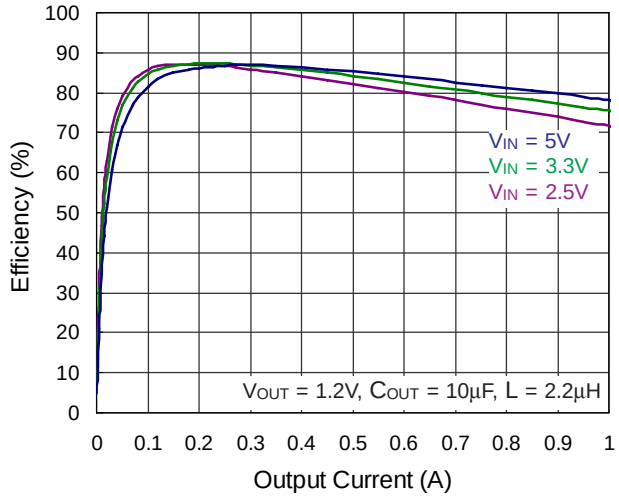
Efficiency vs. Output Current



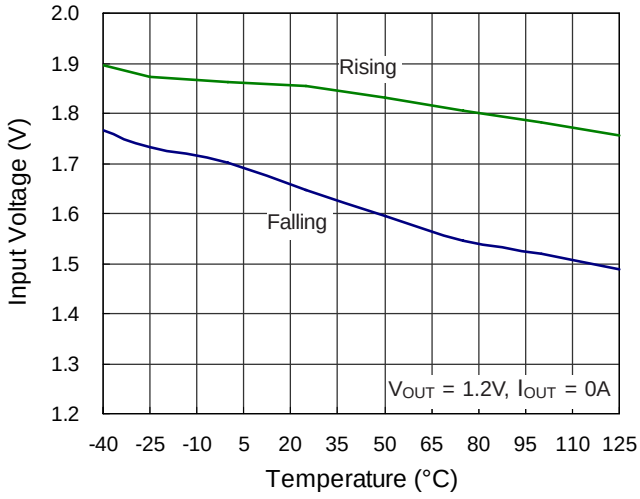
Efficiency vs. Output Current



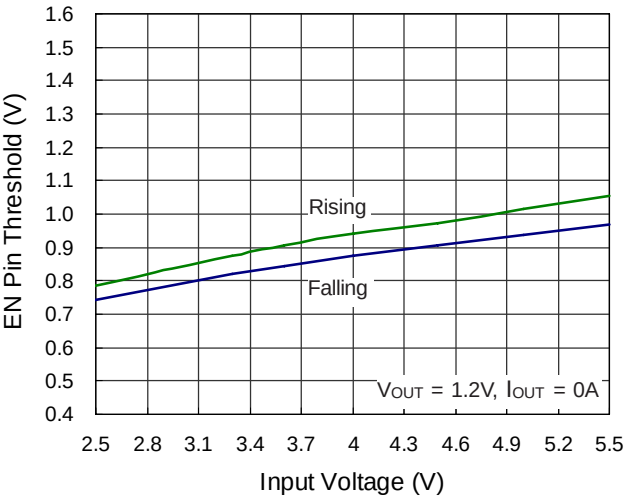
Efficiency vs. Output Current



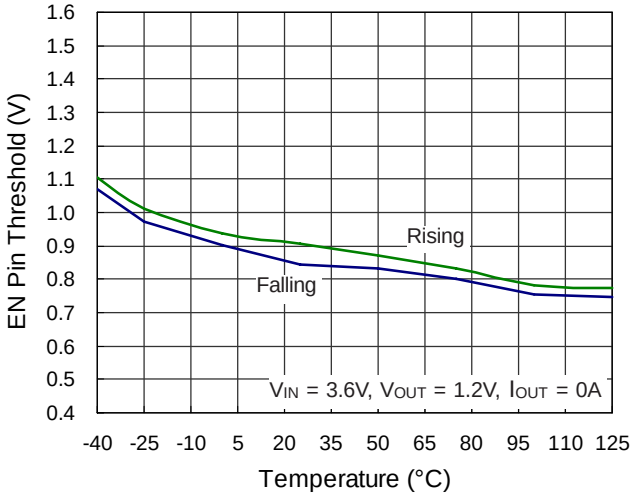
UVLO Voltage vs. Temperature



EN Pin Threshold vs. Input Voltage



EN Pin Threshold vs. Temperature



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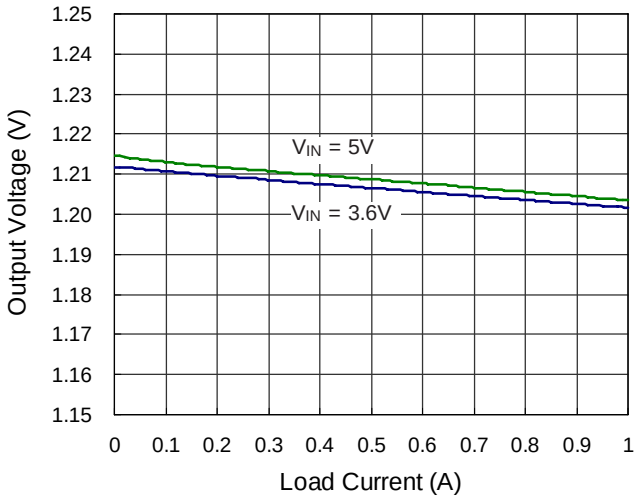
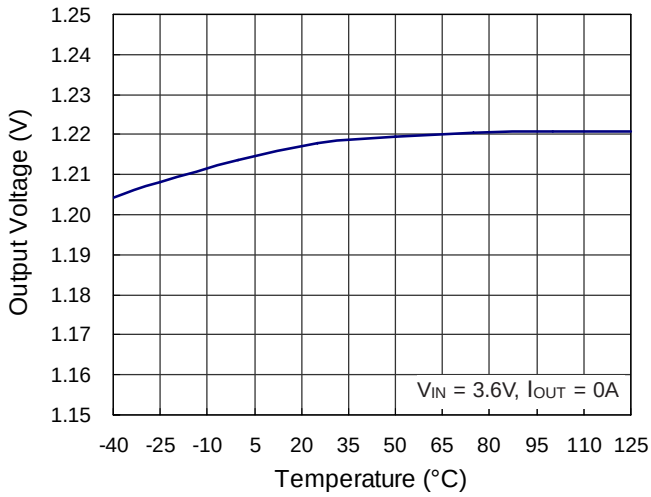
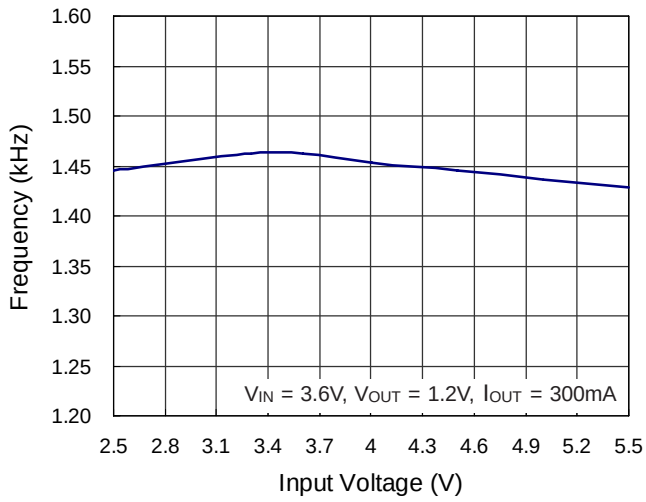
Output Voltage vs. Load Current



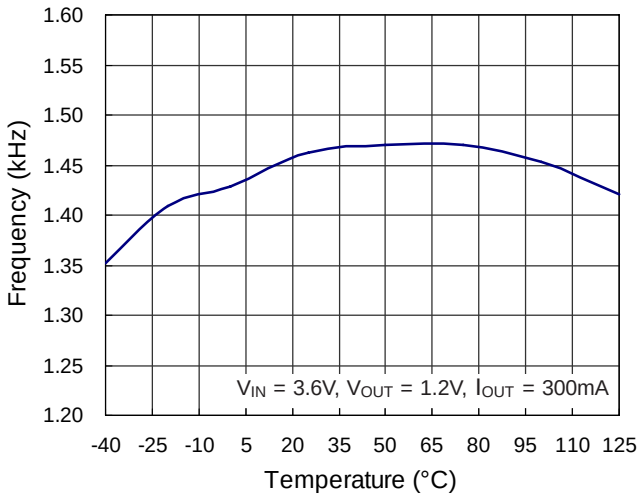
Output Voltage vs. Temperature



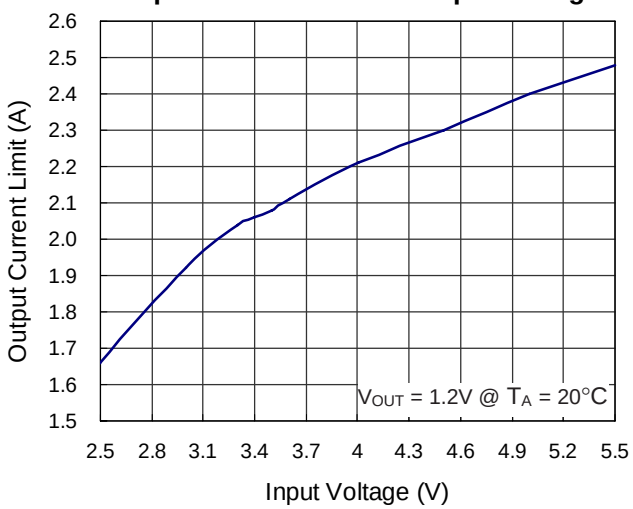
Frequency vs. Input Voltage



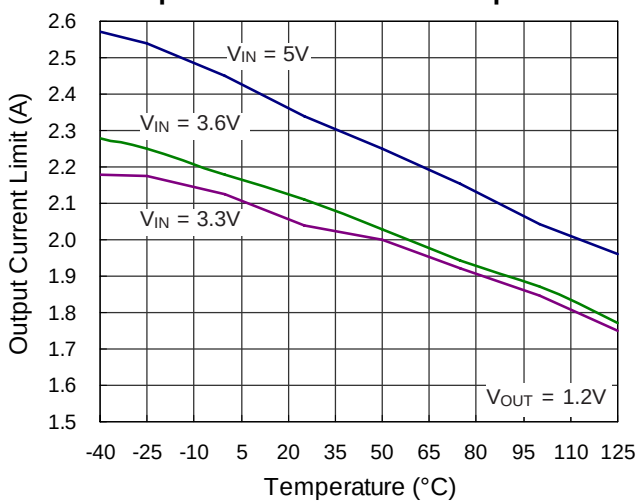
Frequency vs. Temperature



Output Current Limit vs. Input Voltage



Output Current Limit vs. Temperature



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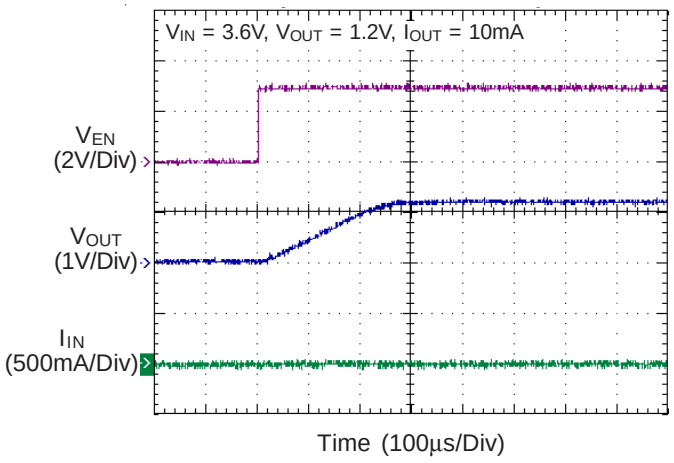
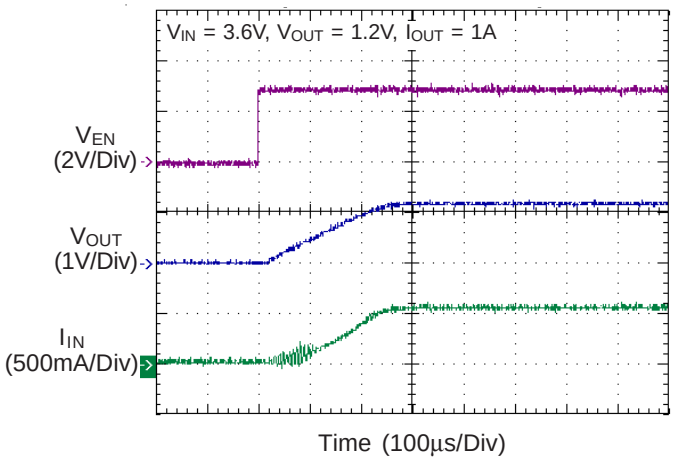
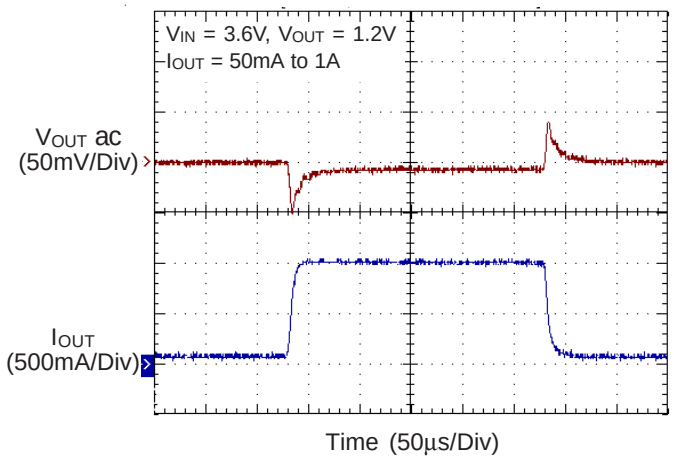
Power On from EN



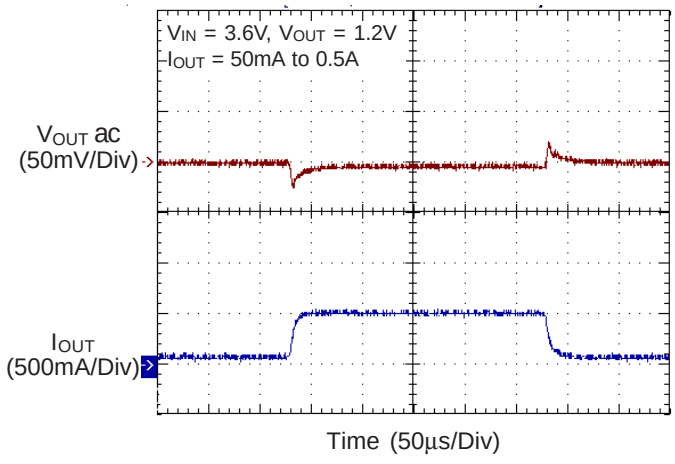
Power On from EN



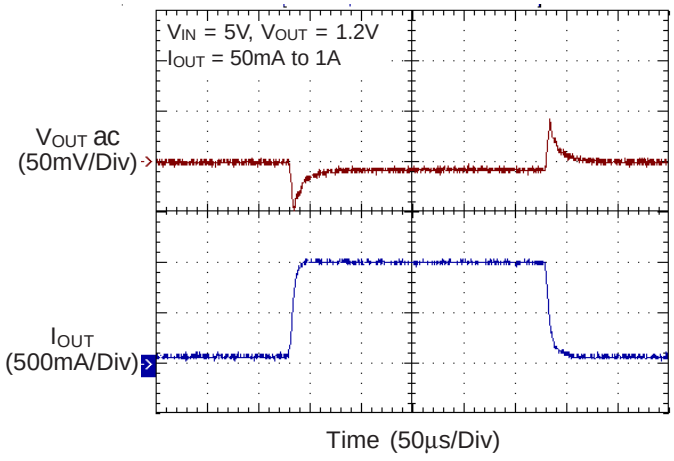
Load Transient Response



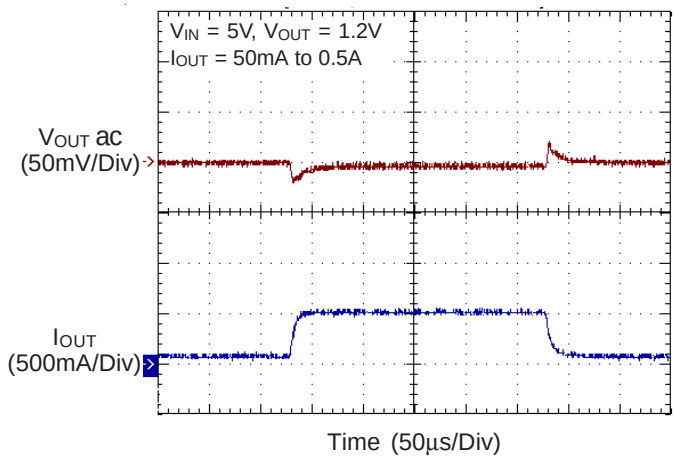
Load Transient Response



Load Transient Response



Load Transient Response



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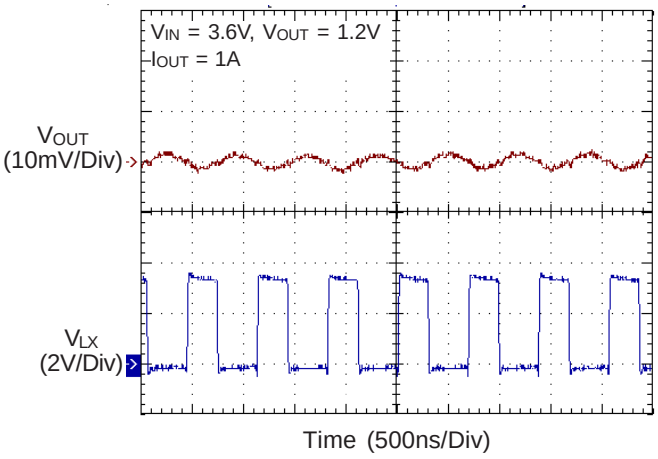
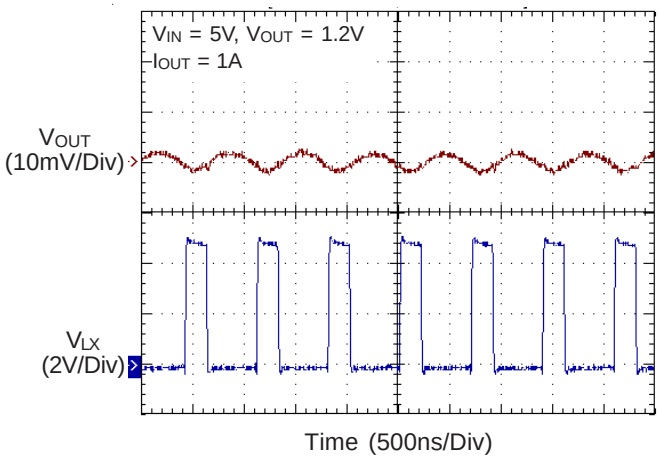
Output Ripple Voltage



Output Ripple Voltage



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Applications Information

The basic RT8010C application circuit is shown in Typical Application Circuit. External component selection is determined by the maximum load current and begins with the selection of the inductor value and operating frequency followed by C_{IN} and C_{OUT}.

Inductor Selection

For a given input and output voltage, the inductor value and operating frequency determine the ripple current. The ripple current ΔI_L increases with higher V_{IN} and decreases with higher inductance.

$$\Delta I_L = \left[\frac{V_{OUT}}{f \times L}\right] \times \left[1 - \frac{V_{OUT}}{V_{IN}}\right]$$

Having a lower ripple current reduces the ESR losses in the output capacitors and the output voltage ripple. Highest efficiency operation is achieved at low frequency with small ripple current. This, however, requires a large inductor.

A reasonable starting point for selecting the ripple current is $\Delta I_L = 0.4(I_{MAX})$. The largest ripple current occurs at the highest V_{IN}. To guarantee that the ripple current stays below a specified maximum, the inductor value should be chosen according to the following equation :

$$L = \left[\frac{V_{OUT}}{f \times \Delta I_{L(MAX)}}\right] \times \left[1 - \frac{V_{OUT}}{V_{IN(MAX)}}\right]$$

Using Ceramic Input and Output Capacitors

Higher values, lower cost ceramic capacitors are now becoming available in smaller case sizes. Their high ripple current, high voltage rating and low ESR make them ideal for switching regulator applications. However, care must be taken when these capacitors are used at the input and output. When a ceramic capacitor is used at the input and the power is supplied by a wall adapter through long wires, a load step at the output can induce ringing at the input, V_{IN}. The ringing can couple with the output and be mistaken as loop instability. At worst, a sudden inrush of current through the long wires can potentially cause a voltage spike at V_{IN} large enough to damage the part.

Output Voltage Setting

The resistive divider allows the FB pin to sense a fraction of the output voltage as shown in Figure 3.

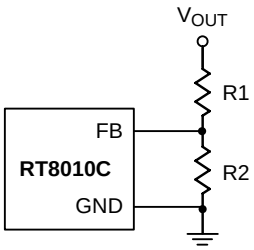

Figure 3. Setting the Output Voltage

For adjustable voltage mode, the output voltage is set by an external resistive divider according to the following equation :

$$V_{OUT} = V_{REF}\left(1 + \frac{R1}{R2}\right)$$

where V_{REF} is the internal reference voltage (0.6V typ.)

Thermal Considerations

The maximum power dissipation depends on the thermal resistance of IC package, PCB layout, the rate of surroundings airflow and temperature difference between junction to ambient. The maximum power dissipation can be calculated by following formula :

$P_{D(MAX)} = (T_{J(MAX)} - T_A) / \theta_{JA}$

Where $T_{J(MAX)}$ is the maximum operation junction temperature, T_A is the ambient temperature and the θ_{JA} is the junction to ambient thermal resistance.

For recommended operating conditions specification of RT8010C DC/DC converter, where $T_{J(MAX)}$ is the maximum junction temperature of the die and T_A is the maximum ambient temperature. The junction to ambient thermal resistance θ_{JA} is layout dependent. For WDFN-6L 2x2 package, the thermal resistance θ_{JA} is 120°C/W on the standard JEDEC 51-7 four layers thermal test board.

The maximum power dissipation at T_A = 25°C can be calculated by following formula :

$P_{D(MAX)}$ = (125°C – 25°C) / 120°C/W = 0.833W for WDFN-6L 2x2 package

The maximum power dissipation depends on operating ambient temperature for fixed $T_{J(MAX)}$ and thermal resistance θ_{JA}.

The derating curve in Figure 4 of derating curves allows the designer to see the effect of rising ambient temperature on the maximum power allowed.

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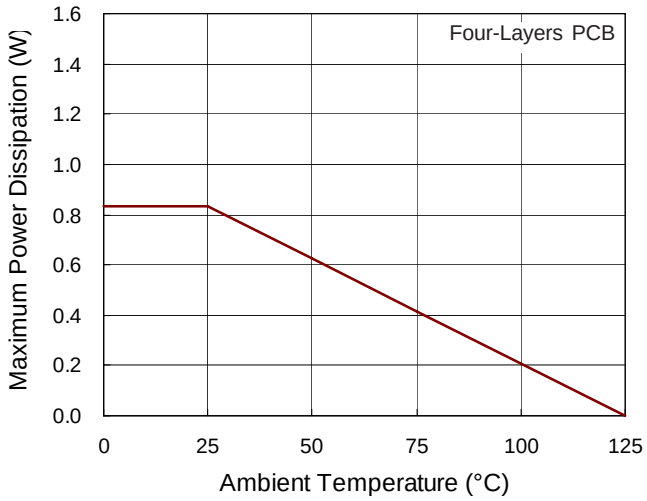

Figure 4. Derating Curve of Maximum Power Dissipation

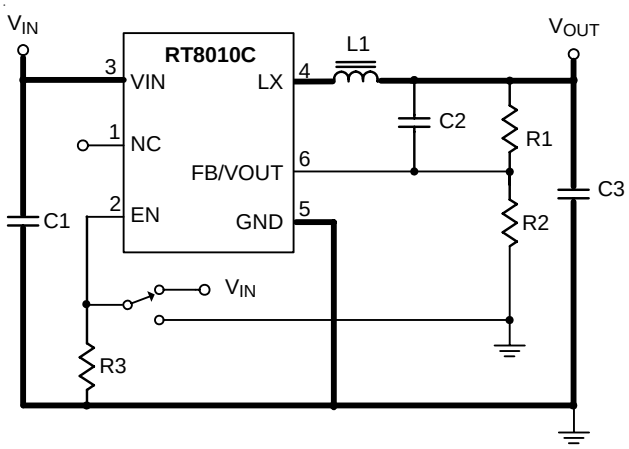

Figure 5. EVB Schematic

Checking Transient Response

The regulator loop response can be checked by looking at the load transient response. Switching regulators take several cycles to respond to a step in load current. When a load step occurs, V_{OUT} immediately shifts by an amount equal to ΔI_{LOAD} (ESR), where ESR is the effective series resistance of C_{OUT}. ΔI_{LOAD} also begins to charge or discharge C_{OUT} generating a feedback error signal used by the regulator to return V_{OUT} to its steady-state value. During this recovery time, V_{OUT} can be monitored for overshoot or ringing that would indicate a stability problem.

Layout Considerations

Follow the PCB layout guidelines for optimal performance of RT8010C.

- For the main current paths as indicated in bold lines in Figure 5, keep these traces short and wide.
- Put the input capacitor as close as possible to the device pins (VIN and GND).
- LX node is with high frequency voltage swing and should be kept within small area. Keep analog components away from LX node to prevent stray capacitive noise pick-up.
- Connect feedback network behind the output capacitors. Keep the loop area small. Place the feedback components near the RT8010C.
- An example of 2-layer PCB layout is shown in Figure 6 for reference.

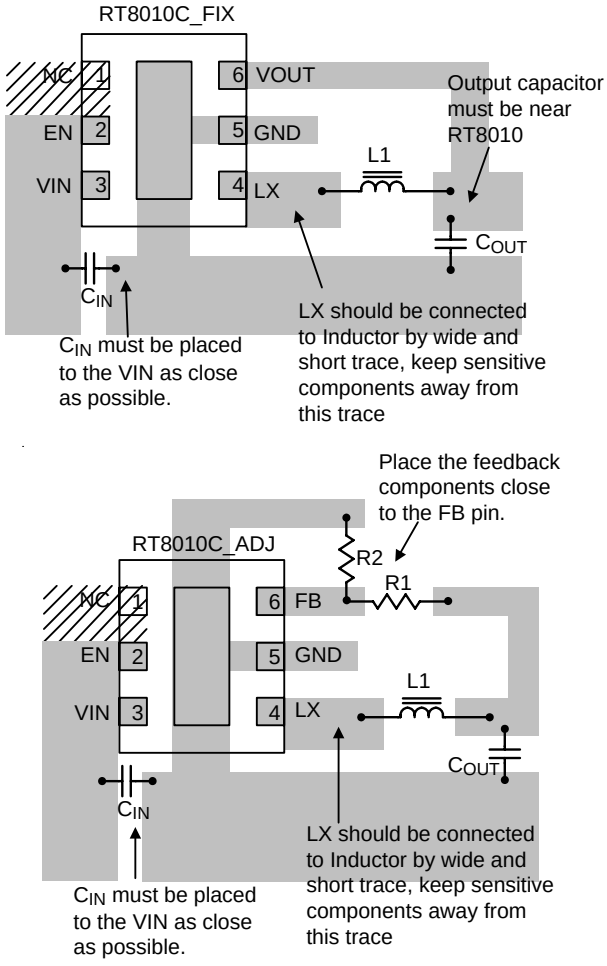

Figure 6. PCB Layout Guide

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Table 1. Recommended Inductors

Supplier	Inductance (μH)	Current Rating (mA)	DCR (mΩ)	Dimensions (mm)	Series
TAIYO YUDEN	2.2	1480	60	3.00 x 3.00 x 1.50	NR 3015
GOTREND	2.2	1500	58	3.85 x 3.85 x 1.80	GTSD32
Sumida	2.2	1500	75	4.50 x 3.20 x 1.55	CDRH2D14
Sumida	4.7	1000	135	4.50 x 3.20 x 1.55	CDRH2D14
TAIYO YUDEN	4.7	1020	120	3.00 x 3.00 x 1.50	NR 3015
GOTREND	4.7	1100	146	3.85 x 3.85 x 1.80	GTSD32

Table 2. Recommended Capacitors for C_{IN} and C_{OUT}

Supplier	Capacitance (μF)	Package	Part Number
TDK	4.7	0603	C1608JB0J475M
MURATA	4.7	0603	GRM188R60J475KE19
TAIYO YUDEN	4.7	0603	JMK107BJ475RA
TAIYO YUDEN	10	0603	JMK107BJ106MA
TDK	10	0805	C2012JB0J106M
MURATA	10	0805	GRM219R60J106ME19
MURATA	10	0805	GRM219R60J106KE19
TAIYO YUDEN	10	0805	JMK212BJ106RD

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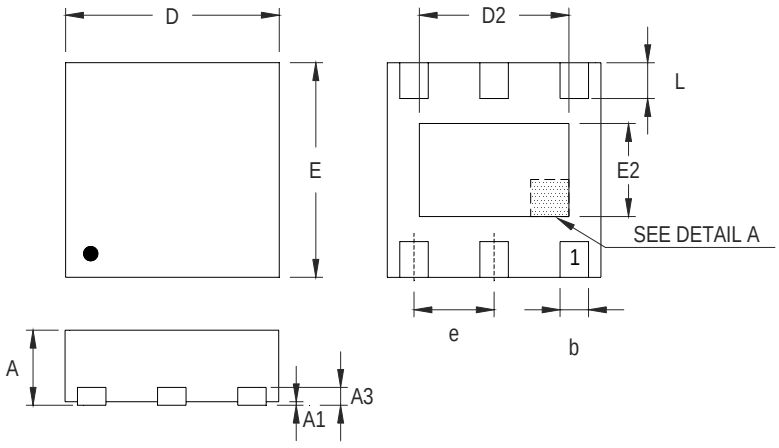
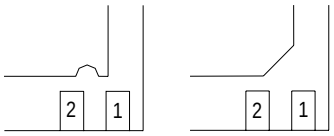
Outline Dimension





DETAIL A

Pin #1 ID and Tie Bar Mark Options

Note : The configuration of the Pin #1 identifier is optional, but must be located within the zone indicated.

Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	0.700	0.800	0.028	0.031
A1	0.000	0.050	0.000	0.002
A3	0.175	0.250	0.007	0.010
b	0.200	0.350	0.008	0.014
D	1.950	2.050	0.077	0.081
D2	1.000	1.450	0.039	0.057
E	1.950	2.050	0.077	0.081
E2	0.500	0.850	0.020	0.033
e	0.650		0.026	
L	0.300	0.400	0.012	0.016

W-Type 6L DFN 2x2 Package

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