Primary Feedback CC/CV PWM Controller for Flyback Converters

General Description
The R7711A is a current mode PWM controller which includes primary side voltage feedback technology. It controls the output voltage and current accurately without shunt regulator and opto-coupler on secondary side to reduce the part count and save costs.

The R7711A is designed especially for low power applications, such as chargers for cell phones, PDAs, and other mobile products. Complete protections are provided, such as output Under-Voltage Protection, output Over-Voltage Protection, VDD Over-Voltage Protection, Over-Temperature Protection, and Secondary Rectifier Short-circuit Protection. The ultra low start-up current and operating current of the R7711A achieves low power consumption in standby mode. The R7711A supports green-mode operation to meet CEC regulations and Energy-Star requirements.

Features
- Programmable Primary-Side CC/CV Regulation
- Low No Load Input Power (<30mW at 230VAC)
- Green Mode PWM Operation
  - Low Start-up Current (<10mA)
  - Triple Mode PWM Operation
- Easy EMI Solution
  - Built-in Jittering Frequency
  - Built-in Soft Gate Driver
- Programmable Cable Drop Compensation
- Adjustable Propagation Delay Compensation
- VDD Over-Voltage Protection(VDDOV)
- Output Over-Voltage Protection(OVP)
- Output Under-Voltage Protection(UVP)
- Secondary Rectifier Short-Circuit Protection (SRSP)
- Internal Over-Temperature Protection(OTP)
- RoHS Compliant and Halogen Free

Applications
- Switching AC/DC Adaptor and Battery Charger
- DVD Open Frame Power Supply
- STB Power
- Cell Phone Charger
- Networking Power Supply

Simplified Application Circuit
## Functional Pin Description

<table>
<thead>
<tr>
<th>Pin No.</th>
<th>Pin Name</th>
<th>Pin Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>GATE</td>
<td>MOSFET Gate Driver Output. Connect this pin to the Gate of an external N-Channel power MOSFET.</td>
</tr>
<tr>
<td>2</td>
<td>GND</td>
<td>Ground of the Controller.</td>
</tr>
<tr>
<td>3</td>
<td>VDD</td>
<td>Power Supply Input. The controller will be enabled when VDD exceeds VTH.ON and disabled when VDD decreases lower than VTH.OFF.</td>
</tr>
<tr>
<td>4</td>
<td>DMAG</td>
<td>Demagnetization Pin. Input and Output Voltage Detection from Auxiliary Winding. The current (ICABLE) flows into this pin to achieve cable drop compensation function. This pin is also used to detect the signal of the rectified input voltage for propagation delay compensation and minimum on-time control.</td>
</tr>
<tr>
<td>5</td>
<td>COMP</td>
<td>Feedback Compensation Pin. This pin is the output of the internal operational transconductance amplifier (OTA) to connect a proper RC network from this pin to GND for feedback loop compensation.</td>
</tr>
<tr>
<td>6</td>
<td>CS</td>
<td>Current Sensing Input. Connect this pin to a current sense resistor used to detect the current of the primary-side winding.</td>
</tr>
</tbody>
</table>
Function Block Diagram

- **VDD**
- **CS**
- **Voltage Sample-and-Hold** (VTH_ON/OFF = 14.5V/8.5V)
- **Oscillator with Frequency Reduction and Jittering**
- **OTA**
- **VREF 2.5V**
- **Peak-current Comparator**
- **DMAG Knee Point Detector**
- **Constant Current Control (KCC = 4.7µs × V)**
- **Cable Voltage Drop Compensation**
- **Over-Voltage Protection (VTH_VDDOV = 27V)**
- **Under-Voltage Lockout (VTH_ON/OFF = 14.5V/8.5V)**
- **UVLO VDDOVP**
- **Shutdown Control Logic**
- **PWM**
- **Output Over-Voltage Protection (VTH_OVP = 3.125V)**
- **Output Under-Voltage Protection (VTH_UVP = 1.2V)** (Debounce: 2048CLKs)
- **Over-Temperature Protection (TTOP = 130°C)**
- **Over-Voltage Protection (VTH_CV)**
- **Voltage Clamping (VCLAMP = 12V)**
- **Voltage Clamping and Current Sampling (ICS = ICLAMP × KI)**
- **Soft Gate Driver**
- **Leading Edge Blanking**
- **Min-On-Time Generator (Tmin = 0.2ns × A / DMAX)** (Debounce: 2048CLKs)
- **PWM**
- **Burst-Mode Comparator (VTH_BURST = 1.1V BURST)**
- **Burst Mode Comparator**
- **Output Enable (VTH_CE)**
- **KNEE Knee Point Detector**
- **Voltage Clamping Current Sampling**
- **Current Sampling (ICS = ICLAMP × KI)**
- **Max. Duty Protection (DMAX = 77%)** (Debounce: 2048CLKs)
- **PWM**
- **Max Duty Protection (DMAX = 77%)**
- **Min-On-Time Generator (Tmin = 0.2ns × A / DMAX)**
- **PWM**
Operation

General Description

The R7711A is a peak current-mode PWM controller designed for off-line flyback converter in DCM (Discontinuous Conduction Mode) operation. It can achieve accurate CV (Constant-Voltage) or CC (Constant-Current) output without voltage and current sensing circuits on the secondary side, as shown the Figure 1. When the output voltage is below the under-voltage threshold (VOUT_MIN), the R7711A works in hiccup mode.

Figure 1. Output Voltage vs. Output Current

Constant-Voltage Operation

The Figure 2 shows the simplified primary-side-regulation circuit. The output voltage signal is indirectly detected via the transformer (TX1) and the resistor-divider (RDMAG1 and RDMAG2). A “Knee point” detection and voltage sample-and-hold circuits are required for sensing the feedback voltage. The sample-and-hold voltage (VSH_Dmag) of the VDMAG is shown in the following equation:

\[
V_{SH_{DMAG}} = (V_{OUT} + V_F) \cdot \frac{N_A}{N_S} \cdot \frac{R_{DMAG1}}{R_{DMAG1} + R_{DMAG2}}
\]

(at the Knee point)

\(V_F\) : the forward voltage of the Diode with \(I_{DO}\) near 0A

In the “Functional Block Diagram”, the OTA compares the VREF (\(V_{REF} = 2.5\,\text{V typ.}\)) and VSH_Dmag to generate the error signal. The peak-current comparator compares the VCOMP with the current signal (VCS) to determine the gate driver outputs duty cycle. The VCOMP is also used to modulate the oscillator frequency for green-mode operation.

Figure 2. Simplified Circuit and Symbol Definition
Programmable Cable Drop Compensation

The R7711A features a cable drop compensation to adaptively compensate the output voltage drop effect due to the output cable impedance. As shown in the figure 4, the ICABLE, proportional to the converter output current, creates an additional voltage offset (ΔVRDMAG2) into the DMAG pin to achieve the cable compensation. The ICABLE is calculated by using the following equation:

\[
ICABLE = 8 \mu A/V \times VCOMP - 11.2 \mu A \quad (ICABLE \geq 0)
\]

Please refer to Figure 5. The DMAG pin is equipped with a low-level voltage clamping circuit to prevent the IC from being damaged by negative voltage. During the t0–t1 as the Figure 3, the main switch (Q1) is turned on, and the circuit outputs the current (ICLAMP) to clamp the VDMAG near 0V when the voltage (V_AUX) of auxiliary winding is negative. The ICLAMP is calculated by using the following equation:

\[
ICLAMP = \frac{VIN}{RDMAG2} \times \frac{NA}{NP}
\]

The R7711A also provides propagating delay compensation through the CS pin. The I_CS (= ICLAMP x KI), proportional to line voltage on the CS pin, and the R_PDC compensate for the propagation delay effect of the CC control loop. Thus, the constant current output can be very close to the preset level at high and low line voltages.

Triple Mode PWM Operation

In Figure 6, the triple mode PWM operation provides excellent green power performance, especially under light load and no load conditions.
Constant-Current Operation
The R7711A features a patented constant current control circuit. The $I_{OUT\_CC}$ can be calculated as the following equation:

$$I_{OUT\_CC} \approx \frac{1}{2} \frac{N_P}{N_S} \frac{V_{TH\_CC} \cdot T_{ON\_D}}{R_{CS} \cdot T_S} = \frac{1}{2} \frac{N_P \cdot K_{CC}}{N_S \cdot R_{CS} \cdot T_S}$$

Frequency Reduction Mode
In Figure 6, to reduce switching losses, the Frequency Reduction (FR) mode is designed to operate at middle load current conditions with the COMP voltage ($V_{COMP}$) between the voltage thresholds $V_{TH\_FRH}$ (3.2V typ.) and $V_{TH\_FRL}$ (1.5V typ.). In this mode, the switching frequency, from 65kHz to 1kHz, is linearly modulated by the $V_{COMP}$.

Burst Mode
To further reduce the switching losses in no load or very light load condition, a burst mode control reduces the average switching frequency when the $V_{COMP}$ is below the $V_{TH\_FRL}$ (1.5V typ.). A Burst-mode voltage threshold ($V_{TH\_BURST}$=1.1V typ.) switches the operating frequency in either $f_{BURST}$ (1kHz typ.) or $f_{MIN}$ (250Hz typ.). The green mode operation meets the CEC regulations and Energy-Star requests.

Min. On-Time
To improve green power at light load or no load conditions, the R7711A works with a minimum on-time ($T_{ON\_MIN}$) and the output voltage is regulated by the modulated switching frequency. The $T_{ON\_MIN}$, shown as the following equation, is a function of the $I_{CLAMP}$:

$$T_{ON\_MIN} = \frac{0.7A \cdot ns}{I_{CLAMP}}$$

Adaptive Blanking Time
In Figure 7, the ringing waveform is induced by the leakage inductance and the peak current of the primary winding at the rising edge of the $V_{DMAG}$. It may cause improper knee point detection and further result in unstable operation. The magnitude and settling time of the voltage ringing increases larger at heavy loads with higher peak currents. Thus, the R7711A provides a modulated blanking time ($T_{BLANK}$) depending on the CS peak voltage ($V_{CSPK}$). The $T_{BLANK}$ can be calculated by using the following equation:

$$T_{BLANK} = 1ms + V_{CSPK} \times 3ms/V$$

Leading Edge Blanking (LEB) for $V_{CS}$
Due to the device’s parasitic capacitors, an initial current spike appears at the rising edge of the GATE voltage ($V_{GATE}$). The spike of the CS voltage may incorrectly trigger the peak current comparator, to turn off the power MOSFET, resulting in running failure of the flyback converter. Thus, the LEB, used to mask the initial voltage spike on the CS pin, is a necessary design for successful PWM operation.
A frequency jittering function is embedded to further reduce EMI (Electromagnetic Interference). In Figure 8, the function modulates the oscillator frequency in a triangular waveform with the period \( T_{JITTER} \) of 4ms (typ.). In this condition, the maximum average \( f_{PWM} \) of the oscillator frequency \( f_{OSC} \) is 65kHz (typ.) and the jittering frequency range \( \Delta f \) is ±6% of the \( f_{PWM} \).

**VDD Under-Voltage Lockout (UVLO) Protection**

The R7711A automatically initializes upon receipt of the supply voltage \( V_{DD} \) on the VDD pin. The UVLO function continually monitors the \( V_{DD} \). When the \( V_{DD} \) exceeds its rising UVLO threshold \( V_{TH\_ON} = 14.5V \) (typ.), the IC is enabled. When the \( V_{DD} \) falls below the falling UVLO voltage threshold \( V_{TH\_OFF} = 8.5V \) (typ.), the GATE voltage is pulled low to shut off the converter. The supply voltage \( V_{DD} \) must be below the absolute maximum rating for safety.

**VDD Over-Voltage Protection (VDD OVP)**

When the \( V_{DD} \) exceeds the VDD over-voltage threshold \( V_{TH\_VDDOV} = 27V \) (typ.) in abnormal conditions, the GATE voltage is pulled low to shut off the converter and the R7711A works in hiccup mode until the fault is removed. This avoids permanent damage of the converter components. The VDD over-voltage may be caused by an incorrectly sensed feedback signal on the DMAG pin or an output over-voltage condition.

**Output Over-Voltage Protection (OVP)**

The R7711A provides accurate output OVP. Once the feedback voltage \( V_{SH\_DMAG} \), sampled on the DMAG pin, is over 125% (typ.) of the reference voltage \( V_{REF} = 2.5V \) (typ.), the R7711A issues an output OVP signal to turn off the controller and prevent the loading device and converter from being damaged. Therefore, the OVP threshold on the output is about 125% of the CV output voltage at the end of the PCB. The R7711A works in hiccup mode until the fault is removed.

**Output Under-Voltage Protection (UVP)**

The output UVP is designed to protect the converter from the output short-circuit conditions. Once the feedback voltage \( V_{SH\_DMAG} \), sampled on the DMAG pin, is below the voltage threshold \( V_{TH\_UVP} = 1.2V \) (typ.), a built-in 11-bit digital timer performs a UVP debounce time (2048 switching cycles = about 30ms) before issuing the UVP signal. The UVP signal turns off the converter to prevent the loading device and converter from being damaged. The R7711A works in hiccup mode until the fault is removed.

**Over-Temperature Protection (OTP)**

The built-in OTP function continuously monitors the junction temperature \( T_J \) of the IC itself. Once the \( T_J \) exceeds the over-temperature level \( T_{OTP} = 150°C \) (typ.), the OTP signal turns off the converter and prevents the IC itself from suffering thermal stress and permanent damage. It's not suggested to use the function as a precise OTP. The R7711A works in hiccup mode until the fault is removed.

**Secondary Rectifier Short-circuit Protection (SRSP)**

The R7711A is equipped with an extra over-current protection (OCP) against secondary rectifier short-circuit conditions in flyback converter. When the secondary rectifier is damaged by short-circuit, the transformer operates in saturation area and huge current stress occurs on the main switch. When the \( V_{CS} \) reaches the OCP voltage threshold \( V_{TH\_OCP} = 1.7V \) (typ.), the R7711A shuts down the converter after the debounce time of a few cycles. The R7711A works in hiccup mode until the fault is removed.
Absolute Maximum Ratings  (Note 1)

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Symbol</th>
<th>Test Conditions</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>VDD to GND</td>
<td></td>
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<tr>
<td>GATE to GND</td>
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<tr>
<td>DMAG, COMP, CS to GND</td>
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<td>Power Dissipation, $P_D @ T_A = 25^\circ C$</td>
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<tr>
<td>SOT-23-6</td>
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<td>Package Thermal Resistance</td>
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<tr>
<td>SOT-23-6, $\theta_{JA}$</td>
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<td>Junction Temperature</td>
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<tr>
<td>Lead Temperature (Soldering, 10 sec.)</td>
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<tr>
<td>Storage Temperature Range</td>
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<td>ESD Susceptibility (Note 3)</td>
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<tr>
<td>HBM (Human Body Model)</td>
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<tr>
<td>MM (Machine Model)</td>
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</tbody>
</table>

Recommended Operating Conditions  (Note 4)

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Symbol</th>
<th>Test Conditions</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Unit</th>
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</thead>
<tbody>
<tr>
<td>VDD Supply Voltage, $V_{DD}$</td>
<td></td>
<td></td>
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<tr>
<td>Junction Temperature Range</td>
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<tr>
<td>Ambient Temperature Range</td>
<td></td>
<td></td>
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</table>

Electrical Characteristics  
($V_{DD} = 15V, T_A = 25^\circ C$, unless otherwise specified)

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Symbol</th>
<th>Test Conditions</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>VDD Section</td>
<td></td>
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<td></td>
<td></td>
<td></td>
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<tr>
<td>VDD Over-Voltage Protection Threshold</td>
<td>$V_{TH_VDDOV}$</td>
<td>$V_{DD}$ Rising</td>
<td>26</td>
<td>27</td>
<td>28</td>
<td>V</td>
</tr>
<tr>
<td>UVLO-On Threshold Voltage</td>
<td>$V_{TH_ON}$</td>
<td></td>
<td>13.5</td>
<td>14.5</td>
<td>15.5</td>
<td>V</td>
</tr>
<tr>
<td>UVLO-Off Threshold Voltage</td>
<td>$V_{TH_OFF}$</td>
<td></td>
<td>7.5</td>
<td>8.5</td>
<td>9.5</td>
<td>V</td>
</tr>
<tr>
<td>VDD Start-up Current</td>
<td>$I_{DD_ST}$</td>
<td>$V_{DD} &lt; V_{TH_ON}$ - 0.1V</td>
<td>--</td>
<td>--</td>
<td>10</td>
<td>$\mu A$</td>
</tr>
<tr>
<td>VDD Operating Current</td>
<td>$I_{DD_OP}$</td>
<td>GATE and COMP pin open</td>
<td>0.3</td>
<td>0.5</td>
<td>0.7</td>
<td>mA</td>
</tr>
<tr>
<td>Oscillator</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Normal Oscillator Frequency at PWM-Mode</td>
<td>$f_{PWM}$</td>
<td>$V_{COMP} &gt; V_{TH_FRH}$</td>
<td>60</td>
<td>65</td>
<td>70</td>
<td>kHz</td>
</tr>
<tr>
<td>Frequency ($f_{PWM}$) Variation Versus VDD Voltage Deviation</td>
<td>$f_{DV}$</td>
<td>$V_{DD}$ = 11V to 24V</td>
<td>--</td>
<td>--</td>
<td>2</td>
<td>%</td>
</tr>
<tr>
<td>Frequency ($f_{PWM}$) Variation Versus Junction Temperature Deviation</td>
<td>$f_{DT}$</td>
<td>$T_A$ = –25°C to 85°C (Note 5)</td>
<td>--</td>
<td>--</td>
<td>6</td>
<td>%</td>
</tr>
<tr>
<td>Jitter Frequency Range</td>
<td>$\Delta f$</td>
<td></td>
<td>--</td>
<td>±6</td>
<td>--</td>
<td>%</td>
</tr>
<tr>
<td>Jitter Frequency Period</td>
<td>$T_{JITTER}$</td>
<td>$V_{COMP} &gt; V_{TH_FRH}$</td>
<td>--</td>
<td>4</td>
<td>--</td>
<td>ms</td>
</tr>
<tr>
<td>Burst Mode Frequency</td>
<td>$f_{BURST}$</td>
<td>$V_{TH_BURST} &lt; V_{COMP} &lt; V_{TH_FRL}$</td>
<td>--</td>
<td>1</td>
<td>--</td>
<td>kHz</td>
</tr>
<tr>
<td>Minimum Frequency</td>
<td>$f_{MIN}$</td>
<td>$V_{COMP} &lt; V_{TH_BURST}$</td>
<td>--</td>
<td>250</td>
<td>--</td>
<td>Hz</td>
</tr>
<tr>
<td>Parameter</td>
<td>Symbol</td>
<td>Test Conditions</td>
<td>Min</td>
<td>Typ</td>
<td>Max</td>
<td>Unit</td>
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<td>-----------------------------------------------</td>
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</tr>
<tr>
<td>GATE Maximum Duty Cycle</td>
<td>$D_{MAX}$</td>
<td></td>
<td>72</td>
<td>77</td>
<td>82</td>
<td>%</td>
</tr>
<tr>
<td>GATE Minimum On-Time</td>
<td>$T_{ON_MIN}$</td>
<td>$I_{CLAMP} = 1,mA$</td>
<td>--</td>
<td>700</td>
<td>--</td>
<td>ns</td>
</tr>
<tr>
<td></td>
<td></td>
<td>$I_{CLAMP} = 250,\mu A$</td>
<td>--</td>
<td>2800</td>
<td>--</td>
<td>ns</td>
</tr>
<tr>
<td><strong>COMP Input Section</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
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<tr>
<td>Frequency Reduction Mode High Threshold</td>
<td>$V_{TH_FRH}$</td>
<td></td>
<td>--</td>
<td>3.2</td>
<td>--</td>
<td>V</td>
</tr>
<tr>
<td>Frequency Reduction Mode Low Threshold</td>
<td>$V_{TH_FRL}$</td>
<td></td>
<td>--</td>
<td>1.5</td>
<td>--</td>
<td>V</td>
</tr>
<tr>
<td>Burst Mode Threshold</td>
<td>$V_{TH_BURST}$</td>
<td></td>
<td>--</td>
<td>1.1</td>
<td>--</td>
<td>V</td>
</tr>
<tr>
<td>Maximum COMP Open Voltage</td>
<td>$V_{COMP_OP}$</td>
<td></td>
<td>--</td>
<td>4.5</td>
<td>--</td>
<td>V</td>
</tr>
<tr>
<td><strong>Current Sense Section</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Reference for Constant Current Control Mode</td>
<td>$K_{CC}$</td>
<td>$K_{CC} = V_{TH_CC} \times T_{ON_D}$</td>
<td>4.37</td>
<td>4.700</td>
<td>5.03</td>
<td>$\mu s \times V$</td>
</tr>
<tr>
<td>CS Over-Current Protection Threshold</td>
<td>$V_{TH_OC}$</td>
<td></td>
<td>--</td>
<td>1.7</td>
<td>--</td>
<td>V</td>
</tr>
<tr>
<td>CS Leading Edge Blanking Time</td>
<td>$T_{LEB}$</td>
<td>(Note 5)</td>
<td>300</td>
<td>375</td>
<td>450</td>
<td>ns</td>
</tr>
<tr>
<td>CS-to-GATE Propagation Delay Time</td>
<td>$T_{PD}$</td>
<td>(Note 5)</td>
<td>--</td>
<td>100</td>
<td>--</td>
<td>ns</td>
</tr>
<tr>
<td>Current Ratio of CS Sourcing to DMAG Sourcing Current</td>
<td>$K_I$</td>
<td>$K_I = I_{CS} / I_{CLAMP,@,GATE,turn-on}$</td>
<td>--</td>
<td>0.02</td>
<td>--</td>
<td>A/A</td>
</tr>
<tr>
<td><strong>Voltage Feedback Compensation Section</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Reference Voltage for CV Regulation</td>
<td>$V_{REF}$</td>
<td>(Note 5)</td>
<td>2.45</td>
<td>2.5</td>
<td>2.55</td>
<td>V</td>
</tr>
<tr>
<td>Gain of Operational Transconductance Amplifier (OTA)</td>
<td>$gm$</td>
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<td>--</td>
<td>$\mu A/V$</td>
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<td>--</td>
<td>$\mu A$</td>
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<td>Maximum Clamp Current of DMAG</td>
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<td>--</td>
<td>$\mu A$</td>
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<td><strong>Gate Driver Section</strong></td>
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<tr>
<td>Rising Time of GATE Output Voltage</td>
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<td>$C_L = 1,nF$</td>
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<td>Falling Time of GATE Output Voltage</td>
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<td>GATE Output Clamping Voltage</td>
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### Protection Section

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<td>Sampled on the DMAG pin at the Knee point</td>
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<td>1.2</td>
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<td>V</td>
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<td>Output Under-Voltage Debounce Time</td>
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<td>Maximum Duty Protection Debounce Time</td>
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<td>--</td>
<td>°C</td>
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</table>

**Note 1.** Stresses beyond those listed "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions may affect device reliability.

**Note 2.** θ_{JA} is measured at T_{A} = 25°C on a low effective thermal conductivity single-layer test board per JEDEC 51-3.

**Note 3.** Devices are ESD sensitive. Handling precaution is recommended.

**Note 4.** The device is not guaranteed to function outside its operating conditions.

**Note 5.** f_{DT}, leading edge blanking time, internal propagation delay time and VREF are guaranteed by design.
Typical Application Circuit
Typical Operating Characteristics

- **VDD OVP Threshold vs. Junction Temperature**
- **VDD Operating Current vs. Junction Temperature**
- **UVLO-On Threshold Voltage vs. Junction Temperature**
- **UVLO-Off Threshold Voltage vs. Junction Temperature**
- **VDD Start-up Current vs. Junction Temperature**
- **PWM Oscillator Frequency vs. Junction Temperature**
Oscillator Frequency vs. COMP Voltage

Converter Constant Current vs. Ambient Temperature

Constant Output Current at $T_A = 25^\circ C = 1A$
R7711A

Application Information

General Description

The R7711A is a peak current-mode PWM controller designed for off-line flyback converter and can achieve accurate CV or CC regulation, as shown in Figure 9.

The Figure 9 shows a typical curve of “output voltage vs. output current” of the charger using the R7711A. If the output current is less than the CC regulated level (I_{OUT_CC}), the CV regulation loop takes control of the converter and regulates the output voltage at the preset voltage level (V_{OUT_SET}). In the CV operation, a cable drop compensation for function adaptively compensates the voltage drop of the output cable and green mode operations, including frequency reduction and burst-mode functions, improve the efficiency of power conversion over the no load to full load range.

In CC operation, the converter works like a current source by regulating the output current at the preset current level (I_{OUT_CC}). In CC operation, a programmable propagation delay compensation reduces the CC variation, which is caused by feedback-loop propagation delay, over the full AC input voltage range.

Once the output voltage is below the under-voltage threshold (V_{OUT_MIN}), the R7711A shuts off the output protect the load and converter. After the output is shut down for a while, the R7711A attempts to regulate the output again without fault latching, resulting in hiccup operation.

Start-up Resistance

The Figure 10 shows the start-up circuit of the R7711A converter at the initial state of power-on condition. The total start-up resistance (R_{ST}) can be calculated by using the following equation:

\[ R_{ST} = \frac{\sqrt{2} \cdot V_{AC\_MIN} - V_{TH\_ON}}{C_{VDD} \cdot V_{TH\_ON} + I_{DD\_ST}} \]

- \( V_{AC\_MIN} \): minimum AC input voltage (90V_{rms} in general)
- \( V_{TH\_ON} \): VDD on threshold voltage (15V max.)
- \( C_{VDD} \): VDD capacitance
- \( T_{ST} \): start-up time of the converter (< 3s in general)
- \( I_{DD\_ST} \): VDD start-up current at the V_{DD} = V_{TH\_ON} - 0.1V

Calculation of the Current-Sensing Resistance

Refer to the Figure 2 and Figure 3. The current-sensing resistance (R_{CS}) can be calculated by using the following equation:

\[ R_{CS} = \frac{1}{2} \cdot \frac{N_p}{N_S} \cdot \frac{K_{CC} \cdot f_{PWM}}{I_{OUT\_CC\_SET}} \]

- \( I_{OUT\_CC\_SET} \): preset output current in CC operation
- \( K_{CC} \): regulated parameter in CC operation
- \( f_{PWM} \): average switching frequency of the converter
- \( N_p \): turns of the primary winding
- \( N_S \): turns of the secondary winding

Figure 9. Output Voltage vs. Output Current

Figure 10. Start-up Circuit
Magnetizing Inductance

The range of the primary-side magnetizing inductance ($L_m$) is mainly determined by two operating conditions. The first condition, "the calculated CS voltage threshold ($V_{TH\_CC}$) in CC operation is not allowed to exceed the maximum CS voltage threshold (1.1V typ.)." Thus, the minimum primary-side magnetizing inductance ($L_{m\_MIN}$) can be calculated by using the following equation:

$$L_{m\_MIN} = \left(\frac{N_P}{N_S}\right)^2 \frac{K_{CC}^2 \cdot f_{PWM} \cdot (V_{OPCB\_CC\(MAX\)) + V_{DO})}{2 \cdot I_{OUT\_CC\(SET\))} \cdot (0.85V)^2}$$

$V_{OPCB\_CC\(MAX\))$ : Max. converter output voltage on the PCB in CC operation (CV-to-CC corner)
$V_{DO}$ : forward voltage of the output diode ($D_O$)

The second condition prevents the converter from entering into CCM (Continuous Conduction Mode) operation. The worst condition happens in CC operation with the minimum output voltage ($V_{OPCB\_CC\(MIN\))$) and the minimum DC input voltage ($V_{IN\_MIN}$). Thus, the maximum primary-side magnetizing inductance ($L_{m\_MAX}$) is calculated by using the following equation:

$$L_{m\_MAX} = \left(\frac{N_P}{N_S}\right)^2 \frac{(V_{OPCB\_CC\(MIN\)) + V_{DO}) - V_{IN\_MIN}}{2 \cdot I_{OUT\_CC\(SET\))} \cdot 0.85}$$

$V_{OPCB\_CC\(MIN\))$ : Min. converter output voltage on the PCB in CC operation; 2.5V is recommended.
$V_{DO}$ : forward voltage of the output diode ($D_O$)

As shown in Figure 11, the “typical” value ($L_m$) of the selected magnetizing inductance must be greater/less than the $L_{m\_MIN}/L_{m\_MAX}$. The operating margins have been taken into consideration and the recommended tolerance of the $L_m$ is less than ±10%. Selecting a $L_m$ which is close to the $L_{m\_MIN}$ is recommended.

Leakage Inductance and Snubber Optimization

As shown in the Figure 12, when the MOSFET turns off, the leakage inductance and its current will induce the ringing voltage on DMAG pin. Due to the ringing voltage, the controller gets the wrong “knee point” detection and the output regulation is worse. Optimizing the leakage inductance and snubber design would reduce the ringing voltage and obtain the well output regulation.
When the GATE pin turns on the power MOSFET, the DMAG pin adaptively sources current to clamp the DMAG voltage near 0V. Meanwhile, the current flowing through the resistor RDMAG2 is proportional to the input voltage and used for the minimum on-time (TON_MIN) control. Therefore, the TON_MIN is adaptively modulated by the input voltage and can be programmed by the RDMAG2. When the GATE pin turns off the power MOSFET, the DMAG pin sinks the current, which is modulated by the COMP voltage and flows through the RDMAG2, to increase the voltage offset (ΔVDAMG2) for cable compensation, as shown in Figure 14. So, the RDAMG2 is concerned with the TON_MIN and cable compensation.

In general, the tD is close to a fixed value in a converter. Therefore, the propagation delay effect can be compensated by using the RPDC over full range of the VIN.

**DMAG pin Resistance**

As shown in Figure 13, the total propagation delay time (tD) of the CV/CC control loop includes the CS-to-GATE propagation delay (TPD) and the Q1 turn-off delay, which operates from the beginning of the falling GATE voltage to the time point when the VDRAIN is equal to the VIN. The tD increases the on-time (TON) of the power MOSFET (Q1) and the peak current (IDSPK) of the primary winding. Thus, the propagation delay effect increases the CC variation. The increment (ΔIDSPK) of the IDSPK can be calculated by using the following equation:

\[ \Delta \text{IDSPK} = \frac{V_{\text{IN}}}{L_{m}} \cdot tD = \frac{V_{\text{CSPK}} - V_{\text{TH,CC}}}{R_{CS}} \]

where:
- V_{\text{IN}}: input DC voltage of the converter
- L_{m}: primary-side magnetizing inductance
- V_{\text{CSPK}}: peak voltage of the CS voltage
- V_{\text{TH,CC}}: CS voltage threshold in CC operation

If the voltage offset (VPDC) between the resistor (RPDC) is equal to the (V_{\text{CSPK}}-V_{\text{TH,CC}}), the propagation delay effect is well compensated. It means the VR_{CSPK} is equal to the V_{\text{TH,CC}}. Thus, the RPDC can be calculated by using the following equation:

\[ R_{PDC} = \frac{R_{\text{DMAG2}}}{K_{i}} = \frac{N_{B}}{N_{A}} \cdot \frac{R_{CS} \cdot tD}{L_{m}} \]

where:
- K_{i}: current ratio of I_{CS} to I_{CLAMP}
- I_{CLAMP}: sourcing current of the voltage clamping circuit
- I_{CS}: sourcing current of the CS pin current during the on-state of the main switch (Q1)
- R_{CS}: current-sensing resistance

Second, the high-side resistance (R_{DMAG2}) can be calculated by using the following equation:

\[ R_{\text{DMAG2}} = 250 \cdot 10^{3} \cdot \frac{N_{A}}{N_{B}} \]

When the GATE pin turns on the power MOSFET, the DMAG pin adaptively sources current to clamp the DMAG voltage near 0V. Meanwhile, the current flowing through the resistor R_{DMAG2} is proportional to the input voltage and used for the minimum on-time (TON_MIN) control. Therefore, the TON_MIN is adaptively modulated by the input voltage and can be programmed by the R_{DMAG2}. When the GATE pin turns off the power MOSFET, the DMAG pin sinks the current, which is modulated by the COMP voltage and flows through the R_{DMAG2}, to increase the voltage offset (ΔVDAMG2) for cable compensation, as shown in Figure 14. So, the R_{DMAG2} is concerned with the TON_MIN and cable compensation. It can be calculated by using the following equations:

\[ R_{\text{DMAG2}} \geq 250 \cdot 10^{3} \cdot \frac{N_{A}}{N_{B}} \]

Second, the low-side feedback resistance (R_{DMAG1}) can be calculated by using the following equation:

\[ R_{\text{DMAG1}} = \frac{R_{\text{DMAG2}}}{V_{\text{OUT,SET}} + V_{\text{F}}} \cdot \frac{N_{A}}{N_{S}} \cdot -1 \]

where:
- V_{F}: the forward voltage of the DO with I_{DO} near 0A
DMAG Decoupling Capacitor

Figure 15. Comparison of the DMAG Voltage Waveforms

Figure 15 shows the DMAG voltage waveforms of the converter operating with no output current. In this condition, all of the time intervals, including the T\textsubscript{ON}, T\textsubscript{ON\_DO} and T\textsubscript{BLANK}, are minimum values. Once the settling time of the ringing voltage on the original DMAG voltage (V\textsubscript{DMAG1}) is more than the T\textsubscript{BLANK}, the ringing voltage may cause incorrect detection of the feedback signal and unstable CV regulation. As shown in Figure 14, the low-pass filter (including the C\textsubscript{DMAG} and the resistor-divider) is a possible solution used to filter the ringing voltage from the V\textsubscript{AUX}. After the low-pass filter is adopted, the smooth waveform (V\textsubscript{DMAG2}) of the DMAG voltage, shown in Figure 16, improves the detection of the feedback signal. The proper C\textsubscript{DMAG} is recommended in the following range:

\[
0.1\mu \leq \frac{R\textsubscript{DMAG1} + R\textsubscript{DMAG2}}{R\textsubscript{DMAG1} \cdot R\textsubscript{DMAG2}} \leq 0.7\mu \frac{R\textsubscript{DMAG1} + R\textsubscript{DMAG2}}{R\textsubscript{DMAG1} \cdot R\textsubscript{DMAG2}}
\]

It is recommended to be careful of output voltage regulation at light load or no load conditions with larger C\textsubscript{DMAG}.

Feedback Compensation

Figure 16. CV Control System Diagram in PFM Operation

The selected values of the compensation components (R\textsubscript{COMP} and C\textsubscript{COMP}) must meet the following equations:

\[
R\textsubscript{COMP} < \frac{R\textsubscript{DMAG1} + R\textsubscript{DMAG2}}{2 \cdot R\textsubscript{DMAG1} \cdot R\textsubscript{DMAG2} \cdot 0.4} \cdot \frac{1}{\mu A^2}
\]

\[
R\textsubscript{COMP} < \frac{R\textsubscript{DMAG1} + R\textsubscript{DMAG2}}{R\textsubscript{DMAG1} \cdot 50 (\mu A) \cdot 38824 (1/V) \cdot F \cdot \frac{N\textsubscript{A}}{N\textsubscript{S}} + R\textsubscript{DMAG2} \cdot 8 (\mu A/V)}
\]

\[
F = \frac{1}{4 \cdot \pi \cdot \sqrt{\frac{L\textsubscript{m} \cdot C\textsubscript{O}}{0.7ns \cdot A \cdot N\textsubscript{P} \cdot R\textsubscript{DMAG2} \cdot \frac{N\textsubscript{A}}{N\textsubscript{S}}}}
\]

\[
C\textsubscript{COMP} > \frac{2 \cdot \pi \cdot R\textsubscript{COMP}^2 \cdot \frac{N\textsubscript{A}}{N\textsubscript{S}} \cdot 38824 (1/KHz) \cdot F}{2 \cdot \pi \cdot R\textsubscript{COMP} \cdot C\textsubscript{COMP} - 1}
\]

The C\textsubscript{3} is used to filter the high-frequency switching noise on the COMP pin. The C\textsubscript{3} can be determined by the following equation:

\[
C\textsubscript{3} < \frac{C\textsubscript{COMP}}{60kHz \cdot \pi \cdot R\textsubscript{COMP} \cdot C\textsubscript{COMP} - 1}
\]
Thermal Considerations

For continuous operation, do not exceed absolute maximum operation junction temperature. The maximum power dissipation depends on the thermal resistance of IC package, PCB layout, the rate of surroundings airflow and temperature difference between junction to ambient. The maximum power dissipation can be calculated by following formula:

\[ P_{D(\text{MAX})} = \frac{T_{J(\text{MAX})} - T_A}{\theta_{JA}} \]

Where \( T_{J(\text{MAX})} \) is the maximum operation junction temperature, \( T_A \) is the ambient temperature and the \( \theta_{JA} \) is the junction to ambient thermal resistance.

For recommended operating conditions specification, the maximum junction temperature is 125°C. The junction to ambient thermal resistance \( \theta_{JA} \) is layout dependent. For SOT-23-6 package, the thermal resistance \( \theta_{JA} \) is 260.7°C/W on the standard JEDEC 51-3 single layer thermal test board. The maximum power dissipation at \( T_A = 25^\circ\text{C} \) can be calculated by following formula:

\[ P_{D(\text{MAX})} = \frac{(125^\circ\text{C} - 25^\circ\text{C})}{(260.7^\circ\text{C}/W)} = 0.38\text{W} \] for SOT-23-6 package.

The maximum power dissipation depends on operating ambient temperature for fixed \( T_{J(\text{MAX})} \) and thermal resistance \( \theta_{JA} \). The Figure 17 of derating curve allows the designer to see the effect of rising ambient temperature on the maximum power dissipation allowed.

![Figure 17. Derating Curve of Maximum Power Dissipation](Single Layer PCB)

Layout Considerations

A proper PCB layout can abate unknown noise interference and EMI issue in the switching power supply. Please refer to the guidelines when you want to design PCB layout for switching power supply:

- The current path (1) from bulk capacitor, transformer, MOSFET, RCS return to bulk capacitor is a huge high frequency current loop. It must be as short as possible to decrease noise coupling and kept a space to other low voltage traces, such as IC control circuit paths, especially. Besides, the path (2) from RCD snubber circuit to MOSFET is also a high switching loop so keep it as small as possible.

- It is good for reducing noise, output ripple and EMI issue to separate ground traces of bulk capacitor (a), MOSFET (b), auxiliary winding (c) and IC control circuit (d). Finally, connect them together on bulk capacitor ground (a). The areas of these ground traces should be kept large.

- Placing bypass capacitor for abating noise on IC is highly recommended. The bypass capacitor should be placed as close to controller as possible.

- In order to minimize reflected trace inductance and EMI, it is minimized the area of the loop connecting the secondary winding, the output diode, and the output filter capacitor must be kept small. In addition, apply sufficient copper area at the anode and cathode terminal of the diode for heatsinking. Apply a larger area at the quiet cathode terminal. A large anode area can increase high-frequency radiated EMI.

- For R7711A applications, it is better to keep the trace from voltage divider resistors close to the DMAG pin.
Figure 18. PCB Layout Guide
Outline Dimension

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SOT-23-6 Surface Mount Package