Primary Feedback CC/CV PWM Controller for Flyback Converters

General Description

The R7711A is a current mode PWM controller which includes primary side voltage feedback technology. It controls the output voltage and current accurately without shunt regulator and opto-coupler on secondary side to reduce the part count and save costs.

The R7711A is designed especially for low power applications, such as chargers for cell phones, PDAs, and other mobile products. Complete protections are provided, such as output Under- Voltage Protection, output Over-Voltage Protection, VDD Over-Voltage Protection, Over-Temperature Protection, and Secondary Rectifier Short-circuit Protection. The ultra low start-up current and operating current of the R7711A achieves low power consumption in standby mode. The R7711A supports green-mode operation to meet CEC regulations and Energy-Star requirements.

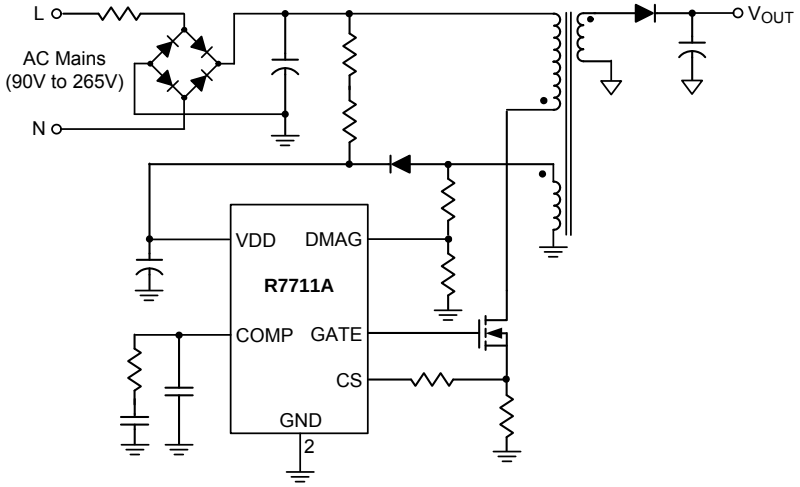
Features

- **Programmable Primary-Side CC/CV Regulation**
- **Low No Load Input Power (<30mW at 230V_{AC})**
- **Green Mode PWM Operation**
  - **Low Start-up Current (<10mA)**
  - **Triple Mode PWM Operation**
- **Easy EMI Solution**
  - **Built-in Jittering Frequency**
  - **Built-in Soft Gate Driver**
- **Programmable Cable Drop Compensation**
- **Adjustable Propagation Delay Compensation**
- **VDD Over-Voltage Protection(VDDOVP)**
- **Output Over-Voltage Protection(OVP)**
- **Output Under-Voltage Protection(UVP)**
- **Secondary Rectifier Short-Circuit Protection (SRSP)**
- **Internal Over-Temperature Protection(OTP)**
- **RoHS Compliant and Halogen Free**

Applications

- Switching AC/DC Adaptor and Battery Charger
- DVD Open Frame Power Supply
- STB Power
- Cell Phone Charger
- Networking Power Supply

Simplified Application Circuit



Ordering Information

R7711A □□

Package Type
E : SOT-23-6

Lead Plating System
G : Green (Halogen Free and Pb Free)

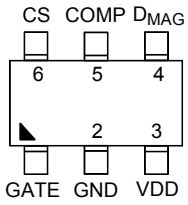
Note :

Richtek products are :

- RoHS compliant and compatible with the current requirements of IPC/JEDEC J-STD-020.
- Suitable for use in SnPb or Pb-free soldering processes.

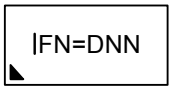
Pin Configurations

(TOP VIEW)



SOT-23-6

Marking Information



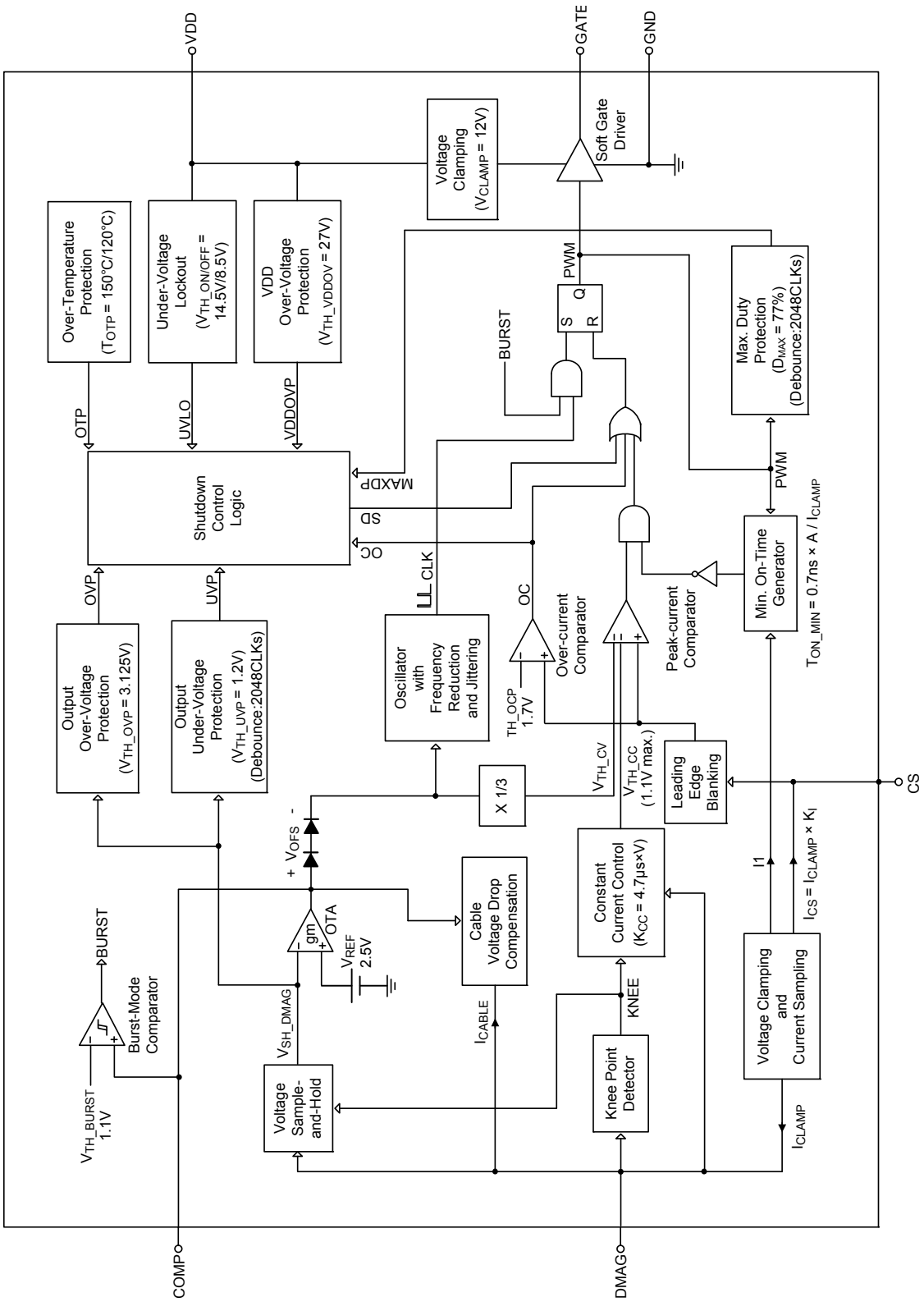
IFN= : Product Code

DNN : Date Code

Functional Pin Description

Pin No.	Pin Name	Pin Function
1	GATE	MOSFET Gate Driver Output. Connect this pin to the Gate of an external N-Channel power MOSFET.
2	GND	Ground of the Controller.
3	VDD	Power Supply Input. The controller will be enabled when V_{DD} exceeds V_{TH_ON} and disabled when V_{DD} decreases lower than V_{TH_OFF}.
4	DMAG	Demagnetization Pin. Input and Output Voltage Detection from Auxiliary Winding. The current (I_{CABLE}) flows into this pin to achieve cable drop compensation function. This pin is also used to detect the signal of the rectified input voltage for propagation delay compensation and minimum on-time control.
5	COMP	Feedback Compensation Pin. This pin is the output of the internal operational transconductance amplifier (OTA) to connect a proper RC network from this pin to GND for feedback loop compensation.
6	CS	Current Sensing Input. Connect this pin to a current sense resistor used to detect the current of the primary-side winding.

Function Block Diagram



Operation

General Description

The R7711A is a peak current-mode PWM controller designed for off-line flyback converter in DCM (Discontinuous Conduction Mode) operation. It can achieve accurate CV (Constant-Voltage) or CC (Constant-Current) output without voltage and current sensing circuits on the secondary side, as shown the Figure 1. When the output voltage is below the under-voltage threshold (V_{OUT_MIN}), the R7711A works in hiccup mode.

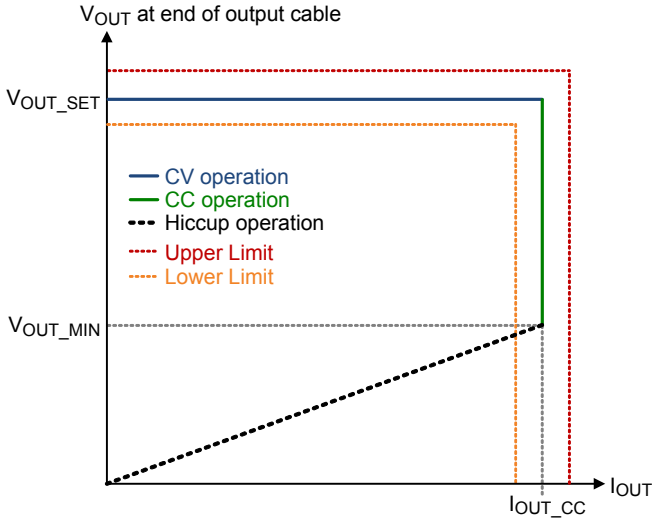


Figure 1. Output Voltage vs. Output Current

Constant-Voltage Operation

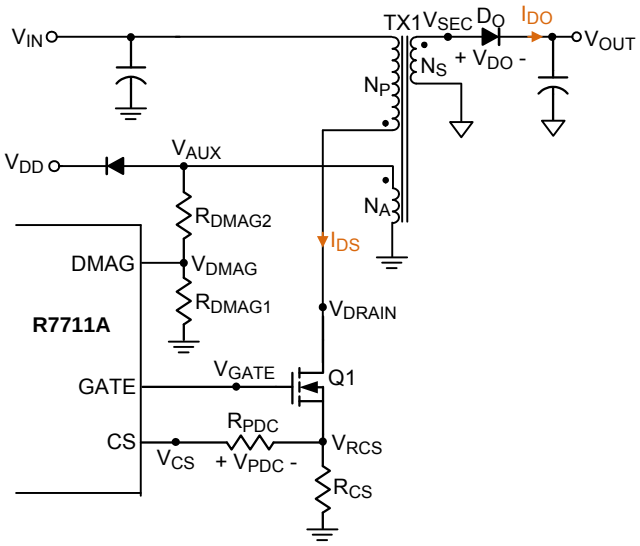
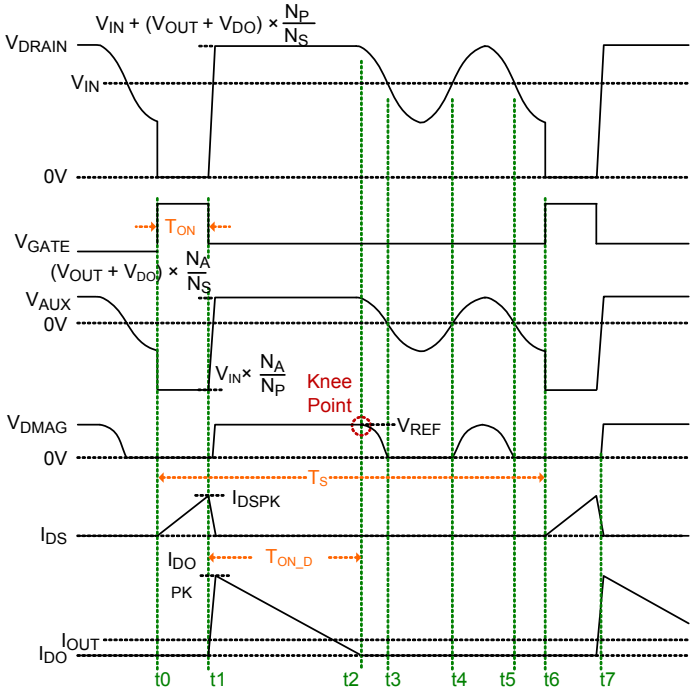


Figure 2. Simplified Circuit and Symbol Definition



t0 ~ t1 (T_{ON}) : Q1 is turned on.
t1 ~ t2 (T_{ON_D}) : D_O is turned on.
t2 : Knee point
t3 ~ t4, t5 ~ t7 : The DMAG voltage is clamped near 0V.
t0 ~ t6 (T_S) : Switcing period of the converter

Figure 3. Operating Waveforms

The Figure 2 shows the simplified primary-side-regulation circuit. The output voltage signal is indirectly detected via the transformer (TX1) and the resistor-divider (R_{DMAG1} and R_{DMAG2}). A "Knee point" detection and voltage sample-and-hold circuits are required for sensing the feedback voltage. The sample-and-hold voltage (V_{SH_DMAG}) of the V_{DMAG} is shown in the following equation :

$$V_{SH\_DMAG} = (V_{OUT} + V_F) \cdot \frac{N_A}{N_S} \cdot \frac{R_{DMAG1}}{R_{DMAG1} + R_{DMAG2}}$$

(at the Knee point)

V_F : the forward voltage of the D_O with I_{DO} near 0A

In the "Functional Block Diagram", the OTA compares the V_{REF} (V_{REF} = 2.5V typ.) and V_{SH_DMAG} to generate the error signal. The peak-current comparator compares the V_{COMP} with the current signal (V_{CS}) to determine the gate driver outputs duty cycle. The V_{COMP} is also used to modulate the oscillator frequency for green-mode operation.

Programmable Cable Drop Compensation

The R7711A features a cable drop compensation to adaptively compensate the output voltage drop effect due to the output cable impedance. As shown in the figure 4, The I_{CABLE}, proportional to the converter output current, creates an additional voltage offset (ΔV_{RDMAG2}) into the DMAG pin to achieve the cable compensation. The I_{CABLE} is calculated by using the following equation :

I_{CABLE} = 8μA/V x V_{COMP} –11.2μA ($I_{CABLE} \geq 0$)

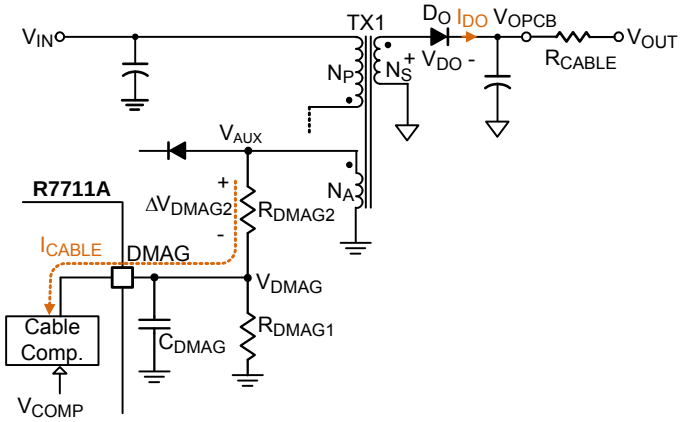


Figure 4. DMAG Current for Cable Compensation

Voltage Clamping Circuit and Propagation Delay Compensation

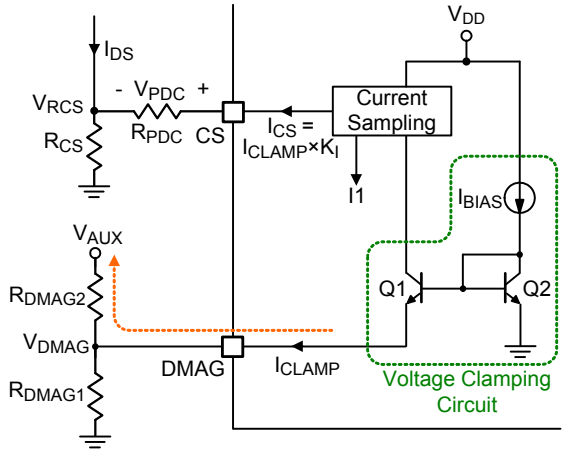


Figure 5. Voltage Clamping Circuit

Please refer to Figure 5. The DMAG pin is equipped with a low-level voltage clamping circuit to prevent the IC from being damaged by negative voltage. During the t0~t1 as the Figure 3, the main switch (Q1) is turned on, and the circuit outputs the current (I_{CLAMP}) to clamp the V_{DMAG} near 0V when the voltage (V_{AUX}) of auxiliary winding is negative. The I_{CLAMP} is calculated by using the following equation :

$$I_{CLAMP} = \frac{V_{IN}}{R_{DMAG2}} \cdot \frac{N_A}{N_P}$$

The R7711A also provides propagating delay compensation through the CS pin. The I_{CS} (= I_{CLAMP} x K_I), proportional to line voltage on the CS pin, and the R_{PDC} compensate for the propagation delay effect of the CC control loop. Thus, the constant current output can be very close to the preset level at high and low line voltages.

Triple Mode PWM Operation

In Figure 6, the triple mode PWM operation provides excellent green power performance, especially under light load and no load conditions.

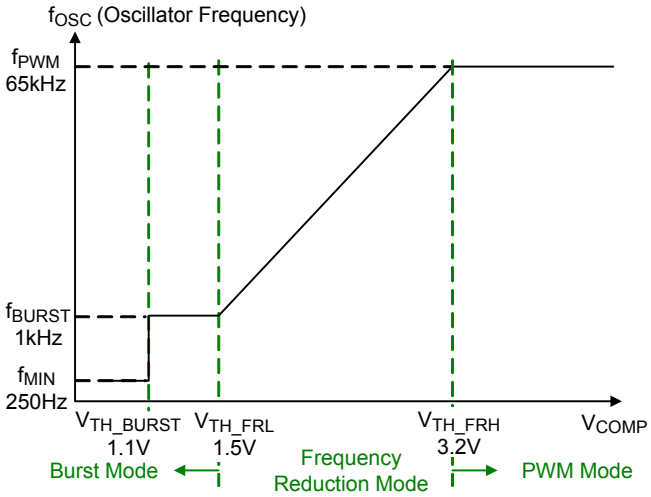


Figure 6. Switching Frequency vs. COMP Voltag

PWM Mode

For improving the efficiency in heavy load conditions, the RT7711A is equipped with a PWM mode operation. In the Figure 6, when the COMP voltage is larger than the voltage threshold (V_{TH_FRH}), the controller enters PWM mode. In this mode, the average switching frequency is fixed at 65kHz (f_{PWM} , typ.)

Frequency Reduction Mode

In Figure 6, to reduce switching losses, the Frequency Reduction (FR) mode is designed to operate at middle load current conditions with the COMP voltage (V_{COMP}) between the voltage thresholds V_{TH_FRH} (3.2V typ.) and V_{TH_FRL} (1.5V typ.). In this mode, the switching frequency, from 65kHz to 1kHz, is linearly modulated by the V_{COMP}.

Burst Mode

To further reduce the switching losses in no load or very light load condition, a burst mode control reduces the average switching frequency when the V_{COMP} is below the V_{TH_FRL} (1.5V typ.). A Burst-mode voltage threshold (V_{TH_BURST}=1.1V typ.) switches the operating frequency in either f_{BURST} (1kHz typ.) or f_{MIN} (250Hz typ.). The green mode operation meets the CEC regulations and Energy-Star requests.

Min. On-Time

To improve green power at light load or no load conditions, the R7711A works with a minimum on-time (T_{ON_MIN}) and the output voltage is regulated by the modulated switching frequency. The T_{ON_MIN}, shown as the following equation, is a function of the I_{CLAMP} :

$$T_{ON\_MIN} = \frac{0.7A \cdot ns}{I_{CLAMP}}$$

Constant-Current Operation

The R7711A features a patented constant current control circuit. The I_{OUT_CC} can be calculated as the following equation :

$$I_{OUT\_CC} \approx \frac{1}{2} \cdot \frac{N_P}{N_S} \cdot \frac{V_{TH\_CC} \cdot T_{ON\_D}}{R_{CS} \cdot T_S} = \frac{1}{2} \cdot \frac{N_P}{N_S} \cdot \frac{K_{CC}}{R_{CS} \cdot T_S}$$

V_{TH_CC} : CS voltage threshold in CC mode

T_{ON_D} : on time of the D_O

T_S : switching period of the converter

N_P : turns of the primary winding

R_{CS} : current-sensing resistance

If the "V_{TH_CC} x T_{ON_D}" is a constant, the I_{OUT_CC} is close to a constant in CC operation. In steady state, the parameter K_{CC} (= V_{TH_CC} x T_{ON_D}) is regulated at 4.7µs x V(typ.).

Adaptive Blanking Time

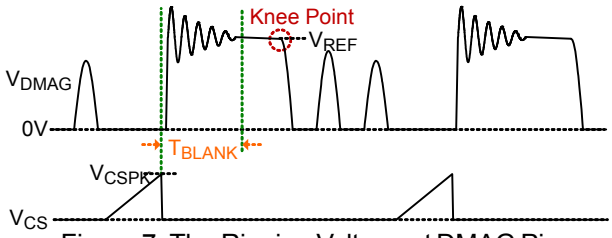


Figure 7. The Ringing Voltage at DMAG Pin

In Figure 7, the ringing waveform is induced by the leakage inductance and the peak current of the primary winding at the rising edge of the V_{DMAG}. It may cause improper knee point detection and further result in unstable operation. The magnitude and settling time of the voltage ringing increases larger at heavy loads with higher peak currents. Thus, the R7711A provides a modulated blanking time (T_{BLANK}) depending on the CS peak voltage (V_{CSPK}). The T_{BLANK} can be calculated by using the following equation :

T_{BLANK} = 1ms + V_{CSPK} × 3ms/V

V_{CSPK} : peak voltage of the CS voltage

Leading Edge Blanking (LEB) for V_{CS}

Due to the device's parasitic capacitors, an initial current spike appears at the rising edge of the GATE voltage (V_{GATE}). The spike of the CS voltage may incorrectly trigger the peak current comparator, to turn off the power MOSFET, resulting in running failure of the flyback converter. Thus, the LEB, used to mask the initial voltage spike on the CS pin, is a necessary design for successful PWM operation.

Frequency Jittering Function

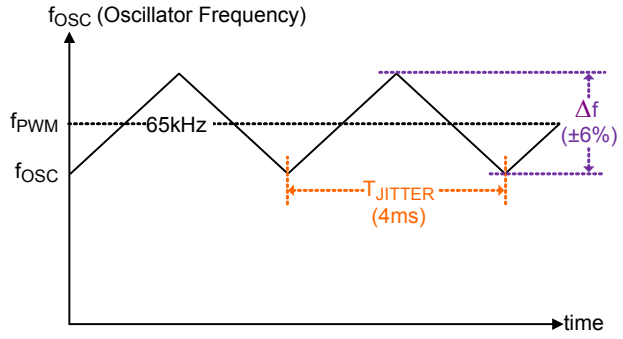


Figure 8. Oscillator Frequency with Jittering

A frequency jittering function is embedded to further reduce EMI (Electromagnetic Interference). In Figure 8, the function modulates the oscillator frequency in a triangular waveform with the period (T_{JITTER}) of 4ms(typ.). In this condition, the maximum average (f_{PWM}) of the oscillator frequency (f_{OSC}) is 65kHz (typ.) and the jittering frequency range (Δf) is ±6% of the f_{PWM}.

VDD Under-Voltage Lockout (UVLO) Protection

The R7711A automatically initializes upon receipt of the supply voltage (V_{DD}) on the VDD pin. The UVLO function continually monitors the V_{DD}. When the V_{DD} exceeds its rising UVLO threshold (V_{TH_ON} = 14.5V typ.), the IC is enabled. When the V_{DD} falls below the falling UVLO voltage threshold (V_{TH_OFF} = 8.5V typ.), the GATE voltage is pulled low to shut off the converter. The supply voltage (V_{DD}) must be below the absolute maximum rating for safety.

VDD Over-Voltage Protection (VDD OVP)

When the V_{DD} exceeds the VDD over-voltage threshold (V_{TH_VDDOV} = 27V typ.) in abnormal conditions, the GATE voltage is pulled low to shut off the converter and the R7711A works in hiccup mode until the fault is removed. This avoids permanent damage of the converter components . The VDD over-voltage may be caused by an incorrectly sensed feedback signal on the DMAG pin or an output over-voltage condition.

Output Over-Voltage Protection (OVP)

The R7711A provides accurate output OVP. Once the feedback voltage (V_{SH_DMAG}), sampled on the DMAG pin, is over 125% (typ.) of the reference voltage (V_{REF} = 2.5V typ.), the R7711A issues an output OVP signal to turn off the controller and prevent the loading device and converter from being damaged. Therefore, the OVP threshold on the output is about 125% of the CV output voltage at the end of the PCB. The R7711A works in hiccup mode until the fault is removed.

Output Under-Voltage Protection (UVP)

The output UVP is designed to protect the converter from the output short-circuit conditions. Once the feedback voltage (V_{SH_DMAG}), sampled on the DMAG pin, is below the voltage threshold (V_{TH_UVP} = 1.2V typ.), a built-in 11-bit digital timer performs a UVP debounce time (2048 switching cycles = about 30ms) before issuing the UVP signal. The UVP signal turns off the converter to prevent the loading device and converter from being damaged. The R7711A works in hiccup mode until the fault is removed.

Over-Temperature Protection (OTP)

The built-in OTP function continuously monitors the junction temperature (T_J) of the IC itself. Once the T_J exceeds the over-temperature level (T_{OTP} = 150°C typ.), the OTP signal turns off the converter and prevents the IC itself from suffering thermal stress and permanent damage. It's not suggested to use the function as a precise OTP. The R7711A works in hiccup mode until the fault is removed.

Secondary Rectifier Short-circuit Protection (SRSP)

The R7711A is equipped with an extra over-current protection (OCP) against secondary rectifier short-circuit conditions in flyback converter. When the secondary rectifier is damaged by short-circuit, the transformer operates in saturation area and huge current stress occurs on the main switch. When the V_{CS} reaches the OCP voltage threshold (V_{TH_OCP} = 1.7V typ.), the R7711A shuts down the converter after the debounce time of a few cycles. The R7711A works in hiccup mode until the fault is removed.

Absolute Maximum Ratings (Note 1)

- VDD to GND ---------- –0.3V to 28V
- GATE to GND ---------- –0.3V to 16V
- DMAG, COMP, CS to GND ---------- –0.3V to 6.5V
- Power Dissipation, P_D @ T_A = 25°C
  SOT-23-6 ---------- 0.38W
- Package Thermal Resistance (Note 2)
  SOT-23-6, θ_{JA} ---------- 260.7°C/W
- Junction Temperature ---------- 150°C
- Lead Temperature (Soldering, 10 sec.) ---------- 260°C
- Storage Temperature Range ---------- –65°C to 150°C
- ESD Susceptibility (Note 3)
  HBM (Human Body Model) ---------- 3kV
  MM (Machine Model) ---------- 250V

Recommended Operating Conditions (Note 4)

- VDD Supply Voltage, V_{DD} ---------- 11V to 24V
- Junction Temperature Range ---------- –40°C to 125°C
- Ambient Temperature Range ---------- –40°C to 85°C

Electrical Characteristics

(V_{DD} = 15V, T_A = 25°C, unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
VDD Section						
VDD Over-Voltage Protection Threshold	V_{TH_VDDOV}	VDD Rising	26	27	28	V
UVLO-On Threshold Voltage	V_{TH_ON}		13.5	14.5	15.5	V
UVLO-Off Threshold Voltage	V_{TH_OFF}		7.5	8.5	9.5	V
VDD Start-up Current	I_{DD_ST}	Rising V_{DD} < V_{TH_ON} - 0.1V	--	--	10	μA
VDD Operating Current	I_{DD_OP}	GATE and COMP pin open	0.3	0.5	0.7	mA
Oscillator						
Normal Oscillator Frequency at PWM-Mode	f_{PWM}	V_{COMP} > V_{TH_FRH}	60	65	70	kHz
Frequency (f_{PWM}) Variation Versus VDD Voltage Deviation	f_{DV}	V_{DD} = 11V to 24V	--	--	2	%
Frequency (f_{PWM}) Variation Versus Junction Temperature Deviation	f_{DT}	T_A = –25°C to 85°C (Note 5)	--	--	6	%
Jitter Frequency Range	Δf		--	±6	--	%
Jitter Frequency Period	T_{JITTER}	V_{COMP} > V_{TH_FRH}	--	4	--	ms
Burst Mode Frequency	f_{BURST}	V_{TH_BURST} < V_{COMP} < V_{TH_FRL}	--	1	--	kHz
Minimum Frequency	f_{MIN}	V_{COMP} < V_{TH_BURST}	--	250	--	Hz

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
GATE Maximum Duty Cycle	D_{MAX}		72	77	82	%
GATE Minimum On-Time	T_{ON_MIN}	I_{CLAMP} = 1mA	--	700	--	ns
		I_{CLAMP} = 250μA	--	2800	--	ns
COMP Input Section						
Frequency Reduction Mode High Threshold	V_{TH_FRH}		--	3.2	--	V
Frequency Reduction Mode Low Threshold	V_{TH_FRL}		--	1.5	--	V
Burst Mode Threshold	V_{TH_BURST}		--	1.1	--	V
Maximum COMP Open Voltage	V_{COMP_OP}		--	4.5	--	V
Current Sense Section						
Reference for Constant Current Control Mode	K_{CC}	$K_{CC} = V_{TH\_CC} \times T_{ON\_D}$	4.37	4.700	5.03	μs x V
CS Over-Current Protection Threshold	V_{TH_OC}		--	1.7	--	V
CS Leading Edge Blanking Time	T_{LEB}	(Note 5)	300	375	450	ns
CS-to-GATE Propagation Delay Time	T_{PD}	(Note 5)	--	100	--	ns
Current Ratio of CS Sourcing Current to DMAG Sourcing Current	K_I	$K_I = I_{CS} / I_{CLAMP}$ at GATE turn-on	--	0.02	--	A/A
Voltage Feedback Compensation Section						
Reference Voltage for CV Regulation	V_{REF}	(Note 5)	2.45	2.5	2.55	V
Gain of Operational Transconductance Amplifier (OTA)	gm	Input Voltage Difference = ±50mV	--	50	--	μA/V
Maximum COMP Sourcing/Sinking Current	I_{gm_MAX}		--	20	--	μA
Maximum Clamp Current of DMAG	I_{CLAMP_MAX}		1500	--	--	μA
Gate Driver Section						
Rising Time of GATE Output Voltage	T_R	C_L = 1nF	--	150	--	ns
Falling Time of GATE Output Voltage	T_F	C_L = 1nF	--	85	--	ns
GATE Output Clamping Voltage	V_{CLAMP}	V_{DD} = 20V, C_L = 1nF	--	12	--	V

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Protection Section						
Output Over-Voltage Protection Threshold	V_{TH_OVP}	Sampled on the DMAG pin at the Knee point	3	3.125	3.25	V
Output Under-Voltage Protection Threshold	V_{TH_UVP}	Sampled on the DMAG pin at the Knee point	--	1.2	--	V
Output Under-Voltage Debounce Time	T_{UVP_DE}	Count of clock cycles	--	2048	--	CLKs
Maximum Duty Protection Debounce Time	T_{DMAX_DE}	Duty = D_{MAX}, Count of clock cycles	--	2048	--	CLKs
Over-Temperature Protection Threshold	T_{OTP}		--	150	--	°C
Over-Temperature Protection Threshold Hysteresis	T_{OTP_HYS}		--	30	--	°C

Note 1. Stresses beyond those listed "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions may affect device reliability.

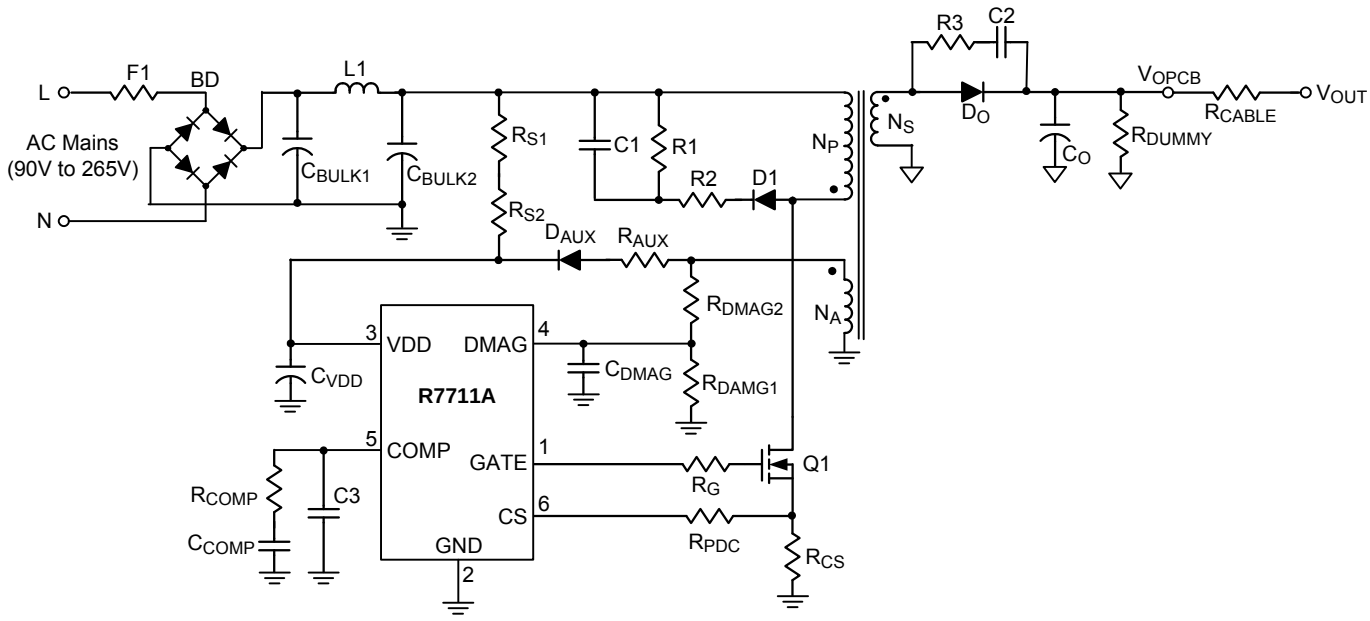
Note 2. θ_{JA} is measured at T_A = 25°C on a low effective thermal conductivity single-layer test board per JEDEC 51-3.

Note 3. Devices are ESD sensitive. Handling precaution is recommended.

Note 4. The device is not guaranteed to function outside its operating conditions.

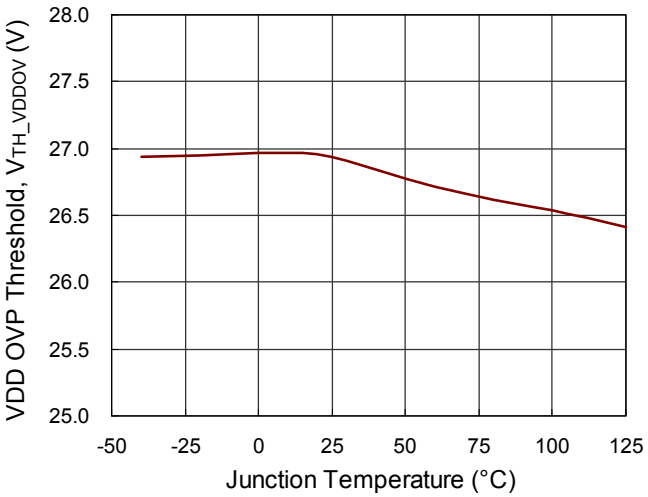
Note 5. f_{DT}, leading edge blanking time, internal propagation delay time and VREF are guaranteed by design.

Typical Application Circuit

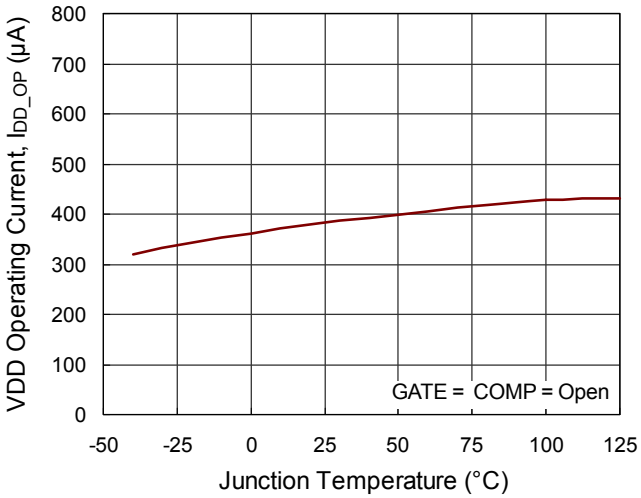


Typical Operating Characteristics

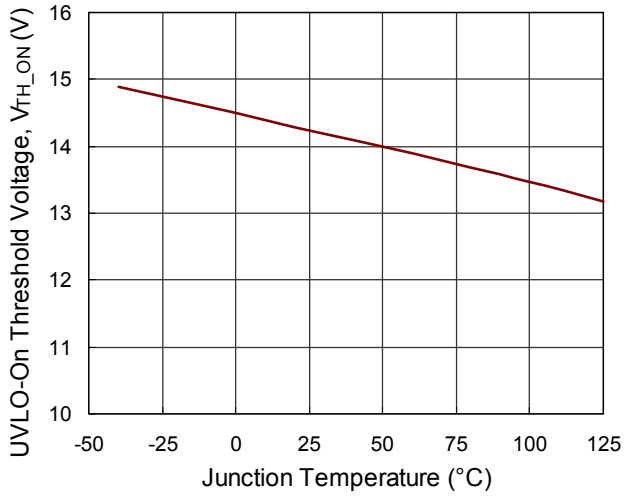
VDD OVP Threshold vs. Junction Temperature



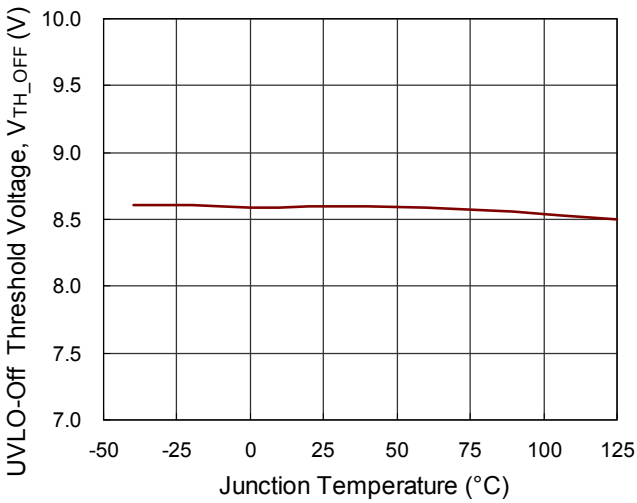
VDD Operating Current vs. Junction Temperature



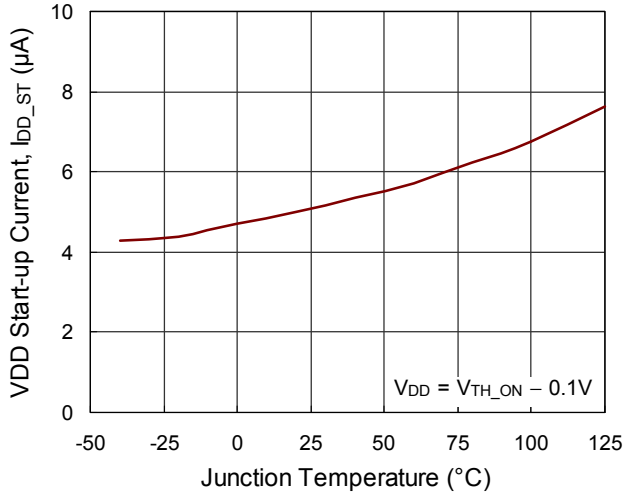
UVLO-On Threshold Voltage vs. Junction Temperature



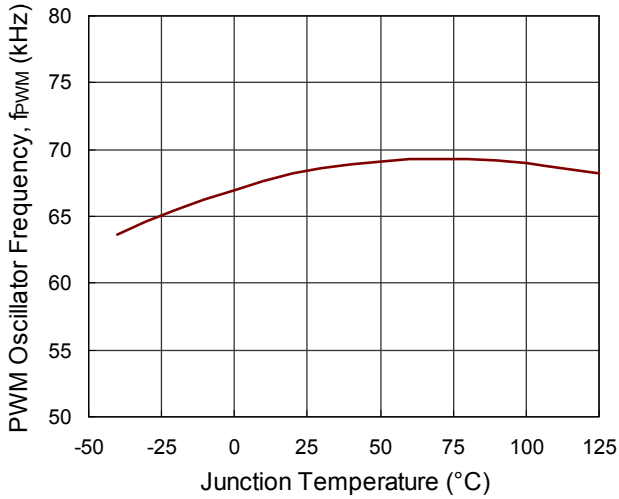
UVLO-Off Threshold Voltage vs. Junction Temperature



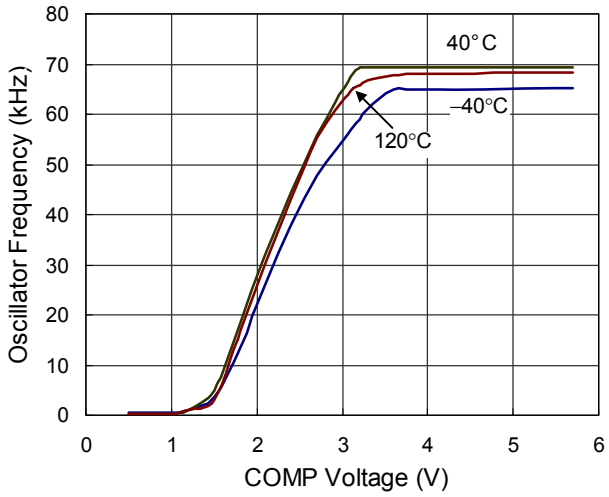
VDD Start-up Current vs. Junction Temperature



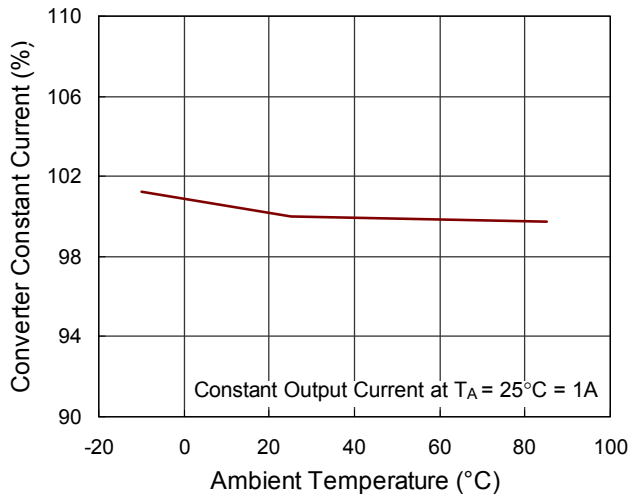
PWM Oscillator Frequency vs. Junction Temperature



Oscillator Frequency vs. COMP Voltage



Converter Constant Current vs. Ambient Temperature



Application Information

General Description

The R7711A is a peak current-mode PWM controller designed for off-line flyback converter and can achieve accurate CV or CC regulation, as shown in Figure 9.

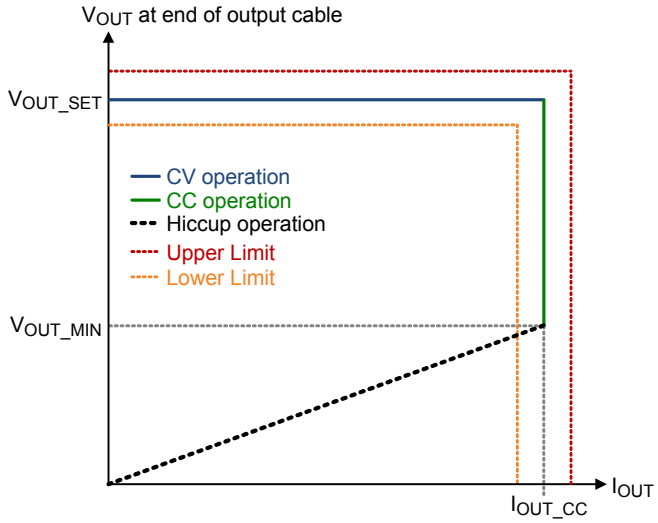


Figure 9. Output Voltage vs. Output Current

The Figure 9 shows a typical curve of "output voltage vs. output current" of the charger using the R7711A. If the output current is less than the CC regulated level (I_{OUT_CC}), the CV regulation loop takes control of the converter and regulates the output voltage at the preset voltage level (V_{OUT_SET}). In the CV operation, a cable drop compensation for function adaptively compensates the voltage drop of the output cable and green mode operations, including frequency reduction and burst-mode functions, improve the efficiency of power conversion over the no load to full load range.

In CC operation, the converter works like a current source by regulating the output current at the preset current level (I_{OUT_CC}). In CC operation, a programmable propagation delay compensation reduces the CC variation, which is caused by feedback-loop propagation delay, over the full AC input voltage range.

Once the output voltage is below the under-voltage threshold (V_{OUT_MIN}), the R7711A shuts off the output protect the load and converter. After the output is shut down for a while, the R7711A attempts to regulate the output again without fault latching, resulting in hiccup operation.

Start-up Resistance

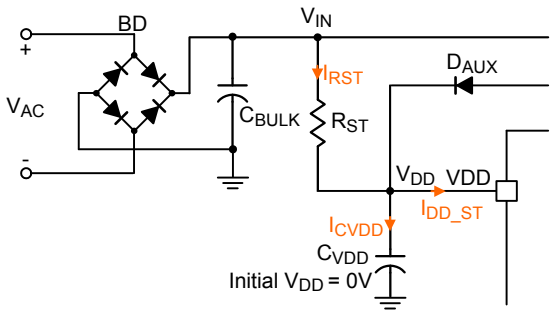


Figure 10. Start-up Circuit

The Figure 10 shows the start-up circuit of the R7711A converter at the initial state of power-on condition. The total start-up resistance (R_{ST}) can be calculated by using the following equation :

$$R_{ST} = \frac{\sqrt{2} \cdot V_{AC\_MIN} - V_{TH\_ON}}{\frac{C_{VDD} \cdot V_{TH\_ON}}{T_{ST}} + I_{DD\_ST}}$$

V_{AC_MIN} : minimum AC input voltage ($90V_{rms}$ in general)

V_{TH_ON} : VDD on threshold voltage (15V max.)

C_{VDD} : VDD capacitance

T_{ST} : start-up time of the converter (< 3s in general)

I_{DD_ST} : VDD start-up current at the $V_{DD} = V_{TH\_ON}$-0.1V

Calculation of the Current-Sensing Resistance

Refer to the Figure 2 and Figure 3. The current-sensing resistance (R_{CS}) can be calculated by using the following equation :

$$R_{CS} = \frac{1}{2} \cdot \frac{N_P}{N_S} \cdot \frac{K_{CC} \cdot f_{PWM}}{I_{OUT\_CC(SET)}}$$

$I_{OUT\_CC(SET)}$: preset output current in CC operation

K_{CC} : regulated parameter in CC operation

f_{PWM} : average switching frequency of the converter

N_P : turns of the primary winding

N_S : turns of the secondary winding

Magnetizing Inductance

The range of the primary-side magnetizing inductance (L_m) is mainly determined by two operating conditions. The first condition, "the calculated CS voltage threshold (V_{TH_CC}) in CC operation is not allowed to exceed the maximum CS voltage threshold (1.1V typ.)". Thus, the minimum primary-side magnetizing inductance (L_{m_MIN}) can be calculated by using the following equation :

$$L_{m\_MIN} = \left(\frac{N_P}{N_S}\right)^2 \cdot \frac{K_{CC}^2 \cdot f_{PWM} \cdot (V_{OPCB\_CC(MAX)} + V_{DO})}{2 \cdot I_{OUT\_CC(SET)} \cdot (0.85V)^2}$$

$V_{OPCB\_CC(MAX)}$: Max. converter output voltage on the PCB in CC operation (CV-to-CC corner)

V_{DO} : forward voltage of the output diode(D_O)

second condition prevents the converter from entering into CCM (Continuous Conduction Mode) operation. The worst condition happens in CC operation with the minimum output voltage ($V_{OPCB\_CC(MIN)}$) and the minimum DC input voltage (V_{IN_MIN}). Thus, the maximum primary-side inductance (L_{m_MAX}) is calculated by using the following equation :

$$L_{m\_MAX} = \frac{\left(\frac{N_P}{N_S}\right)^2 \cdot (V_{OPCB\_CC(MIN)} + V_{DO}) \cdot V_{IN\_MIN}^2 \cdot 0.85}{2 \cdot I_{OUT\_CC(SET)} \cdot \left[V_{IN\_MIN} + \frac{N_P}{N_S} \cdot (V_{OPCB\_CC(MIN)} + V_{DO})\right]^2 \cdot f_{PWM}}$$

$V_{OPCB\_CC(MIN)}$: Min. converter output voltage on the PCB in CC operation; 2.5V is recommended.

V_{DO} : forward voltage of the output diode(D_O)

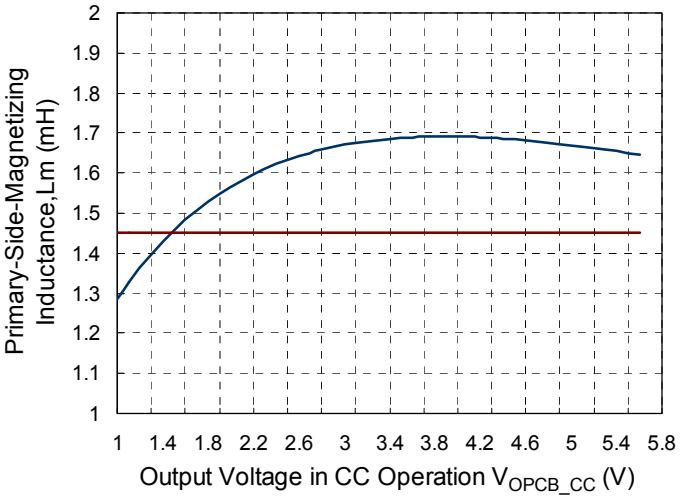


Figure 11. Curves of L_{m_MIN} and L_{m_MAX} vs. V_{OPCB_CC}

As shown in Figure 11, the "typical" value (L_m) of the selected magnetizing inductance must be greater/less than the L_{m_MIN} /L_{m_MAX}. The operating margins have been taken into consideration and the recommended tolerance of the L_m is less than ±10%. Selecting a L_m which is close to the L_{m_MIN} is recommended.

Leakage Inductance and Snubber Optimization

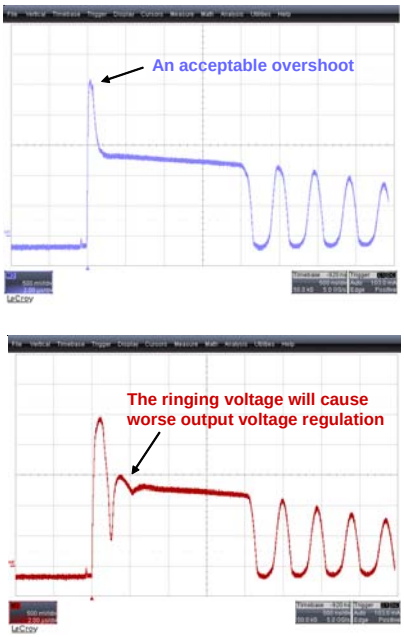


Figure 12. The ringing voltage on DMAG pin

As shown in the Figure 12, when the MOSFET turns off, the leakage inductance and its current will induce the ringing voltage on DMAG pin. Due to the ringing voltage, the controller gets the wrong "knee point" detection and the output regulation is worse. Optimizing the leakage inductance and snubber design would reduce the ringing voltage and obtain the well output regulation.

Propagation Delay Compensation

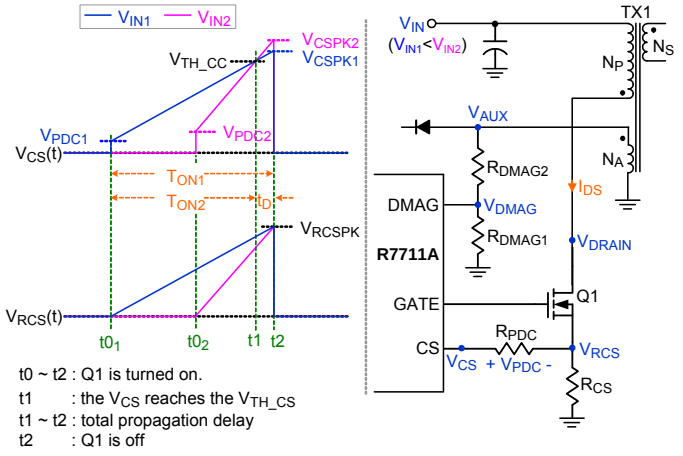


Figure 13. Illustration of Propagation Delay Compensation

As shown in Figure 13, the total propagation delay time (t_D) of the CV/CC control loop includes the CS-to-GATE propagation delay (T_{PD}) and the Q1 turn-off delay, which operates from the beginning of the falling GATE voltage to the time point when the V_{DRAIN} is equal to the V_{IN}. The t_D increases the on-time (T_{ON}) of the power MOSFET (Q1) and the peak current (I_{DSPK}) of the primary winding. Thus, the propagation delay effect increases the CC variation. The increment (ΔI_{DSPK}) of the I_{DSPK} can be calculated by using the following equation :

$$\Delta I_{DSPK} = \frac{V_{IN}}{L_m} \cdot t_D = \frac{V_{CSPK} - V_{TH\_CC}}{R_{CS}}$$

V_{IN} : input DC voltage of the converter

L_m : primary-side magnetizing inductance

V_{CSPK} : peak voltage of the CS voltage

V_{TH_CC} : CS voltage threshold in CC operation

If the voltage offset (V_{PDC}) between the resistor (R_{PDC}) is equal to the (V_{CSPK}-V_{TH_CC}), the propagation delay effect is well compensated. It means the V_{RCSPK} is equal to the V_{TH_CC}. Thus, the R_{PDC} can be calculated by using the following equation :

$$R_{PDC} = \frac{R_{DMAG2}}{K_I} \cdot \frac{N_P}{N_A} \cdot \frac{R_{CS} \cdot t_D}{L_m}$$

K_I : current ratio of I_{CS} to I_{CLAMP}

I_{CLAMP} : sourcing current of the voltage clamping circuit

I_{CS} : sourcing current of the CS pin current during the on-state of the main switch (Q1)

R_{CS} : current-sensing resistance

In general, the t_D is close to a fixed value in a converter. Therefore, the propagation delay effect can be compensated by using the R_{PDC} over full range of the V_{IN}.

DMAG pin Resistance

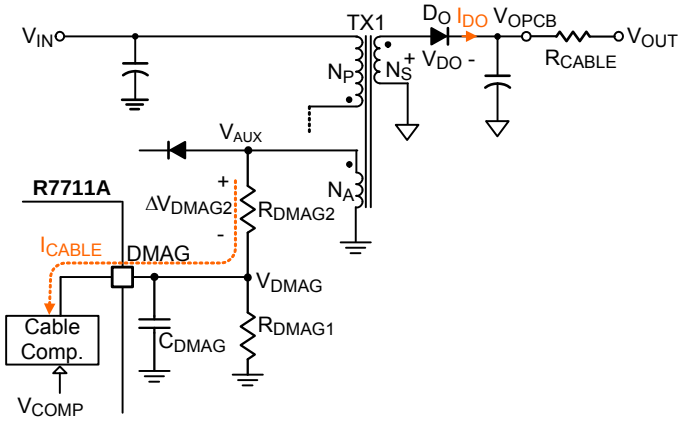


Figure 14. Block Diagram of the Cable Drop Comp

When the GATE pin turns on the power MOSFET, the DMAG pin adaptively sources current to clamp the DMAG voltage near 0V. Meanwhile, the current flowing through the resistor R_{DMAG2} is proportional to the input voltage and used for the minimum on-time (T_{ON_MIN}) control. Therefore, the T_{ON_MIN} is adaptively modulated by the input voltage and can be programmed by the R_{DMAG2}. When the GATE pin turns off the power MOSFET, the DMAG pin sinks the current, which is modulated by the COMP voltage and flows through the R_{DMAG2}, to increase the voltage offset (ΔV_{DAMG2}) for cable compensation, as shown in Figure 14. So, the R_{DAMG2} is concerned with the T_{ON_MIN} and cable compensation. It can be calculated by using the following equations :

$$R_{DMAG2} \geq 250 \cdot 10^3 \cdot \frac{N_A}{N_P}$$

R_{DMAG2} : the high-side resistance of the resistor-divider

Second, the low-side feedback resistance (R_{DMAG1}) can be calculated by using the following equation :

$$R_{DMAG1} = \frac{R_{DMAG2}}{\frac{V_{OUT\_SET} + V_F}{V_{REF}} \cdot \frac{N_A}{N_S} - 1}$$

V_F : the forward voltage of the D_O with I_{DO} near 0A

DMAG Decoupling Capacitor

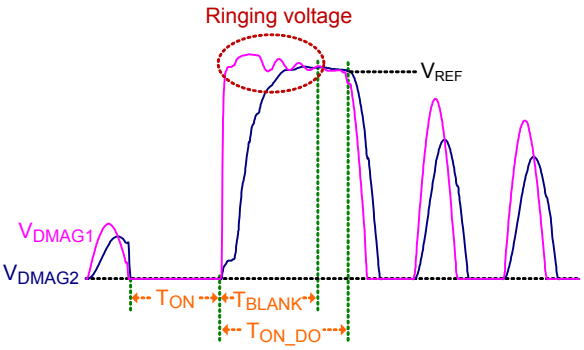


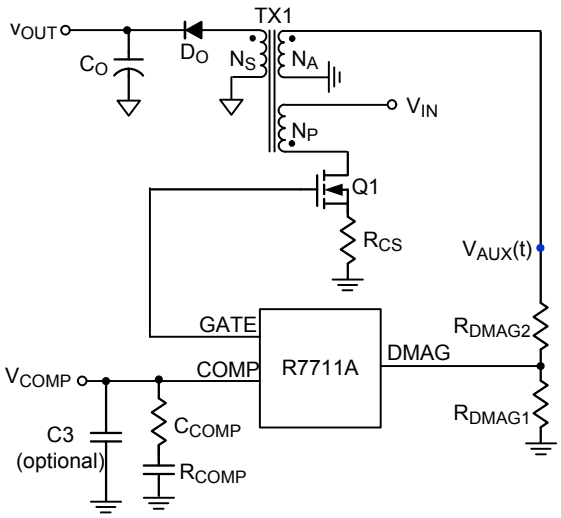
Figure 15. Comparison of the DMAG Voltage Waveforms

Figure 15 shows the DMAG voltage waveforms of the converter operating with no output current. In this condition, all of the time intervals, including the T_{ON}, T_{ON_DO} and T_{BLANK}, are minimum values. Once the settling time of the ringing voltage on the original DMAG voltage (V_{DMAG1}) is more than the T_{BLANK}, the ringing voltage may cause incorrect detection of the feedback signal and unstable CV regulation. As shown in Figure 14, the low-pass filter (including the C_{DMAG} and the resistor-divider) is a possible solution used to filter the ringing voltage from the V_{AUX}. After the low-pass filter is adopted, the smooth waveform (V_{DMAG2}) of the DMAG voltage, shown in Figure 16, improves the detection of the feedback signal. The proper C_{DMAG} is recommended in the following range :

$$\frac{0.1\mu\cdot(R_{DMAG1}+R_{DMAG2})}{R_{DMAG1}\cdot R_{DMAG2}} \le C_{DMAG} \le \frac{0.7\mu\cdot(R_{DMAG1}+R_{DMAG2})}{R_{DMAG1}\cdot R_{DMAG2}}$$

It is recommended to be careful of output voltage regulation at light load or no load conditions with larger C_{DMAG}.

Feedback Compensation



V_{OUT} : small signal of the converter output voltage
V_{COMP} : small signal of the OTA1 output voltage
V_{IN} : DC Input voltage of the converter
$V_{AUX}(t)$: switching voltage at the auxiliary winding

Figure 16. CV Control System Diagram in PFM Operation

The selected values of the compensation components (R_{COMP} and C_{COMP}) must meet the following equations :

$$R_{COMP} < \frac{R_{DMAG1}+R_{DMAG2}}{2\cdot R_{DMAG1}\cdot R_{DMAG2}\cdot 400(\frac{\mu A^2}{V^2})}$$

$$R_{COMP} < \frac{R_{DMAG1}+R_{DMAG2}}{R_{DMAG1}\cdot 50\,(\frac{\mu A}{V})}\cdot\frac{1}{388.24(\frac{1}{V})\cdot F\cdot\frac{N_A}{N_S}+R_{DMAG2}\cdot 8\,(\frac{\mu A}{V})}$$

$$F = \frac{1}{4\cdot\pi\cdot V_{OUT}\cdot L_m\cdot C_O}\cdot\left(0.7ns\cdot A\cdot\frac{N_P\cdot R_{DMAG2}}{N_A}\right)^2$$

$$C_{COMP} > \frac{5\cdot\left(\frac{R_{DMAG1}+R_{DMAG2}}{R_{DMAG1}\cdot 50(\frac{\mu A}{V})}-R_{COMP}\cdot R_{DMAG2}\cdot 8(\frac{\mu A}{V})\right)}{2\cdot\pi\cdot {R_{COMP}}^2\cdot\frac{N_A}{N_S}\cdot 38.824(\frac{kHz}{V})\cdot F}$$

The C3 is used to filter the high-frequency switching noise on the COMP pin. The C3 can be determined by the following equation :

$$C3 < \frac{C_{COMP}}{60kHz\cdot\pi\cdot R_{COMP}\cdot C_{COMP}\text{-}1}$$

Thermal Considerations

For continuous operation, do not exceed absolute maximum operation junction temperature. The maximum power dissipation depends on the thermal resistance of IC package, PCB layout, the rate of surroundings airflow and temperature difference between junction to ambient. The maximum power dissipation can be calculated by following formula :

$P_{D(MAX)} = (T_{J(MAX)} - T_A) / \theta_{JA}$

Where $T_{J(MAX)}$ is the maximum operation junction temperature, T_A is the ambient temperature and the θ_{JA} is the junction to ambient thermal resistance.

For recommended operating conditions specification, the maximum junction temperature is 125°C. The junction to ambient thermal resistance θ_{JA} is layout dependent. For SOT-23-6 package, the thermal resistance θ_{JA} is 260.7°C/W on the standard JEDEC 51-3 single layer thermal test board. The maximum power dissipation at T_A = 25°C can be calculated by following formula :

$P_{D(MAX)}$ = (125°C – 25°C) / (260.7°C/W) = 0.38W for SOT-23-6 package

The maximum power dissipation depends on operating ambient temperature for fixed $T_{J(MAX)}$ and thermal resistance θ_{JA}. The Figure 17 of derating curve allows the designer to see the effect of rising ambient temperature on the maximum power dissipation allowed.

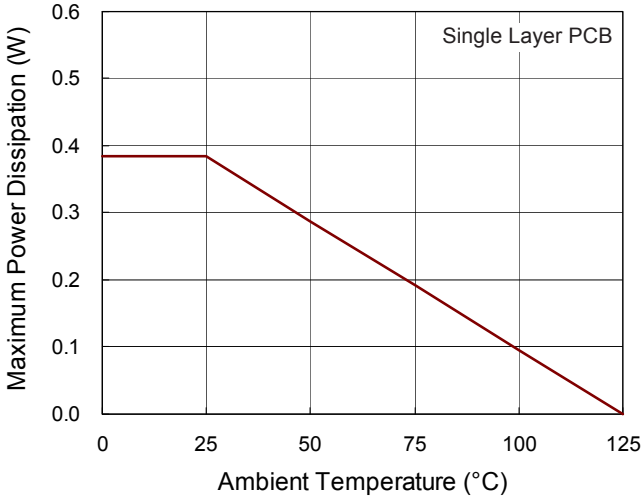


Figure 17. Derating Curve of Maximum Power Dissipation

Layout Considerations

A proper PCB layout can abate unknown noise interference and EMI issue in the switching power supply. Please refer to the guidelines when you want to design PCB layout for switching power supply :

- The current path (1) from bulk capacitor, transformer, MOSFET, RCS return to bulk capacitor is a huge high frequency current loop. It must be as short as possible to decrease noise coupling and kept a space to other low voltage traces, such as IC control circuit paths, especially. Besides, the path (2) from RCD snubber circuit to MOSFET is also a high switching loop so keep it as small as possible.
- It is good for reducing noise, output ripple and EMI issue to separate ground traces of bulk capacitor (a), MOSFET (b), auxiliary winding (c) and IC control circuit (d). Finally, connect them together on bulk capacitor ground (a). The areas of these ground traces should be kept large.
- Placing bypass capacitor for abating noise on IC is highly recommended. The bypass capacitor should be placed as close to controller as possible.
- In order to minimize reflected trace inductance and EMI, it is minimized the area of the loop connecting the secondary winding, the output diode, and the output filter capacitor must be kept small. In addition, apply sufficient copper area at the anode and cathode terminal of the diode for heatsinking. Apply a larger area at the quiet cathode terminal. A large anode area can increase high-frequency radiated EMI.
- For R7711A applications, it is better to keep the trace from voltage divider resistors close to the DMAG pin.

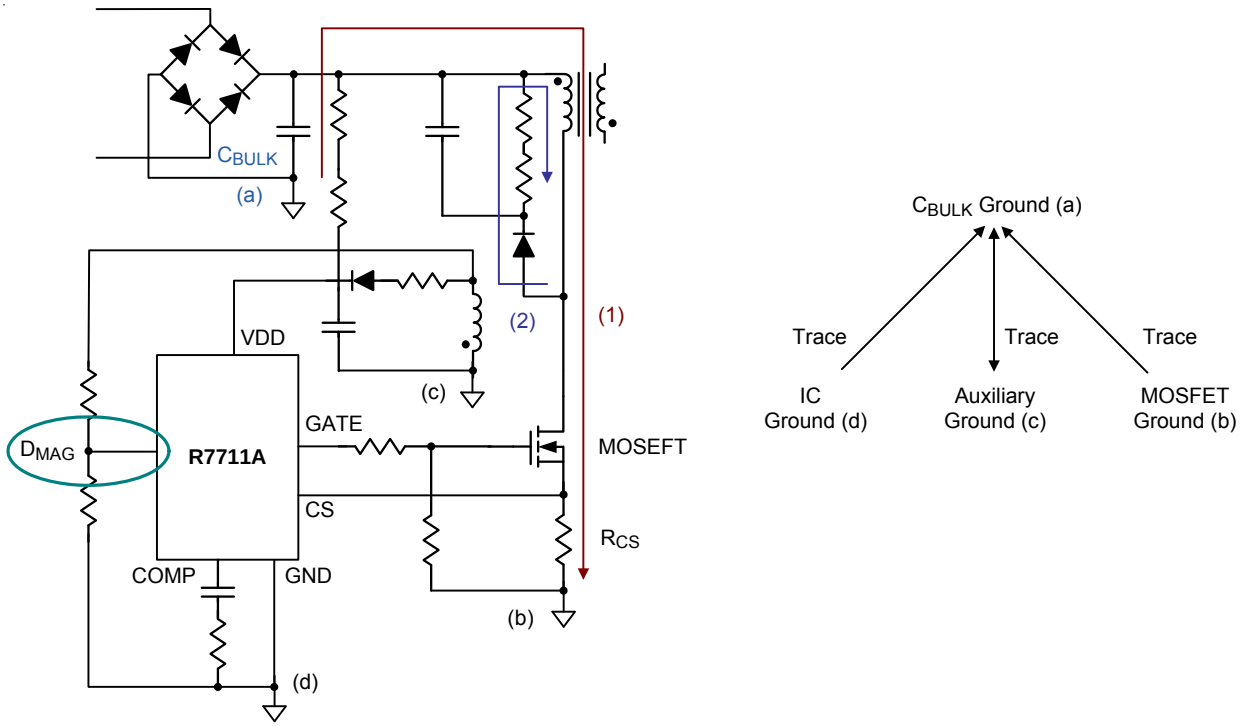
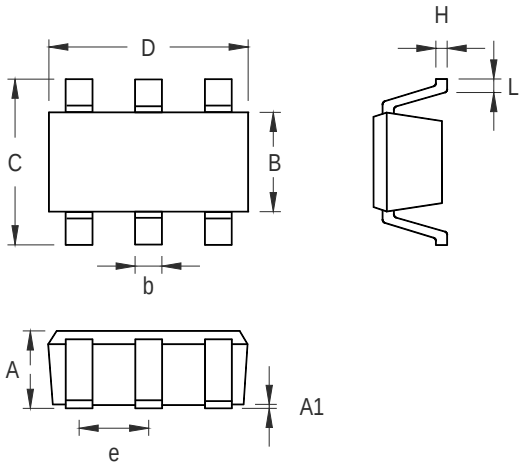


Figure 18. PCB Layout Guide

Outline Dimension



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	0.889	1.295	0.031	0.051
A1	0.000	0.152	0.000	0.006
B	1.397	1.803	0.055	0.071
b	0.250	0.560	0.010	0.022
C	2.591	2.997	0.102	0.118
D	2.692	3.099	0.106	0.122
e	0.838	1.041	0.033	0.041
H	0.080	0.254	0.003	0.010
L	0.300	0.610	0.012	0.024

SOT-23-6 Surface Mount Package

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