

HCPL-9000/-0900, -9030/-0930, HCPL-9031/-0931, -900J/-090J, HCPL-901J/-091J, -902J/-092J

High Speed Digital Isolators

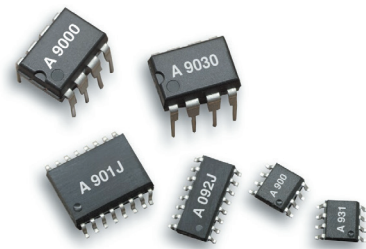


Data Sheet



Lead (Pb) Free
RoHS 6 fully
compliant

RoHS 6 fully compliant options available;
-xxxE denotes a lead-free product



Description

The HCPL-90xx and HCPL-09xx CMOS digital isolators feature high speed performance and excellent transient immunity specifications. The symmetric magnetic coupling barrier gives these devices a typical pulse width distortion of 2 ns, a typical propagation delay skew of 4 ns and 100 Mbaud data rate, making them the industry's fastest digital isolators.

The single channel digital isolators (HCPL-9000/-0900) features an active-low logic output enable. The dual channel digital isolators are configured as unidirectional (HCPL-9030/-0930) and bi-directional (HCPL-9031/-0931), operating in full duplex mode making it ideal for digital fieldbus applications.

The quad channel digital isolators are configured as unidirectional (HCPL-900J/-090J), two channels in one direction and two channels in opposite direction (HCPL-901J/-091J), and one channel in one direction and three channels in opposite direction (HCPL-902J/-092J). These high channel density make them ideally suited to isolating data conversion devices, parallel buses and peripheral interfaces.

They are available in 8-pin PDIP, 8-pin Gull Wing, 8-pin SOIC packages, and 16-pin SOIC narrow-body and wide-body packages. They are specified over the temperature range of -40°C to +100°C.

Features

- +3.3V and +5V TTL/CMOS compatible
- 3 ns max. pulse width distortion
- 6 ns max. propagation delay skew
- 15 ns max. propagation delay
- High speed: 100 MBd
- 15 kV/μs min. common mode rejection
- Tri-state output (HCPL-9000/-0900)
- 2500V RMS isolation
- UL1577 and IEC 61010-1 approved

Applications

- Digital fieldbus isolation
- Multiplexed data transmission
- Computer peripheral interface
- High speed digital systems
- Isolated data interfaces
- Logic level shifting

CAUTION: It is advised that normal static precautions be taken in handling and assembly of this component to prevent damage and/or degradation which may be induced by ESD.

Selection Guide

| Device Number | Channel Configuration | Package |
|---------------|---------------------------|-----------------------------------|
| HCPL-9000 | Single | 8-pin DIP (300 Mil) |
| HCPL-0900 | Single | 8-pin Small Outline |
| HCPL-9030 | Dual | 8-pin DIP (300 Mil) |
| HCPL-0930 | Dual | 8-pin Small Outline |
| HCPL-9031 | Dual, Bi-Directional | 8-pin DIP (300 Mil) |
| HCPL-0931 | Dual, Bi-Directional | 8-pin Small Outline |
| HCPL-900J | Quad | 16-pin Small Outline, Wide Body |
| HCPL-090J | Quad | 16-pin Small Outline, Narrow Body |
| HCPL-901J | Quad, 2/2, Bi-Directional | 16-pin Small Outline, Wide Body |
| HCPL-091J | Quad, 2/2, Bi-Directional | 16-pin Small Outline, Narrow Body |
| HCPL-902J | Quad, 1/3, Bi-Directional | 16-pin Small Outline, Wide Body |
| HCPL-092J | Quad, 1/3, Bi-Directional | 16-pin Small Outline, Narrow Body |

Ordering Information

HCPL-09xx and HCPL-90xx are UL Recognized with 2500 V_{rms} for 1 minute per UL1577.

| Part number | Option | | Package | Surface Mount | Gull Wing | Tape & Reel | Quantity |
|-------------|----------------|--------------------|----------------------|---------------|-----------|-------------|---------------|
| | RoHS Compliant | Non RoHS Compliant | | | | | |
| HCPL-9000 | -000E | No option | 300mil DIP-8 | | | | 50 per tube |
| HCPL-9030 | -300E | -300 | | X | X | | 50 per tube |
| HCPL-9031 | -500E | -500 | | X | X | X | 1000 per reel |
| HCPL-0900 | -000E | No option | SO-8 | X | | | 100 per tube |
| HCPL-0930 | -500E | -500 | | X | | X | 1500 per reel |
| HCPL-0931 | | | | | | | |
| HCPL-900J | -000E | No option | Wide Body SO-16 | X | | | 50 per tube |
| HCPL-901J | -500E | -500 | | X | | X | 1000 per reel |
| HCPL-902J | | | | | | | |
| HCPL-090J | -000E | No option | Narrow Body SO-16 | X | | | 50 per tube |
| HCPL-091J | -500E | -500 | | X | | X | 1000 per reel |
| HCPL-092J | | | | | | | |

To order, choose a part number from the part number column and combine with the desired option from the option column to form an order entry.

Example 1:

HCPL-9031-500E to order product of 300mil DIP Gull Wing Surface Mount package in Tape and Reel in RoHS compliant.

Example 2:

HCPL-0900 to order product of SO-8 package in tube packaging and non RoHS compliant.

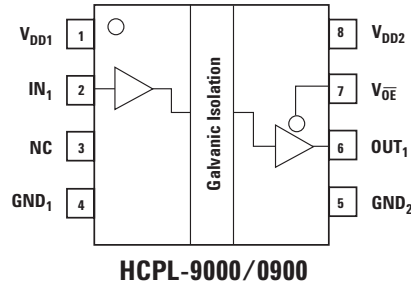
Option datasheets are available. Contact your Avago sales representative or authorized distributor for information.

Pin Description

| Symbol | Description |
|---------------------|--|
| V_{DD1} | Power Supply 1 |
| V_{DD2} | Power Supply 2 |
| IN_x | Logic Input Signal |
| OUT_x | Logic Output Signal |
| GND_1 | Power Supply Ground 1 |
| GND_2 | Power Supply Ground 2 |
| \overline{V}_{OE} | Logic Output Enable (Single Channel), Active Low |
| NC | Not Connected |

Functional Diagrams

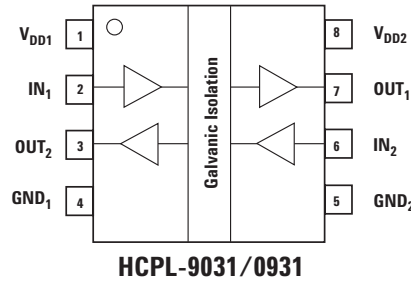
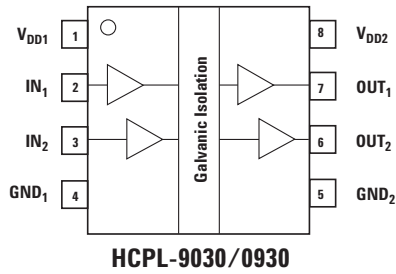
Single Channel



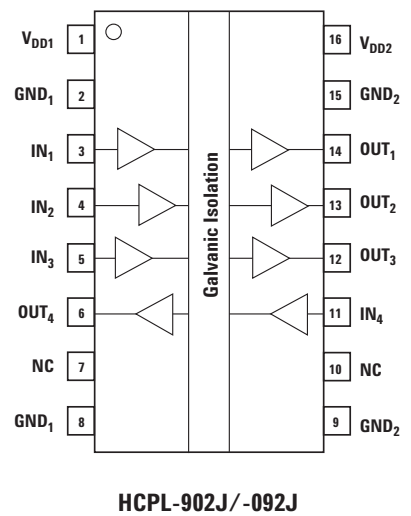
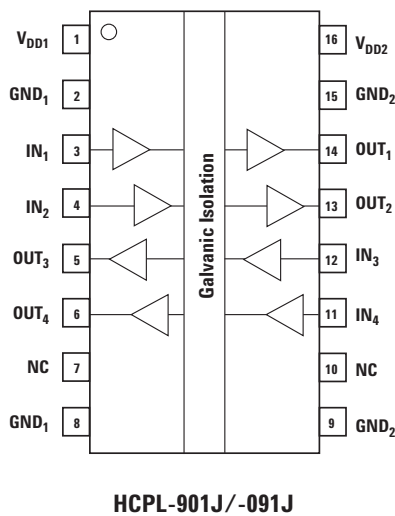
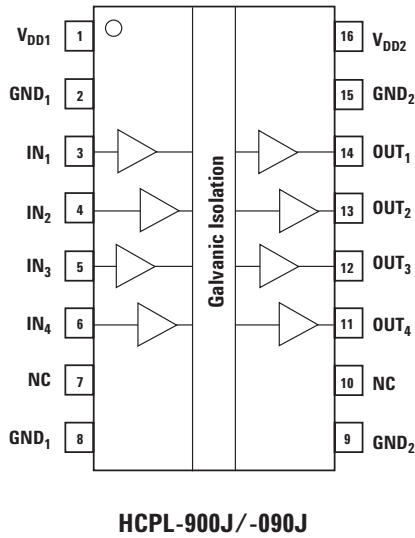
Truth Table

| IN_1 | \overline{V}_{OE} | OUT_1 |
|--------|---------------------|---------|
| L | L | L |
| H | L | H |
| L | H | Z |
| H | H | Z |

Dual Channel

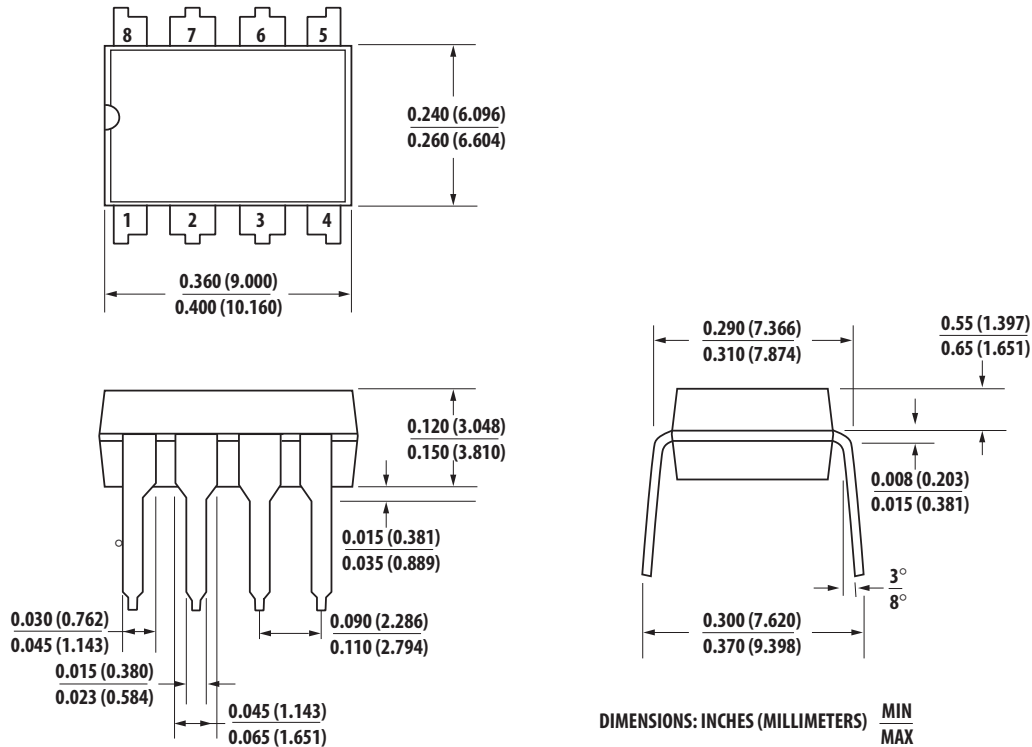


Quad Channel

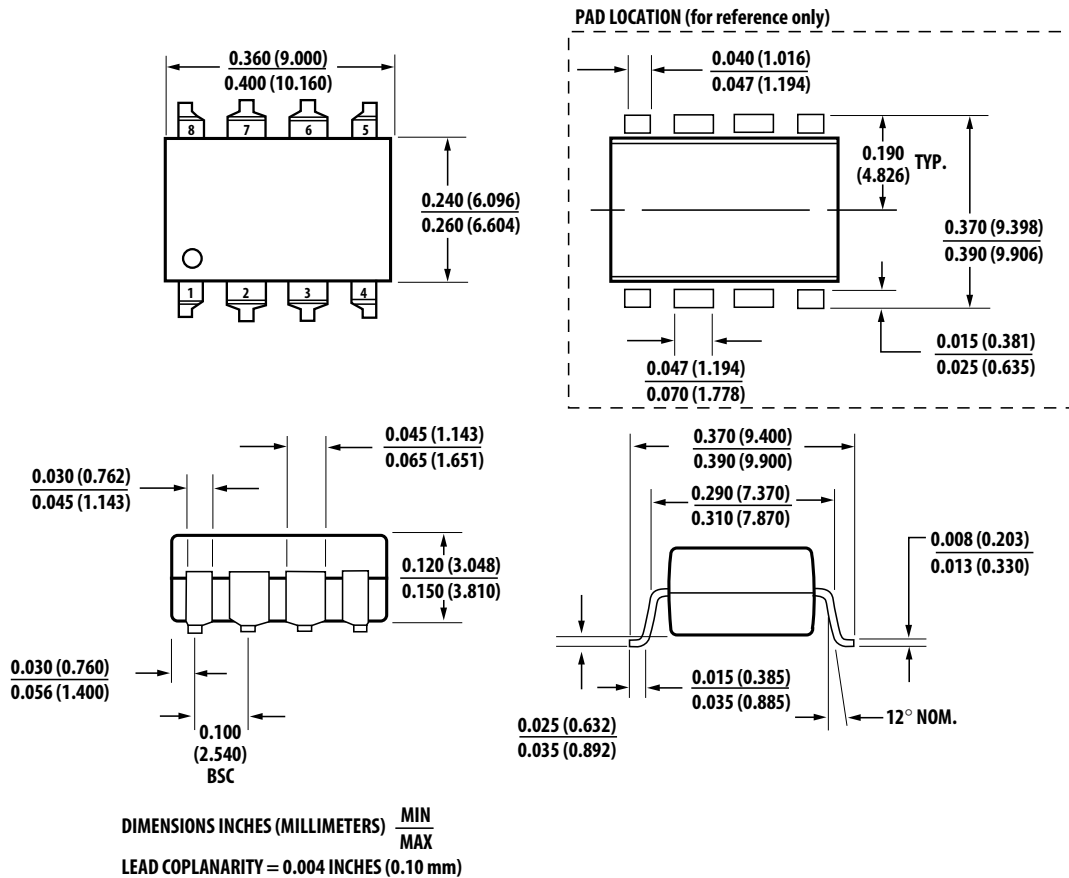


Package Outline Drawings

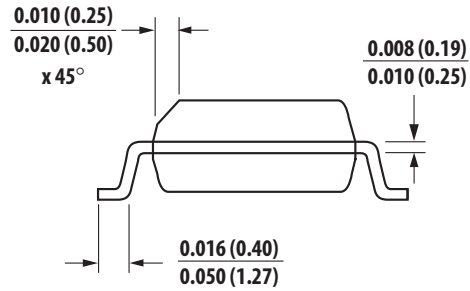
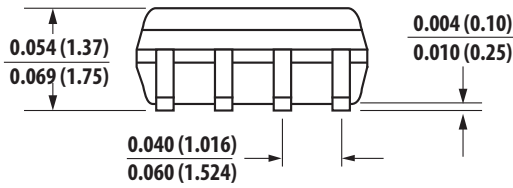
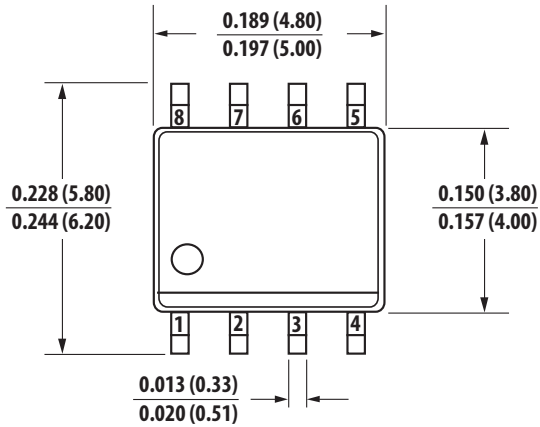
HCPL-9000, HCPL-9030 and HCPL-9031 Standard DIP Packages



HCPL-9000, HCPL-9030 and HCPL-9031 Gull Wing Surface Mount Option 300

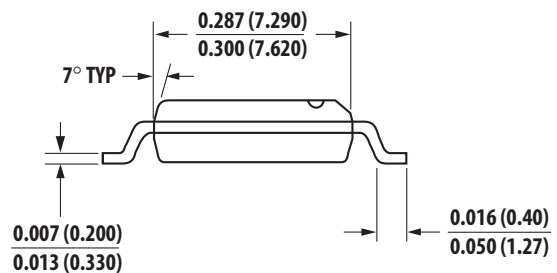
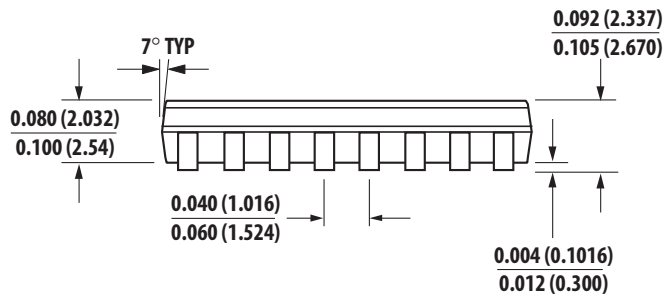
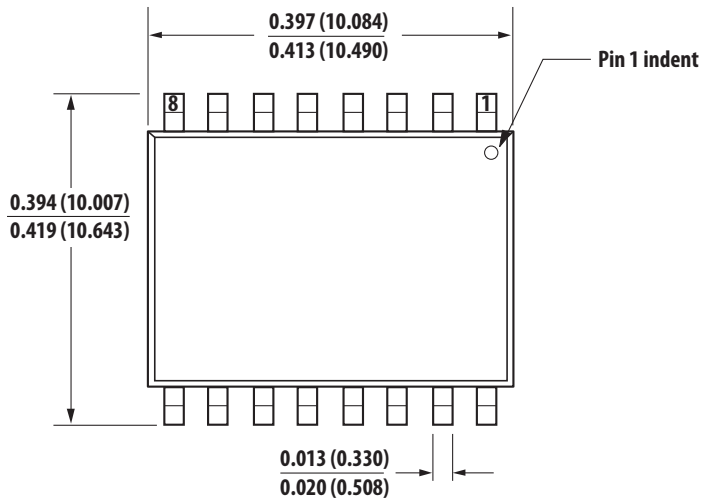


HCPL-0900, HCPL-0930 and HCPL-0931 Small Outline SO-8 Package



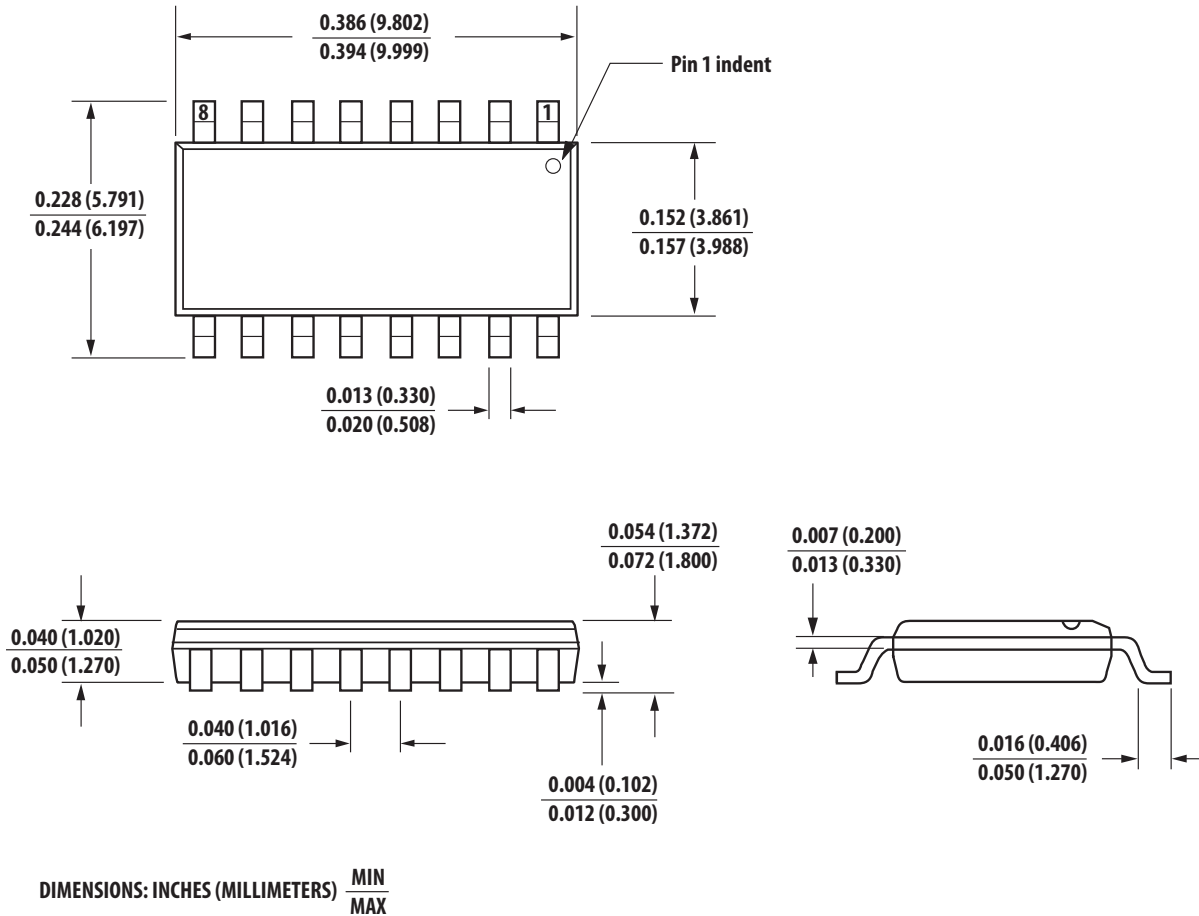
DIMENSIONS: INCHES (MILLIMETERS) MIN
MAX

HCPL-900J, HCPL-901J and HCPL-902J Wide Body SOIC-16 Package



DIMENSIONS: INCHES (MILLIMETERS) MIN
MAX

HCPL-090J, HCPL-091J and HCPL-092J Narrow Body SOIC-16 Package



Package Characteristics

| Parameter | Symbol | Min. | Typ. | Max. | Units | Test Conditions |
|---|----------------|------|------|------|-------|---|
| Capacitance (Input-Output) ^[1] | C_{I-O} | | | | pF | f = 1 MHz |
| Single Channel | | | 1.1 | | | |
| Dual Channel | | | 2.0 | | | |
| Quad Channel | | | 4.0 | | | |
| Thermal Resistance | θ_{JCT} | | | | °C/W | Thermocouple located at center underside of package |
| 8-Pin PDIP | | | 54 | | | |
| 8-Pin SOIC | | | 144 | | | |
| 16-Pin SOIC Narrow Body | | | 41 | | | |
| 16-Pin SOIC Wide Body | | | 28 | | | |
| Package Power Dissipation | P_{PD} | | | | mW | |
| 8-Pin PDIP | | | | 150 | | |
| 8-Pin SOIC | | | | 150 | | |
| 16-Pin SOIC Narrow Body | | | | 150 | | |
| 16-Pin SOIC Wide Body | | | | 150 | | |

Notes:

1. Single and dual channels device are considered two-terminal devices: pins 1-4 shorted and pins 5-8 shorted. Quad channel devices are considered two-terminal devices: pins 1-8 shorted and pins 9-16 shorted.

This product has been tested for electrostatic sensitivity to the limits stated in the specifications. However, Avago recommends that all integrated circuits be handled with appropriate care to avoid damage. Damage caused by inappropriate handling or storage could range from performance degradation to complete failure.

Insulation and Safety Related Specifications

| Parameters | Condition | Min. | Typ. | Max. | Units |
|------------------------------|-------------------------------|------|------------------------|------|--------------------------------|
| Barrier Impedance | | | | | $\Omega \parallel \mu\text{F}$ |
| Single Channel | | | $>10^{14} \parallel 3$ | | |
| Dual Channel | | | $>10^{14} \parallel 3$ | | |
| Quad Channel | | | $>10^{14} \parallel 7$ | | |
| Creepage Distance (External) | | | | | mm |
| 8-Pin PDIP | | 7.04 | | | |
| 8-Pin SOIC | | 4.04 | | | |
| 16-Pin SOIC Narrow Body | | 4.03 | | | |
| 16-Pin SOIC Wide Body | | 8.08 | | | |
| Leakage Current | 240 V _{RMS} 60 Hz | | 0.2 | | μA |

IEC61010-1 Insulation Characteristics*

| Description | Symbol | HCPL-0900 | HCPL-9000 | Units |
|--|--------|-----------|-----------|------------------|
| | | HCPL-0930 | HCPL-9030 | |
| | | HCPL-090J | HCPL-900J | |
| | | HCPL-091J | HCPL-901J | |
| | | HCPL-092J | HCPL-902J | |
| Installation classification per DIN VDE 0110/1.89, Table 1 | | | | |
| for rated mains voltage $\leq 150 \text{ V}_{\text{rms}}$ | | I – III | I – IV | |
| for rated mains voltage $\leq 300 \text{ V}_{\text{rms}}$ | | | I – III | |
| Pollution Degree (DIN VDE 0110/1.89) | | 2 | 2 | |
| Maximum Working Insulation Voltage | VIORM | 150 | 300 | V _{rms} |

Soldering Profile

The recommended reflow soldering conditions are per JEDEC Standard J-STD-020 (latest revision).

Absolute Maximum Ratings

| Parameters | Symbol | Min. | Max. | Units |
|--|-----------------------|------|-----------------|-------|
| Storage Temperature | T_S | -55 | 150 | °C |
| Ambient Operating Temperature ⁽¹⁾ | T_A | -55 | 125 | °C |
| Supply Voltage | V_{DD1}, V_{DD2} | -0.5 | 7 | V |
| Input Voltage | V_{IN} | -0.5 | $V_{DD1} + 0.5$ | V |
| Voltage Output Enable (HCPL-9000/-0900) | V_{OE} | -0.5 | $V_{DD2} + 0.5$ | V |
| Output Voltage | V_{OUT} | -0.5 | $V_{DD2} + 0.5$ | V |
| Output Current Drive | I_{OUT} | | 10 | mA |
| Lead Solder Temperature (10s) | | | 260 | °C |
| ESD | 2 kV Human Body Model | | | |

Notes:

1. Absolute Maximum ambient operating temperature means the device will not be damaged if operated under these conditions. It does not guarantee performance.

Recommended Operating Conditions

| Parameters | Symbol | Min. | Max. | Units |
|----------------------------------|--------------------|------|-----------|-------|
| Ambient Operating Temperature | T_A | -40 | 100 | °C |
| Supply Voltage | V_{DD1}, V_{DD2} | 3.0 | 5.5 | V |
| Logic High Input Voltage | V_{IH} | 2.4 | V_{DD1} | V |
| Logic Low Input Voltage | V_{IL} | 0 | 0.8 | V |
| Input Signal Rise and Fall Times | t_{IR}, t_{IF} | | 1 | μs |

This product has been tested for electrostatic sensitivity to the limits stated in the specifications. However, Avago recommends that all integrated circuits be handled with appropriate care to avoid damage. Damage caused by inappropriate handling or storage could range from performance degradation to complete failure.

3.3V operation: Electrical Specifications

Test conditions that are not specified can be anywhere within the recommended operating range.

All typical specifications are at $T_A = +25^\circ\text{C}$, $V_{DD1} = V_{DD2} = +3.3\text{V}$.

| Parameter | Symbol | Min. | Typ. | Max. | Units | Test Conditions |
|----------------------------|-----------|-----------------|-----------------|------|---------------|--|
| Quiescent Supply Current 1 | I_{DD1} | | | | mA | $V_{IN} = 0\text{V}$ |
| HCPL-9000/-0900 | | | 0.008 | 0.01 | | |
| HCPL-9030/-0930 | | | 0.008 | 0.01 | | |
| HCPL-9031/-0931 | | | 1.5 | 2.0 | | |
| HCPL-900J/-090J | | | 0.018 | 0.02 | | |
| HCPL-901J/-091J | | | 3.3 | 4.0 | | |
| HCPL-902J/-092J | | | 1.5 | 2.0 | | |
| Quiescent Supply Current 2 | I_{DD2} | | | | mA | $V_{IN} = 0\text{V}$ |
| HCPL-9000/-0900 | | | 3.3 | 4.0 | | |
| HCPL-9030/-0930 | | | 3.3 | 4.0 | | |
| HCPL-9031/-0931 | | | 1.5 | 2.0 | | |
| HCPL-900J/-090J | | | 5.5 | 8.0 | | |
| HCPL-901J/-091J | | | 3.3 | 4.0 | | |
| HCPL-902J/-092J | | | 3.0 | 6.0 | | |
| Logic Input Current | I_{IN} | -10 | | 10 | μA | |
| Logic High Output Voltage | V_{OH} | $V_{DD2} - 0.1$ | V_{DD2} | | V | $I_{OUT} = -20\ \mu\text{A}$, $V_{IN} = V_{IH}$ |
| | | $0.8 * V_{DD2}$ | $V_{DD2} - 0.5$ | | V | $I_{OUT} = -4\ \text{mA}$, $V_{IN} = V_{IH}$ |
| Logic Low Output Voltage | V_{OL} | | 0 | 0.1 | V | $I_{OUT} = 20\ \mu\text{A}$, $V_{IN} = V_{IL}$ |
| | | | 0.5 | 0.8 | V | $I_{OUT} = 4\ \text{mA}$, $V_{IN} = V_{IL}$ |

Switching Specifications

| | | | | | | |
|--|-----------------------|-----|-----|----|-------------------|-------------------------|
| Maximum Data Rate | | 100 | 110 | | MBd | $C_L = 15\ \text{pF}$ |
| Clock Frequency | f_{max} | | | 50 | MHz | |
| Propagation Delay Time to Logic Low Output | t_{PHL} | | 12 | 18 | ns | |
| Propagation Delay Time to Logic High Output | t_{PLH} | | 12 | 18 | ns | |
| Pulse Width | t_{PW} | 10 | | | ns | |
| Pulse Width Distortion ^[1] | $ \text{PWD} $ | | 2 | 3 | ns | |
| | $ t_{PHL} - t_{PLH} $ | | | | | |
| Propagation Delay Skew ^[2] | t_{PSK} | | 4 | 6 | ns | |
| Output Rise Time (10 – 90%) | t_R | | 2 | 4 | ns | |
| Output Fall Time (10 – 90%) | t_F | | 2 | 4 | ns | |
| Propagation Delay Enable to Output (Single Channel) | | | | | | |
| High to High Impedance | t_{PHZ} | | 3 | 5 | ns | |
| Low to High Impedance | t_{PLZ} | | 3 | 5 | ns | |
| High Impedance to High | t_{PZH} | | 3 | 5 | ns | |
| High Impedance to Low | t_{PZL} | | 3 | 5 | ns | |
| Channel-to-Channel Skew (Dual and Quad Channels) | t_{CSK} | | 2 | 3 | ns | |
| Common Mode Transient Immunity (Output Logic High or Logic Low) ^[3] | $ CM_H $ $ CM_L $ | 15 | 18 | | kV/ μs | $V_{cm} = 1000\text{V}$ |

Notes:

1. PWD is defined as $|t_{PHL} - t_{PLH}|$. %PWD is equal to the PWD divided by the pulse width.
2. t_{PSK} is equal to the magnitude of the worst case difference in t_{PHL} and/or t_{PLH} that will be seen between units at 25°C .
3. CM_H is the maximum common mode voltage slew rate that can be sustained while maintaining $V_{OUT} > 0.8V_{DD2}$. CM_L is the maximum common mode input voltage that can be sustained while maintaining $V_{OUT} < 0.8V$. The common mode voltage slew rates apply to both rising and falling common mode voltage edges.

This product has been tested for electrostatic sensitivity to the limits stated in the specifications. However, Avago recommends that all integrated circuits be handled with appropriate care to avoid damage. Damage caused by inappropriate handling or storage could range from performance degradation to complete failure.

5V operation: Electrical Specifications

Test conditions that are not specified can be anywhere within the recommended operating range.

All typical specifications are at $T_A = +25^\circ\text{C}$, $V_{DD1} = V_{DD2} = +5.0\text{V}$.

| Parameter | Symbol | Min. | Typ. | Max. | Units | Test Conditions |
|----------------------------|-----------|-----------------|-----------------|-------|---------------|--|
| Quiescent Supply Current 1 | I_{DD1} | | | | mA | $V_{IN} = 0\text{V}$ |
| HCPL-9000/-0900 | | | 0.012 | 0.018 | | |
| HCPL-9030/-0930 | | | 0.012 | 0.018 | | |
| HCPL-9031/-0931 | | | 2.5 | 3.0 | | |
| HCPL-900J/-090J | | | 0.024 | 0.036 | | |
| HCPL-901J/-091J | | | 5.0 | 6.0 | | |
| HCPL-902J/-092J | | | 2.5 | 3.0 | | |
| Quiescent Supply Current 2 | I_{DD2} | | | | mA | $V_{IN} = 0\text{V}$ |
| HCPL-9000/-0900 | | | 5.0 | 6.0 | | |
| HCPL-9030/-0930 | | | 5.0 | 6.0 | | |
| HCPL-9031/-0931 | | | 2.5 | 3.0 | | |
| HCPL-900J/-090J | | | 8.0 | 12.0 | | |
| HCPL-901J/-091J | | | 5.0 | 6.0 | | |
| HCPL-902J/-092J | | | 6.0 | 9.0 | | |
| Logic Input Current | I_{IN} | -10 | | 10 | μA | |
| Logic High Output Voltage | V_{OH} | $V_{DD2} - 0.1$ | V_{DD2} | | V | $I_{OUT} = -20\ \mu\text{A}$, $V_{IN} = V_{IH}$ |
| | | $0.8 * V_{DD2}$ | $V_{DD2} - 0.5$ | | V | $I_{OUT} = -4\ \text{mA}$, $V_{IN} = V_{IH}$ |
| Logic Low Output Voltage | V_{OL} | | 0 | 0.1 | V | $I_{OUT} = 20\ \mu\text{A}$, $V_{IN} = V_{IL}$ |
| | | | 0.5 | 0.8 | V | $I_{OUT} = 4\ \text{mA}$, $V_{IN} = V_{IL}$ |

Switching Specifications

| | | | | | | |
|--|-----------------------|-----|-----|----|-------------------|-------------------------|
| Maximum Data Rate | | 100 | 110 | | MBd | $C_L = 15\ \text{pF}$ |
| Clock Frequency | f_{max} | | | 50 | MHz | |
| Propagation Delay Time to Logic Low Output | t_{PHL} | | 10 | 15 | ns | |
| Propagation Delay Time to Logic High Output | t_{PLH} | | 10 | 15 | ns | |
| Pulse Width | t_{PW} | 10 | | | ns | |
| Pulse Width Distortion ^[1] | $ PWD $ | | 2 | 3 | ns | |
| | $ t_{PHL} - t_{PLH} $ | | | | | |
| Propagation Delay Skew ^[2] | t_{PSK} | | 4 | 6 | ns | |
| Output Rise Time (10 – 90%) | t_R | | 1 | 3 | ns | |
| Output Fall Time (10 – 90%) | t_F | | 1 | 3 | ns | |
| Propagation Delay Enable to Output (Single Channel) | | | | | | |
| High to High Impedance | t_{PHZ} | | 3 | 5 | ns | |
| Low to High Impedance | t_{PLZ} | | 3 | 5 | ns | |
| High Impedance to High | t_{PZH} | | 3 | 5 | ns | |
| High Impedance to Low | t_{PZL} | | 3 | 5 | ns | |
| Channel-to-Channel Skew (Dual and Quad Channels) | t_{CSK} | | 2 | 3 | ns | |
| Common Mode Transient Immunity (Output Logic High or Logic Low) ^[3] | $ CM_H $ $ CM_L $ | 15 | 18 | | kV/ μs | $V_{cm} = 1000\text{V}$ |

Notes:

- PWD is defined as $|t_{PHL} - t_{PLH}|$. %PWD is equal to the PWD divided by the pulse width.
- t_{PSK} is equal to the magnitude of the worst case difference in t_{PHL} and/or t_{PLH} that will be seen between units at 25°C .
- CM_H is the maximum common mode voltage slew rate that can be sustained while maintaining $V_{OUT} > 0.8V_{DD2}$. CM_L is the maximum common mode input voltage that can be sustained while maintaining $V_{OUT} < 0.8V$. The common mode voltage slew rates apply to both rising and falling common mode voltage edges.

This product has been tested for electrostatic sensitivity to the limits stated in the specifications. However, Avago recommends that all integrated circuits be handled with appropriate care to avoid damage. Damage caused by inappropriate handling or storage could range from performance degradation to complete failure.

Mixed 5V/3.3V or 3.3V/5V operation: Electrical Specifications

Test conditions that are not specified can be anywhere within the recommended operating range.

All typical specifications are at $T_A = +25^\circ\text{C}$, $V_{DD1} = +5.0\text{V}$, $V_{DD2} = +3.3\text{V}$.

| Parameter | Symbol | Min. | Typ. | Max. | Units | Test Conditions |
|----------------------------|-----------|-----------------|-----------------|-------|---------------|--|
| HCPL-9000/-0900 | I_{DD1} | | 0.012 | 0.018 | | |
| HCPL-9030/-0930 | | | 0.012 | 0.018 | | |
| HCPL-9031/-0931 | | | 2.5 | 3.0 | | |
| HCPL-900J/-090J | | | 0.024 | 0.036 | | |
| HCPL-901J/-091J | | | 5.0 | 6.0 | | |
| HCPL-902J/-092J | | | 2.5 | 3.0 | | |
| Quiescent Supply Current 2 | I_{DD2} | | | | mA | $V_{IN} = 0\text{V}$ |
| HCPL-9000/-0900 | | | 5.0 | 6.0 | | |
| HCPL-9030/-0930 | | | 5.0 | 6.0 | | |
| HCPL-9031/-0931 | | | 2.5 | 3.0 | | |
| HCPL-900J/-090J | | | 8.0 | 12.0 | | |
| HCPL-901J/-091J | | | 5.0 | 6.0 | | |
| HCPL-902J/-092J | | | 6.0 | 9.0 | | |
| Logic Input Current | I_{IN} | -10 | | 10 | μA | |
| Logic High Output Voltage | V_{OH} | $V_{DD2} - 0.1$ | V_{DD2} | | V | $I_{OUT} = -20\ \mu\text{A}$, $V_{IN} = V_{IH}$ |
| | | $0.8 * V_{DD2}$ | $V_{DD2} - 0.5$ | | V | $I_{OUT} = -4\ \text{mA}$, $V_{IN} = V_{IH}$ |
| Logic Low Output Voltage | V_{OL} | 0 | | 0.1 | V | $I_{OUT} = 20\ \mu\text{A}$, $V_{IN} = V_{IL}$ |
| | | | 0.5 | 0.8 | V | $I_{OUT} = 4\ \text{mA}$, $V_{IN} = V_{IL}$ |

Switching Specifications

| | | | | | | |
|--|-----------------------|-----|-----|----|-------------------|-------------------------|
| Maximum Data Rate | | 100 | 110 | | MBd | $C_L = 15\ \text{pF}$ |
| Clock Frequency | f_{max} | | | 50 | MHz | |
| Propagation Delay Time to Logic Low Output | t_{PHL} | | 12 | 18 | ns | |
| Propagation Delay Time to Logic High Output | t_{PLH} | | 12 | 18 | ns | |
| Pulse Width | t_{PW} | 10 | | | ns | |
| Pulse Width Distortion ^[1] | $ PWD $ | | 2 | 3 | ns | |
| | $ t_{PHL} - t_{PLH} $ | | | | | |
| Propagation Delay Skew ^[2] | t_{PSK} | | 4 | 6 | ns | |
| Output Rise Time (10 – 90%) | t_R | | 2 | 4 | ns | |
| Output Fall Time (10 – 90%) | t_F | | 2 | 4 | ns | |
| Propagation Delay Enable to Output (Single Channel) | | | | | | |
| High to High Impedance | t_{PHZ} | | 3 | 5 | ns | |
| Low to High Impedance | t_{PLZ} | | 3 | 5 | ns | |
| High Impedance to High | t_{PZH} | | 3 | 5 | ns | |
| High Impedance to Low | t_{PZL} | | 3 | 5 | ns | |
| Channel-to-Channel Skew (Dual and Quad Channels) | t_{CSK} | | 2 | 3 | ns | |
| Common Mode Transient Immunity (Output Logic High or Logic Low) ^[3] | $ CM_H $ $ CM_L $ | 15 | 18 | | kV/ μs | $V_{cm} = 1000\text{V}$ |

Notes:

- PWD is defined as $|t_{PHL} - t_{PLH}|$. %PWD is equal to the PWD divided by the pulse width.
- t_{PSK} is equal to the magnitude of the worst case difference in t_{PHL} and/or t_{PLH} that will be seen between units at 25°C .
- CM_H is the maximum common mode voltage slew rate that can be sustained while maintaining $V_{OUT} > 0.8V_{DD2}$. CM_L is the maximum common mode input voltage that can be sustained while maintaining $V_{OUT} < 0.8\text{V}$. The common mode voltage slew rates apply to both rising and falling common mode voltage edges.

This product has been tested for electrostatic sensitivity to the limits stated in the specifications. However, Avago recommends that all integrated circuits be handled with appropriate care to avoid damage. Damage caused by inappropriate handling or storage could range from performance degradation to complete failure.

Applications Information

Power Consumption

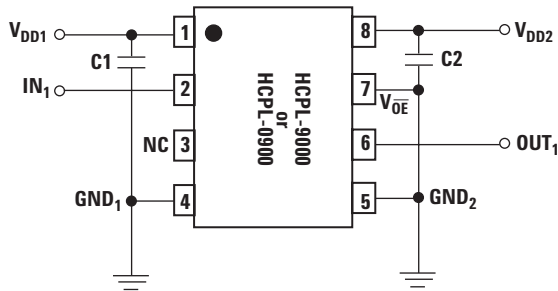
The HCPL-90xx and HCPL-09xx CMOS digital isolators achieve low power consumption from the manner by which they transmit data across isolation barrier. By detecting the edge transitions of the input logic signal and converting this to a narrow current pulse, which drives the isolation barrier, the isolator then latches the input logic state in the output latch. Since the current pulses are narrow, about 2.5 ns wide, the power consumption is independent of mark-to-space ratio and solely dependent on frequency.

The approximate power supply current per channel is:
 $I(\text{Input}) = 40(f/f_{\text{max}})(1/4) \text{ mA}$

where f = operating frequency, $f_{\text{max}} = 50 \text{ MHz}$.

Signal Status on Start-up and Shut Down

To minimize power dissipation, the input signals to the channels of HCPL-90xx and HCPL-09xx digital isolators are differentiated and then latched on the output side of the isolation barrier to reconstruct the signal. This could result in an ambiguous output state depending on power up, shutdown and power loss sequencing. Therefore, the designer should consider the inclusion of an initialization signal in this start-up circuit. Initialization consists of toggling the input either high then low or low then high.



Note: C1, C2 = 47 nF ceramic capacitors

Figure 1. Functional Diagram of Single Channel HCPL-0900 or HCPL-9000.

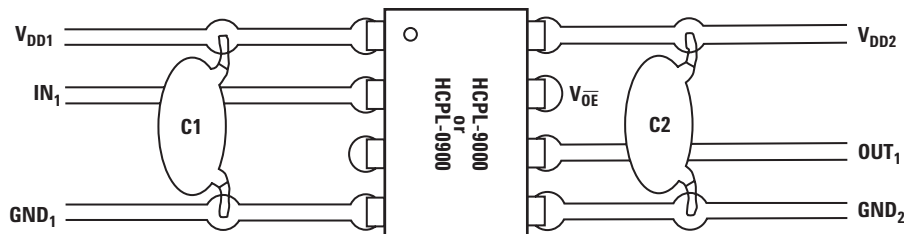


Figure 2. Recommended Printed Circuit Board Layout.

Bypassing and PC Board Layout

The HCPL-90xx and HCPL-09xx digital isolators are extremely easy to use. No external interface circuitry is required because the isolators use high-speed CMOS IC technology allowing CMOS logic to be connected directly to the inputs and outputs. As shown in Figure 1, the only external components required for proper operation are two 47 nF ceramic capacitors for decoupling the power supplies. For each capacitor, the total lead length between both ends of the capacitor and the power-supply pins should not exceed 20 mm. Figure 2 illustrates the recommended printed circuit board layout for the HCPL-9000 or HCPL-0900. For data rates in excess of 10MBd, use of ground planes for both GND_1 and GND_2 is highly recommended.

Propagation Delay, Pulse Width Distortion and Propagation Delay Skew

Propagation Delay is a figure of merit, which describes how quickly a logic signal propagates through a system as illustrated in Figure 3.

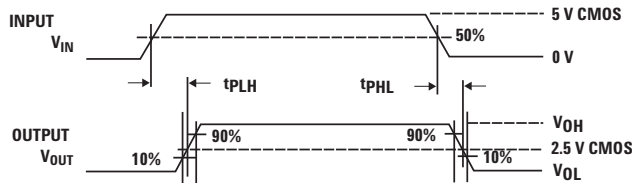


Figure 3. Timing Diagrams to Illustrate Propagation Delay, t_{PLH} and t_{PHL} .

The propagation delay from low to high, t_{PLH} , is the amount of time required for an input signal to propagate to the output, causing the output to change from low to high. Similarly, the propagation delay from high to low, t_{PHL} , is the amount of time required for the input signal to propagate to the output, causing the output to change from high to low.

Pulse Width Distortion, PWD, is the difference between t_{PHL} and t_{PLH} and often determines the maximum data rate capability of a transmission system. PWD can be expressed in percent by dividing the PWD (in ns) by the minimum pulse width (in ns) being transmitted. Typically, PWD on the order of 20–30% of the minimum pulse width is tolerable.

Propagation Delay Skew, t_{PSK} , and Channel-to-Channel Skew, t_{CSK} , are critical parameters to consider in parallel data transmission applications where synchronization of signals on parallel data lines is a concern. If the parallel data is being sent through channels of the digital isolators, differences in propagation delays will cause the data to arrive at the outputs of the digital isolators at different times. If this difference in propagation delay is large enough, it will limit the maximum transmission rate at which parallel data can be sent through the digital isolators.

t_{PSK} is defined as the difference between the minimum and maximum propagation delays, either t_{PLH} or t_{PHL} , among two or more devices which are operating under the same conditions (i.e., the same drive current, supply voltage, output load, and operating temperature). t_{CSK} is defined as the difference between the minimum and maximum propagation delays, either t_{PLH} or t_{PHL} , among two or more channels within a single device (applicable to dual and quad channel devices) which are operating under the same conditions.

As illustrated in Figure 4, if the inputs of two or more devices are switched either ON or OFF at the same time, t_{PSK} is the difference between the minimum propagation delay, either t_{PLH} or t_{PHL} , and the maximum propagation delay, either t_{PLH} or t_{PHL} .

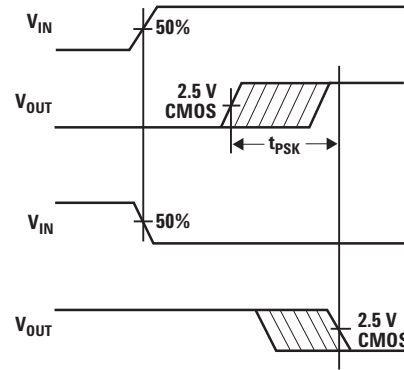


Figure 4. Timing Diagrams to Illustrate Propagation Delay Skew.

As mentioned earlier, t_{PSK} can determine the maximum parallel data transmission rate. Figure 5 shows the timing diagram of a typical parallel data transmission application with both the clock and data lines being sent through the digital isolators. The figure shows data and clock signals at the inputs and outputs of the digital isolators. In this case, the data is clocked off the rising edge of the clock.

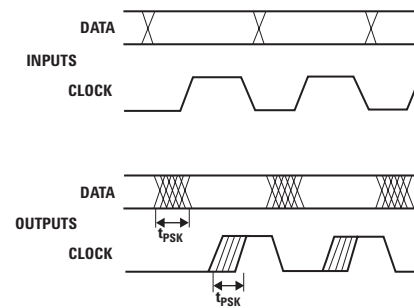


Figure 5. Parallel Data Transmission.

Propagation delay skew represents the uncertainty of where an edge might be after being sent through a digital isolator. Figure 5 shows that there will be uncertainty in both the data and clock lines. It is important that these two areas of uncertainty not overlap, otherwise the clock signal might arrive before all of the data outputs have settled, or some of the data outputs may start to change before the clock signal has arrived. From these considerations, the absolute minimum pulse width that can be sent through digital isolators in a parallel application is twice t_{PSK} . A cautious design should use a slightly longer pulse width to ensure that any additional uncertainty in the rest of the circuit does not cause a problem.

Figure 6 shows the minimum pulse width, rise and fall time, and propagation delay enable to output waveforms for HCPL-9000 or HCPL-0900.

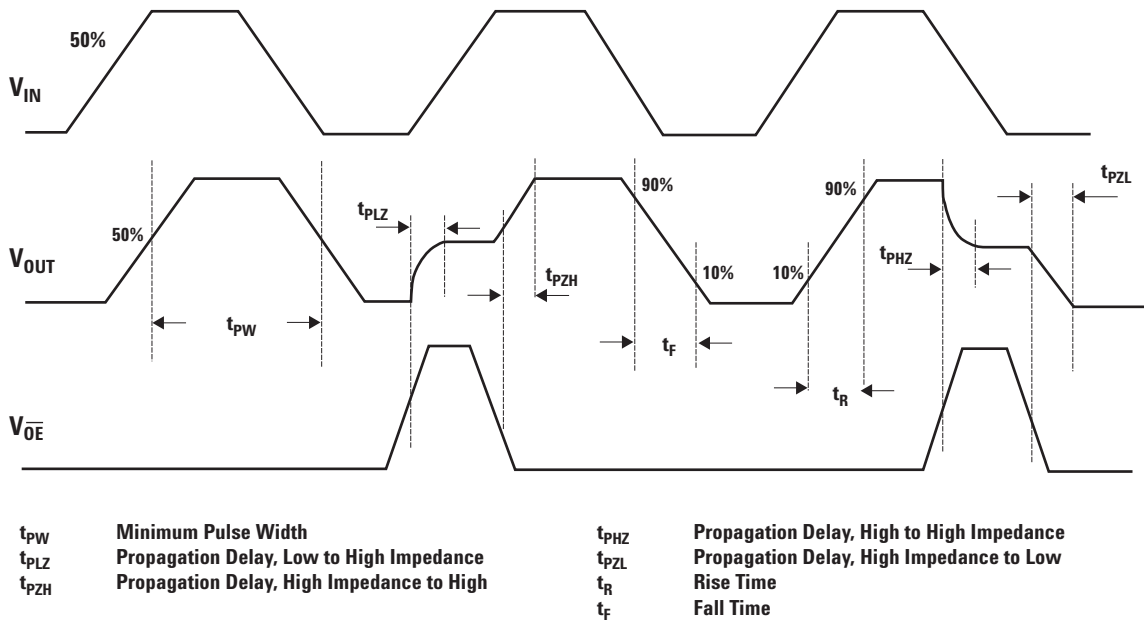


Figure 6. Timing Diagrams to Illustrate the Minimum Pulse Width, Rise and Fall Time, and Propagation Delay Enable to Output Waveforms for HCPL-9000 or HCPL-0900.

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