



AR4100(P) System in Package 802.11n: General Availability

Data Sheet

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**Qualcomm Atheros, Inc.
1700 Technology Drive
San Jose, CA 95112
U.S.A.**

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1 Introduction

1.1 General Description

NOTE This data sheet covers both the AR4100 and the AR4100P products. The devices are functionally equivalent in many ways; where the information is common, the devices are called out as AR4100(P) to cover both products. Otherwise, the product is specifically called out as AR4100 or AR4100P to refer to a particular product.

The AR4100(P) is a small form-factor, single stream, 802.11 b/g/n WiFi System-in-Package (SiP) solution. The AR4100(P) has been developed to support applications hosted by low-resource microcontrollers that send infrequent data packets over the network. Typically, these 802.11 applications will place a higher priority on system cost, power consumption, ease of use, and fast wake-up times as compared to high throughput. The AR4100(P) integrates all WiFi functionality into a low-profile, 8.3 mm x 9.2 mm LGA package that can be easily mounted via low-cost PCB manufacturing flows. The device requires only a few external bypass capacitors and a connection to an antenna for a board level design. As an added cost reduction and convenience, the SiP module is pre-certified with the FCC and other major regulatory bodies.

The AR4100(P) employs the world's lowest power consumption embedded architecture. It has been optimized for client applications in the home and enterprise that have lower data rates, and transmit or receive data on an infrequent basis. The AR4100(P) features standby current consumption as low as 5 μ A. Additional optimizations, including a reduced host driver footprint, allow easy integration with low-cost microcontrollers.

The AR4100(P) also includes Qualcomm Atheros' industry leading high-efficiency, high-output EPA™ power amplifier with zero calibration and integrated LNAs. RF matching circuits, a reference crystal, and a T/R switch are also integrated, eliminating the need for an external RF components and thus enabling direct antenna connection. The end result is a device that is the best-in-class for ease of system design.

At the heart of the AR4100(P) is an ultra low-power radio architecture and proprietary power save technologies. An on-chip embedded CPU handles complete 802.11 b/g/n processing to minimize host processor loading.

The AR4100(P) includes all of the benefits of the AR4100 and also features a fully offloaded IPv4/IPv6 stack. The offloading of the TCP/IP stack significantly reducing processing and memory requirements on the host microcontroller.

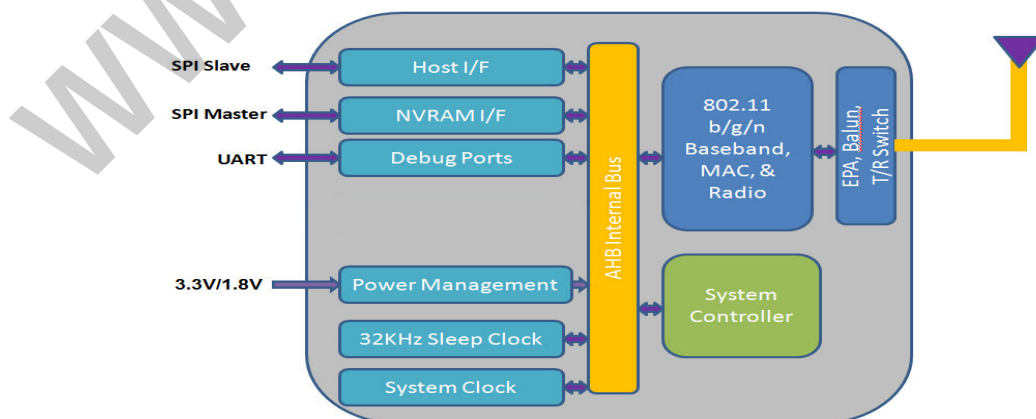
The AR4100(P) also supports a modular certification capability with the FCC and other regulatory agencies. The modular approval requires following the Qualcomm Atheros guidelines in a copy-exactly methodology and reviewing the design to ensure it meets the design guidelines. The review process is managed by a third party firm. More details can be found in the *FCC Modular SiP Approval for AR4100(P)* application note.

1.2 AR4100(P) Features

AR4100(P), ultra-low power, single stream (1x1) IEEE 802.11n featuring:

- Low energy
 - Low power modes consuming as little as 5 μ A of current
 - System reference with standby current as low as 1 μ A
 - Fast wake up when loading firmware from inexpensive external NVMEM (SPI flash device)
- Low system resource requirements:
 - Small, simple host driver
 - Enable low resource MCU hosts
- Simple low cost wireless system integration:
 - Simple to assemble QFN-like package
 - Simple design supporting 2- or 4- layer PCB support
 - Near zero RBOM
 - Integrated: RF front end, RF shield, 32 KHz sleep clock, and system clock
 - Direct connect to a 50- Ω antenna
- Qualcomm Atheros world class leading 802.11n WiFi:
 - Best in class Rx sensitivity for superior throughput rate-over-range performance
 - Integrated high-power, high efficiency linearized Power Amplifier
 - Low Density Parity Check (LDPC) encoding for improved uplink robustness over range
 - WiFi Protected Setup (WPS) 2.0
- Standard interfaces:
 - SPI slave, SPI Master, and UART
- AR4100(P) Features
 - On-SIP integrated IPv4/IPv6 stack reduces CPU and Flash requirements on host microcontroller
 - BSD-like interface provides a common easy interface across different operating systems, simplifying porting of the IP Stack offload
 - TCP or UDP operation

1.3 System Block Diagram



2 Features Summary

2.1 Overview

The AR4100(P) is an IEEE 802.11 (b, g, n) System in Package (SiP) based on cutting edge technology. The AR4100(P) includes full digital MAC and baseband engines handling all 802.11b (CCK) and 802.11g/n (OFDM). An embedded low-power CPU core minimizes host loading to provide an easy to implement solution. The AR4100(P) is architected for ultra-low power consumption, with near-zero power consumption in power down modes with fast wakeup.

2.2 Radio Front End

The AR4100(P) features a high-power high-efficiency on-chip power amplifier that features:

- Qualcomm Atheros proprietary EPA™ linearization technology for WiFi
- Highly integrated LNAs
- Integrated Balun for Tx and Rx paths
- Integrated Rx and Tx RF matching and switching to enable direct antenna connection with high performance, low power consumption, and near-zero RBOM for lowest solution cost

2.3 Power Management

The AR4100(P) requires both 3.3 V and 1.8 V supplies from the system. The AR4100(P) 3.3 V inputs support operating voltage from 4.2 V down to 3.1 V and is tolerant of momentary overvoltage up to 5.5 V. The AR4100(P) power management engine uses advanced power save techniques such as: gating clocks to idle or inactive blocks, voltage scaling to specific blocks in certain states, fast start and settling circuits to reduce Tx and active duty cycles, CPU frequency scaling, and other techniques to optimize power consumption across all operation states.

For applications with a small Tx duty cycle, the AR4100(P) has the ability to quickly wake up and burst data out at a high rate and go back into standby mode, thus taking advantage of the 5 μ A of power consumption in standby mode.

Additionally, Qualcomm Atheros can provide system level design recommendation to take the AR4100 standby current to essentially zero with the use of a high impedance FET.

2.4 Manufacturing Calibration

The AR4100(P) uses internal self-calibration and BIST (built-in self test) circuits to maintain optimal performance over temperature, time and process variation. The AR4100(P) is delivered fully tested and does not require any customer manufacturing line calibration.

2.5 Internal One-Time Programmable Memory

The AR4100(P) includes internal one-time programmable memory which may be used to store the device MAC address. This OTP memory must be programmed during the customer manufacturing flow with a MAC address and additional device information.

2.6 Reference Frequency

The AR4100(P) incorporates an integrated 26-MHz crystal

2.7 Internal Sleep Clock

The AR4100(P) incorporates integrated on-chip low power sleep clocks to regulate internal timing, eliminating the need for any external 32 KHz real time clocks or crystal oscillators.

2.8 Interfaces

The AR4100(P) supports a variety of interfaces for supporting host interface options, and external memory interface options.

- Standard Host Interface
The AR4100(P) supports a generic SPI (GSPI) slave port when interfacing to a host MCU.
- Firmware Loading and Other Interfaces
GSPI master for interfacing to an external NVMEM for firmware load into the AR4100(P) upon powerup

2.9 802.11n

The AR4100(P) incorporates the latest generation of 802.11n technology from Qualcomm Atheros. The AR4100(P) is 802.11n compliant and features frame aggregation, reduced inter-frame spacing (RIFS) and half guard intervals for improved throughput and space time block codes (STBC) on downlink receptions and low density parity check (LDPC) codes on uplink transmissions for improved robustness over range. [Table 2-1](#) shows 802.11n (PHY layer) throughput at different modulations.

Table 2-1 802.11n (PHY layer) Throughput at Different Modulations

MCS	Modulation	Data Rate (Mbps) 20 MHz Bandwidth	
		Full Guard Interval	Half Guard Interval
0	BPSK	6.5	7.2
1	QPSK	13.0	14.4
2	QPSK	19.5	21.7
3	16-QAM	26.0	29.9
4	16-QAM	39.0	43.3
5	64-QAM	52.0	57.8
6	64-QAM	58.5	65.0
7	64-QAM	65.0	72.2

The AR4100(P) features hardware-based AES, AES-CCMP, and TKIP engines for faster data encryption, and supports industry leading security features including WPS 2.0, along with standard WEP/WPA/WPA2 for personal environments.

2.10 Host Offloading (WiFi)

The AR4100(P) integrates extensive hardware signal processing and an embedded on-chip CPU to offload complete 802.11n MAC/Baseband/PHY processing to minimize host processor loading. The AR4100(P) offloads the complete 802.11b/g/n baseband and MAC functions as a standard feature, including:

- Link maintenance
- 802.11 frame transmission sequence to initiate the connection with an AP
- Background scanning, including transmission of probe requests
- Signal quality detection and automated maintenance of current AP list
- Roaming to a new AP
- Rate adaptation, including automatic retry
- Encapsulation of 802.3 frames from the host to 802.11 frames
- Decapsulation of the 802.11 frames to 802.3 frames
- Encryption & decryption (hardware ciphers) for WEP/TKIP/AES-CCMP
- IEEE PowerSave; periodic wakeup while in sleep mode to check for buffered traffic
- Security negotiation
- Wireless protected setup (WPS) 2.0
- WPS registrar
- SoftAP

2.11 AR4100P IP Offloading

The AR4100P SIP includes a TCP/IP and UDP offload capability. This capability can reduce Flash requirements on a host MCU by up to 100 KBytes and also free up CPU cycles. The IP stack is a simultaneous IPv4/IPv6 stack with a BSD-like interface to simplify porting and integration with common embedded operating systems. The supported features of the AR4100P stack (support for DHCP, multicast, and ARP) include:

- ARP
- Fragmentation/reassembly (supported with limitation)
- IPv4/IPv6 header processing
- UDP/TCP socket support
- DHCP v4 client and server
- Neighbor discovery
- Router advertisement
- Broadcast/multicast
- Address auto-configuration
- Multicast
- TCP zero-copy feature

The AR4100P supports many key IPv4 and IPv6 RFCs as shown in [Table 2-2](#) and [Table 2-3](#).

Table 2-2 AR4100P IPv4 Supported RFCs

IPv4 RFC Number
RFC1122: (TCP Timeout/Retransmission)
RFC1122: TCP Zero-Window-Probe
RFC1122: TCP Sliding Window Protocol

Table 2-3 AR4100P IPv6 Supported RFCs

IPv6 RFC Number
RFC-2464: Transmission of IPv6 packets over Ethernet networks
RFC-2460: Internet Protocol version 6
RFC2462: Duplicate Address Detection (DAD)
RFC-2463: ICMPv6
RFC3513: IP Version 6 Addressing Architecture
RFC3484: Default Address Selection
RFC2461: Neighbor Discovery for IPv6 host
RFC4862: Stateless Address Auto-configuration

3 WiFi Functional Description

3.1 Overview

The AR4100(P) is a single chip 802.11 b/g/n device optimized for low power embedded applications. The data path consists of the host interface, mailbox DMA, AHB, memory controller, MAC, BB, and radio. The CPU drives the control path via register and memory accesses.

3.2 XTENSA CPU

At the heart of the chip is the XTENSA CPU. The CPU has these interfaces:

- Code RAM/ROM interface (iBus), going to the virtual memory controller (VMC)
- Data RAM interface (dBus), going to the VMC

3.3 Reset Control

The AR4100(P) CHIP_PWD_L pin can be used to completely reset the entire chip. After this signal has been de-asserted, the AR4100(P) waits for host communication. Until then, the MAC, BB, and SOC blocks are powered off and all modules except the host interface are held in reset.

Once the host has initiated communication, the AR4100(P) turns on its crystal and later on its PLL. After all clocks are stable and running, the resets to all blocks are automatically de-asserted. The only resets that stay asserted are:

- Warm and cold resets to the MAC
- Warm reset to the radio (The cold reset gets automatically de-asserted)

The above resets are deasserted by software. All AR4100(P) reset control logic resides in the RTC block to ensure stable reset generation.

3.3.1 CPU Reset

CPU reset is different from the other resets mentioned above. There are four scenarios where the CPU reset can be asserted:

1. The CHIP_PWD_L pin is asserted or the host has not initiated communication.
2. The polarity of certain package pins are set to enable JTAG debugging via an In-Circuit Emulator (ICE). In this case, the external ICE can assert CPU reset through a package pin.
3. The polarity of a package pin is set to hold the CPU in reset until the host clears an internal AR4100(P) register.
4. An internal AR4100(P) register is set by the host to force the CPU out of an unknown state.

3.3.2 Reset Sequence

After a COLD_RESET event (e.g., host deasserts AR4100_CHIP_PWD_L) the AR4100 enters the HOST_OFF state. From that point the reset sequence is as shown:

1. The host writes the enable bit in the SPI_CONFIG register via the GSPI.
2. This bring the chip to a WAKEUP transient state from where it goes to an ON state (after the PLL clock has stabilized).
3. The ROM code executes the HOST_PROXY, which waits for the host to indicate whether to continue loading and executing firmware or whether to enter a boot message interface (BMI) state. The former is the normal mode; BMI is typically used to continue the host driving the AR4100 via BMI messages. BMI allows loading alternate firmware images into the RAM (e.g., to update the firmware in NVMEM, or run alternate firmware images for special tests).
4. If the host writes a special memory location (variable) to indicate that the firmware is to continue being loaded from host, then it does so and executes the loaded firmware. It eventually sends a WMIREADY event to the host
5. The host can now send further WMI commands.

3.4 Power Transition

The AR4100(P) provides integrated power management and control functions and extremely low power operation for maximum battery life across all operational states by:

- Gating clocks for logic when not needed
- Shutting down unneeded high speed clock sources
- Reducing voltage levels to specific blocks in some states

When the AR4100(P) is in a low power state, the main 1.2 V regulator for digital circuits (DREG) is turned off. All digital circuits that normally rely upon 1.2 V power from DREG are switched to use power from the smaller SREG regulator using a “Make-and-Break” mechanism.

3.4.1 Hardware Power States

AR4100(P) hardware has five top-level hardware power states managed by the RTC block.

[Table 3-1](#) describes the power states.

3.4.2 Sleep State Management

Sleep state minimizes power consumption while saving system states. In SLEEP state, all high speed clocks are gated off and the external reference clock source is powered off. The PAREG supplies are also turned off during SLEEP. For the AR4100(P) to enter SLEEP state, the MAC, and CPU systems must not be active.

The system remains in sleep state until a WAKEUP event causes the system to enter WAKEUP state, wait for the reference clock source to stabilize, and then ungate all enabled clock trees. The CPU wakes up only when an interrupt arrives, which may have also generated the system WAKEUP event.

Figure 3-1 depicts the state transition diagram.

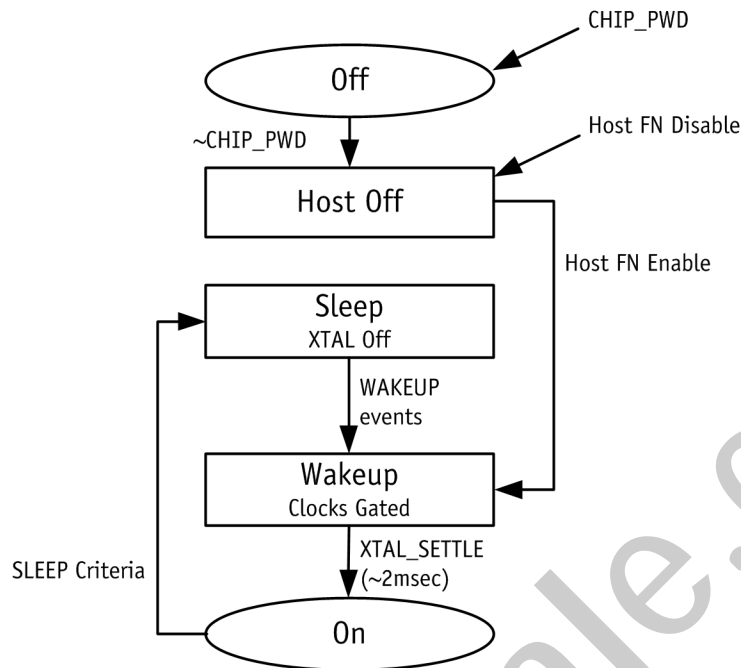


Figure 3-1 AR4100(P) Power States

Table 3-1 Power Management States

State	Description
OFF	CHIP_PWD_L pin assertion immediately brings the chip to this state.
	Sleep clock is disabled.
	No state is preserved.
	Host power LDO turned OFF.
HOST_OFF	WLAN is turned OFF.
	Only the host interface is powered on - the rest of the chip is power gated OFF.
	The host instructs the AR4100(P) to transition to WAKEUP by writing a register in the host interface domain.
	Embedded CPU and WLAN do not retain state (separate entry).
	This state can be bypassed by asserting FORCE_HOST_ON_L during CHIP_PWD_L deassertion.
SLEEP	Only the sleep clock is operating.
	The reference clock is disabled.
	Any wakeup events (MAC, host, LF-Timer, GPIO-interrupt) will force a transition from this state to the WAKEUP state.
	All internal states are maintained.
WAKEUP	The system transitions from sleep states to ON.
ON	The high speed clock is operational and sent to each block enabled by the clock control register.
	Lower level clock gating is implemented at the block level, including the CPU, which can be gated OFF using the WAITI instruction while the system is ON. No CPU, host, and WLAN activities will transition to sleep states.

3.5 System Clocking (RTC Block)

The AR4100(P) has an RTC block which controls the clocks and power going to other internal modules. Its inputs consist of sleep requests from these modules and its outputs consists of clock enable and power signals which are used to gate the clocks going to these modules. The RTC block also manages resets going to other modules with the device. The AR4100(P)'s clocking is grouped into two types: high-speed and low-speed.

3.5.1 High Speed Clocking

The reference clock source drives the PLL and RF synthesizer within the AR4100(P). To minimize power consumption, the reference clock source is powered off in the SLEEP, HOST_OFF, and OFF states.

When exiting SLEEP state, the AR4100(P) waits in WAKEUP state for a programmable duration.

3.5.2 Low-Speed Clocking

The AR4100(P) has eliminated the need for an external sleep clock source thereby reducing system cost. Instead, an internal ring oscillator is used to generate a low frequency sleep clock. It is also used to run the state machines and counters inside the AR4100(P)'s power control module (PCM). The PCM controls all power and isolation control signals for the entire chip.

The AR4100(P) has an internal calibration module which produces a 32.768 KHz output with minimal variation. For this, it uses the reference clock source as the golden clock. As a result, the calibration module adjusts for process and temperature variations in the ring oscillator when the system is in ON state.

3.5.3 Interface Clock

The host interface clock is another clock domain for the AR4100(P). This clock comes from the GSPI host and is completely independent from the other internal clocks. It drives the host interface logic as well as certain registers that can be accessed by the host in HOST_OFF and SLEEP states.

3.6 MAC/BB/RF Block

The AR4100(P) Wireless MAC consists of five major blocks:

- Host interface unit (HIU) for bridging to the AHB for VMC data accesses and APB for register accesses
- Ten queue control units (QCU) for transferring Tx data
- Ten DCF control units (DCU) for managing channel access
- Protocol control unit (PCU) for interfacing to baseband
- DMA receive unit (DRU) for transferring Rx data

3.7 Baseband Block

The AR4100(P) baseband module (BB) is the physical layer controller for the 802.11 b/g/n air interface. It is responsible for modulating data packets in the transmit direction, and detecting and demodulating data packets in the receive direction. It has a direct control interface to the radio to enable hardware to adjust analog gains and modes dynamically.

4 Electrical Characteristics

4.1 Absolute Maximum Ratings

Table 4-1 summarizes the absolute maximum ratings and Table 4-2 lists the recommended operating conditions for the AR4100(P). Absolute maximum ratings are those values beyond which damage to the device can occur.

Functional operation under these conditions, or at any other condition beyond those indicated in the operational sections of this document, is not recommended.

NOTE Maximum rating for signals follows the supply domain of the signals.

Table 4-1 Absolute Maximum Ratings

Symbol (Domain)	Parameter	Max Rating	Unit
AVDD18	Analog 1.8 V Supply	-0.3 to 2.5	V
VDDIO	GPIO I/O Supply	-0.3 to 4.0	V
HOST_POWER	Host Interface I/O Supply	-0.3 to 4.0	V
VDD33	Antenna and PA 3.3 V Supply	-0.3 to 4.0	V
PAREG_BASE	External 3.3 V Supply	-0.3 to 4.0	V
VBAT_42	External 3.3 V Supply	-0.3 to 4.8	V
RF _{in}	Maximum RF Input (Reference to 50-Ω input)	+12 (Including Switch and Balun Loss)	dBm
T _{store}	Storage Temperature	-45 to 135	°C
ESD	Electrostatic Discharge Tolerance	2000	V

4.2 Recommended Operating Conditions

Table 4-2 Recommended Operating Conditions

Symbol (Domain)	Parameter	Min	Typ	Max	Unit
AVDD18	Analog 1.8 V Supply	1.71	1.8	1.89	V
VDDIO	GPIO I/O Supply	1.71	—	3.46	V
HOST_POWER	Host interface I/O Supply	1.71	—	3.46	V
VDD33_PA	Antenna and PA 3.3 V Supply	3.14	—	3.46	V
PAREG_BASE	External 3.3 V Supply	3.14	3.3	3.46	V
VBAT_42	External 3.3 V Supply	3.14	3.3	3.46	V
T _{ambient}	Ambient Temperature	-30	—	85	°C

4.3 DC Electrical Characteristics

Table 4-3 and Table 4-4 list the general DC electrical characteristics over recommended operating conditions (unless otherwise specified).

Table 4-3 General DC Electrical Characteristics (For 3.3 V I/O Operation)

Symbol	Parameter		Conditions	Min	Typ	Max	Unit
V_{IH}	High Level Input Voltage		—	$0.7 \times V_{dd}$	—	—	V
V_{IL}	Low Level Input Voltage		—	—	—	$0.3 \times V_{dd}$	V
I_{IL}	Input Leakage Current	Without Pull-Up or Pull-Down	$0\text{ V} < V_{in} < V_{dd}$ $0\text{ V} < V_{out} < V_{dd}$	0	—	-3	nA
		With Pull-Up	$0\text{ V} < V_{in} < V_{dd}$ $0\text{ V} < V_{out} < V_{dd}$	16	—	48	μA
		With Pull-Down	$0\text{ V} < V_{in} < V_{dd}$ $0\text{ V} < V_{out} < V_{dd}$	-14	—	-47	μA
V_{OH}	High Level Output Voltage		$I_{oh} = -4\text{ mA}$	$0.9 \times V_{dd}$	—	—	V
			$I_{oh} = -12\text{ mA}$	$0.9 \times V_{dd}$	—	—	V
V_{OL}	Low Level Output Voltage		$I_{oh} = 4\text{ mA}$	—	—	$0.1 \times V_{dd}$	V
			$I_{oh} = 12\text{ mA}$	—	—	$0.1 \times V_{dd}$	V

Table 4-4 General DC Electrical Characteristics (For 1.8 V I/O Operation)

Symbol	Parameter		Conditions	Min	Typ	Max	Unit
V_{IH}	High Level Input Voltage		—	$0.7 \times V_{dd}$	—	—	V
V_{IL}	Low Level Input Voltage		—	—	—	$0.3 \times V_{dd}$	V
I_{IL}	Input Leakage Current	Without Pull-Up or Pull-Down	$0\text{ V} < V_{in} < V_{dd}$ $0\text{ V} < V_{out} < V_{dd}$	0	—	-3	nA
		With Pull-Up	$0\text{ V} < V_{in} < V_{dd}$ $0\text{ V} < V_{out} < V_{dd}$	3.5	—	13	μA
		With Pull-Down	$0\text{ V} < V_{in} < V_{dd}$ $0\text{ V} < V_{out} < V_{dd}$	-6.2	—	-23	μA
V_{OH}	High Level Output Voltage		$I_{oh} = -4\text{ mA}$	$0.9 \times V_{dd}$	—	—	V
			$I_{oh} = -12\text{ mA}$	$0.9 \times V_{dd}$	—	—	V
V_{OL}	Low Level Output Voltage		$I_{oh} = 4\text{ mA}$	—	—	$0.1 \times V_{dd}$	V
			$I_{oh} = 12\text{ mA}$	—	—	$0.1 \times V_{dd}$	V

Figure 4-1 and Figure 4-2 show the recommended power up/down and reset sequences for the AR4100(P) using external 3.3 V and 1.8 V supplies.

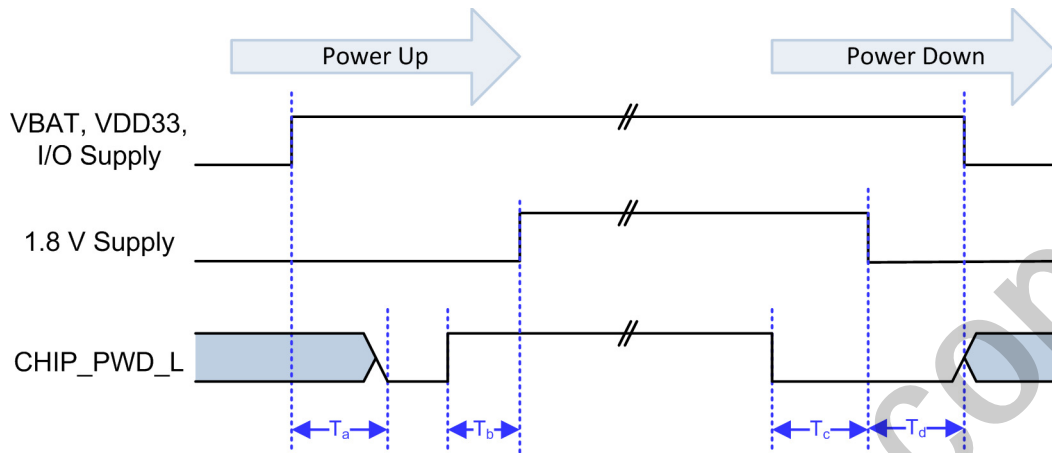


Figure 4-1 Power Up/Power Down Timing

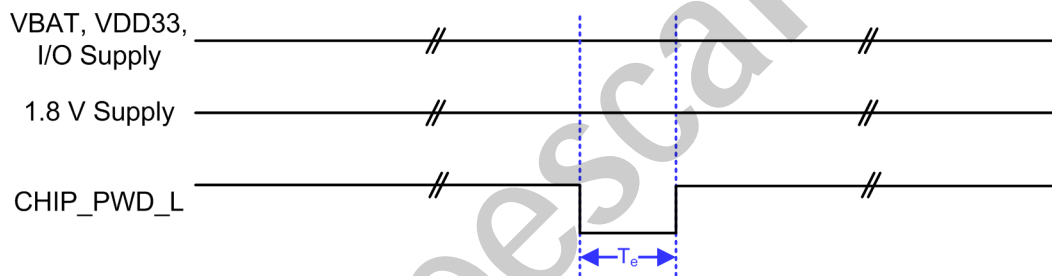


Figure 4-2 Reset and Power Cycle Timing

Where:

- VBAT = VBATT_42
- I/O = VDDIO, HOST_POWER

Table 4-5 Reset and Power Cycle Timing

Variable	Description	Min (μ sec)	Max (μ sec)
T_a	Time between VBAT, VDD33 and I/O supplies becoming valid and 1.8 V supply becoming valid ¹	0	—
T_b	Time between the 1.8 V becoming valid and the CHIP_PWD_L deassertion	0	500
T_c	Time between the CHIP_PWD_L assertion and the 1.8 VG supply becoming invalid	0	—
T_d	Time between the 1.8 V supply becoming invalid and VBAT, VDD33 and I/O supplies becoming invalid	N/A ²	—
T_e	Length of the CHIP_PWD_L pulse	5	—

1. "Supply becoming valid" denotes that the voltage level has reached 90%

2. No strict requirements. This parameter can also be negative.

4.4 Radio Receiver Characteristics

Table 4-6 summarizes the AR4100(P) receiver characteristics.

Table 4-6 Receiver Characteristics for 2.4 GHz Operation

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
F _{RX}	Receive Input Frequency Range	—	2.412	—	2.484	GHz
S _{rf}	Sensitivity					
	CCK	—	—	-95	—	dBm
	OFDM	—	—	-92	—	
	HT20	—	—	-92	—	

4.5 Radio Transmitter Characteristics

Table 4-7 summarizes the transmitter characteristics for the AR4100(P).

NOTE All transmitter characteristics are preliminary and to subject to change without notice.

Table 4-7 Transmitter Characteristics for 2.4 GHz Operation

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
F _{TX}	Transmit Output Frequency Range	—	2.412	—	2.484	GHz
P _{out}	802.11b Mask Compliant	1 Mbps	—	18.5	—	dBm
	802.11g Mask Compliant	6 Mbps	—	19	—	
	802.11n HT20 Mask Compliant	MCS0	—	18.5	—	
A _{pl}	Accuracy of Power Leveling Loop	—	—	±1.5	—	dB

4.6 Typical Current Consumption Performance

Table 4-8 summarizes the low power state current consumption for the AR4100(P).

Table 4-8 Typical Current Consumption: Low Power States (Individual Voltage Rails)

Mode		Typical Current Consumption (mA)	
		1.8 V ²	3.3 V ³
Standby	OFF	0.000	0.004
	HOST_OFF	0.043	0.005
	SLEEP	0.210	0.005
IEEE PS ¹ (2.4 GHz)	DTIM=1	2.011	0.005
	DTIM=3	0.868	0.005
	DTIM=10	0.467	0.005

1. Calculated assuming Rx time of 2ms + 0.1 * DTIM
2. AVDD18, VDDIO
3. PAREG_BASE, VBAT_42, VDD33

4.6.1 Current Consumption for Continuous Receive

Table 4-9 shows the current consumption for continuous Rx.

Table 4-9 Current Consumption for Continuous Rx

Mode/Rate [Mbps]	Typical Current Consumption (mA)		
	1.8 V ¹	3.3 V ²	I/O ³
CCK, 1 Mbps	81	0	5
CCK, 11 Mbps	82	0	5
OFDM, 6 Mbps	83	0	5
OFDM, 54 Mbps	85	0	5
HT20, MCS0	84	0	5
HT20, MCS7	86	0	5

1. AVDD18
2. PAREG_BASE, VBAT_42, VDD33
3. VDDIO

4.6.2 Current Consumption for Continuous Transmit

Table 4-10 shows the current consumption for continuous Tx.

Table 4-10 Current Consumption for Continuous Tx

Mode/Rate [Mbps]	Target Output Power (dBm)	Typical Current Consumption [mA]		
		1.8 V ¹	3.3 V ²	I/O ³
CCK, 1 Mbps	17	59	231	5
CCK, 11 Mbps	17	59	228	5
OFDM, 6 Mbps	17	66	204	5
OFDM, 54 Mbps	17	64	151	5

1. AVDD18
2. PAREG_BASE, VBAT_42, VDD33
3. VDDIO

4.6.3 Measurement Conditions for Current Consumption Parameters

- $T_{\text{ambient}} = 25\text{ }^{\circ}\text{C}$
- All I/O pins except for CHIP_PWD_L are maintained at their default polarities (I/Os without default internal pulls are pulled low)

5 Pin Assignments and Descriptions

Table 5-1 shows the PCB footprint and pin assignments (bottom view of the chip) of the AR4100(P).

Table 5-2 and Table 5-3 show pin assignments and pin definitions.

The following nomenclature is used for signal names:

- NC No connection should be made to this pin
- _L At the end of the signal name, indicates active low signals
- P At the end of the signal name, indicates the positive side of a differential signal
- N At the end of the signal name indicates the negative side of a differential signal

The following nomenclature is used for signal types:

- IA Analog input signal
- I Digital input signal
- IH Input signals with weak internal pull-up, to prevent signals from floating when left open
- IL Input signals with weak internal pull-down, to prevent signals from floating when left open
- I/O A digital bidirectional signal
- OA An analog output signal
- O A digital output signal
- P A power or ground signal

Table 5-1 AR4100 Pin Assignment and Ball-Out

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	
A	GND	AVDD18	AVDD18	VDDIO	SW_ REG_OUT	VDD33	VBAT_42	PAREG_ 33_OUT	PAREG_ _BASE	DVDD12	GND	NC	NC	NC	NC	NC	NC	
B	AVDD12	NC	NC	NC	SW_ REG_OUT	VDD33	VBAT_42	PAREG_ 33_OUT	NC	NC	NC	NC	NC	NC	NC	NC	NC	SPIM_WP
C	HOST_ POWER	NC														NC	SPIM_ HOLD	
D	SPI_MOSI	NC														NC	NC	
E	SPI_CS	NC														NC	GND	
F	NC	NC														NC	NC	
G	SPI_INT														LF_CLKIN	NC		
H	SPI_MISO														NC	NC		
J	SPI_CLK														NC	NC		
K	GND														NC	NC		
L	NC														NC	NC		
M	NC	SPIM_CS_L														NC	NC	
N	NC	SPIM_MISO														NC	NC	
P	NC	SPIM_CLK														NC	NC	
R	NC	SPIM_MOSI	NC	NC	NC	NC	HMODE1	NC	TDI	NC	NC	NC	NC	NC	NC	NC	NC	GND
T	NC	NC	GND	WIFI_ RF	GND	TDO/ UART_TXD	HMODE0	TMS	TCK	UART_ RXD	CHIP_ PWD_L	GND	NC	GND	NC	GND	NC	

E_ GND1	E_ GND2	E_ _GND3	E_ GND4	E_ GND5	E_ GND6
E_ GND7	E_ GND8	E_ GND9	E_ GND10	E_ GND11	E_ GND12
E_ GND13	E_ GND14	E_ GND15	E_ GND16	E_ GND17	E_ GND18
E_ GND19	E_ GND20	E_ GND21	E_ GND22	E_ GND23	E_ GND24
E_ GND25	E_ GND26	E_ GND27	E_ GND28	E_ GND29	E_ GND30
E_ GND31	E_ GND32	E_ GND33	E_ GND34	E_ GND35	E_ GND36

(Note: the 36 E_GND* pins are not aligned with the outer pins.
See "Package Dimensions" on page 26.)

Table 5-2 AR4100(P) Pin Assignments and Descriptions

Pin Number	Pin Name	Pin Number	Pin Name	Pin Number	Pin Name
A1	GND	D16	NC	R4	NC
A2	AVDD18	D17	NC	R5	NC
A3	AVDD18	E1	SPI_CS	R6	NC
A4	VDDIO	E2	NC	R7	HMODE1
A5	SW_REG_OUT	E16	NC	R8	NC
A6	VDD33	E17	GND	R9	TDI
A7	VBAT_42	F1	NC	R10	NC
A8	PAREG_33_OUT	F2	NC	R11	NC
A9	PAREG_BASE	F16	NC	R12	NC
A10	DVDD12	F17	NC	R13	NC
A11	GND	G1	SPI_INT	R14	NC
A12	NC	G16	LF_CLKIN	R15	NC
A13	NC	G17	NC	R16	NC
A14	NC	H1	SPI_MISO	R17	GND
A15	NC	H16	NC	T1	NC
A16	NC	H17	NC	T2	NC
A17	NC	J1	SPI_CLK	T3	GND
B1	AVDD12	J16	NC	T4	WIFI_RF
B2	NC	J17	NC	T5	GND
B3	NC	K1	GND	T6	TDO/UART_TXD
B4	NC	K16	NC	T7	HMODE0
B5	SW_REG_OUT	K17	NC	T8	TMS
B6	VDD33	L1	NC	T9	TCK
B7	VBAT_42	L16	NC	T10	UART_RXD
B8	PAREG_33_OUT	L17	NC	T11	CHIP_PWD_L
B9	NC	M1	NC	T12	GND
B10	NC	M2	SPIM_CS_L	T13	NC
B11	NC	M16	NC	T14	GND
B12	NC	M17	NC	T15	NC
B13	NC	N1	NC	T16	GND
B14	NC	N2	SPIM_MISO	T17	NC
B15	NC	N16	NC	F6, F7, F8, F9, F10, F11, G6, G7, G8, G9, G10, G11, H6, H7, H8, H9, H10, H11, J6, J7, J8, J9, J10, J11, K6, K7, K8, K9, K10, K11, L6, L7, L8, L9, L10, L11	E-GND 1...36 (Note that these pins are not aligned to the outer pins. See "Package Dimensions" on page 26.)
B16	NC	N17	NC		
B17	SPIM_WP	P1	NC		
C1	HOST_POWER	P2	SPIM_CLK		
C2	NC	P16	NC		
C16	NC	P17	NC		
C17	SPIM_HOLD	R1	NC		
D1	SPI_MOSI	R2	SPIM_MOSI		
D2	NC	R3	NC		

Table 5-3 Signal-to-Pin Relationships and Descriptions

Signal Name	Pin	Type	Reset State	I/O Pad Supply Domain	Description	
Digital Control						
HMODE0	T7	I	—	VDDIO	WiFi host mode select, see design guide for configuration details, floating input must be tied high or low.	
HMODE1	R7	I	—	VDDIO	WiFi host mode select, see design guide for configuration details, floating input must be tied high or low.	
CHIP_PWD_L	T11	I, PD	Low	HOST_POWER	WLAN Power Down	
					0	Power down
					1	WLAN awake
Host Interface (SPI Mode)						
SPI_MOSI	D1	I/O	PU	HOST_POWER	SPI data Input	
SPI_CLK	J1	I	—	HOST_POWER	SPI clock must be driven.	
SPI_MISO	H1	I/O	PU	HOST_POWER	SPI data output	
SPI_INT	G1	I/O	PU	HOST_POWER	SPI interrupt	
SPI_CS	E1	I/O	PU	HOST_POWER	SPI chip select	
Master SPI Flash Interface						
SPIM_CLK	P2	I/O	—	VDDIO	Master SPI clock for SPI flash interface	
SPIM_CS_L	M2	I/O	High	VDDIO	Master SPI chip select for SPI flash interface	
SPIM_HOLD	C17	I/O	—	VDDIO	Allows pausing of SPI Flash operation. Held high in legacy SPI flash operation; in Quad Mode this pin functions as IO3, increasing the data rate in RDWR burst operations.	
SPIM_MISO	N2	I/O	High	VDDIO	Master SPI data input for SPI flash interface	
SPIM_MOSI	R2	I/O	—	VDDIO	Master SPI data output for SPI flash interface	
SPIM_WP	B17	I/O	—	VDDIO	Allows users to protect the SPI flash content when held low. In legacy SPI flash operation this pin is in pull up mode; in Quad Mode this pin functions as IO2, increasing the data rate in RDWR burst operations.	
RF Port						
WIFI_RF	T4	A_I/O	—	—	RF antenna port	
System Test						
LF_CLKIN	G16	I/O	—	VDDIO	The AR4100(P) uses an internal low frequency sleep clock. Designers must ground the LF_CLKIN.	
TMS	T8	I, PU	High	VDDIO	WiFi JTAG TMS; Used with debugging only	
TCK	T9	I, PU	High	VDDIO	WiFi JTAG TCK; Used with debugging only	
TDI	R9	I, PU	High	VDDIO	WiFi JTAG TDI Used with debugging only	
TDO	T6	I, PU	High	VDDIO	WiFi JTAG TDO; Used with debugging only	
UART_RXD	T10	I/O	Low	VDDIO	Reconfigured after software download as debugging UART RXD	
UART_TXD	T6	O	High	VDDIO	Reconfigured after software download as debugging UART TXD	

Table 5-4 Signal-to-Pin Relationships and Descriptions

Signal Name	Pin	Type	Description
Power Supply			
GND	A1, A11, E17, K1, R17, T3, T5, T12, T14, T16	P	All ground pins must be grounded, follow design note recommendations.
E-GND 1...36	F6, F7, F8, F9, F10, F11, G6, G7, G8, G9, G10, G11, H6, H7, H8, H9, H10, H11, J6, J7, J8, J9, J10, J11, K6, K7, K8, K9, K10, K11, L6, L7, L8, L9, L10, L11	P	Ground pads at center of package, all 36 must be connected to the ground plane with sufficient vias, follow design note recommendations. (Note that these pins are not aligned to the outer pins. See "Package Dimensions" on page 26.)
AVDD18	A2, A3	P	Power supply input; Wi-Fi 1.8 V digital, RF, baseband, and synthesizer supplies.
VDDIO	A4	P	Power supply input; Wi-Fi digital IO supply for XTAL oscillator.
SW_REG_OUT	A5, B5	P	Leave unconnected
VDD33	A6, B6	P	Power supply input; Wi-Fi antenna and WiFi PA 3.3 V supplies.
VBAT_42	A7, B7	P	Power supply input; see design guide for details.
PAREG_33_OUT	A8, B8	P	Power supply; see design guide for details.
PAREG_BASE	A9	P	Power supply; see design guide for details.
DVDD12	A10	P	Power supply bypass; Wi-Fi digital 1.2 V supply from internal LDO, connect to external bypass capacitor.
AVDD12	B1	P	Power supply bypass; Wi-Fi analog 1.2 V supply from internal LDO, connect to external bypass capacitor.
HOST_POWER	C1	P	Power supply input; 1.8 V or 3.3 V Host IO power supply input
NC	A12, A13, A14, A15, A16, A17, B2, B3, B4, B9, B10, B11, B12, B13, B14, B15, B16, C2, C16, D2, D16, D17, E2, E16, F1, F2, F16, F17, G17, H16, H17, J16, J17, K16, K17, L1, L16, L17, M1, M16, M17, N1, N16, N17, P1, P16, P17, R1, R3, R4, R5, R6, R8, R10, R11, R12, R13, R14, R15, R16, T1, T2, T13, T15, T17	—	No connect

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6 Package Dimensions

Figure 6-1 and Figure 6-2 show the AR4100(P) package dimensions.

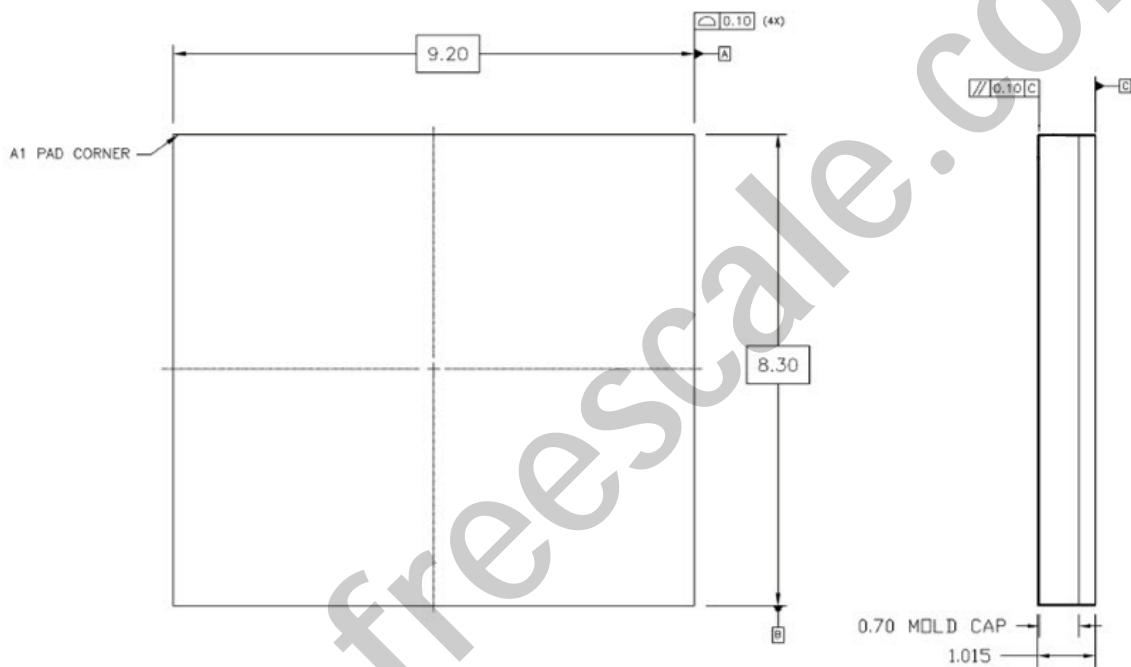


Figure 6-1 AR4100(P) Package Dimensions (Top and Side Views)

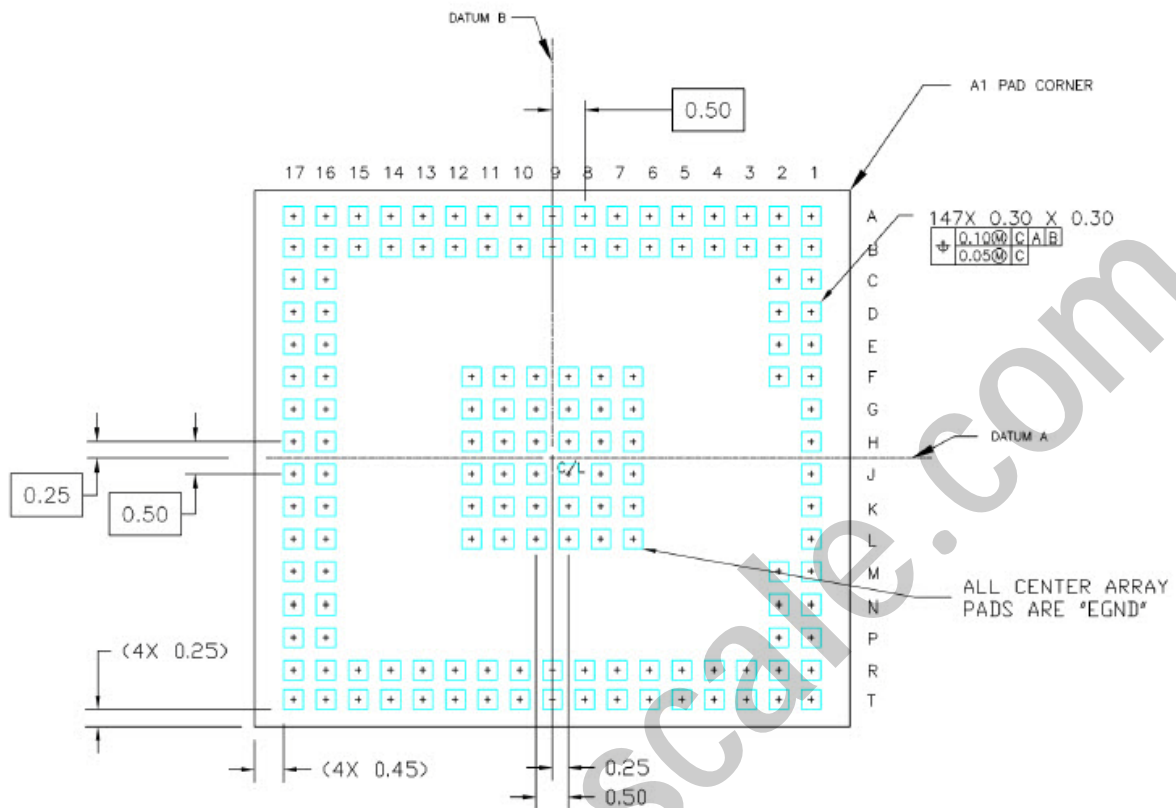


Figure 6-2 AR4100(P) Pin Assignments (Bottom View)

7 Assembly Guidelines

This section describes the assembly guidelines and solder material information.

Manufacturer Name	Kester
Solder Past Part Number	EM808-Sn96.5% Ag3.0% Cu0.5% SAC305 alloy with Type 3 powder, water soluble solder paste

8 Design Guidelines

8.1 Design Guidelines

See the *AR4100 Hardware Reference Guide* for detailed design guidelines.

8.2 Manufacturing Requirements

The AR4100(P) is fully calibrated during the manufacturing and testing process.

The AR4100(P) requires additional OTP programming during integration into end systems. More specifically, customers will need to program a MAC address into the AR4100(P).

9 Ordering Information

For more information on the AR4100 or other solutions from Qualcomm Atheros, contact your local representative:

Qualcomm Atheros, Inc.

t +1 408.773.5200

f +1 408.773.9940

Qualcomm Atheros, Inc. Hong Kong Limited

t +852 8206.1131

f +852 8206.1301

Qualcomm Atheros KK-Japan

t +81 3.5501.4100

f +81 3.5501.4129

Atheros (Shanghai) Co., Ltd.

t +86 21.5108.3626

f +86 21.5027.0100

Qualcomm Atheros Intl, LLC-Taiwan

t +886 2.8751.6385

f +886 2.8751.6397

Qualcomm Atheros Korea

t+82 31.786.0428

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